DESIGN AND FABRICATION OF 4H-SiC DETECTORS TOWARDS SINGLE PHOTON COUNTING

by

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ABSTRACT OF THE DISSERTATION

Design and Fabrication of 4H-SiC Detectors towards Single Photon Counting

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This thesis covers initiative works and innovative improvements in designing, fabricating and calibrating the world's first 4H-SiC single photon avalanche diodes (SPADs). In comparison to previous SiC APDs, the SiC SPADs have completely different targets. Major improvements are made in almost all aspects from wafer structure design, mask design, to characterizations. The robust and radiation-hard SiC SPADs, which are designed to replace the bulky PMTs and fragile Si SPADs, target at ultra high sensitive UV detection, towards the ultimate sensitivity—quantum limit. SiC SPADs can be widely used in missile and aircraft alarm system, none-line-of-sight (NLOS) and quantum communications, UV 3-D imaging, downhole exploration, as well as many NASA applications, such as low-earth orbit fluorescence observations.

The following areas are discussed in details in this thesis: wafer structure and mask design, a new bevel and MJTE edge termination technology for SiC SPADs, as well as improvements for an ultra low dark current, high quantum efficiency, and low dark count rate and high single photon detection efficiency. Future work is also proposed for further improving SiC SPADs.

The milestones in this thesis work include, the world's first SiC SPAD fabricated in 2004; the world's largest SiC SPAD (260μm×260μm) in 2004; a single photon counting measurement system with passive quenching circuit in 2004; a SiC SPAD with the highest gain (10^9) in 2005; a SiC SPAD with the lowest dark current (<4fA at 50% of breakdown voltage and <26fA at 95% of breakdown voltage) in 2007; the world's first SiC SAM SPAD with thick absorption layer, high quantum efficiency (~58%), and a significantly lower dark count rate than the first SiC SPAD in 2007; a new bevel edge termination technology; and a new p-type metal recipe leading to a low 10^{-4}~ low $10^{-5}\Omega cm^2$ specific contact resistance for p-type 4H-SiC with minimum consumption of SiC (<1500Å) in 2007.

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I. INTRODUCTION

1.1 Detection of High Energy Signals of Ultraviolet, Extreme Ultraviolet, X-ray and Nuclear Particles

The most widely used traditional light sensors include semiconductor detectors (typically Si and InP), and photo multiplication tubes (PMTs). They are used to detect objects which radiate or reflect visible and infrared signals. However, there are many other objects (even from outer space) which emit UV signals, cosmic rays, or nuclear radiation particles. These emissions are associated with combustions, explosions, cosmic rays, or high-energy nuclear particles. For example, UV is emitted from combustions emanating from rockets, missiles, aircrafts, utility power line failures, and high voltage switching. Cosmic particles also generate UV fluorescence in low-Earth orbit (1). Accelerators and cyclotrons produce high-energy radiation (UV, EUV, X-ray) and nuclear particles. Detection of these signals is very important to high-energy physics and to a host of other applications. Recently, traditional high power UV lamps are gradually replaced with the new, high efficient UV LEDs and UV lasers. As a result, the residential UV applications are rapidly growing, such as air and liquid cleaning and material curing. All these applications prefer visible-blind or solar-blind UV detectors. In theory traditional semiconductor detectors can be used for the signal detection of the high energy radiation since the signal energy is higher than their band gaps. However, in most cases the strong background visible and infrared lights give rise to extremely high noise levels and thus lead to lead to very poor signal to noise ratio. For example, the solar radiation at sea level covers a wide range from 290nm to infrared as shown in Fig. I-1. Moreover, the harsh environments (high radiation and extreme

temperatures) experienced by the detectors often reduce the lifetime of devices, causing damage or long-term reliability problem. The development of radiation-hard, highly sensitive detectors for high energy signals is very desirable. The issue of high sensitivity is especially important since the detectors often are located in hazardous environments where early detection is critical.

Since visible and infrared background noises are always strong, a short-pass filter has to be utilized with traditional radiation detectors to improve the signal to noise ratio. However, building a short-pass filter which blocks a wide spectrum from the visible to the infrared is technically difficult. Many short-pass filters are very costly and have poor transmittance for the interested band (<15%) (2). Another important application is non-line-of-sight (NLOS) UV communications and UV quantum communications (3) (4), where high background noise causes a very high bit error rate. For these applications, solar-blind detectors with high UV (or EUV and X-ray) to visible rejection ratio are highly sought after. The applications can be classified into two areas: at one end, which includes many space applications, a very large detection area and ultra low dark current are required, and speed is not critical (Class A); at the other end, which includes covert communication, high speed and high gain are required (Class B). And imaging capability is always a plus for both.

Technically, the Class A application is relatively easy to accomplish simply by resorting to SiC, and the author and collaborators have reported SiC (5) (6) that have,

(a) High quantum efficiency in a wide UV, EUV and X-ray spectrum.

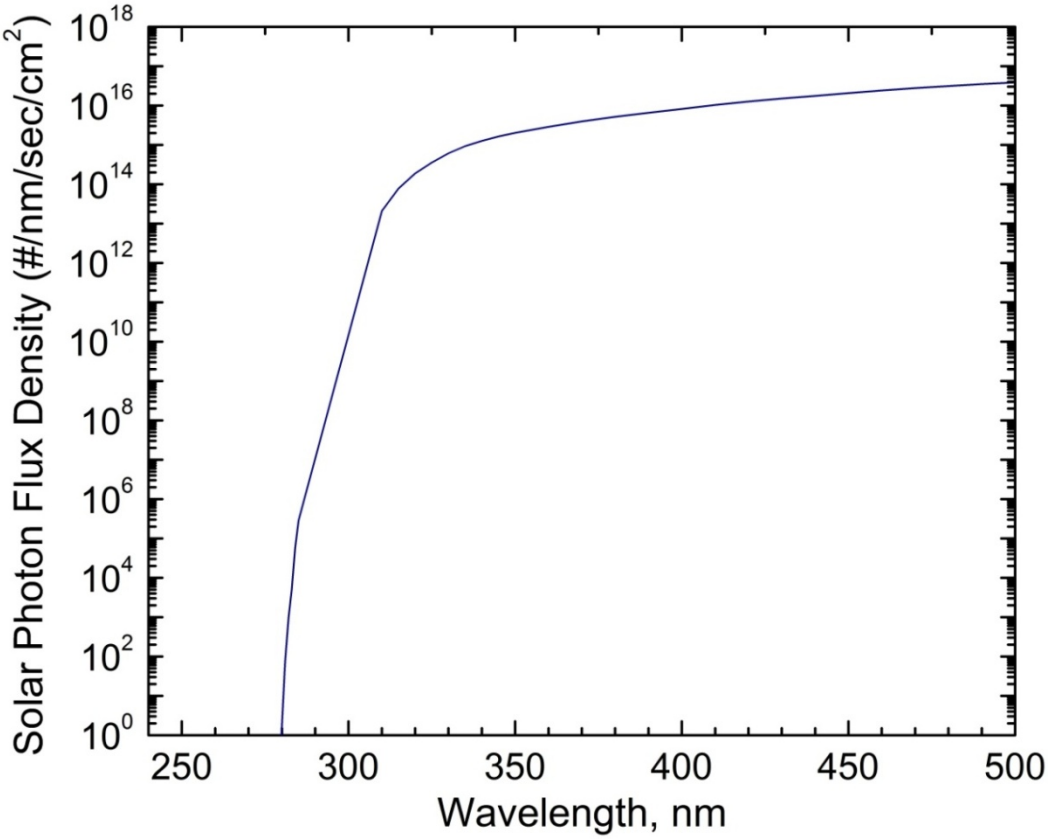


Fig. I-1 Solar radiation spectrum at sea level.

(b) A very large detection area up to 1cm×1cm (6), either in discrete format, or in array format.

(c) A very low dark current, typically below 10pA/cm^2 for some application which requires large detection area and <1fA/cm^2 noises at low voltages.

(d) High UV to visible rejection ratio, typically >10^3 or higher

(e) Radiation hardiness and excellent long-term reliability.

One of the most difficult issues for Type A detectors is its coverage in the EUV range. For each semiconductor material, there are some wavelengths between 100nm~300nm (Fig. I-2) where the absorption depth is extremely shallow (<50Å). A majority of the lights are absorbed in a region very close to the surface and are recombined there due to high surface defects density. In SiC, this problem has been addressed by applying a semitransparent Ni as the Schottky contact.

The Class B applications are challenging for device fabrications. It requires detectors to have,

(a) High speed for communication purpose, typically response speed should be in the order of 100MHz or higher.

(b) Proper spectrum coverage in UV, EUV, X-ray spectrum. As the high-energy signal is usually very weak, a discriminative spectrum coverage only favoring the interested range is required. For example, 280nm is the most interested wavelength for NLOS communications and time-of-flight applications. The Sun radiation after the atmosphere absorption typically becomes negligible for wavelength 290nm and shorter, and wavelength shorter than 270nm

usually propagates very limited length in air, leaving a narrow communication window around 280nm which can be used for UV communications.

(c) A very high gain larger than 10^6 for single photon counting purpose.

(d) Large detecting apeture size (up to $1cm^2$) if possible, with ultra low leakage current, and/or very low dark count rate, and/or very low noises.

(e) Imaging capabilities.

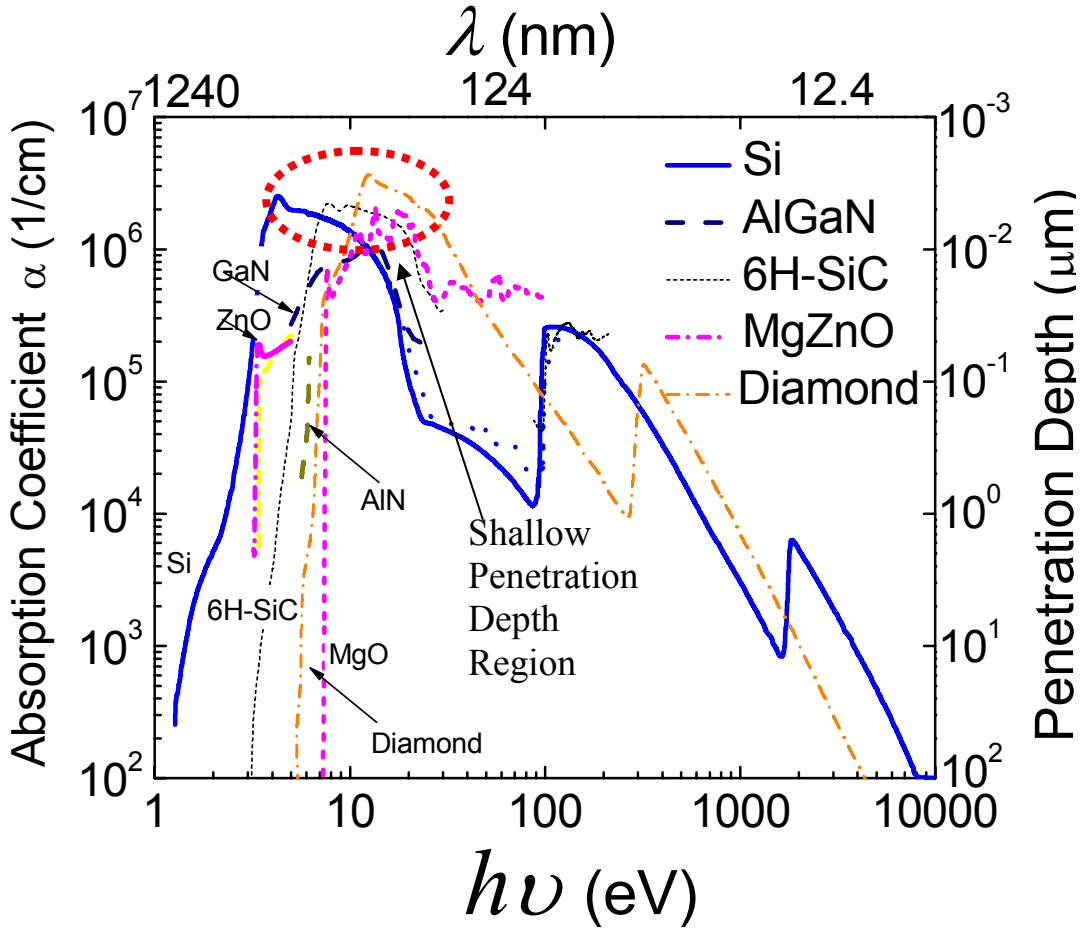


Fig. I-2 Penetration Depth of Silicon, SiC, GaN and some other related materials. Please notice that two extremes in penetration depth appear in the EUV and Soft X-ray range: a very shallow penetration depth <100A for 6H-SiC around 10eV, and very long penetration depth at high-energy end (tens of microns), which will be addressed later.

Many UV applications require very high sensitivity for weak signal detection. The signal flux for some NASA applications, for example, could be as low as one photon per minute for a large $1cm^2$ area. There are always applications which require higher sensitivity than the capability of current technology. Among all the semiconductor detectors for UV and X-ray detections, single photon counters based on avalanche photo diode structure have the best potential for ultra weak light detection. Before we start the discussion of SiC single photon counters, it needs to mention that SiC charge coupled devices (CCD) also meet most of the requirements for Type B applications, except speed. Limited by the material maturity and progressing technology for high quality 4H-SiC MOSFET and MOS capacitor, 4H-SiC CCD has not been developed. Our research on SiC MOSFETs in the last two years resolved many issues related to SiC CCD, including reducing the surface defects and improving the channel mobility; but still, 4H-SiC CCD has many challenging issues remaining, including how to ensure a high-quality SiC-SiO_2 interface towards a high charge transfer efficiency (CTE) higher than 99.9999%, restricting of carrier diffusion, long-term reliability related to interface degradation due to radiation and large temperature variations in space, etc. CCDs are usually slow, and cannot meet the critical speed requirement for communications and 3D-imaging applications.

For high-speed weak-signal optical applications, avalanche photo diodes have the best potential. Traditional APDs are operated in linear mode and are used for relatively strong light where the noise and dark current is negligible. However, when signal intensity is extremely weak, the noise in linear mode becomes not tolerable. Plus, the distribution of linear gain in an APD is not at all Gaussian. Instead, but characterized as McIntyre

distribution, which is heavily distorted in low gains and/or weak signals. Many Si APDs face problem of linearity and high noise floor level. In recent years, Si single photon avalanche diodes (SPADs) have been developed with excellent time resolution of <100psec, which leads to a special resolution of 2cm. However, when using Si SPADs for solar-blind UV applications, there are several fundamental problems: poor UV sensitivity due to shallow penetration depth around 280nm, poor radiation hardiness, very limited in size and the needs of short pass filter blocking a wide spectrum from 290nm to infrared. A SiC SPAD could solve these problems.

SiC APDs are first developed by SiCLAB at Rutgers by Dr. Feng Yan. These APDs are operated under linear mode, where the light is relatively strong and the noises due to dark current and multiplication fluctuation is negligible. In this thesis, we will discuss how to develop SiC SPADs which meet requirements of Class B applications. SPADs counts the individual pulse numbers regardless variations of multiplication amplitudes (to some extend of course) and many dark carriers from surface which are not fully multiplied could be discarded. Providing the ultimate sensitivity, single photon counter will approach the quantum limit, and enable many applications in astronomy (7), single molecule detection (8) (9) (10), VLSI testing (11), DNA sequencing for weak fluorescence detections (12) (13), etc. The sensitivity of the single photon counter can be further improved by applying external time correlated circuit since signals usually have coherence but dark counts do not (4) (14).

After providing the landscape of the high energy signal detections, we will review the excellent property of SiC to see why SiC is chosen for single photon and other UV applications.

1.2 Why SiC?

4H-SiC is widely acknowledged as a promising semiconductor material for power applications because of its wide band-gap, high breakdown electric field, high electron saturation velocity and high thermal conductivity. It is also discovered that 4H-SiC has superior advantages over Si and GaN or other III-nitrides for high energy signal detections.

(a) 4H-SiC has a wide indirect bandgap (3.26eV at 300K), which makes it an intrinsically visible-blind material and have very high UV to visible rejection ratio. This property makes SiC detectors having orders of magnitude less responsivity for visible and infrared background noises. Fig. I-3 shows the Quantum Efficiency (QE) of a SiC PiN detector by the author. The detector has a high QE around 300nm and a large UV to signal rejection ratio (>10^4). As a result, the detectors have very weak response to most of the solar radiation spectrum as shown in Fig. I-4. In comparison to Si detectors, it becomes much easier to make SiC detectors solar-blind if a short pass filter can be introduced to block the UV radiation only from 290nm to 400nm, while Si detectors require short pass filters blocking all the spectrum from 290nm to infrared.

(b) Because of its wide bandgap, SiC has ultra low thermal generation rate and very low intrinsic carrier density (10^{18} times lower than that in Si), which gives SiC detectors multiple advantages. It makes very low dark current and very large detector area possible. For CCD structures, the extremely low thermal generation enables very long integration time, high transfer efficiency and very low noise and will greatly increase the sensitivity of the CCD. For SPADs, potentially the SiC

dark count rate (DCR) could be orders of magnitude lower than that of Si. Also it makes SiC single photon counter capable of operating in a wide temperature range.

(c) 4H-SiC happens to have a proper penetration depth in the most interested solar-blind wavelength (~1μm @270nm, Fig. I-5) in the UV range (15), which is very important for semiconductor fabrication. In comparison, silicon's penetration depth at 270nm is less than 100A (ssolid line in Fig. I-2), which make Si SPAD difficult to sense the solar blind wavelength.

(d) Because of the compact crystallography, 4H-SiC has excellent radiation-hardiness and long-term reliability. It has been measured that SiC exhibits radiation hardness to a dose of 5×10^{13} for 63.3 MeV protons without seeing any degradation (16). Displacement energy (E_d) is widely used for measuring the radiation hardiness and is one of the most fundamental parameters. It is defined as the minimum energy that must be imparted to a lattice atom to remove it from its lattice site. Fig. I-6 plots the displacement energy of some commonly used semiconductors (17). The displacement energy of SiC is 22eV in contrast to Si's 12eV. Hence, SiC detectors will have better radiation hardness and thus longer lifetime in strong radiation environments than Si detectors. For example, the DCR of Si SPADs used installed on the NASA ICESat satellite has been reported to increase 55.5counts/day in near-earth orbit satellite (18) due to the radiation damage, and a distinct increase (2500cts/s per device) in the dark counts due to a solar storm is also observed (18). The damage is mainly due to high energy protons (with energy of up to hundreds of MeV) with an average dose of 2×10^{9} particles/cm^2/year.

(e) 4H-SiC also has native thermal oxide, which greatly reduces the surface leakage current and improves devices' long-term reliability. This is a very important property for avalanche based detectors (APDs), since the critical field of SiC is 2.0MV/cm~5.0MV/cm, if without proper edge terminations the edge breakdown always happens first. For III-nitride APDs which has a similar bandgap and critical field as SiC, because it has no native oxide layers and its material quality is substantially inferior in comparison to that of SiC in terms of defect density, the GaN APDs tend to fail after a few drives (19).

(f) 4H-SiC has a high thermal conductivity and a very high power failure density (20) (21) as shown in Fig. I-7. This is an important property for 4H-SiC APDs, since 4H-SiC APDs tends to operate at higher breakdown voltage than Si APDs.

(g) 4H-SiC has a higher saturation velocity in comparison to that in Si which favors applications where speed is critical.

(h) 4H-SiC has a much lower defect density than any other III-nitride wide bandgap semiconductors. For example, AlGaN grown on GaN with proper Al concentration (>40%) is a near solar-blind material. However, GaN itself has a 10^5 higher defect density than SiC (22) even with the most recently released GaN free-standing substrate. Also it is very difficult to make high Al concentration in AlGaN and to have low defect density simultaneously. The high defect density of GaN and AlGaN greatly increases their leakage current in devices: for PiN it is 540× higher (23) than our SiC PiN diode; and for SBD, it is 1000× worse (24) than our SiC SBD. For APDs, the performance gap between SiC and III-nitride is even larger, SiC APDs has 380× better dark current density (regardless the area is 33× smaller),

100x better gain, 270× larger in dimension than typical GaN (25) (26) and AlGaN (27) APDs.

(i) Most importantly, 4H-SiC has very different ionization coefficients (28) for electrons and holes and the hole ionization coefficient is very high. In Fig. I-8, β and α are the hole and electron ionization coefficients. It can be seen that for 4H-SiC, β>>α, especially when electric field is low, which will be detailed in the design chapter. The very different β and α enables SiC APDs to have very low excess noises. GaN is believed to have a unit ionization ratio (29), which will lead to a high excess noise (30). SiC APDs have 10× lower excess noise than GaN APDs (31) (32). Note however that GaN could use superlattice to alter α and β.4H-SiC also has a high hole ionization coefficient, which is about 9× higher than Wurtzite GaN at 3.3MV/cm. It needs to be pointed out that Wurtzite usually has a better crystal quality than zinc-blende GaN and is currently used for GaN APD fabrication. A higher ionization coefficient will benefit counting efficiency for SPADs, since carriers are easier to initiate avalanche multiplications.

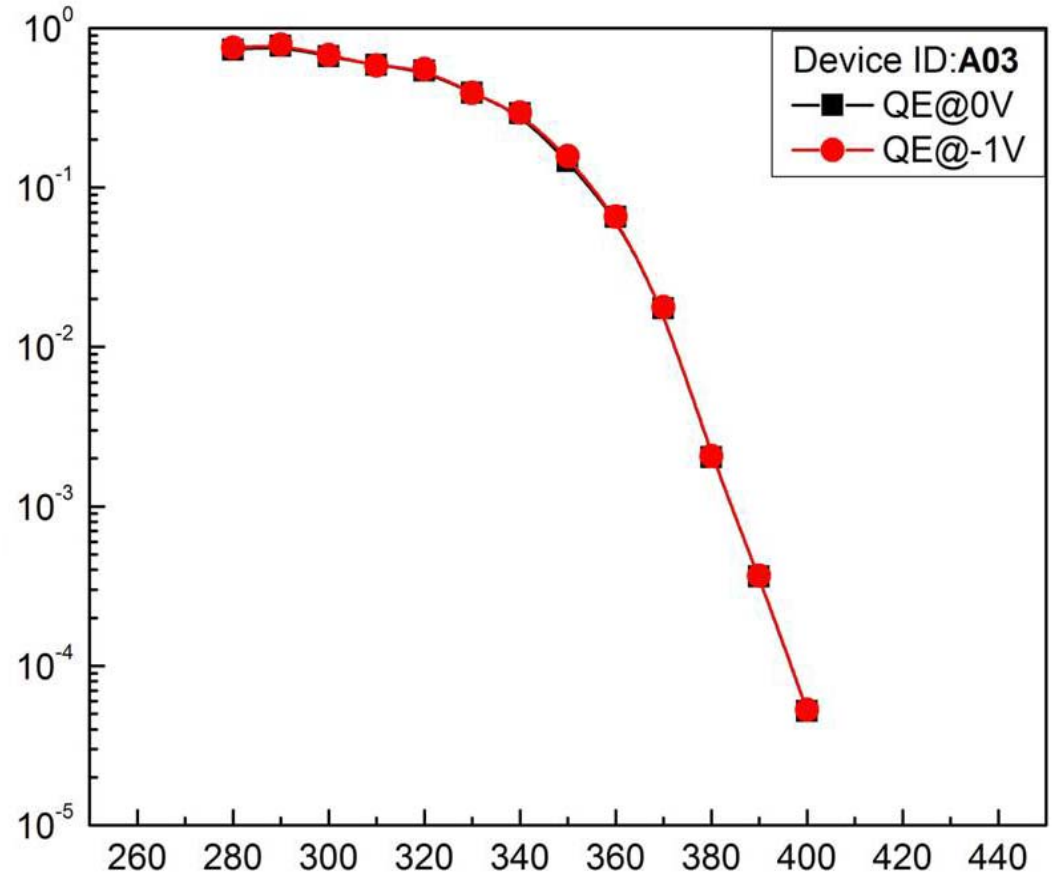


Fig. I-3 High QE in UV (82%) and high UV to visible rejection ratio (>10^4) for our SiC PiN with 5μm of absorption layer.

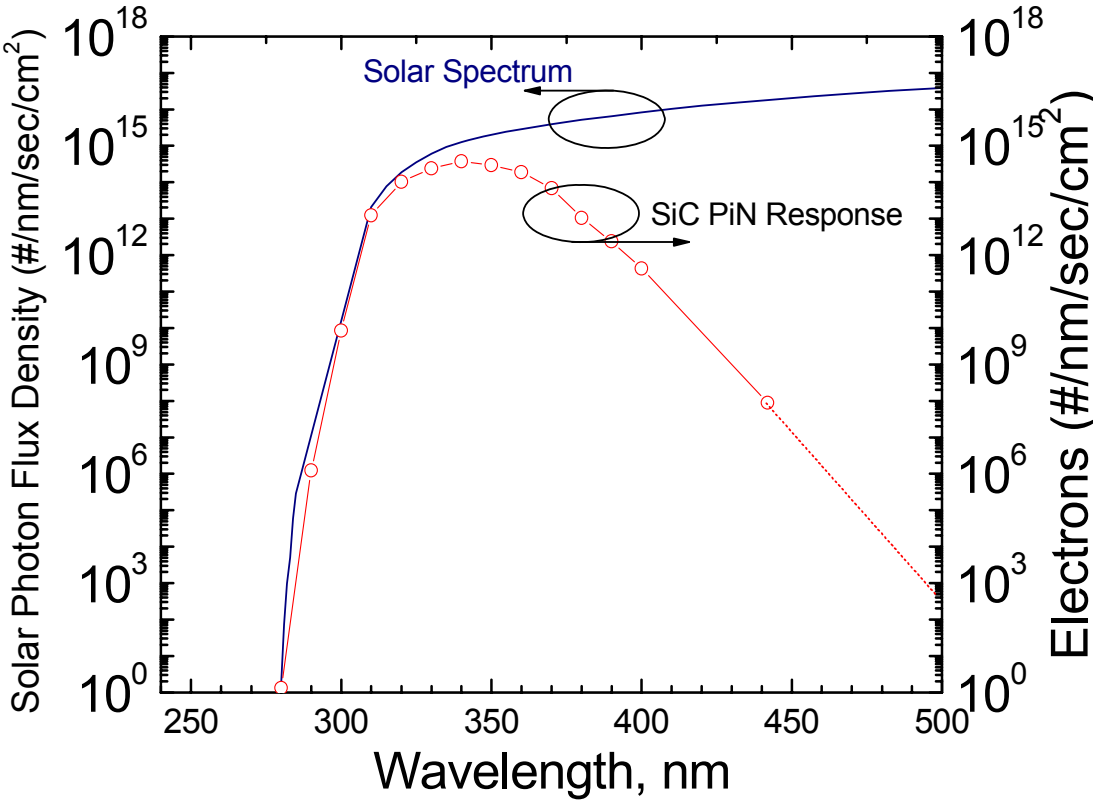


Fig. I-4 Solar Radiation Spectrum and number of carriers generated by our SiC PIN diode under solar radiations. Due to the wide bandgap of SiC, the response of SiC PiN to Solar radiation is orders of magnitude lower than that of Si.

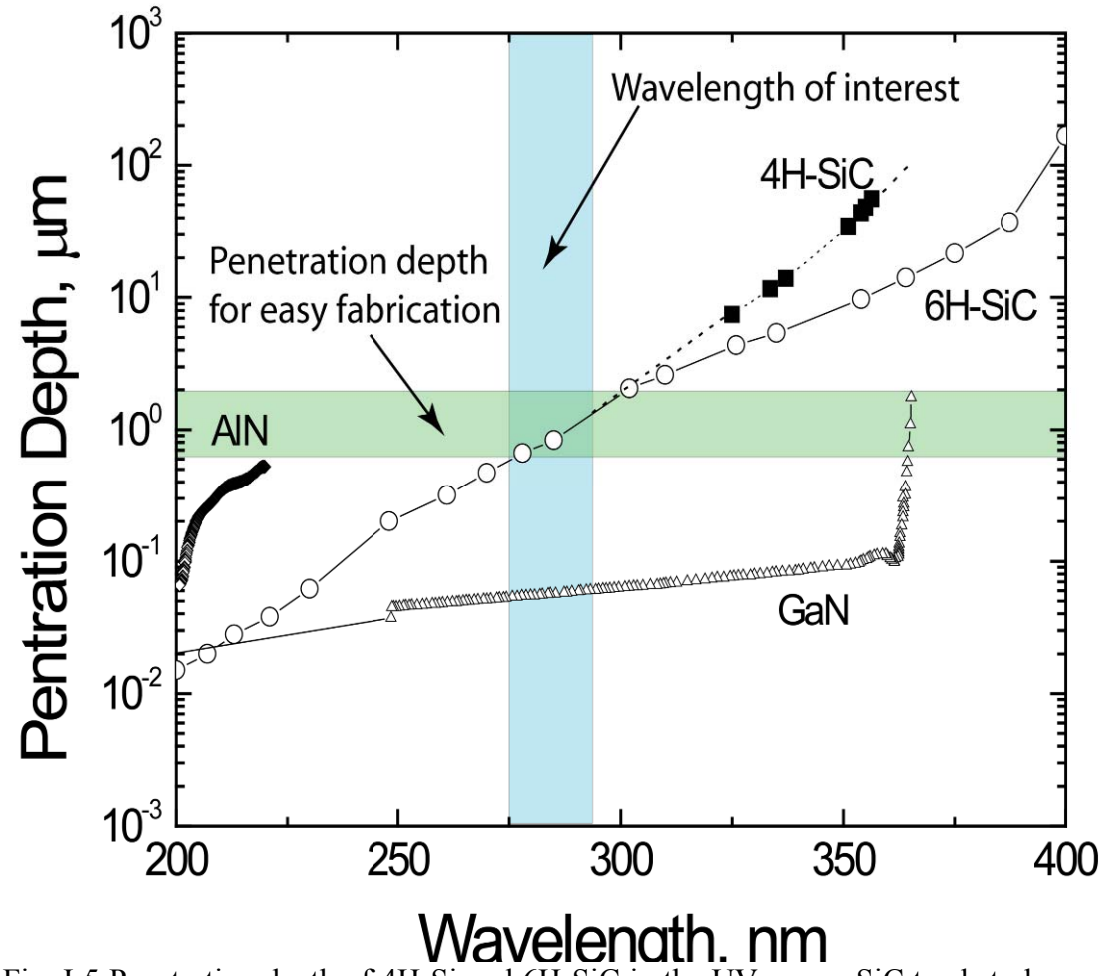


Fig. I-5 Penetration depth of 4H-Si and 6H-SiC in the UV range. SiC tends to have a proper penetration depth at the interested solar blind wavelength favoring the semiconductor fabrication, and make high quantum efficiency possible.

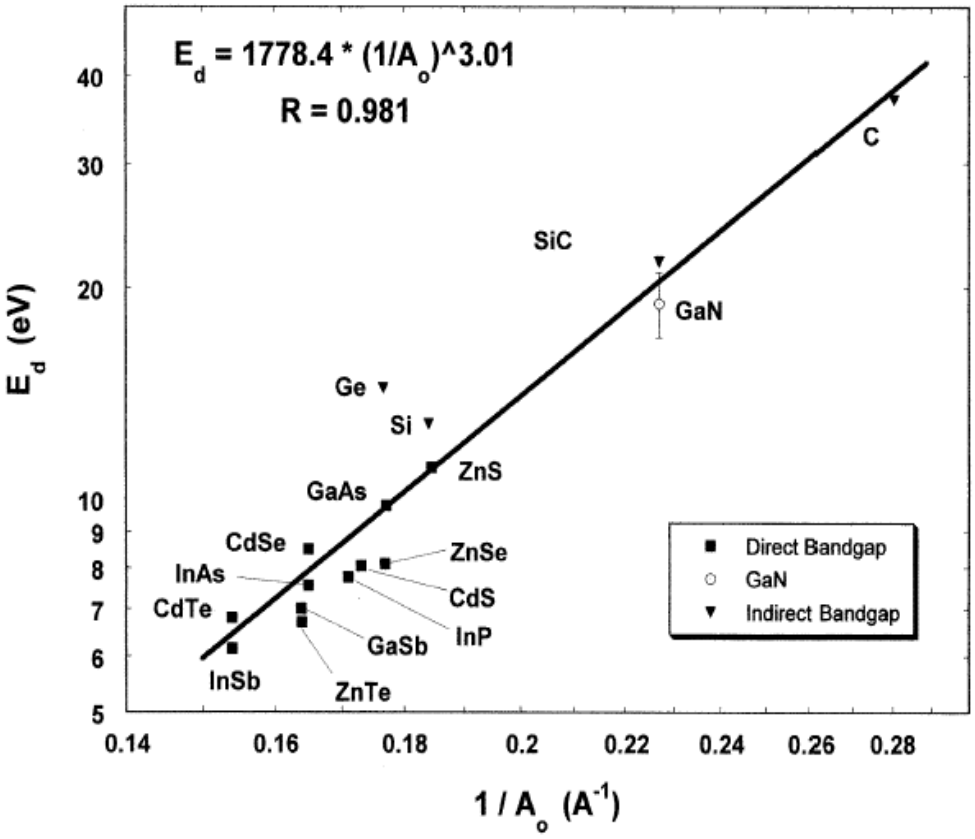


Fig. I-6 The displacement energy of some common semiconductors.

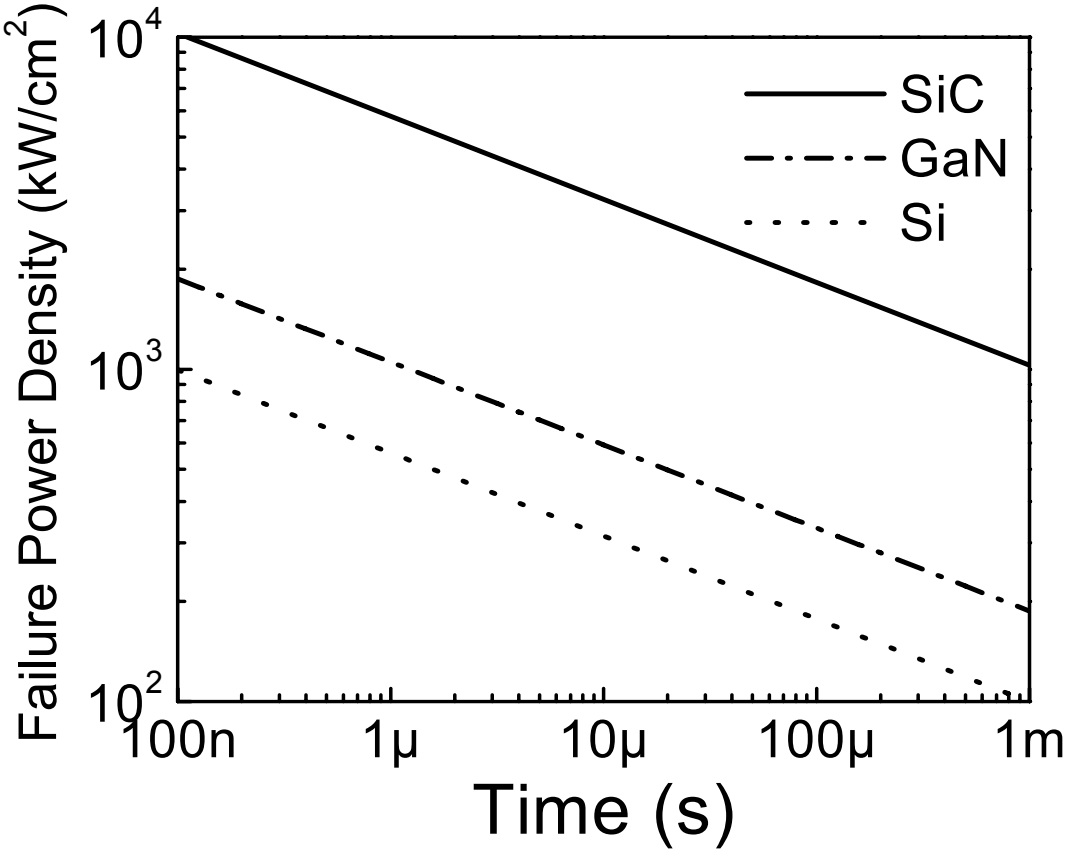


Fig. I-7 The failure power density of Si, GaN, and SiC vs. pulse width. High failure power density is very important for devices operating in single photon counting mode or in space where spontaneous cosmic ray radiation may cause instantaneous high current, resulting in device failure if the device power density go beyond the failure power density.

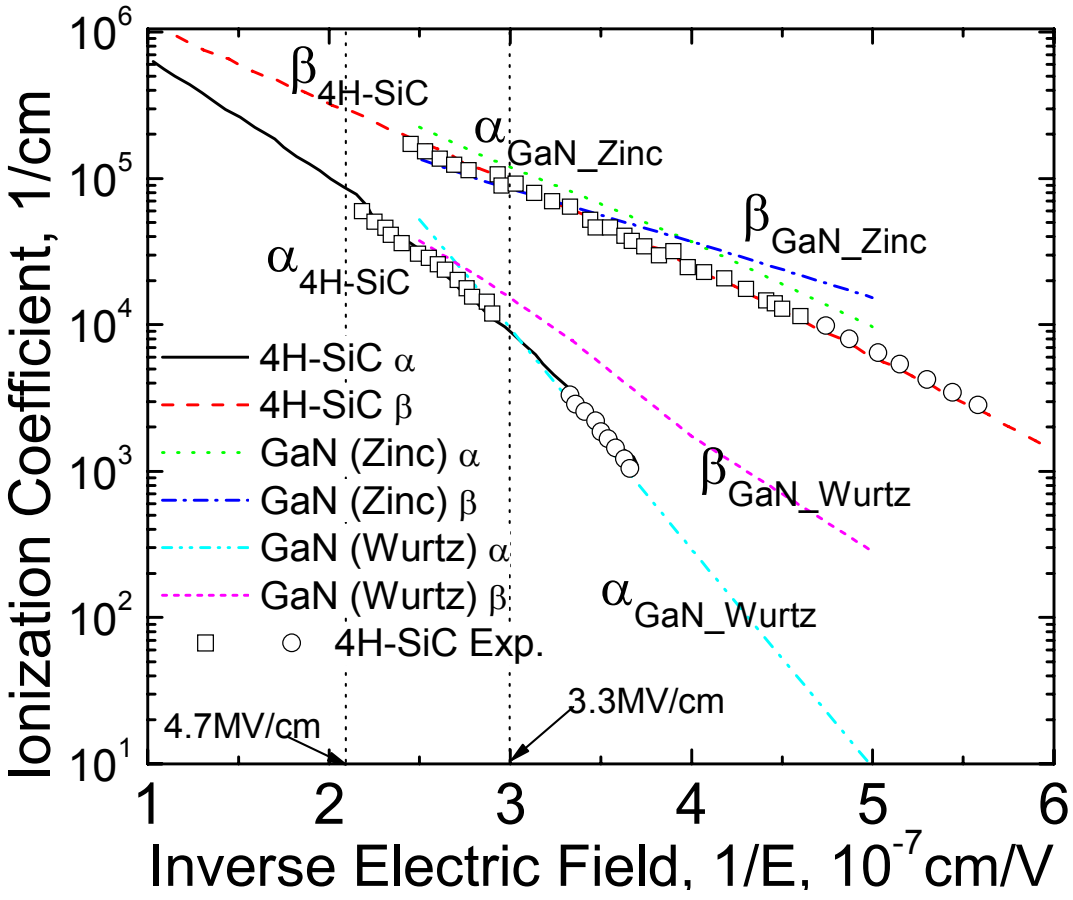


Fig. I-8 Experimental electron& hole impact ionization coefficients of 4H-SiC and GaN, which are the keys to the design of the extremely low dark count rate SPADs described in this thesis.

1.3 Si and InP Single Photon Counting: Recent Advances and Applications

This thesis work on 4H-SiC single photon counter started in year 2002. The original purpose of designing Si SPADs is to replace the bulky, higher voltage photo multiplication tubes (PMTs). PMTs are very sensitive to lights and have ultra low dark count rate when operating at Geiger mode. However, traditional PMTs are bulky and fragile, are power consuming, have high operating voltages (33), and require very expensive filters for UV detection. Most of PMTs need an operating voltage higher than 1000V. Another drawback is that it is easy to be damaged in harsh environment. Since 2002, major improvements have been made to Si and InP single photon counters. In 2004, NASA developed Si SPADs for Land Elevation Satellite (ICESat) with a peak quantum efficiency of 65% at 532nm, 15-17 MHz counting rate, and less than 200Hz dark count at -10^{o}C cooled by TE cooler (34) (18). Si SPAD single photon detection efficiency could be 60%~70% for 500nm~700nm (34) (35). The Si SPAD researchers quickly developed 1-D and 2-D arrays for imaging purpose (36) (12). One of the advantages of Si SPADs is their integration capability with standard CMOS fabrication which can combine the SPAD with quenching circuits (37) and time resolving circuits for time-correlated single photon counting, and time-of-flight (TOF) to produce two-dimensional and three-dimensional image (38), and optical time-domain reflectrometry (39). The integrated system is first developed in year 2000 with standard BiCMOS technology (40), and then in year 2002, integrated with CMOS passive quenching circuit, Si single photon counters area developed with a fast 32nsec dead time but very limited size (30μm^2) (41). Recently a 64-pixel array (42) has been demonstrated with each pixel size of 38μm×180μm, which provides a distance precision of ±0.75% for 2m-5m range. The major advantage of these 1-D or 2-D array detectors over CCD is their extreme sensitivity and

speed, which allows them to operate under very weak light singals, with ultra high time-resolution and space resolution.

For fiber communications, while the linear-mode NIR sensors towards the single photon counting is still on the horizon, the Geiger mode photon counter based on InP/InGaAs (aiming at 1.55μm signals) becomes commercially available in 2006 (43). To avoid the high DCR associated with the narrow bandgap of InGaAs, wider bandgap APDs also based on InP are developed. InAlAs/InGaAs SPADs targeting at 1.4μm signals wavelength (44) and InGaAsP/ InP targeting at 1.06μm (45) are reported with a DCR <100kHz at a ~10% detection frequency. It needs to be pointed out that the detection efficiency of both InP and Si based single photon counters are low in the fiber communication wavelength. An effort of upconversion of frequency (>95% efficiency) has been done so that the state-of-the-art Si SPAD could be used (46). The high speed readout circuits of single photon counters have also been thoroughly studied (47) (48) and are readily available in market (49).

The first 4H-SiC APDs was developed by Dr. Feng Yan at SiCLAB, Rutgers University in 1997, which demonstrated a gain of $>10^6$ and low leakage current density of $10nA/cm^2$ (50) for a $100\times100\mu m^2$ SiC APD. The maximum area of SiC APD fabricated is 540μm×540μm. About 20 papers have been published on SiC APDs and arrays based on a variety of edge termination technologies. The world's first SiC SPAD (51), in collaboration with NASA and United Silicon Carbide, Inc., New Brunswick, NJ, was developed by the author on year 2004. Since then, a research group from University of Taxes, Austin led by the world renowned avalanche photodetector research Dr. Joe Campbell, started their SiC

single photon counting development (52) after examing some earlier SiC APD devices fabricated by SiCLAB at Rutgers University. Excellent results have been reported by Dr. Campbell's team with a low DCR of 28kHz at 325nm and a detection efficiency of 3.6% (53).

1.4 Challenges in this Ph.D Thesis Research.

The transit from regular APDs to single photon counters is not easy due to the following reasons, and SiC SPAD is not achieved until this thesis work:

a. A single photon counter requires a very high optical gain as well as a very low DCR simultaneously. Typically when operating at Geiger mode, the gain is larger than 10^5 for a SPAD. A traditional APD operating at linear mode, with meaningful signal to noise ratio, often operates at gain of ~1000 because of the linearity problem. It will be detailed later that a high gain $>10^5$ is often necessary for single photon counting for actual applications because of external and thermal noises. A SPAD has to be capable of producing a distinguishable current pulses initiated by one photon-generated electron/hole.

b. Many photon counting applications have speed requirement, requiring the SPAD to operate 10MHz to 1GHz (3).

c. The mechanism of the dark counts in a SiC single photon counter is not well studied, thus methods of effectively suppressing the DCRs require careful study. It is clear that for Si and InGaAs, the major source of dark counts is mainly from its thermal generation or epitaxial interface defects, and cooling is always the most effective way to suppress the DCR. Another effective way is to scale down the size. For SiC, the thermal generation at room temperature is negligible and most of the dark carriers are generated through defects, either from defects on device surface, at epitaxial layer interface or through crystal defects. Understanding the mechanism of DCR is critical for developing SiC SPADs. It is possible to design proper wafer structures to limit the activation of these crystal defects. Also a lot of work has to be

done to reduce the surface defect density and to reduce surface electric field. In this thesis we proved that the defects-dominant DCR is not sensitive to temperature, thus the cooling is not necessary. Another positive side is that SiC SPAD can operate at a wide temperature range.

d. Edge termination is critical for SiC SPADs. SPADs require 100% bulk (crystal) breakdown, and SiC has a very high critical field (2MV/cm~5MV/cm). Without perfect edge termination, surface breakdown always happens before reaching bulk breakdown voltage because of the high surface defect density. Blocking 80% of the bulk value might be considered very successful for power devices, but for APDs, a 99% is a complete failure.

e. Ohmic contact is another critical issue as it is related to gain uniformity issue and quenching of avalanche breakdown, as will be addressed later.

Almost all of these issues have been studied more or less in the early day's SiC APD development, but there are more to be done when the devices are used for single photon counting purpose. Even in nowdays, Si SPAD detector size is still very limited and the price is high. Not every "good" Si APD can be used as single photon counter because of similar issues mentioned above.

Six sets of 4H-SiC SPADs have been fabricated and not all of them are successful. However, those unsuccessful devices provided very useful information towards a final success. Indeed, the majority of the thesis work is in understanding of how a 4H-SiC SPAD can be made, the source of dark current and dark counts, designing of wafer structures and

mask structures which are compatible with the current wafer growth technology and processing technology, the developing of the edge termination and p-type Ohmic contact for a wide range of doping, establishing the testing environments, coordinating with the wafer growers for a good epitaxial growth. In the following sections two successful sets of samples will be discussed in details: the first successful set of SiC SPADs and the final successful set of SiC SPADs with the best performance. They include several different wafer structures. Other research work, including SiC PiN, SiC semi-transparent SBD, and those unsuccessful SPADs will be briefly discussed when needed (such as in Ohmic contact sections). The sets of SiC SPADs are listed in Table I-1.

Table I-1 Several sets of fabricated SiC SPADs.

No.	Year	Name	Notes
1	2003-2004	6H-SPAD1	Very high defects density on wafer. The devices could not be driven to breakdown with both bevel and MJTE.
2	2003-2004	4H-SPAD1	Very high defects density on wafer. The device could not be driven to breakdown with both bevel and MJTE. Bevel surface is not good.
3	2004-2005	FQ-C FQ-D	Very high doping of p++ layer (>1e20) is successfully grown. The MJTE structure is successful but bevel is not. The first SiC SPAD is reported.
4	2005	DL31	No good Ohmic contact. MJTE leakage is very low. E-beam curing machine is down and no bevel structure is fabricated.
5	2005-2006	DL32	Ohmic contact is improved but dark count rate is high. E-beam curing machine is successfully repaired. Possible reasons of dark counts are identified. New approaches such as polyimide bridge are studied. The method of reducing the P.R. to SiC etching ratio is studied and possible solutions are provided.
6	2007	AD-B AD-E AD-C CM-A CM-B	SiC bevel etching has breakthrough during fabrication of this set. A new machine is purchased which is capable of substrate cooling. The etching ratio of P.R. to SiC are improved from 15:1 to 4.4:1. A dark current of <26fA at 90% of V_{br} are achieved for a large 23840μm^2 device area. Both MJTE and Bevel are fabricated. Ohmic contact problems are successfully solved and a low specific resistance <1e-3Ωcm^2 is achieved even for a p layer with doping of only 6e18cm^{-3}. However, the devices are contaminated due to a repairing of the DI water before the last step finished. Some samples are successful recovered after excessive cleaning.

II. DESIGN OF 4H-SIC SPADS

In this chapter, the design of wafer structure and mask for 4H-SiC SPADs is presented in details.

2.1.1 Design of Wafer Structure and Simulation Results

Two different groups of wafer structures are designed for this thesis work: one is based on p/n structure, including FQ serials wafers and DL serials wafers; the other is based on p/i/n structure, including AD serials wafers, CL serials wafers and C01 serials wafers.

2.1.1.1 Wafers with p/n Structures

One of the major purposes of developing SiC SPADs is to replace high voltage PMTs for UV measurement. Thus, a robust SiC SPAD with low operating voltage is an excellent candidate. To have a SPAD with as the lowest operating voltage, high-high p/n junction diodes are designed for the first set of SiC SPADs.

The FQ wafer is originally designed for a positive bevel, meaning the p layer doping is lower than the n layer doping (from bottom to top):

1st layer: Al doping, >1e19cm^{-3}, 0.15μm

2nd layer: Al doping, 1.e18cm^{-3}, 0.25μm

3rd layer: Nitrogen doping, 5e18cm^{-3}, 0.20μm

4th Layer: buffer layer and n-type substrate

The SIMS result (Fig. II-1) shows that the wafer has roughly same doping level for both p and n layers. The simulation (Fig. II-2) shows that it has breakdown voltage of 66.2V and a critical field of 4.7MV/cm.

Another set of wafers used for SiC SPAD fabrication are DL serials wafers. The wafer has a similar structure as the FQ wafer. SIMS measurement shows that it could be used to form a positive bevel, as shown in Fig. II-3. Simulation results are shown in Fig. II-4. This wafer has a lower doped p++ top layer.

As the first attempt of fabricating SiC SPADs, the wafer structures are not designed for high quantum efficiency or low dark count rate. We will focus on FQ wafer on which the first successful SPADs are fabricated.

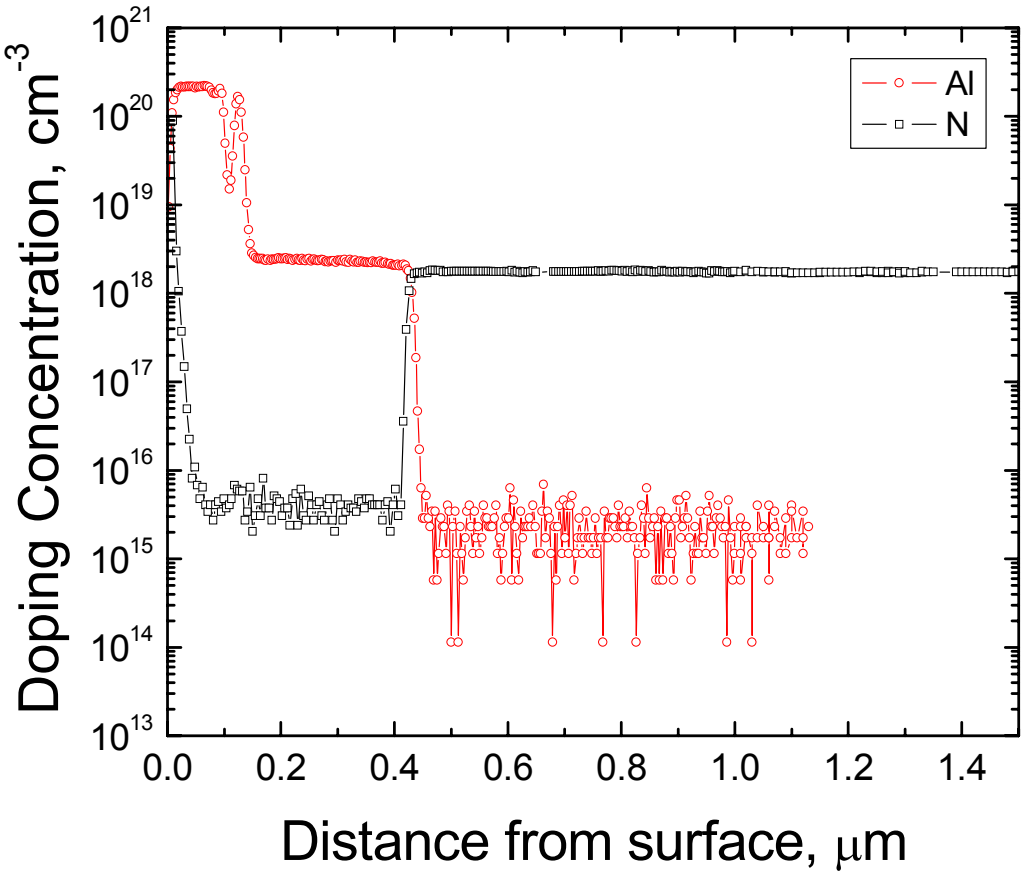
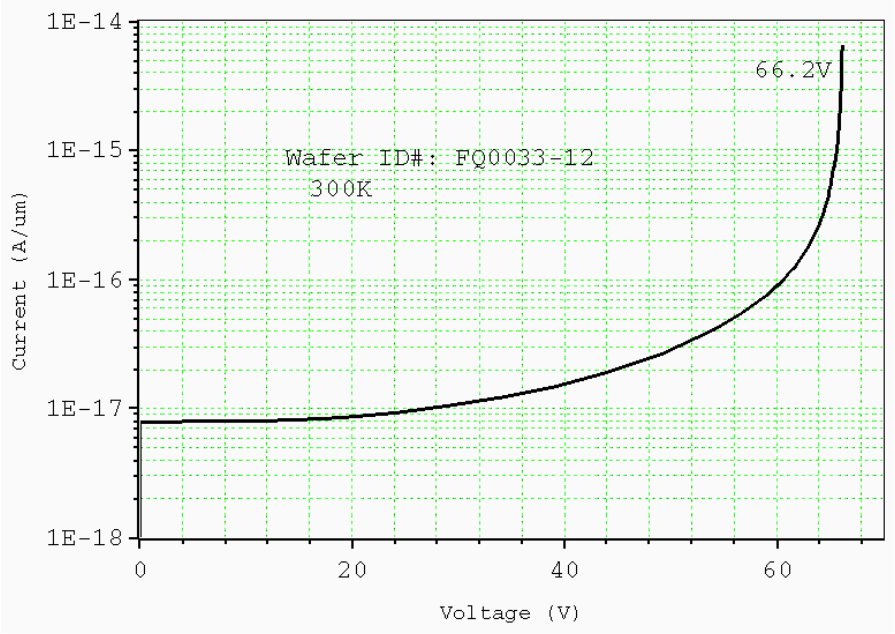


Fig. II-1 SIMS measurement for FQ wafer used for the first SiC SPAD.



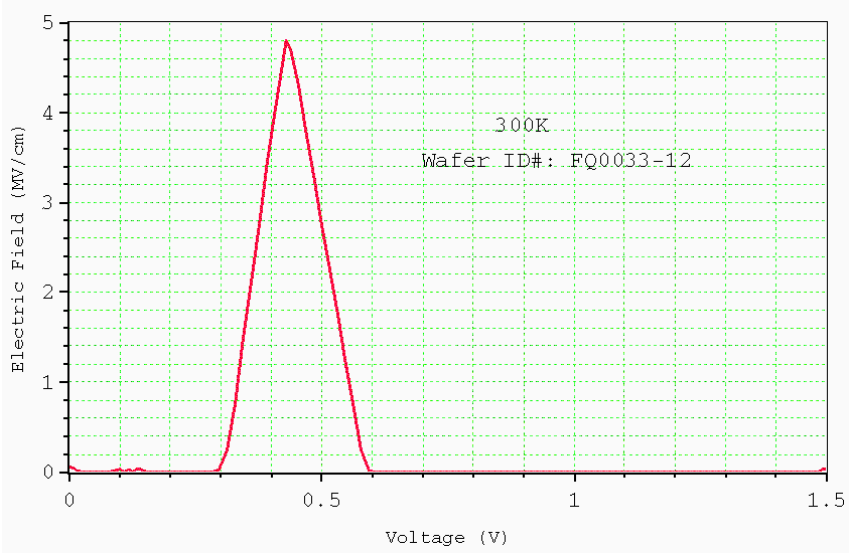


Fig. II-2 Simulation result based on SIMS measurement for FQ wafer. The simulation assumes an ideal edge termination.

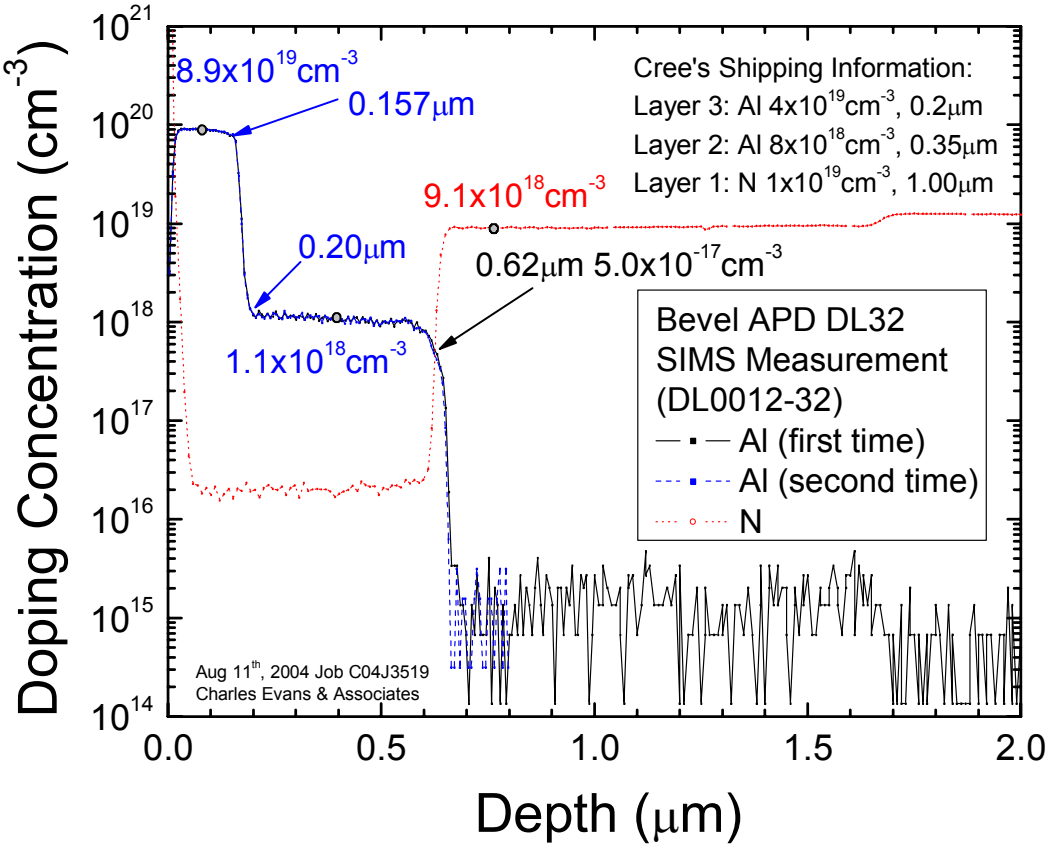


Fig. II-3 SIMS simulation on wafer DL32. The wafer has a structure which could be used for positive bevel edge termination.

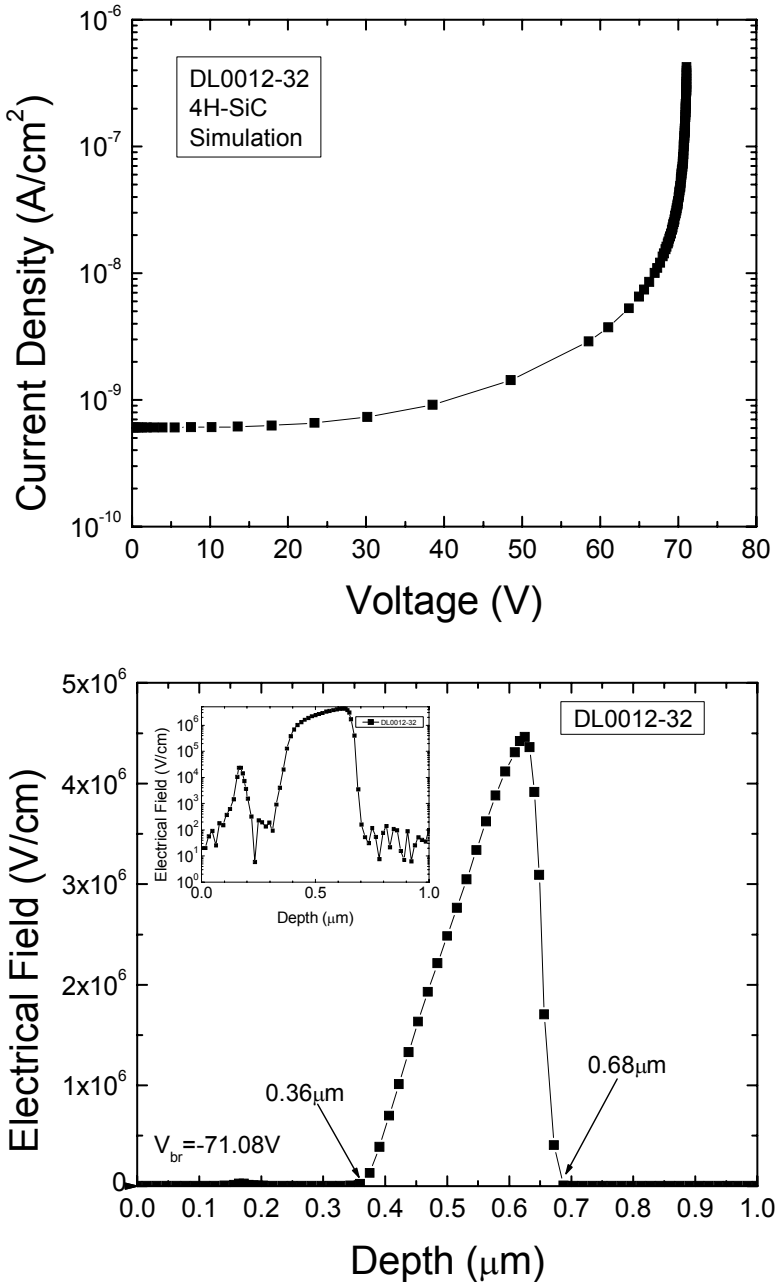


Fig. II-4 Simulation result based on SIMS measurement for wafer DL.

2.1.2 PiN Wafer Structures

The major problem associated with the first set of SiC SPADs is their high DCR, and their hight dark current. A low DCR is one of the most important targets for SiC SPADs, and a low dark current is equally important The dark current I_D has two components: surface leakage I_{DS} and internal leakage I_{DI}.

$$I_D = I_{DS} + I_{DI} \quad \text{(Eq. 2.1)}$$

These two components might have completely different effects on DCR. The total dark current sets a lower limit for the signal intensity. When the dark current is high, even with low DCR, one will not be able to calibrate the detectivity of a single photon counter for weak signals. Also, the dark current level is related to the surface morphology and reliability of a SPAD. Please note that the major purpose of the edge termination is to reduce the surface electric field and ensure the breakdown will not happen on surface. Therefore, the surface leakage carriers might not be fully multiplied and not likely to be detected as dark count pulses in the Geiger mode. Also, the surface defect scattering will reduce the multiplication gain. On the other hand the internal dark carriers could be fully multiplied, if they are generated in multiplication region or driven into the region. Thus how to suppress the internal dark carriers becomes the key task for reducing the DCR.

The first single photon counter is fabricated with Multiple Junction Edge Termination (MJTE technology). With first intuition, one might make the assumption thatthe lower the voltage, the less average surface field and the less leakage current. If the intuition were true, it would nicely allow researchers to design and fabricate SiC SPADs with lower voltage and lower DCR simultaneously. Unfortunately, this is not the case. The first major problem

associated with the low voltage is the very narrow depletion region and the high tunneling current, which is an internal leakage current, and causes high DCR. How this tunneling happens in a wide bandgap semiconductor like SiC is still not well studied. For SiC the I_{DI} is probably a result of defect-assisted tunneling. With help of defect levels close to the mid bandgap, the carriers might be pumped from the valence band to the conduction band under a high electric field. At high field, the effective barrier width becomes narrow. One supporting evidence is that after we suppress the surface leakage to a very low level, the leakage current and DCR is still very different from device to device. It implies that at least this is not a simple, direct tunneling effect.

To further reduce the DCR, a PiN structure is designed with a lowly doped layer. For SiC, the "i" stands for either n- or p- layer with doping less than $10^{16}cm^{-3}$. The lowly doped layer not only increases the barrier width, but also reduces the peak electric field in SiC.

The PiN wafers include three sets of wafers: AD, CM and C01. The wafer structures for these wafers are shown in Fig. II-5 to Fig. II-10.

To fully illustrate the effect of the field limiting layer, a detailed simulation is made for wafer C01 structure with and without the "i" layer (Fig. II-8). With the field limiting layer, the peak bulk electric field is reduced from 4.4MV/cm to 3.2MV/cm, and the depletion region width is more than doubled. The surface electric field distributions for 5^{o} bevel for both structures are also simulated (Fig. II-9). It can be been clearly seen that the surface field is almost unchanged with or without the field limiting layer. The field limiting layer mainly increases the tunneling barrier width and reduced the bulk electric field in SiC.

We will focus on the AD wafers in this thesis. The separation and absorption (SAM) SAM layer structure is designed as:

1st layer (p-contact layer): Al doping, >3e19cm^{-3}, 0.2μm

2nd layer (field termination p layer): Al doping, 1.3e18cm^{-3}, 0.3μm

3rd layer (field limiting i layer): Nitrogen doping, <5e15cm^{-3}, 0.3μm

4th layer (field confinement n layer): Nitrogen doping, 1e18cm^{-3}, 0.05μm

5th layer (absorption layer): Nitrogen doping, 5e15cm^{-3}, 3μm

6th Layer: buffer layer and n-type substrate

The SIMS measurement shows the following deviations from the original design and we will discuss them in the following chapters.

(a) There seems to be two non-continuous growth interfaces, with one of them in the multiplication region and the other in the absorption region side. It will be interesting to know if the non-continuous grown epitaxial structure will create more DCR than the continuously grown pn structure designed for the first SiC SPAD.

(b) The p++ layer is doped at 2e19cm^{-3}, which is slightly lower than the specification. We need an improved OOhmic contact scheme for this doping and thickness.

(c) The p doping is low and depletion region extended into the p++ layer. This might cause problems for the MJTE structure.

(d) The field limiting layer is p-type due to memory effect but it should not create any problems.

We will also exam if this structure has higher QE than the first SiC SPADs.

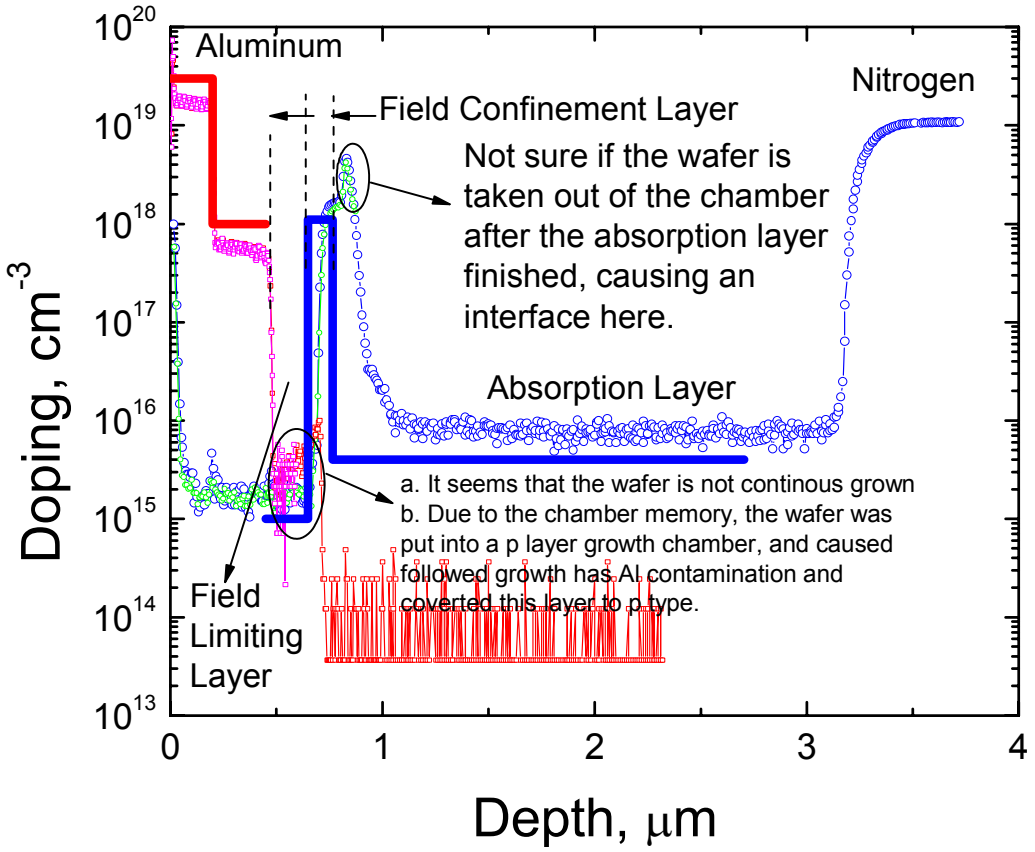


Fig. II-5 SIMS measurement for AD wafer. The solid line is the original wafer design. And the dotted line is measurement results.

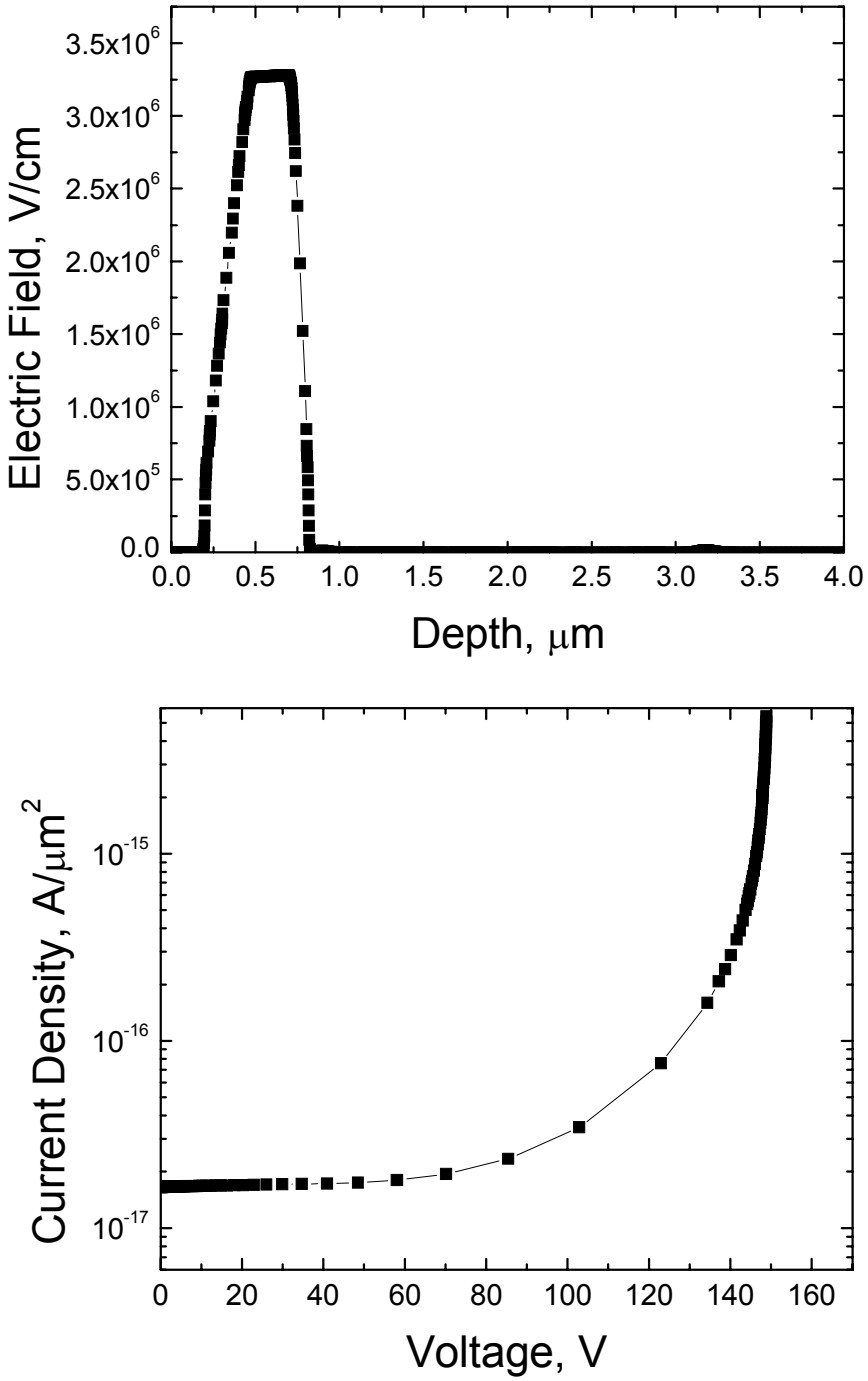


Fig. II-6 Simulation results based on SIMS measurements for wafer AD.

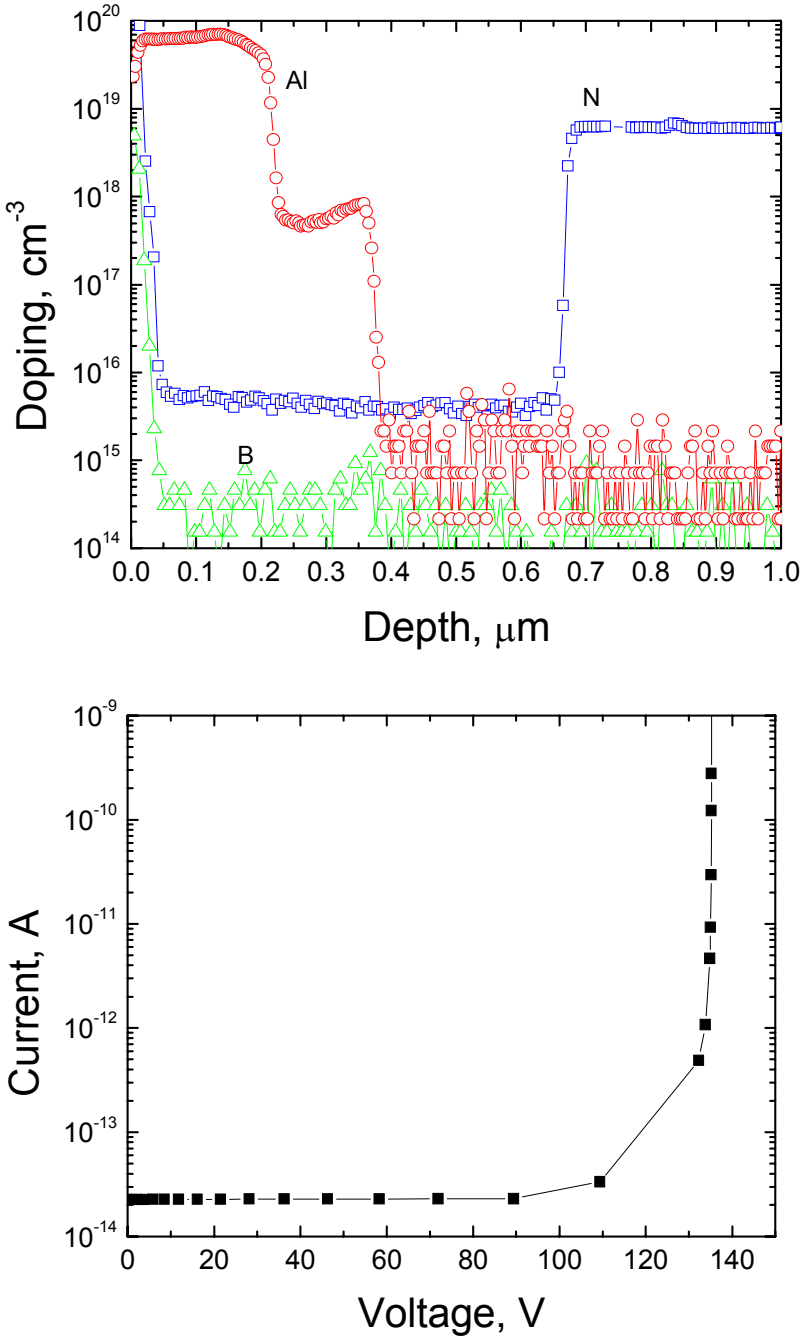


Fig. II-7 SIMS measurement for C01 wafer (top figure) which has a breakdown voltage of 135V (bottom figure, simulation based on SIMS measurement).

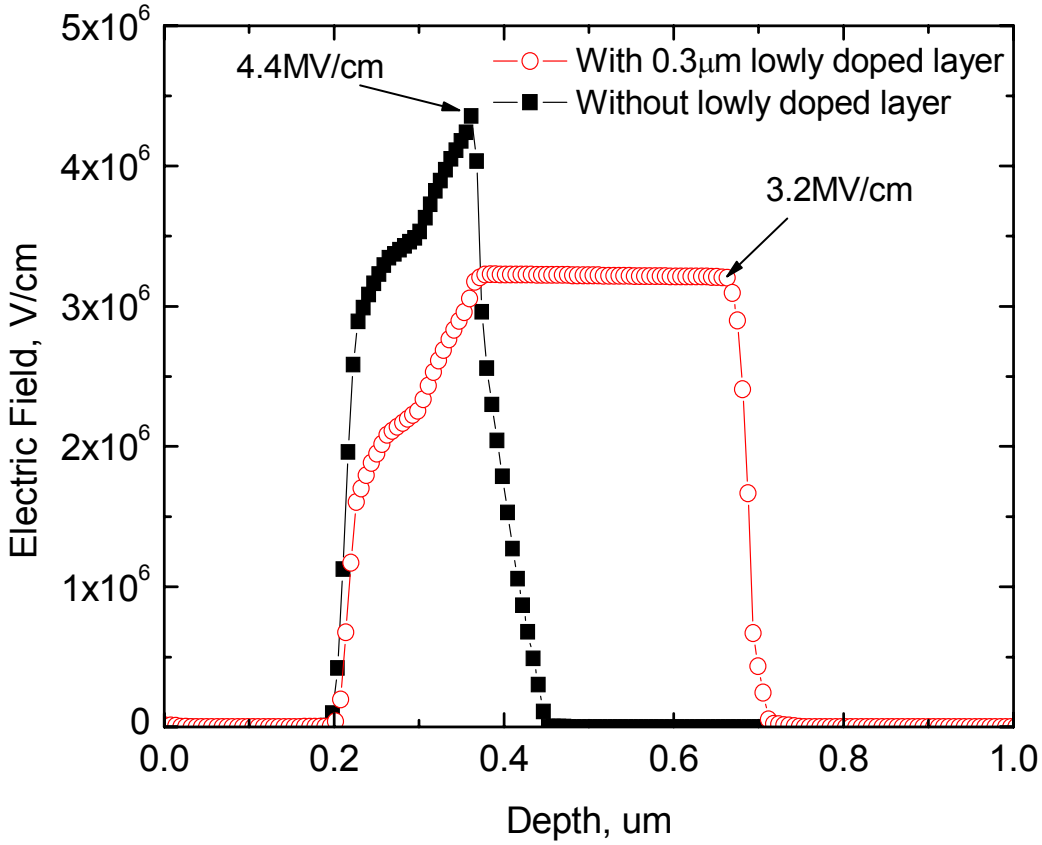


Fig. II-8 Electric field simulation for C01 wafer based on SIMS structure (red circle) and a structure assuming no field limiting layer is grown (dark square).

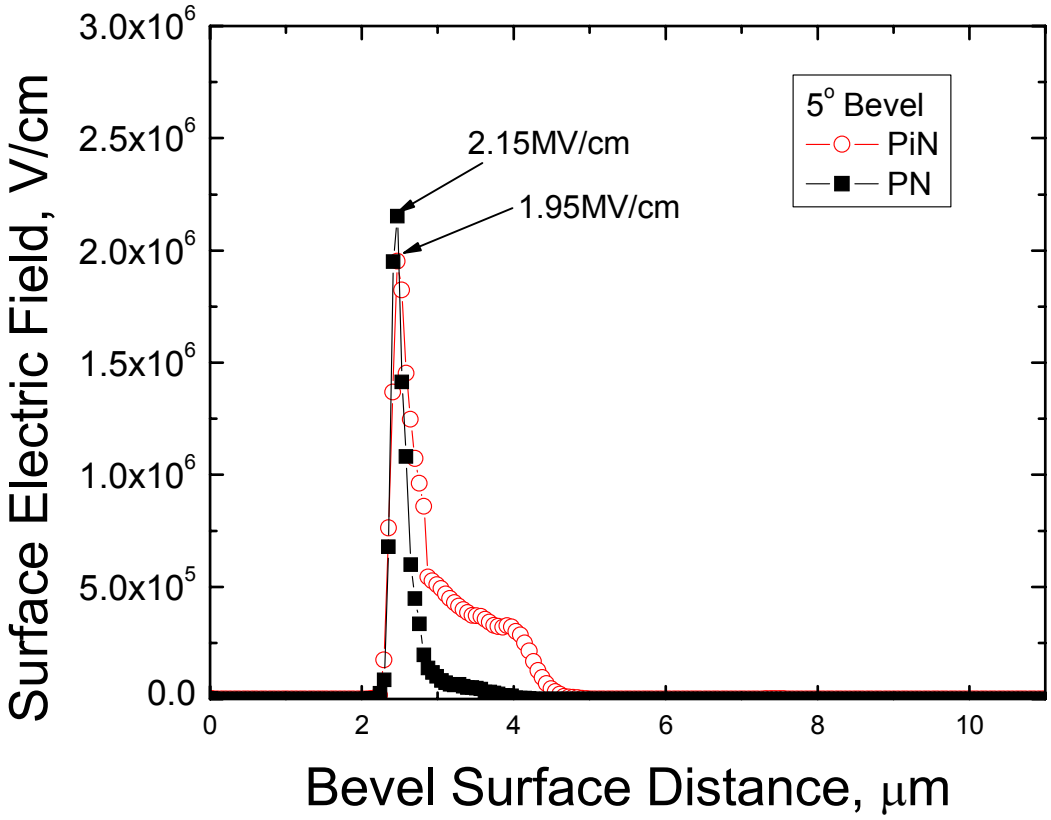


Fig. II-9 The surface electric field simulation for structures of a PiN (red circle) structure based on SIMS measurement and a PN (dark square) structure without the field limiting layer at breakdown voltage.

2.2 Design of Mask Structure

Two sets of masks are used for this thesis work. One has two MJTE steps (Mask-I); and the other is designed with three MJTE steps, which also can be used for bevel structures (Mask-II). The details of Mask-II design is presented in Appendix E.

2.2.1 Mask-I design

Mask-I set consists of 6 masks, including two optional masks. Three types of devices are designed, with mesa areas of 160μm×160μm, 210μm×210μm, and 260μm×260μm. The corresponding optical window areas are 74μm×34μm, 112μm×61μm and 150μm×105μm, respectively. The probing area is sitting on the same active mesa as the optical window. The OOhmic contact area has similar size as the probing region. A top view of mask design for a 160μm×160μm mesa device is shown in Fig. II-10. The exact dimensions of the device mesa size, JTE width, optical window area, Ohmic contact area and bevel width are summarized in Table II-1.

The Mask-I provides two steps of JTEs, each step with a wide 15μm width. It keeps a compact structure, with a small probing area and an optical window on the same active mesa mesa for a easy fabrication. There are several drawbacks:

a. The probing pad is too small for our wire bonding facility at Rutgers and USCI and occupies a too large area on the active region, especially for small devices. A minimum 90μm×60μm bonding pad is needed. So the devices can be probed and tested on die, but cannot be packaged, except for very large devices with very low yield.

b. Its two-step JTE might not be sufficient when the epitaxial layer doping and thickness variation is large.

c. The square shape of the mask design makes the mask set difficult for bevel structures which prefer a circular shape.

d. The optical measurement system has been modified to a fiber coupled system. Thus the light spot is more close to a Gaussian distribution. The rectangular shape of the optical window makes calibration inaccurate as the UV light is over-fill the devices. A circular optical window is preferred.

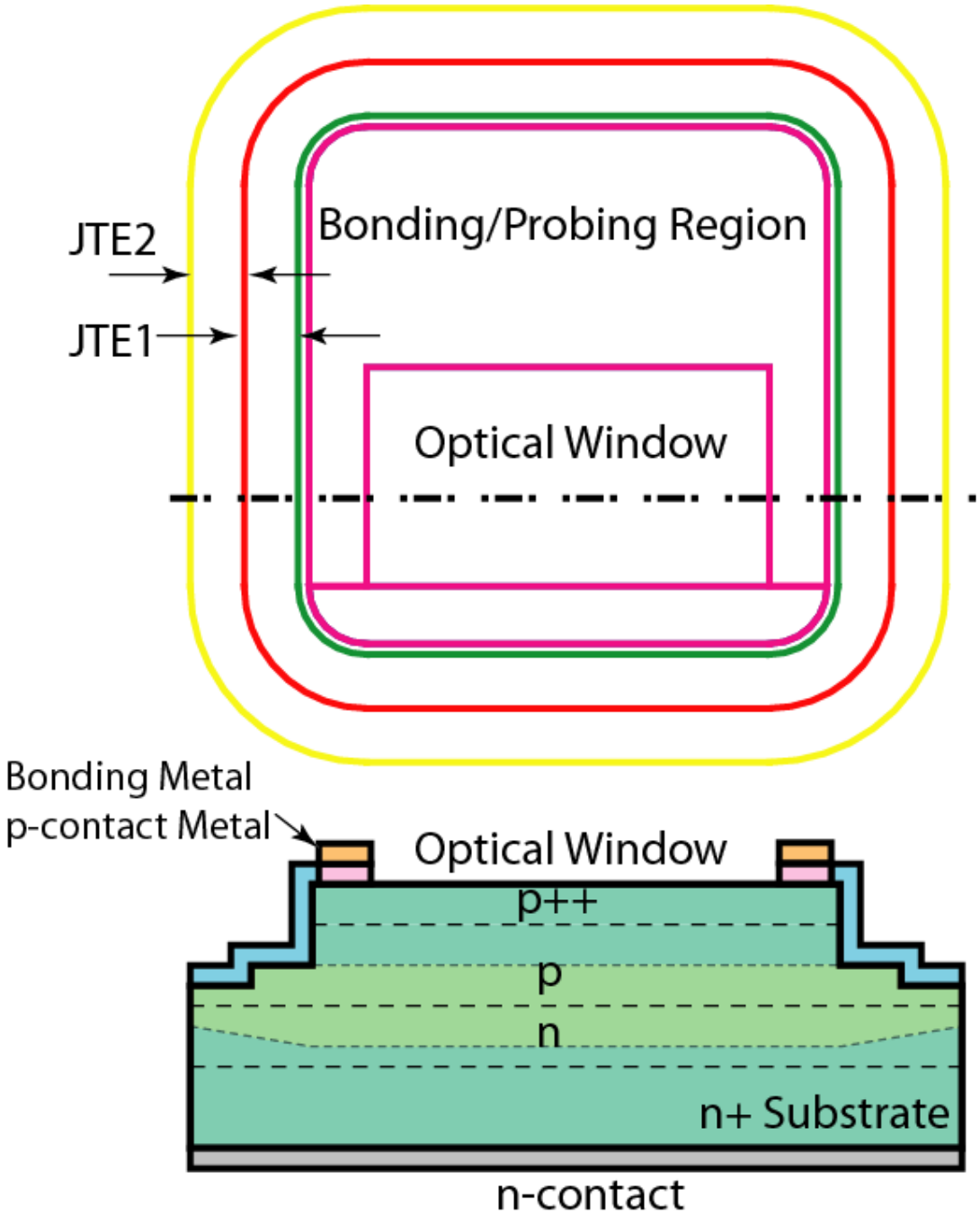


Fig. II-10 Mask design and crosee-sectional view of a 160umx160um mesa device with 74umx34um optical window and two 15μm JTE steps.

Table II-1 Dimensions of devices designed on Mask-I.

Set ID	Device ID	Mesa Area	Bevel Width	Optical Window Area	Ohmic Contact Area	Bonding Pad Type
I	I-160	24,012 μm^2 (160μm×160μm)	15μm~ 30μm	2,526μm^2 74μm×34μm	6,232μm^2	On-mesa
	I-210	42,039μm^2 (210μm×210μm)	15μm~ 30μm	6,832μm^2 112μm×61μm	13,684μm^2	
	I-260	65,003μm^2 (260μm×260μm)	15μm~ 30μm	15,750μm^2 150μm×105μm	21,471μm^2	

2.2.2 Mask-II Design

To overcome the problems associated with the Mask-I, Mask-II is designed. Mask-II consists of 11 masks. Not all the masks are needed for each SPAD structures. The set is designed for multiple device structures, including bevel and MJTE, regular p/n, p/i/n structure or upside down p/n, p/i/n structures, as well as nuclear particle detectors. The structure also considered RF excess noise measurement requirements. Two types of devices are designed: one type with on-mesa bonding pad and the other with off-mesa bonding pad. The following aspects are emphasized for Mask-II set design.

a. Smooth mesa design is for both Bevel and MJTE edge terminations.

For all devices, a smooth edge is designed without any straight lines and sharp corners. This design not only keeps the device area minimum, but also is optimized for an easy bevel formation. The SiC bevel formation, as will be detailed in the next chapter, depends on the photoresist bevel formation. Photoresist is baked at high temperature to form the bevel. Any lines with different curvature (such as a straight lines and corners) tend to cause a different surface tension and finally transfer a different bevel angle on SiC. Those locations with large bevel angle will become the weakest link at breakdown voltage. To keep the same bevel angle, Mask-II is designed to have uniform curvature for each type device.

b. Circular optical window design is for calibration with fiber optical system.

For the on-mesa type, the circular optical window dimension varies from Φ50μm to Φ1mm, and the JTE step has two types, 6μm×3 for small devices and 10μm×3 for large devices.

c. Large bonding pad design is for wire bonding purpose.

All the bonding pads are designed to have a minimum size of 90μm×60μm for both the on-mesa and off-mesa type of devices.

d. Off-mesa design targeting for the lowest dark count rage and for devices with a variety of operating voltages.

To minimize the device mesa area and thus to minimized the dark count rate, off-mesa type of devices is designed where the bonding pad is pulled out to a bonding mesa where the SiO_2 and Si_3N_4 is not removed. With only a few volts of voltage drop on the dielectric layer, the bonding mesa will not provide any noticeable leakage current. For low voltage devices, in the bridged region, where the area is small, the dielectric layer will block all the voltage; for high voltage devices, polyimide can be filled and help to block the voltage. A testing on polyimide voltage blocking shows a 3μm polyimide will block 400V without any problem.

e. A three-step JTE design providing more tolerance for wafer epitaxial layer thickness and doping variations.

f. A front contact for substrate for different wafer structures, and/or for excess noise and speed measurement. They are beyond this thesis work. Readers of interest can check the Appendix A for details.

Examples of two SiC SPADs both with Φ50μm optical windows are shown in Fig. II-11 and Fig. II-12. One is designed with on-mesa bonding pad and the other with off-mesa bonding pad. With the identical optical window size, the on-mesa type device has a mesa area of 23,850μm^2, versus the off-mesa type area of 12,868μm^2. It is well known (54) for Si

SPADs that the device dark count rate drops almost exponentially with device diameter (Fig. II-13). The reason is concluded as the "gettering" effect which helps smaller device to "squeeze" out the defects during high temperature annealing. For SiC, it is unlikely that such an effect will be an effective way to remove the defects. However, we do observe that smaller devices have much higher yield and lower dark current (Fig. II-14). Without sacrificing the optical window area where the light is absorbed, the off-mesa devices tends to have lower dark count rate and higher yield. It needs to note that there is one major drawback of the off-mesa devices other than the additional step of processing (overlay metal to connect the active mesa and the bonding mesa): Ohmic contact. In comparison to the large p-type Ohmic contact area of 9,147μm^2 for the on-mesa type, the off-mesa type only has a p-contact area of 3,007μm^2. It will be detailed later that a poor Ohmic contact resistance tends to self-quench the device and result in a much higher dark count rate, as a higher bias has to be used. In other words, the off-mesa devices has higher requirement on OOhmic contact.

The device dimension for Mask-II is summarized in Table I-1.

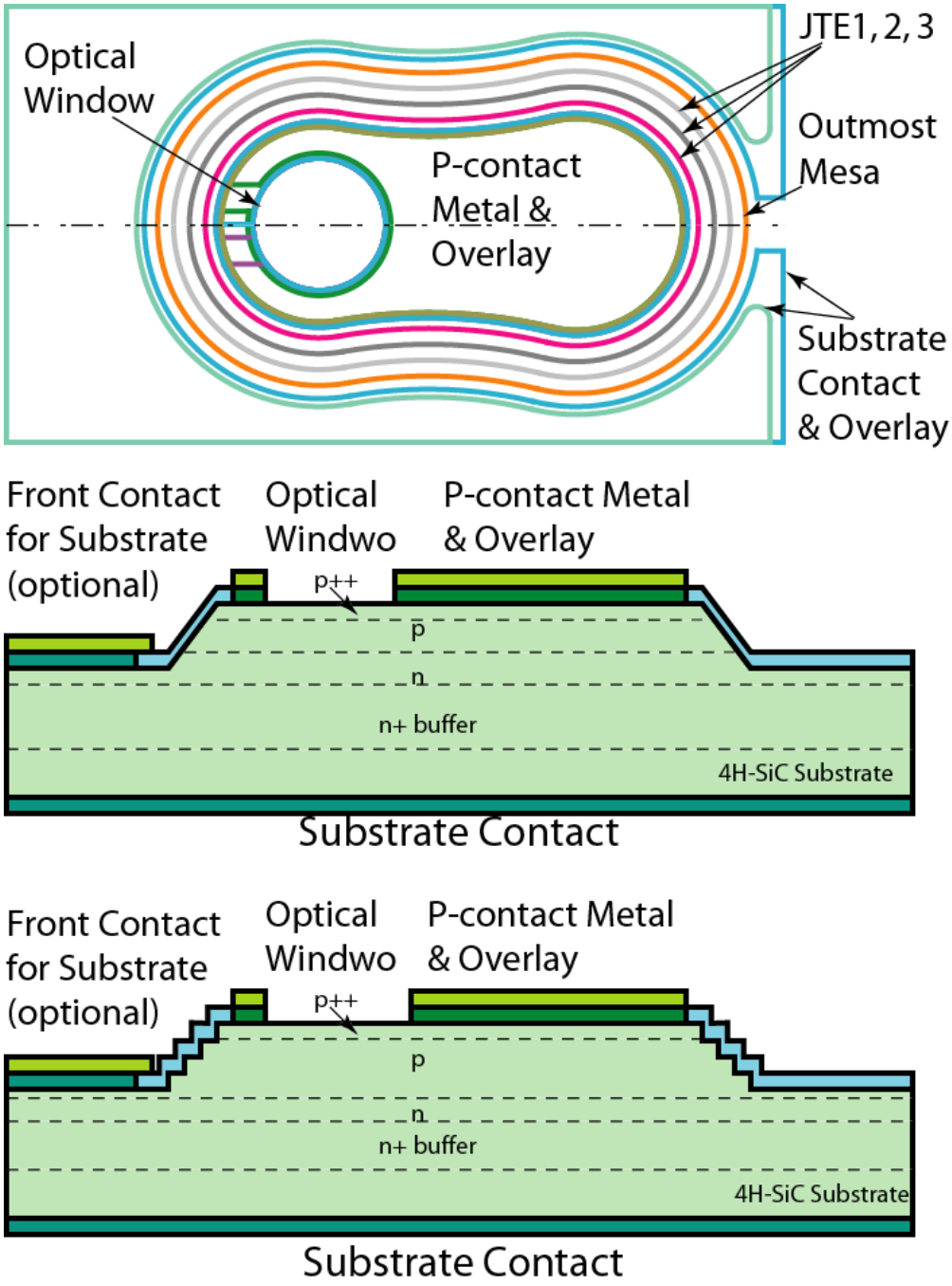


Fig. II-11 Mask design in Mask-II for a SiC SPAD with Φ50um optical window and an on-mesa bonding pad. The cross-sectional views with Bevel and MJTE are also shown.

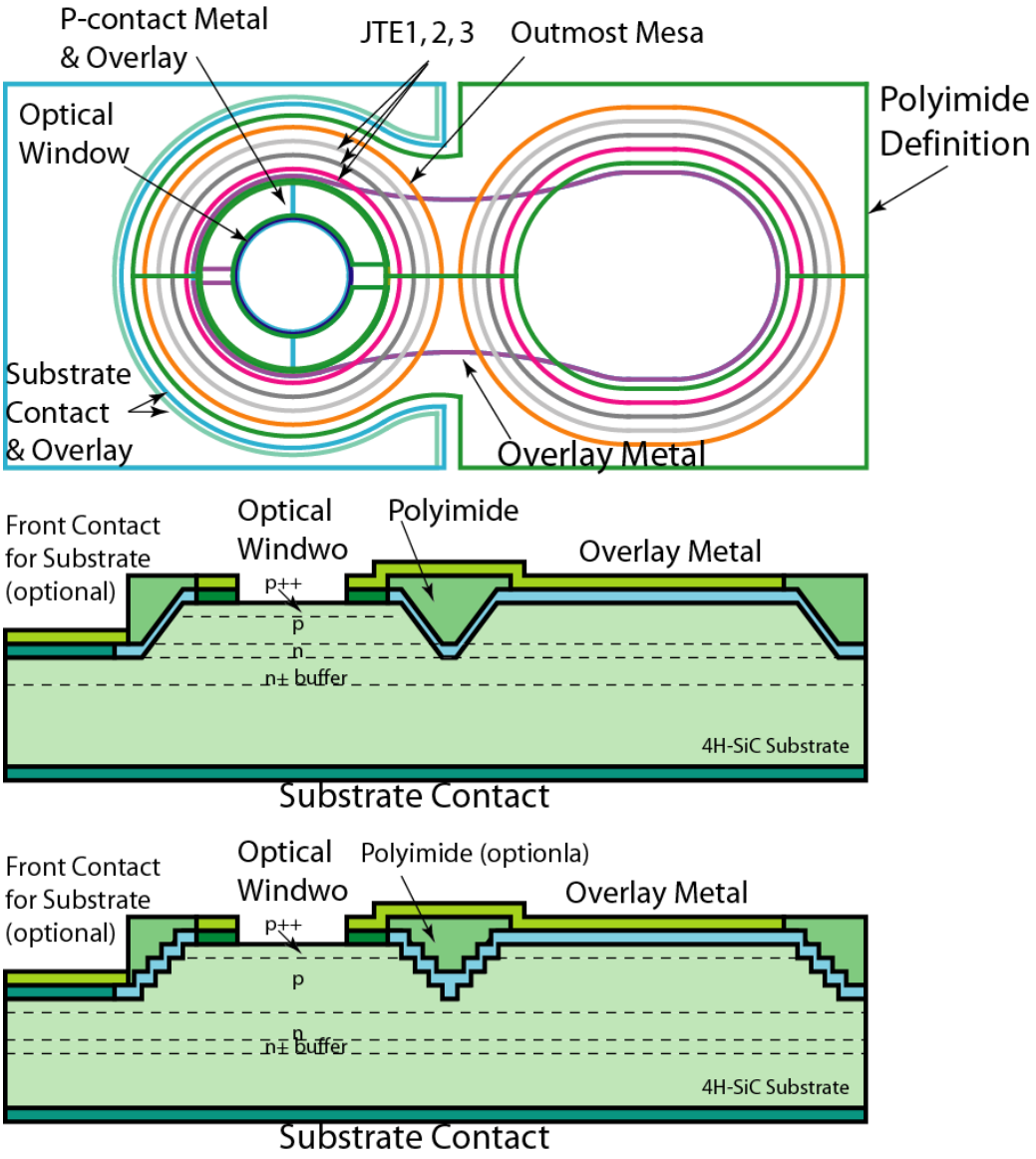


Fig. II-12 Mask design in Mask-II for a SiC SPAD with Φ50um optical window and an off-mesa bonding pad. The cross-sectional views with Bevel and MJTE are shown in the middle and bottom figure. The optional polyimide bridge is also shown.

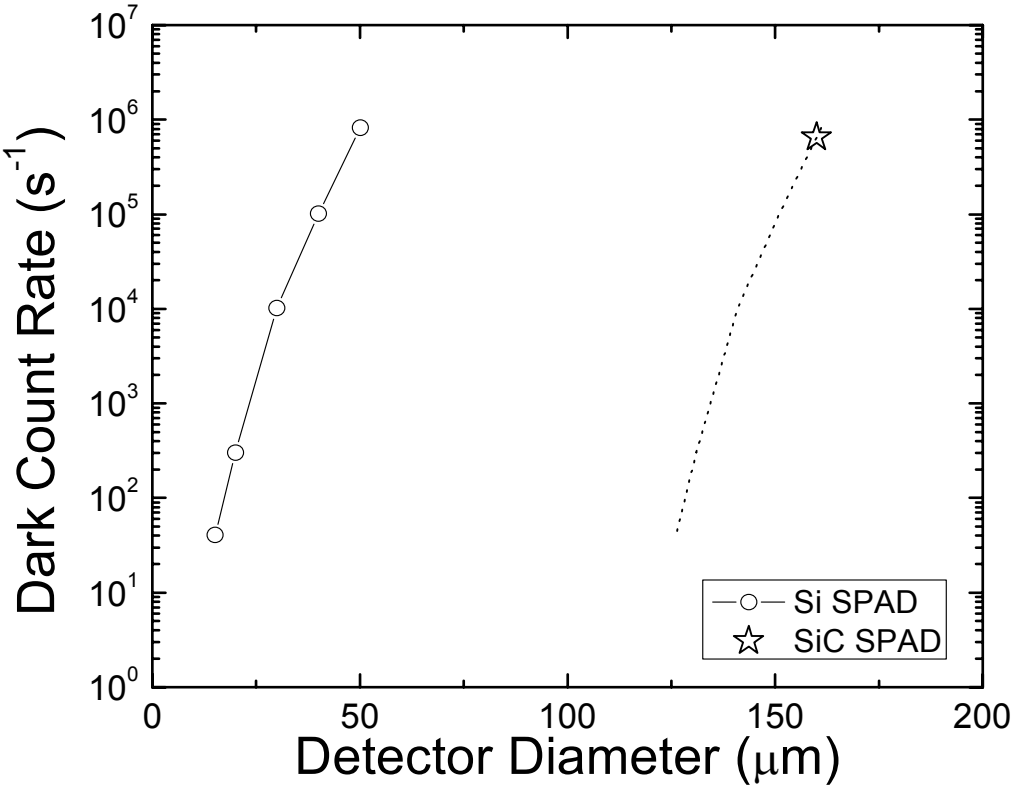


Fig. II-13 Dark count rate of a fabricated SiC SPAD and state-of-the-art Si SPADs.

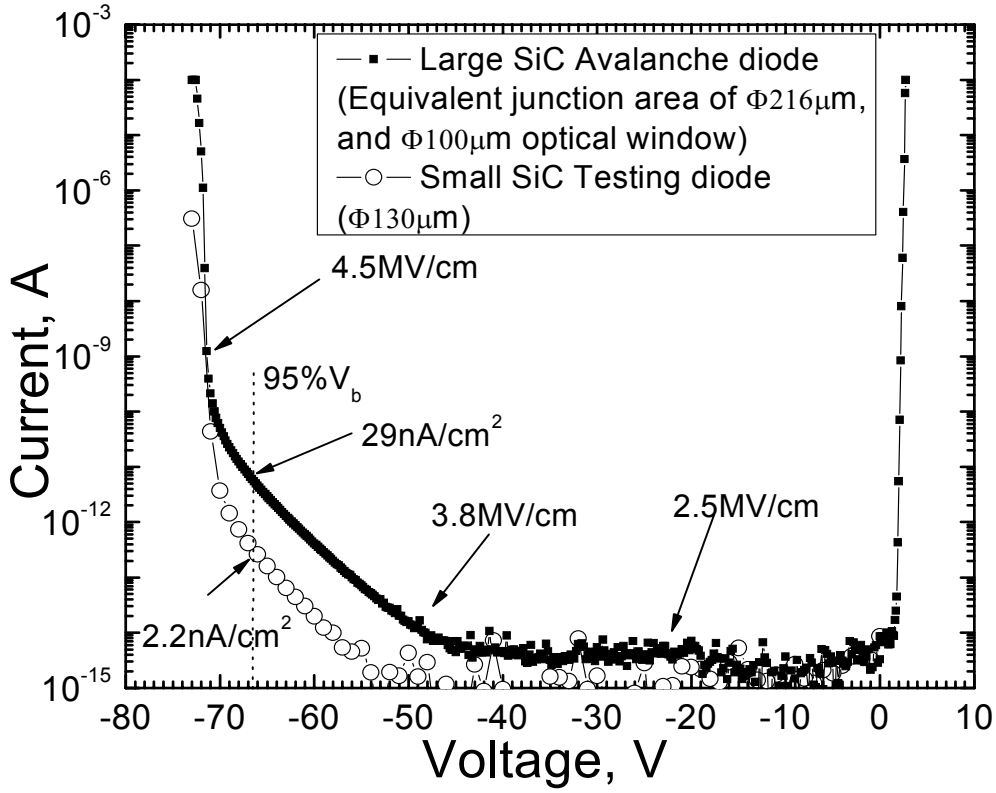


Fig. II-14 I-V measurement of two typical 70V V_b 4H-SiC avalanche diodes. The small erdevice shows one order of magnitude lower dark current density at 95% of Vbr despite of the area is 36% of the bigger one.

Table II-2 Dimensions of devices designed in Mask-II.

Set ID	Device ID	Mesa Area	JTE width	JTE Step No.	Bevel Width	Optical Window Area	Ohmic Contact Area	Bonding Pad Type
II	II-50A	23,850μm^2	6μm	3	18μm	1,963μm^2 Φ50μm	9,147μm^2	On-mesa
	II-100A	36,603μm^2	6μm	3	18μm	7,850μm^2 Φ100μm	11,827μm^2	
	II-200A	78,560μm^2	6μm	3	18μm	31,415μm^2 Φ200μm	23,165μm^2	
	II-200	84,046 μm^2	10μm	3	30μm	31,415μm^2 Φ200μm	17,290μm^2	
	II-500A	264,208μm^2	10μm	3	30μm	170,585μm^2 Φ500μm	16,832μm^2	
	II-500B	264,208μm^2	10μm	3	30μm	186,743μm^2 Φ500μm	7,746μm^2	
	II-1mmA	1,020,703 μm^2	10μm	3	30μm	769,396μm^2 Φ1mm	79,366μm^2	
	II-30C	8,171μm^2	6μm	3	18μm	707μm^2 Φ30μm	1,625μm^2	Off-mesa
	II-50C	12,868μm^2	6μm	3	18μm	1,963μm^2 Φ50μm	3,007μm^2	
	II-100C	24,328μm^2	6μm	3	30μm	7,850μm^2 Φ100μm	7,854μm^2	
	II-Test	7,529μm^2	6μm	3	30μm	707μm^2 Φ30μm	1,298μm^2	On-mesa

2.2.3 Executive Summary of Mask Design

Two sets of masks are designed for SiC SPAD fabrication. For better comparison, the mesa area as a function of optical window is shown in Fig. II-15. The on-mesa type devices in Mask-II (triangles) has similar mesa area as the devices in Mask-I (black squares) but are capable of a bevel structure. The off-mesa type devices in Mask-II (circle) apparently have a smaller mesa area thus tend to have lower dark count rate. The Ohmic contact area as a function of optical window area is shown in Fig. II-16. The off-mesa type has 1/3 to 2/3 of Ohmic contact area in comparison to an on-mesa device. Thus they have higher requirement on Ohmic contact. The small testing diode has a smaller area than the regular type and thus has better chance for a lower DCR.

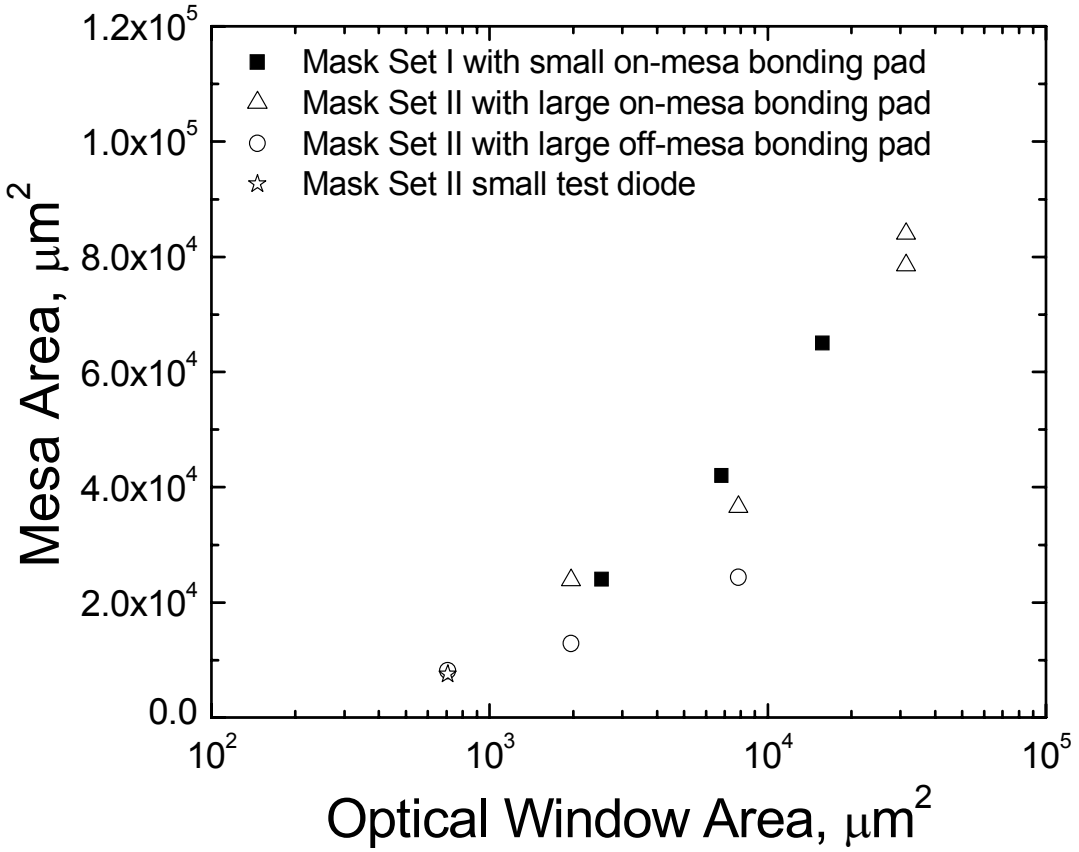


Fig. II-15 Comparison of mesa area as a function of the optical window for Mask-I and Mask-II.

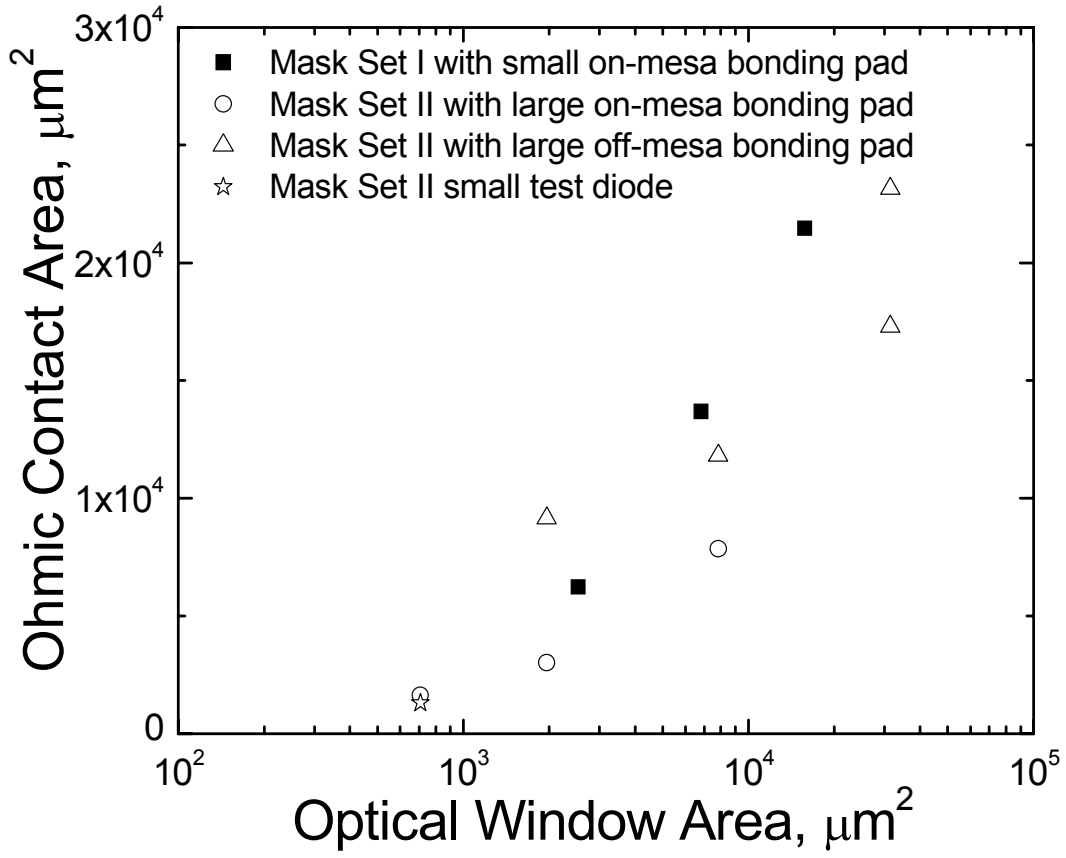


Fig. II-16 Comparison of Ohmic contact area as a function of optical window area for Mask-I and Mask-II.

III. PROCESSING TECHNOLOGY STUDY

3.1 Study of Edge Termination Technologies

4H-SiC has a high critical field >2.0MV/cm. Since a low operating voltage (<200V) is desired for SiC SPADs, the critical field is usually 3.2MV/cm~4.7MV/cm, depending on the wafer epi layer structure which will be detailed in the later sections. As a result of the high critical field, the edge termination is the most critical technology for a successful SPAD. Any edge breakdown will completely disable the devices and the SPAD will provide no gain. For power devices, many edge termination technologies are widely used, including planar junction terminations, floating field rings, field plates, etch contour and surface implantation (including resurf), bevel, and multiple junction edge terminations (MJTE) , etc. Among them, the positive bevel and MJTE turn out to be the best for SiC SPADs as they are able to ensure 100% bulk breakdown. In this section, study on improving these two technologies for SPAD fabrication is discussed.

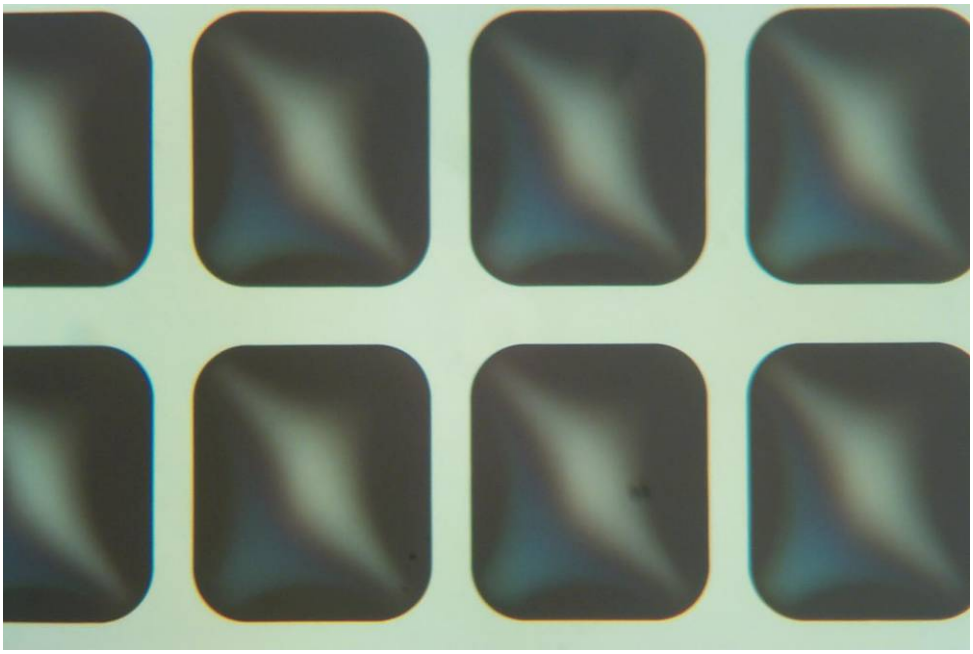
3.1.1 Bevel Edge Termination Technology

4H-SiC bevel etching is first developed by Dr. Feng Yan during his development of the first SiC APD. The concept is first to create a photoresist bevel by high temperature baking, then to harden the photoresist by electron beam curing (as shown in Fig. III-1), and finally to transfer the photoresist bevel to SiC bevel by using ICP etching. The etching gas is usually O_2-CF_4 mixture in our lab. With increasing of the CF_4 concentration, the etching ratio of photoresist to SiC will be decreased, which is preferred as there will be less damage on photoresist and it will lead to a smooth surface. However, with low O_2 concentration, for the Unaxis ICP machine, the chance of polymer formation is greatly increased. These polymers,

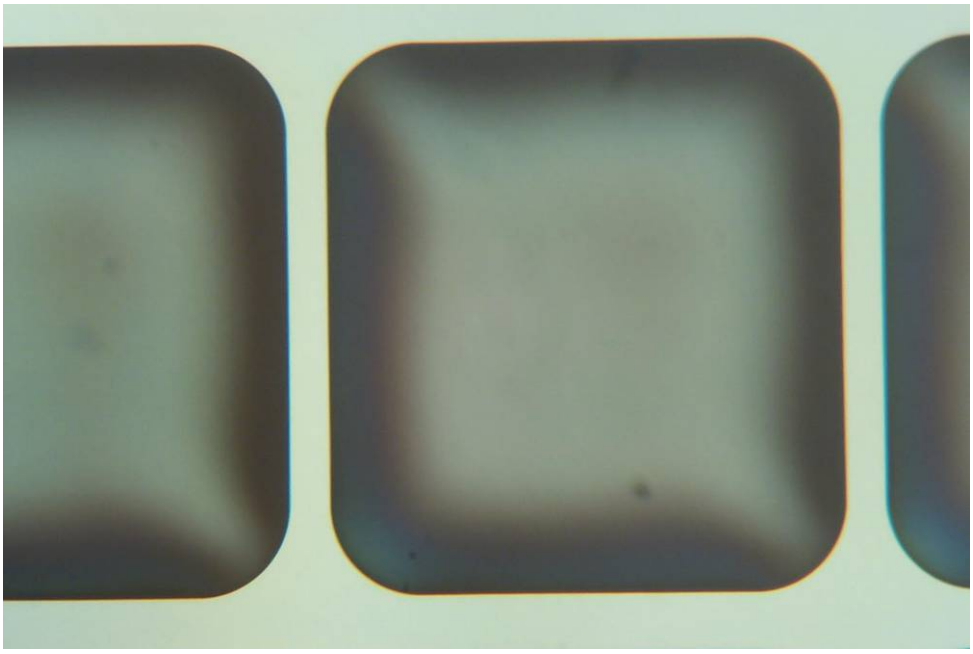
once formed by plasma, function as very tough micro etching masks and will lead to a very rough SiC surface. The possible reasons of polymer formation include the presence of Fluoride-based chemicals and gases (such as CF_4 or SF_6) and the presence of carbon. Unfortunately, a large quantity of carbon atoms (in photoresist and CF_4 molecules and SiC) exists in our ICP etching. The polymer problem becomes more and more serious after several years of usage, until a previous Ph.D. student (Dr. Kiyoshi Tone) did some studies and discovered that a high concentration of oxygen will help to eliminate polymers in most of the cases. Apparently that the polymer formation is related to chamber condition, but reasons and mechanisms are still not clear. This high oxygen concentration, however, becomes the biggest problems for SiC bevel etching. For example, by using such an etching recipe of

CF_4=20sccm, O_2=10sccm, Power=700W, Voltage=50V, Pressure=7mTorr,

the photoresist to bevel etching ratio is about 15:1 as shown in Fig. III-2. It can be seen that the top part of the bevel already becomes rough, where the photoresist is significantly damaged by the oxygen plasma, the surface becomes rough and finally transfer to SiC bevel surface.

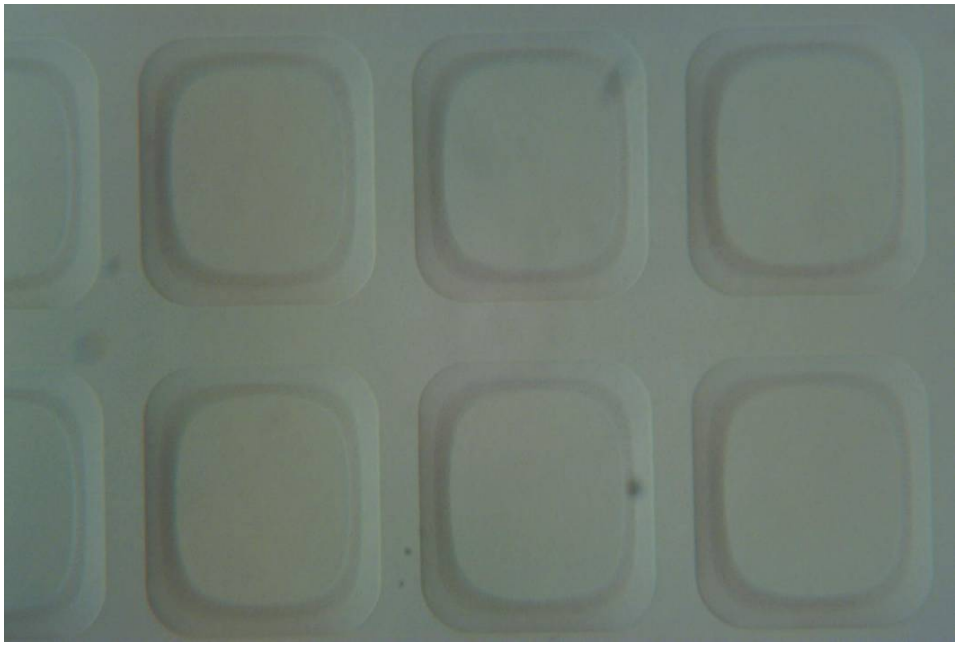


(a) Photoresist bevel for small 50um optical window devices

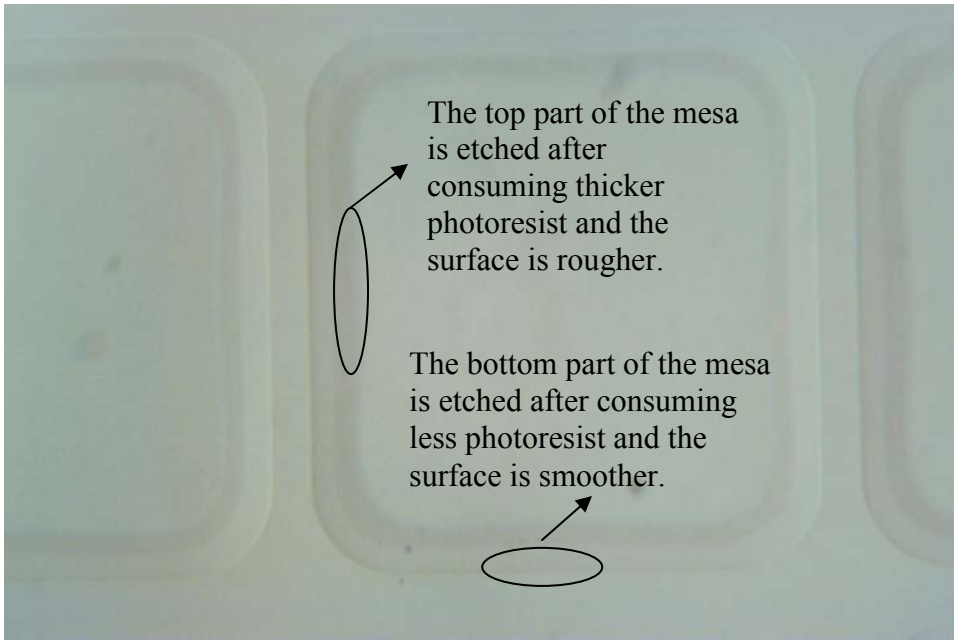


(b) Photoresist bevel for large 200um optical window devices

Fig. III-1 Photoresist after baking and e-beam curing for SiC bevel etching.



(a) SiC bevel for small 50um optical window devices



(b) SiC bevel for large 200um optical window devices

Fig. III-2 SiC bevel etching by using Unaxis ICP 790 system. The etching condition is 700W, 50V, O_2:CF_4=20:10, 7mTorr. The P.R. to SiC etching ratio is about 15:1. The total etching thickness is 0.65um.

The author has been struggling with the only ICP system (Unaxis) and the only available etching gases of O_2 and CF_4. One way to solve the problem is to eliminate the CF_4 and use chloride based gases such as BCl_3 or Cl_2. However, these gases are toxic and a load-lock has to be used. Rutgers SiCLAB placed an order in early 2006 for such a system but its shipment has been delayed repeatedly and it is still not delivered by the manufacturer at the writing of this thesis. One of the critical contributions of this thesis work to SiC SPAD fabrication comes from a well-known fact from PECVD dielectric film growth, but is always ignored by many people when doing ICP etching: substrate **temperature**. In PECVD system the substrate temperature is critical for the film growth rate. The higher of the substrate temperature, the higher of the growth rate and higher film density (thus the higher of the refraction index). It is very popular that the PECVD substrate is heated up to 250~300^{o}C for a reasonable growth rate and film quality. In the Unaxis ICP system, the substrate is gas (nitrogen) cooled, which does not provide enough cooling for high power high voltage SiC etching. The robust Si-C bond requires much higher etching power and voltage than Si-Si bond and the chamber substrate temperature increases dramatically after a few minutes of SiC etching. It is possible that the polymer formation is also related to the substrate temperature. Another ICP system (System A) is thus recommended and purchased by the collaborating company United Silicon Carbide, Inc., which is featured with a water-cooled substrate. With the water cooled ICP system, a polymer-free etching is achieved by using CF_4 only without any O_2. This becomes the biggest breakthrough in SiC bevel etching. The photoresist to SiC etching ratio is greatly reduced from 15:1 to 4.4:1, which allows significant less photoresist consumption for a given SiC etching depth. For the same etching thickness, the photoresist consumption is greatly reduced.

To make the system running smoothly, three major improvements are made before the final SiC SPAD is fabricated. The original condition is a-1 and b-1 (as detailed below), and later a-2 and b-2 improvements are made at the same time; and the last improvements are a-3 and b-3.

(a) The system originally comes with a gas tubing directly pointing to the sample and the strong gas flow blows away the sample (condition a-1). The gas tube is replaced with a ring-type gas tube but it becomes a perfect ground to the plasma and causes the matching network unable to tune and finally burned several matching network (condition a-2). Eventually the gas tube is buried inside the chamber wall and it becomes not a problem for a stable plasma (condition a-3).

(b) The substrate is sitting in the middle (in terms of height) of the chamber and plasma generated on both the top side and the bottom side (condition b-1). The bottom-plasma causes unstable ICP plasma and finally damages the matching network. The substrate height is first reduced and a back cover is added to stop the back-plasma problem (condition b-2). However, the reducing of height causes the ICP plasma difficult to couple with the substrate RIE plasma, which delivers problems to SiC bevel etching in two aspects:

- The plasma is not stable and it is difficult to couple ICP plasma with the RIE plasma, especially for low bias voltage. High bias voltage could not be used as it causes SiC surface damage.
- Because the ICP plasma is significantly higher than the substrate, the SiC etching rate becomes very low. The ICP plasma is believed to be the major source of gas ionization and etching for SiC. When the substrate is sitting outside the ICP plasma, there are

fewer ions than the condition b-1. However, for photoresist, where both atoms and ions can etch it. So it almost maintains a same photoresist etching rate as before. As a result, the photoresist to SiC etching ratio degrades from the original 3:1 to 6:1 under the same condition of 700W, 50V, CF_4=40sccm, pressure=10mTorr. The 3:1 etching ratio gives mirror-like etching surface as shown in Fig. III-3. But it never reappears after the chamber is modified, which indicate that there are still rooms for research towards a lower ratio than the current 4.4:1.

To eliminate the above problems, a low-profile chamber is redesigned so that ICP plasma move downwards, and the substrate directly sitting in the middle of ICP plasma (condition b-3). The b-3 condition improves the SiC etching rate and slightly reduces photoresist to SiC etching ratio.

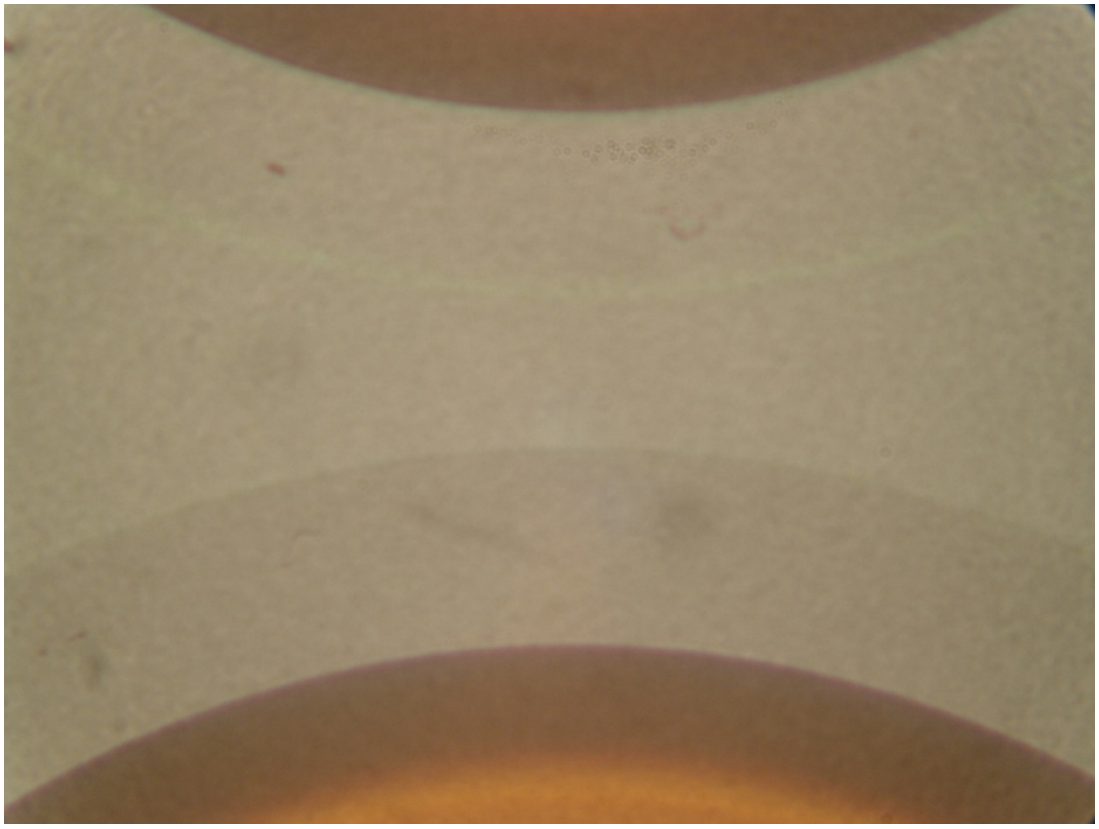


Fig. III-3 SiC bevel etching by the ICP system A with original machine configurations. The stage is high, the gas is provided right above the sample and there is no back-plasma stopper. It gives a photoresist to SiC etching ratio of 3:1, which is the lowest among all references.

From the improvements above, we are able to carefully exam the bevel etching conditions, not only from different recipes, but also from different plasma formation mechanisms. It is difficult to know the exact mechanism how SiC and photoresist is etched. Some efforts have been made through observing the radiation spectrum, but the spectrum can only reflect the "approximate" concentration of ionized components and etching products, it does not provide detailed information how the ions or atoms breaks the atomic bond and remove the atomic layers. From our experiments with different etching conditions above, it might be reasonable to assume that the most effective SiC etching compounds are "ions", while both ions and neutral atoms will etch photoresist. Based on this assumption, we may how the following recipe parameters affect the photoresist to SiC etching ratio:

a. Power: a higher power might reduce the ratio as it will help to ionize more atoms and leave fewer atoms in chamber. However, since we have chosen a high etching power (700W), there is not much room for a higher power for safety reasons.

b. Voltage: a strong voltage bias will increase the SiC etching rate. But the high energy bombardment is not preferred for detector purpose, since they cause SiC surface damage and increase the leakage current. A very low voltage will significantly reduce the SiC etching rate but might not change the photoresist etching as significantly. Thus there will be an optimum condition for SiC bevel etching.

c. Pressure: a low pressure will increase the ion concentration and might improve the ratio. However, the lowest possible pressure is limited by the ICP machine since the original 10mTorr or 7mTorr is not high.

d. Gas flow: a low gas flow will increase the ion concentration and might improve the ratio. Again, the lowest possible gas flow rate is limited by the corresponding mass flow controller of the machine.

After all the improvements have been done, a detailed bevel etching study is carried out and the results are listed in Table III-1, which basically confirm the assumptions above. The etching time is chosen so that SiC etching depth is about 1μm, which gives us the best evaluating the etched SiC surface quality.

a. There are no significant differences on photoresist to SiC etching ratio for power 600W, 700W and 800W (condition ID 3, 5, 6).

b. Voltage: the low voltage slightly increases the etching ratio from 5.0 (at 25V) to 6.0 (at 50V). This corresponds to condition ID 7, 8, and 9. The 100V is also tested but all the photo resist are etched away and the ratio is >1:6.5.

c. Pressure: When the gas flow rate is 5sccm and the pressure is reduced from 10mTorr to 3mTorr, the ratio is slightly reduced (condition ID 3 and 4). As the machine minimum resolution of pressure is 1mTorr, it is difficult to maintain a stable a 3mTorr pressure. Thus a 5mTorr pressure is recommended. There are little differences for 5mTorr and 10mTorr, however, when the gas flow rate reduced from 5sccm to 3sccm. Actually at this gas flow rate, it is not easy for the machine to maintain 10mTorr, as the main valve is only $<8^{o}$ open (almost closed).

d. Gas flow rate: The gas flow rate has relatively large effect on the ratio. When reducing the gas flow rate from 40sccm to 3sccm, the ratio changed from 1:6.6 to 1:4.4, with the pressure of 10mTorr. When reducing the pressure from 10mTorr to 5mTorr

with 3sccm flow rate, the ratio keeps almost no change, indicating most of the gases are ionized.

e. Substrate temperature: with water cooling, we are able to test the etching with different substrate temperature. It is known that with high substrate temperature, the etching rate will increase. However, it is not known if the ratio changes and how it will change with substrate temperature. The author tests the substrate temperature at 15^{o}C, 21.5^{o}C and 30^{o}C (condition ID 2, 3, 9 for gas flow rate of 5sccm and condition ID 12, 15 for gas flow rate of 3sccm). When the gas flow rate is 5sccm, the ratio is high when the substrate temperature is 15^{o}C and the ratio does not show significant change when the temperature is 21.5^{o}C and 30^{o}C. When the gas flow rate is 3sccm, it seems that increase the substrate temperature degrade the P.R. to SiC etching ratio (ratio becomes larger). How the temperature affects the etching ratio is still not clear. A larger temperature range might be needed for further research. It is not recommended to use temperature less than the cleanroom temperature to prevent moisture condensing on the substrate surface.

f. High temperature re-baking of photoresist: High temperature baking might change the photoresist shape and bevel angle. So the author tests a re-baking of photoresist after e-beam curing when the photo resist is already hard. The shape of the photoresist does not change when baking at higher temperature. However, the etching ratio seems to be higher. The mechanism is not clear. Probably the tension of reshape still remains and causes some damage in photoresist.

All the etched SiC surfaces look similar under microscope (Fig. III-4).

Table III-1 SiC ICP etching test on ICP system A.

(a) P.R. all gone after etching and the SiC surface has dots.
(b)The lowest possible flow rate is 3sccm. The plasma is not stable when flow rate is 2sccm.
(c) Sample is additional baked after E-beam curing at 190°C for 3 hours.

ID	ICP Etching Conditions					Etch Time (min)	SiC Etch Rate (A/min)	PR Etch Rate (A/min)	PR:SiC Ratio	SiC Etch Depth (μm)	Note Fig.# In Fig. III-4
	Pwr (W)	Bias (V)	CF_4 (sccm)	P (mTorr)	Sub Tem (°C)						
1	700	50	40	10	21.5	20	560	≥3680	≤6.6:1	1.12	Fig.(b)
2	700	50	5	10	21.5	20	730	≥3680	≤5:1	1.46	Fig.(c)
3	700	50	5	10	15.0	20	693	~4000	~5.7:1	1.39	Fig.(d)
4	700	50	5	3	21.5	15	812	4467	5.5:1	1.22	Fig.(e)
5	800	50	5	10	21.5	15	882	4667	5.3:1	1.32	Fig.(f)
6	600	50	5	10	21.5	20	615	3287	5.3:1	1.23	Fig.(g)
7	700	100	5	10	21.5	15	1362	N.A. (a)	>6.5:1	2.04	Dots(a) Fig.(h)
8	700	25	5	10	21.5	20	460	2800	6.0:1	0.92	Fig.(i)
9	700	50	5	10	30.0	20	810	~4000	~5:1	1.62	Fig.(j)
10	**700**	**50**	**3(b)**	**10**	**21.5**	**15**	**783**	**3467**	**4.4:1**	**1.18**	**Best(b) Fig.(k)**
11	700	50	3	15	21.5	18	747	4111	5.5:1	1.35	Fig.(l)
12	**700**	**50**	**3**	**5**	**21.5**	**15**	**834**	**3867**	**4.6:1**	**1.25**	**Best Fig.(m)**
13	700	50	3	5	21.5	15	826	4867	5.8:1	1.24	190°C(c) Fig. (o)
14	700	50	3	10	21.5	15	706	4733	6.7:1	1.07	190°C(c) Fig.(p)
15	700	50	3	5	30.0	14	843	4429	5.3:1	1.18	Fig.(q)

(a) Before etching

(b) Sample1 (40sccm)

(c)Sample 2 (5sccm)

(d) Sample 3 (15°C)

(e)Sample 4 (3mTorr)

(f) Sample 5 (800W)

(g) Sample 6 (600W)

(h) Sample 7 (100V)

(i) Sample 8 (25V)

(j) Sample 9 (30°C)

(k) Sample 10 (3sccm)

(l) Sample 11 (15mTorr)

(m)Sample 12 (5mTorr 3Sccm)

(n) 190°C Re-baked Sample

(o) Sample 13 (190°C 5mTorr 3sccm)

(p) Sample 14 (190°C 10mTorr 3sccm)

(q) Sample 15 (30°C 5mTorr

Fig. III-4 SiC etching by ICP system A with the final machine configuration. Different conditions are tested as illustrated in Table II-1.

3.1.2 Multiple Junction Edge Termination (MJTE) Technology

Multiple Junction Edge Termination (MJTE) is widely used in power device fabrication with ion-implanted or p-type epitaxial layer doped in $10^{17}cm^{-3}$ range. The structure usually comes with a very thick n- drift layer. The multiple junctions allow variation tolerances due to epitaxial or implantation growth and etching. The implanted/epitaxial layer thickness, doping, etching depth and oxidation consumptions all contribute uncertainties. First one needs to prepare a control sample cut from the real sample. With progressive etching of JTE1 step h (as illustrated in Fig. III-5 where a three-step MJTE is shown), when the optimum etching depth of h_{opt} is reached, the breakdown voltage of the testing diode will be the highest. Later, , the real sample JTE1 will be etched to h_{opt}-h_{ox} where h_{ox} is the oxidation margin. The method is very effective when applied to power devices with implanted p layer. However, it has to be modified when used on detector fabrication.

For SPADs, the leakage current is required to be 10^{6}~10^{12} times lower than a power device. Thus epitaxial layer is used for the detectors which typically give much lower leakage current than implanted diodes. It is not only the breakdown voltage itself but also the leakage current level which is important to SPADs. At a leakage current level of 1pA of less, surface morphology becomes an important factor which sometimes determines the leakage current level. Moistures and etching conditions will significantly affect the leakage current and one might miss the optimum condition and make wrong judgment. Moreover, with progressive etching of JTE1, before reaching the optimum condition, surface breakdown always happens during the testing which causes damages. With additional etching, usually the surface cannot be fully recovered from previous damages unless a very deep etching is done. However the large etching steps cannot be used for detectors fabrication. The

progressive etching depth is much shallower than a power device (only 1/5~1/10). It is partially because of the 5x~10x higher doping of p layer after considerations of limiting of light absorptions and requirement of low operating voltages. The other reason is detectors has much higher leakage current requirement and need accurate JTE etching depth. Since the device leakage current is different from device to device because of the defects, changing to another new device after a test will not lead to a reliable determination of h_{opt}. Thus, At least ten to twenty devices have to be included to ensure that statistically the leakage current reduction can be observed.

For detectors, the author makes the following modifications for MJTE SPAD fabrication in comparison to MJTE power devices and previous APD fabrication:

a. Metal masks instead of photoresist masks are used for all MJTE steps to avoid any possible surface roughness. In SiCLAB, for the power device the standard recipe always uses photoresist as mask for shallow SiC etching.

b. For detector, to reduce surface roughness, a shallow JTE is etched with metal as mask. Also, the JTE step is not as thick as the power device case (where 500Å is very popular), since the epi doping is higher and leakage current requirement is stringent. The JTE step thickness is usually chosen as 100~200ÅA for detector purpose, or even <100Å sometimes.

c. Multiple devices (typically in the order of 30) are tested after each etching step, including some new devices which have never been tested (thus never damaged). Sometimes the etched devices are not re-measured until several additional etching steps have been made and the surface is recovered.

It is obviously that MJTE fabrication is more complicated and time-consuming in processing than bevel edge terminations. It requires more masks, more fabrication steps and more time for measurement—all will introduce dusts and reduce the yield. All these problems might be overcome by using new testing structures, which will be discussed in the last chapter as a future work. It has to be emphasized that there are also many advantages on MJTE edge terminations:

- It has fewer requirements on etching systems than bevel structure. For example, the polymer is the biggest problem when using Freon based gases. And substrate cooling or toxic etching gases are needed for bevel.
- It is a clean processing. No photoresist related etchings are involved thus no concern of polymer formation.
- It allows more different epi-layer structures including very thick epi-layers where it is not easy to create bevels, which is a peculiar advantage.

A detailed MJTE optimization will be provided in following SPAD processing chapters.

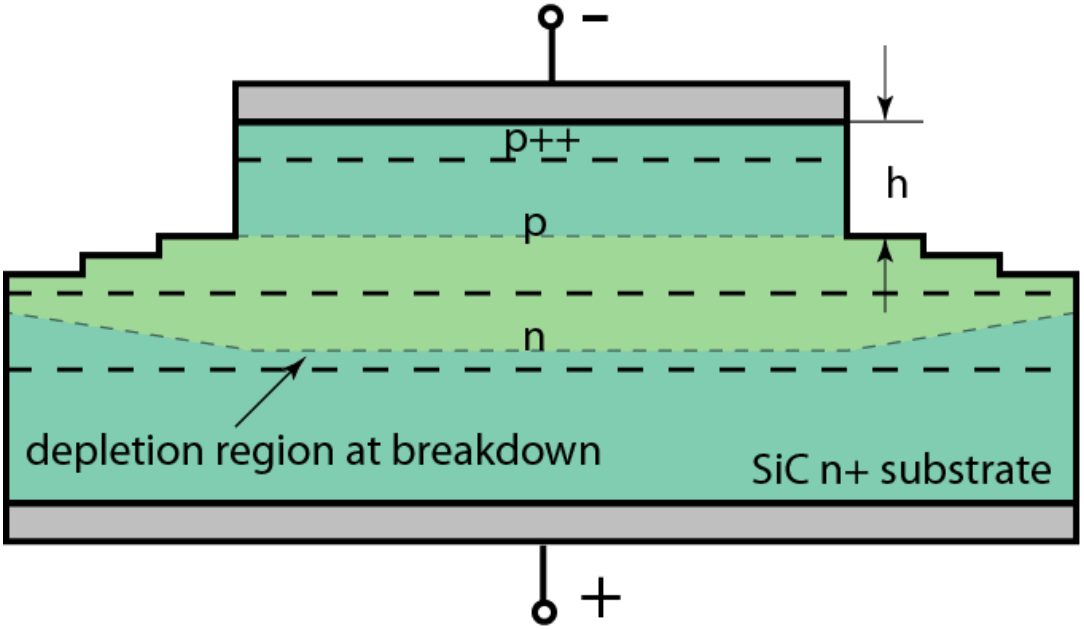


Fig. III-5 Illustration of MJTE optimization.

2.3.3 Comparison of Bevel and MJTE Edge Terminations

With the improved the water cooled ICP system A, we are able to compare the leakage current of devices made on the same wafer but with different edge termination. The two samples are processed simultaneously after the edge termination etching is made separately. The details of the processing are provided in the following chapters. The I-V measurements Fig. III-6 show negligible differences in leakage current, indicating both edge termination technologies are very effective for SiC SPAD fabrication.

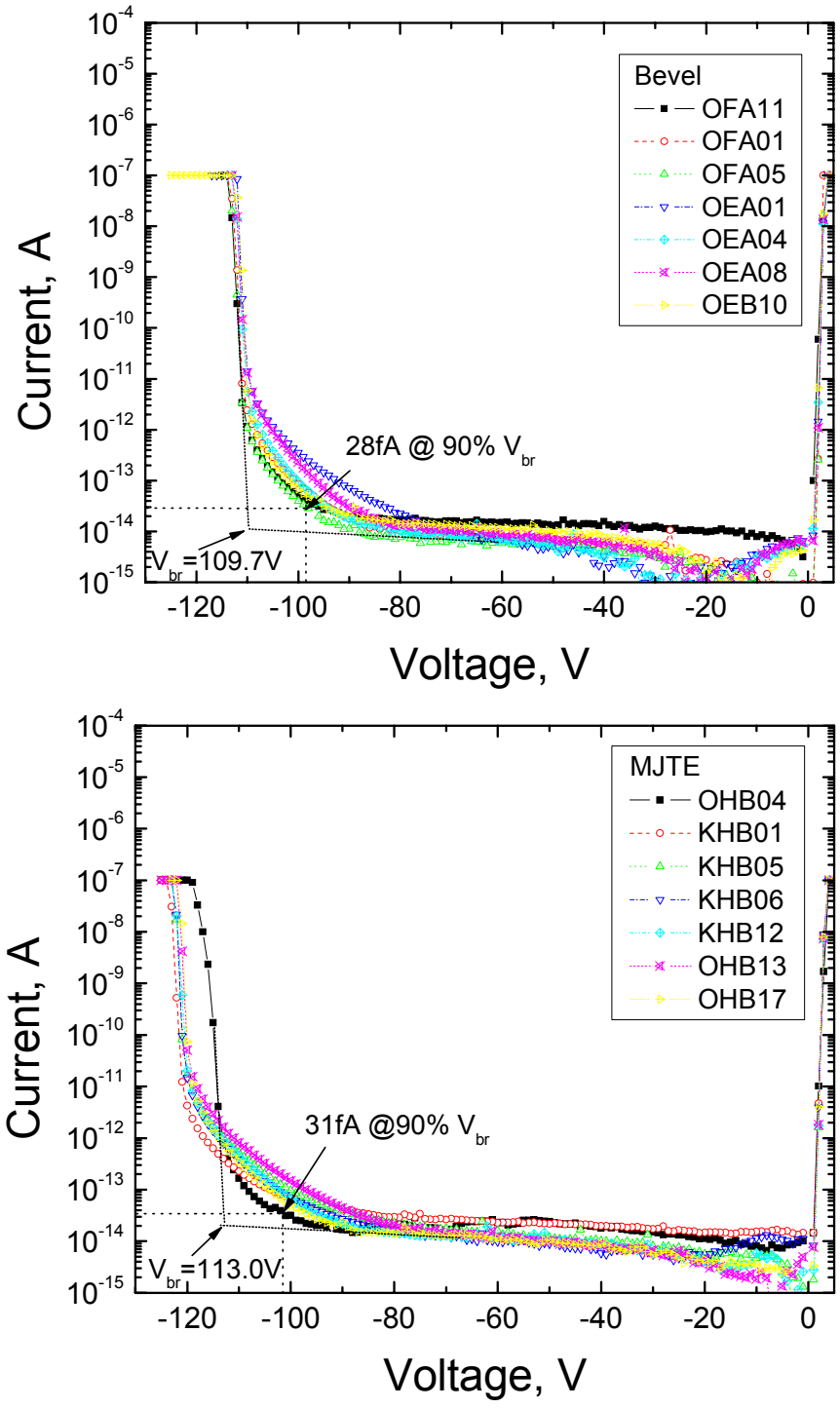


Fig. III-6 Comparison of samples with different edge terminations. The sample is processed at the same time after the edge termination is done for each sample.

3.2 P-Type Ohmic Contact Study

The fabricated SPADs have a vertical structure where the n-type substrate is used for the cathode. With the large area of the substrate and easy n-contact formation, the cathode Ohmic contact is usually not a problem. Indeed, the top p-type Ohmic contact is often the biggest concern because, a) the p doping could be as low as 5e18 cm^{-3}; b) the p-type Ohmic contact area is usually very small because of the limited mesa area for low dark count rage and need of area for optical window, especially for small area devices; and c) the top p++ layer thickness is usually ≤0.20μm for a high quantum efficiency, which gives limited thickness for metal silicide formation. A large contact resistance, as will be discussed later in the single photon measurement section, will cause self-quenching problem for the devices. The self-quenching problem will affect single photon counting with different quenching circuits since all quenching methods are based on passive quenching. The self-quenching will force the device to bias at a higher voltage for a reasonable signal voltage output and will lead to a higher dark count rate. Thus, a low p-contact resistance is critical to the performance of SPAD.

Cree, the largest SiC wafer supplier, as well as many other SiC wafter/epi growth companies and organizations, usually claims an achievable p-type epi layer doping ≥1e19cm^{-3}. However, the guarantee is set with an automated assumption of ±50% doping variations. Our SIMS results shows that the p-type doping varies from 6e18cm^{-3} (as the CM serials wafers purchased on year 2006) to 2e20cm^{-3}. In this section we will present a detailed study of p-type Ohmic contact for APDs and PiN detectors.

Four different metal combinations are studied: 1) Ti/TiN or Ti/TiW; 2) Ni/TiN or Ni/TiW; 3) Ni/AlTi/Ni/Pt or Ni/AlTi/Ni/TiW; and 4) Ni/Ti/AlTi/Ti/AlTi/TiN. All contact

metals are covered by an inner metal layer to prevent oxidations during high temperature annealing, such as TiW, TiN or even Pt. Other than the metal configurations, another important factor is the annealing temperature.

To determine the specific resistance, TLM patterns are designed in the streets of the masks. An example of the TLM pattern measurement results are shown in Fig. III-7 and Fig. III-8. The wafer for SiC particle detector based on APD structure has a 1e20cm^{-3} doped 0.5μm thick p++ layer. Ni/AlTi/Ni/TiW (500A/400A/1500A/1500A) are used as the p-contact metal. Since the p++ layer is very thick, it is not a concern of the nickel silicides consumption in the p++ layer. Annealing in Ar-H_2 (95%-5%) at four different temperatures is tested: 950^{o}C, 900^{o}C, 850^{o}C and 800^{o}C as shown in Table III-2. It can be seen that with decreasing the annealing temperature the specific contact resistance also decreases from 8.5e-5 Ωcm^2 to 2.6e-5 Ωcm^2, which is consistent with previous research on nickel based p-type Ohmic contact.

Table III-3 summarizes the specific contact resistance with different p-contact metals.

Table III-2 Ni/AlTi/Ni/TiW Ohmic contact study for 1e20 p-epi. The TiW is used for: a. preventing oxidation during annealing. b. preventing oxidation and reaction during polyimide annealing. c. preventing oxidation during polyimide planarization by oxygen plasma. d. avoiding short-time HF side etching of metals during opening optical window.

Annealing Temp	Best Ohmic Contact (Ω cm^2)	Worst Ohmic Contact (Ω cm^2)	Average Ohmic Contact (Ω cm^2)
950^{o}C for 10min in Ar-H_2	2.2e-5	1.1e-4	8.7e-5
900^{o}C for 10min in Ar-H_2	6.5e-5	2.7e-4 (edge, not reliable)	6.5e-5
850^{o}C for 10min in Ar-H_2	1.8e-5	4.8e-5	3.0e-5
800^{o}C for 10min in Ar-H_2	5.6e-6 to1.0e-5 (edge, not reliable)	2.6e-5	2.6e-5

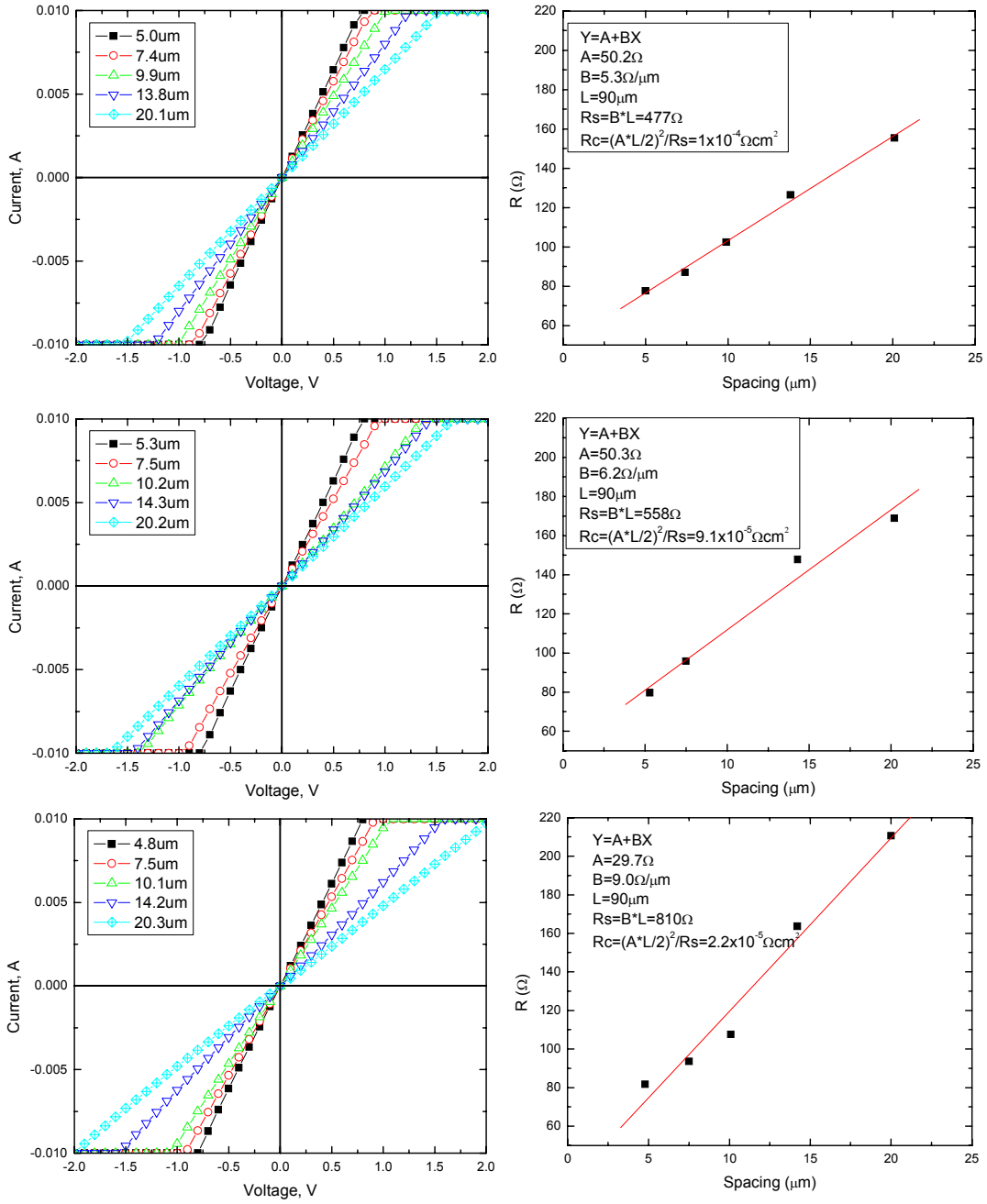


Fig. III-7 HK-BA after 950°C annealing in Ar-H_2 gas for 10min. P-metal: Ni/AlTi/Ni/TiW. The doping of the p-layer is 1e20cm^{-3}.

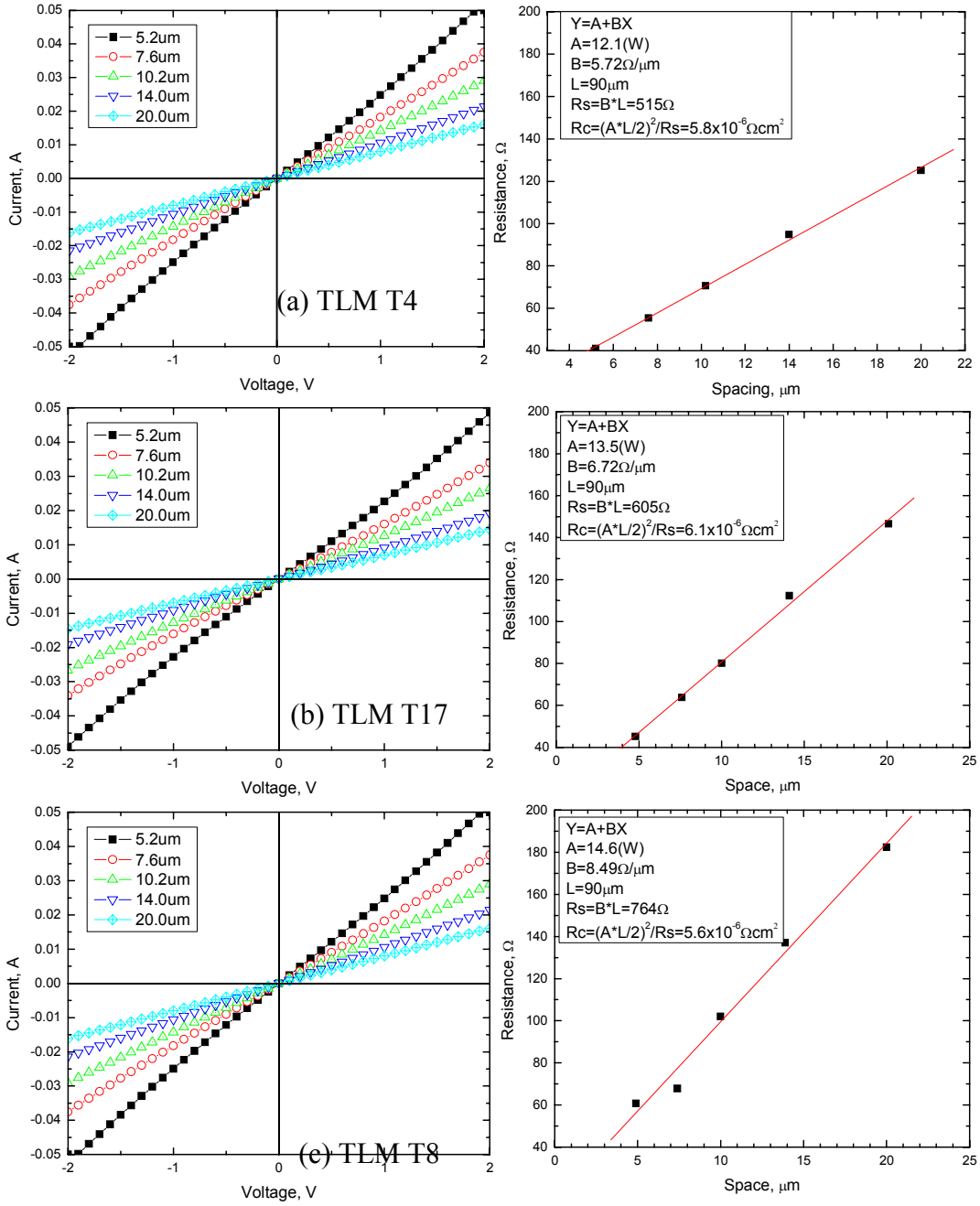


Fig. III-8 HK-BA after 800°C annealing in Ar-H_2 gas for 10min. P-metal: Ni/AlTi/Ni/TiW. The doping of the p-layer is 1e20cm^{-3}.

Table III-3 Summery of several Ohmic contact study on p-type SiC material.

ID	Year	P++ doping (cm^{-3})	Metal configuration (thickness in Å)	Annealing conditions (Gas: Ar-H_2)	Specific Contact Resistance ($10^{-5}\Omega\cdot cm^2$)			Device Type
					Best	Worst	Ave.	
DL	2005	9e19	Ti/TiN (800/1500)	900°C for 10min	No ohmic contact			SPAD
DL	2005	9e19	Ni/AlTi/Ni/TiW (500/400/1500/1500)	850°C for 10min	No ohmic contact, but have higher current than Ti/TiN at 2V			SPAD
HK	2005	1e20	Ni/AlTi/Ni/TiW (500/400/1500/1500)	950°C for 10min	2.2	11	8.7	Nuclear Particle
				900°C for 10min	6.5	27	6.5	
				850°C for 10min	1.8	4.8	3.0	
				800°C for 10min	<1.0	2.6	2.6	
AD	2007	2e19	Ni/AlTi/Ni/TiW (500/400/1500/1500)	800°C, 850°C, and 950°C 10min each	No Ohmic contact.			SPAD
			Ni/Ti/AlTi/Ti/AlTi/TiN (400A/100A/300A/100A/300A/1500A)	850°C 3min	Low $10^{-5}\Omega cm^{-2}$			
CM	2007	6e18	Ni/AlTi/Ni/TiW (500/400/1500/1500)	800°C, 850°C, 10min each	No Ohmic contact.			SPAD
			Ni/Ti/AlTi/Ti/AlTi/TiN (400A/100A/300A/100A/300A/1500A)	800°C 3min	Low $10e^{-4}\Omega cm^{-2}$			

Notes: All specific contact resistance is based on I-V measurement of TLM patterns at 0.5V, which might be different from some previous work which is at 2V. Sometimes the 0.5V determined specific resistance is 1~2 orders of magnitude higher than the 2V determined value.

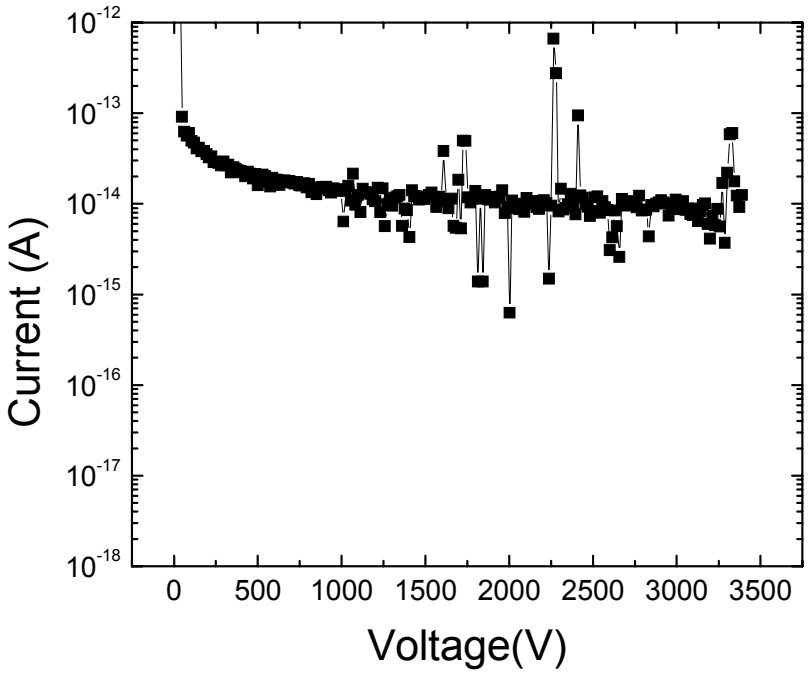
2.5 Characterization system setup

2.5.1 Dark Current and Gain Measurement

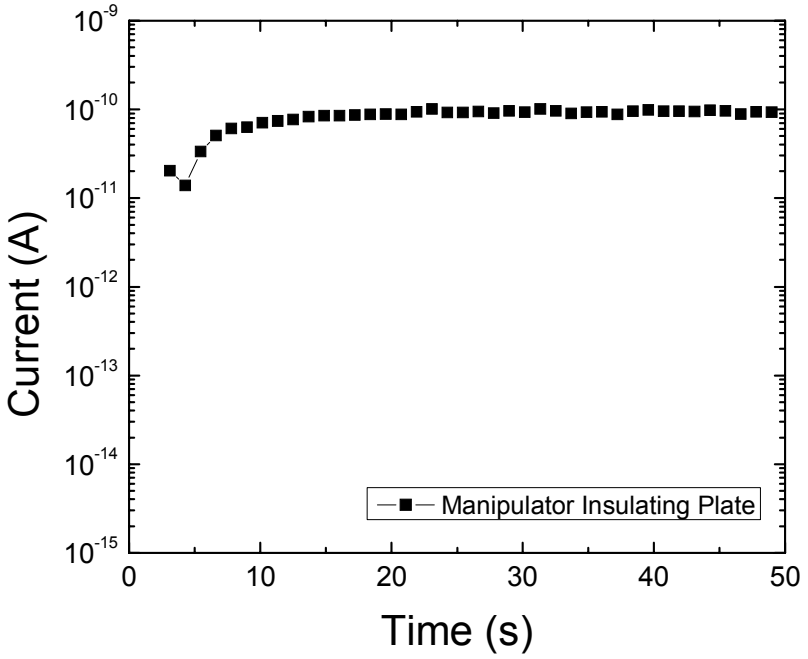
Usually the UV signals are very weak. For our UV system, after the fiber coupling, the UV light (200nm~400nm) typically generates a current of pA range in SiC SPADs at each wavelength out of the monochronometer. The photo current for wavelength below 270nm and above 380nm usually is less than 1pA for small devices. It is possible to replace current lamp with a more powerful UV lamp, but it will require water cooling and exhausting system to pump out the O_3 generated by high power UV light. Also for application, the UV signals are usually extremely weak. Thus, a fA measurement system is required for SPAD dark current and gain calibration.

Such a system is commercially available but very expensive. After doing some research, the author finds that only two materials are good insulating materials of fA measurement setup. One is Teflon (PTFE), and the other is sapphire. Both have a resistivity higher than $10^{18}\Omega$ cm. This is important as the SiC SPAD operating voltage is in the order of 100V~250V, to ensure a leakage current of <10fA, the isolation material must have a resistance higher than $10^{16}\Omega$. Sapphire is expensive and hard to machinery. The author finds some PTFE plate similar to the dimension of insulating plate used for our manipulators (1cm×2cm, 2mm thick). The plate is tested at high voltage of 400V and shows a leakage of 10fA (Fig. III-9), and later the author finds that the leakage happens on surface, not through the PTFE bulk. The test proves that the PTFE has no problem to block 400V with a leakage current in the noise level. The insulating plates used for our manipulator demonstrate a leakage current of 100pA. A design and photo of such a manipulator is shown in Fig. III-10.

Several important locations on the probe station are all insulated by Teflon. With Aluminum foil coated shielding box, the system is capable of measurement of sub-fA current.

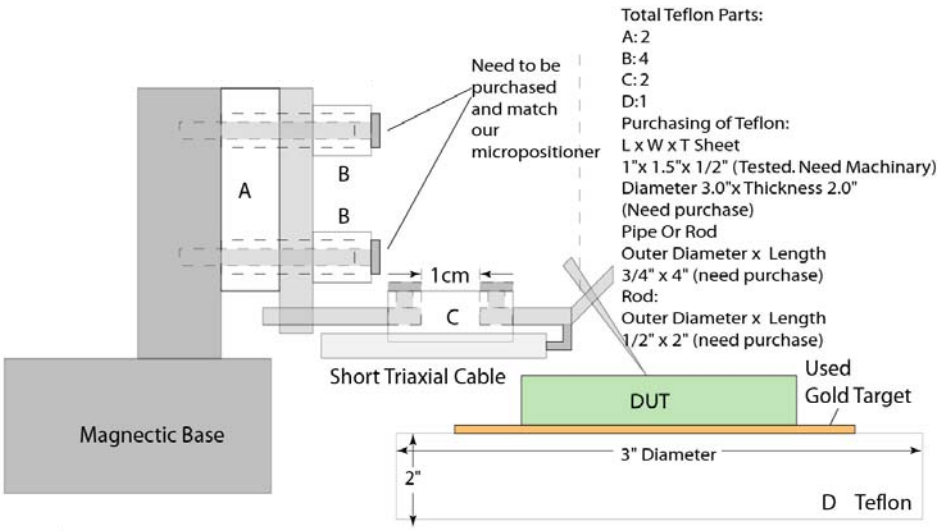


(a) Testing of a 2cm×1cm×2mm PTFE plate at 400V



(b) Testing of a 2cm×1cm×2mm insulating plate originally installed on our manipulators at 400V

Fig. III-9 Comparison of leakage current of a PTFE plate which has a similar size of the insulating plate originally installed on our manipulator.



Special Requirement:
A. All Teflon has to be Teflon PTFE, not other flouropolymers can be used.
B. All surfaces including interholes have to be polished. No rough surface anywhere.
C. All Teflon parts have to be able to disassembled so that we can clean them by Acid and Acetone.
D. The triaxial cable has to be short and low-noise.
E. For Teflon Part D, it needs to be flat and parallel --- none of the plate is flat when purchased, need machine work.

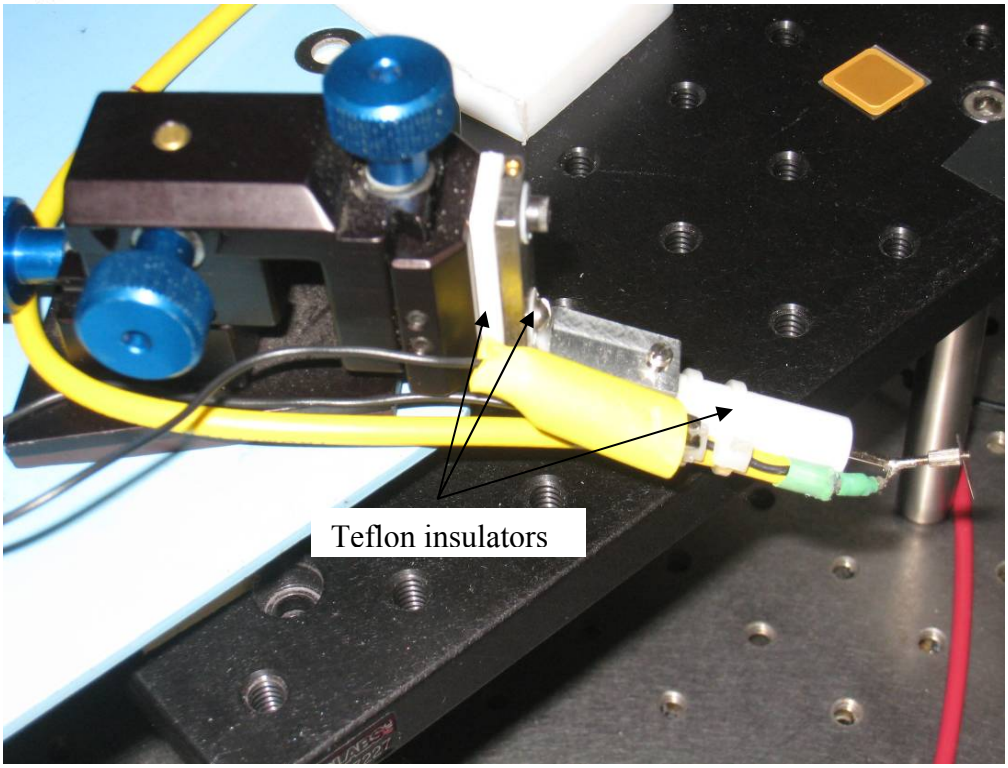


Fig. III-10 Design of a triaxial cable probe with PTFE Teflon insulating towards a fA range of measurement.

2.5.2 Quantum Efficiency Calibration

The original system for QE measurement is set up with mirrors, lens, lock-in amplifier, and preamplifier by Dr. Feng Yan, which is capable to couple strong UV lights into the detector. However, there are several drawbacks:

a. It takes several hours to have mirrors and lights properly coupling UV light to the detector. And the screws which are used to adjust and fix the mirrors and lens tend to move during such a long setup time. The light beam can move a drastic distance in comparison to the tiny SPAD dimensions. Once that happens, a new adjustment and light intensity calibration has to be made.

b. The lock-in amplifier depends on the researchers experiences to identify fake signals. Sometimes a wrong judgment could be made, especially when the signal is weak.

Collaborated with Dr. Feng Yan, the author revised the system with a Φ50μm core fiber (as illustrated in Fig. III-11). By the time of the SPAD work starts, the fiber-coupled QE measurement system is already set up for characterization of SiC detectors. Furthermore, the author made the following improvements for SPAD QE measurement:

a. A fiber with thicker core (500μm instead of 50μm in diameter) is used so that the light coupling to the device is better and the light uniformity is better. This is important for those wavelength with weak light intensity or weak photo response.

b. The measurement system is improved to a fA range measurement. The lock-in amplifier, preamplifier, and HP4145B is replaced with a Keithley 4200SCS. The

Keithley 4200SCS is not only capable of fA range measurement, but also capable of a high voltage measurement, up to +/-210V.

The modified system shown in Fig. III-12, not only has higher sensitivity in quantum efficiency measurement, but also has better data reliability, since the parts which can be shifted during measurement are greatly reduced.

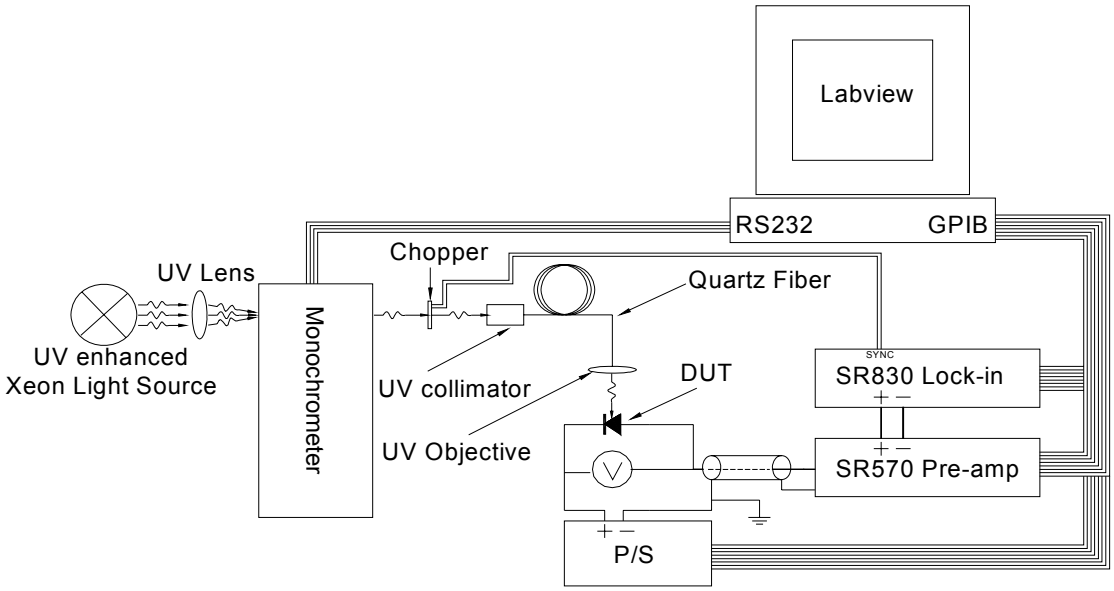


Fig. III-11 Original setup of quantum efficiency measurement.

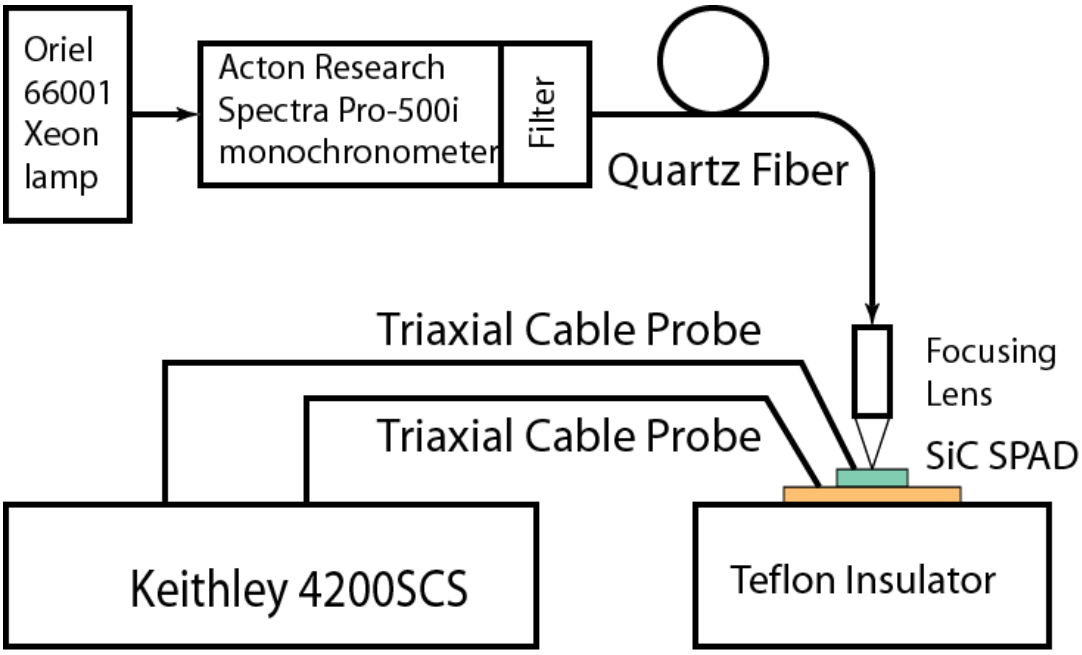


Fig. III-12 Measurement setup for quantum efficiency measurements

2.5.3 Single Photon Counting Measurement

Currently there are three quenching circuit commercially available for Si SPADs: passive, gate and active quenching circuit. However, at year 2002, when the thesis work starts, none of the quenching circuits can be purchased. To make things worse, the later developed commercial Si SPAD quenching circuits cannot be directly apply to SiC SPAD, since it requires higher excessive voltage and larger pulse height. The small Si SPADs (≤Φ30μm) can be biased significantly higher than the operating voltage without suffering a high dark count rate. For example, for a currently commercially available Si SPAD, the operating voltage could be as low as 30V. It can be biased at 35V and the dark count rate is still low (<1k). This is an important property for Si SPAD, as the device can be over biased at with a certain voltage (excessive voltage) which is large enough for a higher pulse height, and when the light is coming, the high photo current will generated a noticeable voltage drop on a large load resistor (>100k), then quench the device. For SiC, there is no such luck. The high electric field makes a much sharper avalanche breakdown in dark. Even with 0.5V excess voltage, the dark count rate increase dramatically. So for SiC SPAD, the voltage drop (pulse height) on the load resistor is smaller than the case of Si. To get a large enough pulse for commercial quenching circuit, an amplifier has to be used to boost the signal. Such an amplifier is not easy to made, as it requires: a. GHz operation, b. Low threshold, c. differential input to eliminate the noises (or has an adjustable low cut-off threshold).

To measure the single photon counting capability of a SiC SPAD, the author thus designs a simple but effective passive quenching circuit as shown in Fig. III-13. The load resistor is chosen as 200Ω. The avalanche current pulse will generate a small voltage drop on

the load resistor but large enough to quench the SiC SPAD. The voltage pulse is monitored and recorded by a fast oscilloscope. The signal is readout and analyzed by computers.

An experiment with different load resistor values have been made, which shows that 200Ω gives the best result. A smaller resistor will not generate enough voltage drops which can be distinguished from external noise level. A large resistor, however, tends to couple more noises and quench the SPAD even with small avalanche current pulse. The 200Ω turns out to be the best value at our lab conditions.

The light source for single photon counting is selected with UV LEDs. LEDs with two wavelengths 350nm and 280nm are purchased. The reason that Xeon UV lamp is not used for single photon counting is that its power supply generated too much noise to the passive quenching circuit, which shifts the base line of the oscilloscope by more than +/- 30mV. Also, the power supply for monochrome meter generates significant noise to the quenching circuit. LEDs, which can be driven with batteries, do not have this problem. The 350nm LED has strong light output around 350nm and has a long tail to 400nm. The light above 400nm could be removed by filter. The reason that a 350nm LED is chosen is that 350nm UV light has long penetration depth and it will help to identify the light absorption for a structure with thick absorption layer as will be discussed in the single photon counting chapter. The 280nm is a wavelength of interest. And a 280nm LED is also used for single photon counting measurement. The details of single photon counting measurement will be provided in chapter IV and V.

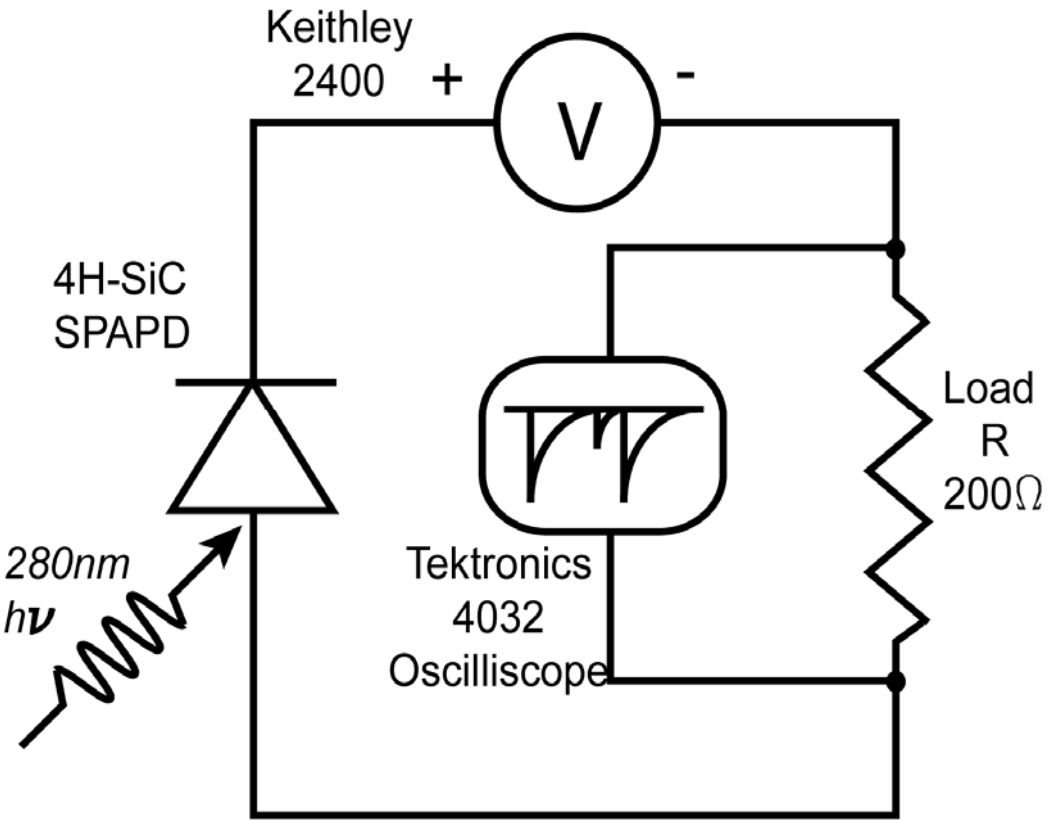


Fig. III-13 Passive quenching circuit for single photon counting measurement.

2.5.4 Temperature Dependence Measurement

In the previous SiC APD research by Dr. Feng Yan, a temperature setup using an electric oven has been setup. The setup, however, not only introduces a much higher electric noise, but also has a higher leakage path which makes it not suitable for single photon counting purpose. A new measurement is set up with TE cooler which has an area of 13mmx13mm. For many applications, a fan is used on the hot side to remove the heat so that the cold side could have lower temperature. For single photon counting, such a fan will generate too much noise and cannot be applied. A gigantic heat sink is thus used and the TE cooler is mounted on it with thermal paste. A thermal couple is also mounted on the top side of the TE cooler for temperature reading Fig. III-14. To prevent water condensation on sample surface, the entire probe station is purged with nitrogen.

It is important to know that the temperature on top of SiC sample is slightly different from the thermal couple reading on top of the TE cooler. The temperature difference depends on the measurement setup, sample size and the temperature range. If the one side of the TE cooler is significantly cooled, the sample surface temperature might be higher due to thermal conductivity, purging gas temperature, and sample size. Such a temperature differences, could be measured with a SiC similar size dummy sample with thermal couple mounted on top of it. Fig. III-15 shows when cooling down to freezing point, the sample surface temperature is about $2^{o}C$ higher than the temperature reading from the thermal couple mounted on TE cooler.

Breakdown voltage decreases with reducing of the temperature, which is a signature of avalanche breakdown. When studying the dark count rate temperature dependence, one has to realize the breakdown voltage shift as well. Fig. III-16 shows the setup for measuring

the breakdown voltage shifting with temperature and the measured result, and the Fig. III-17 shows the setup for dark count rate measurement with temperature dependence. The setup could be used for both low temperature (up to about -20^{o}C) and high temperature measurement (up to about +60^{o}C) with one stage of TE cooler. A wider temperature range is doable but it requires much larger current and cannot be driven by batteries. . Reducing temperature does not significantly reduce the dark current for a SiC SPAD. So, whether the cooling will suppress the dark count rate is an interesting topic.

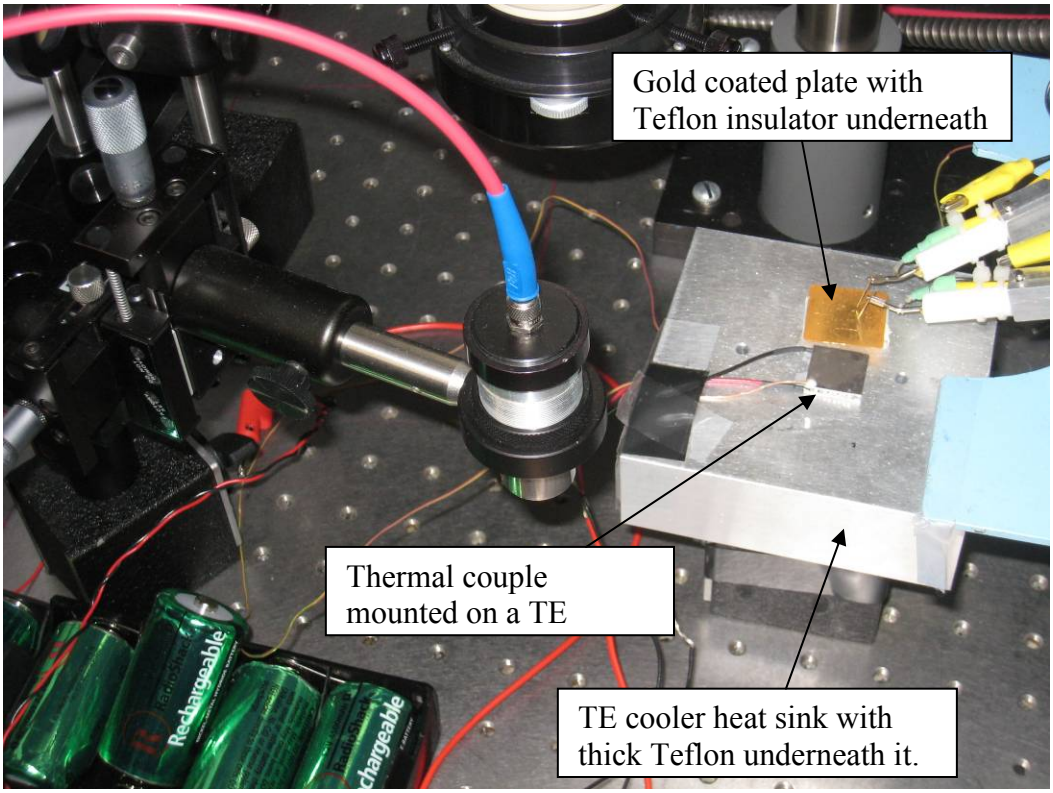


Fig. III-14 Temperature dependence setup for SiC SPAD single photon counting measurement.

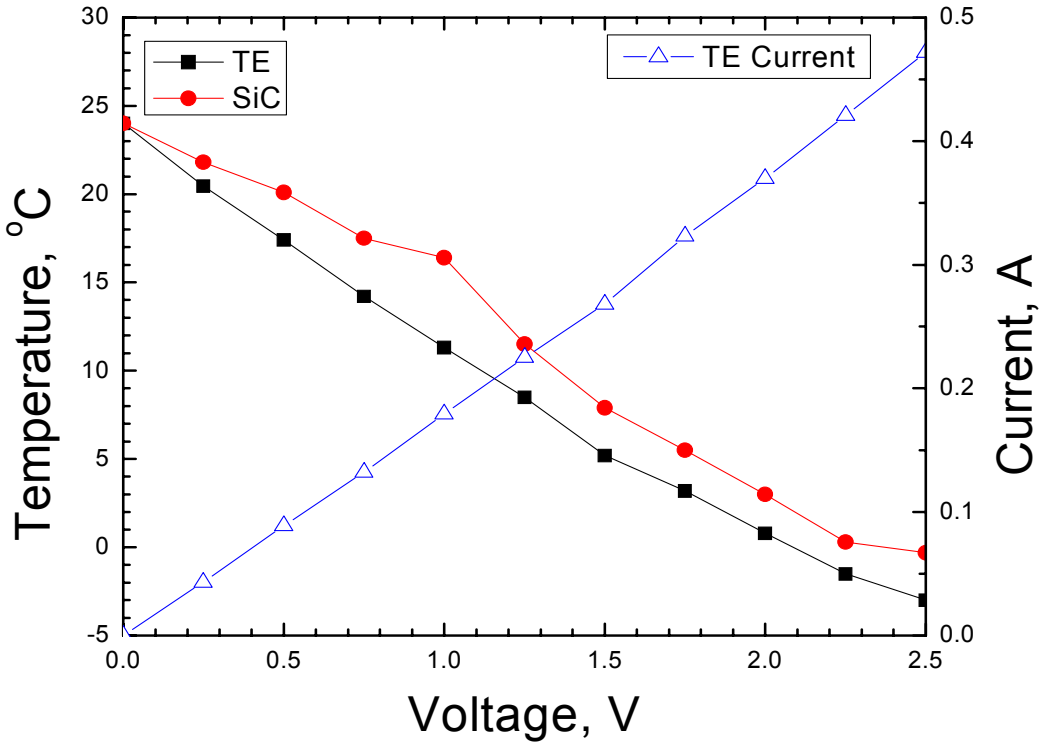


Fig. III-15 Melcor TE cooler testing with a 1.0×0.8cm^2 SiC sample. The temperature difference is 2°C~4°C between the TE cooler cool surface and the SiC top surface). The TE cooler could be driven by battery pack (2.5V or 3V, 500mA) to reduce the terrible noise from the voltage source.

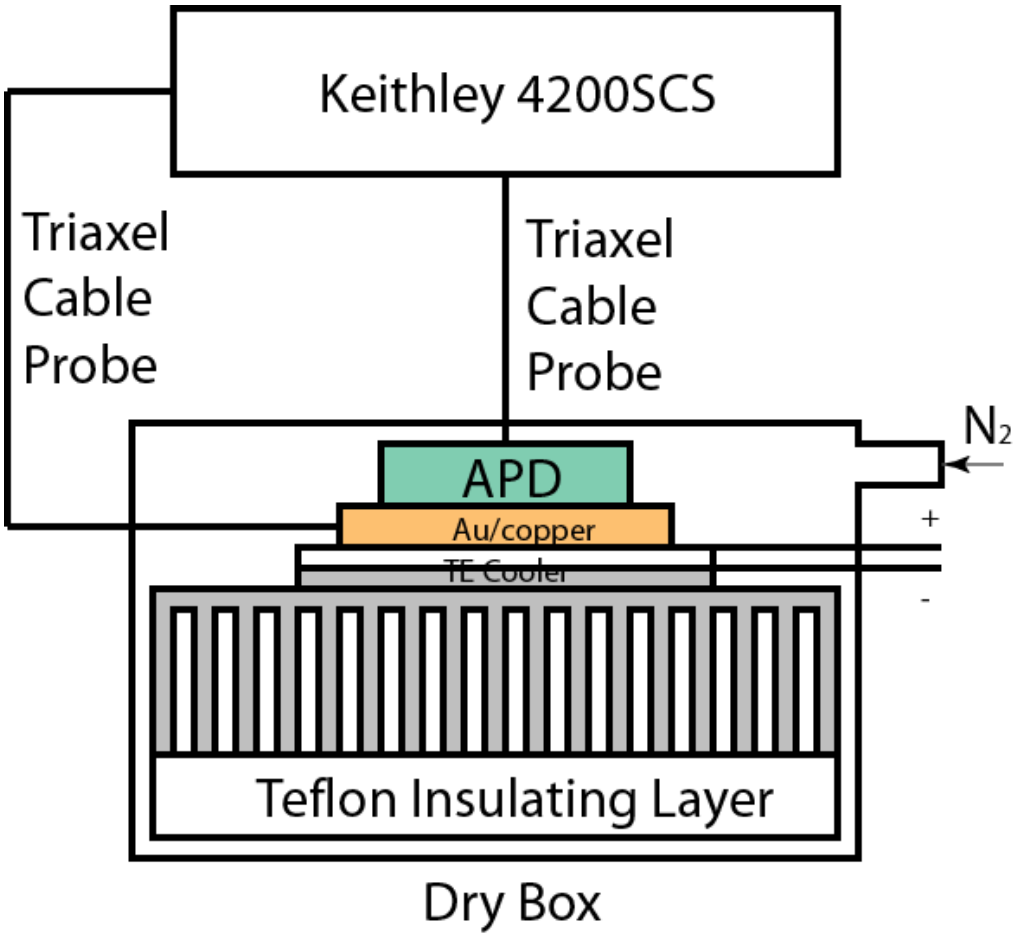


Fig. III-16 . Avalanche breakdown voltage temperature dependence measurement.

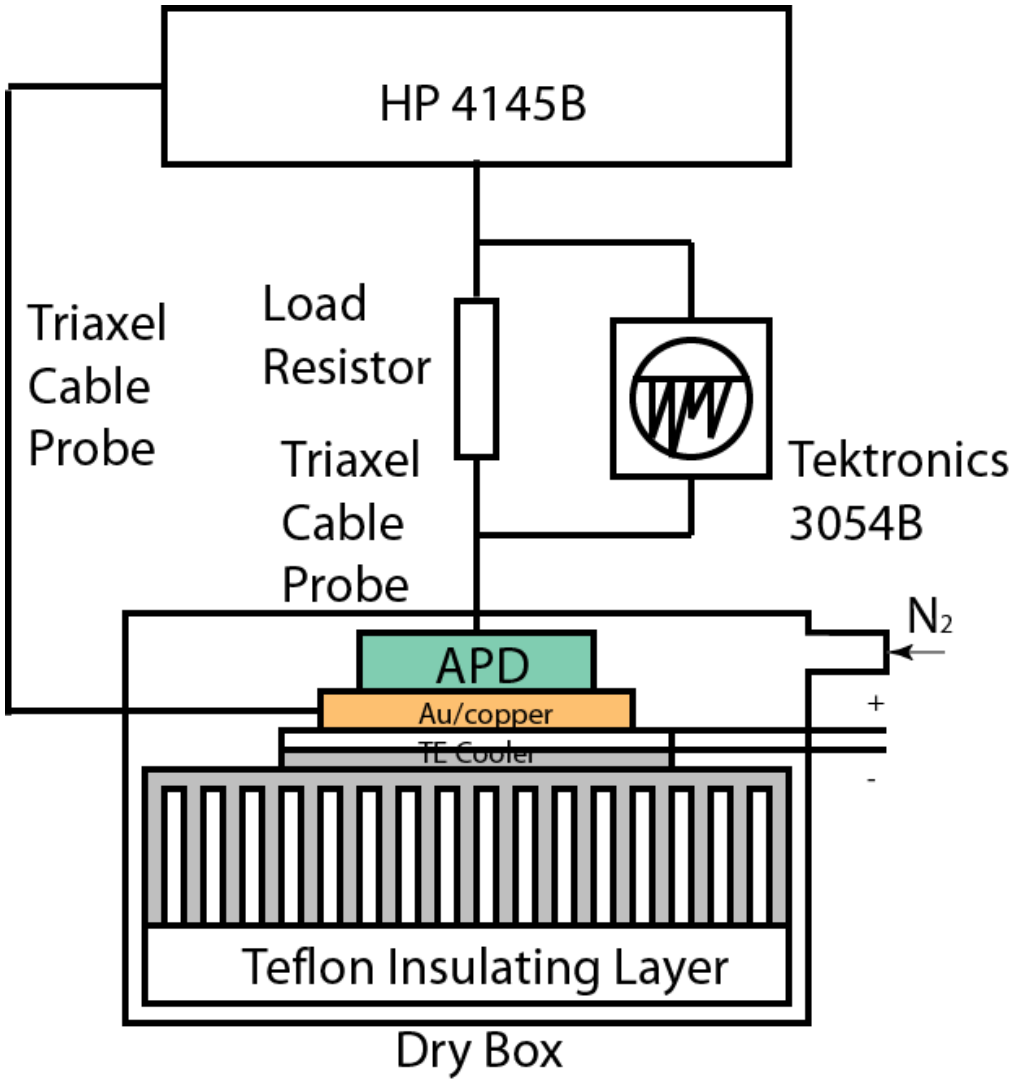


Fig. III-17 Dark count rate (DCR) measurement for Phase I samples with passive quenching circuit.

IV. PROCESSING AND CHARACTERIZATION OF THE WORLD'S FIRST 4H-SIC SPAD

4.1 Processing of FQ-C sample

The first SiC SPADs are made on wafer FQ. For the FQ-C sample, the mask set with two JTE steps is used. The wafer has a structure as shown in Fig. II-1. Since the p layer doping is as high as $2.4\times10^{18}cm^{-3}$, the depletion region in the p layer is only <1400Å. Thus a thin JTE step height is chosen as 300Å. The SIMS and simulation result shows the depletion region starts around 3000Å from the surface, and the electric field peaks at 4400Å where the p/n junction locates (Fig. II-2). It would be expected the optimum depth will be somewhere within 3000 Å ~4400 Å. A cross-sectional view for JTE1 optimization is shown in Fig. IV-1. Fig. IV-2 shows the I-V measurement for JTE1 optimization. As the leakage current is already low, the surface condition will significantly change the device I-V performance. Thus, using one single device is no longer reliable. Moreover, before reaching optimum condition, the breakdown might happen at surface and the I-V measurement will cause surface damage. Thus multiple devices are measured in six locations. And each time new devices which are never measured before are included for a more reliable result. The I-V measurement shows the following optimum depth at each location (the two I-V lines with minimum reverse leakage current):

Location A: 4000Å, 4200Å

Location B: 4000Å, 4200Å

Location C: 4000Å

Location D: 4000Å, 4200Å

Location E: 4000Å

Location F: 4200Å

Location G: 4000Å

Location H: No prediction.

So the optimum condition is determined as 4000Å. Considering the oxidation consumption, the optimum etching depth of the real sample is determined as 3800Å. Please note the there are also thickness measurement uncertainties, typically in the order of ±10~20%. In such a case, the best scenario for the real sample etching is to follow exactly the same etching sequence as the dummy sample except the last one or two etching step for a 200Å oxidation margin. All the testing and etching should be done within a few days so that the ICP chamber condition (especially the Si substrate condition) does not change much. The etching curve with etching time is shown in Fig. IV-3.

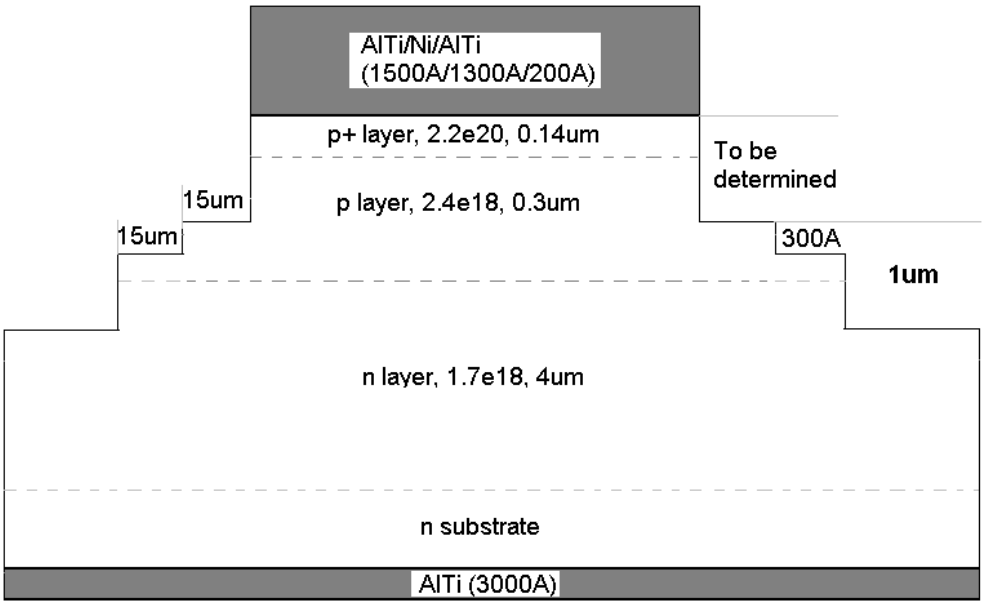


Fig. IV-1 Crosssection view of the MJTE APD structure.

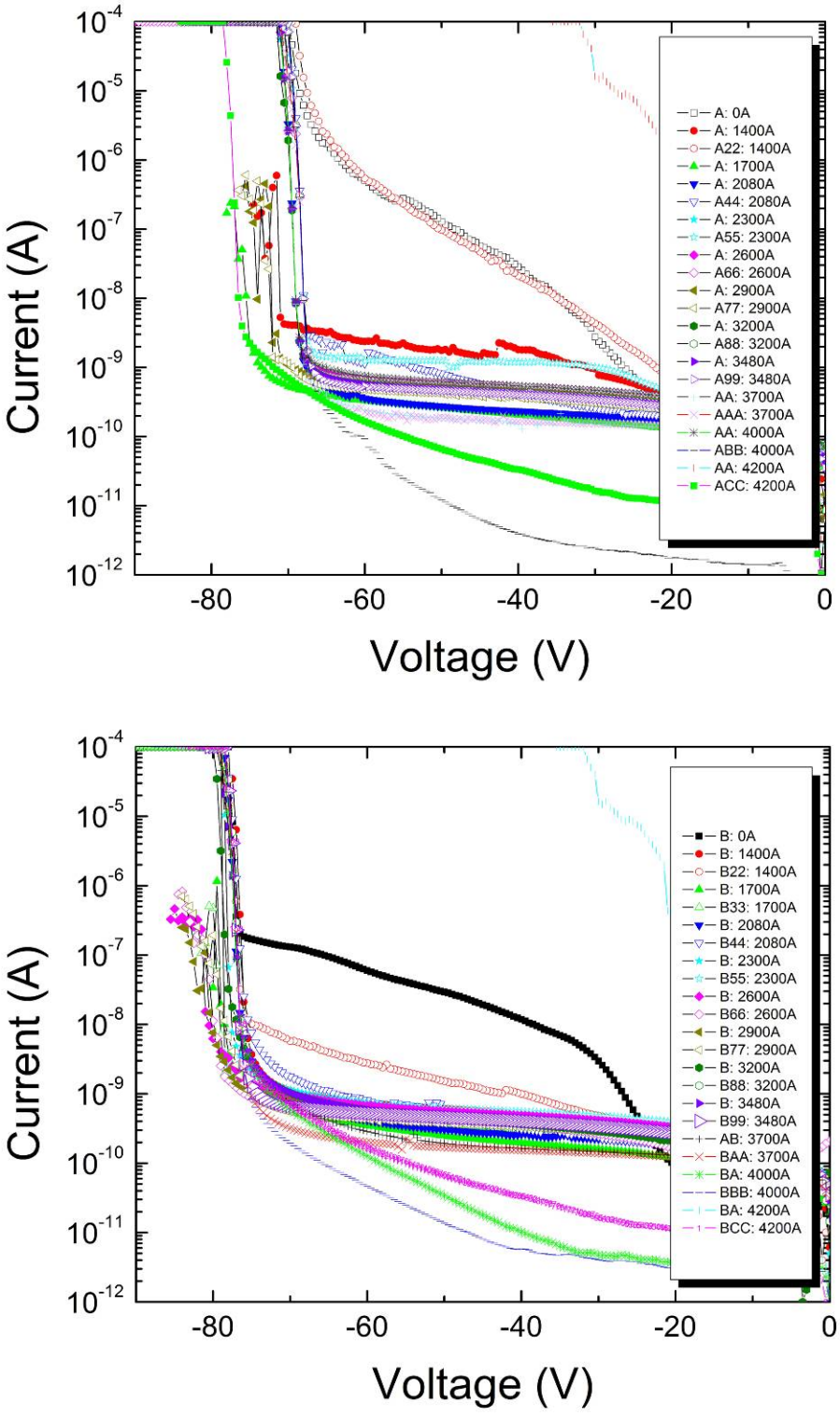
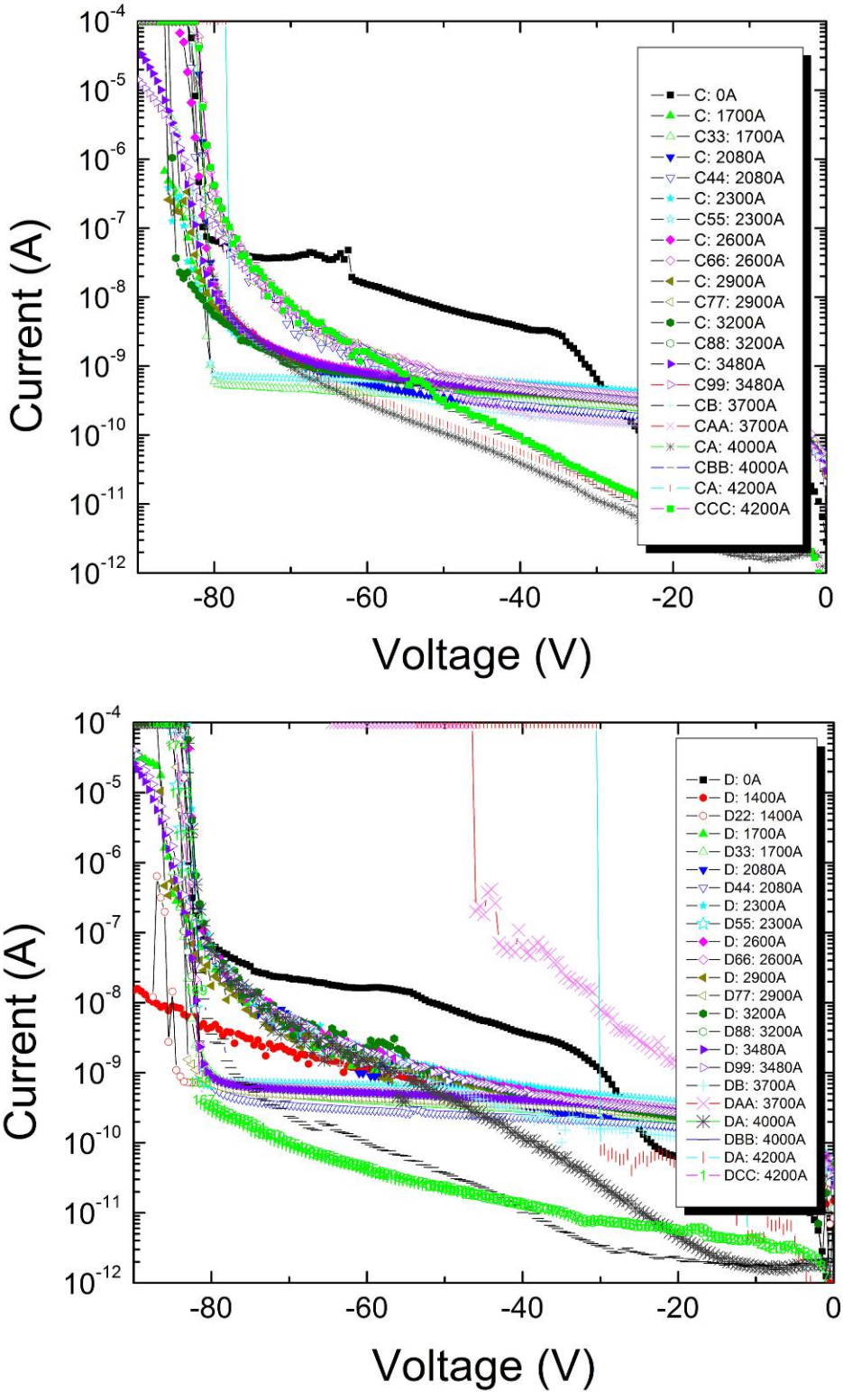
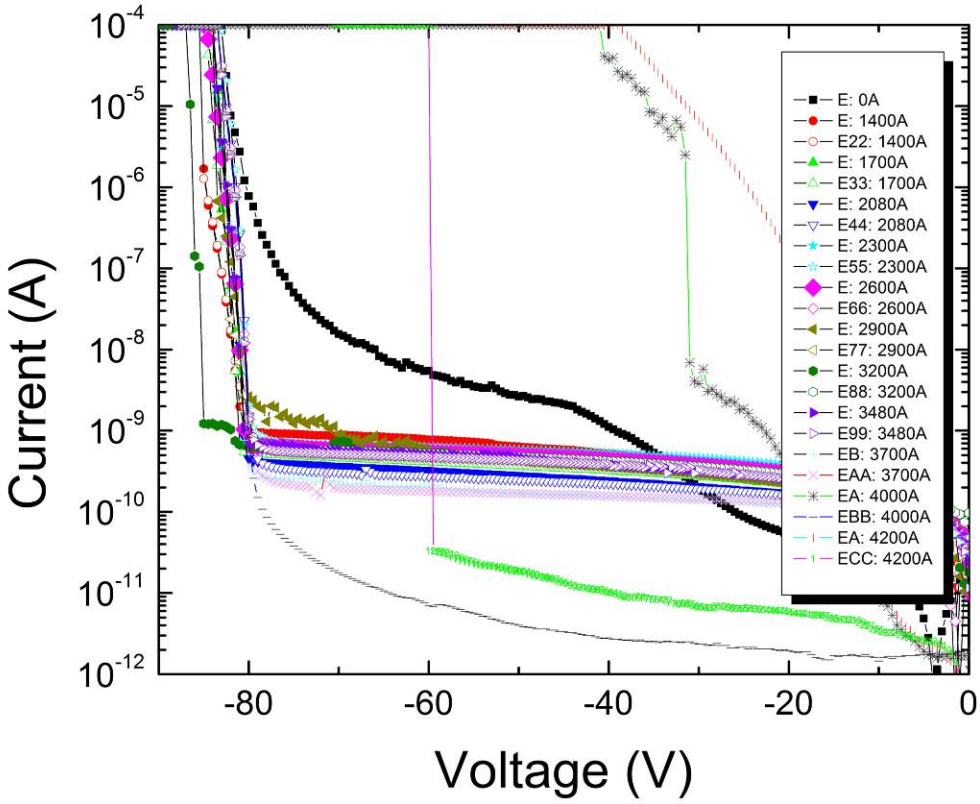
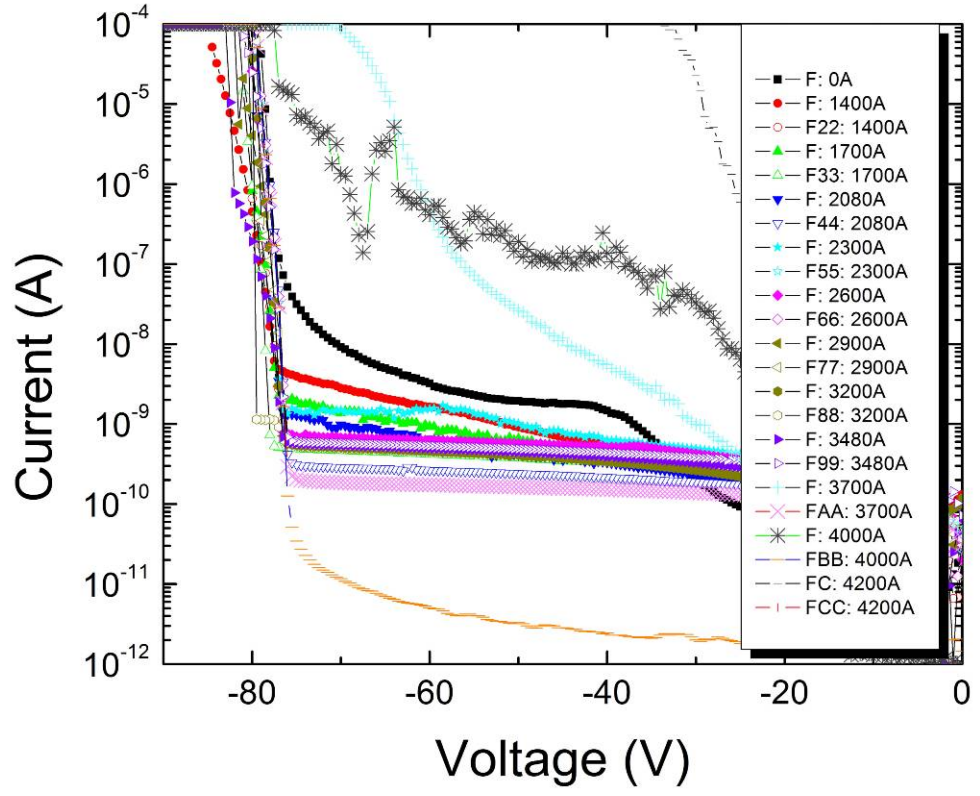


Fig. IV-2 JTE1 optimization for FQ-C sample. The measurement is made at six different locations, with multiple devices measured at each location. The above two figures shows location A and B. More figures continued in the following pages.

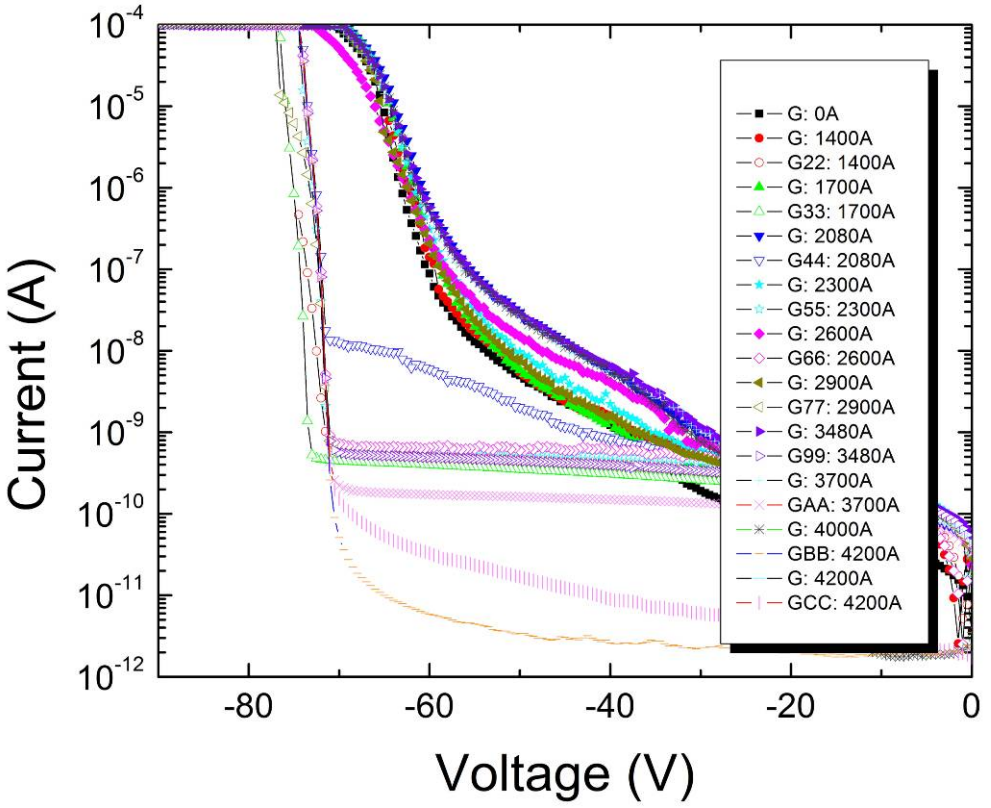


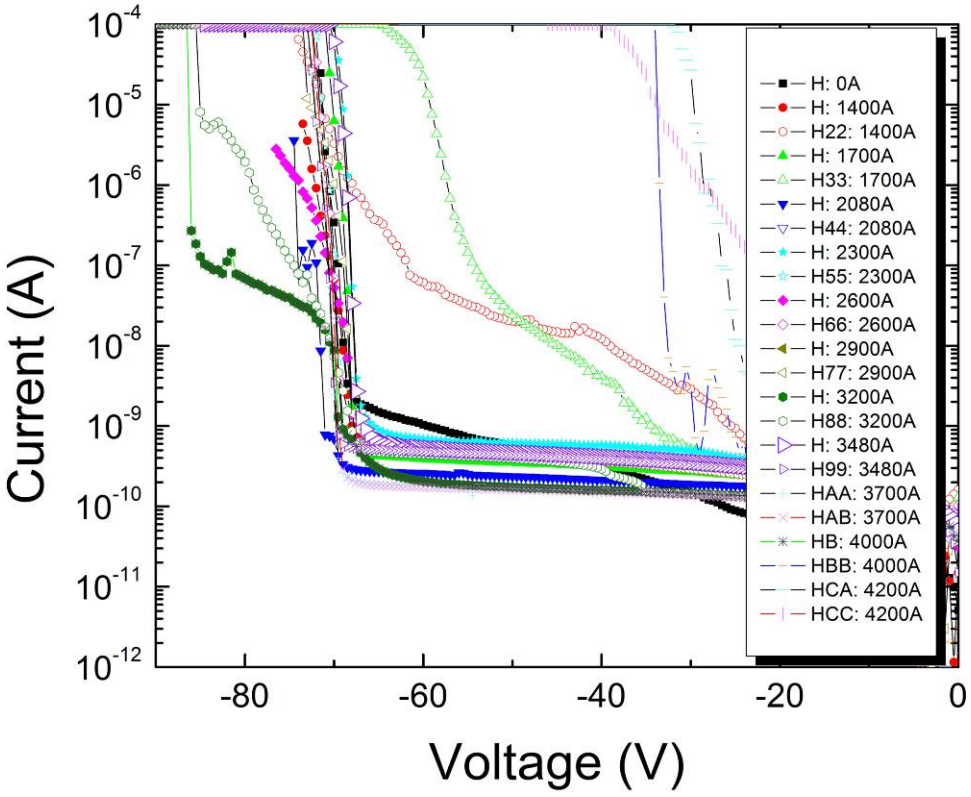
(Continued from the previous page) JTE1 optimization for FQ-C sample: Location C and D.





(Continued from previous pages) JTE1 optimization for FQ-C sample: Location E and F.





(Continued from previous pages) JTE1 optimization for FQ-C sample: Location G and H.

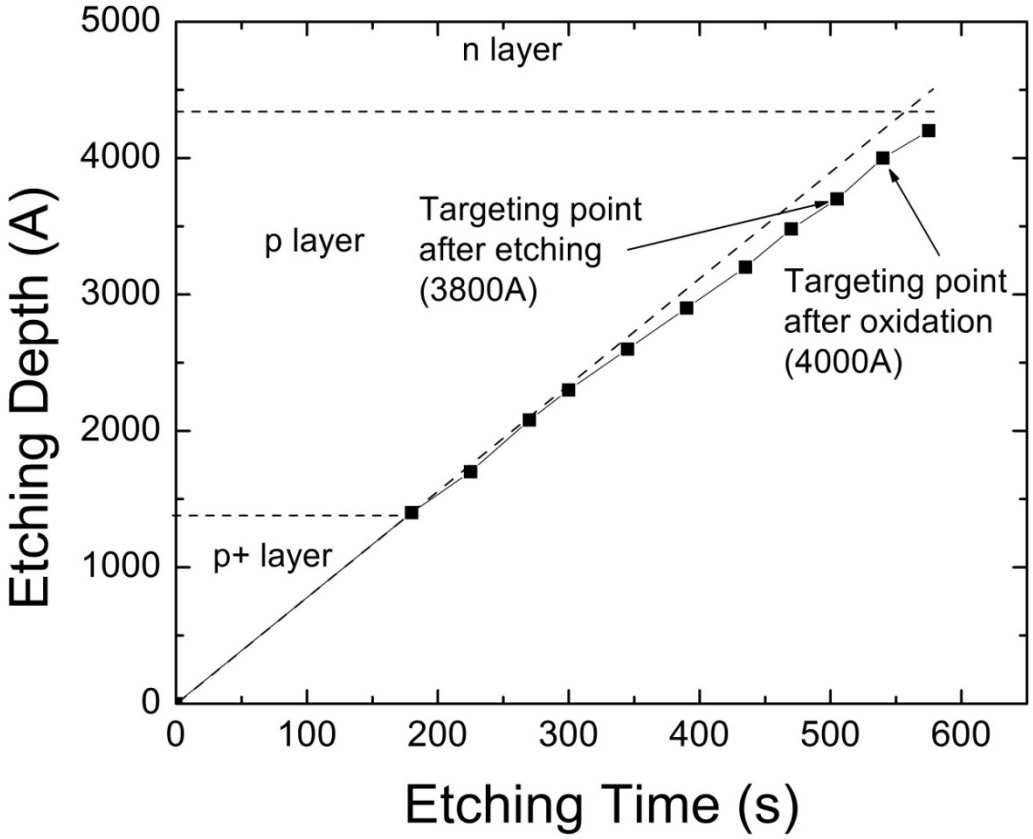


Fig. IV-3 SiC etching for JTE1 under 700W, 20V, CF_4:O_2=10:20, 7mTorr.

After JTE1 optimization, the sample is carefully cleaned by the following steps (Clean Recipe **CleanOx**):

Metal Cleaning:

- RCA II ($HCl:H_2O_2:H_2O$=4:1:1) for 30min in 80^oC water bath.
- 10% of 49% HF for 5min in ultrasonic.

Pre-cleaning:

- AZ400T cleaning for 30min in 80^oC water bath.
- Sulfuric acid for 30min in 80^oC water bath.
- 10% of 49% HF for 5min in ultrasonic.
- RCA I ($NH_4OH:H_2O_2:H_2O$=4:1:1) for 30min in 80^oC water bath.
- RCA II for 30min in 80^oC water bath.
- 10% of 49% HF for 5min in ultrasonic.

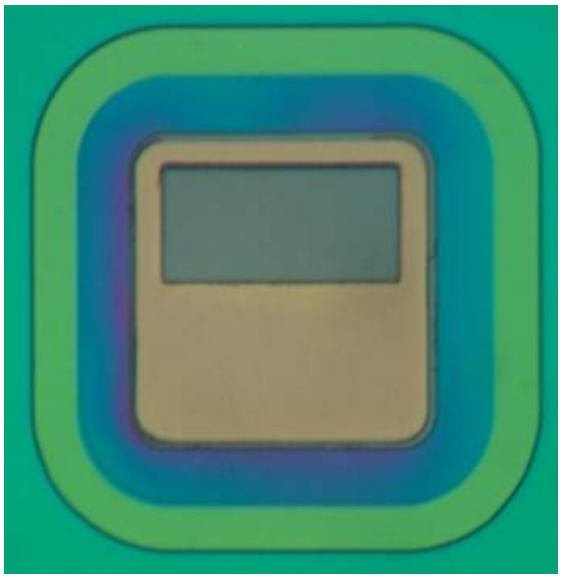
Oxidation Cleaning:

- RCA I ($NH_4OH:H_2O_2:H_2O$=4:1:1) for 30min in 80^oC water bath.
- RCA II for 30min in 80^oC water bath.
- 10% of 49% HF for 5min in ultrasonic.

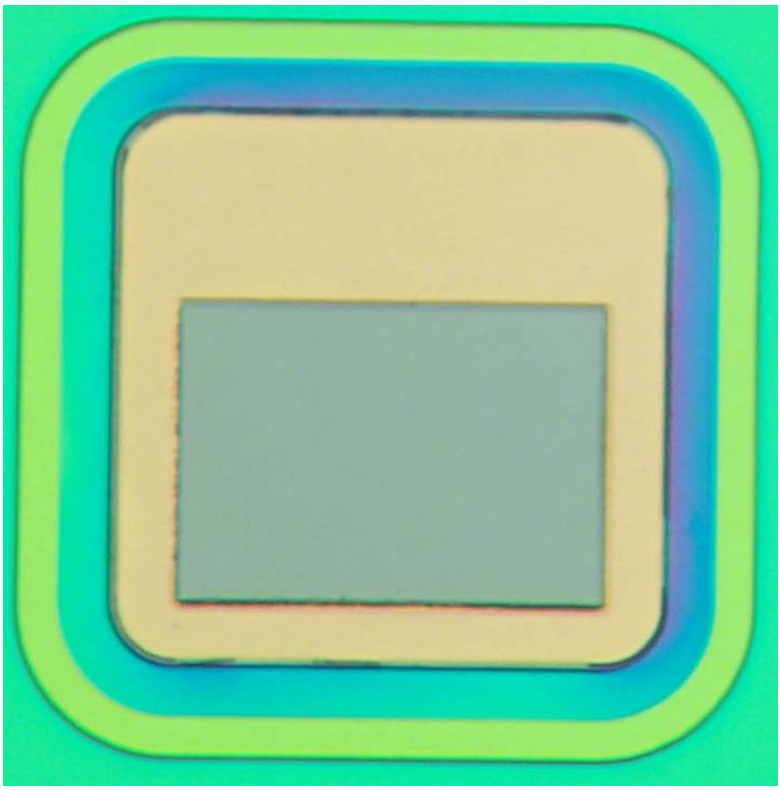
DI water rinse is done after each cleaning step. The samples are loaded into oxidation chamber for 0.5hours sacrificial oxidation. The sample is taken out and HF is used to remove the sacrificial oxide followed by an Oxidation Cleaning. Then a three-hour thermal oxidation is done at 1150^oC, followed by one hour Argon annealing at the same temperature.

After taken out from oxidation chamber, the samples are loaded into PECVD chamber for 5000Å SiO_2 and 2500Å Si_3N_4 dielectric layer.

Then the front side optical window is opened by 10% HF with over etching of 1min. The etching provides a guide for the p-contact window etching which follows a similar step. Then the p-contact metal (Ti/TiN (800Å/1500Å) is sputtered and lift-off is done by AZ400T photoresist stripper at 80^{o}C. The front side is then protected by hard baked photoresist. The backside oxide is removed by HF, and AlTi/Ni (250Å/3000Å) is sputtered. Both the front side metal and backside metal are annealed at 950^{o}C for 10min. This finishes all the steps for an on-die measurement. If necessary, an overlay metal of Ti/Au (800Å/5000Å) could be done with the same p-contact mask and lift-off for wire bonding purpose. Two fabricated SiC SPADs with junction area of 160μmx160μm and 260μmx260μm are shown in Fig. IV-4.



(a) 160umx160um SiC SPAD



(b) 160umx160um SiC SPAD

Fig. IV-4 Photos of the world's first SiC SPADs.

4.2 I-V and Gain Measurement for Sample FQ-C Devices

The dark current measurement for two good SiC SPADs on FQ-C sample is shown in Fig. IV-5. One device has a junction area of 160μm×160μm, and the other is 260μm×260μm. They have slightly different breakdown voltages 76.7V and 73.7V, respectively. At 90% of V_{br} of each device, the dark current is 7pA and 23pA respectively, which is corresponding to a dark current density of 27nA/cm^2 and 34nA/cm^2.

The gain of the 160μm×160μm device is measured by measuring the photo current with weak UV light. The unit gain voltage is chosen as 50% of the breakdown voltage. And the gain G is defined as,

$$G(V) = \frac{Net\ photo\ current}{Net\ unit\ gain\ photo\ current} = \frac{I_{Photo}(V) - I_{Dark}(V)}{I_{Photo}(50\%\ V_{br}) - I_{dark}(50\%\ V_{br})},$$

where the $I_{Photo}(V)$ *and* $I_{Dark}(V)$ are the measured currents under weak UV illumination and in darkness, and $I_{Photo}(50\%\ V_{br}) - I_{dark}(50\%\ V_{br})$ is the net photo current at unit gain voltage. The gain measurement result is shown in Fig. IV-6. The device can easily have a high gain of >10^7. The single photon count bias voltage is also shown in Fig. IV-6.

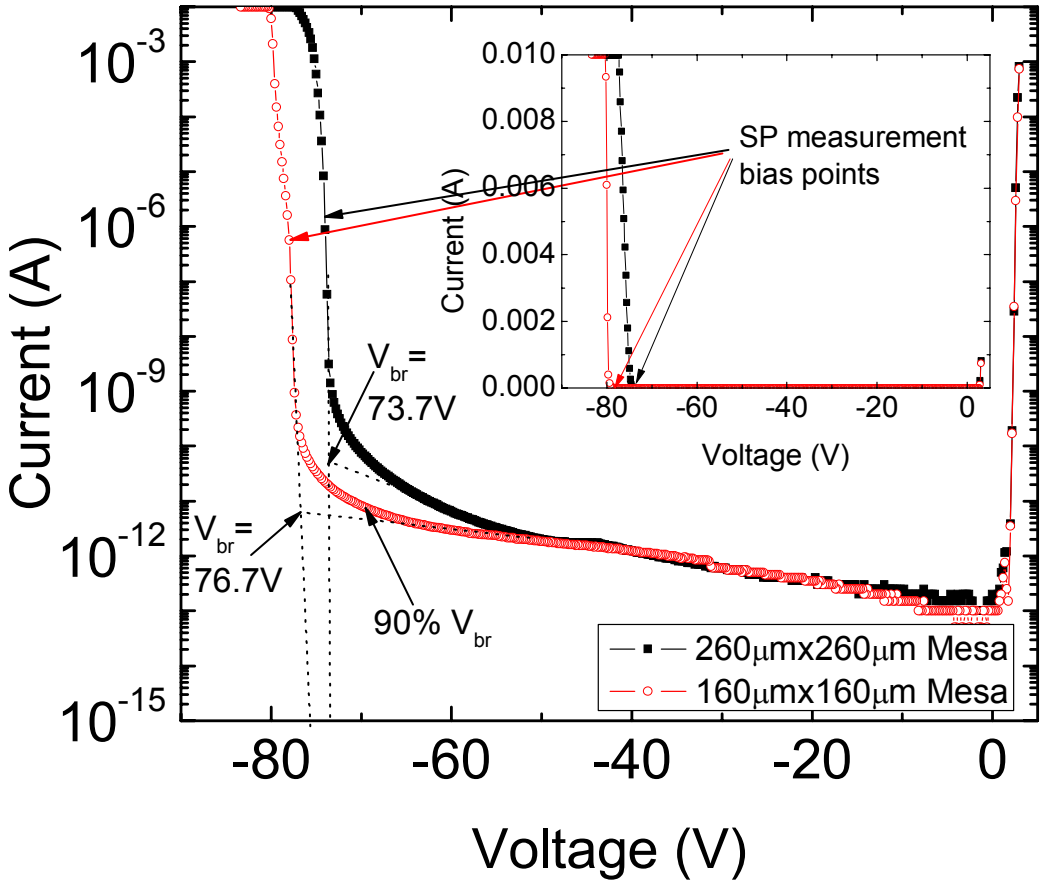


Fig. IV-5 I-V measurement for two good SiC SPADs on sample FQ-C with MJTE edge terminations.

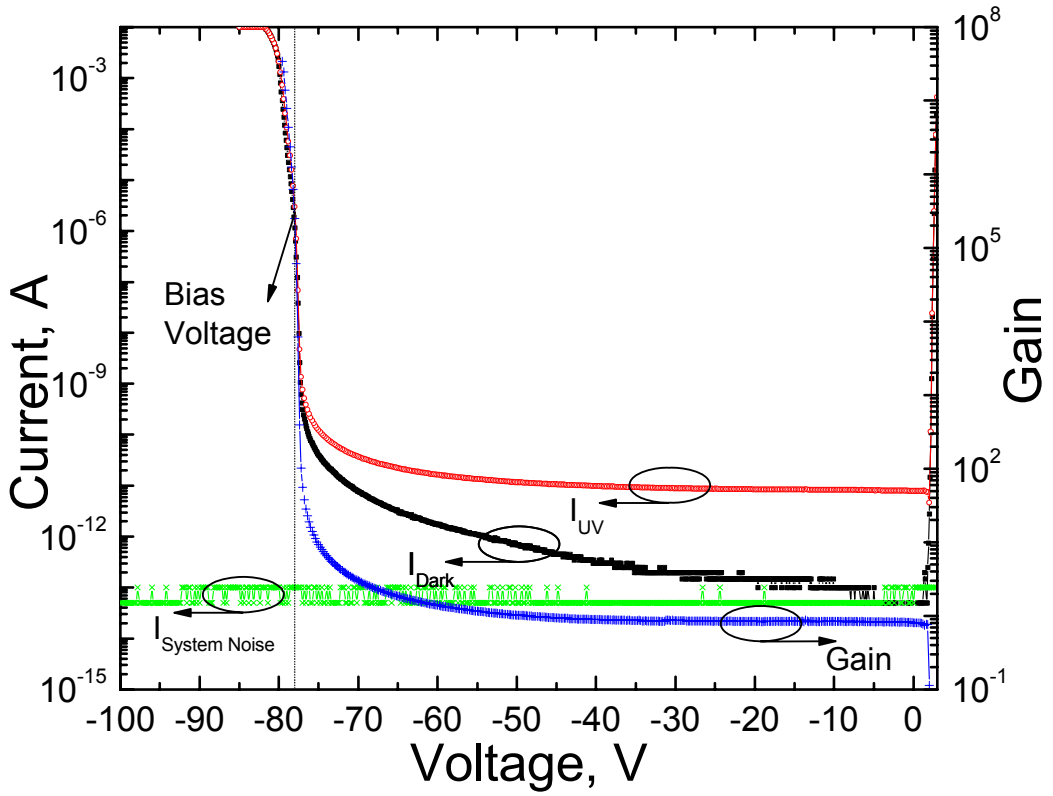


Fig. IV-6 Gain measurement for a 160μm×160μm SiC SPAD on FQ-C sample.

4.3 Quantum efficiency measurement for wafer FQ-C devices

The quantum efficiency (QE) of the FQ-C devices is also measured at three different voltages: -5V, 50% of V_{br} and 90% of V_{br}, as shown in Fig. IV-7. The device has a peak QE around the most interested wavelength 270nm and 280nm, which has a proper penetration depth in SiC (Fig. I-5). The small device has slightly higher measured QE (18%) than that (15%) of the large device, which most likely due to the light absorption in the edge termination area. A more accurate way to determine the QE will be addressed later when more devices with different dimensions are available.

The QE shows a good roll-over towards the longer wavelength. The light current above 380nm is too weak to measure with HP4145B. A more sensitive machine Keithley 4200SCS is purchased and we will see the improvement of QE measurement in the next chapter. Also, a long-pass filter is purchase to remove the 200nm light coupled out of the monochrome meter when measuring the wavelength above 380nm.

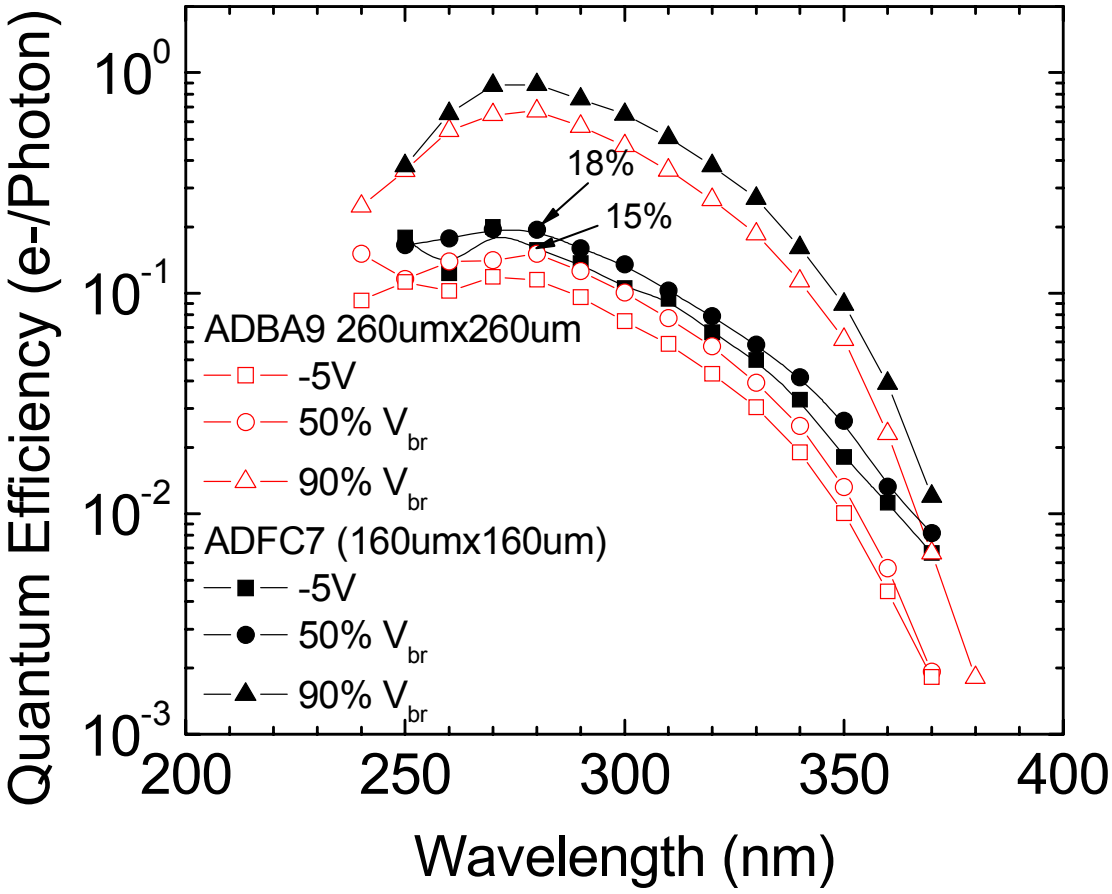


Fig. IV-7 Quantum efficiency measurement for SiC SPADs on sample FQ-C at three different bias voltages: -5V, 50% of V_{br} and 90% of V_{br}.

4.4 Single Photon Measurement for FQ-C Devices

As explained in the previous chapters, LEDs instead of UV lamps are used for single photon counting measurement, because of the noise from the UV lamp power supply and monochrome meter power supply. A 350nm LED is used for the single photon counting measurement. The manufacture provides the relative power intensity of the LED radiation, as shown in Fig. IV-8. It will not be accurate in estimating the light intensity if one assumes the light is concentrated at 353nm. In reality, the calibration Si detector has a much stronger responsivity at higher wavelength Fig. IV-9. With the known responsivity of the Si calibration detector and measured SiC spectrum QE, one can easily figure out the total photons coupled into the SiC SPAD and generated e/h pair number Fig. IV-10.

The dark count measurement for a 160μm×160μm device is shown in Fig. A total of 4.5MHz of pulses are counted. It is obvious that at 78.0V, the dark count rate is still low and the pulse height is significantly higher than the background noise level.

Based on the analysis of Fig. IV-10, a total of 1.9×10^{-10}W photons (372MHz) are incident into the 74μm×34μm optical window (plus the surrounding area, the total optical sensitive area is 3662μm^2), and 6.2MHz contributes to the light current, with an average QE of 1.7% comparing to the 353nm QE of 2.6%, since the light power in the longer wavelength is not sensitive to SiC SPADs. The single photon counting efficiency (SPDE) is thus determined as 4.5MHz/372MHz=1.2%.

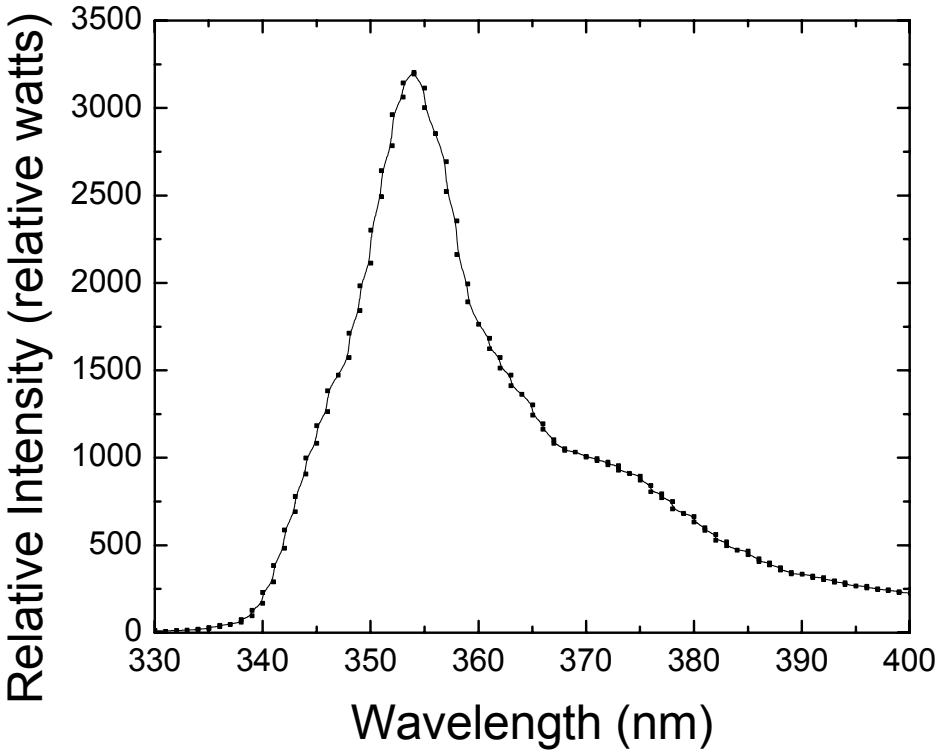


Fig. IV-8 Relative power intensity of the 353nm UV LED.

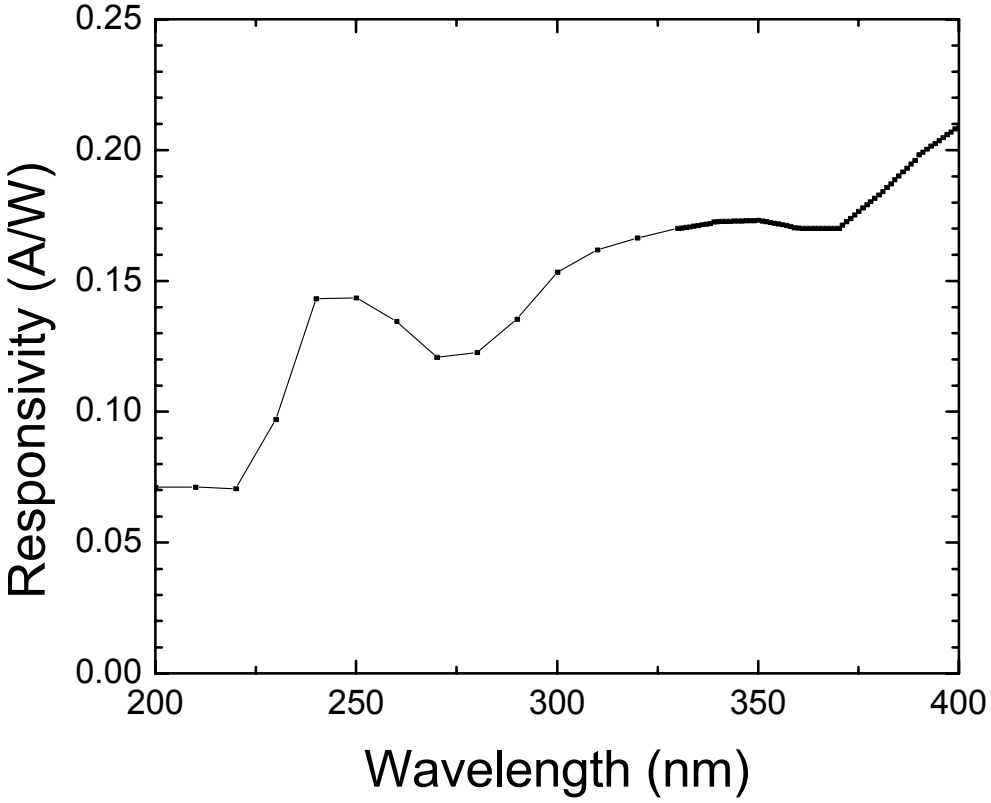


Fig. IV-9 Responsivity of the standard Si detector for light intensity calibration.

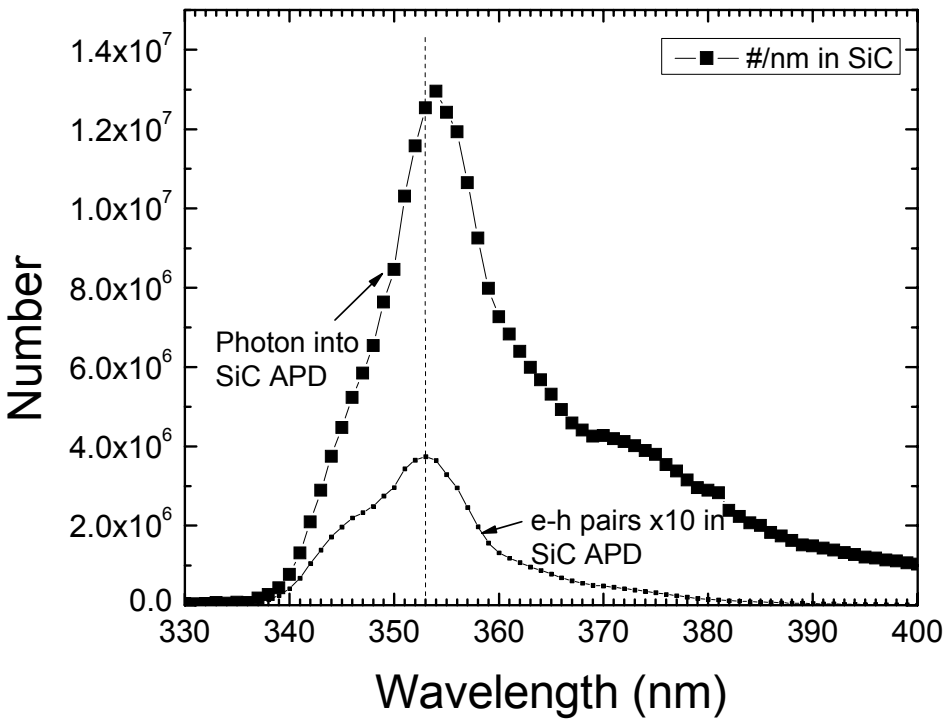


Fig. IV-10 Photons coupled into a SiC SPAD and generated e/h pair number based on a standard Si calibration detector and the measured QE of SiC SPAD.

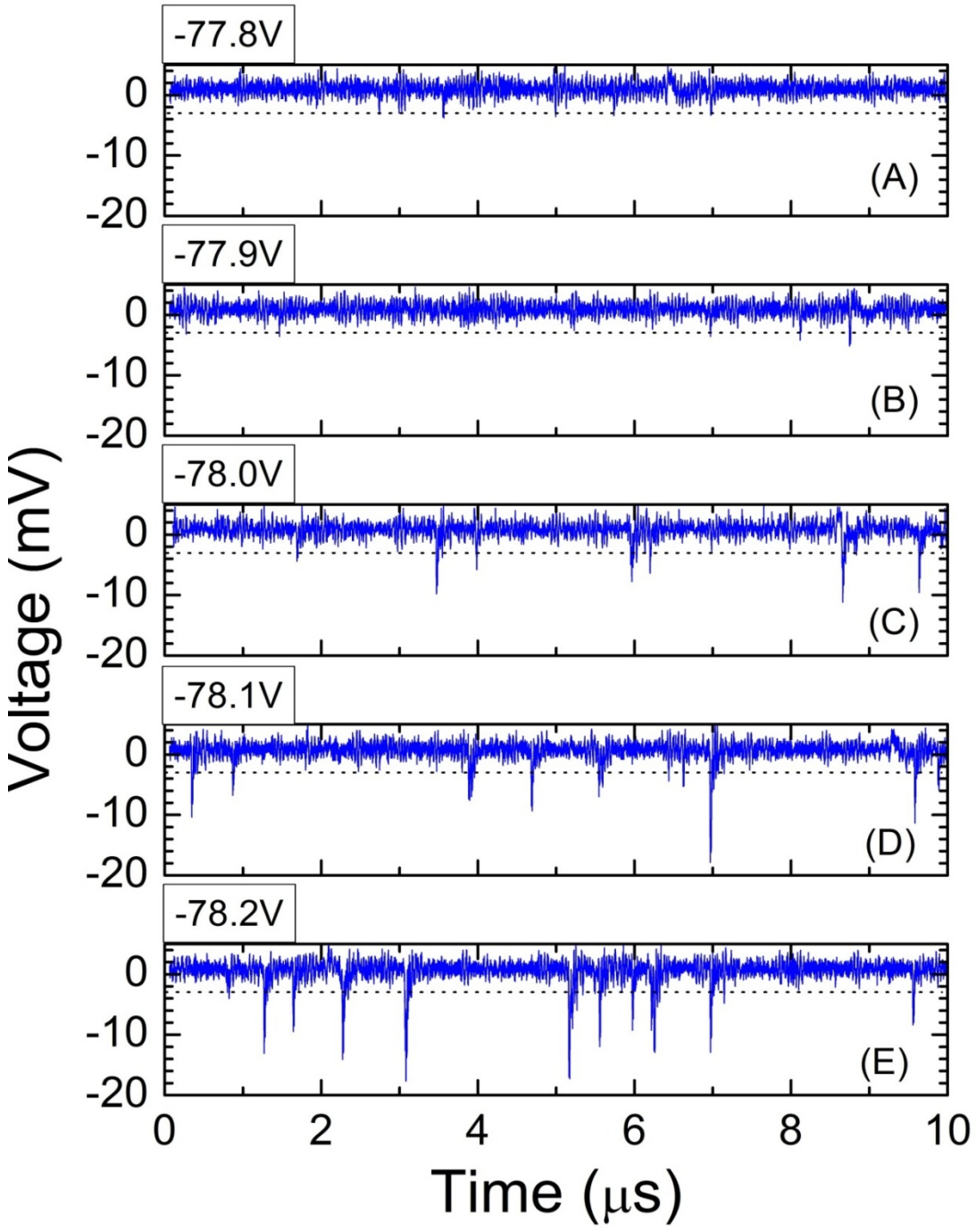


Fig. IV-11 Dark count measurement for FQ-C a 160umx160um SiC SPAD on sample FQ-C.

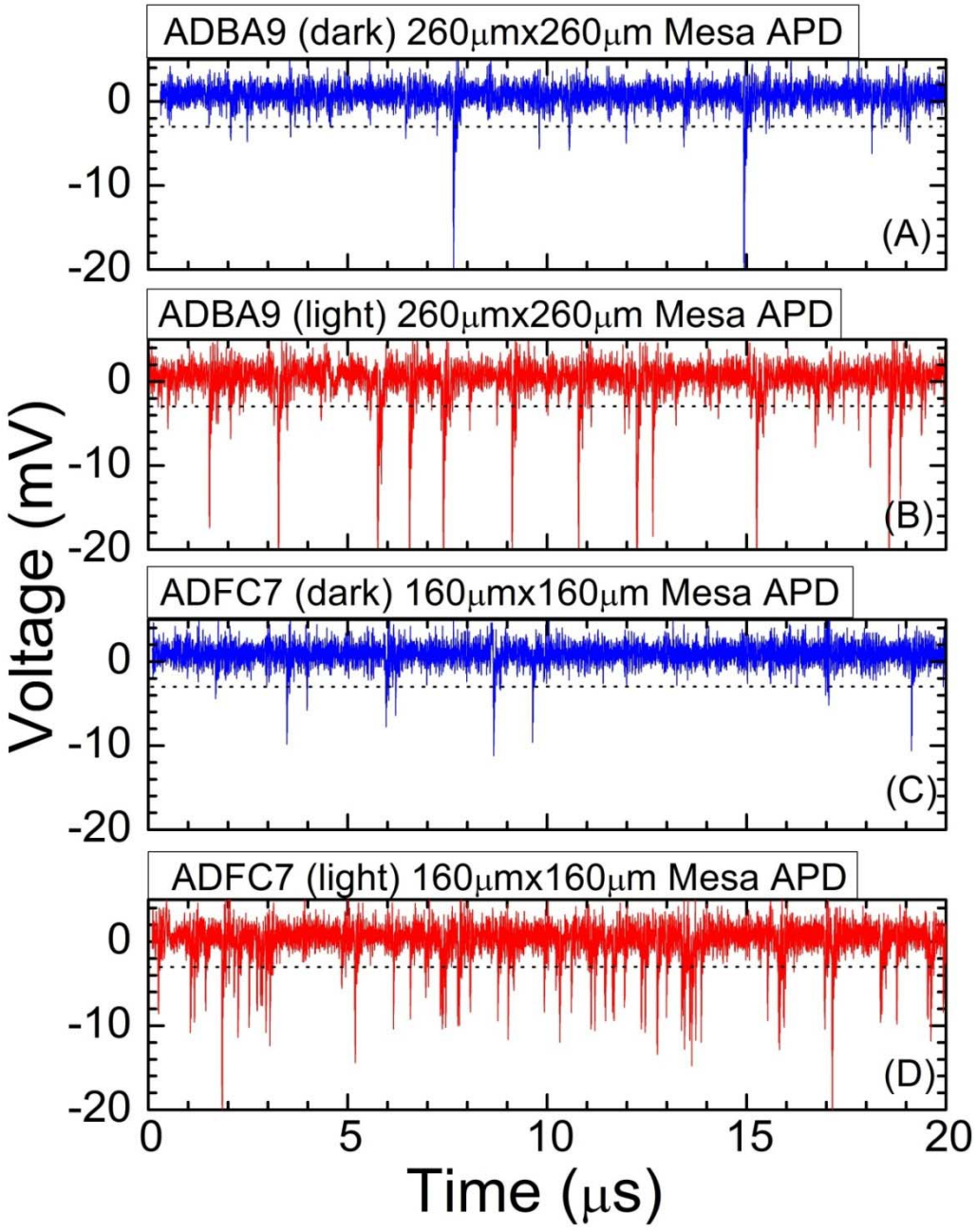


Fig. IV-12 Single photon counting measurement for a 160μm×160μm (ADFC7) device and a 260μm×260μm device (ADBA9). ADFC7 is biased at –78.0V and ADBA9 is biased at –74.05V, respectively.

4.5 Measurement of sample FQ-D devices: Giga Gain and Dark Count Rate Temperature Dependence Measurement

Sample FQ-D is processed with sample FQ-C but have slightly larger JTE step depth (350Å). The JTE1 optimization is quite similar to FQ-C sample. Since both samples are from the same wafer, the QE differences are very minor and within the experimental error, which will not be detailed here.

The measured device is aggressively driven to 10mA and survives. With its size and high bias voltage, the power density reaches 3.1kW/cm^2. It proves the robustness of the SiC SPADs. The single photon counting measurement is shown in Fig. IV-14 (dark count) and Fig. IV-15 (photon count).

For Si and InP SPADs, cooling is always an effective way to suppress dark count rate. For Si SPADs, dark count rate drops about one order of magnitude for every 30^{o}C temperature drop. For SiC, it is not surprised that with heating, the dark current will increase and the dark count rate will also increase. But no study has been done to see if the dark count rate will decrease when the temperature is reduced. It is an interesting topic since at room temperature the intrinsic carriers in 4H-SiC is negligible and reducing the temperature does not significantly reduce the intrinsic carrier density in SiC. All the carriers in SiC are related to defects, which is not the same case of high temperature where intrinsic carriers starts to be significant.

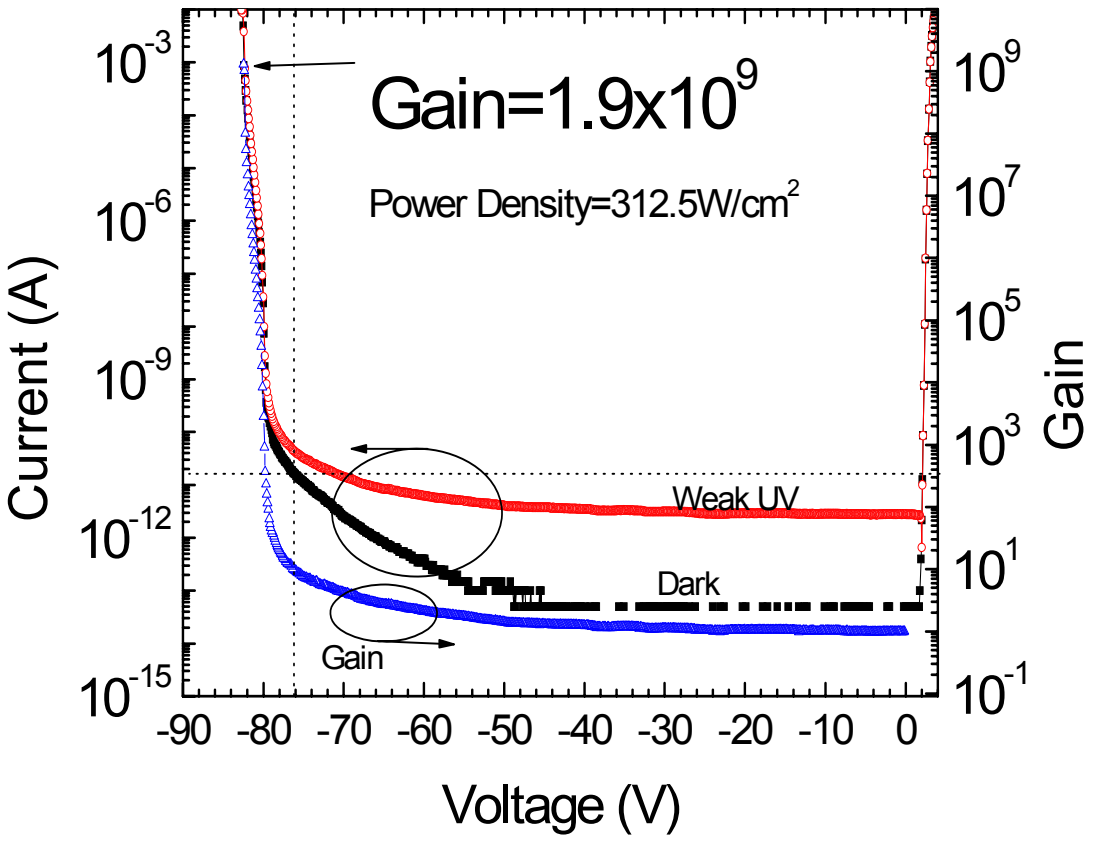


Fig. IV-13 SiC SPAD capable of a 10^9 gain.

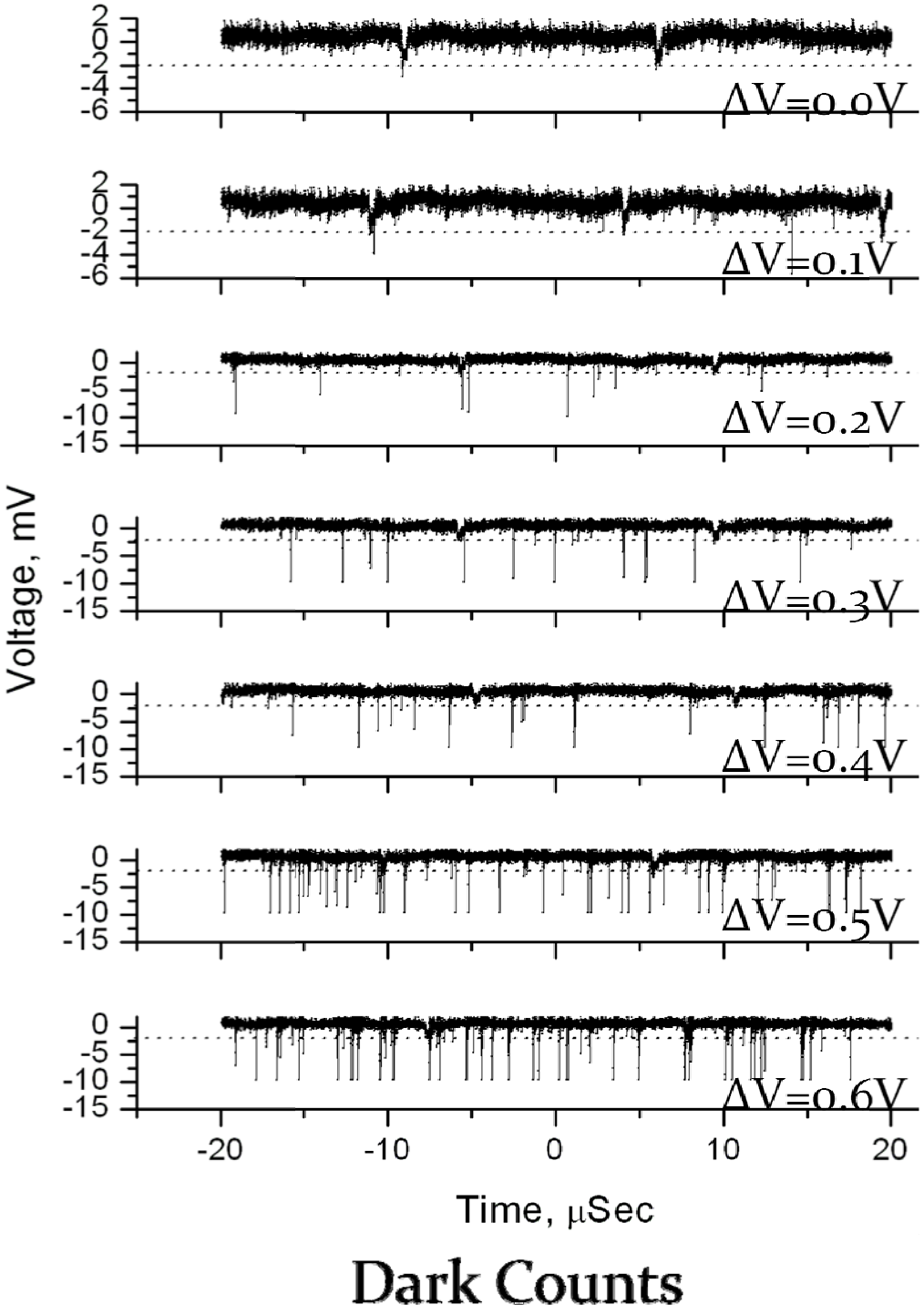


Fig. IV-14 Dark count rate measurement for a FQ-D device (160μm×160μm).

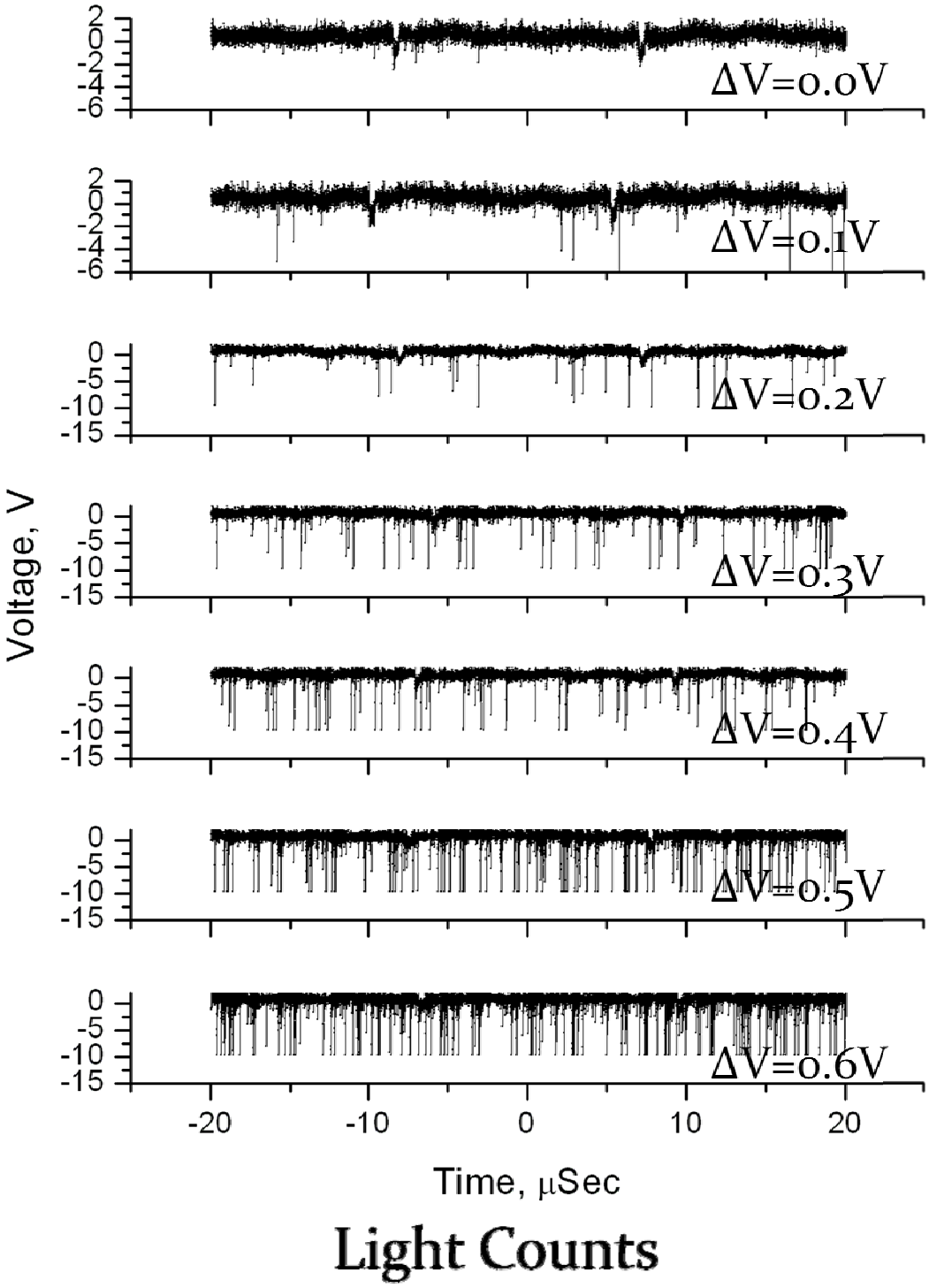


Fig. IV-15 Photon count rate measurement for a FQ-D device (160μm×160μm).

To determine the dark count rate temperature dependence, one should realize that the dark count rate is a strong function of bias voltages, and breakdown voltages reduce with temperature reduce, which is a signature of avalanche breakdown. Our experiment result confirms such breakdown voltage temperature dependence (Fig. IV-16). With 24^{o}C temperature drop, the breakdown voltage shifts about 0.17V. When the temperature drops, at a given bias, due to the actual breakdown voltage shift, the dark count rate increases instead of decreases. In Fig. IV-17, it is clearly shown that other than the breakdown voltage shift, there is not dark count rate change at all. NASA also helps to identify the dark count rate temperature dependence with a Thomas-Hall Effect cooler which can reduce the temperature to the liquid temperature of the used gas. The method is used for InP SPAD dark count rate before at NASA. And it is shown that there is not dark count rate reducing even when the device is cooled 100^{o}C below the room temperature.

The temperature dependence study clearly shows that the dark count carrier generation is not temperature sensitive when operating at room temperature and below. For SiC SPADs, other methods have to be found to suppress the dark count rate. As discussed in the previous chapter, a field-limiting layer and smaller device size are designed and in the next chapter, it will be proven to be very effective in reducing the dark count rate.

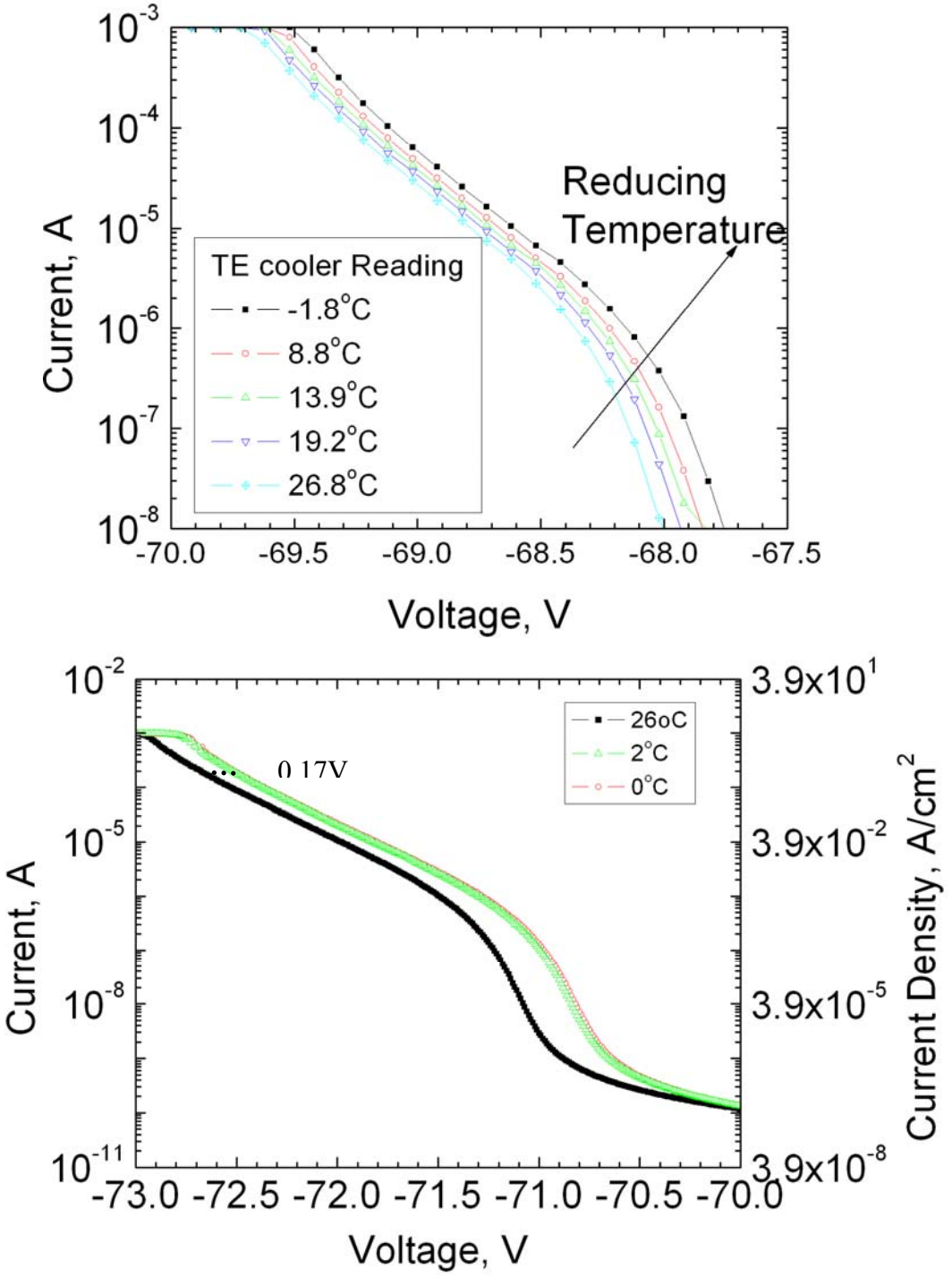


Fig. IV-16 A SiC SPAD shows a 0.17V shift of breakdown voltage for a 24°C temperature drop.

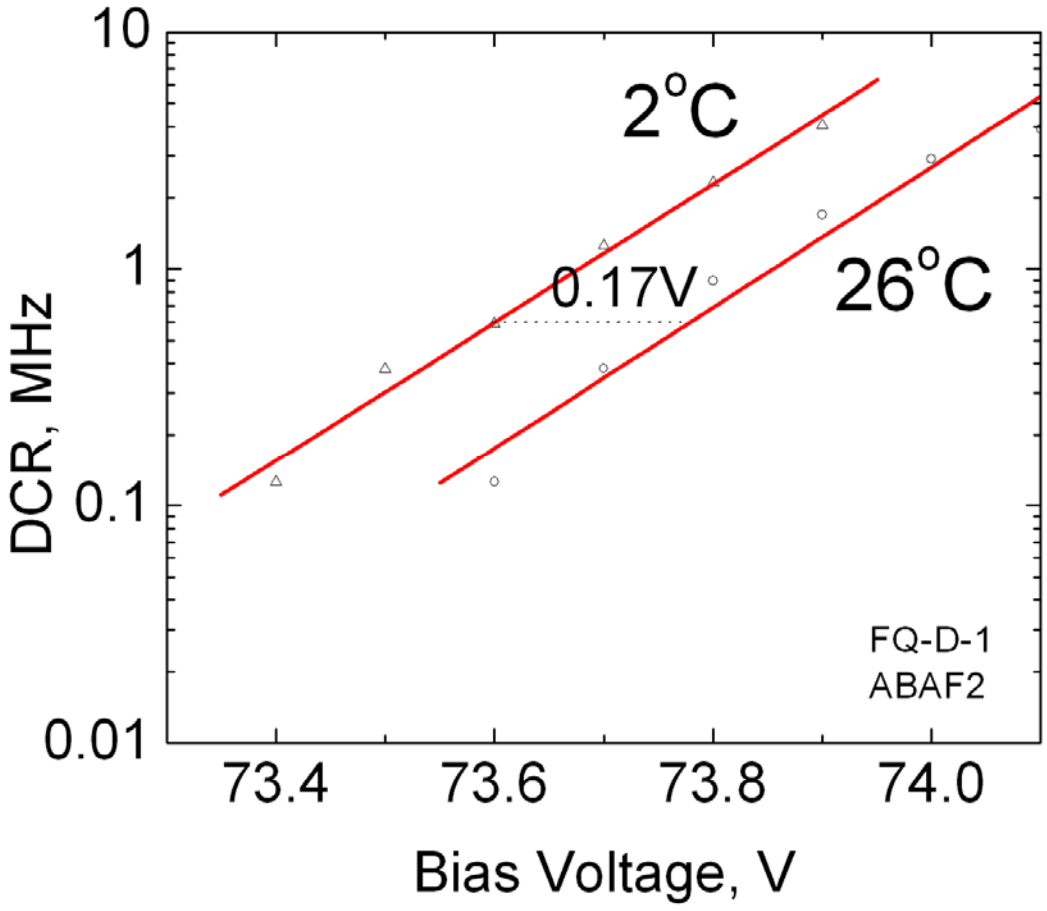


Fig. IV-17 Dark count rate (DCR) measurement for a FQ-D SiC SPAD with passive quenching circuit.

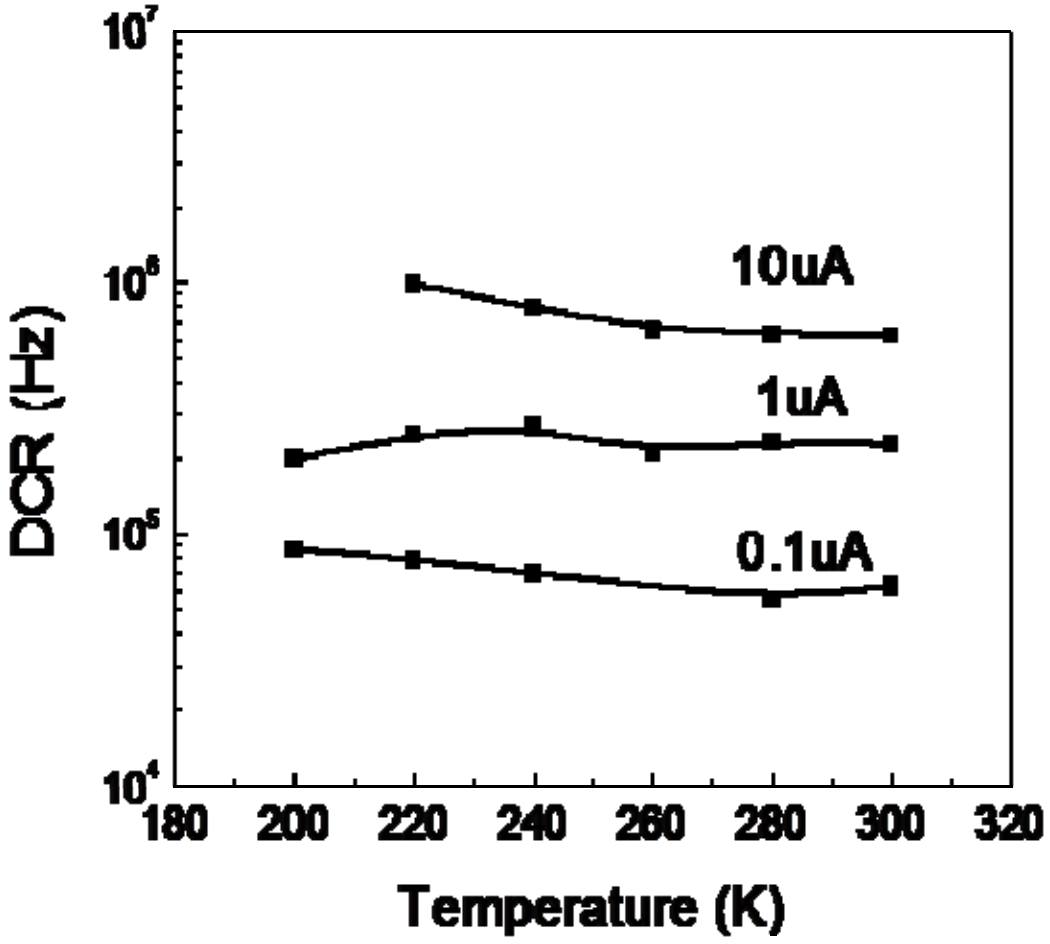


Fig. IV-18 Dark count rate measurement by NASA GSFC Center. The device is driven by a current source at different current level and temperature is controlled by Thomas-Hall Effect cooler.

V. PROCESSING AND CHARACTERIZATION OF IMPROVED SIC SPADS

The improved version of SiC SPADs focused on the following aspects:

a. An i (either n- or p-) layer is introduced in the multiplication region to suppress the defect-assisted tunneling current. A thick absorption layer is designed for high quantum efficiency. The structure is designed to be a SAM structure.

b. A new mask set (Mask-II) with three-JTE steps is designed and is also capable of bevel formation. The mask set also addresses the wire bonding issues associated with the first mask set.

Both MJTE and bevel structures are processed. Three wafers are designed and processed, and the successful devices from a SAM wafer are detailed.

5.1 Bevel samples

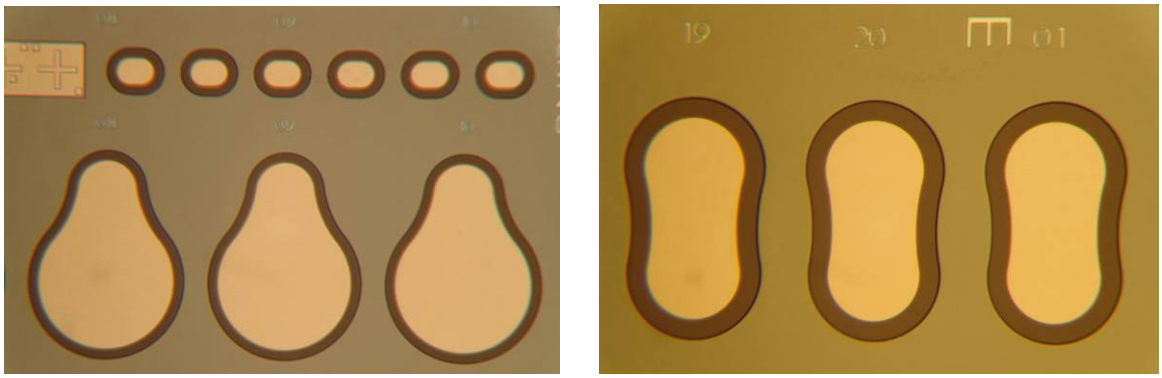
5.1.1 Processing of bevel samples

The bevel formation is illustrated in Fig. V-1. The sample is first patterned with photoresist, then baked at high temperature to form the photoresist bevel, and cured in E-beam machine to harden the photoresist. Then an ICP etching is done to transfer the photoresist bevel to SiC bevel. Because the etching of photoresist is faster than SiC (ratio 4.4:1), the SiC bevel angle could be very small. After etching the sample is carefully cleaned to remove the remaining photoresist and protection metals, then it is sent to an oxidation chamber for a 0.5 hour sacrificial oxidation, a three-hour thermal oxidation, followed by thick PECVD SiO_2 and Si_3N_4 layer deposition. After oxidation and dielectric film deposition, the backside oxide is removed by hydrofluoric acid. AlTi/Ni metals are sputtered as the n-contact metal. The sample is sent to an RTA for an n-contact annealing at 950^{o}C for 10min. The front side dielectric layers are then etched by ICP and hydrofluoric acid. P-contact metals are sputtered followed by a short time p-contact annealing. If wirebonding is needed or the structure has off-mesa bonding pad, an overlay metal (Ti/Au 800 Å/5000Å) can be sputtered.

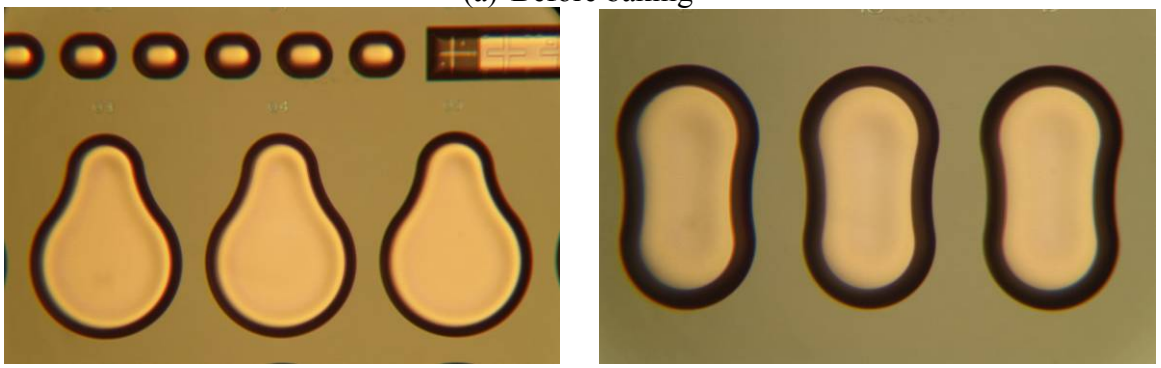
The first p-contact metal is Ni/AlTi/Ni/TiW (800Å/400Å/1500Å/1500Å), which is proved to be better than the Ti/TiN for p-type ohmic contact from previous power device study. However, there is no p-type Ohmic contact when using Ni/AlTi/Ni/TiW on samples from wafer AD (Fig. V-2). Even worse, the leakage current is very high after annealing (**Fig. V-3**). It is probably that AlTi forms alloy spikes or Ni consumes too thick a SiC layer so that the top p++ layer is consumed. From simulation (Fig. II-6), we know that the depletion

region extends slightly into the p++ layer due to a lower than expected p layer doping density. Without good Ohmic contact (the specific contact resistance $<10^{-2}\Omega cm^2$) the serials resistance will quench the SPAD and a much higher bias has to be applied, which will lead to a high DCR. A new Ohmic contact metal combination with a six-layer metals Ni/Ti/AlTi/Ti/AlTi/TiN (600Å/100Å/350Å/ 100Å/350Å/1300Å, setting point) is tried which gives very good Ohmic contact (low $10^{-5}\Omega cm^2$, Fig. V-4) on the AD samples with a top layer doped at $2e19cm^{-3}$. We also tried the same metal recipe on a wafer with the top layer only doped to $6\sim7e18cm^{-3}$. The new metal combination also gives a specific contact resistance of $10^{-4}\ \Omega cm^2$ (Fig. V-5). There is no leakage current degradation after annealing. The details of I-V measurement for a fabricated SiC SPAD are shown in the following sections.

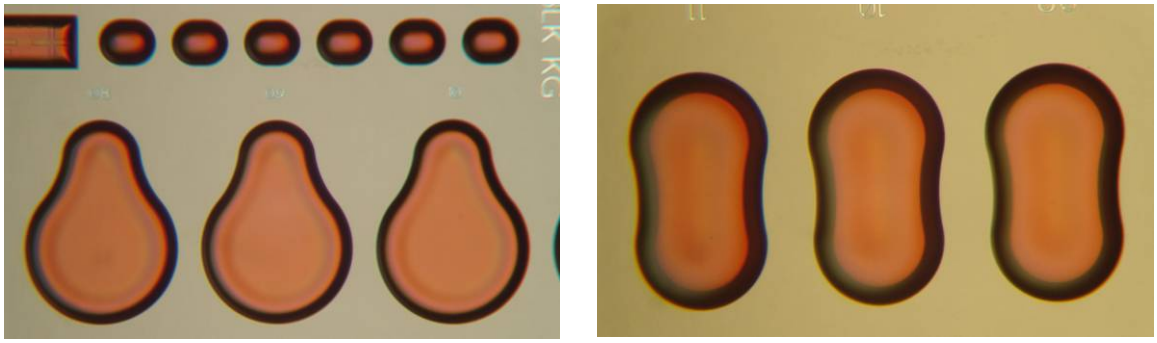
A fabricated Bevel SPAD is shown in Fig. V-6.



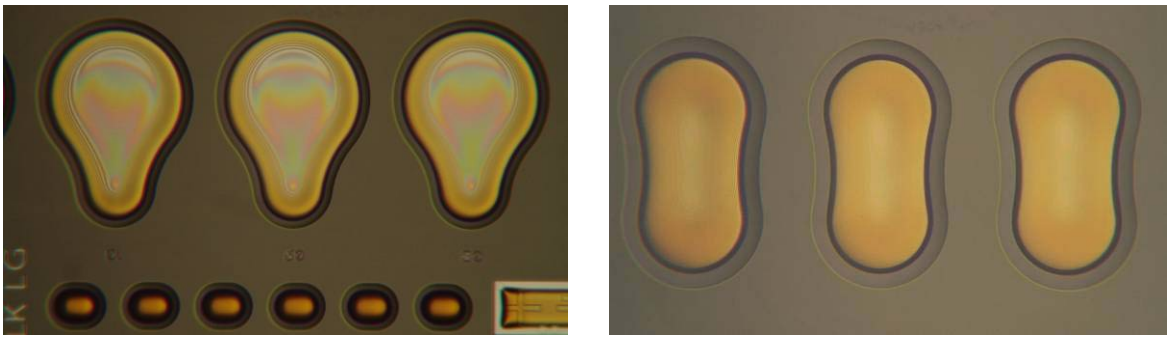
(a) Before baking



(b) After baking

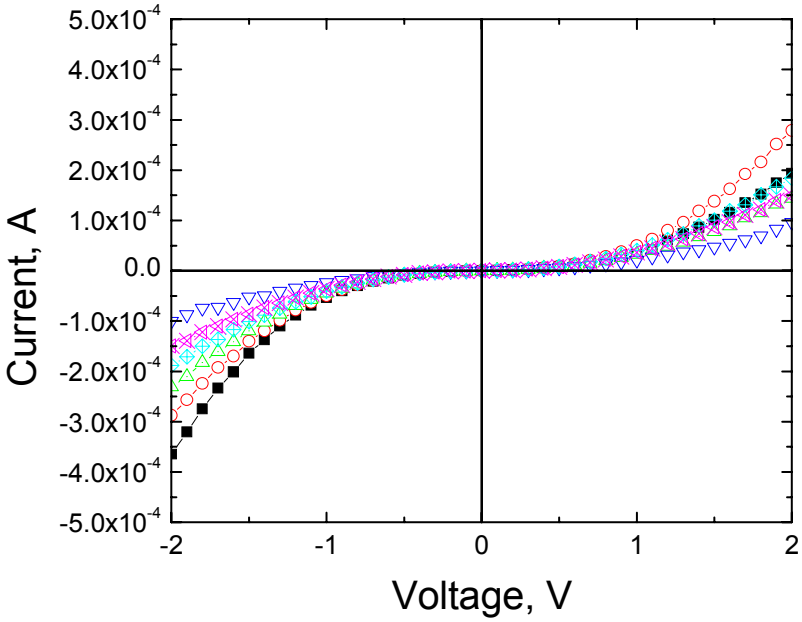


(c) After curing

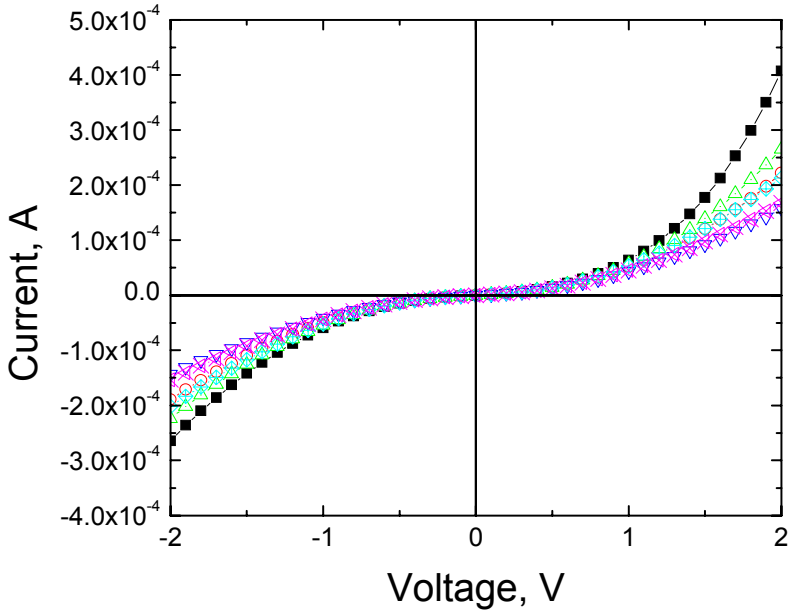


(d) After ICP etching

Fig. V-1 Processing of bevel edge termination SiC SPADs.

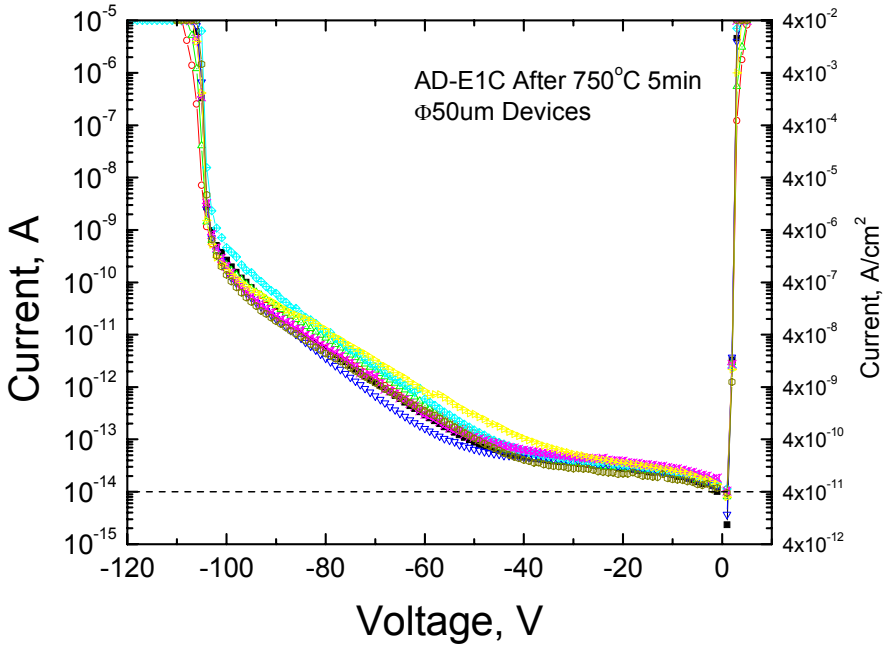


(a) Anneal at 750°C for 5min

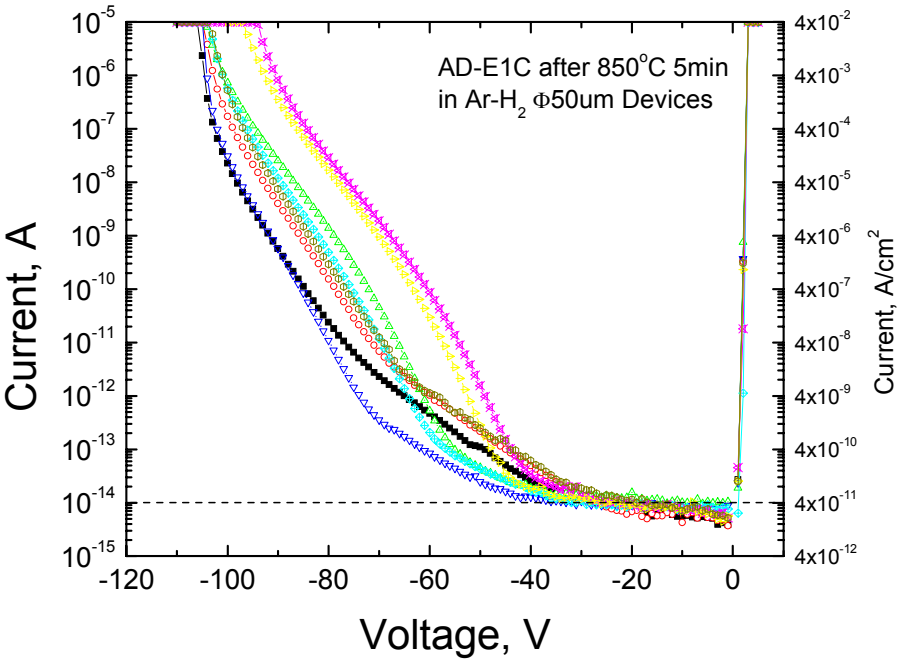


(b) Anneal at 850°C for 5min

Fig. V-2 TLM pattern I-V measurement of a testing sample from sample AD-E. The metal is Ni/AlTi/Ni/TiW (800Å/400Å/1500Å/1500Å per machine setting).



(a) Device shows high leakage current after annealing at 750°C 5min.



(b) Device shows high leakage current after 850°C 5min annealing.

Fig. V-3 I-V measurement for devices with Ni/AlTi/Ni/TiW after p-contact annealing.

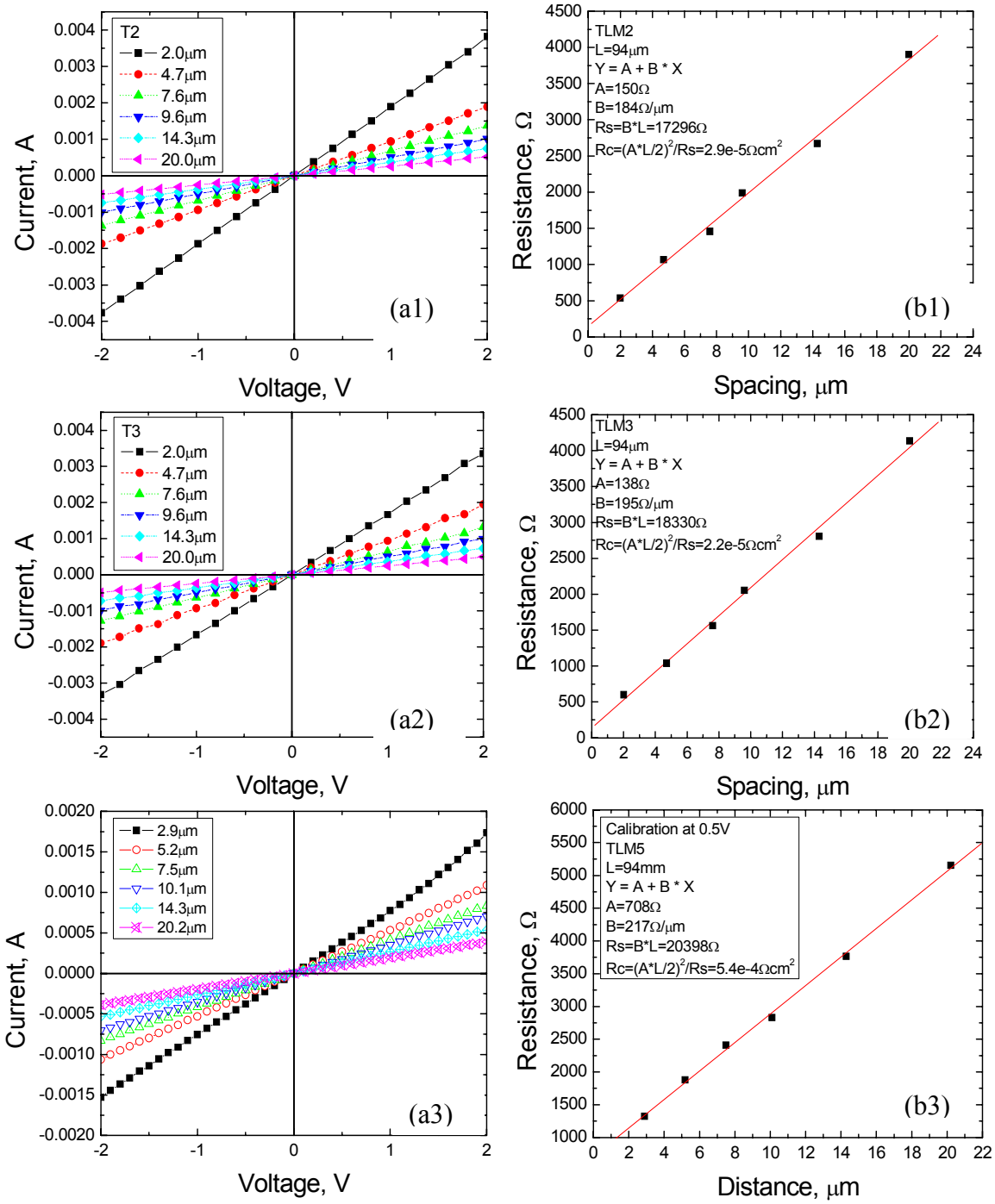


Fig. V-4 TLM measurement for AD samples with a metal scheme of Ni/Ti/AlTi/Ti/AlTi/TiN, which is significantly better than previous Ni/AlTi/Ni in two aspect: a very decent Ohmic contact resistance and no shorting due to thick Ni silicide. The p++ layer doping is 2e19cm^{-3}. The total metal thickness is about 3000A.

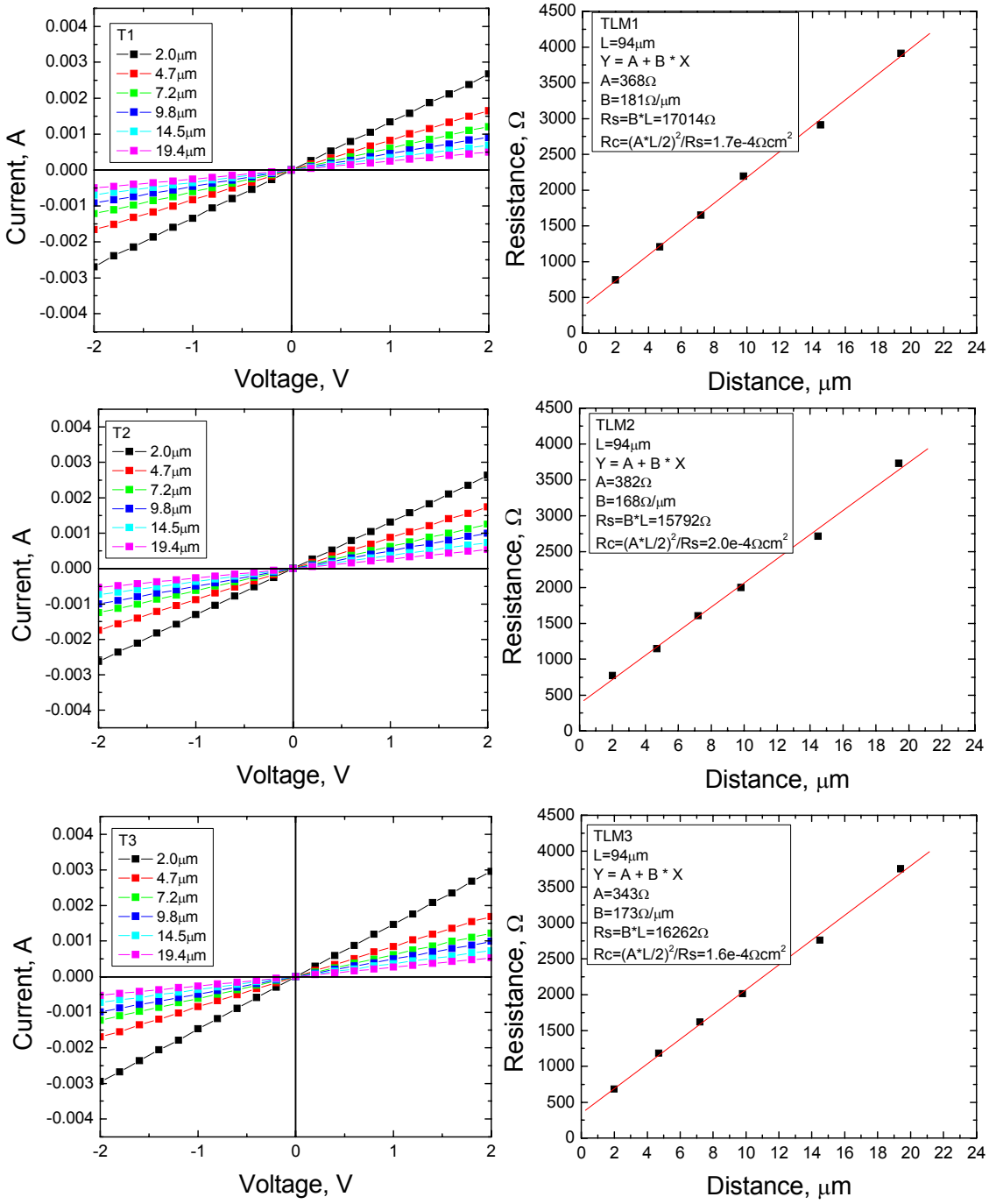


Fig. V-5 TLM measurement for sample CM-A1 with a metal combination of Ni/Ti/AlTi/Ti/AlTi/TiN. The p++ layer doping is 6~7e18cm^{-3}. The total metal thickness is about 3000A.

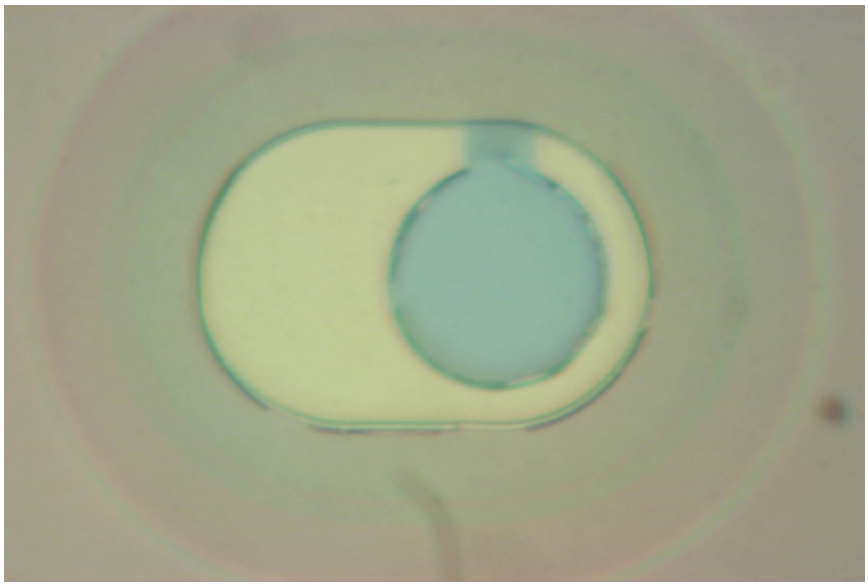


Fig. V-6 A fabricated SiC SPAD with Φ30um optical window.

5.1.2 I-V and Gain measurement

The I-V measurement result for a small bevel SiC SPAD (active area of 7529μm^2) is shown in **Fig. V-7**. The device shows an excellent dark current (<10fA at 90% of V_{br}, or 0.13nA/cm^2) and is capable of 10^7 gain. The light current and gain, however, do not show any sign of a SAM structure. Probably the field confinement layer is doped higher or is thicker than designed as a result of epitaxial non-uniformity. The low dark current also allows single photon testing with ultra weak light. In this measurement, a weak light which only generates 300fA light current is used.

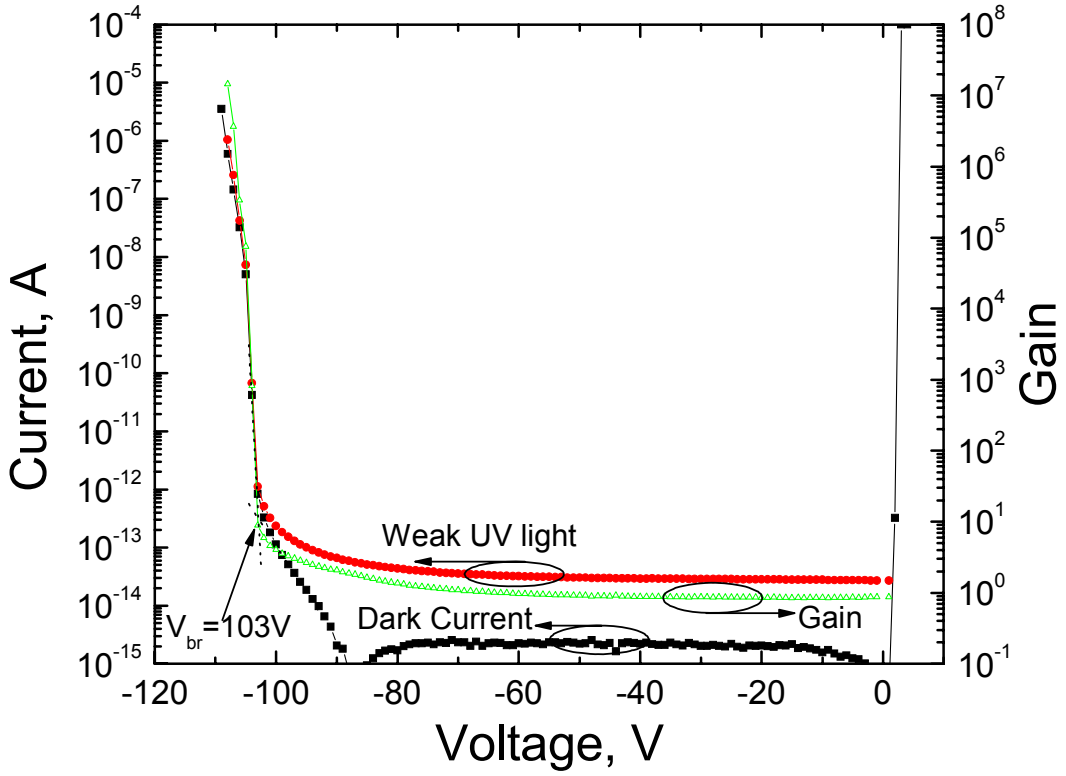


Fig. V-7 I-V and gain measurement for a small Bevel SiC SPAD.

5.1.3 Quantum efficiency measurement

The small bevel SPAD shows reasonable quantum efficiency (peaked 37% at 260nm) for solar blind wavelength as shown in Fig. V-8. The diode shows almost identical QE when biased at -5V and 50% V_{br}, indicating that the field confinement layer is not fully depleted at 50% V_{br}. At higher voltage, the gain and light current does not increase much. All these evidences seem to imply that this diode is not a SAM diode. The light current below 380 nm could not be measured, since the UV light is too weak and the device area is small. For wavelength shorter than 240nm, the light is largely absorbed by the quartz fiber and the Si detector has a higher leakage current than the light current, thus the light intensity could not be calibrated. The device shows reasonable QE of 37% and 25% at 260nm and 280nm. The device apparently has $>10^4$ UV to visible rejection ratio.

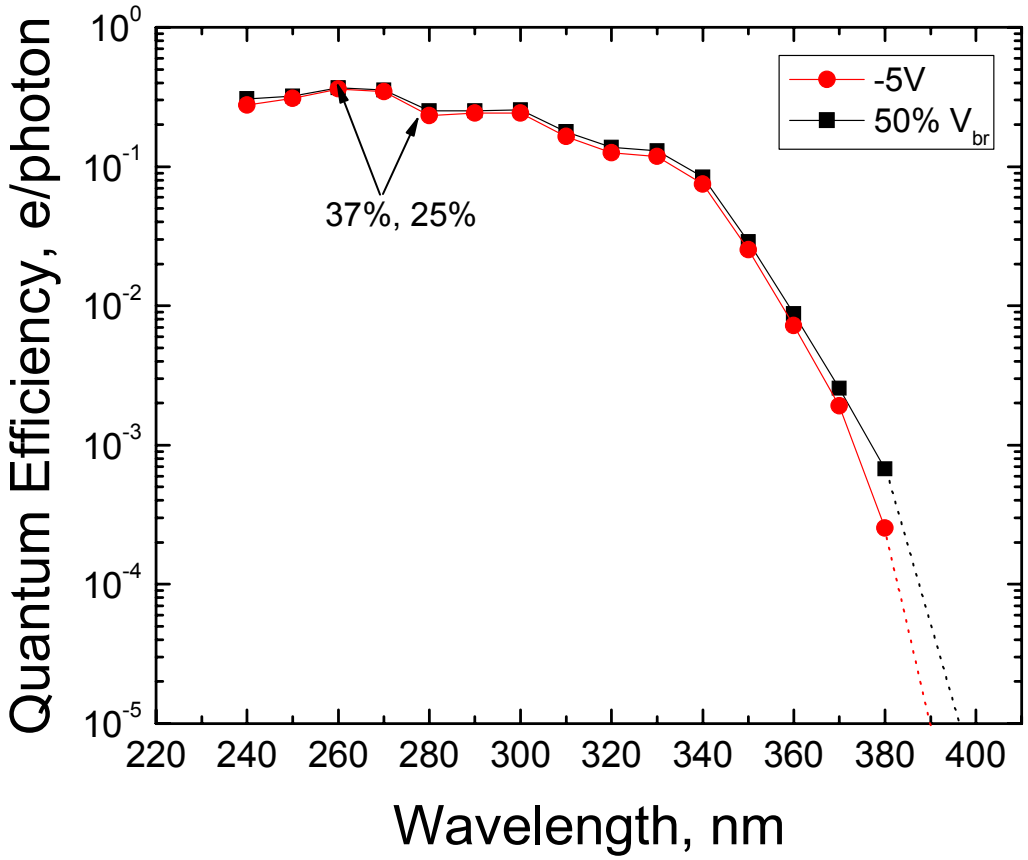


Fig. V-8 QE measurement for a small SiC SPAD with Φ30um optical window.

5.1.4 SP measurement

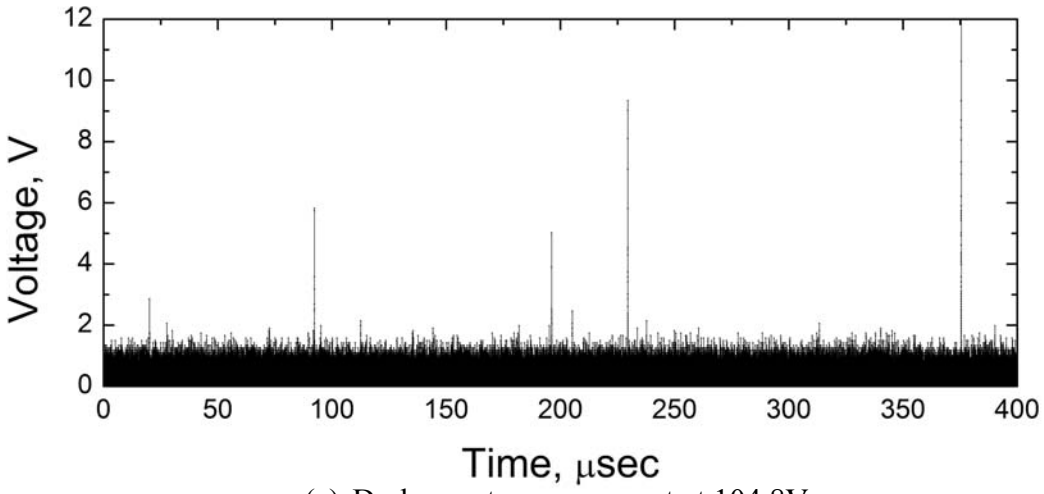
Since dark count rate is a strong function of bias voltage and different devices might have different bias voltages, for better comparison, a parameter F is introduced. Single photon counting efficiency (SPDE), QE, and counting efficiency (CE) are parameters which usually have little dependence to device areas. SPDE is the ratio of the number of pulses counted and the number of injected photons. SPDE calibrates the efficiency of the detector for single photon counting and represents the sensitivity of a detector. The CE describes the probability of a photo generated carrier to be multiplied and counted eventually. DCR, which shows a device noise level, however, is a strong function of the device area. It therefore would be meaningful to define a signal-to-noise ratio parameter *F* as

$$F(\lambda)=SPDE(\lambda)/DCRD,$$

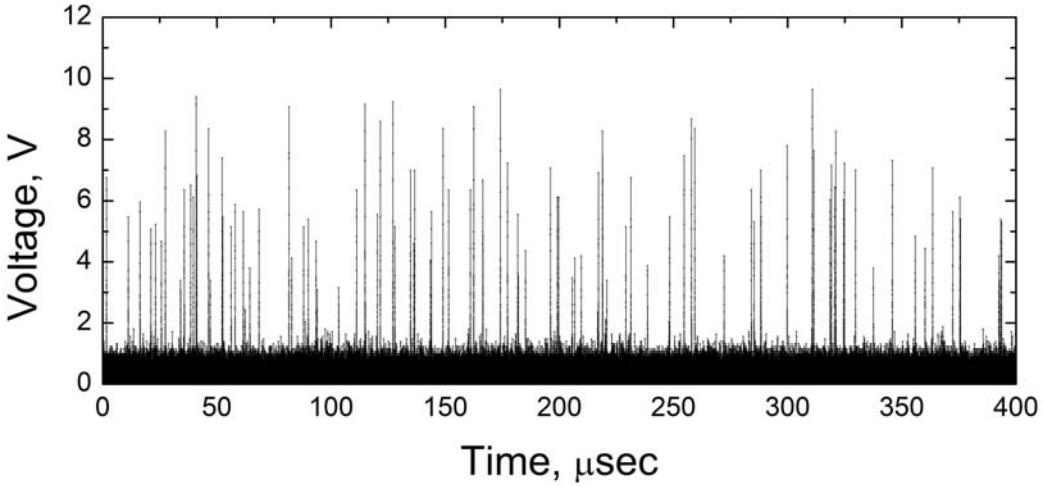
where the DCRD is dark count rate density, defined as the DCR per unit junction area. *F* has a unit of $\mu m^2 sec$, but it has less dependence on area than a direct ratio of SPDE*(λ)*/DCR. *F* should keep constant regardless of the device area *if* the dominant dark counts are from intrinsic carriers or from uniformly distributed defects. With current SiC quality, *F* actually favors small devices because defects might be the dominant sources for dark counts, and more fatal defects are likely to be included in larger area devices. Also, the DCR is a function of the threshold voltage. At high threshold voltages, the DCR could be close to zero and the SPDE is small but finite. In such a case, F could approach infinite. So F is far from a figure-of-merit in a strict sense. It is only meaningful when the device size is similar, and both SPDE and DCR are in the range of practical applications.

Due to the extremely low dark count rate and narrow pulse width, the single photon counting measurement needs to record data over a long time frame. Thus a deep memory (10^7 data record length) oscilloscope with fast response (2.5G/s sampling rate) is used. The single photon counting measurement under 280nm LED illuminations for the bevel SiC SPAD is made at different bias voltage and threshold voltages. A minimum of 4msec (10M points) are recorded. Fig. V-9 shows a segment of the measurement results (400μsec) at 104.8V. And the results are summarized in Fig. V-10 and Fig. V-11. At 105.0V and for most of the threshold voltages, the SPDE varies but is >1%, while the dark count rate is not higher than 20kHz. In the program, after counting each pulse, a 16nsec dead time is set to remove the after-pulses and fake pulses due to noises. After-pulses are due to the release of carriers which are trapped in defects levels after the photo/dark carrier avalanche breakdown. Another source of additional pulse count is due to noises. When noises superimpose on a pulse, the pulse might have multiple peaks, which will cheat the counting program. A long enough deadtime will help to remove this problem. If a longer dead time is needed, one might have to use low light intensity to reduce the chance that two photons arrive within the dead time. For our measurement, the light intensity is about 11MHz, or one photon per 91nsec on average. Thus within 16nsec, the chance that two or more photons arrive is low.

At 280nm, the diode has a SPDE/DCR of 2.28%/12.9kHz at 104.8V. The area of the diode is about 1/3 of the first SiC SPAD. The average F is around $10^{-2}\mu m^2 sec$, and the peak is about $1.8\times10^{-2}\mu m^2 sec$.



(a) Dark count measurement at 104.8V.



(b) UV count measurement at 104.8V under extremely weak UV light (light current 300fA).

Fig. V-9 Single photon counting measurement for a bevel SiC SPAD.

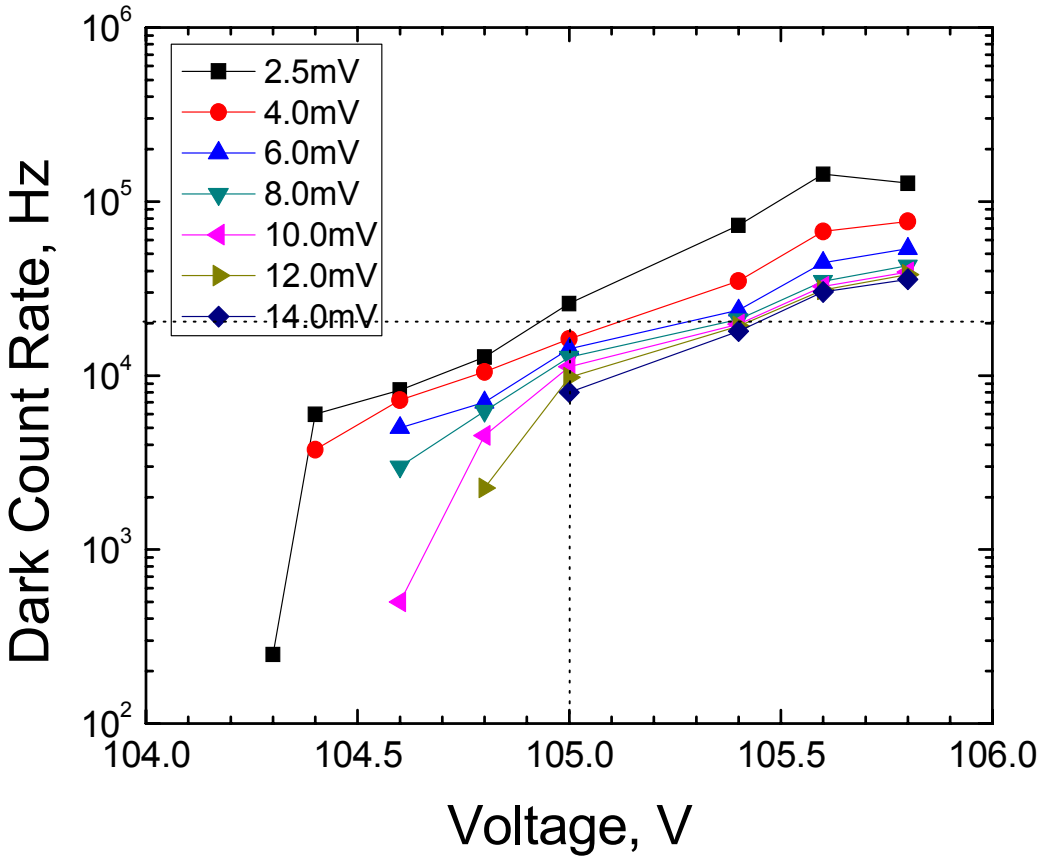


Fig. V-10 Dark count rate measurement for a small bevel SiC SPAD.

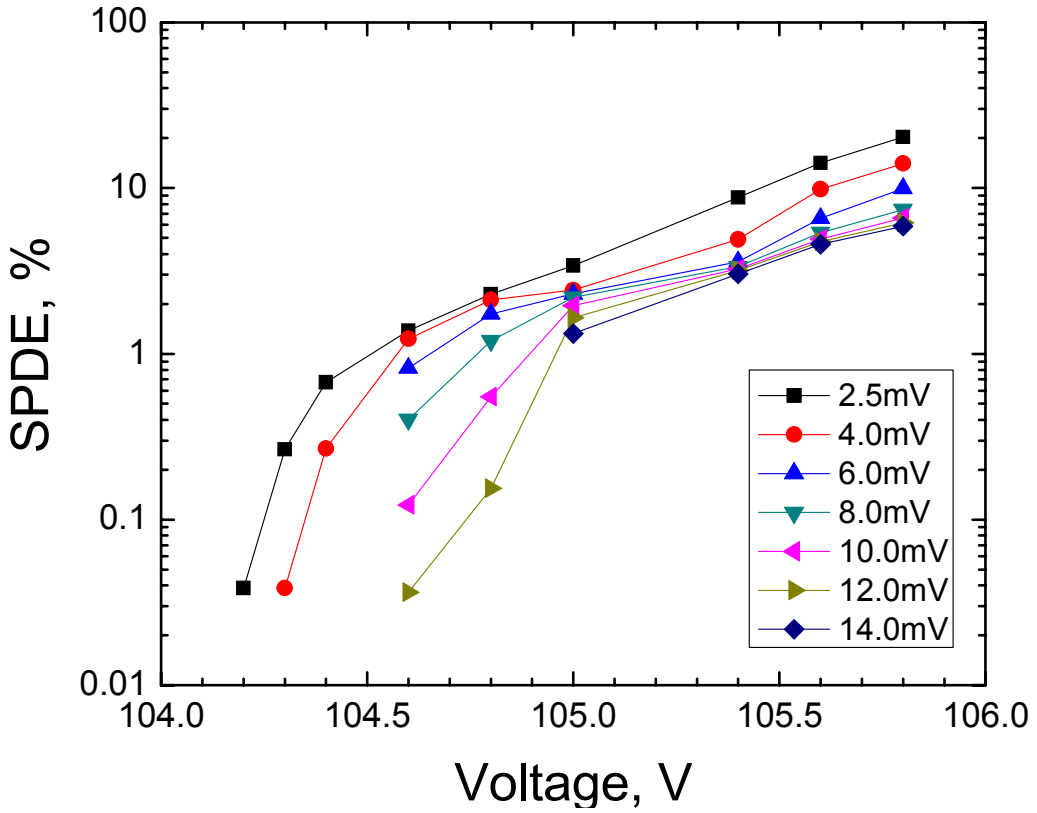


Fig. V-11 Single photon detection efficiency measurement for a small bevel SiC SPAD.

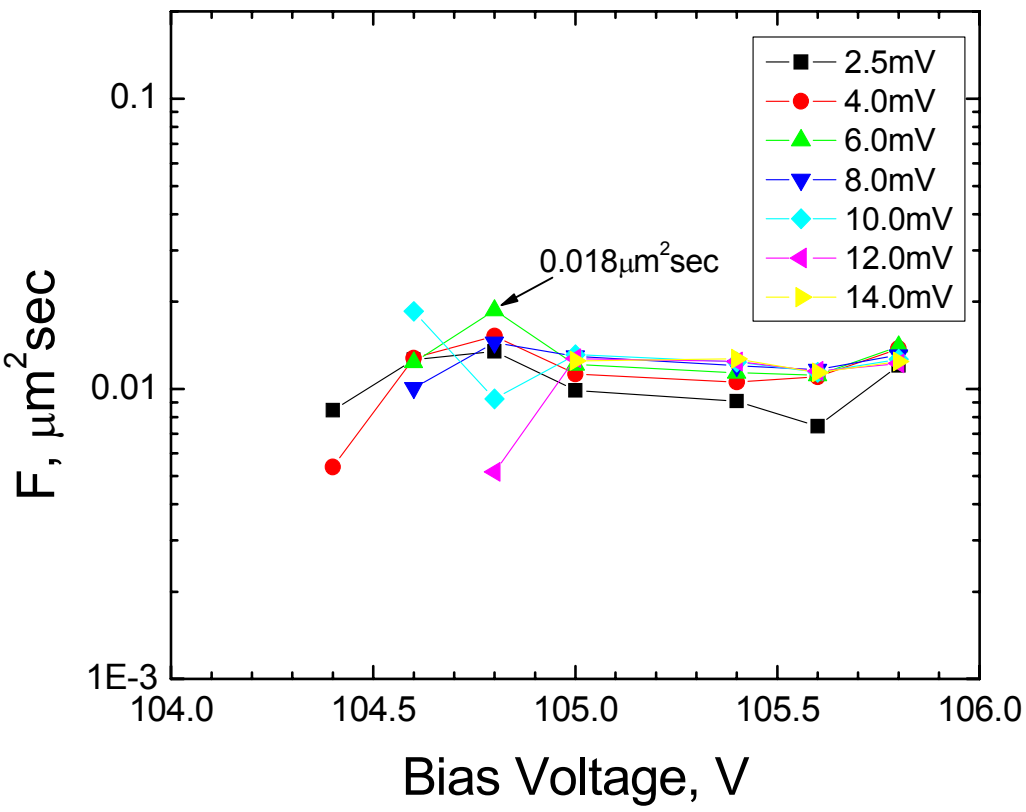
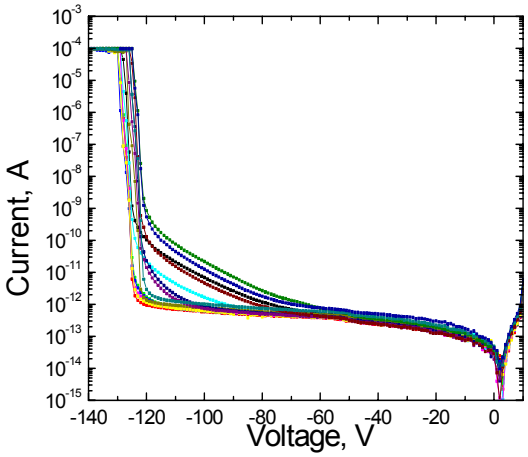


Fig. V-12 Calculation of F as a function of bias voltage and threshold voltage.

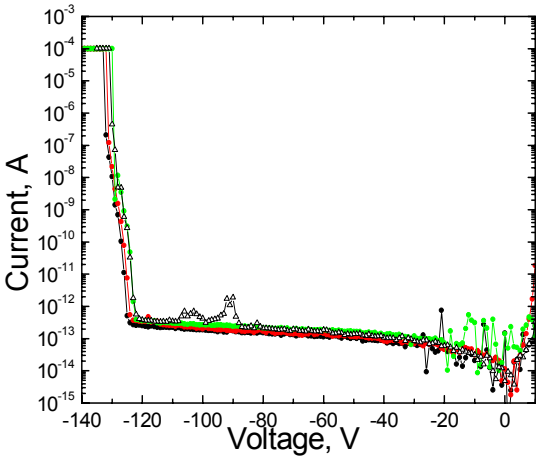
5.2 MJTE sample

5.2.1 Processing of sample AD-B MJTE sample: MJTE

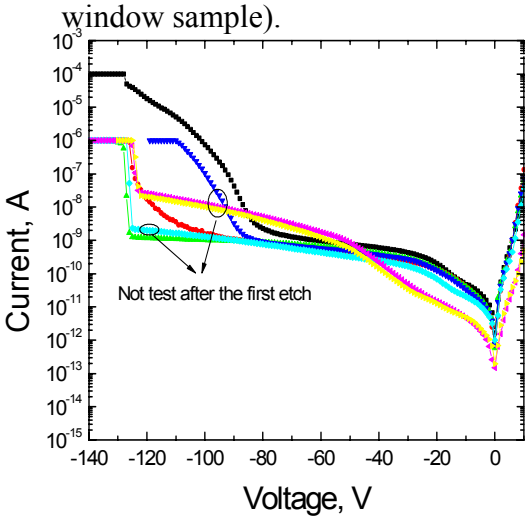
The processing of MJTE optimization confirms the SIMS measurement and simulation results. The lightly doped p layer does not provide enough charges to compensation the positive charges in the depleted n-layer at breakdown voltage. Thus the depletion region extends slightly into the p++ layer. As a result, the voltage corresponding to the lowest dark current when the p++ layer on a JTE step is just barely removed. Then depending on which one of the three JTE steps touches p layer, the "optimum" depth varies and shows a difference of 300Å, which is the JTE step depth. In Fig. V-13, the "optimum" depth is 1700Å where the lowest (outmost) JTE touches the p layer. In Fig. V-14, the "optimum" depth is one JTE step height lower, implying the next step touches the p layer. Several factors make the MJTE more difficult than the regular case. First, even a very thin p++ layer (such as a few Å after oxidation) remains on top of JTE step will be very conductive and disable the JTE effect. Also because the oxidation consumption on the p++ layer (~500Å/3hour) is faster than p layer (~350Å/3hour), plus the etching depth uncertainties, it is difficult to precisely control the etching depth within a few Å so that p++ layer is just consumed in oxidation. There is no other choice but making over etching to ensure the p++ layer is completely removed. There is another factor which will introduce extra charges: surface charges. The surface charges tend to deplete the JTE step so that there is a larger tolerance on etching. The remaining process steps are identical to the bevel samples, including oxidation, silicon nitride window opening, front and bake side metal formation, and corresponding metal annealing. A fabricated SiC SPAD is shown in Fig. V-15.



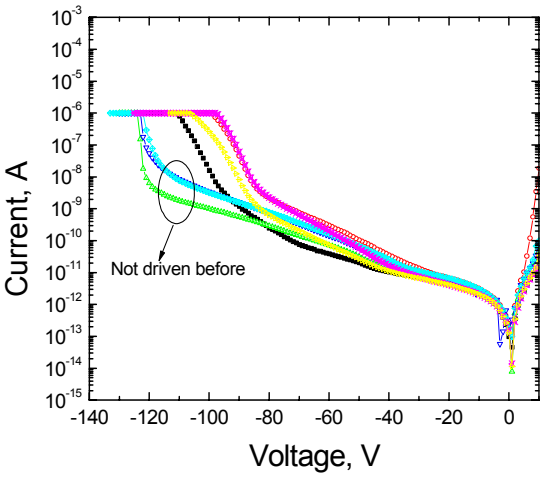
(a) After removing the p++ layer (etching depth ~1700A on JTE1) on top of JTE3 (Φ50um optical window sample).



(b) After removing the p++ layer (etching depth ~1700A on JTE1) on top of JTE3 (Testing APDs).



(c) With etching of 1880A (Φ50um optical window sample).



(d) With etching of 2300A (Φ50um optical window sample)

Fig. V-13 The JTE1 optimization for the first dummy sample AD-A2 of the 2nd set samples.

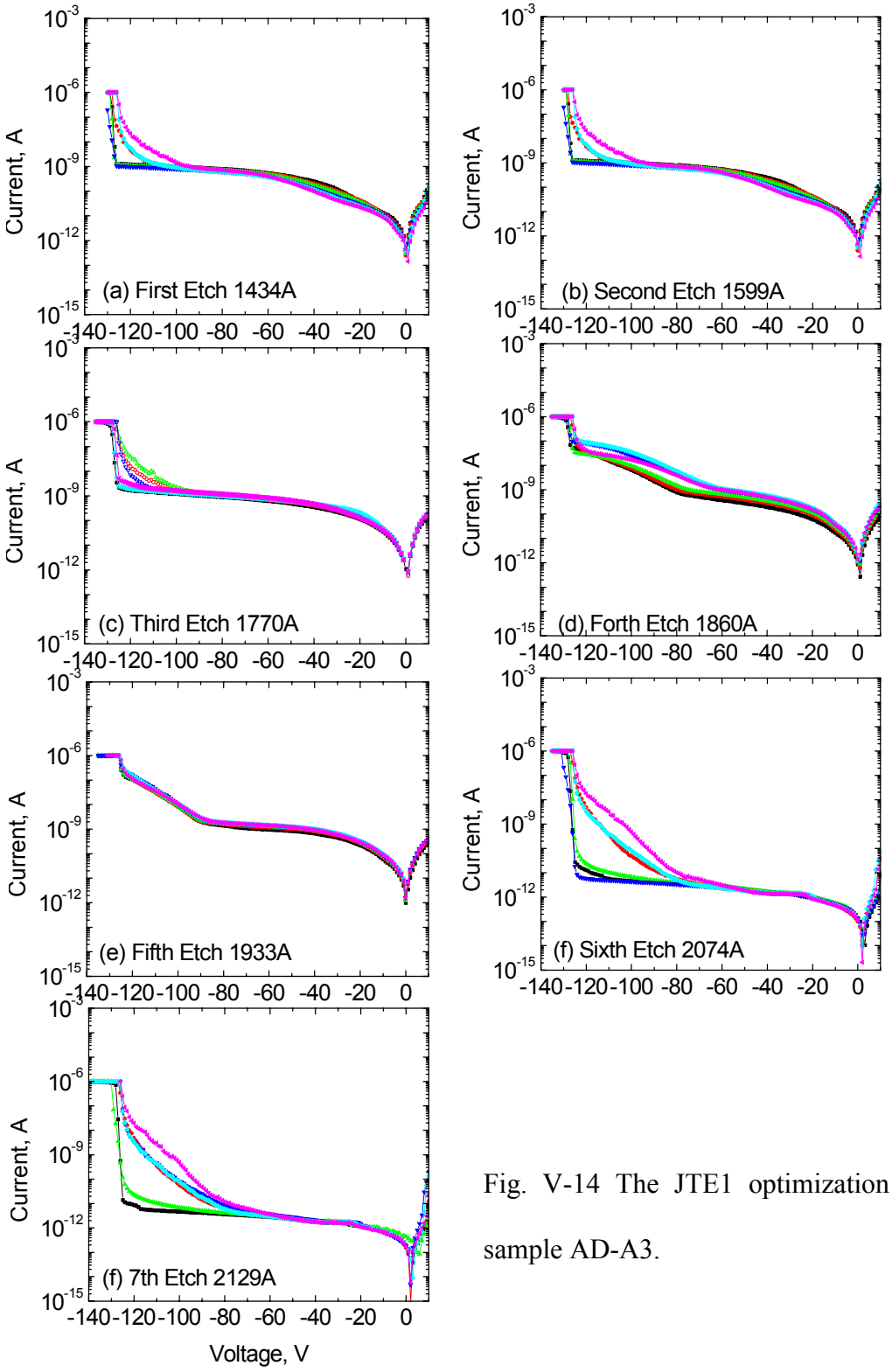


Fig. V-14 The JTE1 optimization of sample AD-A3.

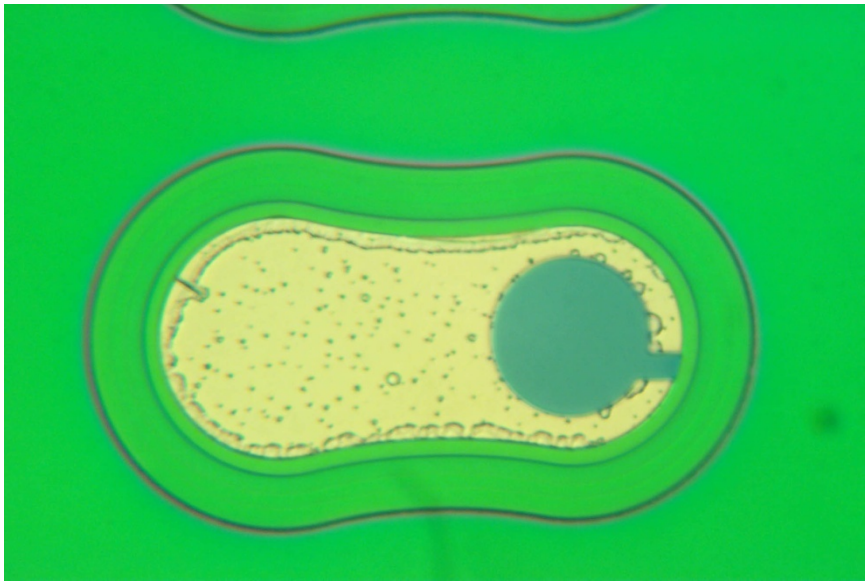


Fig. V-15 A fabricated MJTE device with Φ50μm optical window.

5.2.2 I-V and Gain measurement for AD-B MJTE sample

The I-V measurement result for some good devices with Φ50μm optical window after all the processing steps is shown in Fig. V-16. The dark current at 90% V_{br} is about 54fA. The device has an area of 23,850μm^2. Thus the dark current density is 0.23nA/cm^2. In comparison to the first SiC SPAD with 27nA/cm^2 dark current density at 90% V_{br}, the dark current density for the improved SiC SPAD is about 117× lower. The gain measurement result is shown in Fig. V-17.

It is interesting that the light current is increased when the bias is above 50V. The behavior implies that it is a SAM diode. More evidences will be provided in the quantum efficiency measurement section.

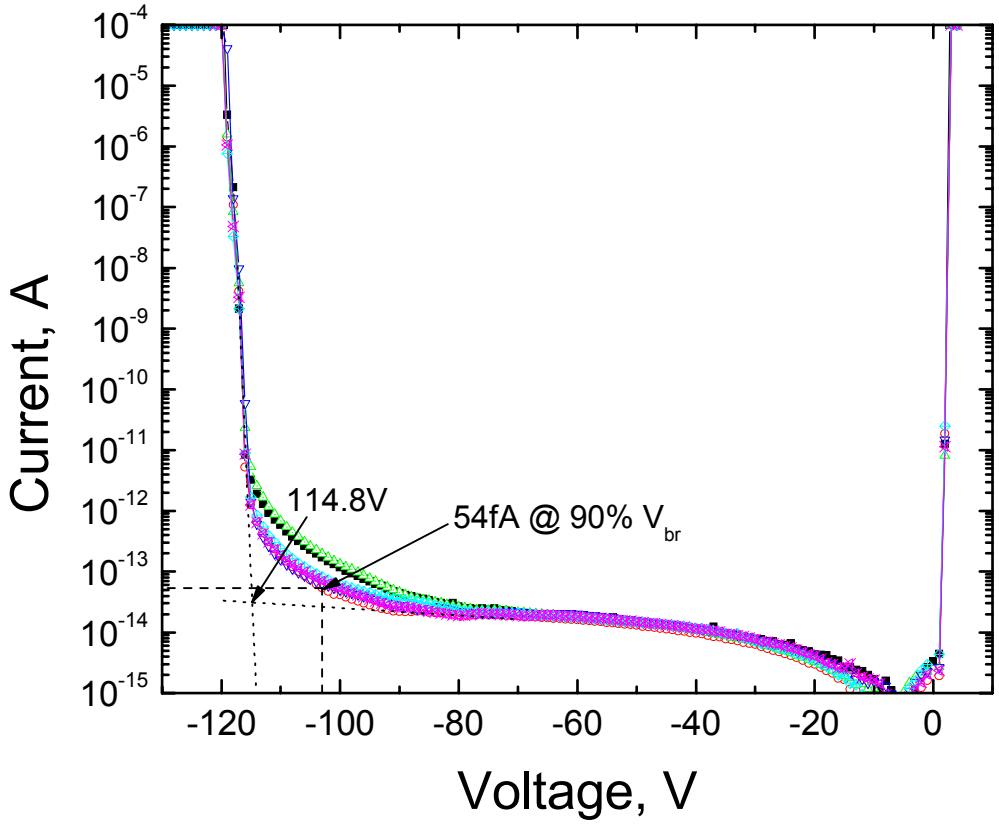


Fig. V-16 I-V measurement for some good devices with Φ50μm optical window.

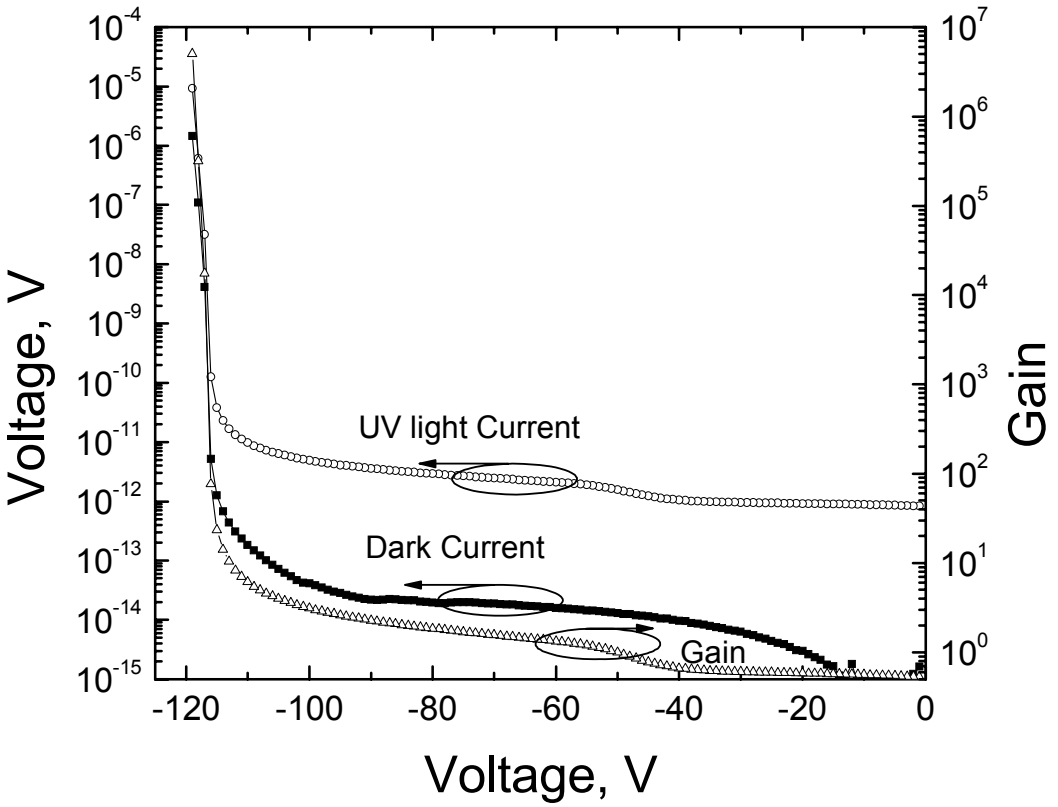


Fig. V-17 I-V and Gain measurement for a MJTE SiC SPAD

5.2.3 Quantum efficiency measurement

The QE is measured from 240nm to 390nm. The device shows a very good quantum efficiency peaked around 270nm~280nm (Fig. V-8, 58% and 56%). The UV to visible rejection ratio is $>10^5$. Due to the small size of the device, wavelength longer than 390nm is not measured. The fiber system has a cut-off frequency at 240nm, and the shorter wavelength is not measured, either. The margin region on top of the mesa is also considered as active region. The JTE region contribution seems to be negligible. A more accurate QE measurement should use under-fill light injection instead of over-fill light illumination. But such a UV focus probing system is expensive and not available yet and we leave it to future work.

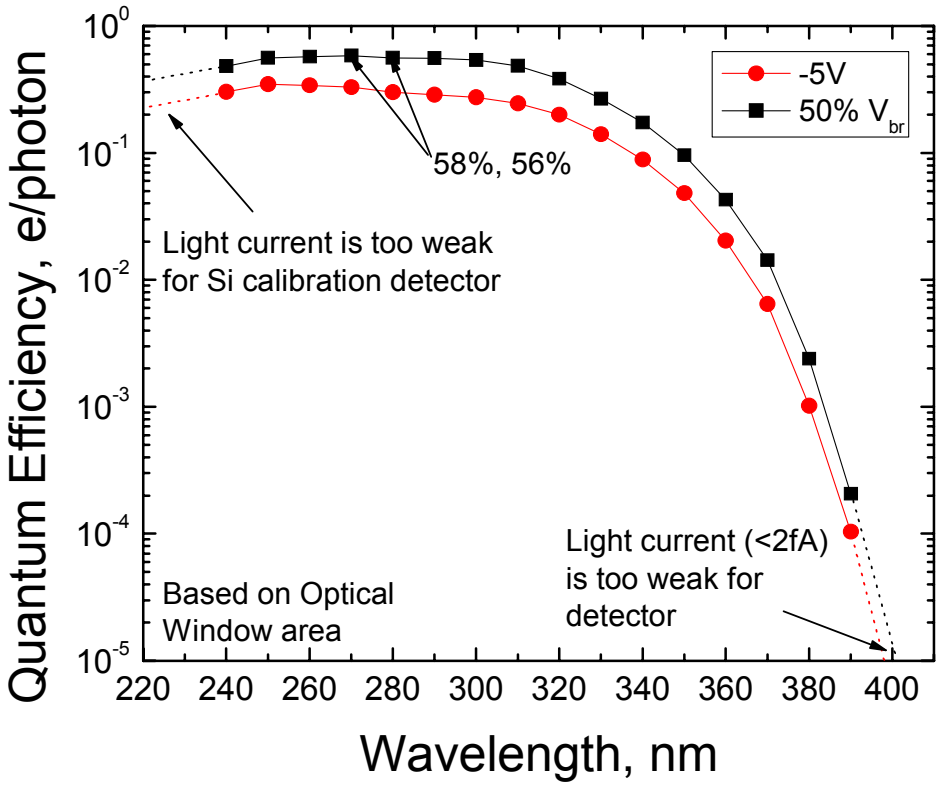


Fig. V-18 QE measurement for a AD-B MJTE device with Φ50μm optical window.

5.2.4 Single Photon Counting Measurement

One of the good devices is measured as shown in Fig. V-19.

Comparing to the previous SiC SPAD UV count waveforms, the waveforms of the MJTE SAM SPAD is clearly different. For 280nm, some of the pulse height is similar to dark counts, while there are some other pulses with higher voltages. The differences becomes more obvious when the illumination is a 350nm LED. The large pulse percentage is significantly higher. Assuming the total pulse number are pulses above 2.5mV (minimum threshold voltage). The percentage of pulse numbers above different threshold voltages are shown in Fig. V-20. There are almost no large pulses with height above 12mV in darkness, but there are many for UV pulses from 350nm LED illuminations.

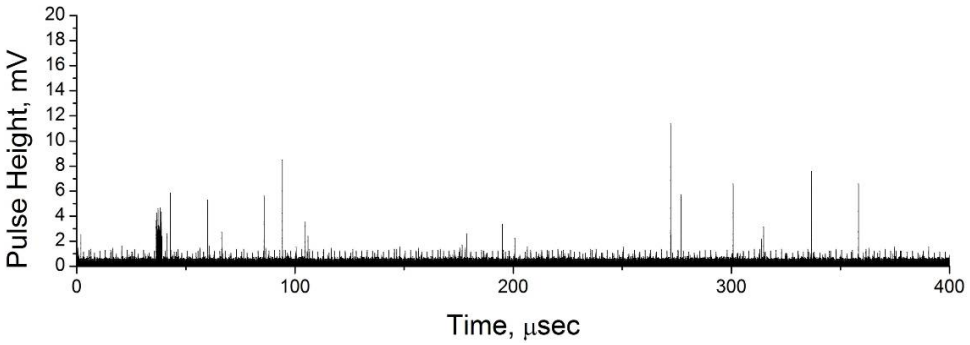
It is known that 4H-SiC has a penetration depth of 34.5μm at 351nm (Fig. I-5). At 350nm, the penetration depth in 4H-SiC is about 34.5μm. With AD wafer structure Fig. II-5, it can be calculated that the top p++ layer absorbs 0.5% of 350nm light, the p and i layers absorb 1.4% and the field confinement n layer and thick absorption layer absorb 8.7% of light. The substrate absorbs ~90% of the light. For the light absorbed in the neutral region (the top p++ and substrate), within a few diffusion length, the photon generated carriers might be diffused into the depletion region and collected. The calculation does not consider surface reflection (there are not enough data for refraction index for 4H-SiC). Thus, majority of the absorbed photons should be located in the thick absorption n- layer if it is fully depleted. The high quantum efficiency and the enhancement of long wavelength QE seems to indicate that the n- layer is depleted. If that is the case, we should observe that the large pulses dominant under 350nm illuminations. Hole injection is the dominant inject for this case. From previous discussions (Fig. I-8), we know that the hole has a higher ionization

coefficient. Thus most of the carriers should experience a full multiplication initiated by holes and the pulses are higher than the pulses initiated by electrons and pulses from carriers generated inside the multiplication region. But only about 20% of pulses are higher than 12mV. The fact probably indicates an existing of hot spots in this device. It is estimated (51) from the average pulse height and pulse width that average gain is in the order of 10^5~10^6 for SiC SPADs. Another research group led by Dr. Joe Campbell carefully studied the gain uniformity of 4H-SiC PiN APDs (55). Their i layer is doped as $2.8\times10^{15}cm^{-3}$ by Al, and the thickness is 1800Å. It is believed that a <10% doping variation in the i layer will cause space non-uniformity when the gain is above 1000. In Geige mode, since the APD needs to be biased at a much higher gain, the spatial non-uniformity could not be negligible. In , we illustrate the hot spot problem associated with the high gain. If a local region (a hot spot) where the doping is slightly higher or the epitaxial layer is thinner than neighboring regions, the breakdown voltage of the hot spot is lower than the adjacent area. Thus when breakdown happens, the carriers in the hot spot will tend to experience a higher multiplication while the contribution of it neighboring region is lower. The problem becomes more and more prominent when the gain is higher and higher. To have a pulse significantly higher than the threshold voltage in order to screen out circuit noises, the gain must be high enough (10^5~10^6). Thus the counting efficiency is mainly limited by the hot spot area. If the epitaxial layer is uniformly doped, then the entire optical window area will be “hot” and effective to multiply carriers. Also, because of the hot spot problem, the counting efficiency will be far away from 100%.

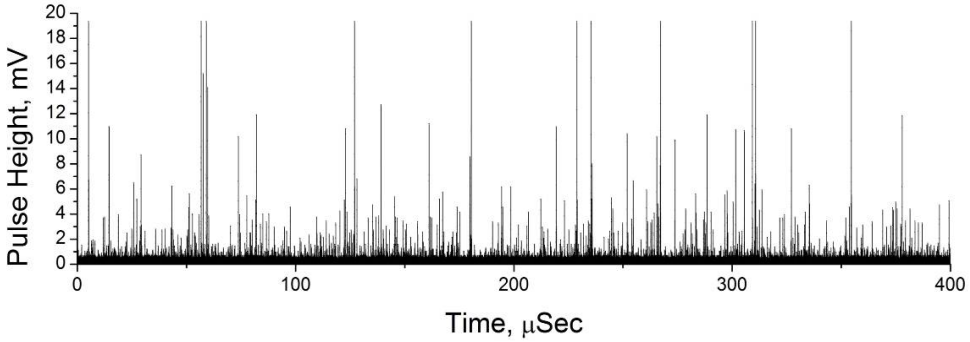
For 280nm case, the penetration depth is estimated in the order of 0.5~1.0μm. If the 280nm UV penetration depth in 4H-SiC is same as that of 6H-SiC (0.7μm), about 22%, 39%,

and 39% of the photons are absorbed in the top p++ layer, p&i layer, and n&n- layer, respectively. For those light absorbed in the multiplication region, the pulse height should be similar to the dark counts, since most of the dark carriers are also generated in the high field multiplication region. For the carriers generated in the n&n- layers, the holes will be driven back to the multiplication region and tend to be fully multiplied, and the pulse height is large.

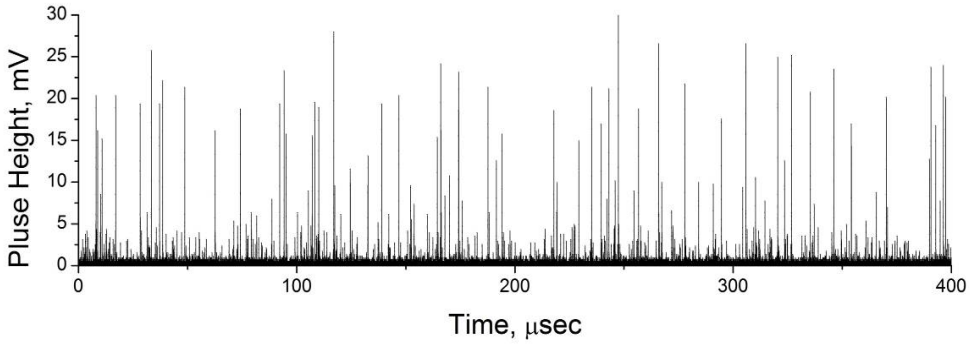
The DCR measurement result is shown in Fig. V-22. The SPDE and F results for 280nm are shown in Fig. V-23 and Fig. V-24. And the SPDE and F for 350nm are shown in Fig. V-25 and Fig. V-26. F peaks around 117.2~117.4V, with a value of $3.0\times10^{-2}\mu m^2$sec (117.2V) and $2.3\times10^{-2}\mu m^2$sec (117.4V) for 280nm, and $0.29\times10^{-2}\mu m^2$sec (117.2V) and $0.51\times10^{-2}\mu m^2$sec (117.4V) for 350nm. The corresponding SPDE/DCR is 4.5%/47kHz 7.4%/60kHz for 280nm, and 0.56%/47kHz 1.2%/60kHz for 350nm, respectively. The CE is 7.5% and 12.3% for 280nm and 6.2% and 13.3% for 350nm, for 117.2V and 117.4V respectively. There are not major differences for CE under different wavelength illumination. Please notice that this device is significantly better than the first SiC SPAD. At 116.4V, the SPDE/DCR for 350nm is 1.2%/60kHz, in comparison to 1.2%/650kHz.



(a) Dark count measurement



(b) UV count measurement under illuminations of 280nm LED



(c) UV count measurement under illuminations of 350nm LED

Fig. V-19 Single photon counting measurement results for a SiC MJTE SAM SPAD.

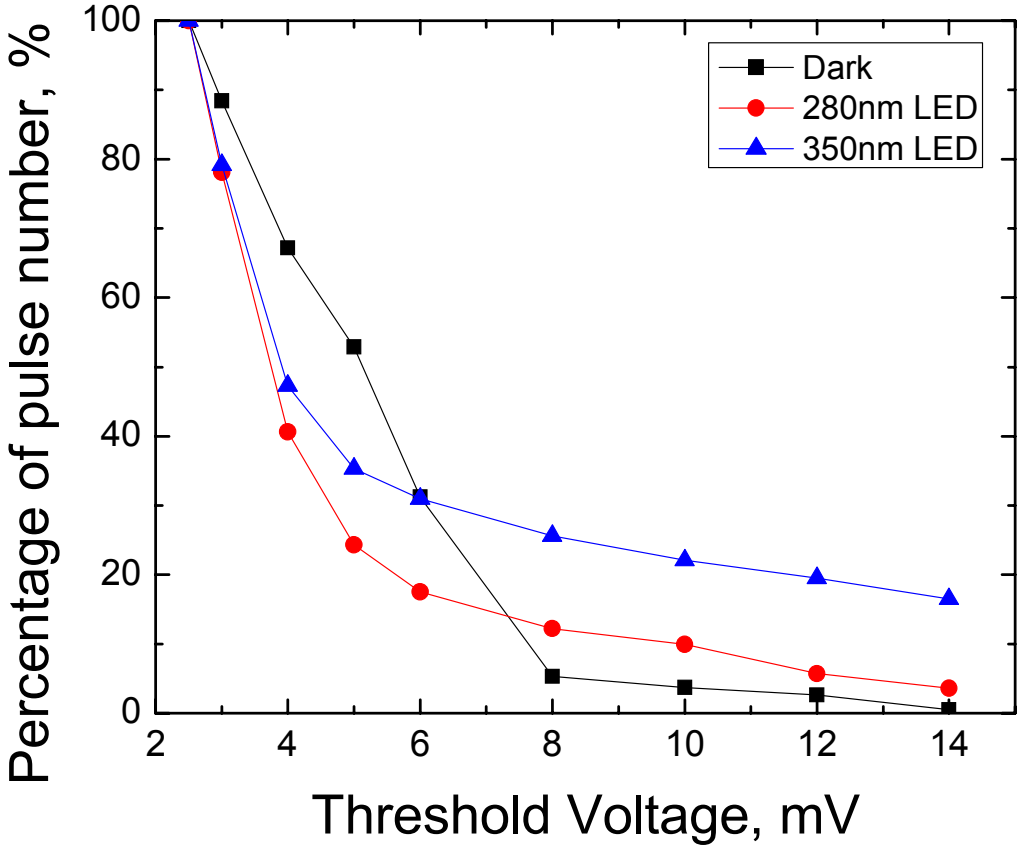


Fig. V-20 Pulse number percentage as a function of threshold voltage for dark counts and UV counts at 280nm and 350nm. The percentage is calculated with a minimum threshold of 2.5mV.

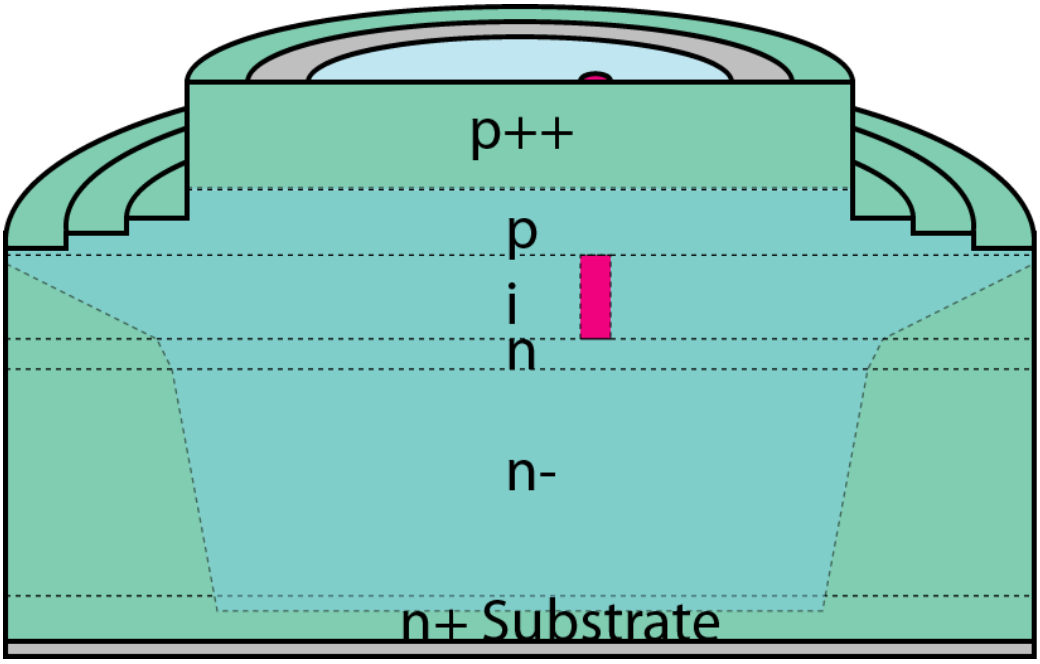


Fig. V-21 Illustration of possible hot pot problem associated with a high gain necessary for SiC SPADs working at Geige mode.

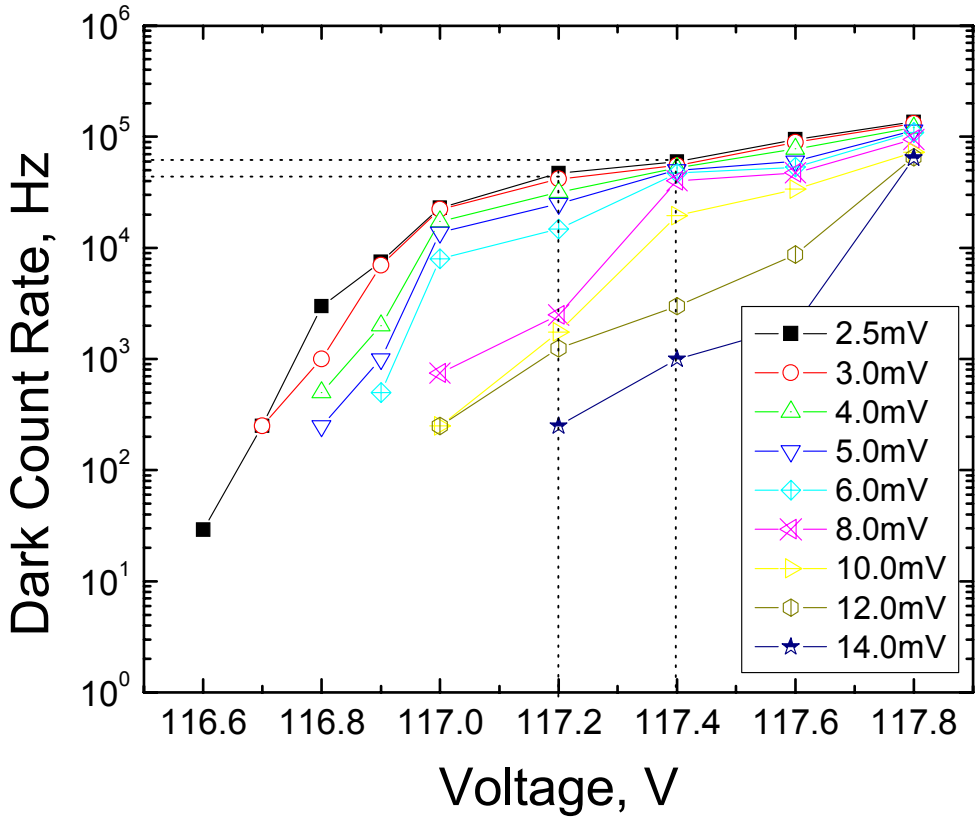


Fig. V-22 Dark count rate measurement result for an AD-B MJTE SPAD with a 50um optical window.

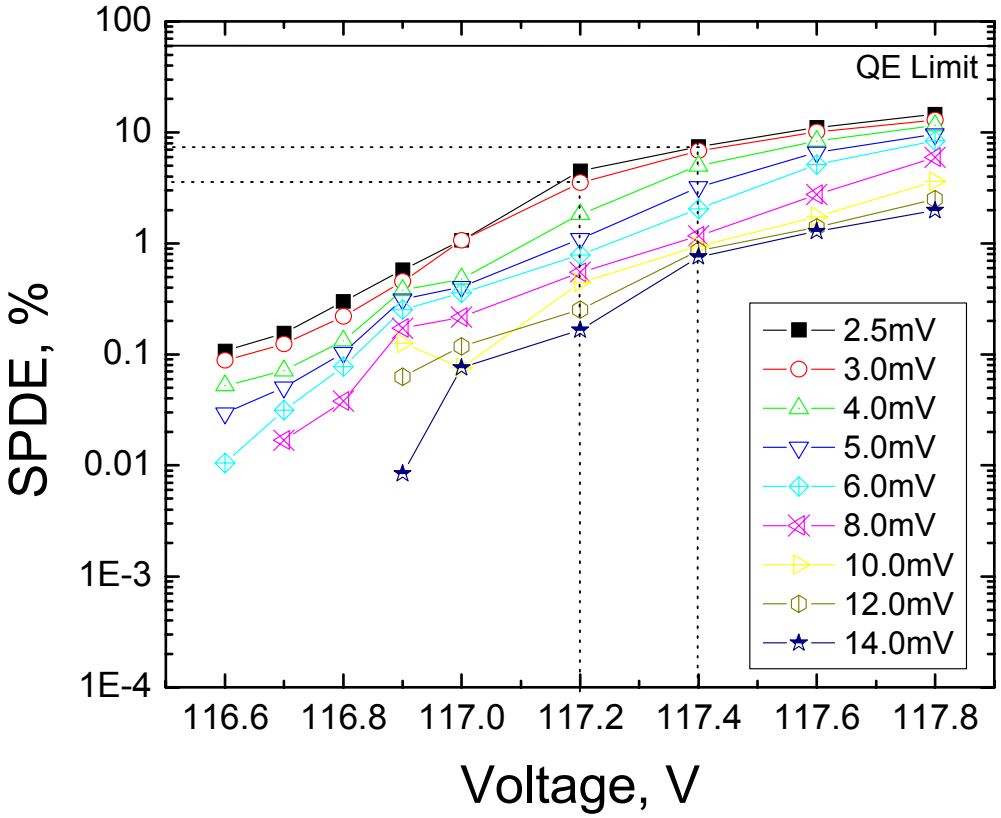


Fig. V-23 SPDE measurement result for a MJTE SPAD with a 50um optical window. The UV light is from a 280nm LED.

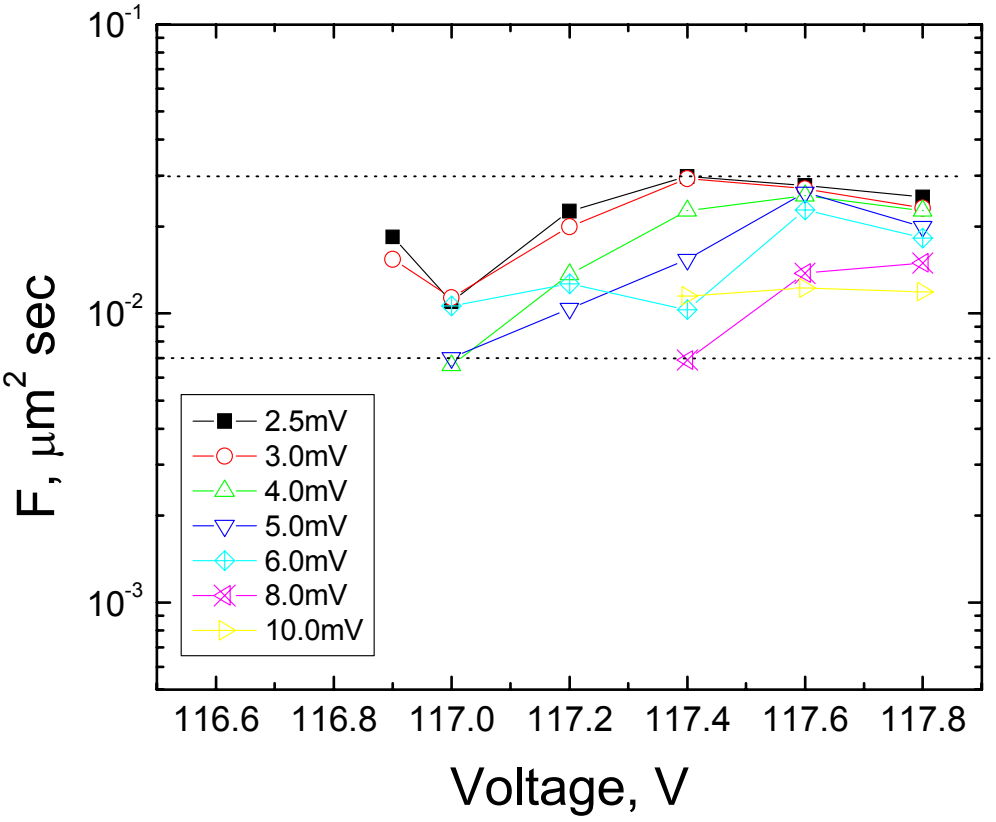


Fig. V-24 Calculation of F from 280nm SPDE and DCR.

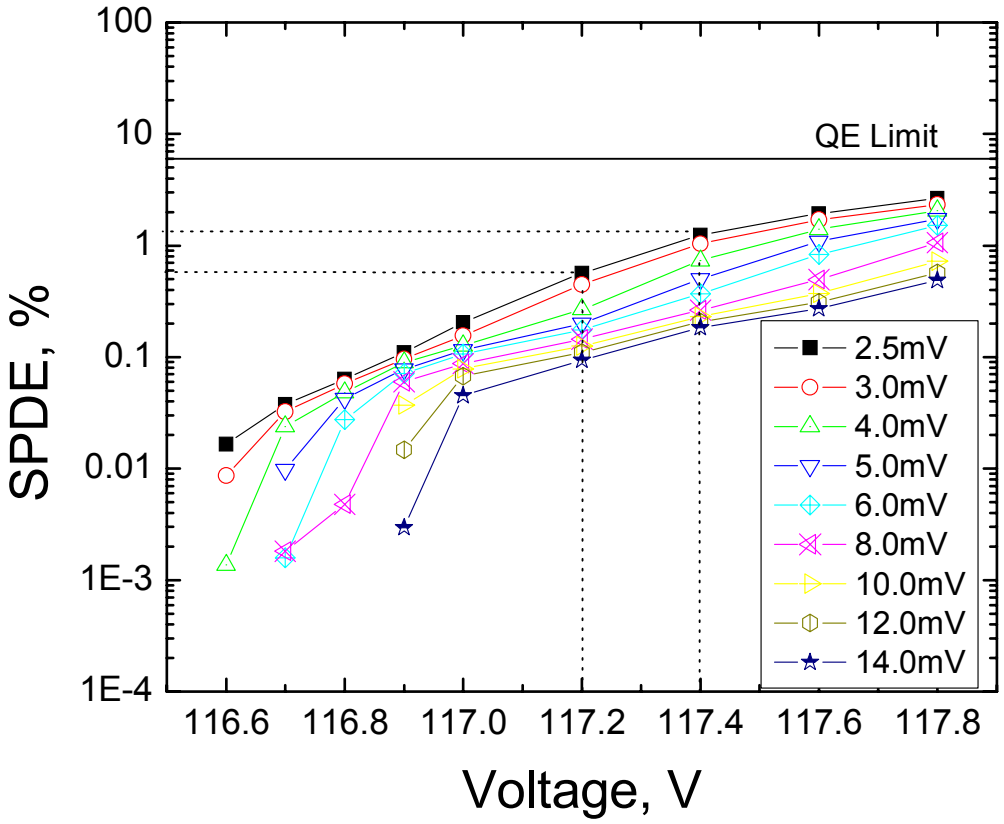


Fig. V-25 SPDE measurement result for a MJTE SPAD with a 50um optical window. The UV light is from a 350nm LED.

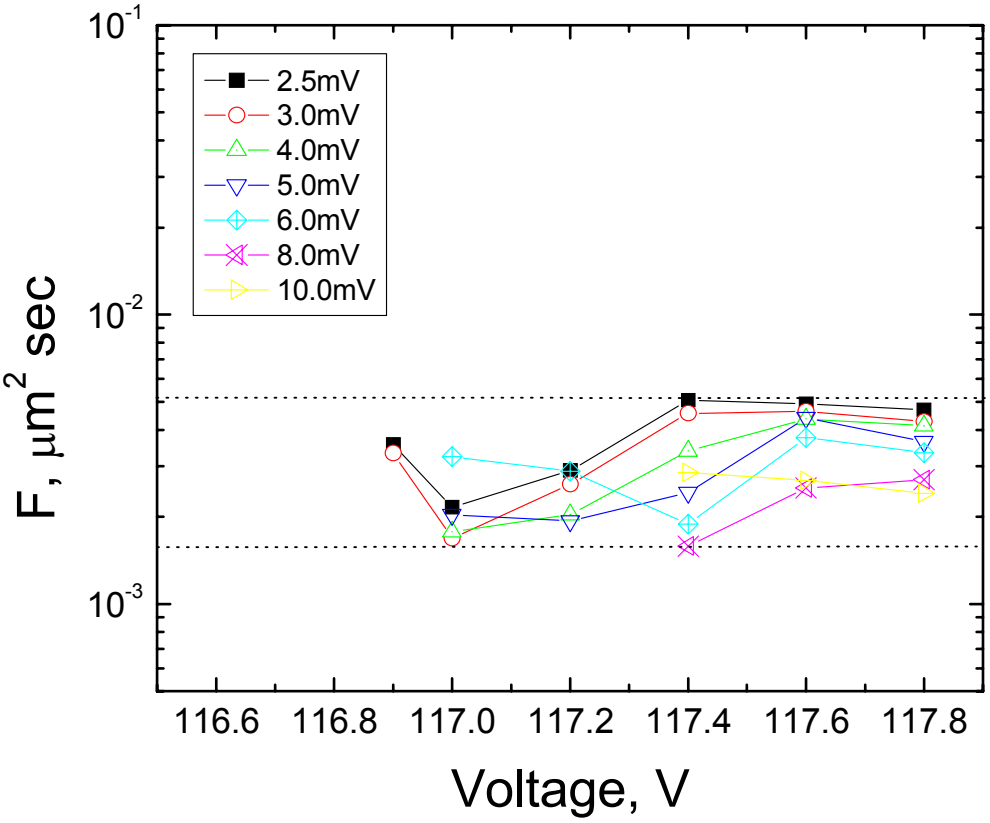


Fig. V-26 Calculation of F from 350nm SPDE and DCR.

5.3 Comparison of fabricated SiC SPADs

The first SiC SPAD has a junction (active) area of $2.4\times10^4\mu m^2$ ($0.36\times10^4\mu m^2$). The bevel SPAD and the MJTE SAM SPAD has a junction (active) area of $0.76\times10^4\mu m^2$ ($0.27\times10^4\mu m^2$) and $2.4\times10^4\mu m^2$ ($0.51\times10^4\mu m^2$), respectively. So the SAM SPAD has a similar area as the first SPAD, but with larger active area. The bevel SPAD is significantly smaller in size.

For the first SiC SPAD under 350nm LED illumination, the SPDE/DCR is 1.2%/650kHz (117.4V). For the SAM SPAD, the SPDE/DCR at the same wavelength is 1.2%/60kHz. Since they have almost identical area, there is more than one order of magnitude improvement in DCR by using the SAM structure.

At 280nm, the SAM SPAD has a SPDE/DCR of 4.5%/47kHz (at 117.2V), and the corresponding value of the small bevel device is 2.28%/12.8kHz (104.8V). Since the small bevel sample area is only 1/3 of the MJTE SAM device, the F is actually slightly lower. This is probably due to a lower QE for the small bevel SPAD.

VI. CONCLUSION AND FUTURE WORK

1. Milestone Works in this Thesis Work

In this thesis work, the world's first SiC SPAD is developed and optimizations on the structure and processing technology are made, which significantly reduce the dark count rate and improves the sensitivity. The milestones of this thesis work includes,

1. The world's first SiC SPAD in 2004.
2. The world's largest SiC SPAD (260μm×260μm) in 2004.
3. A fA measurement system is successfully set up in 2003.
4. A single photon counting measurement system with passive quenching circuit is successfully set up in 2004.
5. A SiC SPAD with the highest gain (10^9) in 2005.
6. A SiC SPAD with the lowest dark current (<4fA at 50% of breakdown voltage and <26fA at 95% of breakdown voltage) in 2007.
7. The improved SiC SAM SPAD with thick absorption layer and high quantum efficiency 58% in 2007. The SPDE/DCR is 4.5%/47kHz at 280nm.
8. A Bevel SiC SPAD with low dark count rate 12.8kHz and high SPDE (2.28% for 280nm) in 2007.
9. New bevel edge termination technology based on CF_4 etching only which gives a photoresist to SiC etching ratio of 4.4:1. It was observed a 3:1 ratio is possible. The original ratio before this thesis work is 15:1 in 2007.

10. New p-type metal recipe which gives low 10^{-4} ~ low $10^{-5}\Omega cm^2$ specific contact resistance for p-type 4H-SiC, which can be doped as low as $6e18cm^{-3}$. The Ohmic contact annealing consumes very minor SiC (<1500A) (2007).

2. Future Work

Other than improving the material quality of 4H-SiC (better doping uniformity, lower defects level, etc.), the future work probably should concentrate on the following aspects in SiC SPADs research:

- Avalanche photo transistor. Photo transistors provide additional gain to avalanche photo diode. The idea is to provide additional gain to the avalanche photo diode so that the gain space uniformity could be improved. A structure of a photo transistor is shown in Fig. VI-1. Two structures might be considered. The top figure shows a structure with emitter on top and avalanche junction (Base-Collector junction) at the bottom, and the bottom figure reverse the sequence so that the quantum efficiency is higher, but it needs really small angle for the edge termination. The additional gain of a photo transistor, which could be easily above 50 according to our power device fabrication, will allow the avalanche diode be biased at a lower voltage, and lead to a possibility of achieving a lower dark count rate.
- Active quenching circuit: Both passive quenching and gate quenching circuit has been studied, but the active quenching circuit for SiC SPADs is not. Active quenching provides the best suppression of after-pulse problem.
- A thicker field-limiting layer and anti-reflection coating towards a higher quantum efficiency and lower dark current. Such a structure can be achieved by using the MJTE structures. As the leakage current will be very low and the traditional MJTE optimization

will not be able to provide an accurate prediction on the device performance. Thus a structure as shown in Fig. VI-2 could be used for determining the optimum MJTE condition. A calculation based on 6H-SiC data is provided in the Appendix B. About 25% of the UV (280nm) is reflected from bare SiC surface. Thus proper anti-reflection coating is necessary for a high QE.

- Gain uniformity study for single photon counting. The gain uniformity for a SiC PiN APD has been studied, but not for SiC SPAD yet. The study will provide very useful information to identify the exact reason of low SPDE for SiC SPADs.
- A better bevel edge termination technology. It has been observed by the author that a P.R. to SiC etching ratio of 3:1 is possible. However, the right condition could not be found again after several etch machine reconstructions. Further study for a smaller bevel angle can lead to a better surface and deeper etching. Also, another ICP system using HCl or BCl_3 has been ordered and it is believed that the HCl or BCl_3 chemical etching of SiC may lead to a smoother surface with less consumption of photoresist.

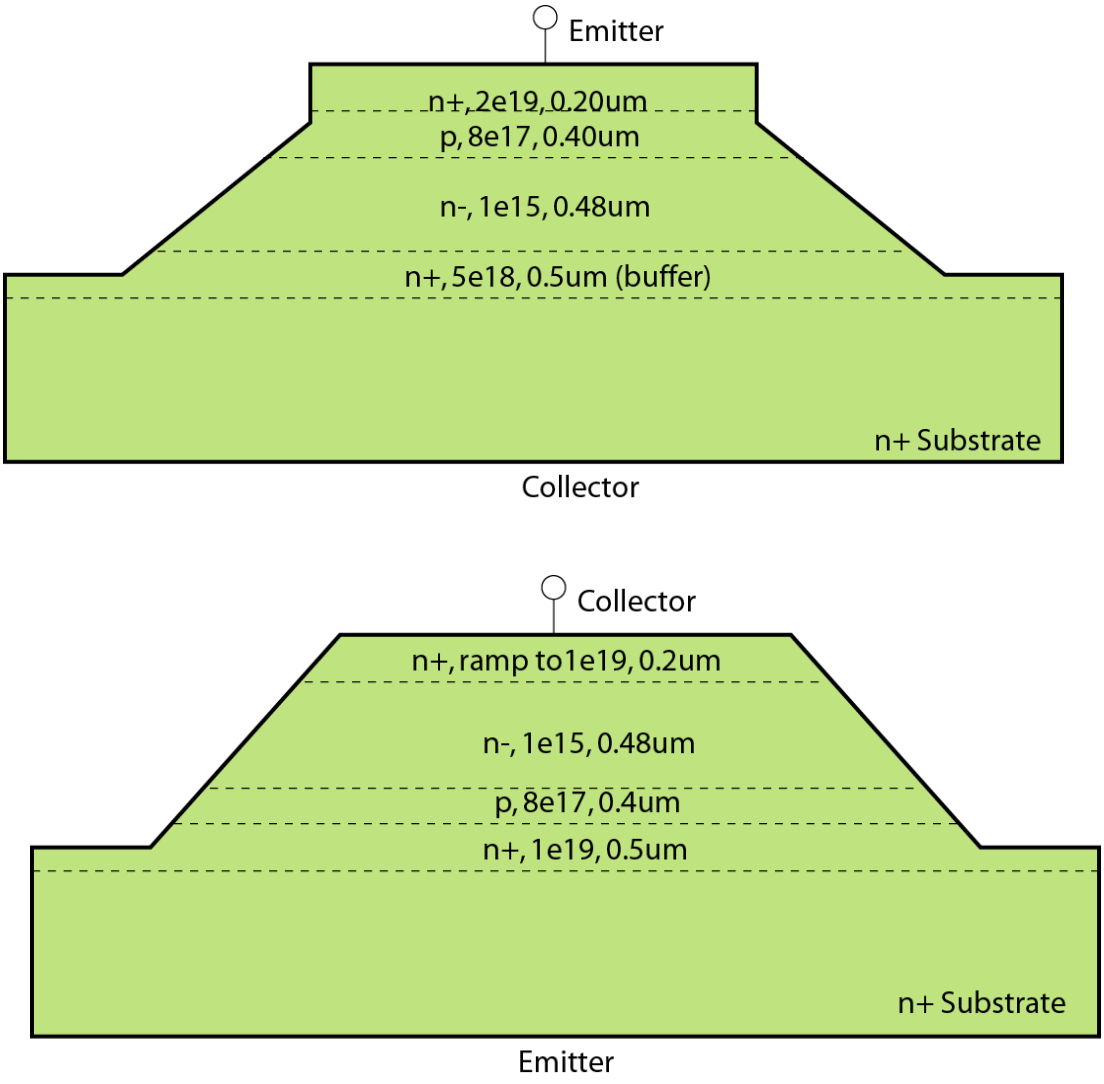


Fig. VI-1 Cross-sectional view of an avalanche photo transistor

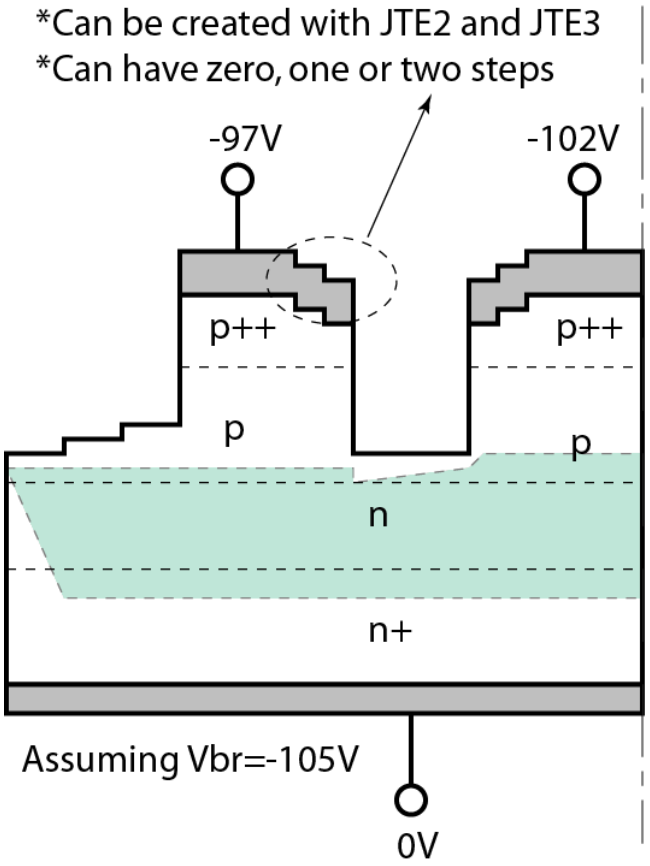


Fig. VI-2 A testing structure for MJTE APD fabrication. The structure is similar to a LJFET with a gate controlled by the substrate. By using one or two steps pre-etching with JTE2 and JTE3 (depending on the oxidation margin and JTE depth), the testing structure allows the actual device to be etched at the same time as the etching of this testing structure—When this structure shows the channel is off, the depletion region is barely touching the top of the first JTE step.

APPENDIX A. MASK-II DESIGN FOR SIC SPADS

APD Mask II is designed for three different vertical structures:

1. MJTE APD (p++ layer is the top epi-layer)----MJTE
2. Beveled APD (p++ layer is the top epi-layer)—Bevel_T
3. Beveled APD (p++ layer is the top epi-layer)—Bevel_B

The lateral structures have three types:

a. Bonding pad on top of the same mesa as the device (Type A)

b. Bonding pad on a different mesa mesa with polyimide separating them (Type C)

c. Particle detector without optical window (Type P)

Of all the nine possible combinations, the following combinations are of particular interest for several proposal reports:

- MJTE-C has minimum mesa size and is possible for minimum dark count rate
- Bevel_B-C is the most complicated structure in terms of processing--all masks are needed.
- Bevel_B-A: good candidate for linear array
- MJTE-A has the simplest processing: good candidate for linear array
- MJTE-P: for particles detection

For illustration, MJTE-C (Φ30μm), Bevel_B-C (Φ30μm), Bevel_B-A (Φ50μm), MJTE-A (Φ50μm), and MJTE-P (Φ250μm) cross-sectional views (Fig. E1-E5) are plotted. All dimensions are drawn to scale unless it is too small (for example, MJTE steps are exaggerated and thus are not drawn to scale). Fig. E6-E15 shows the mask design.

Though there is not enough time and budget during this thesis work for more research studies such as speed measurement, excess noises and a upside-down SAM (with absorption layer on the top), the Mask-II set are designed with additional features of front metal contact for substrate for all these purpose.

[1] Upside down n/p structure as shown in Fig.E-2. For SAM structures, the solar blind wavelength penetration depth is not very deep (in the order of 1μm). Thus the absorption layer is preferred to be on top of the multiplication region. Moreover, hole injection is preferred for a high ionization rate and low excess noise. Thus, the n layer should be designed on the very top and p layer should be designed at the bottom. As the p-type SiC substrate is not mature yet, a thick p layer has to be grown in a n+ type substrate to ensure a high quality epitaxial grown. In such a case, a substrate contact has to be in the front.

[2] The SiC SPAP has very noise power which makes the excess noise measurement not easy. Other research groups have confirmed that the noise power is in the order of -110dbm in comparison to a standard 50Ω resistor. In such a case, the external noise has to be suppressed to below this level. If one uses one RF cable to probe p and another RF cable to probe n, the noise introduce will be much higher than -110dbm. The two terminals of the device have to be probed on the front side by the same RF probe. In such a case, the front substrate contact has to be made.

[3] The speed of a Si SPAD could be easily in the a few GHz range. There is no speed measurement for SiC SPAD, but we would expect it also in the RF range. In such a case, a front substrate contact will make the speed measurement easier, though there are some tricks when such a contact is not available. One of such tricks is to use a probe which has a three-tip probe and use the neighboring devices as the bottom contact since they are forward biased.

The tip spacing has to match the period of the mask design between devices. Also, additional noises are introduced in such a case. A front substrate contact will overcome these problems.

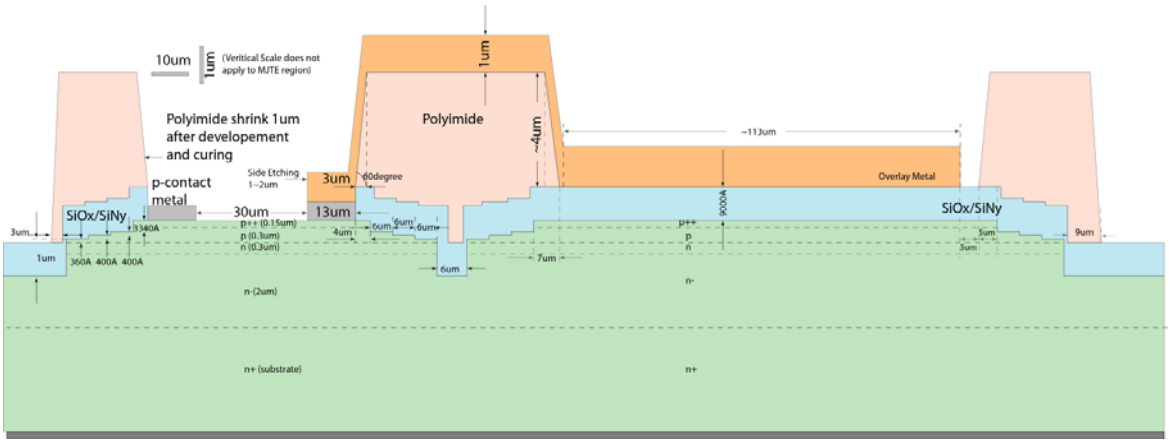


Fig. E-1 MJTE-C (Φ30um optical window)

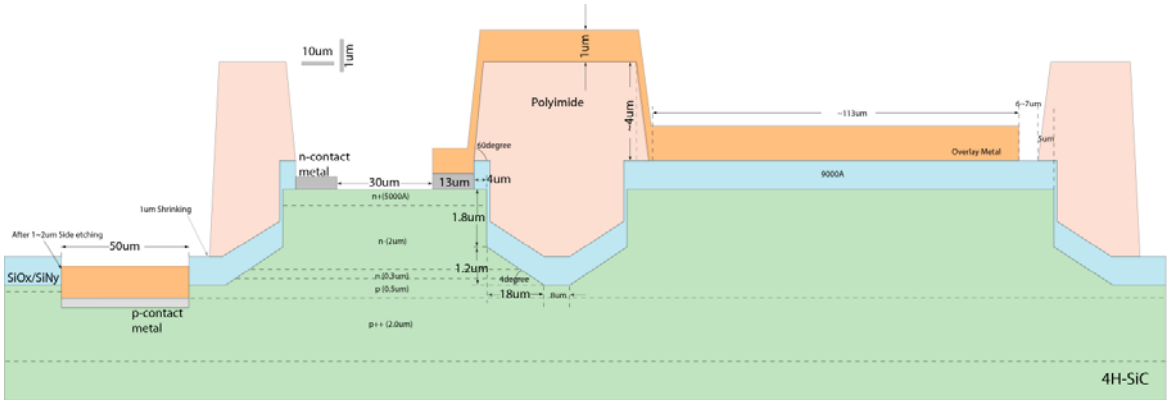


Fig. E-2 Bevel_B-C (Φ30um optical window)

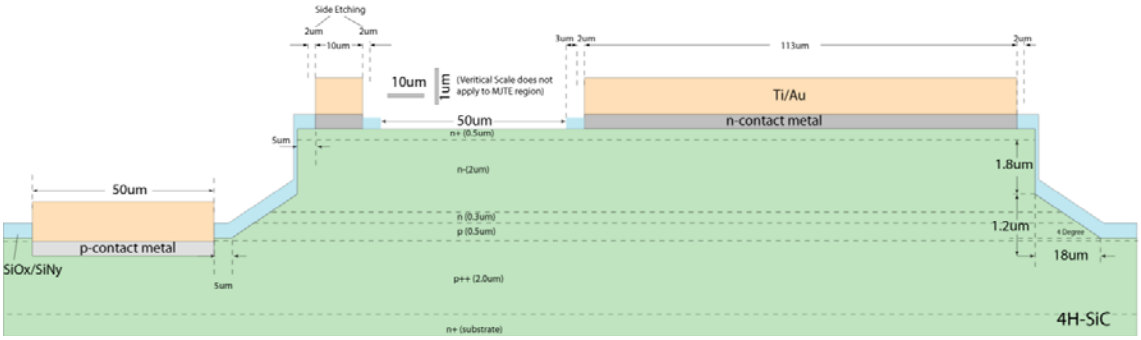


Fig. E-3 Bevel_B-A (Φ50um optical window)

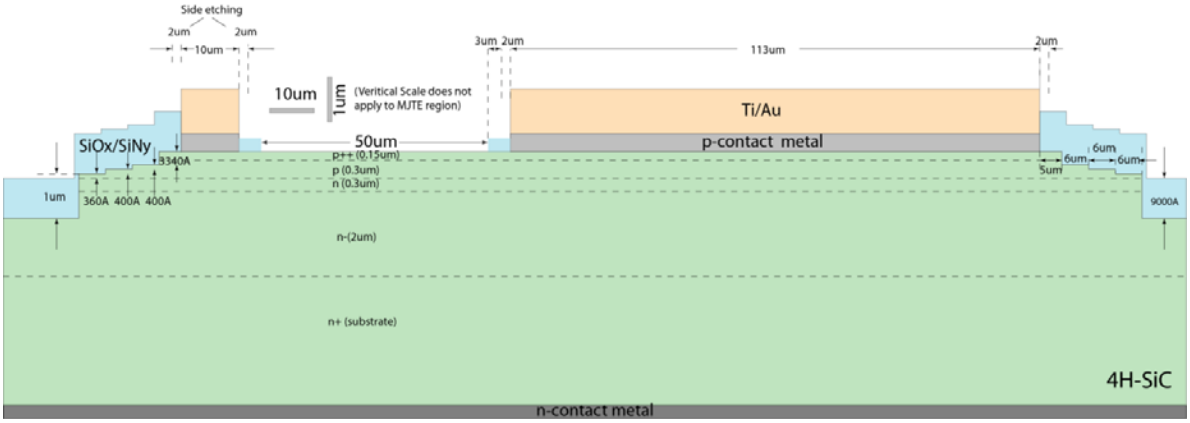


Fig. E-4 MJTE-A (Φ50μm optical window)

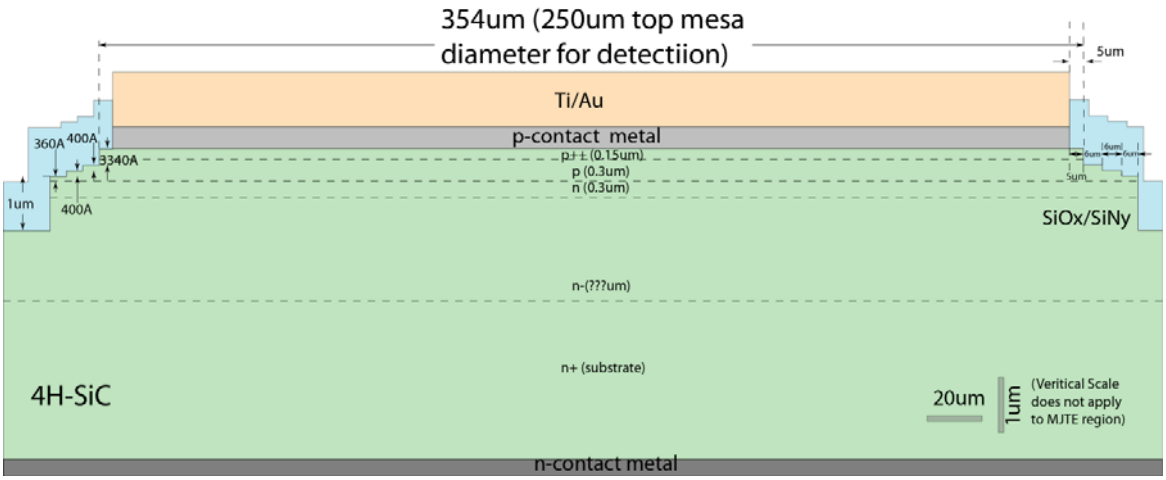


Fig. E-5 MJTE-P (Φ250μm detection area)

A. Linear Array Type A and Type P:

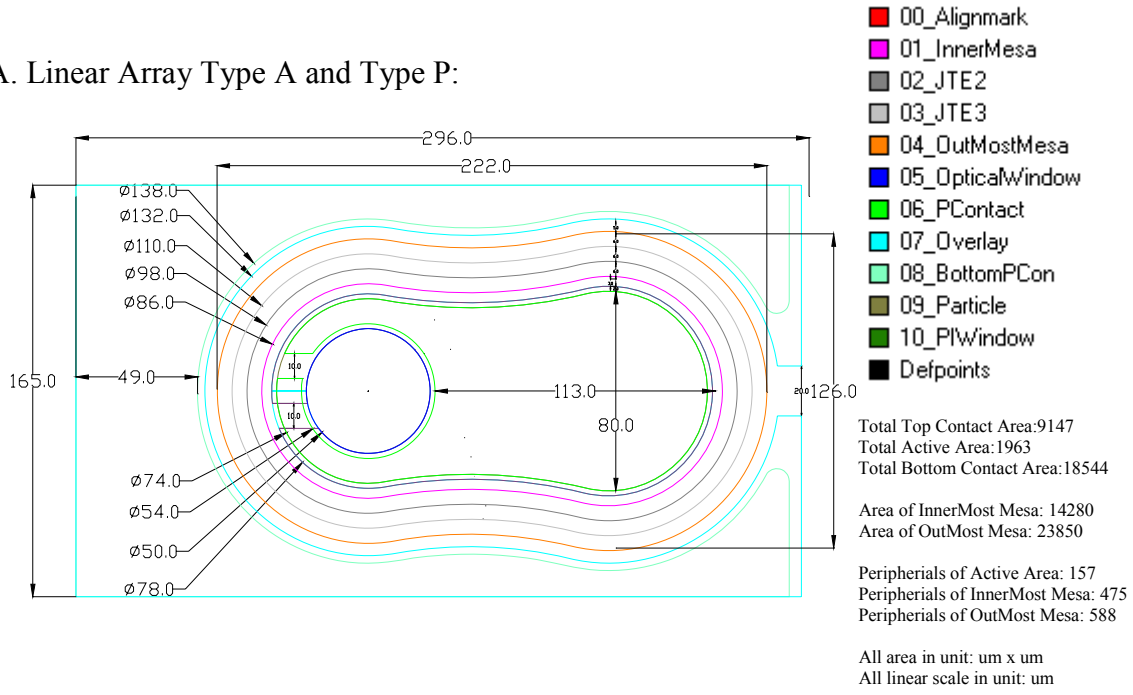


Fig. E-6. Φ50μm Optical Window Type A Devices

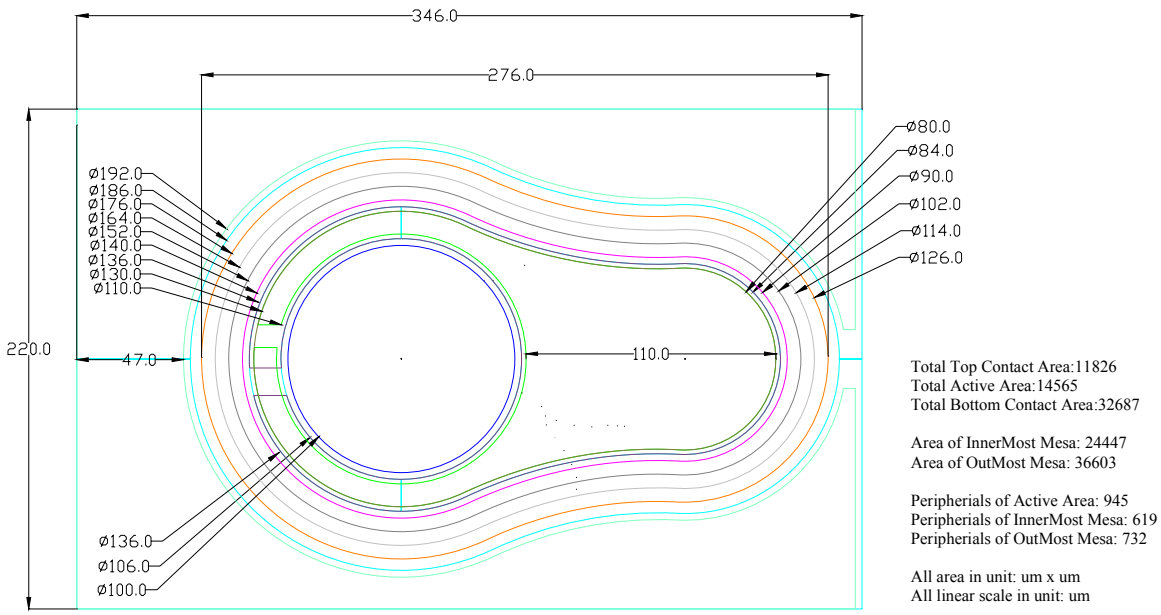


Fig. E-7. Φ100μm Optical Window Type A Devices

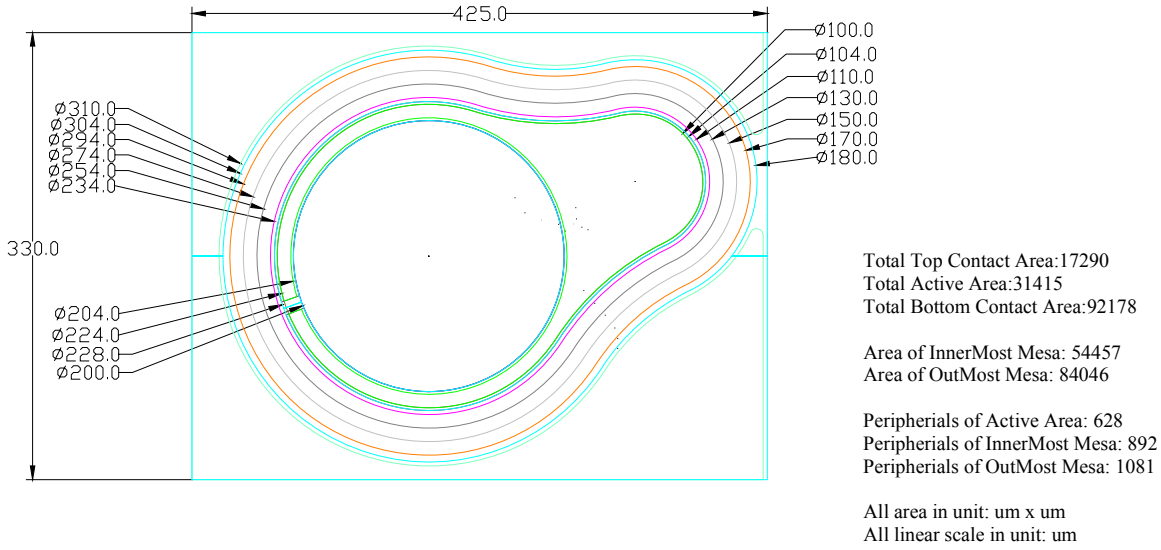


Fig. E-8 Φ200μm (Φ234μm particle) Optical Window Type A Devices (10μm JTE)

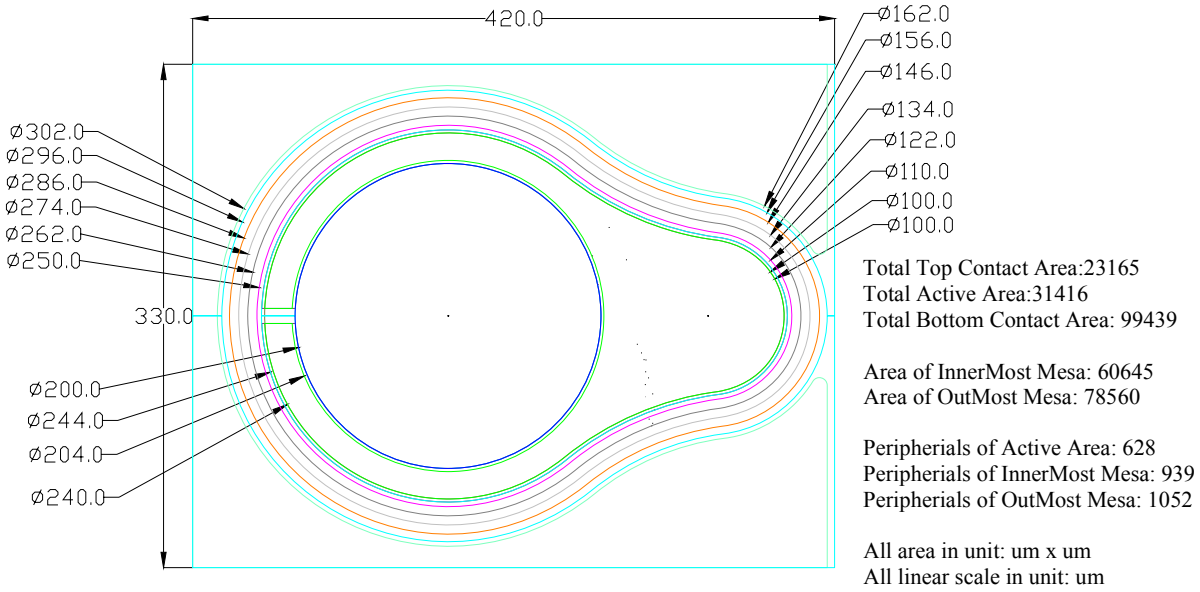


Fig. E-9 Φ200µm (Φ250µm particle) Optical Window Type P Devices (6µm JTE)

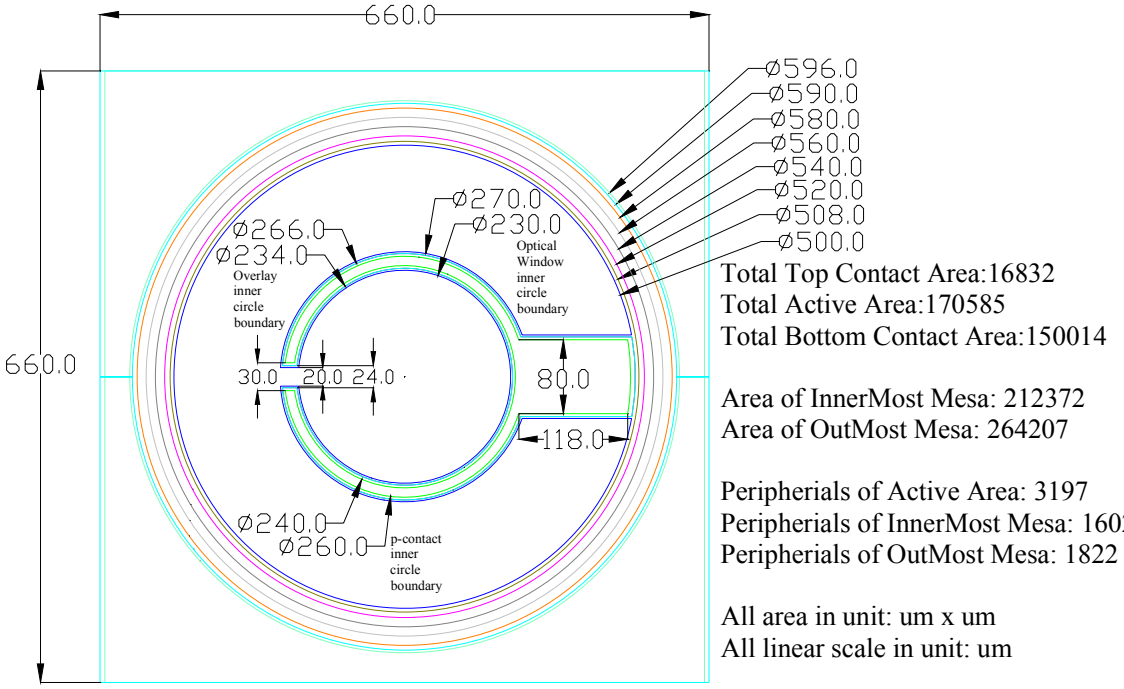


Fig. E-10 Φ500µmA1 Optical Window Type A Devices (10µmJTE)

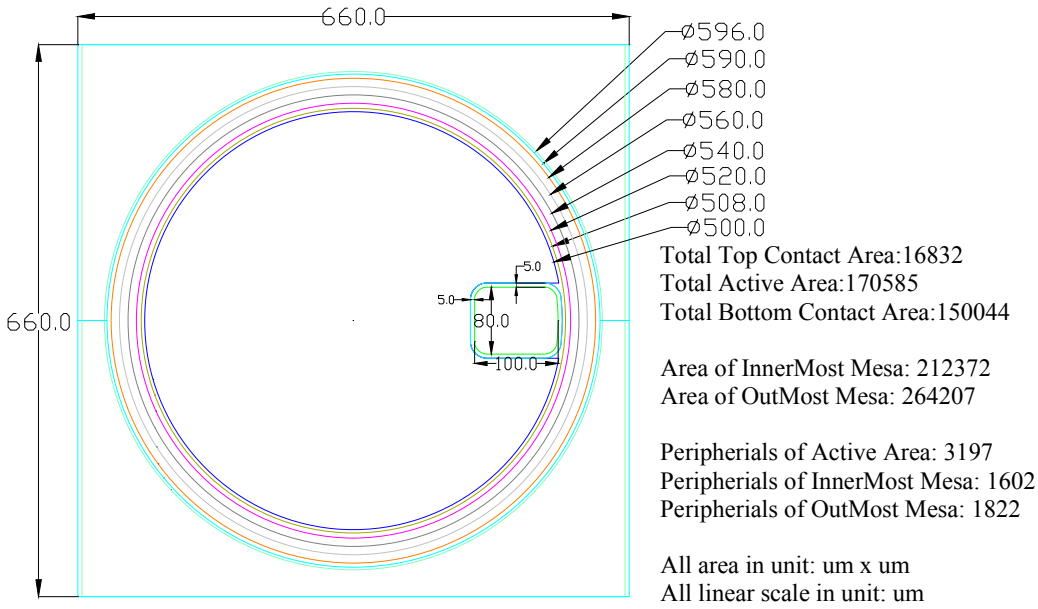


Fig. E-11 Φ500μmA2 Optical Window Type A Devices

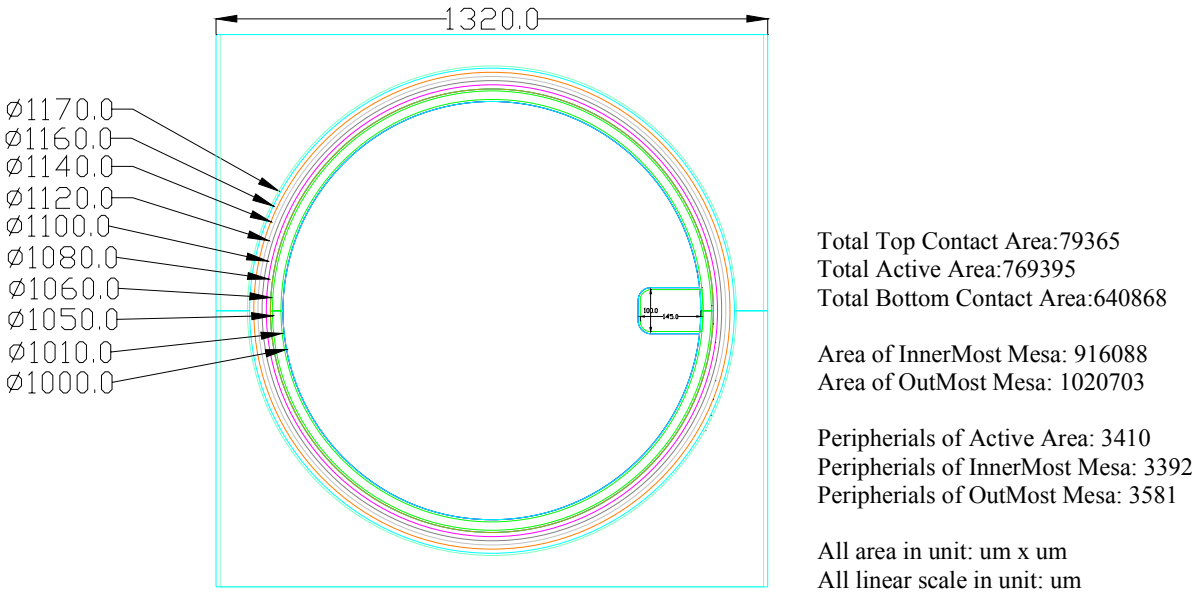


Fig. E-12 Φ1000μm Optical Window Type A Devices

B. Linear Array Type C:

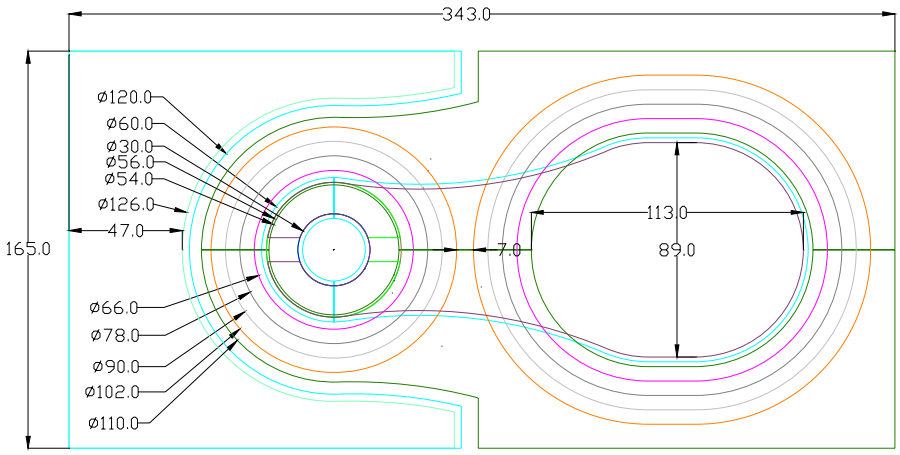


Fig. E-13 Φ30μm Optical Window Type C Devices

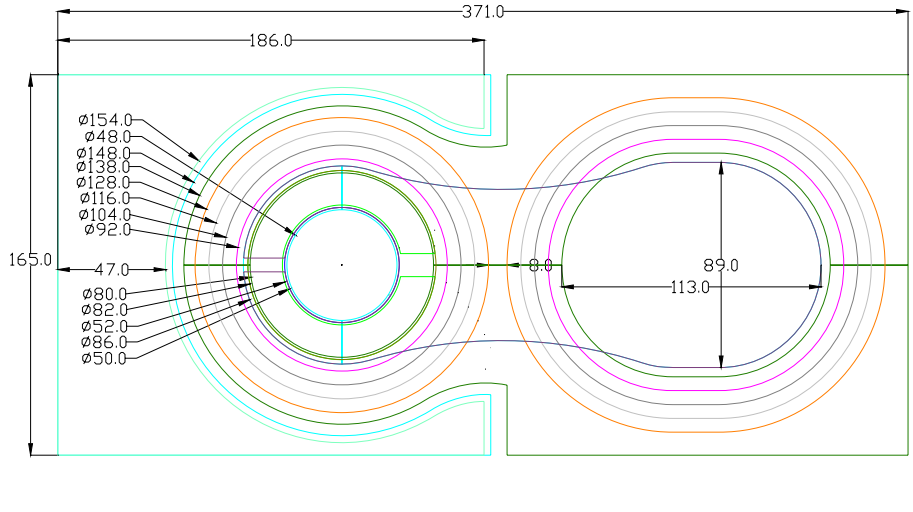


Fig. E-14 Φ50μm Optical Window Type C Devices

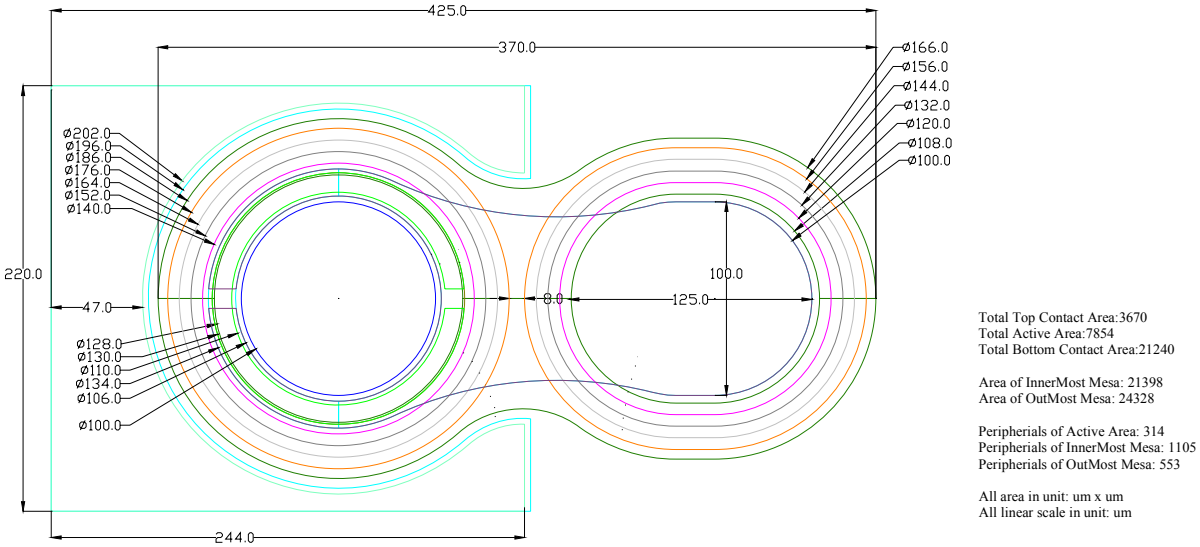


Fig. E-15 Φ100μm Optical Window Type C Devices

APPENDIX B. ANTI-REFLECTION COATING FOR SOLAR BLIND WAVELENGTH

This is a preliminary study for anti-reflection (AR) coating for SiC. As there are no refraction index data for 4H-SiC, the calculation is based on data of 6H-SiC. Also, the refraction index data for SiO_2 and Si_3N_4 grown in our lab is not calibrated for the UV wavelength, since we do not have proper instruments for the purpose. All data used for this calculation are from references (15). According to our experimental study on Si_3N_4 at infrared wavelength (1.55μm), our PECVD grown Si_3N_4 layer has very accurate thickness (1%), and refraction index varies from 1.96~2.04 (about ±2%). During Si_3N_4 deposition, there are yellow powders (due to not-fully reacted Silane) coated on the wall and some of them might clog the gas flow shower anode. the refraction index of Si_3N_4 will be changed as result of hydrogen trapped in the film. We do not have calibration on SiO_2. Thus, in this calculation, we assume a larger variation range for thickness and refraction index. For single layer, the thickness/refraction index variations are set as ±5%, ±3%; for double-layer and triple-layer, they are ±3% and ±3%.

The calculation shows that without AR coating, the SiC surface will reflect 25% of the UV light at 270nm~280nm. The data used for the calculation is shown in the next page.

Refraction Index:

SiC: (6H-SiC)

λ(nm)	n	k
270	2.98*	0.208*
275.5	2.96	0.203 [2]
280	2.95*	0.199*
290	2.91*	0.191*
300	2.88*	0.182*
310	2.85	0.174[2]

(use this data for all wavelengths)

Si_3N_4:

λ	n	k
261	2.2340	0.0012
270*	2.2117*	0.0006*
275.5	2.1980	0.0002
291.7	2.1670	0
300	2.15*	0*
310	2.1410	0*

SiO_2:

λ	n	k
269.9	1.4981	0*
275.3	1.4959	0*
280.3	1.4940	0*
289.4	1.4910	0*
302.1	1.4872	0*

* No experimental data available. The data shown is either assumed data or data from its neighboring wavelength.

Simulations:

If available, using the refraction index at given wavelength; otherwise, use the data mostly close to it. Simulate λ of 270, 275, 280, 290, 300nm.

Single-Layer AR coating

λ(nm)	Center values of d_{siob}/n_{siob}	Center Reflection	Variations of d_{siob}/n_{siob}	Reflection variations (best~worst)
270nm	1360Å/1.4959	<1.95%	±5%/±3%	1.4%~4.9%
280nm	1398Å/1.4940	<1.95%	±5%/±3%	1.4%~4.8%

Double-Layer AR coating

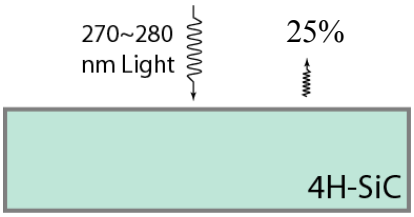
λ(nm)	Center values of d_{sioc}, d_{sinc} / n_{sioc},n_{sinc}	Center Reflection	Variations of d_{sioc}, d_{sinc} /n_{sioc},n_{sinc}	Reflection variations (best~worst)
270nm	1085Å, 788Å/ 1.4959, 2.1980	<0.01%	±3%, ±3%/ ±3%, ±3%	<0.01%~ 4.6%
280nm	1049Å, 763Å/ 1.4940, 2.1980	<0.01%	±3%,±3%/ ±3%, ±3%	<0.01%~ 5.6%

Triple-Layer AR coating

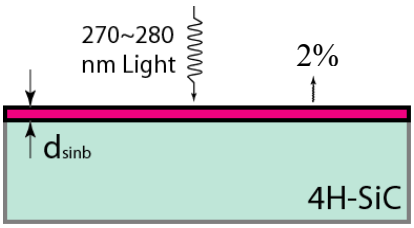
λ(nm)	Center values of d_{siod1}, d_{sind}, d_{siod2}/ n_{siod1}, n_{sind}, n_{siod2}	Center Reflection	Variations* of d_{siod1}, d_{sind}, d_{siod2}/ n_{siod1}, n_{sind}, n_{siod2}	Reflection variations (best~worst)
270nm	1011Å, 688Å, 1103Å / 1.4959, 2.1980, 1.4959	<0.01%	±3%, ±3%, ±3%/ ±3%, ±3%, ±3%	<0.01%~ 5.6%
280nm	1288Å, 801Å,957Å / 1.4940,2.1980,1.4940	<0.01%	±3%,±3%, ±3%/ ±3%, ±3%, ±3%	<0.01%~ 3.8%

* Assumptions: The variations of d_{siod1} and d_{siod2} are identical; so as n_{siod1} and n_{siod2}.

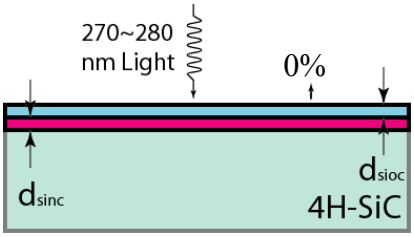
Table E-1. AR coating design for SiC UV detectors centered at 270nm or 280nm.



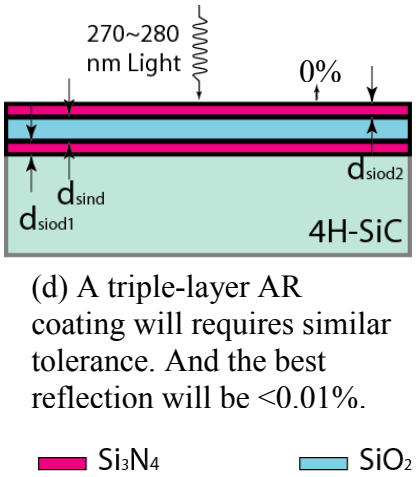
(a) Without AR coating, SiC reflects 25% of UV light in 270~280nm



(b) A single layer of Si_3N_4 AR coating could reduce to 2% and good dielectric layer growth tolerance.



(c) A double-layer of Si_3N_4/SiO_2 AR coating could further reduce to <0.01%. But dielectric layer growth tolerance will be tight.



(d) A triple-layer AR coating will requires similar tolerance. And the best reflection will be <0.01%.

Fig. E-1 Designing of AR coating for SiC detectors. The AR coating could reduce the reflection from ~25% to 2% or <0.01%.

REFERENCES

1. TOPIC: X7 Operations of Exploration Equipment. *Small Business Innovation Research & Technology Transfer 2006 Program Solicitations.* [Online] National Aeronautics and Space Administration .
http://www.sbir.nasa.gov/SBIR/sbirsttr2006/solicitation/SBIR/TOPIC_X7.html.
2. Solar Blind UV (SBI-2) Imager . [Online] Ofil Ltd.
http://www.ofilsystems.com/Products/imagers/index.html.
3. G. A. Shaw, A. M. Siegel, J. Model. Ultraviolet Comm Links for Distributed Sensor Systems. *IEEE Newsletter.* Oct 2005, p. 26.
4. I. P. S. Choi, H. N. J. Fernando, P. D. Townsend, M. Wahl. Applicaiton of a new time-correlated single photon counting instrument in a fiber-based quantum cryptography system. *Proc. of SPIE.* 2006, Vol. 6372.
5. X. Xin, F. Yan, T. W. Koeth, C. Joseph, J. Hu, J. Wu, J. H. Zhao. Demonstration of 4H-SiC visible-blind EUV. *ELECTRONICS LETTERS.* Oct 13, ELECTRONICS LETTERS, Vol. 41, 21.
6. F. Yan, X. Xin, S.Aslam, Y. Zhao, D. Franz, J. H. Zhao, M. Weiner. 4H-SiC UV photo detectors with large area and very high specific detectivity. *IEEE Journal of Quantum Electronics.* Sep 2004, Vol. 40, 9, pp. 1315-1320.
7. N. S. Nightingale. A new silicon avalance photo diode photon counting detector module for astronomy. *Exp. Astron.* 1991, Vol. 1, pp. 407-422.
8. L. Q. Li, L. M. Davis. Single photon avalanche diode for single molecule detection. *Rev. Sci. Instrum.* 1993, Vol. 64, pp. 1524-1529.
9. S. Tada. A novel single-photon counting technique applied to highly sensitive measurement of [Ca2+]i transient in human aortic smooth muscle cells. *Journal of biomechanical Engineering.* Oct 2006, Vol. 128, p. 777.
10. R. Niesner, K-H Gericke. Quantitative determination of the single molecule detection regime in fluorescence fluctuation microscopy by means of photon counting hisogram analysis. *The Journal of Chemical Physics.* 2006, Vol. 124, 134704, p. 1.
11. *Tools for noninvasive optical characterization of CMOS circuits.* F. Stellari, F. Zappa, S. Cova, L. Vendrame. Washington, D. C. : s.n., 1999. Proc. IEDM'99.
12. G. Gudkov, V. Dhulla, A. Borodin, D. Gavrilov, A. Stepukhovich, A. Tsupryk. 32-Channel single photon counting module for ultra sensitive detection of DNA sequences. *Proc. of SPIE.* 2006, Vol. 6372.
13. L. Alaverdian, S. Alaverdian, O. Bilenko, I. Bogdanvo, E. Filippova, D. Gavilov, B. Gorbovitski, M. Gouzman, G. Gudkov, S. Domratchev, V. Gorfinkel. A family of novel DNA sequencing instruments based on single photon detecction. *Electrophoresis.* 2002, Vol. 23, p. 2804.
14. C. Xu, J. M. Roth, W. H. Knox, K. Bergman. Ultra-sensitive autocorrelation of 1.5um light with single photon counting silicon avalanche photodiode. *IEE Electronics Letters.* 2002, Vol. 38.
15. E. D. Palik. *Handbook of Optical Constants of Solids.* s.l. : Orlando Acdemic Press, 1985.
16. Z. Luo, T. Chen, A. C. Ahyi, A. Sutton,B. Haugerud, J. D. Cressler, D. Sheridan,J. R. Williams, P. W. Marshall, R. A. Reed. Proton radiation effects in 4H-SiC diodes and MOS capacitors. *IEEE Transactions on Nuclear Science.* 2004, Vol. 51, 6.

17. A. Ionascut-Nedelcescu, C. Carlone, A. Houdayer, H. J. von Bardeleben, J.-L. Cantin, and S. Raymond. Radiation Hardness of Gallium Nitride. *IEEE Trans. Nucl. Sci.* 2002, Vol. 46, 9, p. 2733.
18. X. Sun, P. L. Jester,S. P. Palm, J. B. Abshire, J. D. Spinhirne, M. A. Krainak. In Orbit performance of Si avalanche photodiode single photon counting modules (SPCM) used in the Geoscience Laser Altimeter System on ICESat. *Proc. of SPIE.* 2006, Vol. 6372, pp. P1-P5.
19. J. C. Campbell, S. Demiguel, F. Ma, A. Beck, X. Guo, S. Wang, X. Zheng, X. Li, J. D. Beck, M. A. Kinch, A. Huntington, L. A. Coldren, L. A. Decobert, N. Tscherptner. Recent Advances in Avalanche Photodiodes. Jul/Aug 2004, p. 777.
20. P. G. NEUDECK, W. Huang, M. Dudley, C. Fazi. Non-micropipe Dislocations in 4H-SiC Devices: Electrical Properties and Device Technology Implication. [Online] http://www.grc.nasa.gov/WWW/SiC/publications/MRS98PaperPGN498.pdf.
21. N. I. Kuznetsov, and A. S. Zubrilov. Deep centers and electroluminescence in 4H-SiC diodes with a p-type base region. 1995, pp. 181-185.
22. *Ultra high-quality silicon carbide single crystals.* D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, K. Takatori. 2004, Nature, V.430.
23. S-S Liua, P-W Lia, W. H. Lanb, Y-C Cheng. The improvement of GaN p-i-n UV sensor by 8-pair AlGaN/GaN superlattices structure. 2006, pp. 33-36.
24. M. L. Lee, J. K. Sheu, Y. K. Su, S.J. Chang, W. C. Lai, G. C. Chi. Reduction of dark current in AlGaN-GaN Schottky-barrier photodetectors with a low-temperature-grown GaN cap layer. *IEEE Electron Devices Letters.* Sep 2004, Vol. 25, 9, pp. 593-595.
25. S. Verghese, K. A. McIntosh, R. J. Molnar, L. J. Mahoney, R. L. Aggarwal, M. W. Geis, K. M. Molvar, E. K. Duerr, I. Melngailis. GaN avalanche photodiodes operating in linear gain mode and Geiger mode. Mar 2001, p. 502.
26. J. B. Limb, D. Yoo, J. H. Ryou, W. Lee, S. C. Shen, R. D. Dupuis, M. L. Reed, C. J. Collins, M. Wraback, D. Hanser, E. Preble, N. M. Williams, K. Evans. GaN Ultraviolet avalanche phtodiodes with otpical gain greater than 1000 grown on GaN Substrates by metal-organic chemical vapor deposition. *Applied Physics Letters.* 2006, Vol. 89, pp. 011112-1.
27. C. Bulutay, C. Sevik. Gain and temporal response of AlGaN solar-blind avalanche photodiodes: An ensemble Monte Carlo analysis. *Applied Physics Letters.* Aug 2003, Vol. 83, 7, p. 1382.
28. A. O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt. Ionization rates and critical fields in 4H silicon carbide. *Applied Physics Letters.* 1997, Vol. 71, 1, pp. 90-92.
29. I. H. Oguzman, E. Bellotti, K. F. Brennan, J. Kolnik, R. Wang, P. P. Rude. Theory of hole-initiated impact ionization in bulk zincblende and wurtzite GaN. *J. App. Phys.* 1997, Vol. 81, pp. 7827-7834.
30. R. J. McIntyre. Multiplication noise in uniform avalanche diode. *IEEE Trans Electron Devices.* 1966, Vols. ED-13, 1, pp. 164–168.
31. B. K. Ng, J. P. R. David, R. C. Tozer, G. J. Rees, F. Yan, C. Qin, J. H. Zhao. Performance of thin 4H-SiC UV avalanche photodiodes. *IEE Proceedings: Optoelectronics.* Apr 2003, Vol. 150, 2, pp. 187-190.
32. *High gain, low noise 4H-SiC UV avalanche photodiodes.* B. K. Ng, J. P. R. David, R. C. Tozer, G. J. Rees, F. Yan, F., C. Qin, J. H. Zhao. s.l. : Proceedings of the Twenty-Ninth International Symposium on Compound Semiconductors, 2003. Institute of Physics Conference Series, v 174, Compound Semiconductors 2002. pp. 355-358.

33. *A high-speed high-responsive PMT-based detector.* Yuri V. Shcherbakov, Gennadij D. Domashenko. PART 1, s.l. : SPIE -International Society for Optical Engineering, Bellingham WA, WA 98227-0010, United States, 2007, Proceedings of SPIE - The International Society for Optical Engineering, Vol. v 6279, p. 62791F.
34. X. Sun, M.l A. Krainak, J. B. Abshire1, J. D. Spinhirne, C. Trottier, M. Davies, H. Dautet, G. R. Allan, A. T. Lukemire, J. C. Vandiver. Space-qualified silicon avalanche photodiode single photon counting modules. *Journal of Modern Optics.* July 2004, Vol. 51, 9-10, pp. 1333-1350.
35. G. S. Suller, R. D. Harkins, A. M. Wallace. Multiple Wavelength time-of-light sensor based on time-correlated single photon counting. *Review of Scientific Instruments.* 2005, Vol. 76. 083112.
36. J. C. Jackson, D. Phelan, A. P. Morrison, R. M. Redfern, A. Mathewson. Toward integrated single-photon-counting microarrays. *Opt. Eng.* 2003, Vol. 42, 1, p. 112.
37. A. Gallivanoni, I. Rech, D. Resnati, M. Ghioni, S. Cova. Monolithic active quenching and picosecond timing circuit suitable for large-area single-photon avalanche diodes. *Optics Express.* June 12, 2006, Vol. 14, 12, p. 5021.
38. *A CMOS single photon avanlanche diode array for 3D-imaging.* C. L. Niclass, A. Rochas, P-A Besse, E. Charbon. 2004. 2004 IEEE International Solid-State Circuits Conference. Section 6/Imaging/6.7.
39. G. Ripamonti, M. Ghioni, S. Vanoli. Photon timing OTDR: a multiphoton backscattered pulse approach. *Electron. Lett.* 1990, Vol. 26, pp. 1569-1572.
40. A. Biber, P. Sitz, H. Jackel. Avalanche photodiode imager sensor in standard BiCMOS technology. *IEEE Trans. Electron Dev.* Nov 2000, Vol. 47, 11, pp. 2241-2243.
41. A. Rochas, G. Ribordy, B. Furrer, P. A. Besse, and R. S. Popovic. First passively-quenched single photon counting avalanche photodiode element integrated in a conventional CMOS process with 32ns dead time. *Applications of Photonic Technology.* 2002, Vol. 5, p. 107.
42. D. Stoppa, M. Scandiuzzo, L. Gonzo. A CMOS 3-D Imager Based on Single Photon Avalanche Diode. *IEEE Trans. on Circuits and Systems.* Jan 2007, Vol. 54, 1, p. 4.
43. G. Williams. Single-photon-counting APDs operate in the near infrared. *Laser Focus World.* July 2006, p. 119.
44. J. Boisvert, G. S. Kinsey, D. McAlister, T. Isshiki, R. Sudharsanan, M. Krainak. Large Area InAlAs/InGaAs single photon counting avalanche photodiodes. *Laser Radar Technology and Applications.* 2004, Vol. IX, p. 126.
45. K. Forsyth, N. Clay. Geiger-mode InGaAsP/InP APDs optimized for single photon counting at 1.06um. *Proc. of SPIE.* 2006, Vol. 6372.
46. H. Pan, H. Dong, H. Zeng. Efficient single-photon counitng at 1.55um by intracavity frequency upconversion in a unidirectional ring laser. *Applied Physics Letters.* 2006, Vol. 89, 19, p. 191108.
47. A. Bergamaschi, F. Arfelli, E. Castelli, et al. High-speed single photon counting read out electronics for a digial detection system for clinical synchrotron radiation mammography. *Nuclear Instruments and Methodes in Physics Research A.* 2004, Vol. 518, pp. 415-417.
48. S. Cova, M. Ghioni, A. Lacaita, C. Samori, and F. Zappa. Avalanche photodiodes and quenching circuits for single photon detection. *Appl. Opt.* 1996, Vol. 35, pp. 1956-1976.
49. Micro Photon Devices. [Online] Micro Photon Devices. http://www.microphotondevices.com/products.asp.

50. F. Yan. *4H-SILICON CARBIDE AVALANCHE PHOTODIODES.* Ph. D. Dissertation. Piscataway : Rutgers, The State Univ. of New Jersey, 2002.
51. Xin, X., et al. Demonstration of the first 4H-SiC UV single photon counting. *IEE Electronic Device Letters.* 2005, Vol. 41, 4, p. 212.
52. A. L. Beck, G. Karve, S. Wang, J. Ming, X. Guo, J. C. Campbell. Geiger Mode Operation of Ultraviolet 4H-SiC. *IEEE PHOTONICS TECHNOLOGY LETTERS.* 2005, Vol. 17, 7, p. 1507.
53. A. L. Becka, X. Guo, H. Liu, C. Ghatak-roya, J. Campbell. Low dark count rate 4H-SiC Geiger mode avalanche photodiodes. *Proc. of SPIE.* 2006, Vol. 6372, 63720O.
54. D. M. Taylor, J. C. Jackson, A. P. Morrison, A. Mathewson, J. G. Rarity. Characterization of novel active area silicon avalanche photodiodes operating in the Geiger mode. *Journal of Modern Optics.* 2004, Vol. 51, 9-11, pp. 1323-1332.
55. X. Guo, A. L. Beck, J. C. Campbell, D. Emerson, J. Sumakeris. Spatial Nonuniformity of 4H-SiC Avalanche Photodiodes at High Gain. *IEEE JOURNAL OF QUANTUM ELECTRONICS.* 2005, Vol. 41, 10, pp. 1213-1216.

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PUBLICATIONS

[1] “High performance 4H-SiC single photon avalanche diode operating at solar blind wavelength”, X. Xin, J. Hu, P. Alexandov, J. H. Zhao, B. L. VanMil, D. K. Gaskill, K.-K. Lew, R. Myers-Ward, C. Eddy, Jr., SPIE Optics East (Presented, to be published), Sep 9-12, 2007, Boston, MA

[2] “4H-SiC Single Photon Avalanche Diode for 280nm UV Applications”, J. Hu, X. Xin, P. Alexandov, J. H. Zhao, B. L. VanMil, D. K. Gaskill, ICSCRM 2007 (accepted), Oct 14-19, 2007, Otsu, Japan

[3] “High Sensitive visible-blind extreme ultraviolet Ni/4H-SiC Schottky photodiodes with large detection area”, J. Hu, X. Xin, J. H. Zhao, Optics Letters, 31 (12), 1591-1593 (2006)

[4] “Demonstration of 4H-SiC Visible-Blind EUV and UV Detector with Large Detection Area”, X. Xin, F. Yan, T. W. Koeth, C. Joseph, J. Hu, J. Wu, J. H. Zhao, IEE Electronic Letters Electronics Letters 41, 1192 (2005)

[5] “Development of Ultra High Sensitivity UV Silicon Carbide Detectors”, F. Yan, X. Xin, P. Alexandrov, C. M. Stahle, B. Guan, J. H. Zhao, Materials Science Forum Vols. 527-529, 1461-1464 (2005)

[6] “Demonstration of High-voltage 4H-SiC Bipolar RF Power Limiter”, M. Su, X. Xin, L. X. Li, J. H. Zhao, Materials Science Forum Vols. 527-529, pp. 1371-1374, (2006)

[7] "Demonstration of 4H-SiC UV single photon counting avalanche photodiode”, X. Xin, F. Yan, X. Sun, P. Alexandrov, C. M. Stahle, J. Hu, M. Matsumura, X. Li, M. Weiner, J. H. Zhao, Source: Electronics Letters, 41(4), 212-214 (2005)

[8] "4H-SiC UV photo detectors with large area and very high specific detectivity", Y. Yan, X. Xin, S. Aslam, Y. Zhao, D. Franz, J. H. Zhao, M. Weiner, Source: IEEE Journal of Quantum Electronics, 40(9), 1315-1320 (2004)

[9] "Demonstration of the first 4H-SiC metal-semiconductor-metal ultraviolet photodetector", Z. Wu, X. Xin, F. Yan, J. H. Zhao, Source: Materials Science Forum, v 457-460, n II, Silicon Carbide and Related Materials, 1491-1494 (2003)

[10] "Quadrupole pairing and downturn of moment of inertia for the superdeformed band ^{194}Hg(1)", X. Xin, (Phys. Dept., Peking Univ., Beijing, China); S. X. Liu, Y. A. Lei, J. Y. Zeng, Source: Physical Review C, 62(6), 067303/1-4 (2000)

[11] "Influence of band interaction on the spin prediction of superdeformed rotational bands", Liu, S.X. (Dept. of Phys., Peking Univ., Beijing, China); X. B. Xin, Y. A. Lei, J. Y. Zeng, Source: Journal of Physics G, 26(1), 79-92 (2000)

[12] "Influence of quadrupole pairing on the variation of $J^{(2)}$ of the superdeformed band Hg^{194}(1)" , X. Xin, Y. A. Lei, S. X. Liu, J. Y. Zeng, 17, 94, Chinese Physics Letters (2000)

[13] "Spin assignment of the first discovered superdeformed band Dy^{152}(1) and some superdeformed bands in neighboring nuclei", Chinese Physics Letters, S. X. Liu, X. Xin, J. Y. Zeng, 1999, 16(9), 632-634, (1999)

[14] "New Evidence of Extraterrestrial Cause For the Cretaceous-Tertriary Extinction – The Abundance of Ruthenium and its Correlation with Iridium", X. Xin, X. Y. Xu, W. X. Ji, Chinese Science Bulletin 39 (10), 842-845 (1994)