DESIGN, FABRICATION AND PROCESS DEVELOPMENTS OF 4H-SILICON CARBIDE TIVJFET

By

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A Dissertation submitted to the Graduate School-New Brunswick

Rutgers, The State University of New Jersey

In partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Graduate Program in Electrical and Computer Engineering

Written under the direction of

Professor Jian H. Zhao

And approved by

New Brunswick, New Jersey

January, 2008

ABSTRACT OF THE DISSETATION

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This Ph.D thesis describes and reviews the state-of-the-start 4H-SiC power junction field-effect transistors (JFET). The purpose of thesis research includes design and fabrication of TIVJFET and investigations on the improvements on existing processing technologies, targeting simpler, reliable process that improves device performance.

Fabrication results are presented. Among the results is a normally-off 10 kV, 106 mΩcm^2 TIVJFET with a record-high value for figure of-merit (FOM) ($V_B^2/R_{SP\text{-}ON}$) of 943 MW/cm^2 among all normally-off SiC FETs.

Processing technologies underwent significant improvements. Simpler and more reliable processes were developed, including Bosch dry etching, Ni self-aligned silicide, thick gate-overlay and oxide trench-fill. All new processes were confirmed in test TIVJFET fabrication and results were presented.

A 430V normally-off TIVJFET of very low $R_{SP\text{-}ON}$ of 1.6mΩcm^2 was achieved using new developed process. This device has a channel resistance is 0.5mΩcm^2, corresponding to only one third of channel resistance reported in [25]. This $R_{SP\text{-}ON}$ is the lowest among all 400V class normally-off SiC FETs reported to date.

A 1568V normally-on TIVJFET was fabricated using new developed processes. $R_{ON\text{-}SP}$ was 2.0mΩcm^2 when current gain was over 12000 (V_{GS}=2.5V). And $R_{ON\text{-}SP}$ was 1.75mΩcm^2 when current gain was over 120 (V_{GS}=3V). This R_{SP_ON} is the lowest among all 1500V class normally-on SiC FETs reported to date. Comparing with the device reported in [16], at the same current gain of 100, this R_{SP_ON} corresponded to a 37% reduction.

ACKNOWLEGEMENT

I would like to express my deep gratitude to Prof. Jian H. Zhao for giving me excellent technical guidance and constant encouragement throughout this dissertation research. I would like to thank Prof. Kuang Sheng, Prof.Wei Jiang of the department and Dr. Maurice Weiner of United Silicon Carbide, Inc., for their critical reading of this dissertation.

I would like to thank Dr. Leonid Fursin for helping me initiate my study on 4H-SiC devices. I would also like to express my appreciation for the invaluable discussions and help from Mr. Petre Alexanderov, Mr. Yongxi Zhang and all my colleagues.

I would like to acknowledge the contribution of Mr. Ming Su for the study of Ni silicide process and Mr. Petre Alexanderov for drawing some of the masks. I would also like to acknowledge Dr. Xueqing Li for the numerical simulations.

I would like to acknowledge the financial support provided by United Silicon Carbide, Inc., which made this project possible.

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Chapter 1. INTRODUCTION

1.1 Why 4H-SiC?

Physical properties of important semiconductor materials were listed in Table 1.1 [2].

Compared with Si, the high critical electric field enables SiC device to achieve excellent figure of-merit (FOM) (V_B^2/Ron-sp), especially for high-power applications. The wide band-gap and high thermal conductivity of 4H-SiC makes it good candidate for high-temperature and radiation-hard applications. High saturation electron velocity makes it an excellent material for RF applications. For power switching applications, compared with currently dominating Si-based devices, 4H-SiC devices can offer high frequency, compact systems with reduced cooling. Compared with other poly-type SiC, 4H-SiC clearly has wider band-gap and/or higher electron mobility. Thus 4H-SiC is particularly attractive for power devices [1,2].

Compared with other wideband gap materials: GaN and diamond, 4H-SiC material technology is by far the most mature. Currently, 4-inch 4H-SiC wafers are available from Cree, Inc with zero micropipe density (ZMP^{TM}) [3].

Table 1.1. Physical Properties of important semiconductors for high-voltage power devices [2]

Material	E_g eV	n_i cm^{-3}	ε_r	μ_n $cm^2/V\cdot s$	E_c MV/cm	v_{sat} $10^7 cm/s$	λ W/cm·K	Direct Indirect
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7×10^{-1}	11.1	350	1.3	1.4	0.8	I
InN	1.86	$\sim10^{3}$	9.6	3000	1.0	2.5	-	D
3C-GaN	3.27	8×10^{-9} *	9.9	1000	1	2.5	1.3 *	D
2H-GaN	3.39	1.9×10^{-10}	9.0	900	3.3	2.5	1.3	D
3C-SiC	2.2	6.9	9.6	900	1.2	2.0	4.5	I
4H-SiC	3.26	8.2×10^{-9}	10	720[a]	2.0	2.0	4.5	I
				650[c]				
6H-SiC	3.0	2.3×10^{-6}	9.7	370[a]	2.4	2.0	4.5	I
				50[c]				
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20	I
BN	6.0	1.5×10^{-31}	7.1	5	10	1.0 *	13	I
AlN	6.1	$\sim10^{-31}$	8.7	1100	11.7	1.8	2.5	D

Note: a – mobility along a-axis, c – mobility along c axis, * - estimate

1.2 4H-Silicon Carbide Power JFET

High Temperature Reliability: Compared with bipolar FETs, unipolar FETs have the advantage of high switching speed. Among SiC unipolar FETs, SiC JFETs are much more reliable than SiC MOSFETs under high temperature and high electric field.

Great progress has been made in the development of power SiC MOSFETs. 4H-SiC MOSFET with an extremely low on-resistance of 1.8 $m\Omega cm^2$ and a blocking voltage of 660 V has been reported and very fast switching speed was achieved, with a rise time of 19 ns and a fall time of 39 ns [4]. However, the reliability of SiC MOSFETs under high temperature and high electric field remains a major concern [5-6].

As for Si-based MOSFET, presently SOI HTMOS devices operating reliably at temperatures in excess of 225°C for time periods greater than five years are available [7], but the ability of Si-based electronics to operate at higher temperatures remains questionable [6].

SiC JFETs, free of gate oxide, are excellent devices to fully explore the benefit of SiC. With dedicated high temperature packages, 4H-SiC JFET has been characterized at 450°C [8] and has demonstrated feasibility of at

least 500h life at 500°C [9]. This enables SiC JFET switching circuits to operate in extremely wide temperature ranges. A DC-DC converter built with 4H-SiC JFETs and 4H-SiC Schottky diodes was tested at ambient temperature upto 400°C [10] and 4H-SiC JFET switching experiment down to cryogenic temperature 30K has been reported [11].

SiC VJET: In terms of device structure, JFETs can be designed to be Lateral (Source, gate and drain terminals are all on the wafer front-side) or Vertical (Source, gate terminals are on the wafer front-side while drain terminal is placed on wafer backside). VJFET structure allows higher cell packing density, thus has lower on-resistance. High voltage class (larger than several kV) devices use almost exclusively vertical structure.

In terms of processing, SiC JFETs can be fabricated with epitaxial regrowth or without. Epitaxial re-growth in the middle of the device fabrication is not desirable since it increases manufacturing costs.

In terms of application, JFETs could be designed either to be normally-on (conduct high drain current at 0V gate bias) or normally-off (can block high drain-to-source voltage at 0V gate bias). Normally-on structure in principal could conduct a higher current density and provide a lower specific on-resistance than normally-off devices, due to the wider

channel opening in normally-on devices. However, normally-off structure is preferred for practical applications because it is fail-safe.

Among normally-on SiC JFET [12-18], one of the best results is a 1710V, 2.77mΩcm^2 4H-SiC TIVJFET [16]. And normally-on 4H-SiC JFET utilizing epitaxial re-growth has been reported capable of blocking 700V, with extremely low on-resistance of 1.0 mΩcm^2, the lowest in this voltage class for all power FETs, including SiC devices and GaN HEMTs [17]. This device requires expensive epitaxial re-growth, but it represented a great improvement in the on-state conduction capability of 4H-SiC VJFETs, bringing the performance closer to the ideal limit of 4H-SiC. With dedicated-gate drive, Normally-on JFET also has very high switching speed. 41MHz switching frequency has been demonstrated using normally-on 4H-SiC JFET [18].

Normally-off SiC JFET can be realized by monolithically integrating a lateral, low- voltage, normally-off JFET with a normally-on, high-voltage VJFET [19-22]. Among them, the best results are 5.3 kV 4H-SiC SEJFET with specific on-resistance (R_{SP_ON}) of 69 mΩcm^2 [21] and a 4,340V, 40 mΩcm^2 Normally-off 4H-SiC VJFET [22].

Hybrid, normally-off VJFETs can also be formed by packaging a low-voltage, normally-off Si MOSFET switch together with a high-voltage,

normally-on switch [13]. But incorporation with Si MOSFET will limit the device reliability at high temperature. And all-SiC-JFET-cascode switch is more desirable. Recently an all-SiC-JFET-cascode switch has been demonstrated with a specific on-resistance of 3.6 mΩcm^2 and over 1000 V blocking capability, which could be operated at temperatures exceeding 150 °C [23]. This SiC cascode circuit shows comparable switching speeds to typical Si power MOSFETs in the same voltage range.

Clearly, it is desirable to realize the normally-off VJFET by a purely vertical structure, because removing the LJFET part will reduce the device resistance. Normally-off trench and implanted VJFET (TIVJFET) structure is simple to fabricate (no epitaxial re-growth is needed) and can achieve a high current density [25]. Scalable design from 1.7kV to 14kV has been reported on this structure [24] and excellent normally-off TIVJFETs were demonstrated ranging from 1.7kV to 10kV classes. Normally-off 4H-SiC TIVJFET was first demonstrated in 2003 [25], with specific-on-resistance (R_{ON-SP}) of 3.6 mΩcm^2 and blocking voltage (V_B) of 1726 V. This corresponds to a figure of-merit (FOM) (V_B^2/Ron-sp) of 830 MW/cm^2, which is 27 times higher than the state-of-the-art Si Cool-MOS power discrete devices [26]. This work presented a great improvement in the on-state conduction capability of 4H-SiC normally-off VJFETs, bringing the

performance closer to the ideal limit of 4H-SiC. At 10kV class, 4H-SiC TIVJFET offers an excellent blocking voltage/specific on-resistance trade-off [27,28]. The reported devices showed blocking voltage (V_B) of 11.1 kV and specific on-resistance (R_{SP_ON}) of 124 mΩcm^2 [27], and V_B of 10 kV and R_{SP_ON} of 106 mΩcm^2, which has a record-high value for figure of-merit (FOM) (V_B^2/Ron-sp) of 943 MW/cm^2 among all normally-off SiC FETs [28].

SiC LJET: Despite its lower cell packing density (thus higher on-resistance), Lateral JFETs have the unique advantage to realize power integrated circuit by monolithic integration. Due to its superior high temperature reliability, SiC-LJFET offers an excellent approach to "smart power integrated circuits". A 50 mΩcm^2, 800V normally-on SiC JFET was reported in 2004 [29]. By increasing cell packing density and utilizing double-gate structure, first high-voltage normally-off lateral JFET on 4H-SiC was demonstrated with a low specific on-resistance of 12.4 mΩcm^2 and 430V blocking voltage [30]. And this same device structure was soon improved to 9.1 mΩcm^2, 1000V [31]. This corresponds to a figure of-merit (FOM) (V_B^2/Ron-sp) FOM of 116 MW/cm^2, which is by far the best among all lateral SiC power devices, including lateral SiC MOSET. Also in this

paper [31], low-voltage logic inverter circuits based on the same lateral JFET process have been monolithically integrated on the same chip. Proper logic-inverter function has also been demonstrated.

1.3 Purpose of Thesis Research

In his PHD Thesis work [32], K. Tone developed a feasible fabrication process and demonstrated excellent TIVJFET with blocking voltages between 1000~2000V.

To fully taking advantage of the superior material properties of 4H-SiC, there was a strong interest to demonstrate JFET with higher blocking voltages, for example, 10kV.

The fabrication process described in K. Tone ‘s Thesis employed some clever tricks and he demonstrated its feasibility by producing excellent devices. Still, some processes were time-consuming and even became impossible when device-packing density was increased.

The best normally-off TIVJFET reported [25] before this thesis work had $R_{ON\text{-}SP}$ of 3.6mΩcm^2. And 50% of this total resistance was contributed by device channel resistance. (The wafer drift-layer consists of 9μm doped to 7×10^{15} cm^{-3}, corresponding to 1.0 mΩcm^2. Wafer substrate has also

$0.8m\Omega cm^2$. And that makes the channel resistance to be $1.8m\Omega cm^2$.) To push for better device performance, channel resistance has to be reduced.

Therefore, the purposes of this thesis research are:

(1) To fabricate 4H-SiC normally-off TIVJFETs with blocking voltages of 10kV and with low specific on-resistance.

(2) To develop simpler, more robust fabrication processes and to demonstrate new processes in actual device fabrication.

(3) To develop new fabrication processes targeting TIVJFETs with reduced on resistance.

Chapter 2. Review of TIVJFET Design and Fabrication

Most of the material covered in this chapter was described in detail elsewhere [32]. For the benefit of readers who are unfamiliar with K.Tone's work and for the purpose of comparison: the basic TIVJFET structure design will be briefly reviewed first in this chapter. Then the basic fabrication process will also be reviewed and the steps where improvements are desired will be pointed out.

2.1 Design and Fbrication of TIVJFET

Unit cell design and wafer structure

The cross sectional view of a typical TIVJFET [25, 32] is shown in Fig 2.1. It consists of three N type epi-layers. The channel layer doping concentration, channel width (W_{VC} in Fig 2.1), and drift layer doping concentration and thickness needs to be optimized according to required blocking voltages, using Computer simulations [24]. Unit cell pitch should be chosen in accordance with channel width and process capability, so as to maximize cell-packing density.

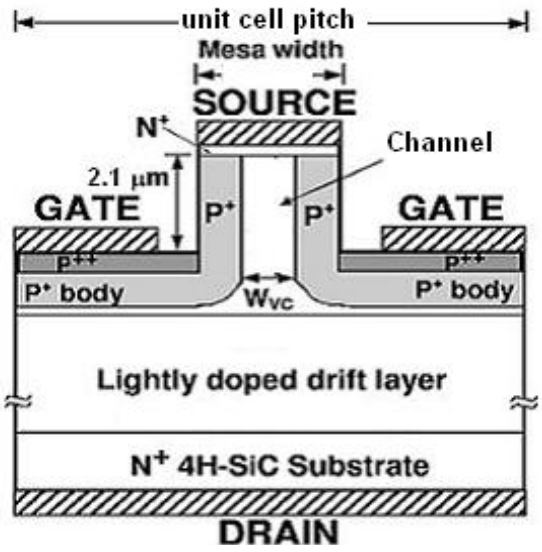


Fig. 2.1: A typical TIVJFET unit cell cross section and wafer structure.

Basic fabrication process

TIVJFET structure has several advantages. Being a JFET it is free of Gate Oxide reliability problem. It has a purely vertical structure resulting in lower R_{SP_ON} . Rounded gate body P-N junction can reduce electric field crowding, resulting in higher blocking voltage. And by taking advantages of vertical mesa structure, none of the masks needs critical alignment [25, 32].

TIVJFET fabrication process has been described in detail in literatures [25, 32]. The fabrication sequences are reviewed briefly in the following for comparison purpose. The following description explains the basic fabrication process.

Gate Trench etching. With AlTi metal layer serving as hard mask, gate trenches are etched by plasma dry etching.

Al implantation. Using Mo as implantation mask, Al implantation was done by self-alignment techniques. The actual implantation takes place in three stages. The purpose of the implantation is to create (1) the p-body under the trench bottom for blocking, (2) the p-gates on the sidewalls for the vertical-JFET gate and (3) the p+ region at the trench bottom for the gate contact.

Post implantation annealing. After implantation, the wafer should be annealed at 1550°C for 30min in the ambient of ultra-high purity argon, to restore residual lattice damage and activate the implants. During annealing the wafer should be loaded in carbon crucible face-to-face with blanket SiC substrate. Silicon Carbide powders are also used in the crucible to suppress silicon evaporation from wafer surface.

MJTE formation. MJTE structure is formed by ICP etching [25, 32] to optimize device reverse-blocking capability.

Surface Passivation. After complete cleaning, sacrificial oxidation is to be done for 0.5 hour at 1100°C in wet oxygen to form a thin layer of oxide and subsequently removed by BHF. The purpose of step is to remove defects on the wafer surface after previous implantations and ICP etching processes. After this, the passivation oxide will be grown for 2 hour at 1100°C in wet oxygen.

Ohmic contats. Source ohmic contact can be done by self-aligned process through photoresist planarization and etch-back [25, 32]. Gate ohmic contact can be done by lithography and liftoff. A single ohmic contact annealing at 1,050°C for 10 min will be done to form ohmic contacts.

Polyimide planarization and metal overlay. Finally, polyimide planarization layer will be coated and etched back and thick overlay metal for source and gate will be deposited.

2.2 Fabrication Challenges for TIVJFET

Gate Trench etching . Channel width for 4H-SiC TIVJFET is usually in submicron range, thus very sensitive to process non-uniformity. To improve device yield, not only good line-width uniformity is necessary, smooth mesa sidewall and vertical mesa profile is also very desirable. Plasma-etching conditions should be optimized to provide near vertical mesa sidewall.

Ohmic contacts. In established process sequences, Gate ohmic contact was done by lithography and liftoff. Lithography became much more expensive with increased packing density and smaller line-width. New processes should be studied and hopefully simpler and more reliable process will be found.

Gate overlay. In established process sequences, gate was connected together by thin ohmic contact layer only. This process resulted in large effective gate resistance. This will increase device RC time constant,

reducing switching speed. Additional process to add thicker gate overlay is highly desirable.

Polyimide planarization. Conventional TIVJFET process used polyimide planarization layer to fill the trenches. Polyimide layer was then etched back in oxygen plasma and thick overlay metal for source and gate was deposited. Polyimide planarization is a fast, easily controllable process. But being an organic material, its ability to withstand high temperature (>250°C) is questionable. Thus trench-fill using PECVD oxide layer should be studied.

Chaptor 3. High performance TIVJFETs and process improvements

3.1 Design and fabrication of normally-off 10kV TIVJFET

To fully taking advantage of the superior material properties of 4H-SiC, there was a strong interest to demonstrate TIJFET with very high blocking voltages. This section gives the details of a work that has been reported elsewhere [28].

1. Unit Cell design, wafer structure and device layout

Cross sectional view of the second TI-VJFET device unit cell structure is shown in Fig 3.1 (a). And the wafer structure was shown in Fig 3.1 (b). The device uses a drift layer of 100μm with doping of $6\times10^{14}cm^{-3}$, enough to block 10kV. The channel layer is 4μm doped to $5\times10^{15}cm^{-3}$ and is covered by an n^+ ohmic contact cap layer. The vertical channel width (W_{VC}) is 0.7μm. The device mask layout is shown in Fig 3.1 (c).

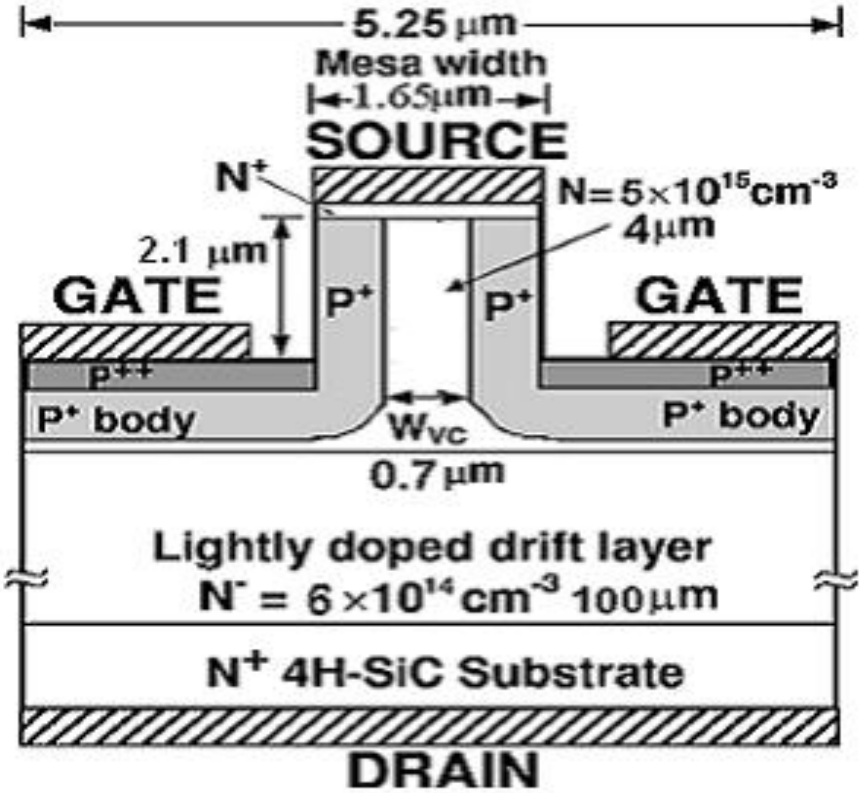


Fig 3.1(a). Cross-sectional view of a unit cell of the 10kV 4H-SiC TI-VJFET.

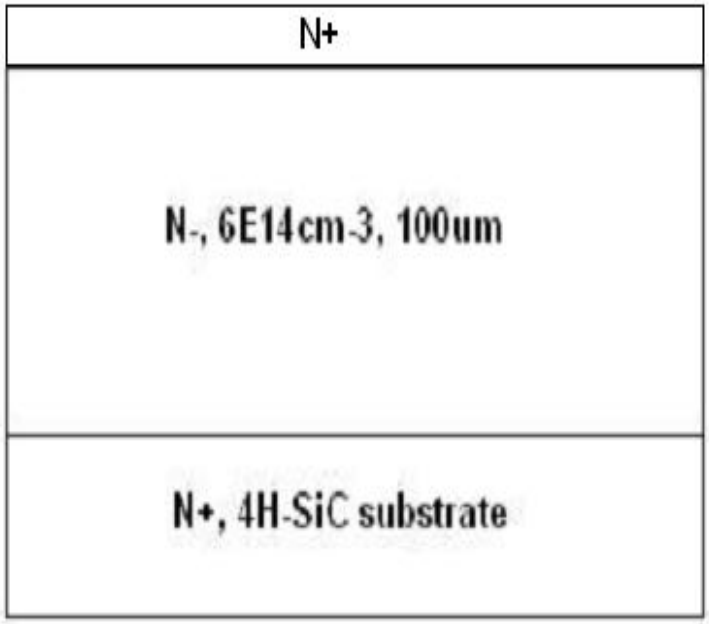


Fig 3.1(b): Wafer epi-layer structure of the 10kV 4H-SiC TI-VJFET. Wafer resistance is about 100~110 mΩcm^2.

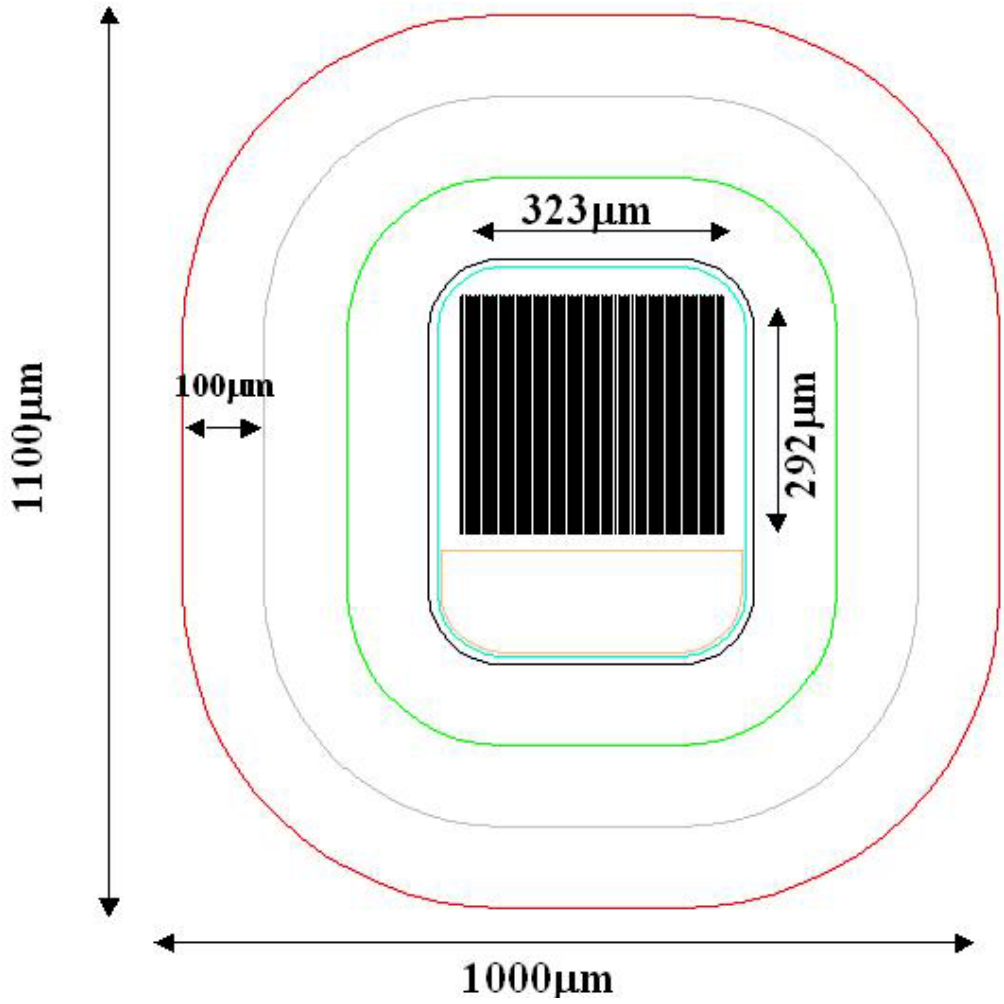
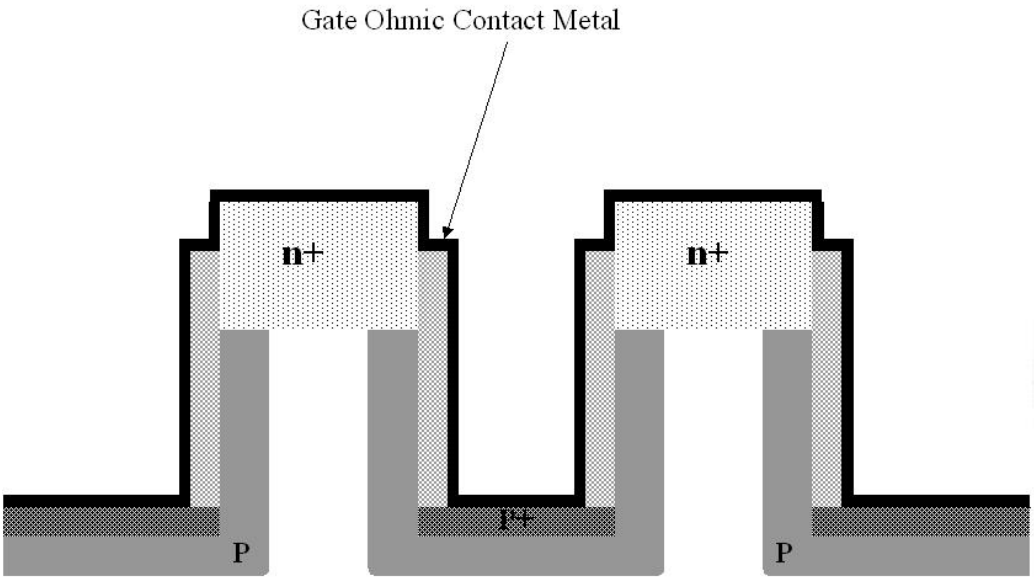


Fig 3.1(c): Mask Layout of the 10kV 4H-SiC TI-VJFET.

2. Process Improvements

Self-aligned Gate contact formation by PR planarization. In the process sequence of [25,32], gate ohmic contact formation was formed by lithography and liftoff. But lithography became much more difficult with increased packing density and smaller line-width, requiring very expansive equipments. To overcome this problem, an alternative process was used (Fig 3.2). After wafer surface passivation, passivation layer on source and gate were simultaneously etched by plasma. Then gate ohmic contact was formed by self-aligned process using PR planarizaion trick.

Gate Metal Deposition



PR Planarization and Etchback followed by Gate Metal Wet Etching

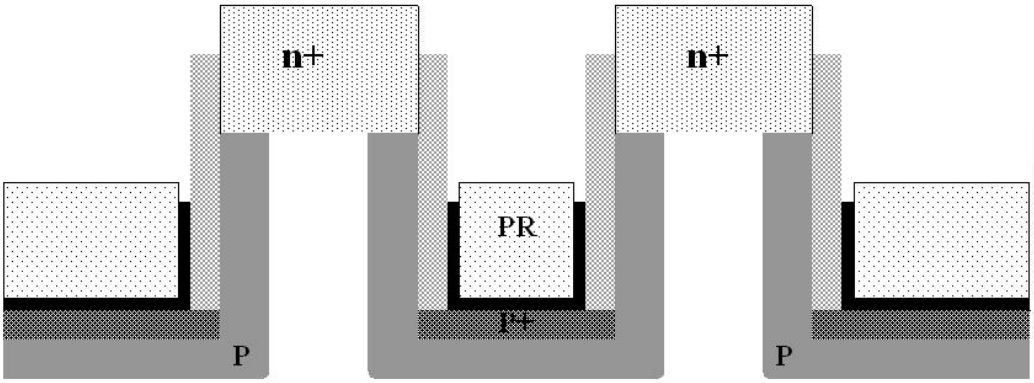


Fig 3.2: Self-aligned gate contact formation.

3. Critical Fabrication Conditions

Sidewall Al implantation Condition

Implantation energy and dose has to be controlled accurately to get accurate sub-micron channel width (Fig.3.3). Note that due to channeling effect, the Al implantation resulted in a tail of about 0.1μm per decade [32].

MJTE optimization and formation.

MJTE structure was optimized on a separate test sample. MJTE structure has three stages, each stage 100μm wide. The depths of outer two JTE stages were 400Å each. The depth of the innermost step has been optimized to get maximum breakdown voltage (Fig.3.4). Optimum blocking voltage/reverse leakage corresponded to about 5400Å etching depth for innermost JTE step. After optimum MJTE structure had been confirmed, it was reproduced on a wafer with TIVJFET devices. Considering thermal oxidation consumption, 5100Å was used as optimum JTE-1 depth.

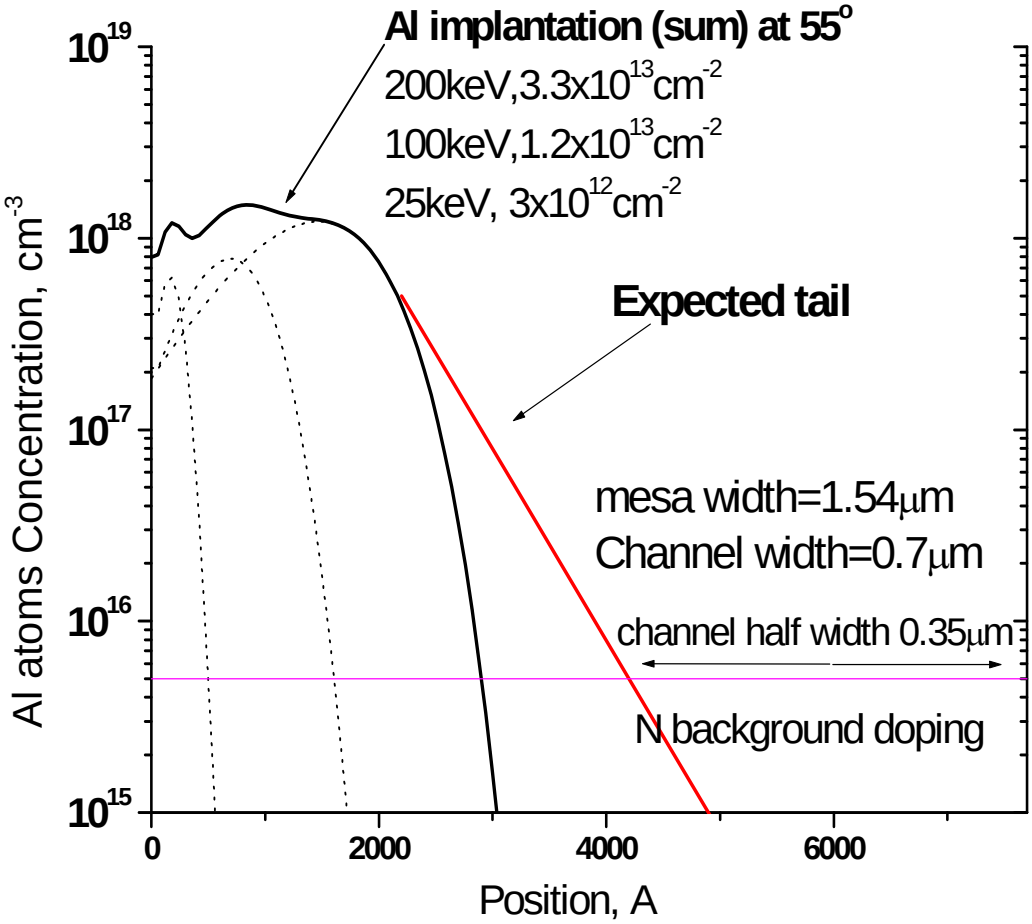


Fig 3.3: Sidewall Al implantation profile.

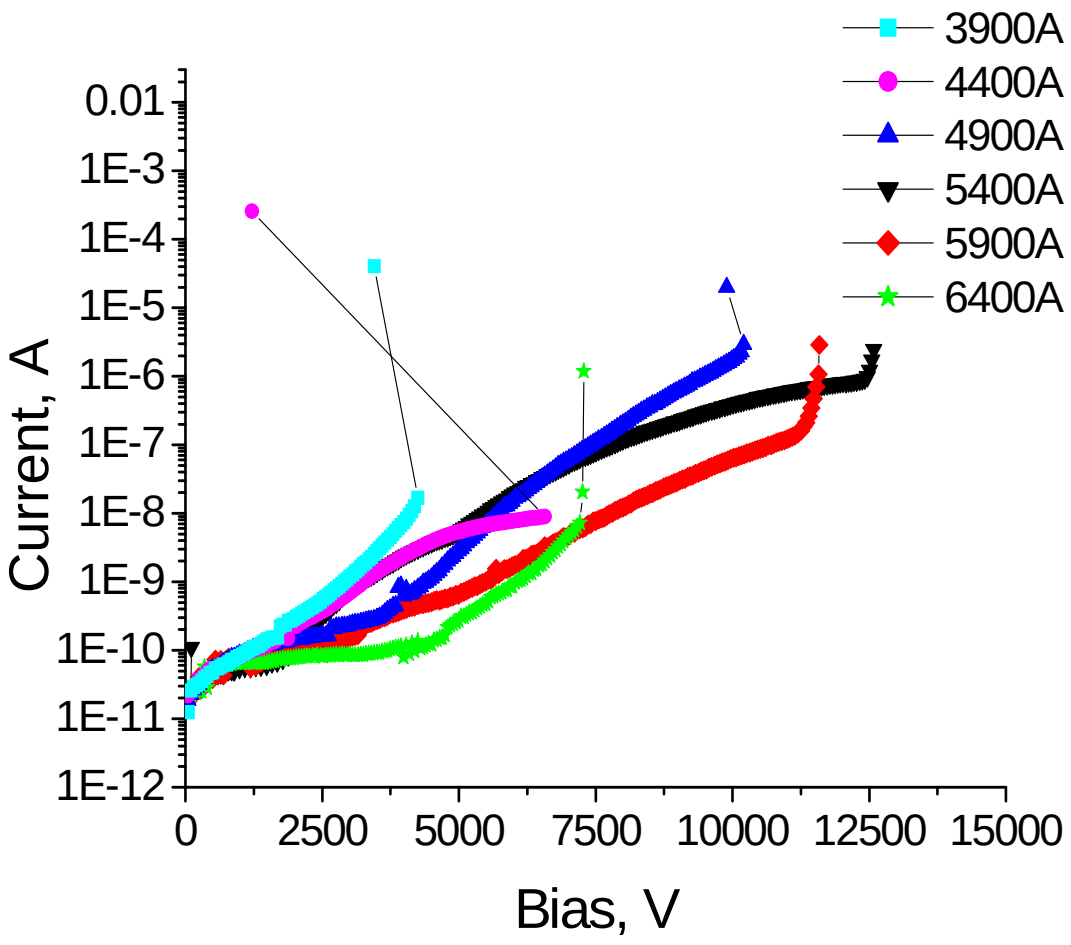


Fig 3.4: JTE-1 depth optimization.

4. Device Characterization

Fig 3.5 shows a finished device. Fig 3.6 shows I-V curves of the fabricated TI-VJFET. The blocking voltage V_B has been measured in excess of 10kV at V_G=0V. Forward J_D reaches 50A/cm^2 at V_D=5.2V and V_G=3V and 22.2A/cm^2 at V_D=2V and V_G=3V, respectively. The specific on-resistance (R_{SP_ON}) is 87mΩcm^2 for J_D=23A/cm^2 at V_D=2V and V_G=3V. This low specific on-resistance includes the effect of current spreading because the drift layer is very thick. Computer simulation including current spreading in JTE region shows a specific on resistance of 106 mΩcm^2, which corresponds to a the lowest R_{SP_ON} reported up to date for a unipolar switch with ≥10kV blocking voltage and a record high value of 943MW/cm^2 for the figure of merit V_B^2/R_{SP_ON} for normally-off SiC FETs. The gate currents corresponding to each of the gate bias voltages are also shown in Fig 3.6. It is seen that when gate bias is 3V, the corresponding gate current is 0.5mA. When the gate bias is reduced to 2.5V the gate current is decreased to 24μA. Hence, the gate current gains are 150 and 1667 for gate biases of 3V and 2.5V, respectively.

Fig 3.5: Finished 10kV TIVJFET,
device active area is $9.3\times10^{-4}cm^2$

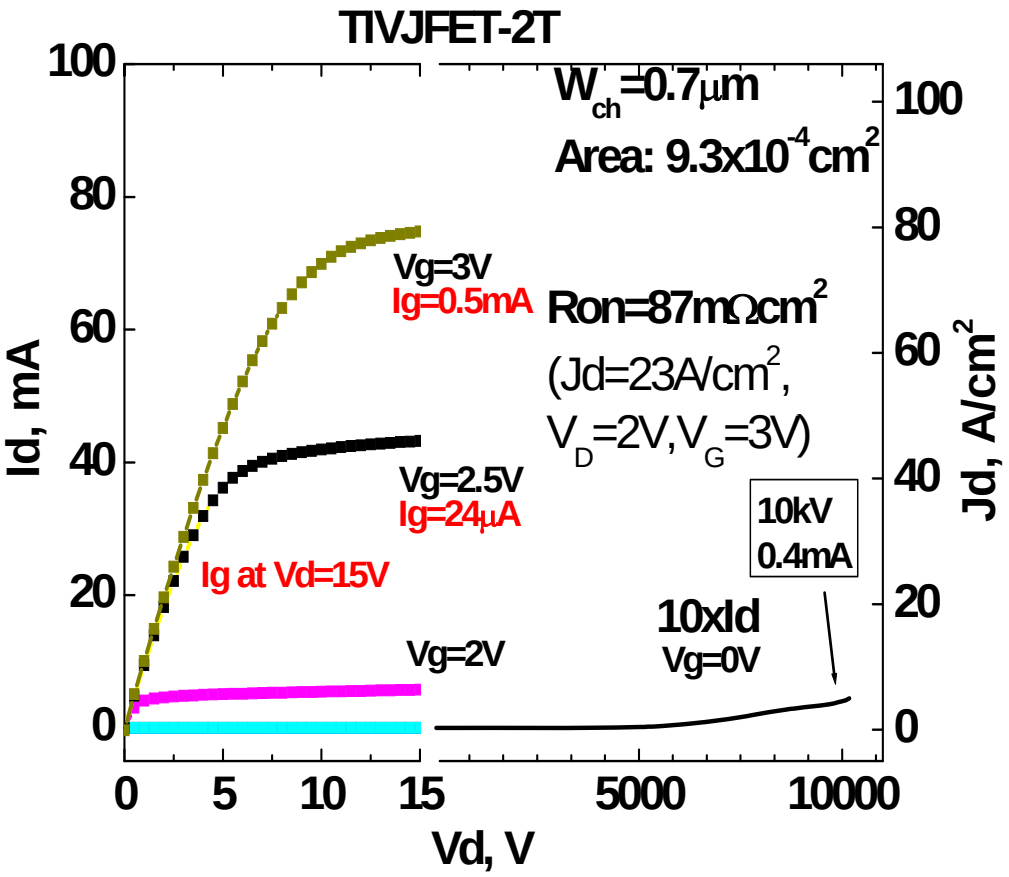


Fig 3.6: Measured I-V curves of a fabricated 10 kV TI-VJFET.

3.2 Process improvements and high performance TIVJFET fabricated by new processes

As mentioned in previous sections, problems with fabrication process of SiC TIVJFET were exposed and needed to be addressed. Processes that need to be improved include: SiC dry etching method, self-aligned ohmic contact formation, adding thick gate overlay metal, and oxide trench-fill.

3.2.1 Bosch process:

A nearly vertical mesa sidewall is desirable because it improves the channel width uniformity in the vertical direction.

Established 4H-SiC dry etching process uses CF4/O2 mixture in ICP and the plasma will chemically and physically etch 4H-SiC [32-33]. A typical SEM picture of etched mesa is shown in Fig 3.7. This mesa sidewall is not very vertical.

Bosch process is used in Si deep trench dry etching [34] and maybe helpful for improving SiC etching process. Bosch dry etching recipe uses alternative polymer deposition and anisotropic dry etching to achieve more vertical etching profile. A typical etched mesa profile measured by AFM is shown in Fig 3.8 (a), (b). The sidewall profile is nearly vertical.

Bosch process also reduced side-etching, making narrower trench width possible. This will increase device-packing density and may help reduce device on resistance.

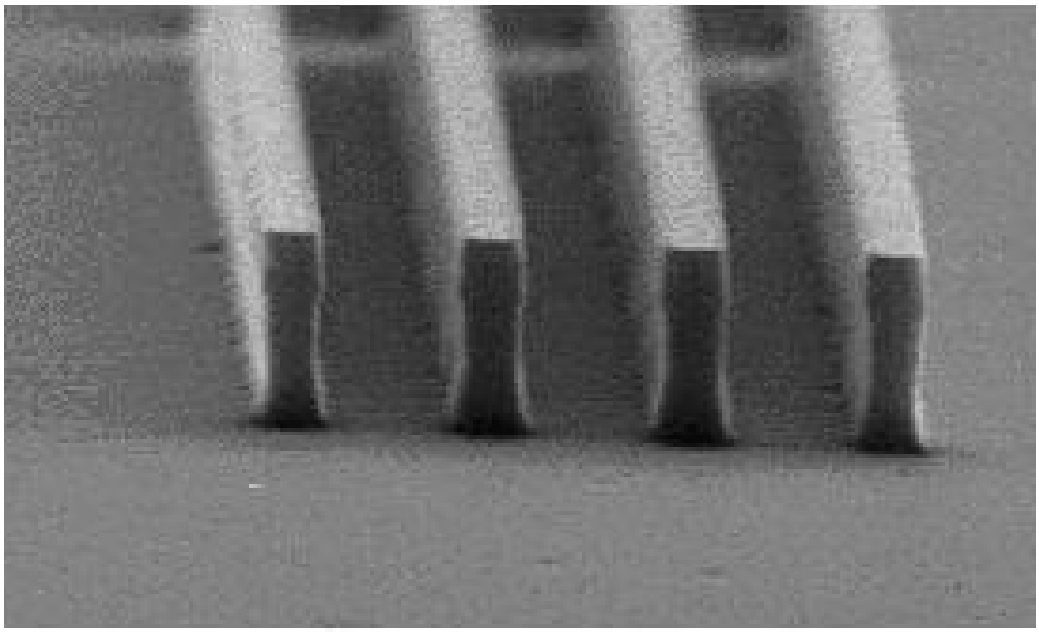


Fig 3.7: A typical SEM picture 4H-SiC mesa structure etched by recipe in [32]. The pitch of the structure is 3.7μm. The mesa width is about 1.0μm and the narrowest part is in the channel part, about 0.8μm. The mesa height is about 4μm.

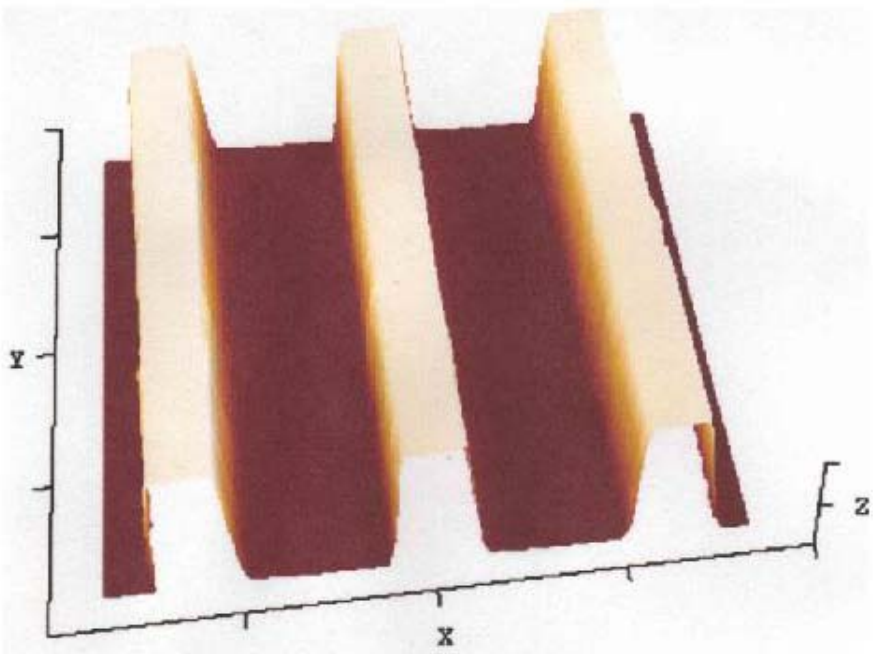


Fig 3.8(a): A typical AFM 3-dimensional surface scan of 4H-SiC trench structure etched by Bosch process. The pitch of the structure is 3.7μm. The mesa width is about 1.2μm at 50% height. The mesa height is about 3.7μm.

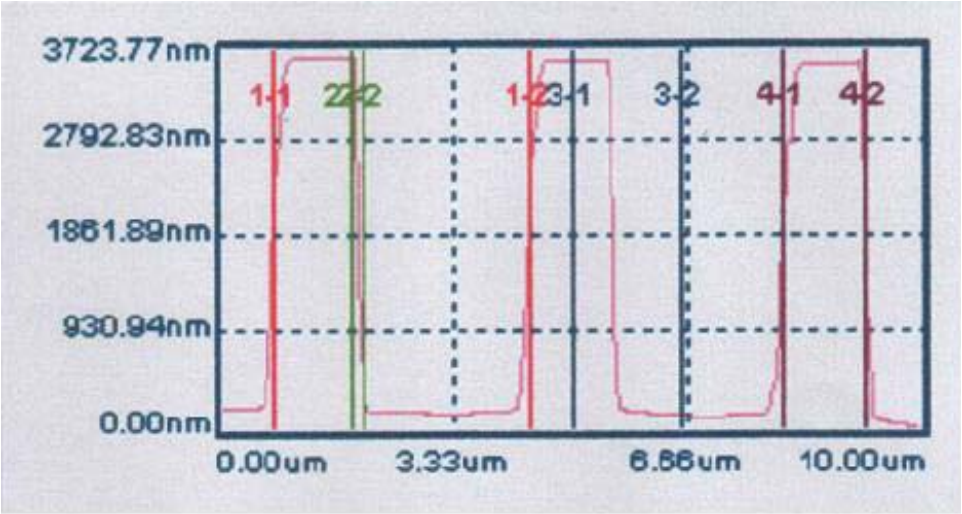


Fig 3.8(b): Vertical profile of the trench structure measured by AFM. Sidewall angle was determined to be 86.96°.

3.2.2 Ni Contact and SiN recess process:

SiC group in Rutgers university also developed a self-aligned Ni contact process. However, SiN passivation layer may react with Ni, forming silicide residues on SiN layer.

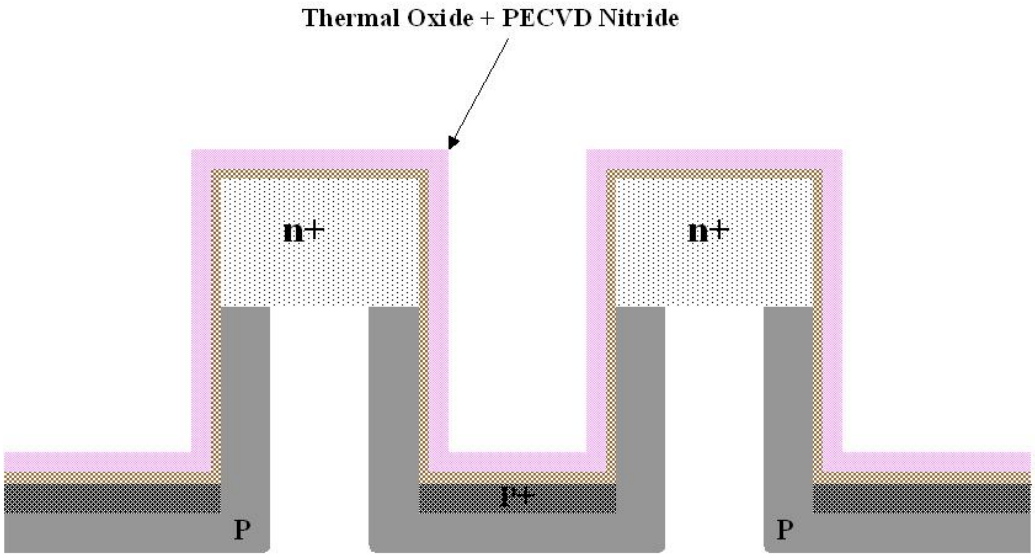
SiN is needed because MJTE is chosen to be the edge termination of power devices, which has the advantage of reaching high blocking voltages. The disadvantage of MJTE is that it relies on delicate electric-charge balance. And if ions diffuse into thermal oxide layer, ion charges can disrupt the charge balance of edge termination structure, resulting in device blocking failure. PECVD SiN is denser than PECVD SiO2, and almost impenetrable to mobile ions. Thus SiN became an indispensable passivation layer over thermal oxide.

To prevent Ni/SiN reaction, SiN needs to be removed from mesa region, so that mesa sidewall is SiN-free. But at the same time thermal oxide on mesa sidewall needs to be left intact because thermal SiO2 is very important for mesa sidewall passivation (where the gate-source junction is located) and also for self-aligned Ni silicide process.

To achieve these goals, a recessed SiN process was implemented (Fig 3.9), taking advantage of a dry etching recipe with large SiO2/SiN selection radio. ICP plasma etcher can separately control plasma power and substrate bias voltage. At certain fixed plasma power level (e.g. 300W), CF_4 plasma will etch SiN layer rapidly at even 0V substrate bias. But SiO2 layer will not be etched at this power level unless biasing voltage was raised to a certain level (e.g. 200V). Thus etching at 0V bias voltage allows us to selectively etch SiN only, leaving Thermal SiO2 intact.

Note the overlap of SiO_2 above SiN layer (or SiN recess) is very important. Without this overlap, Ni will react with SiN layer, damaging passivation layer in a large area (Fig 3.10).

(a) Surface Passivation



(b) Isotropioc SiN dry etching

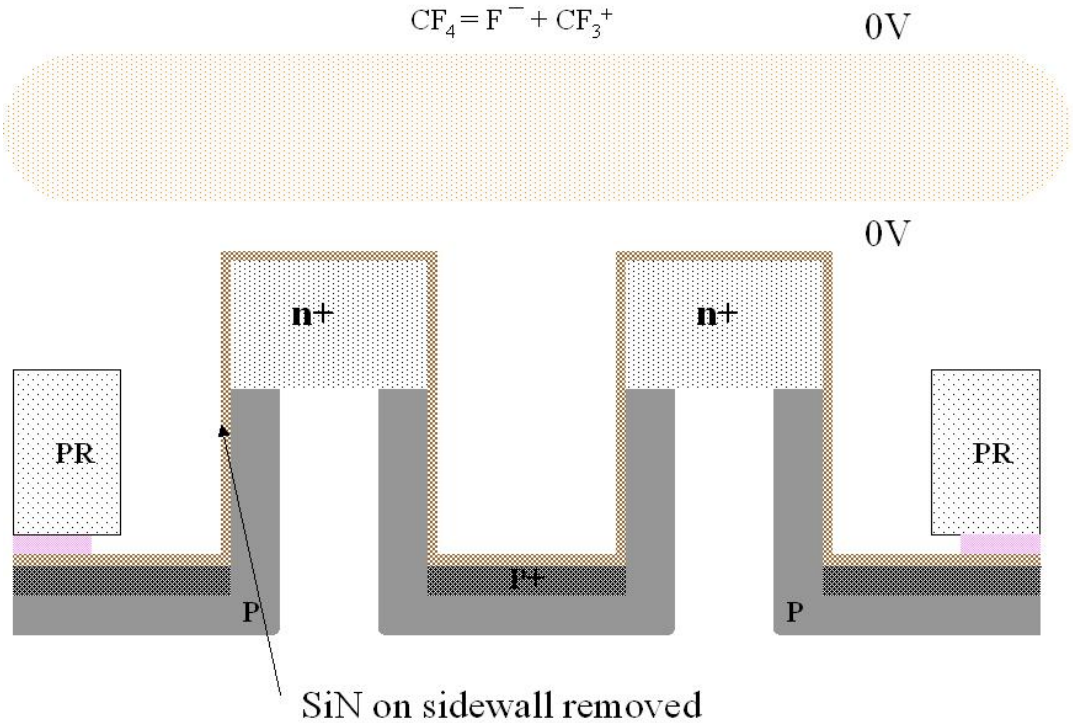
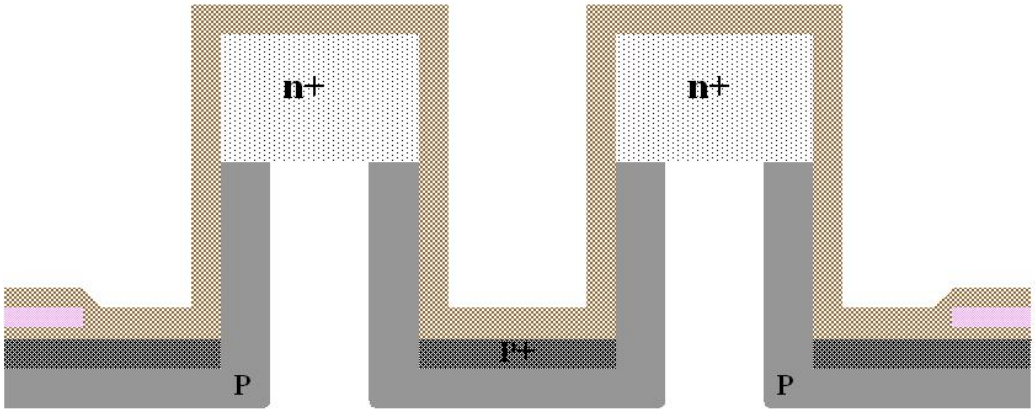


Fig 3.9: Ni contact process with recessed SiN.

(c) Add PECVD SiO_2



(d) Anisotropic SiO_2 dry etching: oxide overlaps nitride

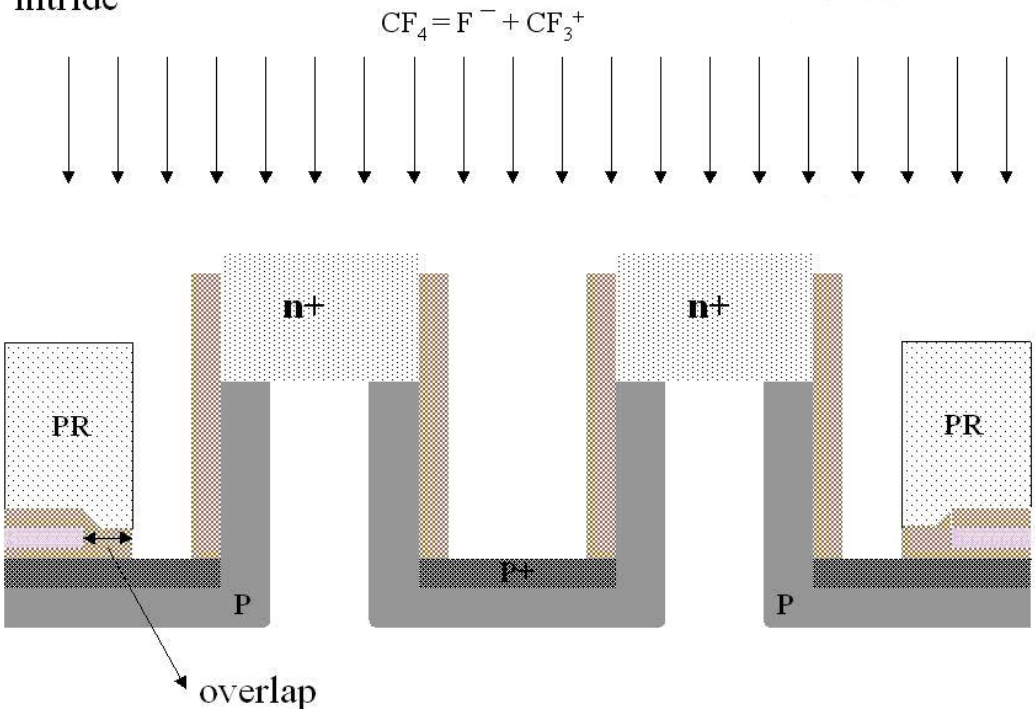


Fig 3.9(cont.): Ni contact process with recessed SiN.

(e) Forming silicide

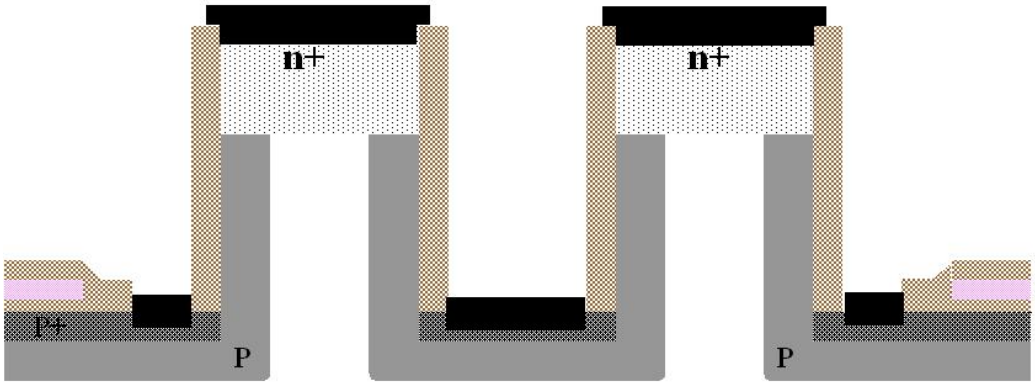
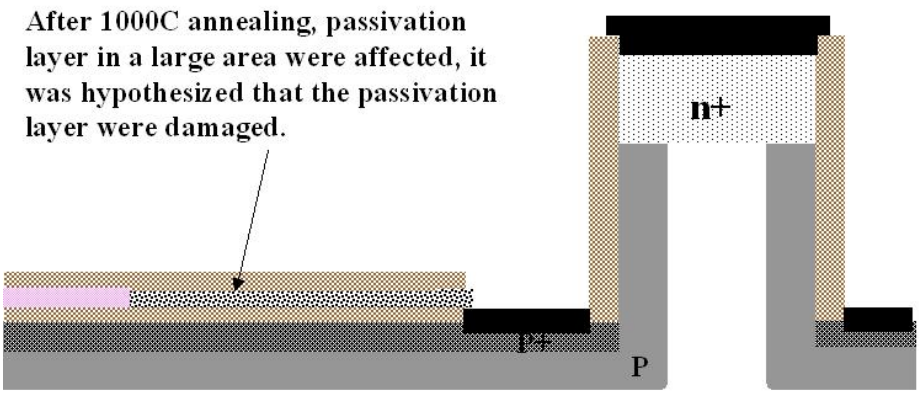


Fig 3.9(cont.): Ni contact process with recessed SiN.



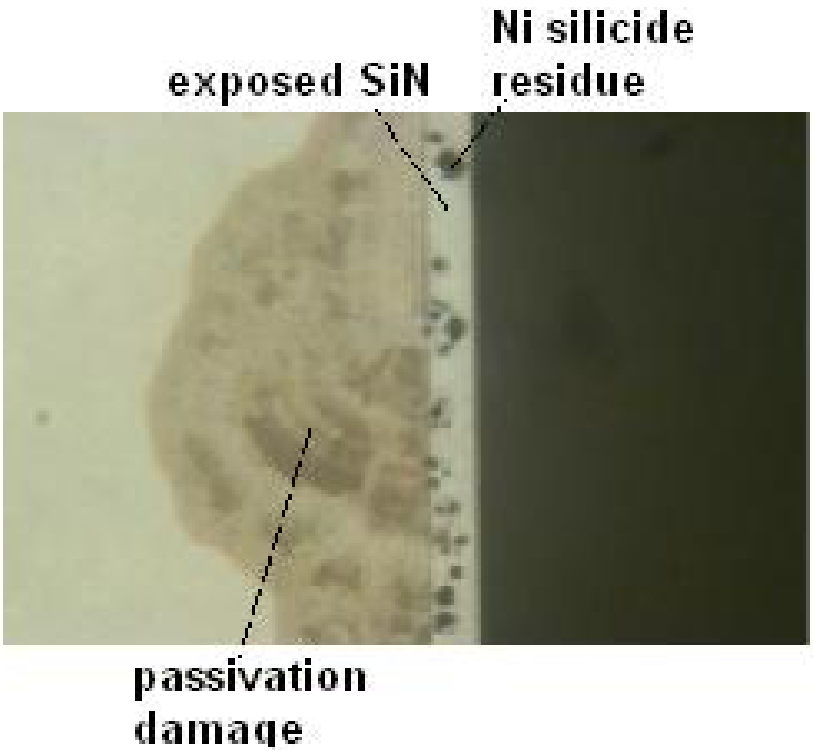


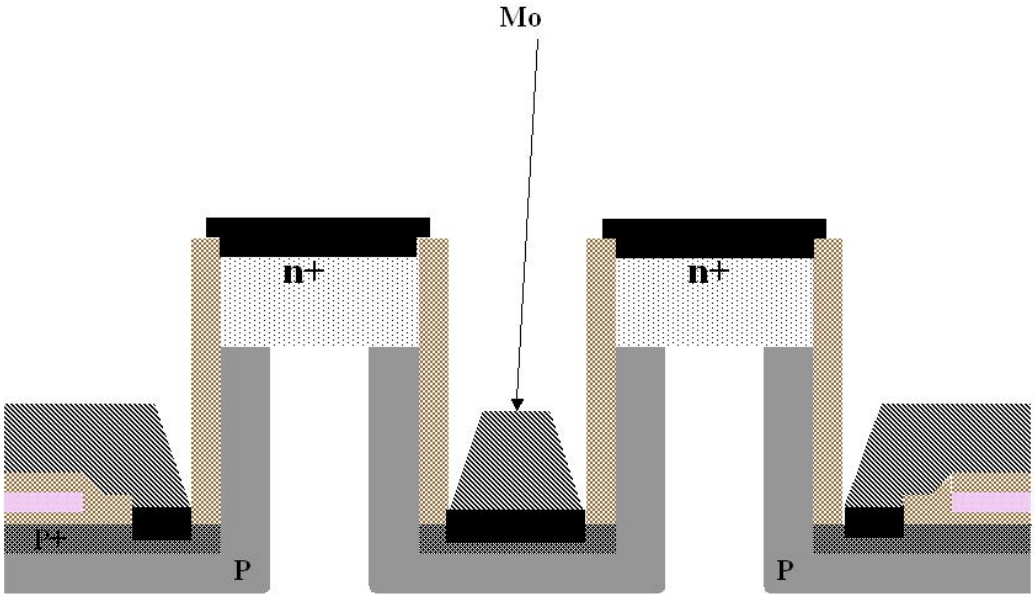
Fig 3.10: Passivation layer affected in silicide process without recessing SiN.

3.2.3 Thick gate overlay process:

To increase device-switching speed, it is necessary to reduce resistance-capacitance (RC) constant. While capacitance is pre-determined by junction area and doping, gate effective resistance can be reduced by adding thick gate overlay. Lower gate resistance will also help to uniformly bias gate-source junction across the whole device area, reducing device on-resistance.

Al would be a nice choice due to its low resistance and good adhesion and low stress. But hillocks are known to form in Al at temperatures above 250C. This causes difficulty for subsequent PECVD dielectric deposition.

Initially, thick Cu layer was experimented because Cu offers low resistivity and good thermal stability. However, due to lack of a good wet etchant, Cu wet etching process has a very small process window, and the etching rate is also very sensitive to temperature. For a more robust process, another metal composition was tried. Mo gate overlay was experimented (Fig 3.11). Mo wet etching process window is larger and not very sensitive to temperature, thus easier to control. Mo also has good thermal stability and therefore it is selected as gate overlay metal.



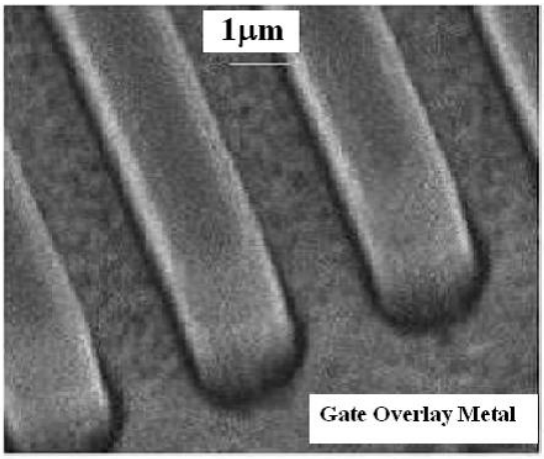


Fig 3.11: Mo gate-overlay.

3.2.4 1.6mΩcm^2, 430V normally-off TIVJFET

To evaluate new processes, a normally-off TIVJFET structure targeting low on-resistance was fabricated. The wafer structure and schematic unit cell cross-section is shown in Fig 3.12. The device used an n-type epi-layer of 4.6μm with doping of 1.2×10^{16}cm^{-3}, part of which served as the channel layer, the remaining 2μm n-type epi-layer serving as the drift layer. On top of this layer was an n$^+$ ohmic contact cap layer.

The mask layout is shown in Fig 3.13. The device active area is 9.0×10^{-4}cm^2. The period of one unit cell is 3.8 μm. Comparing with the unit cell width of 5.5 μm [25], this corresponds to a 50% increase in device packing density.

New processes described in section 3.2 were used on this device: including Bosch trench etching process, Ni contact process with SiN recess and thick gate overlay process.

Fabrication started with gate trench etching by Bosch process. The resulting mesa and trench structure is shown in Fig 3.14. The mesa lower part has a width of 1.53μm. Then tilted Al implantation was done, to form a highly vertical channel with a channel width of 0.72μm (Fig 3.15).

The sample was then annealed at 1,550°C for 30 min to activate implanted Al. Surface passivation was done by thermal oxidation at 1,100°C

for 2 hours in wet O_2 followed by a 200-nm PECVD silicon nitride. Source and gate ohmic contacts were done by Ni contact with SiN recess. Then source, gate and drain ohmic contacts were annealed at 1,000°C for 5 min. To reduce gate resistance, thick gate-overlay metal was deposited and patterned using Mo gate-overlay process. Finally, polyimide planarization layer was coated and etched back to fill the trenches. Contact windows were opened and thick source overlay metal was deposited.

The fabricated devices were characterized by using a Tektronix 371-A High Power Curve Tracer and a probing station. The forward I-V was measured using both voltage drive and current drive mode. Fig 3.16 shows I-V curves of the fabricated TI-VJFET. The blocking voltage V_B has been measured to 430V at V_G=0V, confirming normally-off operation. Note that the leakage current has been multiplied by a factor of 1000 to show the detailed dependence. Drain current is 0.17A at V_{GS} of 3V and V_{DS} of 0.3V, corresponding to an on resistance of 1.76Ω. Considering that device active area is $9.0\times10^{-4}cm^2$, device specific on resistance (R_{SP_ON}) is about $1.6m\Omega cm^2$, the lowest among all 400V class normally-off SiC FETs reported to date. It is seen that current gain (I_D/I_G) is over 100 and 4000 at V_{GS} of 3V and 2.5V respectively.

The total R_{SP_ON} has two major contributors: wafer intrinsic resistance and device channel resistance. Wafer substrate has about 0.8mΩcm^2 (400μm thick, 0.02Ωcm) and wafer drift-layer (2μm doped to 1.2×10^{16} cm^{-3}) has about 0.13mΩcm^2, so the wafer intrinsic resistance is 0.97mΩcm^2. Thus channel resistance is estimated to be 0.67mΩcm^2.

It is interesting to compare with the TIVJFET reported in [25], which has R_{SP_ON} (measured at V_{GS}=5V) of 3.6mΩcm^2. The wafer drift-layer consists of 9μm doped to 7×10^{15} cm^{-3}, corresponding to 1.0 mΩcm^2.
Wafer substrate has resistance of 0.8mΩcm^2. And that makes the channel resistance to be 1.8mΩcm^2.

So the channel resistance of this device is reduced to about 37% of that in [25]. The reduction may be attributed to higher channel layer doping, higher device packing density and the use of new processes, most likely thick gate overlay helped (Fig 3.17~ 3.18). Note that without Bosch process and silicide process, it is very difficult to increase device-packing density, thus the new processes are essential in achieving this low channel resistance.

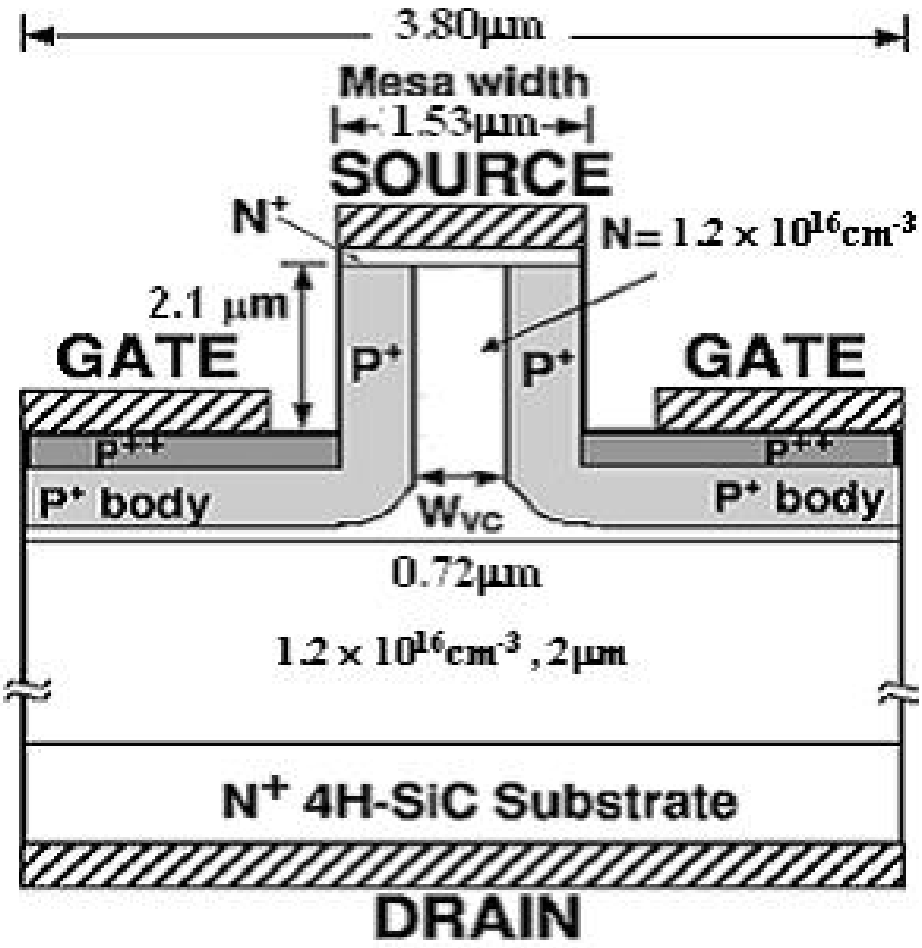


Fig 3.12(a): Cross-section of 430V TIVJFET.

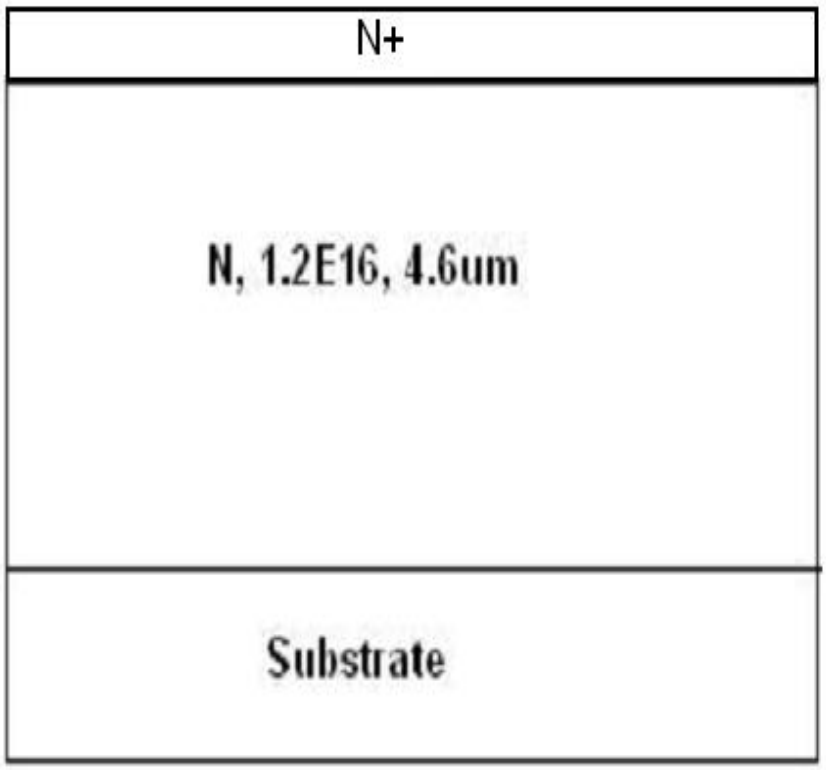


Fig 3.12(b): wafer structure of 430V TIVJFET. Wafer resistance is about 1.1 mΩcm^2.

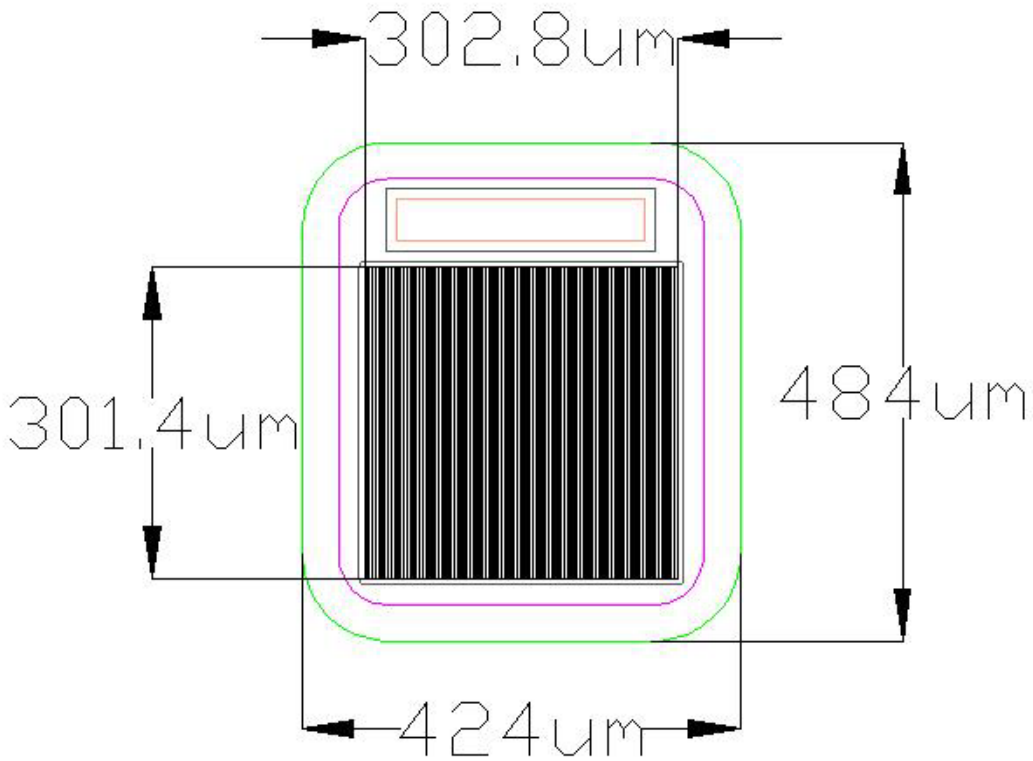


Fig. 3.13(a): Mask layout of 430V TIVJFET. The active area of the device is 9×10^{-4}cm^2.

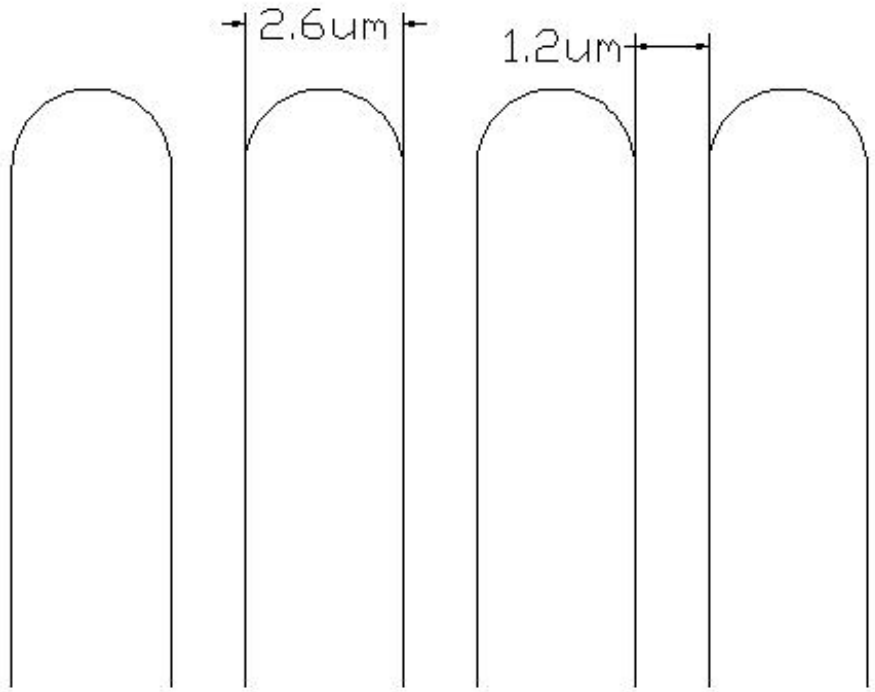


Fig 3.13(b): Mask detail: mesa width is 2.6 μm
and trench width is 1.2 μm. Period is 3.8 μm.

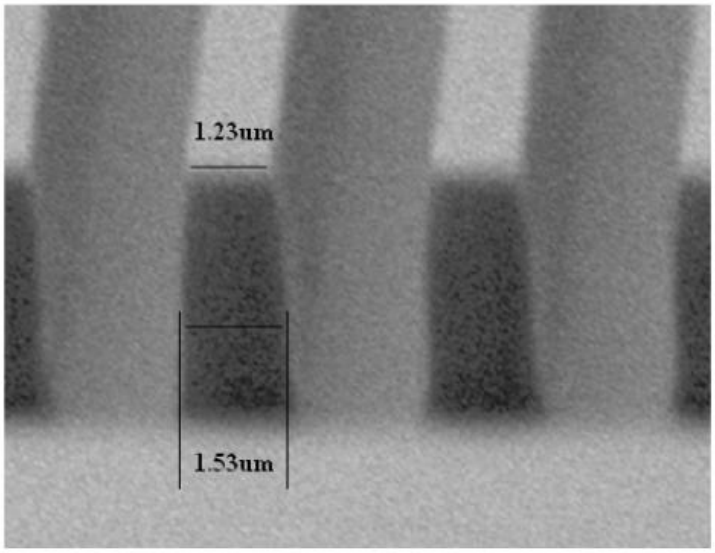


Fig 3.14: Etched mesa-trench structure.

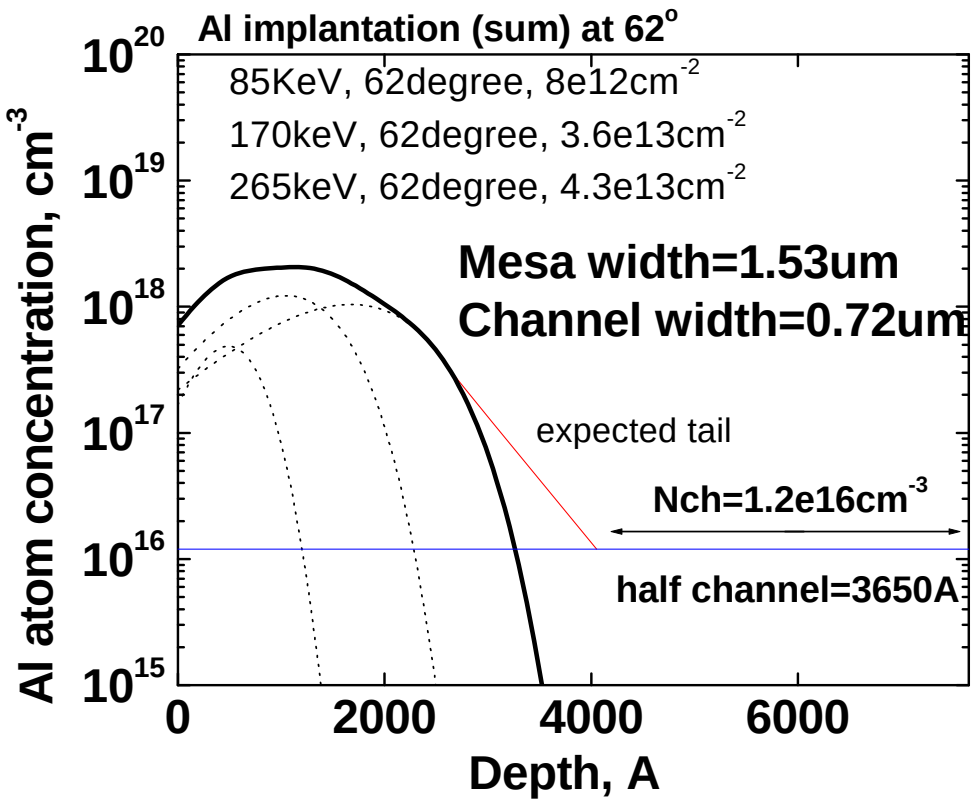


Fig 3.15: Simulated tilted Al implantation profile.

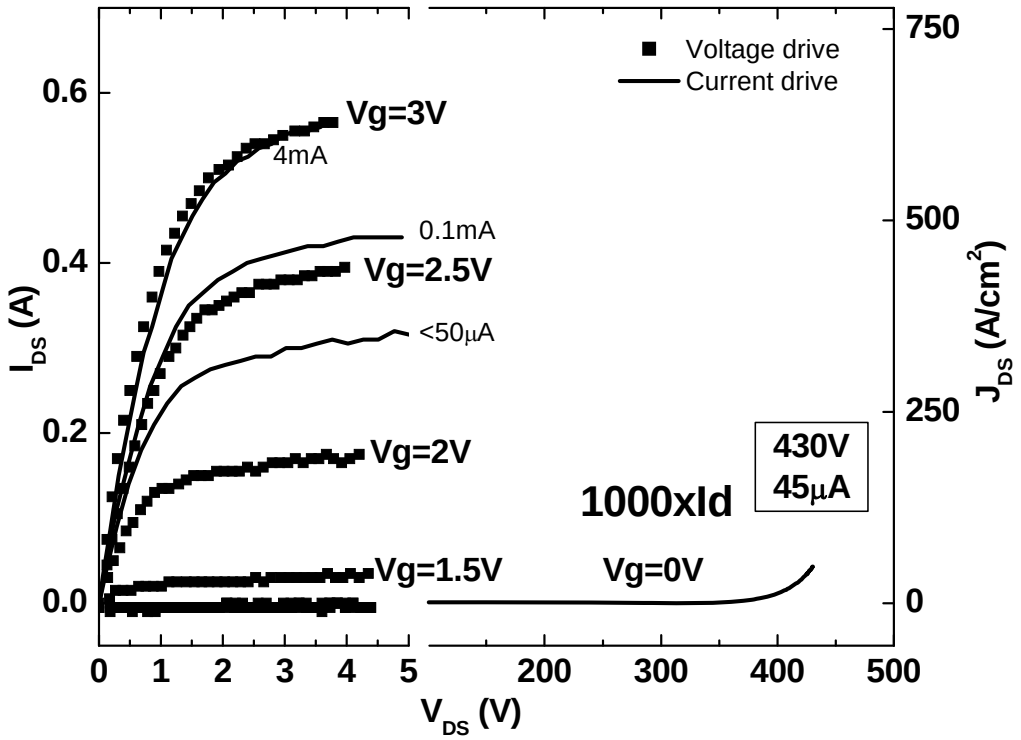


Fig 3.16: I-V curve of 430V TIVJFET.

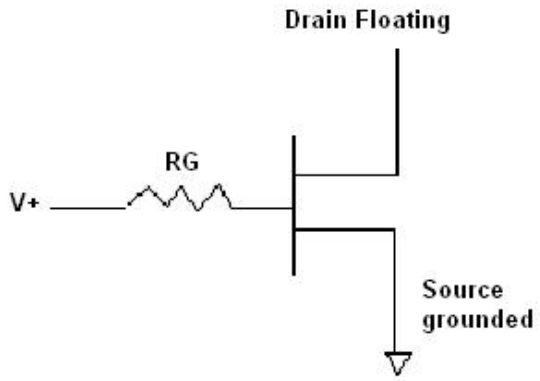


Fig 3.17: Gate-source diode forward IV curve will give a series resistance: the equivalent gate resistance.

Gate effective resistance was also measured to evaluate effectiveness of thick gate overlay. As shown in Fig.3.17 and Fig 3.18, by using mask design with gate bus added and thick gate overlay, Gate resistance of TIVJFET with is very small.

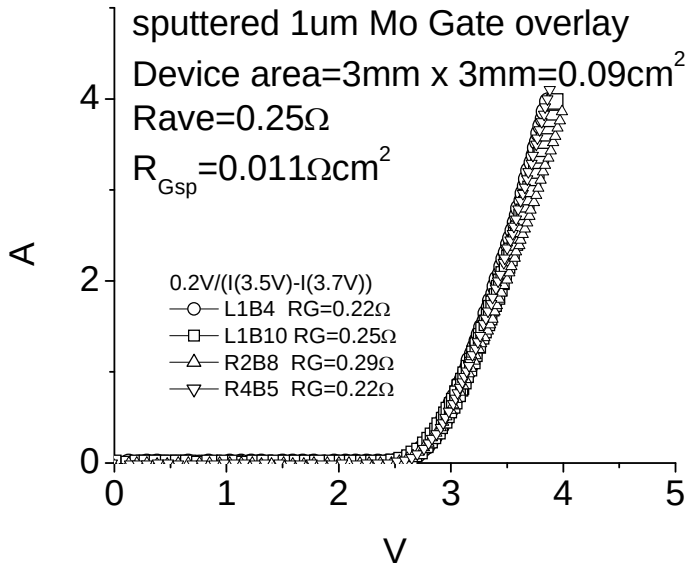


Fig 3.18(a): Gate resistance of a TIVJFET device with 1um Mo gate overlay is only $0.011\Omega cm^2$.

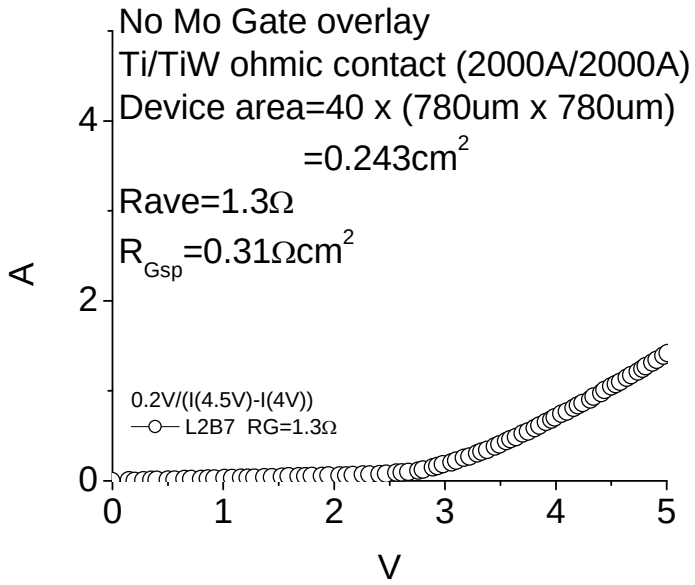


Fig 3.18(b): Gate resistance of a TIVJFET device without gate overlay is $0.31\Omega cm^2$.

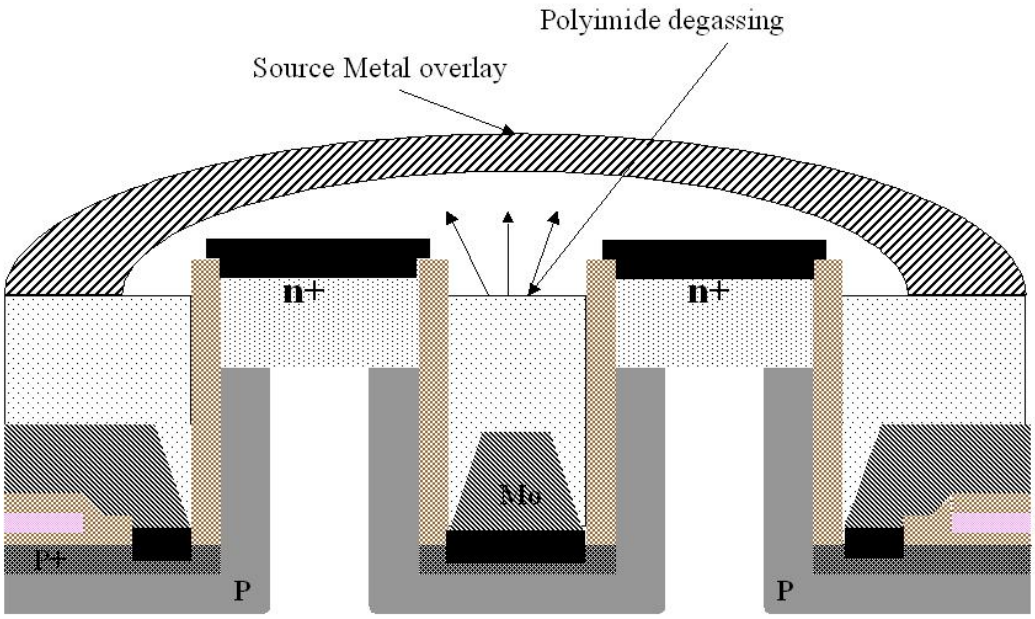
3.2.5 Oxide trench-fill process:

Conventional TIVJFET process [25, 32] uses polyimide planarization layer to fill the trenches. Polyimide layer was then etched back in oxygen plasma and thick overlay metal for source and gate was deposited. The advantage of polyimide planarization is that it is a fast, easily controllable process: polyimide can be simply deposited by spinning. And by adjusting spinning speed, acceptable thickness uniformity can be achieved. And etch back of polyimide is also very fast: 1μm polyimide can be etched in a few minutes (depending on plasma power).

The disadvantage of polyimide is that it cannot withstand high temperature (Fig 3.19), this is not acceptable because SiC device is targeting high-temperature applications.

The obvious alternative is oxide trench filling. PECVD SiO2 layer was deposited and planarized (Fig 3.20).

(a) Polyimide degassing



(b) Overlay bubbles up

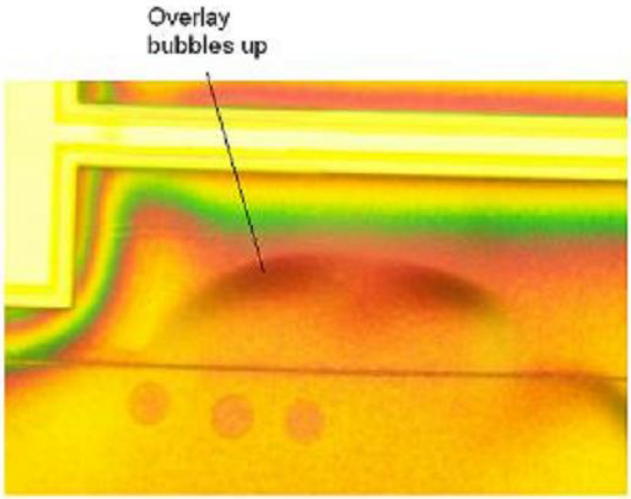


Fig 3.19: It was hypothesized that Polyimide degassing at 250C, causing source overlay to bubble.

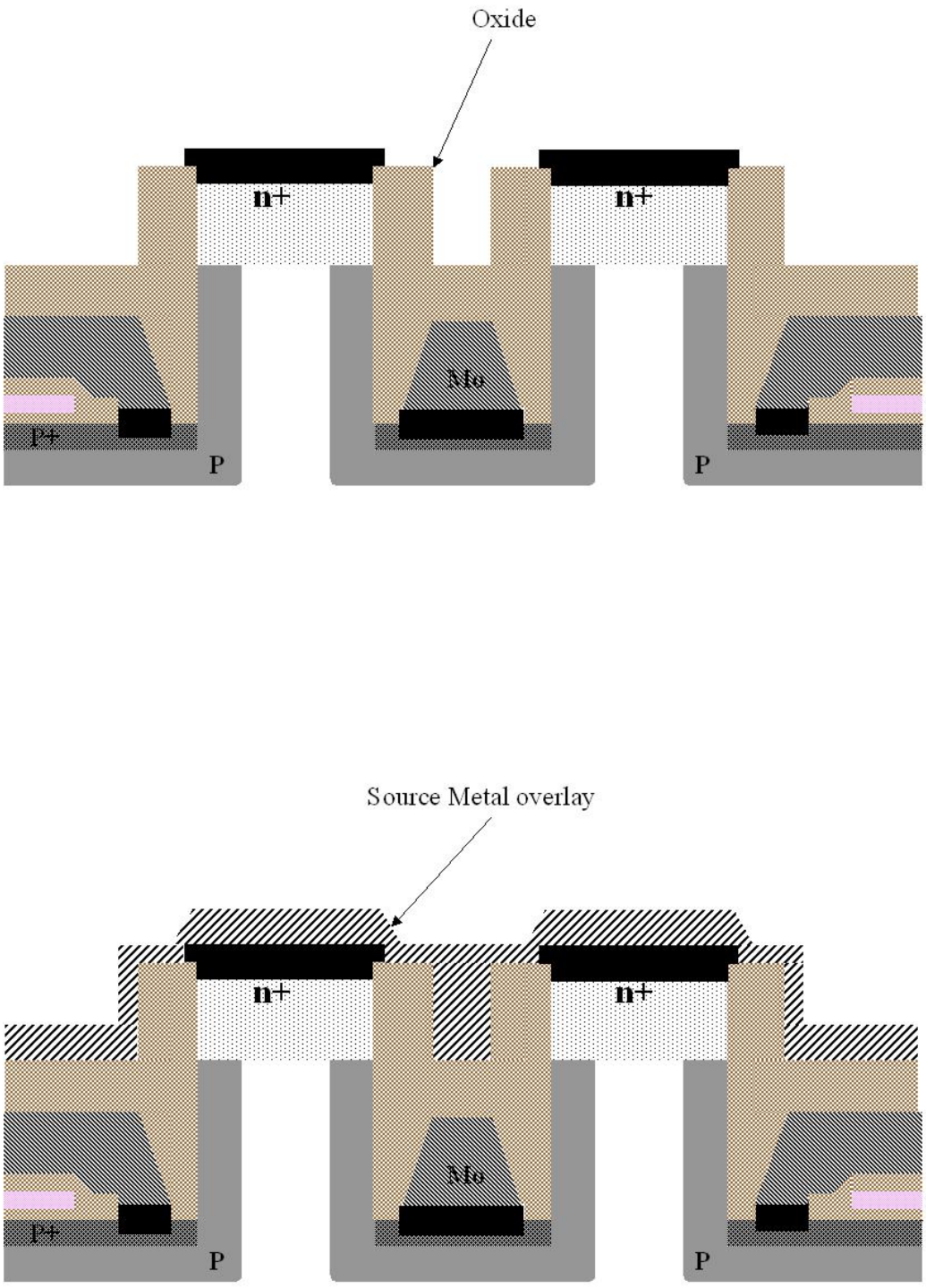


Fig 3.20: Oxide fill and metal overlay.

3.2.6 2.0mΩcm^2, 1568V normally-on TIVJFET

The revised Oxide planarization process was successfully implemented in a batch of normal-on TIVJFET. Wafer structure and correctional view is shown in Fig 3.21. The device used an n-type epi-layer of 15μm with doping of 2×10^{16}cm^{-3}, part of which served as the channel layer, the remaining 12μm n-type epi-layer serving as the drift layer. On top of this layer was an n^+ ohmic contact cap layer.

The period of one unit cell is 3.8 μm. Comparing with the unit cell width of 5.5 μm [16], this corresponds to a 50% increase in device packing density. There were two device sizes: big and small. The small device active area is 9.0×10^{-4}cm^2.

New processes described above were used on this device: including Bosch trench etching process, Ni contact process with SiN recess, thick gate overlay process and oxide trench fill process.

Fabrication started with gate trench etching by Bosch process. The resulting mesa and trench structure is shown in Fig 3.22. The mesa widths were ranged from 1.3~1.7μm across wafer. Then tilted Al implantation was done, to form highly vertical channels with channel width ranged from

0.5~0.9μm (Fig 3.23). The sample was then annealed at 1,550°C for 30 min to activate implanted Al.

MJTE structure was optimized on a separate test sample. MJTE structure has three stages, each stage 15μm wide. The depths of outer two JTE stages were 400Å each. The depth of the innermost step has been optimized to get maximum breakdown voltage (Fig.3.24). Optimum blocking voltage/reverse leakage corresponded to about 2400Å etching depth for innermost JTE step. After optimum MJTE structure had been confirmed, it was reproduced on a wafer with TIVJFET devices. Considering thermal oxidation consumption, 2200Å was used as optimum JTE-1 depth.

Surface passivation was done by thermal oxidation at 1,100°C for 2 hours in wet O_2 followed by a 200-nm PECVD silicon nitride. Source and gate ohmic contacts were done by self-aligned Ni silicide process (with SiN recess process). Then source, gate and drain ohmic contacts were annealed at 1,000°C for 5 min. To reduce gate resistance, thick gate-overlay metal was deposited and patterned using Mo gate-overlay process. Finally, SiN/Oxide/SiN layer were deposited and etched back to fill the trenches. Contact windows were opened and thick source overlay metal was deposited.

For switching applications, Gate resistance should be reduced to increase switching speed. The Gate effective resistance of the fabricated device was extracted from the forward I-V curve of Gate-Source junction (Fig. 3.25). As can be seen that the specific gate effective resistance is as small as $8.4 m\Omega cm^2$.

For normally-on JFET, a negative gate bias is needed to achieve maximum blocking voltage. A reliable gate-source junction is needed to sustain this negative gate bias. Fig. 3.26 shows the reverse gate-source junction I-V curve of fabricated TIVJFET. It can be seen that the gate-source junction leakage current is still small up to 30V reverse bias, which is enough to pinch off the vertical channel (Fig. 3.27).

The fabricated devices were characterized by using a Tektronix 371-A High Power Curve Tracer and a probing station. The forward I-V was measured using both voltage drive and current drive mode. Fig 3.27 shows I-V curves of the fabricated small devices of different channel width. Note that the leakage current has been multiplied by a factor of 10000 to show the detailed dependence.

Devices shown in Fig 3.27 (a) and (e) are particularly interesting. Fig 3.27 (a) can be compared with the TIVJFET reported in [16]. Fig 3.27 (e) can be compared with SiC-BGSIT reported in [17].

For the device in Fig 3.27 (a), the blocking voltage V_B has been measured to 1650V at V_G=-5V. Drain current is 0.225A at V_{GS} of 3V and V_{DS} of 0.47V, corresponding to an on resistance of 2.09Ω. Considering that device active area is $9.0\times10^{-4}cm^2$, device specific on resistance (R_{SP_ON}) is about 1.88mΩcm^2. At V_{GS} of 2.5V, V_{DS}=0.51V, forward current is 0.195A. It has specific on-resistance of 2.35mΩcm^2 when V_{GS}=2.5V. It is seen that current gain (I_D/I_G) is over 100 and 8000 at V_{GS} of 3V and 2.5V respectively.

It is interesting to compare Fig 3.27 (a) with the TIVJFET reported in [16] (Fig.3.28). Both devices needed small negative gate bias to close channel completely and they had similar blocking voltages. Device in [16] had R_{SP-ON} (measured at V_{GS}=5V) of 2.77mΩcm^2 while the device in Fig 3.27 (a) had R_{SP-ON} (measured at V_{GS}=3V) of 1.88mΩcm^2, corresponding to a 32% reduction. The reduction of on-resistance may be attributed to higher device packing density, higher channel doping density and optimized processing technology.

For the device in Fig 3.27 (e), the blocking voltage V_B has been measured to 1568V at V_G=-26V. At V_{GS} of 3V, V_{DS}=0.33V, forward current is 0.17A. It has specific on-resistance of 1.75mΩcm^2 when V_{GS}=3V. At V_{GS} of 2.5V, V_{DS}=0.47V, forward current is 0.21A. It has specific on-resistance of 2.0mΩcm^2 when V_{GS}=2.5V. Current gain is over 12000 and 120 when

V_{GS} is 2.5V and 3V respectively. The $R_{SP\text{-}ON}$ (measured at V_{GS}=2.5V) of 2.0mΩcm^2 is the lowest of all 1500V class normally-on SiC FETs reported to date.

For big TI-VJFET, device yield map was shown in Fig 3.29 and Table 3.1. I-V curve of two big devices with best voltages were shown in Fig. 30. Big device blocking-yield is low. It is hypothesized that big device size is large, thus the gate-drain junction breakdown voltage is limited by processing defects.

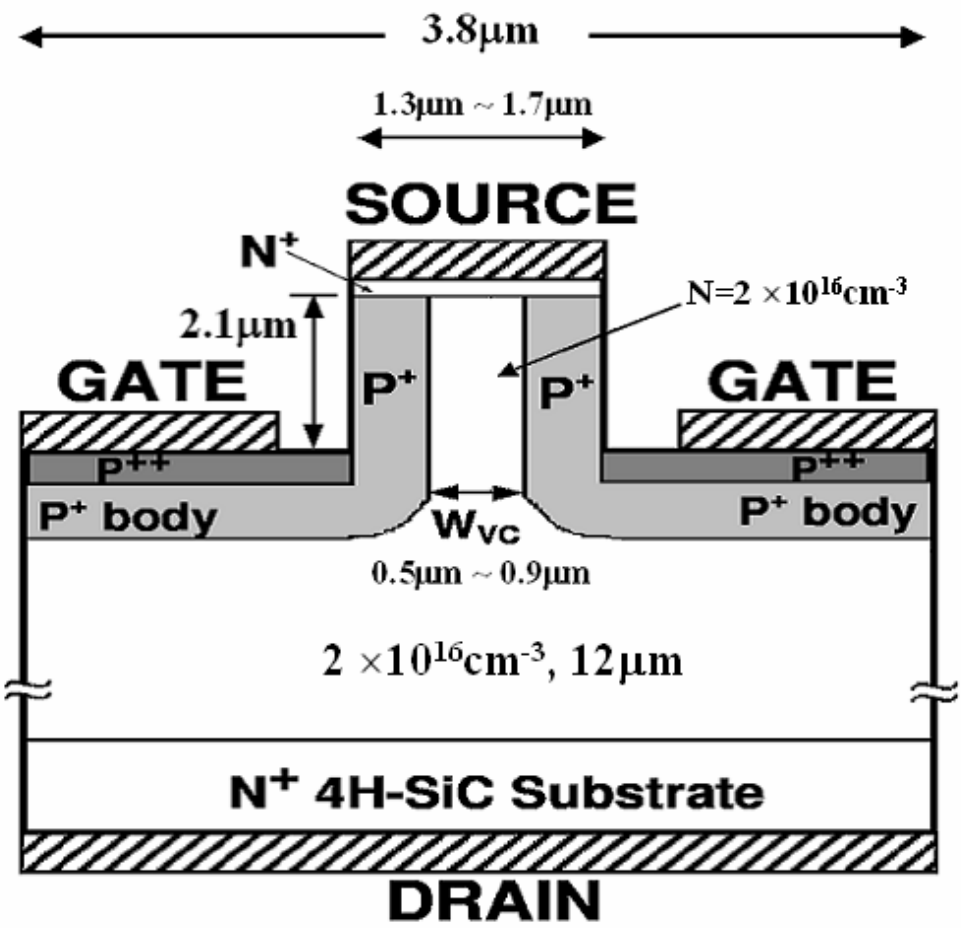


Fig 3.26(a): Cross-section of TIVJFET.

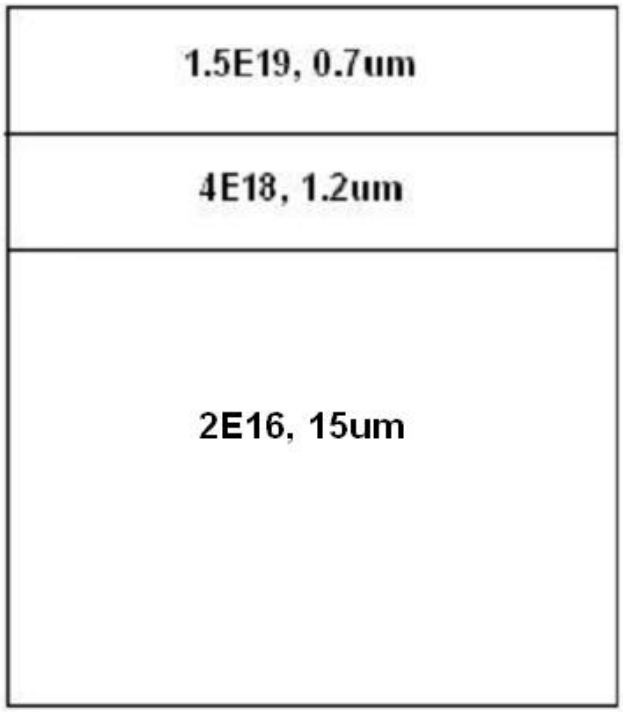


Fig 3.26(b): wafer structure of TIVJFET.

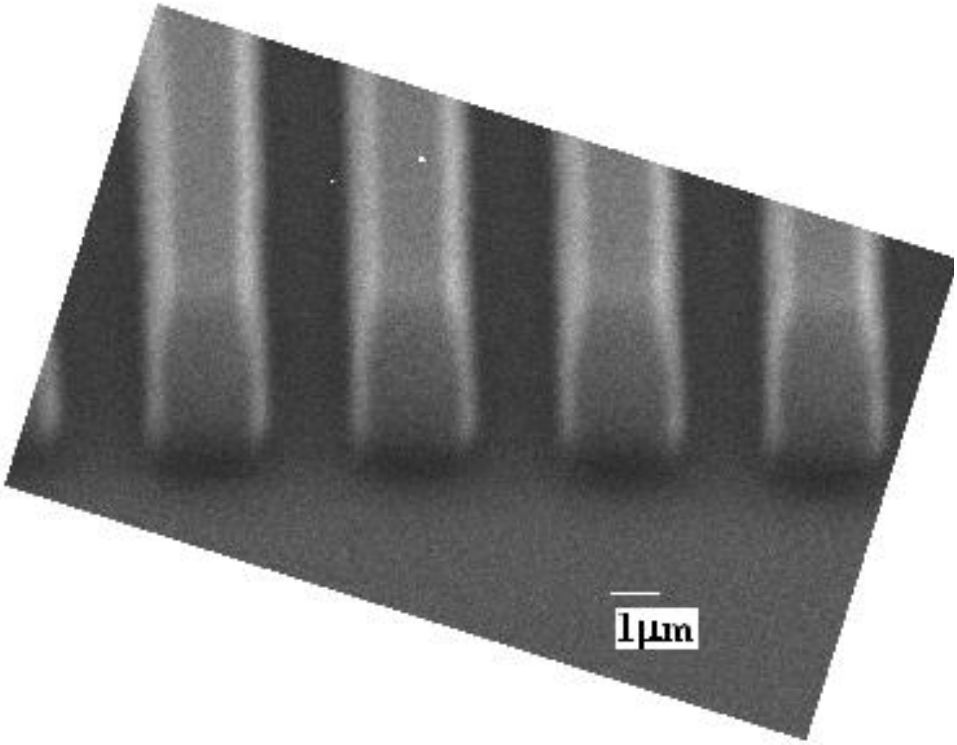


Fig 3.22: Etched mesa-trench structure.

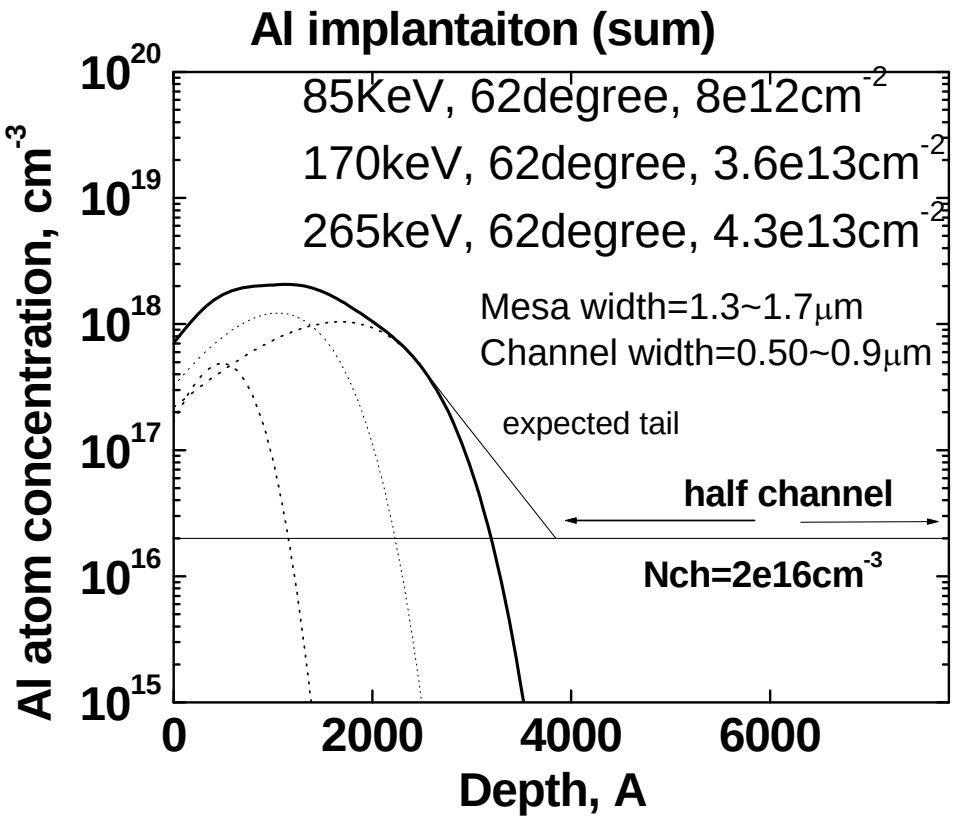


Fig 3.23: Sidewall Al implantation profile.

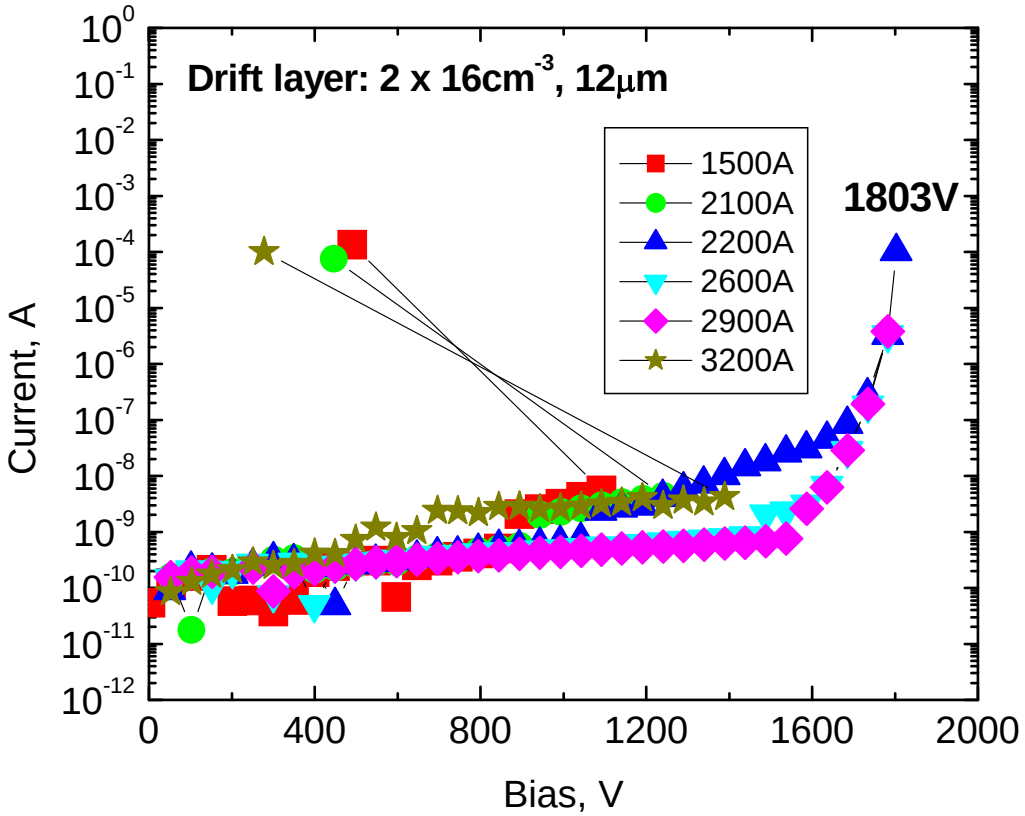


Fig 3.24: wafer MJTE optimization. Considering oxidation consumption. JTE-1=2200A.

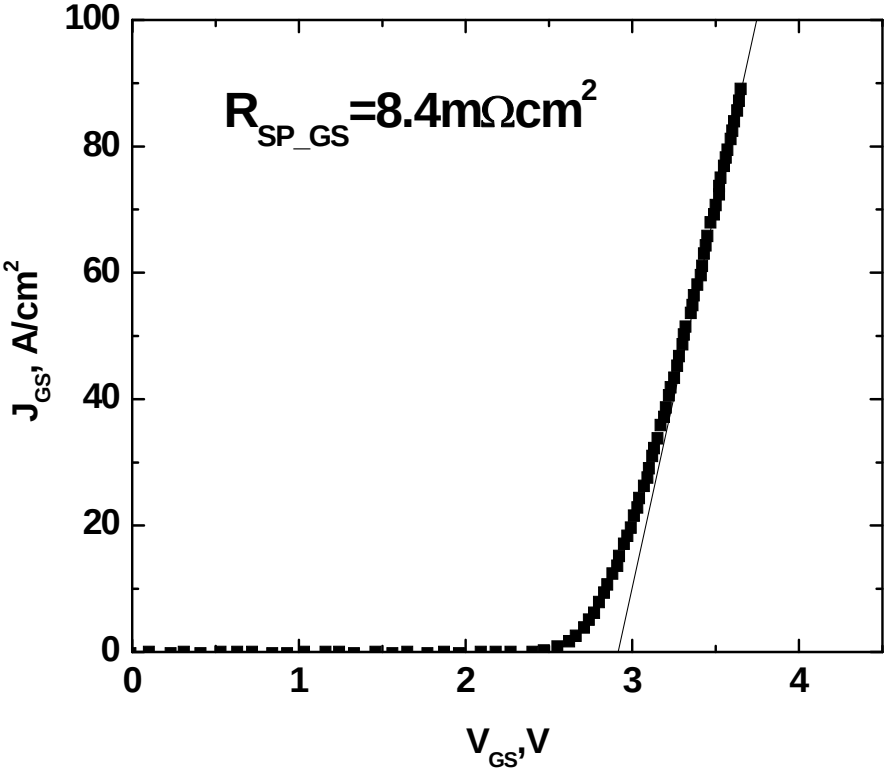


Fig. 3.25: Gate effective resistance is as small as 8.4mΩcm^2.

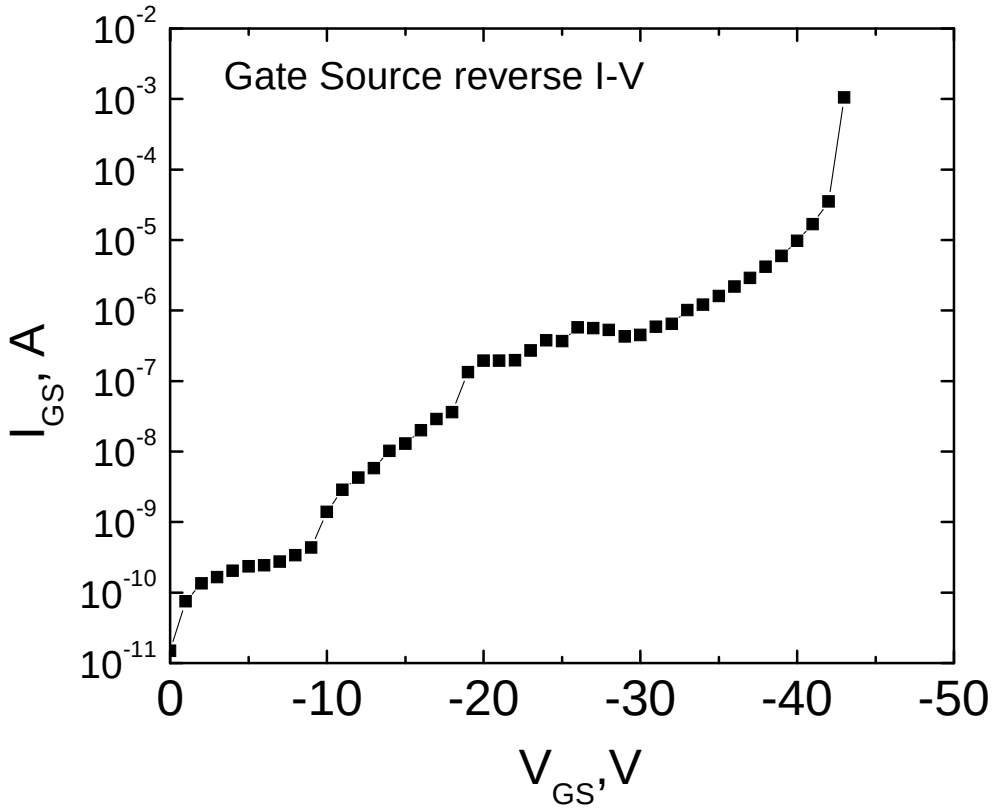


Fig. 3.26: Gate source junction reverse I-V curve of a small TIVJFET.

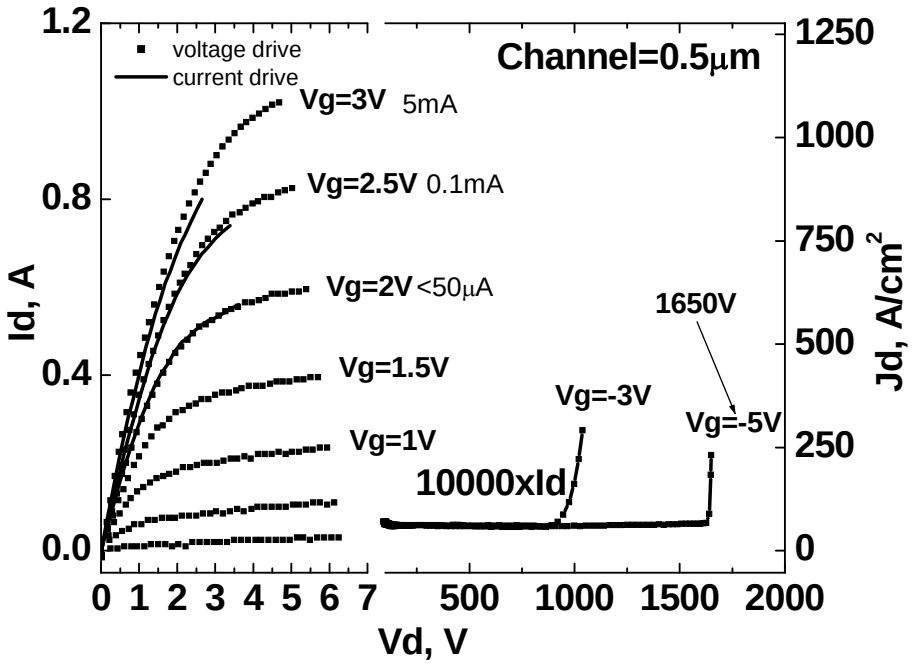


Fig 3.27(a): I-V curve of small TIVJFET with channel width of 0.5μm. At V_{GS} of 3V, V_{DS}=0.47V, forward is 0.225A. It has specific on-resistance of 1.88mΩcm^2 when V_{GS} =3V. At V_{GS} of 2.5V, V_{DS}=0.51V, forward current is 0.195A. It has specific on-resistance of 2.35mΩcm^2 when V_{GS}=2.5V. Current gain is over 8000 and 100 when V_{GS} is 2.5V and 3V respectively.

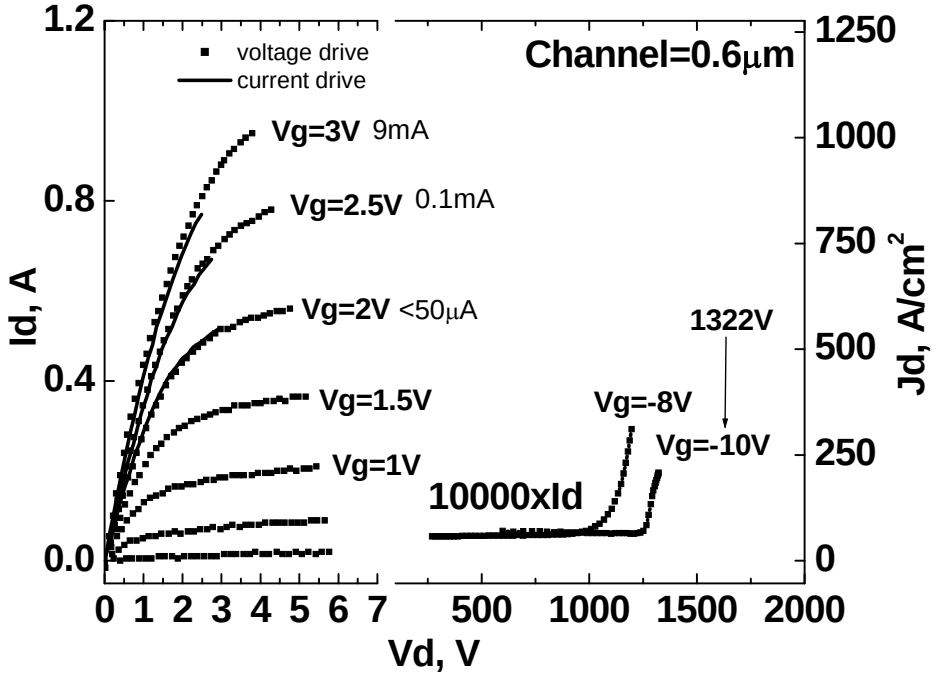


Fig 3.27(b): I-V curve of small TIVJFET with channel width of 0.6μm. At V_{GS} of 3V, V_{DS}=0.4V, forward current is 0.19A. It has specific on-resistance of 1.90mΩcm^2 when V_{GS}=3V. At V_{GS} of 2.5V, V_{DS}=0.44V, forward current is 0.17A. It has specific on-resistance of 2.33mΩcm^2 when V_{GS}=2.5V. Current gain is over 8000 and 100 when V_{GS} is 2.5V and 3V respectively.

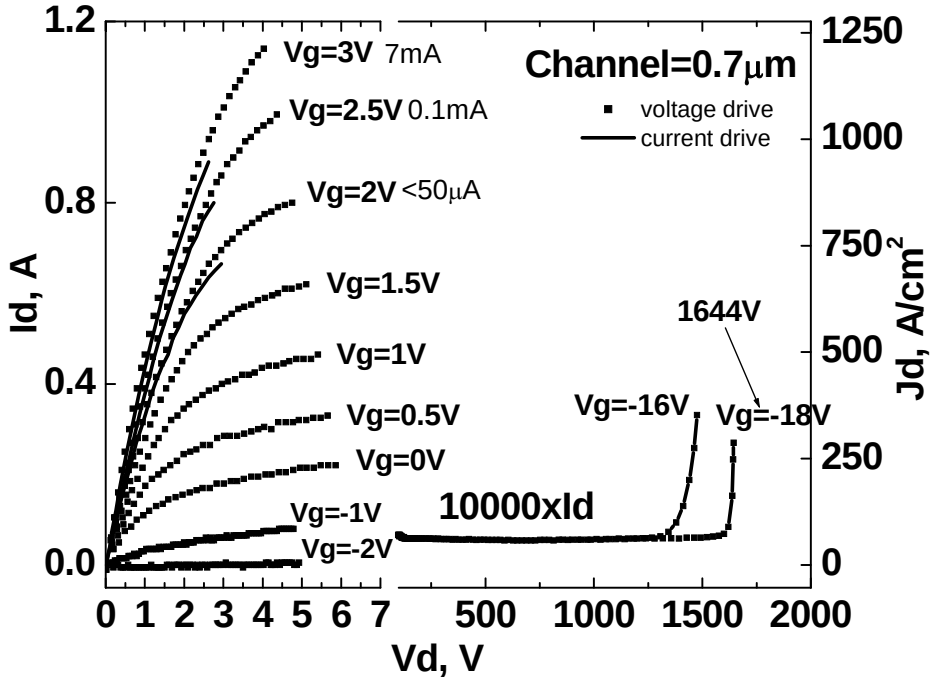


Fig 3.27(c): I-V curve of small TIVJFET with channel width of 0.7μm. At V_{GS} of 3V, V_{DS}=0.41V, forward current is 0.21A. It has specific on-resistance of 1.76mΩcm^2 when V_{GS}=3V. At V_{GS} of 2.5V, V_{DS}=0.47V, forward current is 0.19A. It has specific on-resistance of 2.23mΩcm^2 when V_{GS}=2.5V. Current gain is over 10000 and 100 when V_{GS} is 2.5V and 3V respectively.

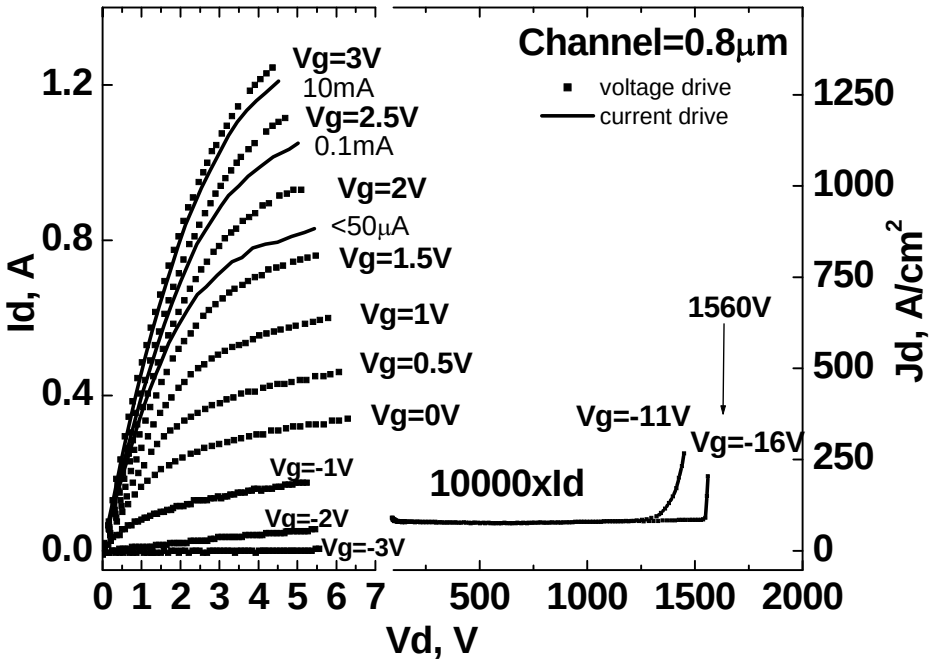


Fig 3.27(d): I-V curve of small TIVJFET with channel width of 0.8μm. At V_{GS} of 3V, V_{DS}=0.35V, forward current is 0.185A. It has specific on-resistance of 1.7mΩcm^2 when V_{GS}=3V. At V_{GS} of 2.5V, V_{DS}=0.39V, forward current is 0.17A. It has specific on-resistance of 2.06mΩcm^2 when V_{GS}=2.5V. Current gain is over 10000 and 100 when V_{GS} is 2.5V and 3V respectively.

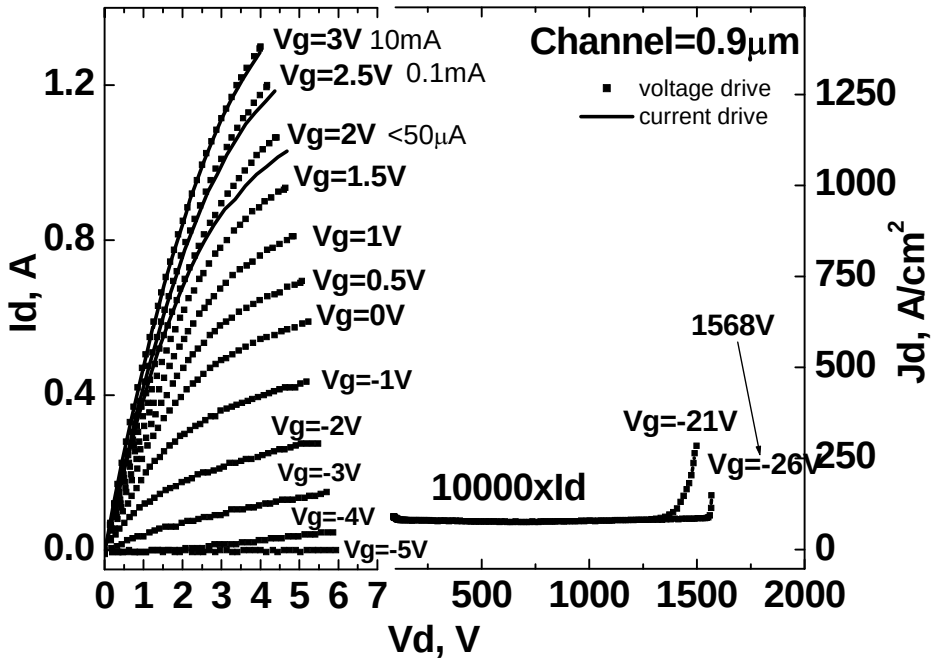


Fig 3.27(e): I-V curve of small TIVJFET with channel width of 0.9μm. At V_{GS} of 3V, V_{DS}=0.33V, forward current is 0.17A. It has specific on-resistance of 1.75mΩcm^2 when V_{GS}=3V. At V_{GS} of 2.5V, V_{DS}=0.47V, forward current is 0.21A. It has specific on-resistance of 2.0mΩcm^2 when V_{GS}=2.5V. Current gain is over 12000 and 120 when V_{GS} is 2.5V and 3V respectively.

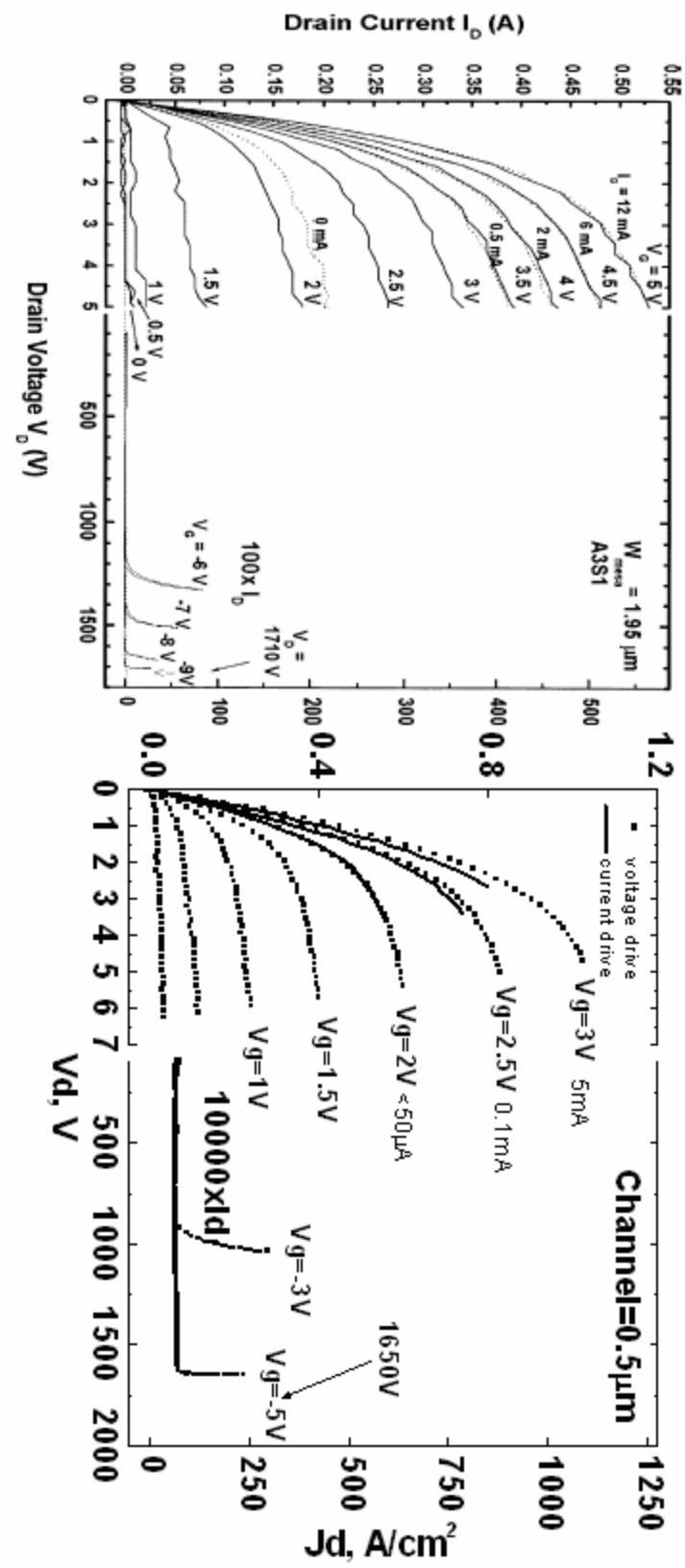


Fig. 3.28: Comparison of Fig 3.26(a) (1.88mΩcm^2) and device reported in [16] (2.77 mΩcm^2), this is a 32% reduction.

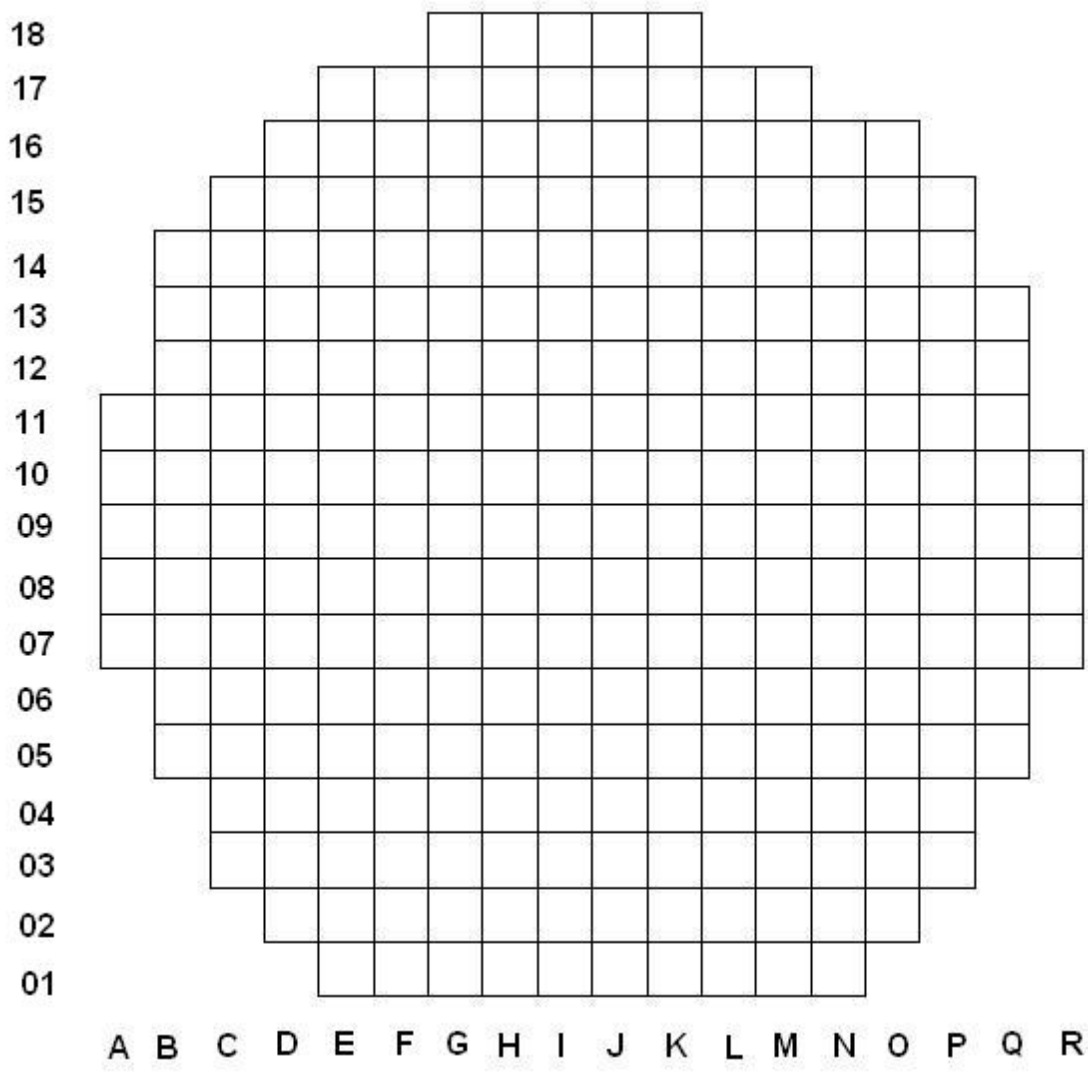


Fig 3.29: Big device placement map on 3-inch wafer. Each big device has active area of $9.36\times10^{-2}cm^2$.

18							50V 9.1mΩcm^2 0.5μm		
17							237V 3.3mΩcm^2 0.8μm		
16									
15									
14									
13		318V 4.2mΩcm^2 0.6μm							
12					50V 2.5mΩcm^2 0.6μm			353V 3.5mΩcm^2 0.9μm	
11				448V 2.4mΩcm^2 0.5μm					57V 3.7mΩcm^2 0.7μm
10								100V 3.3mΩcm^2 0.8μm	
09		195V 3.3mΩcm^2 0.9μm	205V 3.0mΩcm^2 0.7μm						
08							236V 3.6mΩcm^2 0.5μm	254V 3.1mΩcm^2 0.7μm	
07			96V 3.3mΩcm^2 0.6		155V 2.7mΩcm^2 0.6μm			130V 3.6mΩcm^2 0.9μm	
06			86V 2.8mΩ 0.9μm	154V 2.2mΩcm^2 0.5μm	60V 2.1mΩcm^2 0.8μm		106V 4.0mΩcm^2 0.5μm		
05		50V 3.5mΩcm^2 0.7μm		125V 2.8mΩcm^2 0.6μm		70V 2.6mΩcm^2 0.5μm			
04			74V 3.8mΩcm^2 0.5μm						
03				341V 3.0mΩcm^2 0.6μm	330V 2.5mΩcm^2 0.9μm	277V 3.2mΩcm^2 0.5μm			
02					183V 3.0mΩcm^2 0.6μm	122V 2.8mΩcm^2 0.7μm			
01									
	A	B	C	D	E	F	G	H	I

Table 3.1: Big device mapping on 3-inch wafer. The top number in each device represent the blocking voltage V_B at leakage current I_{DS} of 10μA, with gate bias V_{GS} of –30V. The middle number represents R_{SP_ON} at current density of 100A/cm^2. The third number represents the vertical channel width.

18									
17									
16		328V 3.1mΩcm^2 0.7μm	263V 3.5mΩcm^2 0.5μm	243V 3.4mΩcm^2 0.6μm	174V 3.4mΩcm^2 0.7μm	160V 3.7mΩcm^2 0.5μm			
15				245V 3.2mΩcm^2 0.7μm			382V 5.0mΩcm^2 0.5μm		
14	85V 3.5mΩcm^2 0.6μm		190V 3.2mΩcm^2 0.9μm		71V 3.6mΩcm^2 0.5μm	403V 3.2mΩcm^2 0.9μm			
13						180V 5.7mΩcm^2 0.6μm			
12			58V 4.3mΩcm^2 0.9μm		229V 3.6mΩcm^2 0.5μm				
11		231V 3.0mΩcm^2 0.9μm	468V 4.3mΩcm^2 0.5μm		217V 3.1mΩcm^2 0.7μm	519V 3.9mΩcm^2 0.8μm			
10	90V 4.0mΩcm^2 0.5μm								100V 4.5mΩcm^2 0.7μm
09	265V 4.1mΩcm^2 0.7μm						230V 3.3mΩcm^2 0.7μm	150V 3.0mΩcm^2 0.9μm	
08		212V 3.3mΩcm^2 0.5μm		130V 3.5mΩcm^2 0.7μm	436V 3.5mΩcm^2 0.8μm				110V 5.1mΩcm^2 0.8μm
07		119V 3.1mΩcm^2 0.7μm		386V 3.6mΩcm^2 0.9μm			206V 3.4mΩcm^2 0.7μm	200V 3.1mΩcm^2 0.8μm	
06								246V 3.2mΩcm^2 0.5μm	
05							142V 3.5mΩcm^2 0.6μm		
04							188V 3.3mΩcm^2 0.8μm		
03	233V 3.0mΩcm^2 0.7μm			152V 3.4mΩcm^2 0.6μm					
02				174V 3.1mΩcm^2 0.9μm	315V 3.7mΩcm^2 0.5μm				
01					205V 3.4mΩcm^2 0.7μm				
	J	K	L	M	N	O	P	Q	R

Table 3.1(cont.): Big device mapping on 3-inch wafer. The top number in each device represent the blocking voltage V_B at leakage current I_{DS} of 10μA, with gate bias V_{GS} of –30V. The middle number represents R_{SP_ON} at current density of 100A/cm^2. The third number represents the vertical channel width.

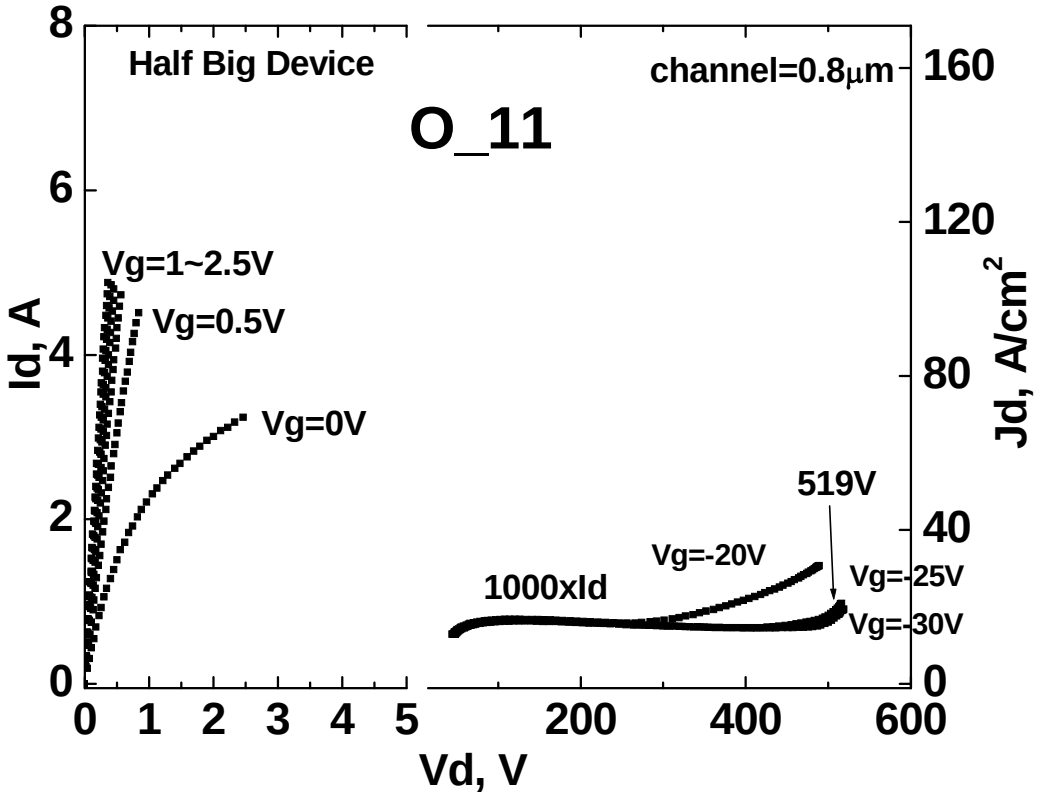


Fig 3.30 (a): A typical big TIVJFET I-V curve. The device active area is $9.36\times10^{-2}cm^2$. The vertical channel width is 0.9μm.

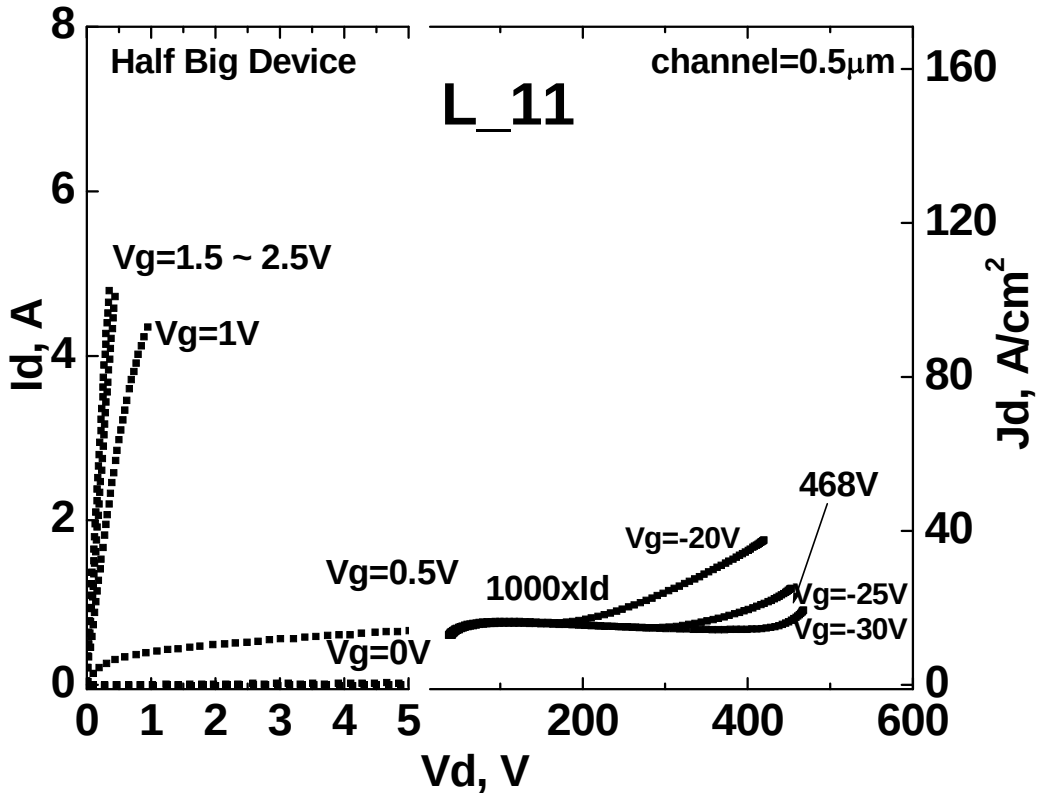


Fig 3.30 (b): A typical big TIVJFET I-V curve. The device active area is $9.36\times10^{-2}cm^2$. The vertical channel width is 0.5μm.

Chapter 4. Conclusions

Comparison with Latest Publications

4H-Silicon Carbide TIVJFET is an excellent candidate for high temperature and high power switching applications. This thesis reviewed a fabrication process that lead to the fabrication of a normally-off 10 kV, 106 mΩcm^2 TIVJFET with a record high value of 943MW/cm^2 for the figure of merit V_B^2/R_{SP_ON} for normally-off SiC FETs.

The fabrication challenges were discussed and developments of simpler, more reliable processes were described. And new processes were confirmed by several batches of TIVJFETs with various structures.

A 430V normally-off TIVJFET of very low R_{SP_ON} of 1.6mΩcm^2 was achieved using new developed processes. This device had a channel resistance is 0.67mΩcm^2, corresponding to about one third of channel resistance reported in [25]. This R_{SP_ON} is the lowest among all 400V class normally-off SiC FETs reported to date.

A 1568V normally-on TIVJFET was fabricated using new developed processes. R_{ON-SP} was 2.0mΩcm^2 when current gain was over 12000 (V_{GS}=2.5V). And R_{ON-SP} was 1.75mΩcm^2 when current gain was over 120 (V_{GS}=3V). This R_{SP_ON} is the lowest among all 1500V class normally-on

SiC FETs reported to date. Comparing with the device reported in [16], at the same current gain of 100, this R_{SP_ON} corresponded to a 37% reduction.

The newly developed processes were essential in achieving these low channel resistances.

Future Work Suggestions

Some of the processes developed in this thesis needed further studies:

(1) Gate trench etching mask definition: currently, AlTi layer was defined by contact lithography with 1μm precision and metal wet etching. Advanced technology such as nano-imprint lithography and metal dry etching should improve channel width uniformity.

(2) Oxide trench fill: Oxide etchback process is time consuming and even with SiN added as top cover, shorting problems may still happen sometimes due to pinholes in dielectric layer. New processes like CMP (chemical and mechanical polishing) should be implemented to simplify oxide planariztion process and help reducing pinholes.

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