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All Organic Memory Devices Utilizing C₆₀ Molecules and Insulating Polymers

By

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Abstract of Dissertation

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The convergence of mobile technologies combined with stricter power requirements and increasing demands have strained the current memory technology. Newer technologies such as phase changing, ferroelectric, and magnetic random access memories are unsatisfactory in meeting the new requirements. We propose a new memory technology based on our initial discovery of charge storage in C₆₀ molecules within poly (4-vinyl phenol) (PVP). To understand the memory potential, we created single-layer devices consisting of ~30nm films of PVP+C₆₀ sandwiched between aluminum (Al) electrodes. Current versus voltage (I-V) sweeps showed a significant hysteresis of 75nA, with distinguishable memory states. Room temperature charging of C₆₀ was confirmed indirectly through capacitance versus voltage measurements and directly by monitoring the A_{1g} characteristic peak of C₆₀ during Raman measurements. We demonstrated memory operations by applying read-write-erase (RWE) pulses. The PVP+C₆₀ devices exhibited memory retention for over 1 hour and response times of around 10ns. Characteristic hysteresis was demonstrated at the nanoscale. Conduction models were fitted at room temperature to the

I-V curves. It was found that combination of direct and Fowler-Nordheim tunneling were the principle conduction mechanisms.

For a more technologically viable memory device, we developed a multi-layer device structure, consisting of a polystyrene (PS) capping layer. The resulting asymmetrical I-V curve exhibited a hysteresis ratio of 10^3 . RWE cycles were measured with clearly distinguishable states. The memory retentions were measured over 2 hours and the response time around 10ns. The stability of the multi-layer devices was improved. I-V measurements at temperatures varying from 4.2 K to 298 K were performed to construct a theoretical model. The I-V curves were found to be temperature independent and exhibited similar tunneling behaviors as the single-layer devices. A simple model for conduction and memory operation is proposed based on the I-V fits.

These devices exhibit the characteristics needed to satisfy the new demands for memory application and have the potential of becoming the first universal memory technology. They possess the high speed, non-volatility, thermal stability, and potentially high memory densities to make them ideal for use in laptops, iPhones, mp3 players, portable video players, GPS systems, and other mobile devices.

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Chapter 1 Introduction

1.1 Inorganic Memories

1.1.1 Current Technology

Memory devices play an important role in electronics, accounting for more than 20% of the semiconductor market [1]. Most memories are fabricated using the complementary metal oxide semiconductor technology (CMOS), the same technology used for fabricating computer chips. There are several different types of memory devices. The selection of the type of memory required for a given application is based on technology requirements and cost. The cost versus data access time for the three most common memory technologies available are shown in Figure 1-1a [2]. The existing three types of memory technologies can be broken down into two categories: volatile and non-volatile, as shown in Figure 1-1b. Volatile memories are generally fast, but require power to maintain their information. Non-volatile memories retain their information even after powering down but have a history of generally being significantly slower. However, newer memory technologies such as ferroelectric random access memories (FeRAM), magnetic random access memories (MRAM), and phase changing memories (PCM) are proving to be almost as fast as volatile memories. In addition to inorganic memories, organic memories are also being developed that use different memory storage technologies, such as redox reactions, charge storage, and charge transfer. These newer technologies should not only have the advantage of being non-volatile but also decrease the cost by utilizing cheap fabrication technologies [2]. Each type of memory as shown in Figure 1-1b will be discussed later, but the primary focus of this thesis will be the demonstration and fabrication of an all-organic memory technology using charge storage in fullerene molecules as the memory mechanism.

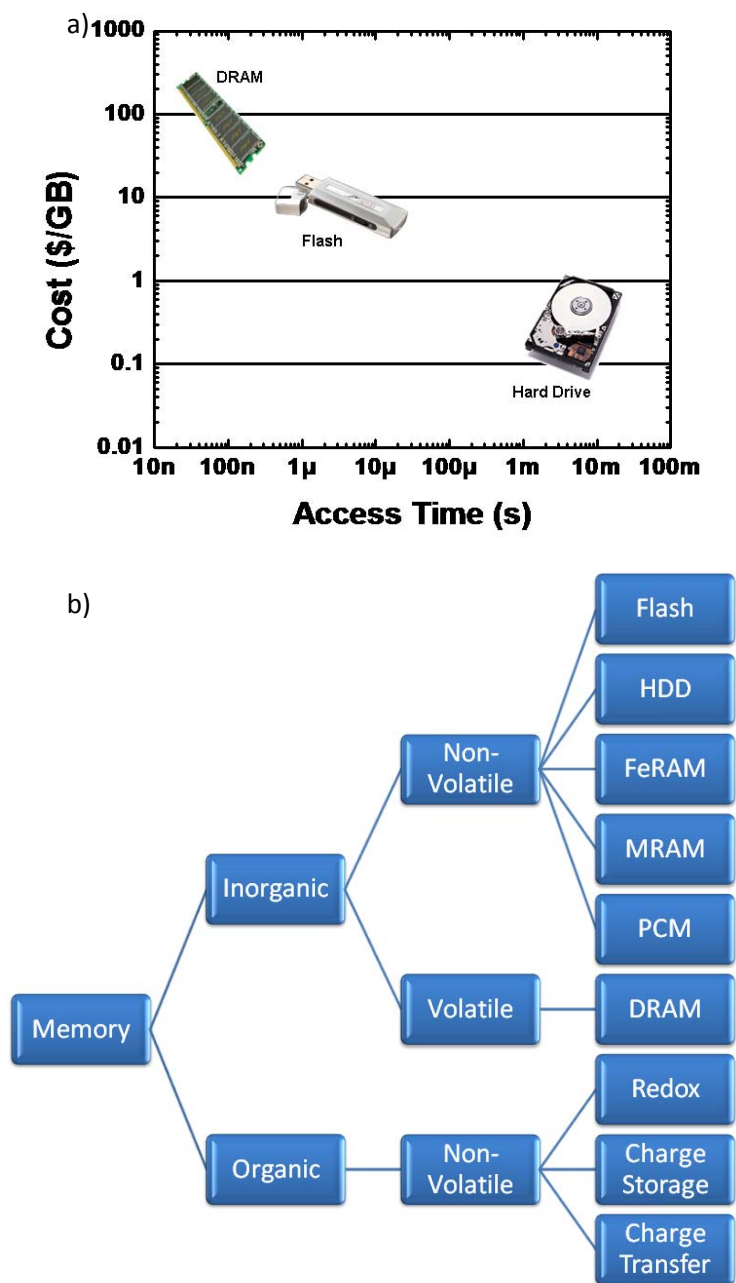


Figure 1-1 – a) Cost versus performance properties of existing memory device technologies [2]
b) Flow chart showing different types of memory technologies and mechanisms.

1.1.2 Dynamic Random Access Memory

The first type of memory, dynamic random access memory (DRAM), falls into the volatile memory category. DRAM is fabricated using standard CMOS technology using standard photolithography. A single DRAM cell is shown in Figure 1-2a consisting of a transistor (called the pass transistor) and a capacitor with column and row lines for connections. The row line connects to the gate of the transistor allowing it to control the connection of the column line to the capacitor. During a write operation, the row line is raised to turn on the pass transistor. The column line is charged according to the data being written. A '1' bit is written by the column line charging the capacitor, and a '0' bit is written by discharging the capacitor through the column line. Reading operations are performed in a similar fashion, except that the column line is used to sense the charge stored on the capacitor. DRAM can operate at high frequencies by using a capacitor to store the information. However, the charge can leak out over time, creating the need to refresh the data at predetermined intervals. This process reduces the speed of the DRAM chip but, despite this slowdown, the average access times are in the nanoseconds. The refreshing process also consumes power. In addition, when the power to the chip is turned off, the charge stored in the capacitor naturally discharges causing the memory to reset.

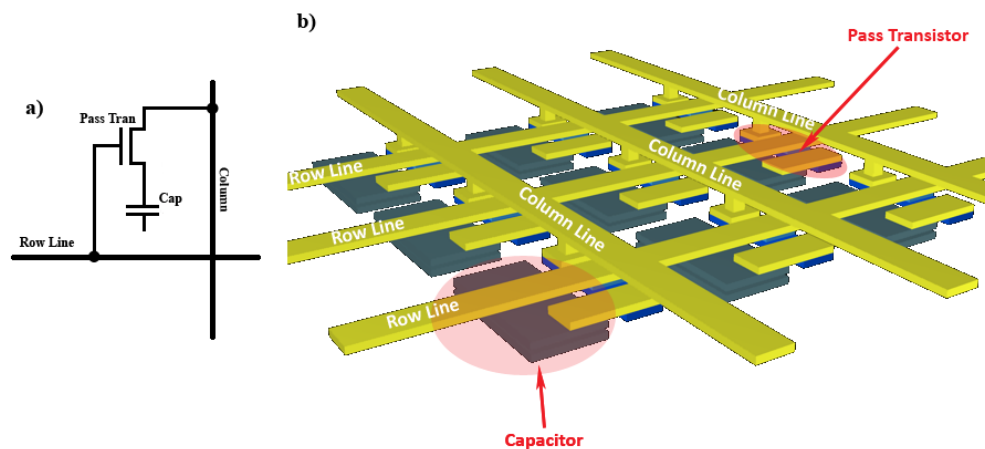


Figure 1-2 – a) Schematic of a single DRAM cell b) Array of DRAM cells [3].

1.1.3 Flash Memory

The second type of memory is called flash technology. Similar to DRAM, flash memories are also fabricated using standard lithography techniques. Unlike DRAM, flash relies on charge storage in an insulator, which does not naturally leak out unlike the charge stored in a capacitor. The retention of charge allows flash to retain its information after a power down, making this type of memory non-volatile. A schematic of a flash cell is depicted in Figure 1-3a and an array of cells in Figure 1-3b.

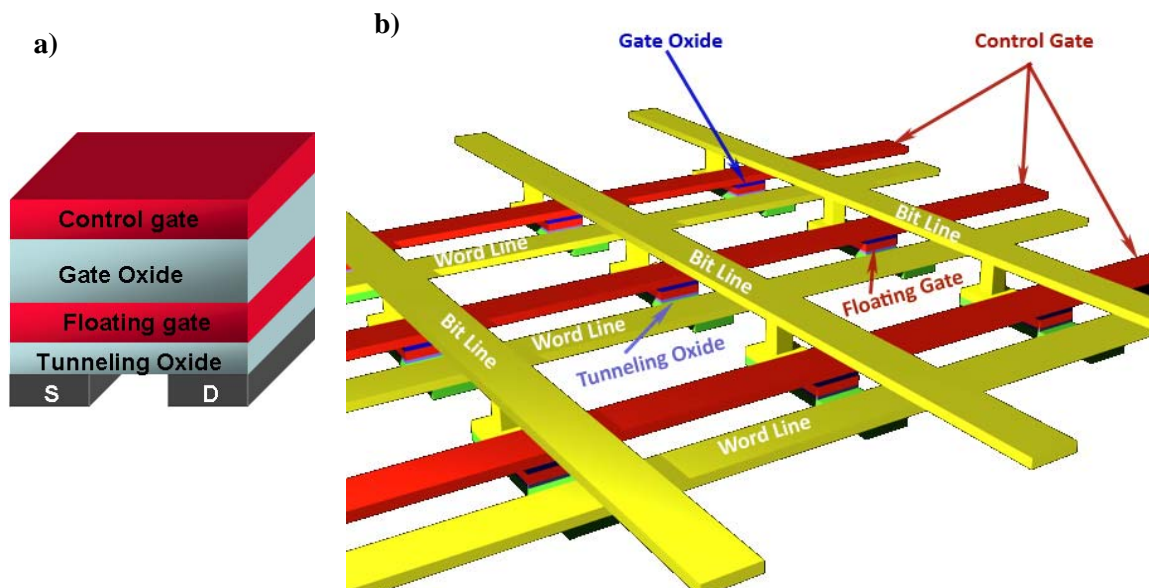


Figure 1-3 – a) Schematic of flash cell. The channel of the transistor is composed of p-type silicon. b) Array of flash memory cell [1, 4-7].

The flash cell is composed of a floating gate and control gate, together called a double gate. The control gate operates as a standard gate for transistors, controlling the flow of current in the channel of the transistor, between the Source (S) and Drain (D) contacts. The floating gate is electrically isolated by surrounding it with a thin oxide known as the tunneling oxide, which

separates it from the channel, and a gate oxide to separate it from the control gate. The isolated floating gate stores charges, which affects the functionality of the control gate. The thickness of the tunneling oxide is chosen so that tunneling and hot electron injection can occur while maintaining capability of charge storage in the floating gate. Conversely, the gate oxide is thick enough such that tunneling or hot electron injection cannot occur. A write operation is performed by turning the transistor ON with a high Drain (D) to Source (S) voltage, so that the electrons traveling in the channel gain enough energy to pass over the barrier formed by the tunneling oxide. The stored charges screen the applied Gate (G) voltage during reading operations and cause a voltage threshold shift. A negatively charged floating gate is considered a '0' bit and a neutral condition as '1' bit. The cell can be erased by applying a negative gate voltage and positive voltages to both the source and drain contacts. This condition allows Fowler-Nordheim (i.e. field enhanced as described later in this chapter) tunneling of electrons to occur from the floating gate to the channel. Multiple cells are typically erased at once, due to the high voltages used during erasing. In fact, this is where the name flash comes from, since arrays of cells are erased at once. While the charge storage in the floating gate does allow for non-volatile operation, it is also the reason for high power consumption, due to the high voltages used during write and erase procedures. flash memories typically run slower than DRAM memories because they need to allow enough time for the hot electrons to pass through the tunnel oxide to create a sufficiently large threshold shift. The typical access times are in the order of microseconds as opposed to nanoseconds for DRAM. In addition, the use of a double gate structure requires that the dielectric used is a triple layer of oxide-nitride-oxide. This adds additional processing steps that keep the cost of flash memories relatively high.[1, 4, 6, 7]

1.1.4 Hard Disk Drive

The third type of memory is hard disk drives (HDD), which are also non-volatile and use magnetic domains on spinning disks known as platters to store information. HDDs rely on magnetic domains that are layered onto a platter. A head moves across the platter, which spins at approximately 10,000 RPM, and by using the phenomena called Giant Magnetoresistance (GMR), the head can sense the polarity of the magnetic field associated with each domain as shown in Figure 1-4. The head is composed of two magnetic layers separated by a non-magnetic spacer, weakly coupling the two layers. One layer is pinned to specific polarity while the resistance is changed by having the unpinned layer align itself to the direction of the magnetic fields associated with the domains. When the unpinned and pinned layers are aligned, the resistance is low. However, when the two layers are oppositely aligned, the resistance increases sharply. The high resistance is due to scattering of spin up and down electrons in both layers. The low resistance occurs when both layers are aligned allowing one type of spin-polarized electrons to easily pass through the layers. Write and erase procedures are performed by the head inducing a magnetic field that is sufficiently strong to flip the polarity of the magnetic domains in the platters. By scaling the magnetic domains down to the nanoscale, high memory densities are achieved. However, the reliance on mechanical parts needed to rotate the platter and position the head slows down the operation of the HDD. The average seek times (time to find and read the data) for a HDD is in milliseconds, as opposed to nanoseconds for flash and DRAM memories.

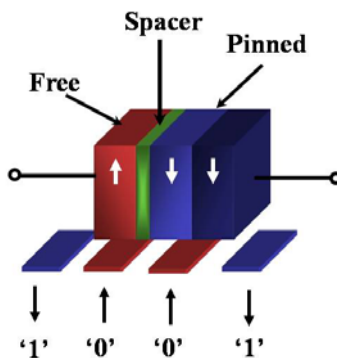


Figure 1-4 – Schematic of a hard drive in action. The head is composed of free and pinned magnetic layer separated by a spacer. The free magnetic layer will align itself to the magnetic domain on the platters. When the polarity is aligned with the pinned layer, the resistance across the head is low and when the layers are oppositely aligned the resistance significantly increases.

1.2 Future Memory Technologies

While DRAM, flash, and HDD each have their advantages, their drawbacks mean that none of these technologies are universal and so they are only suitable for specific niche applications. DRAM is used in applications that require high speed but where power consumption and large capacity is not necessary such as in the main memory of computers. flash memory systems are used where speed is not critical but power consumption and reliability are important. flash memories are ubiquitous in portable devices, ranging from mp3 players to digital cameras and cell phones. HDD memories are reserved for applications requiring very high memory densities, where data access time and power consumption are not a concern. Thus, HDDs are used for storage of user data and memory backups. Recently, there has been a push to converge several applications together, such as cell phones, mp3 players, and computers through the development of an universal memory technology. However, new memory technology that combines the advantages of the three main existing technologies is required in order to satisfy new demands. Below, we summarize the features of some new memory technologies that seek to replace existing devices.

1.2.1 Ferroelectric Random Access Memory

Ferroelectric random access memory (FeRAM) is an alternative memory technology based on the polarization of a ferroelectric material. The ferroelectric material is typically lead zirconium titanate (PZT) which belongs to a family of materials called perovskites which have the generalized chemical formula ABO_3 with PZT being $Pb\left(Zr_xTi_{(1-x)}\right)O_3$. The crystal structure of PZT (Figure 1-5a) is such that a semi-permanent dipole exists due to the fact that the center atom is slightly offset creating a non-uniform distribution of charge within the crystal, the dipole. Information is written by applying a voltage on the capacitor, which creates an electric field across the ferroelectric material. The inherent dipole then aligns itself to the electric field, and remains polarized when the field is removed. The PZT is sandwiched between two metal contacts in a capacitor configuration and is accessed through a transistor, as shown in Figure 1-5b. The gate of the access transistor is connected to the word lines, source is connected to the plate lines and the drain to the bit lines. If the stored charge from the polarized dipole is positive then a '0' bit is stored and if it is negative, a '1' bit is stored. A '1' bit is written by applying a positive voltage onto the plate line and grounding the bit line. The appropriate cell is targeted by turning on its associated transistor via its word line. To store a '0' bit the same process occurs except the bit line is positively charged and the plate line is grounded, creating the positive electric field and storing the '0' bit. Information is read by applying a positive voltage on the plate line and floating the bit line, while asserting the correct word line. This forces the capacitor to store a positive charge. If the previous state was a '0' bit, then no detectable change occurs on the bit line. However, if the information stored was a '1' bit, then a detectable signal occurs on the bit line. Because this process is destructive, the information must be written back, creating a two-step process for reading operations. [8]

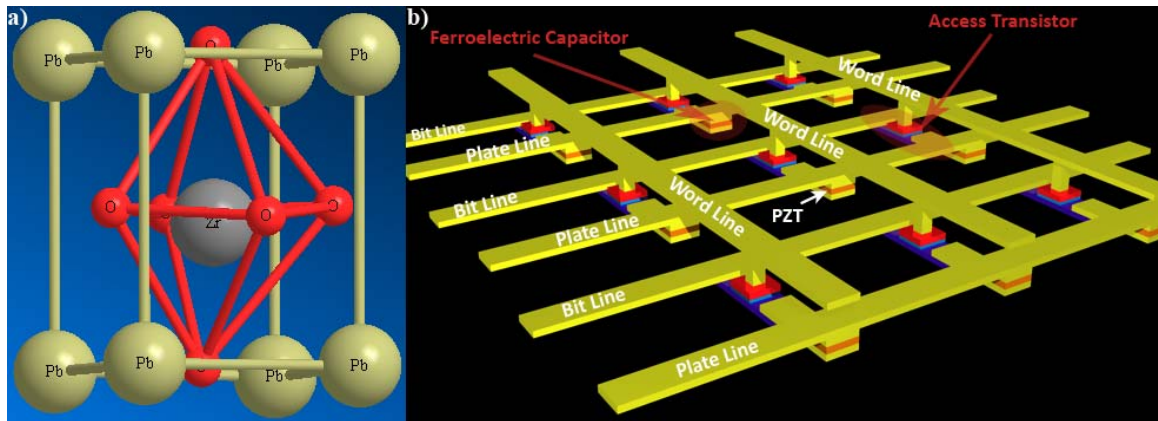


Figure 1-5 – a) Unit cell of lead zirconium titanate (PZT). b) FeRAM memory array, consisting of a ferroelectric capacitor connected to an access transistor. [8]

1.2.2 Magnetic Random Access Memory

Magnetic Random Access memory (MRAM) is another alternative memory system that is potentially universal. MRAM is designed to take advantage of magnetism, similar to HDD based technologies. Figure 1-6 shows a schematic of a MRAM memory array. Each cell consists of pinned magnetic layer and a free magnetic layer, separated by a tunneling layer (typically aluminum oxide[9]). Together they make up the magnetic tunneling junction, or MTJ. The MTJ is connected in series with an isolation transistor and a sense electrode. In addition, the MTJ is surrounded by two electrically isolated write lines, one on top and the other on the bottom. The cell is written by first turning off the isolation transistor and then sending current through the two write lines, inducing a magnetic field across the MTJ. The free magnetic layer in the MTJ will align itself to the induced field's direction. When the field is removed, the free magnetic layer retains the induced alignment. The cell can then be read by asserting the correct isolation transistor and passing a current through the MTJ and into the sense electrode. If the free magnetic layer in the MTJ is aligned to the pinned layer (parallel), then the resistance is low and

a '0' bit is read. However if the free layer is not aligned to the pinned layer (anti-parallel) then the resistance is sharply higher, giving a '1' bit. [9-12]

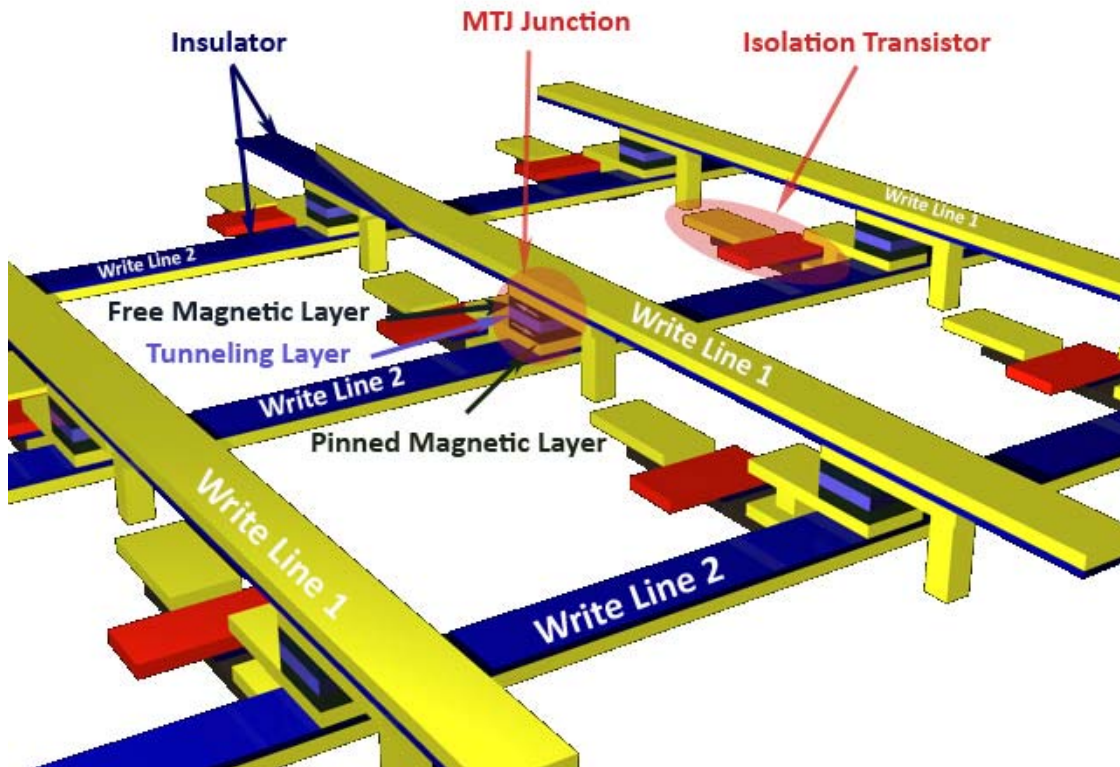


Figure 1-6 – MRAM memory array, consists of a magnetic tunneling junction (MTJ) connected to an isolation transistor. The MTJ is composed of a pinned and a free magnetic layer, separated by a tunneling layer. During the write operation, the current in the write lines induce a magnetic field, which orients the free magnetic layer. If the alignment is parallel to the pinned layer then the resistance is low, and when it is anti-parallel, the resistance is high. [9-12]

1.2.3 Phase Changing Memory

Phase changing memory (PCM), also known as Ovonic Unified Memory (OVM), is the third alternative memory solution that has been proposed. Instead of relying on polarization as in FeRAM or magnetic fields as in MRAM, PCM memories rely on the phase of material to store information. A PCM memory array is shown in Figure 1-7. The phase changing material is a chalcogenide alloy of germanium, antimony and tellurium (GeSbTe). Each cell consists of a resistive heater connected to the chalcogenide material. The cells are arranged in a cross-point architecture and are accessed by referencing the appropriate top and bottom electrodes. Information is written by heating the chalcogenide material to over 200°C via the electrical resistor. Above 200°C, the material changes from an amorphous state to a crystalline state reducing its resistance. To erase information, the material is heated above 600°C, to melt it and then quickly cooled to return it back to its amorphous state. The change in phase state occurs rapidly, within the order of 100ns. The cell is read by sending a small probe current to detect if the material is amorphous (high resistance) or crystalline (high conductance). [13, 14]

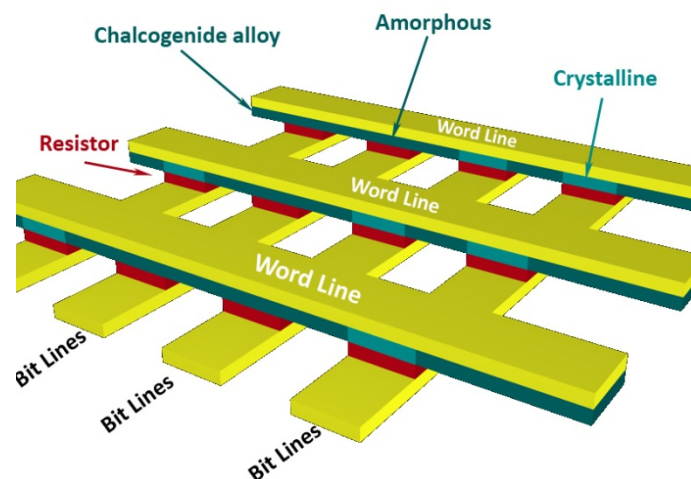


Figure 1-7 – Phase Changing Memory (PCM) array. A chalcogenide layer is connected to a resistor, which heats up the layer. Above 200°C, the material changes from amorphous to crystalline. The crystalline state gives a low resistance, while the amorphous state gives a high resistance state. [13, 14]

1.2.4 Future Memory Technology Limitations

FeRAM, MRAM, and PCM memories are designed to help meet the future memory demands while also addressing the shortcomings of the current technologies. The continued increase in memory density is accomplished by scaling down the technology, and is becoming increasingly difficult. For HDD based memories, the smaller magnetic domains become harder to detect due to the superparamagnetic effect. Similar effect occurs in DRAM, where the smaller charge associated with the smaller capacitors becomes increasingly more difficult to amplify and detect. Flash on the other hand have charge leakage issues, from the continued thinning of the oxides as the devices scale down. The newer memories solve these issues by using state-of-the-art materials as compared to standard CMOS technology. However, these new materials, whether ferroelectric, magnetic, or chalcogenide alloys, are difficult to integrate into the current manufacturing process. In addition, their larger cell sizes, except for PCM, make them difficult to achieve high memory densities despite their ability to scale further than the current technology. Table 1.1 compares the newer memory technologies with the current memory technology. Despite the lower densities, the newer memories are capable of operating at higher speeds than DRAM memories. However, both FeRAM and PCM consume 1mJ or more per bit, with MRAM consuming over 10mJ per bit. The high power demands also severely limit their uses, especially in the mobile applications. Combined, these factors force the cost of the new memory technologies to be significantly higher than the current technology. Memory based on FeRAM and MRAM technologies are commercially available today, costing approximately \$10K per Gb. PCM technology based devices are currently under development and not commercially available. Although FeRAM, MRAM, and PCM have tried to displace existing technology, the limitations with these newcomer technologies do not appear to offer a universal solution. Thus, there is an opportunity for additional technology to address the needs of memory devices.

Table 1.1 – Comparison of both current and new memory technologies. Despite the non-volatility and the high speeds of the new memory technologies, its cost, power and density make them incompatible with future memory needs. [1, 8, 10, 13, 15-17] ¹ No commercial product available

| Technology | Density | Speed | Power (J/bit) | Cost (\$/Gb) | Non-Volatile | Commercially Available |
|--------------|---------|------------|---------------|-------------------|--------------|------------------------|
| HDD | 500Gb | 1ms | 1mJ | 0.1 | Yes | Yes |
| DRAM | 2Gb | 50ns | 1mJ | 100 | No | Yes |
| FLASH | 30Gb | 10 μ s | 1 μ J | 10 | Yes | Yes |
| FeRAM | 64Mb | 100ns | 1nJ | 10,000 | Yes | Yes |
| MRAM | 4Mb | 100ns | 10mJ | 10,000 | Yes | Yes |
| PCM | 256Mb | 100ns | 1mJ | ---- ¹ | Yes | No |

1.3 Organic Memory Devices

An article by Scott from IBM Almaden Research Center [2] raises several issues related to emerging memory devices technology. He argues that the newcomer memory devices must exceed the existing speed and cost constraints of today's entrenched technologies. In addition, the new technology should also meet the new demands such as long term data retention (at least 10 years and up to 100 years for archiving), low power consumption (a few milliwatts or less for flash type of memory which is equivalent to 1nJ to write and 1pJ to read per bit) and large number of rewrite cycles.

Molecular devices that exhibit switching behavior [18-32] and negative differential resistance [27-30] could be an alternative to overcoming the limitations of silicon based microelectronics. However, scalable device fabrication is a major hurdle that must be overcome if molecular memories are to be realized. Memory devices from organic materials have the

potential to overcome many of the fabrication issues. For example, the low temperature spin on processing of organic memory technology allows the deposition of multiple layers which can lead to increase in density per given feature size. Organic materials and devices are of intense interest, since they can be deposited at low temperatures, inexpensively and over large areas on plastic, glass and metal foils. A recent review of organic materials and devices by Forrest [33] highlights the importance of this rapidly growing field.

Numerous devices such as field effect transistors, light emitting diodes and solar cells have been demonstrated with organic materials [33-39]. However, far fewer attempts have been undertaken to manufacture fully organic memory devices [2, 40-49]. Most of the reported organic memory devices are in fact hybrids of inorganic nano-particles, originally developed as three layers (organic semiconductor/metal thin film/ organic semiconductor) sandwiched between metal electrodes [43, 44]. More recently, inorganic nano particles have been dispersed in a polymer matrix, sandwiched between two metal electrodes [41, 42]. The current-voltage characteristics of these hybrid memory devices generally exhibit bi-stability, which is used as the basis for the memory device [41-45]. Recently, Möller *et al.* showed that a combination of organic materials and silicon diodes could be used in write-once read-many-times (WORM) memory devices [47]. In addition, macroscopic memory devices using Au nano-particles dispersed in a polymer matrix have also been demonstrated [50, 51].

1.3.1 Physics of Organic Memory Devices

1.3.1.1 Fundamental Conduction Mechanisms

In order to develop and optimize the performance of organic memory devices, it is important to thoroughly understand the mechanism responsible for the memory effect in

organic materials. The mechanisms can be determined through knowledge of charge transport through the material. Since most organic memory devices utilize either an insulating or semiconducting material, conduction mechanism in organic materials has been understood. However, before describing the specific details of charge transport through the devices that were investigated, we provide a thorough background of the various conduction mechanisms.

Electrical conduction through organic devices can be modeled through the same process that occurs for their inorganic counterparts. The six main conduction mechanisms associated with organic electronics are Direct Tunneling, Fowler-Nordheim Tunneling, Thermionic Emission, Schottky Emission, Poole-Frenkel, and Variable-Range Hopping. Thermionic, Schottky, and Poole-Frenkel are emission mechanisms. They are injection-limited, where the current is dictated by the injection of electrons through the contacts. In contrast, Hopping, Fowler-Nordheim, and Direct Tunneling are conduction-limited processes. Which occur when the contact interfaces can provide large number of carriers, but the organic layer is not capable of conducting most of them. Each mechanism will be discussed in detail in the following sections.

Direct Tunneling

Direct tunneling is a quantum mechanical effect in which electrons from the Fermi level of the metal contact tunnel through the barrier formed by the interfaces of an insulator and metal layers. Figure 1-8a schematically depicts the band diagram during direct tunneling. In Figure 1-8a, 'd' is the barrier width, E_F is the Fermi level of metals, E_{vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, and Φ_b is the barrier height between the metal contact and the insulator. The barrier height results from difference

between the electron affinity of the insulator and the work function of the metal contact. The relationship is described by:

$$\Phi_B = \Psi_M - \chi \quad (1.1)$$

A mathematical description of the tunneling process can be derived by solving the time independent Schrödinger's equation for a square barrier, and finding the probability of an electron tunneling from one contact to the other, $D(E_x)$, known as the Wentzel-Kramers-Brillouin (WKB) approximation shown in Equation (1.2).[52]

$$D(E_x) = e^{-\frac{4\pi}{h} \int_x^{x+d} \sqrt{2m(\Phi_B(x) - E_x)} dx} \quad (1.2)$$

Where h is Plank's constant, x is the position of the interface of the first metal contact and insulator in the x-direction, m is the mass of an electron, $\Phi_B(x)$ is the height of the barrier, and E_x is the energy of the incident electron in the x-direction. Using Equation (1.2) and calculating the net flow of electrons across the barrier, Equation (1.3), the current flow across the insulator, can be derived.[52, 53]

$$I = V \frac{q^2 \sqrt{2mq\Phi_B}}{4\pi\hbar^2 d} e^{-\frac{2d}{\hbar} \sqrt{2mq\Phi_B}} \quad (1.3)$$

Where I is the current flowing between the metal contacts, V is the applied voltage, d is the barrier width, Φ_B is the barrier height, \hbar is Planck's constant, and m is the mass of the electron. By solving Equation (1.3) for V , the voltage dependence can be derived.

$$I \propto V \quad (1.4)$$

In addition, based on Equation (1.3), direct tunneling is a temperature independent mechanism. Equation (1.4) is used to fit the direct tunneling model to experimental data. Figure 1-8b depicts an example of an experimental data fitting to the theoretical model. Due to the linear relationship of Equation (1.4) a straight line is fitted in a Current (I) vs. Voltage (V) graph

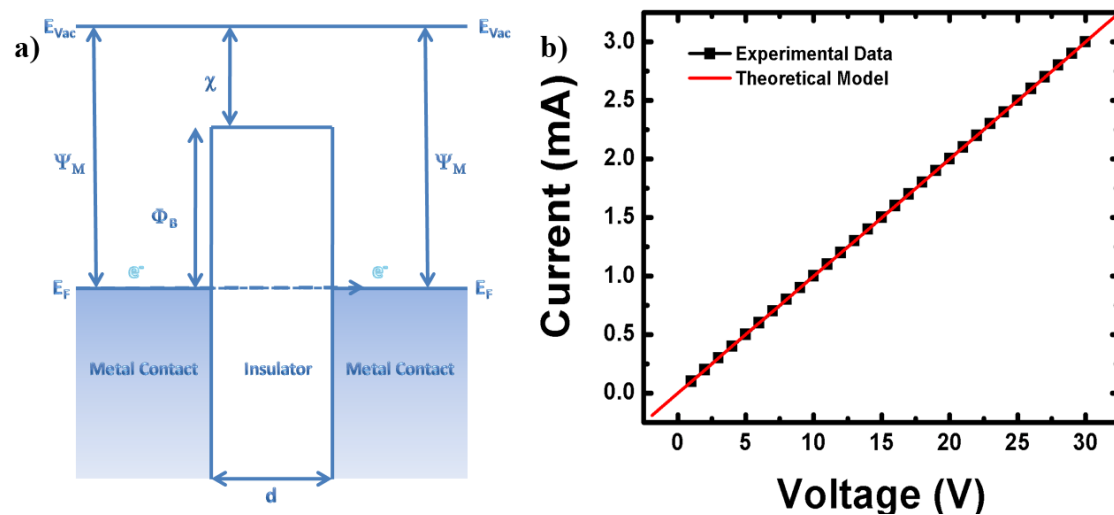


Figure 1-8 – a) Band diagram during direct tunneling, where ‘d’ is the barrier width, E_F is the metals Fermi level, E_{Vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, and Φ_B is the barrier height between the metal contact and the insulator. b) Example of fitting the direct tunneling model to experimental data.

Fowler-Nordheim Tunneling

Fowler-Nordheim tunneling, similar to direct tunneling, is a quantum mechanical effect in which electrons from the Fermi level of a metal contact tunnel through the barrier formed by the interfaces of an insulator and metal layers. Unlike direct tunneling, electrons tunnel through a triangular barrier resulting from applying large voltage. Figure 1-9a schematically depicts the band diagram without an applied voltage and Figure 1-9b with a large applied voltage. In Figure 1-9a and b, ‘d’ is the barrier width before band bending, E_F is the Fermi level of metals, E_{Vac} is the

vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, and Φ_B is the barrier height between the metal contact and the insulator. The large applied voltage bends the bands significantly such that the barrier width that the electron sees is thinner, allowing electrons to tunnel from the Fermi level of the metal contact. Without the bias to bend the bands, as is the case in Figure 1-9a, the barrier width is too large for significant number of electron to tunnel through. A mathematical description can be derived, similar to the method for direct tunneling, by solving the time independent Schrödinger's equation for a triangular barrier, as opposed to the square barrier used for direct tunneling. Next, using the WKB approximation in conjunction with the net flow of electrons across the barrier, one can derive the expression for the current flow across the insulator, [54-57].

$$I = \frac{q^3}{16\pi^2\hbar(q\Phi_B)} V^2 e^{-\frac{4\sqrt{2m^*}(q\Phi_B)^{\frac{3}{2}}}{3q\hbar V}} \quad (1.5)$$

Where I is the current flowing between the metal contacts, V is the applied voltage, d is the barrier width, Φ_B is the barrier height, \hbar is Planck's constant, and m^* is the effective mass of the electron. By solving Equation (1.5) for $\frac{1}{V}$, the voltage dependence can be derived.

$$\ln\left(\frac{I}{V^2}\right) \propto \frac{1}{V} \quad (1.6)$$

Based on Equation (1.5), Fowler-Nordheim tunneling is independent of temperature. Using Equation (1.6) one can fit the Fowler-Nordheim tunneling model to experimental data, by plotting the data as $\ln\left(\frac{I}{V^2}\right)$ vs. $\frac{1}{V}$. Figure 1-9c depicts an example of an experimental data

fitting to the theoretical model. Due to the linear relationship of Equation(1.6), a straight line can be fitted to the data.

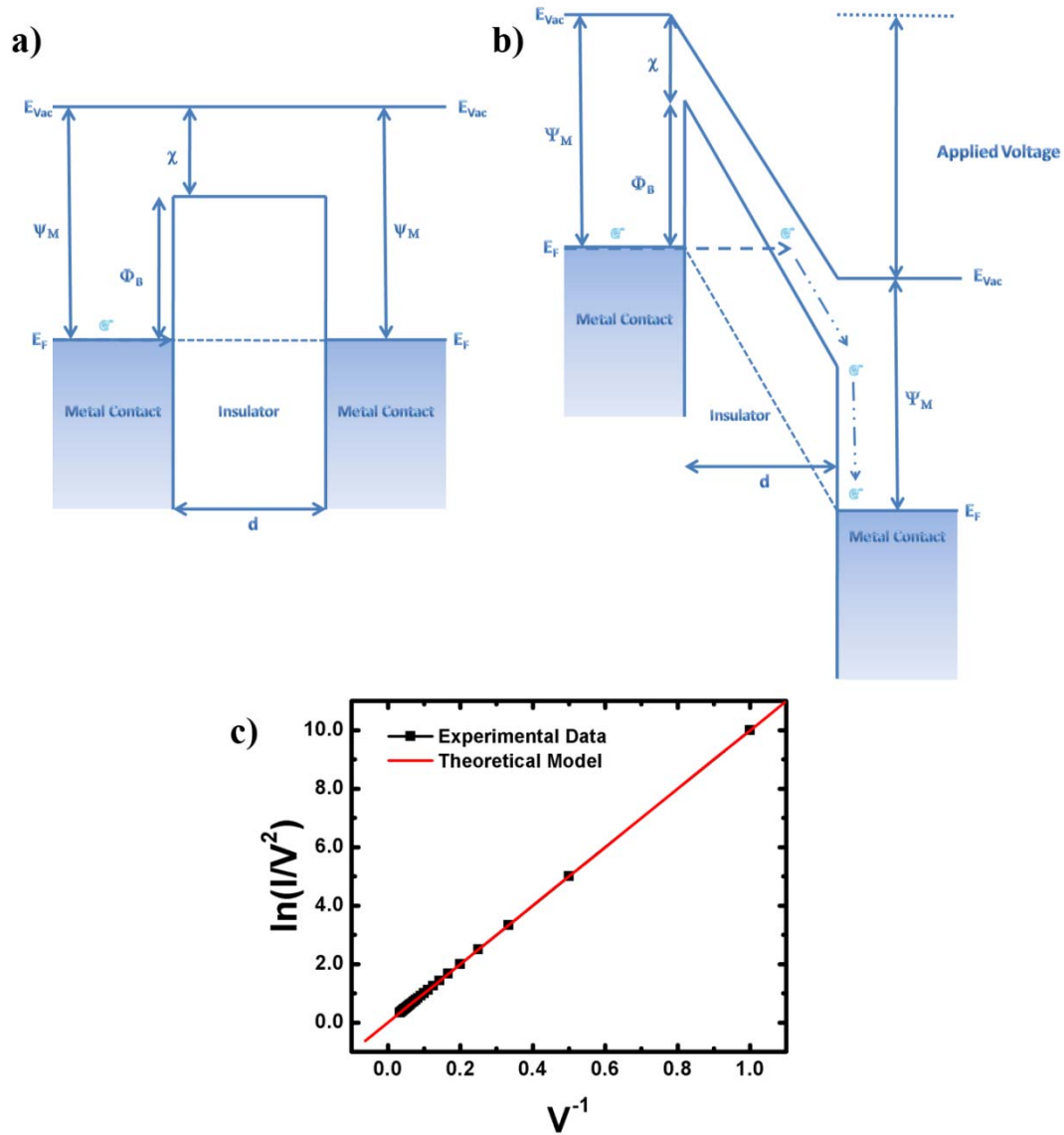


Figure 1-9 – a) Band diagram without bias, where ‘d’ is the barrier width, E_F is the metals Fermi level, E_{Vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, and Φ_B is the barrier height between the metal contact and the insulator. b) Band diagram with a large bias, causing significant bending of the bands near the positive biased contact. The reduced barrier width allows for Fowler-Nordheim tunneling to occur. c) Example of fitting the Fowler-Nordheim tunneling model to experimental data.

Thermionic Emission

Thermionic emission involves exciting electrons to higher energies in a metal contact, allowing them to overcome the potential barrier between the metal contact and an insulator. Unlike direct or Fowler-Nordheim tunneling, the electrons require thermal excitation (through interaction with phonons) to overcome the barrier. Figure 1-10a schematically depicts the band diagram during thermionic emission. In Figure 1-10a, 'd' is the barrier width before band bending, E_F is the Fermi level of metals, E_{vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, and Φ_B is the barrier height between the metal contact and the insulator. A mathematical description can be derived by first considering emission into vacuum with zero bias and assuming that the thermionic emission is thermodynamically equivalent to the evaporation of a monotonic gas. Thus, one can start off using the equation for heat of evaporation based on the second law of thermodynamics. [58]

$$L = RT^2 \frac{d \log(p)}{dT} \quad (1.7)$$

Where L is the heat of evaporation, T is the temperature, p is the vapor pressure, and R is the gas constant. Using the kinetic theory of gasses, the number of electrons striking the metal contact interface is calculated by Equation (1.8). [58]

$$n = \frac{p}{\sqrt{2\pi m k_B T}} \quad (1.8)$$

Where n is the number of electrons, p is the vapor pressure, m is the mass of an electron, k_B is the Boltzmann constant, and T is the temperature. Therefore, the current emitted is described by Equation (1.9). [58-61]

$$I = \frac{qm}{2\pi^2\hbar^3} (k_B T)^2 e^{\frac{-\Phi_B}{k_B T}} \quad (1.9)$$

Where I is the current flowing out of the metal, q is the fundamental charge, \hbar is Plank's constant divided by 2π , and Φ_B is the barrier height. Equation (1.9) is for emission into a vacuum, to describe emission through an insulator the mass of the electron in Equation (1.9) must be change to an effective mass m^* , giving: [60]

$$I = \frac{qm^*}{2\pi^2\hbar^3} (k_B T)^2 e^{\frac{-\Phi_B}{k_B T}} \quad (1.10)$$

When a bias is applied between the metal contacts, Equation (1.10) becomes: [60, 61]

$$I = \frac{qm^*}{2\pi^2\hbar^3} (k_B T)^2 e^{\frac{-\Phi_B}{k_B T}} e^{\frac{q\sqrt{\frac{qV}{4\pi\epsilon d}}}{k_B T}} \quad (1.11)$$

Where I is the current flowing between the metal contacts, V is the applied voltage, d is the barrier width, Φ_B is the barrier height, \hbar is Planck's constant, m^* is the effective mass of the electron, k_B is Boltzmann constant, q is the fundamental charge of an electron, and T is the temperature. By solving Equation (1.11) for \sqrt{V} , the voltage dependence can be derived. [61]

$$\ln(I) \propto C_1 \sqrt{V} - C_2 \quad (1.12)$$

Equation (1.11) can also be solved for $\frac{1}{T}$ giving Equation (1.13), the temperature dependence of Thermionic emission. [61]

$$\ln\left(\frac{I}{T^2}\right) \propto \frac{1}{T} \quad (1.13)$$

Using Equations (1.12) and (1.13) one can fit the Thermionic emission model to experimental data, by plotting the data as $\ln(I)$ vs. \sqrt{V} and $\ln\left(\frac{I}{T^2}\right)$ vs. $\frac{1}{T}$. Figure 1-10b and c depict an example of fitting experimental current vs. voltage and temperature data to the theoretical model. Due to the linear relationship of Equations (1.12) and (1.13), a straight line can be fitted to both types of data.

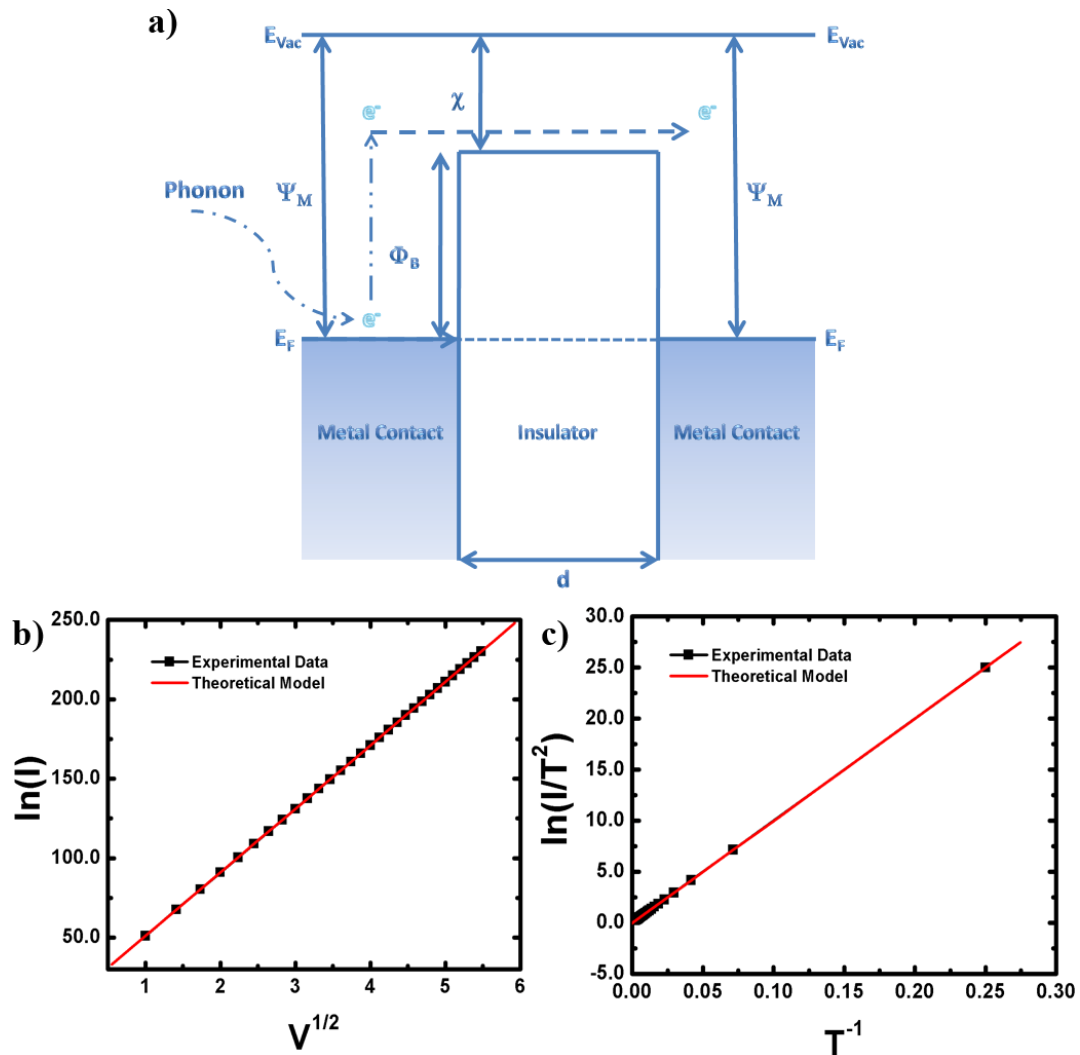


Figure 1-10 – a) Band diagram without bias, where ‘d’ is the barrier width, E_F is the metals Fermi level, E_{Vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, and Φ_B is the barrier height between the metal contact and the insulator. b) Example of fitting the Thermionic emission model to experimental data for current vs. voltage. c) Example of fitting the Thermionic emission model to experimental data for current vs. temperature.

Schottky Emission

Schottky emission is similar to Thermionic emission in that electrons are thermally excited to energies greater than the barrier. Unlike in Thermionic emission, band bending allows for lower energy electrons to overcome the potential barrier. The enhanced band bending is due to electrostatic forces at the interface of the metal contact and the insulator, this concept is known as image force. Figure 1-11a schematically depicts an image force case. When a point charge is placed close (at a distance of x) to an infinite conducting flat sheet, it induces a potential on the surface of the sheet, as in Figure 1-11a(i). The induced charge is equivalent to a point charge with an opposite charge at an equal distance ($-x$) as the original point charge. In the metal insulator interface case, the original point charge is an electron emitted from the contact into the insulator (located at a distance x for the interface) and induces a potential on the interface. This potential is equivalent to a hole at distance $-x$ from the interface, as in Figure 1-11a(ii). The force exerted on the electron can be found by using Coulomb's law and taking the distance as twice the distance of the electron and the interface [62-64].

$$F(x) = \frac{q^2}{4\pi\epsilon(2x)^2} \quad (1.14)$$

Where $F(x)$ is the force on the electron with respect to distance, x is the distance from the electron to the interface, $\epsilon = \epsilon_0\epsilon_r$ is the dielectric constant of the insulator, and q is the fundamental charge of an electron. By integrating Equation (1.14), the electron's potential as a function of distance can be found [62-64].

$$V_{\text{image}}(x) = -\frac{q^2}{16\pi\epsilon x + \frac{q^2}{\Psi_M}} \quad (1.15)$$

Where Ψ_M is the metal's work function. Combining Equation (1.15) with the potential from an applied field, the total potential of the electron, V_M , can be found [62-64].

$$V_M = -\frac{q}{2} \sqrt{\frac{qE}{\pi\epsilon}} \quad (1.16)$$

The potential V_M reduces the barrier height formed between the metal contact and insulator, creating an effective barrier height Φ_{eff} : [62-64]

$$\Phi_{\text{eff}} = \Phi_B - \frac{q}{2} \sqrt{\frac{qE}{\pi\epsilon}} \quad (1.17)$$

The resulting band diagram is depicted in Figure 1-11b, 'd' is the barrier width before band bending, E_F is the Fermi level of metals, E_{vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, Φ_B is the barrier height between the metal contact and the insulator, Φ_{eff} is the effective barrier height from the potential V_M resulting from the image force and applied voltage, and V_{image} is the potential of an electron due to the image force. A mathematical description of Schottky emission can be derived by considering number density of electrons with enough energy to overcome the effective barrier in the x-direction. [62-64]

$$N(v)dv = \frac{2m^{*2}}{\hbar^3} \frac{d\vec{v}}{1 + e^{\frac{E_{KE} - E_F}{k_B T}}} \quad (1.18)$$

Where $N(v)dv$ is the number density, m^* is the effective mass of an electron, \hbar is Plank's constant divided by 2π , k_B is Boltzmann's constant, E_F is the Fermi energy of the metal, and E_{KE} is the kinetic energy of electrons with velocity \vec{v} . Using the fact that insulators have wide band gaps, we can simplify Equation (1.18): [62-64]

$$N(v)d\vec{v} = \frac{2m^{*2}}{\hbar^3} e^{\frac{E_{KE}-E_F}{k_B T}} d\vec{v} \quad (1.19)$$

By intergrading Equation (1.19), an equation for current from Schottky emission can be found. [62-64]

$$I = \frac{4\pi q m^*}{\hbar^3} (k_B T)^2 e^{\frac{-\Phi_{eff}}{k_B T}} e^{\frac{q\sqrt{4\pi\epsilon d V}}{k_B T}} \quad (1.20)$$

Where I is the current flowing between the metal contacts, V is the applied voltage, d is the barrier width, Φ_{eff} is the barrier height, \hbar is Planck's constant, m^* is the effective mass of the electron, k_B is Boltzmann constant, q is the fundamental charge of an electron, and T is the temperature. By solving Equation (1.20) for $V^{\frac{1}{2}}$, the voltage dependence can be derived, as in Equation (1.21).

$$\ln(I) \propto \sqrt{V} \quad (1.21)$$

Equation (1.20) can also be solved for $\frac{1}{T}$ giving Equation (1.22), the temperature dependence of Schottky emission.

$$\ln\left(\frac{I}{T^2}\right) \propto \frac{1}{T} \quad (1.22)$$

Using Equations (1.21) and (1.22) one can fit the Schottky emission model to experimental data, by plotting the data as $\ln(I)$ vs. \sqrt{V} and $\ln\left(\frac{I}{T^2}\right)$ vs. $\frac{1}{T}$. Figure 1-11c and d depict an example of fitting experimental current vs. voltage and temperature data to the theoretical model. Due to the linear relationship of Equations (1.21) and (1.22), a straight line can be fitted to both types of data.

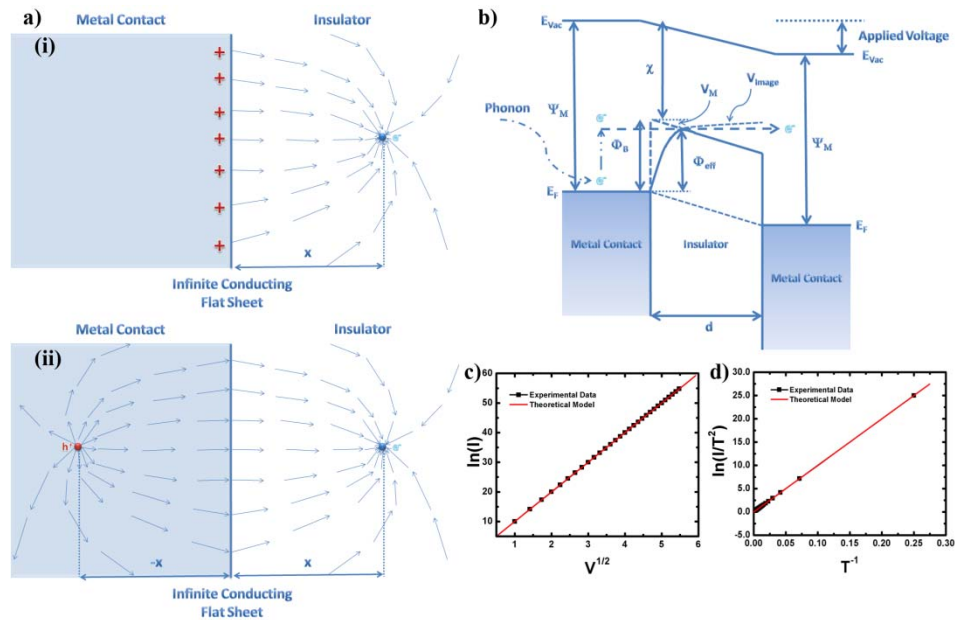


Figure 1-11 – a) (i) An electron as a point charge placed distance x from the interface of the metal contact and insulator. The interface acts as an infinite conducting flat sheet. An induced distribution of charge develops on the interface. **(ii)** The induced charge distribution is equivalent to a hole at a distance of $-x$ from the interface. **b)** Band diagram with bias, where ' d ' is the barrier width, E_F is the metals Fermi level, E_{vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, Φ_B is the barrier height between the metal contact and the insulator, Φ_{eff} is the effective barrier height from the potential V_M resulting from the image force and applied voltage, and V_{Image} is the potential of an electron due to the image force. **c)** Example of fitting the Schottky emission model to experimental data for current vs. voltage. **d)** Example of fitting the Schottky emission model to experimental data for current vs. temperature.

Poole-Frenkel

Poole-Frenkel conduction is similar to Schottky emission in that electrons are thermally excited to higher energies to conduct. Schottky emission relied on thermally exciting electrons in the metal to overcome a lowered potential barrier, due to both an image force and an applied voltage. Poole-Frenkel instead relies on thermally exciting electrons in traps or donors inside the insulator's conduction band instead of the metal contact. Unlike Schottky emission, the barrier is lowered by the positively charged traps induced by exciting electrons and not by the image force. The force exerted on the electron can be found by using Coulomb's law.[62, 65]

$$F(x) = \frac{q^2}{4\pi\epsilon r^2} \quad (1.23)$$

Where $F(x)$ is the force on the electron with respect to distance, r is the distance from the electron to the trap or donor, ϵ is the dielectric constant of the insulator, and q is the fundamental charge of an electron. By integrating Equation (1.23), the electron's potential as a function of distance can be found.[62, 65]

$$V(r) = -\frac{q^2}{4\pi\epsilon r} \quad (1.24)$$

Combining Equation (1.24) with the potential from an applied field, the total potential of the electron, V_M can be found.[62, 65]

$$V_M = -2\sqrt{\frac{q^3 E}{4\pi\epsilon}} \quad (1.25)$$

The potential V_M reduces the barrier height as seen by an electron in the trap or donor level.

The resulting band diagram is depicted in Figure 1-12a, 'd' is the barrier width before band

bending, E_F is the Fermi level of metals, E_{vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, Φ_B is the barrier height between the metal contact and the insulator, and V_M is the reducing potential from the Coulombic force of the trap or donor site and the applied voltage. A mathematical description of the Poole-Frenkel mechanism can be derived by assuming that no thermally generated free electrons can exist in the conduction band since the band gap of an insulator is significantly larger than $k_B T$. Instead, only electron excited from a trap or donor site can occupy the conduction band. Therefore, the number density of electrons in the conduction band can be described by Equation (1.26).[62]

$$n_c = N_t - n_t \quad (1.26)$$

Where n_c is the number density, N_t is the number density of traps or donor sites, n_t and is the number density of occupied sites. By using the fact that the rate of electrons thermally excited from the trap or donor sites must equal the rate of the sites being filled and the Equation for conductivity $\sigma = n_c e \mu$, the conductivity of the insulator can be derived as: [62, 63, 65]

$$\sigma = \sqrt{N_{eff}} \sqrt{N_t} q \mu e^{\frac{E_t}{2k_B T}} e^{\frac{\sqrt{q^3 V}}{k_B T}} \quad (1.27)$$

Where σ is the conductivity of the insulator during an applied voltage, V is the applied voltage, N_{eff} is the effective density of states in the conduction band, N_t is the number density of traps or donors, μ is the mobility, E_t is the energy level of the traps or donors, ε is the dielectric constant of the insulator, k_B is Boltzmann constant, q is the fundamental charge of an electron,

and T is the temperature. Equation (1.11) can be multiplied by the applied voltage (Ohm's law: $I = \sigma V$) to derive the Poole-Frenkel equation for current.

$$I = V\sigma = V\sqrt{N_{eff}}\sqrt{N_D}q\mu e^{\frac{E_t}{2k_B T}} e^{\frac{\sqrt{q^3 V}}{\sqrt{4\pi\epsilon}} \frac{1}{k_B T}} \quad (1.28)$$

By solving Equation (1.28) for \sqrt{V} , the voltage dependence can be derived.

$$\ln\left(\frac{I}{V}\right) \propto \sqrt{V} \quad (1.29)$$

Equation (1.28) can also be solved for $\frac{1}{T}$ giving the temperature dependence of the Poole-Frenkel mechanism.

$$\ln\left(\frac{I}{V}\right) \propto \frac{1}{T} \quad (1.30)$$

Using Equations (1.29) and (1.30) one can fit the Poole-Frenkel model to experimental data, by plotting the data as $\ln\left(\frac{I}{V}\right)$ vs. \sqrt{V} and $\ln\left(\frac{I}{V}\right)$ vs. $\frac{1}{T}$. Figure 1-12b and c depict an example of fitting experimental current vs. voltage and temperature data to the theoretical model. Due to the linear relationship of Equations (1.29) and (1.30), a straight line can be fitted for both types of data.

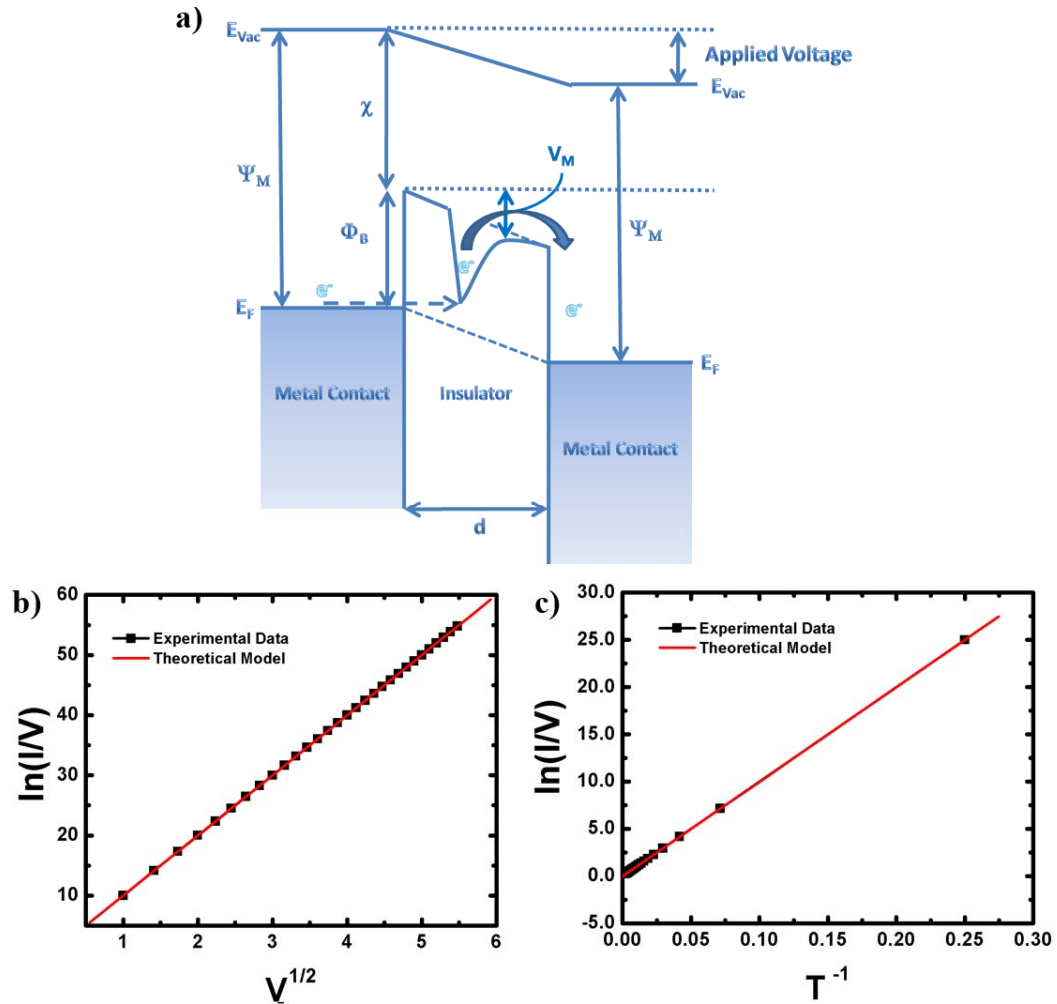


Figure 1-12 – a) Band diagram with bias, where ‘d’ is the barrier width, E_F is the metals Fermi level, E_{Vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, Φ_B is the barrier height between the metal contact and the insulator, V_M reducing potential of the trap’s barrier. V_M results from the coulombic force associated with the positive trap after a n electron jump. b) Example of fitting the Poole-Frenkel model to experimental data for current vs. voltage. c) Example of fitting the Poole-Frenkel model to experimental data for current vs. temperature.

Variable-Range Hopping

Variable-range hopping involves thermally assisted transfer of electrons between localized states. The transfer can occur via absorption of a phonon, allowing the electron to overcome the energy difference in the states, or through quantum mechanical tunneling

between states with equal energy. Figure 1-13a schematically depicts the band diagram during thermionic emission. In Figure 1-13a, 'd' is the barrier width before band bending, E_F is the Fermi level of metals, E_{vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, and Φ_B is the barrier height between the metal contact and the insulator. A mathematical description of the variable-range hopping can be derived by combining the probability of the two individual events occurring. For thermal excitation to an unoccupied site the probability will be governed by Equation (1.31). [62, 66, 67]

$$P_{Therm} \propto e^{-\frac{\Delta E}{k_B T}} \quad (1.31)$$

Where P_{Therm} is the probability that an electron will be thermally excited from one state to another, ΔE is the energy difference between the two states, k_B is Boltzmann's constant, and T is the temperature. ΔE can be determined as a function of the distance between the states R and the density of state near the Fermi level, N_F . [62, 66, 67]

$$\Delta E = \frac{3}{4\pi N_F R^3} \quad (1.32)$$

The probability for tunneling between sites separated by a distance R is: [62, 66, 67]

$$P_{Tun} \propto e^{-2\alpha R} \quad (1.33)$$

Where P_{Tun} is the tunneling probability, R is the distance and α is the inverse localization length. By combining Equations (1.31) to (1.33) the conductance σ can be found. [62, 66-68]

$$\sigma \propto e^{-\frac{2\alpha R}{4\pi N_F R^3 k_B T}} \quad (1.34)$$

Both tunneling and thermal excitation processes are competing, thus an optimum range must be present and can be found by maximizing Equation (1.34). [62, 66-68]

$$\sigma = Ae^{-\left(\frac{B}{T^{1+d}}\right)} \quad (1.35)$$

Where A is a proportionality constant, d is the number of dimensions, and where: [62, 66-68]

$$B = \frac{4\Delta E}{k_B T^{\frac{3}{4}}} \quad (1.36)$$

Using Ohm's law, $I = \sigma V$, the equation for the current in variable-range hopping is:

$$I = V\sigma = VAe^{-\left(\frac{B}{T^{1+d}}\right)} \quad (1.37)$$

By solving Equation (1.37) for V , the voltage dependence can be derived, as in Equation (1.38).

$$I \propto V \quad (1.38)$$

Equation (1.28) can also be solved for $\frac{1}{T^{1+d}}$, where d is the number of dimensions, giving the

temperature dependence of the variable-range hopping model.

$$\ln\left(\frac{I}{V}\right) \propto \frac{1}{T^{1+d}} \quad (1.39)$$

Using Equations (1.38) and (1.39) one can fit the variable-range hopping model to experimental

data, by plotting the data as I vs. V and $\ln\left(\frac{I}{V}\right)$ vs. $\frac{1}{T^{1+d}}$.

Figure 1-13b and c depict examples of fitting experimental current vs. voltage and temperature data for three dimensions to the theoretical model. Due to the linear relationship of Equations (1.38) and (1.39), a straight line can be fitted for both types of data.

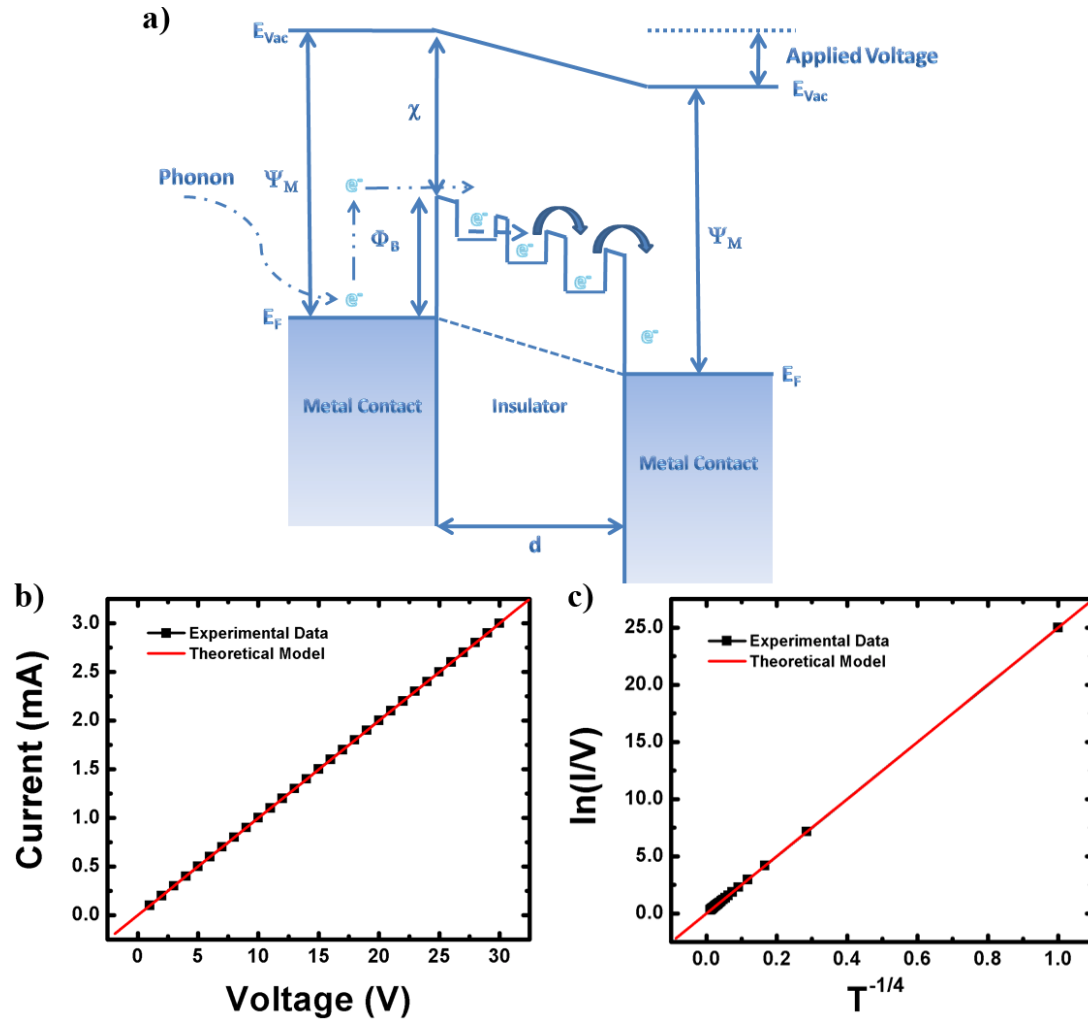


Figure 1-13 – a) Band diagram with bias, where ‘ d ’ is the barrier width, E_F is the metals Fermi level, E_{Vac} is the vacuum level, Ψ_M is the work function of the metal, χ is the electron affinity of the insulator, and Φ_B is the barrier height between the metal contact and the insulator. b) Example of fitting the variable-range hopping model to experimental data for current vs. voltage. c) Example of fitting the variable-range hopping model to experimental data for current vs. temperature for three dimensions.

Summary of Conduction Mechanisms

Table 1.2 summarizes all six conduction mechanisms and their voltage and temperature dependences. Both tunneling processes rely on quantum tunneling. However, the high voltages associated with Fowler-Nordheim tunneling create a triangular shape barrier. As a result, the distance for the carrier from the Fermi energy of the metal electrode to tunnel is effectively reduced, increasing the current as compared to direct tunneling. The thermal emission process is temperature dependent and relies on thermal energy for the carriers to overcome the barrier. Schottky emission allows the carriers to be transported by lowering the potential barrier by both an image force and application of an external electric field, allowing carriers with lower thermal energies to conduct. Poole-Frenkel emission occurs by thermally exciting carriers from traps located within the barrier, which are populated via tunneling (from the Fermi level of the metal contact) through a lowered potential barrier due to image forces and applied electric fields. Variable-range hopping occurs across the barrier by thermally assisted transport from one trap to the next through the barrier. By measuring the I-V characteristics of memory devices and fitting the curves with the six mechanisms allows an understanding of the charge transport through organic materials. Determination of the appropriate conduction mechanism makes it easier to optimize the structure and performance of memory devices. Indeed, we have applied a combination of models summarized in Table 1.2 to describe the charge transport in our memory devices.

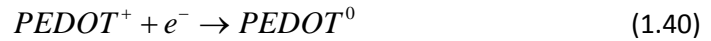
Table 1.2 – Temperature and voltage dependences of some of the conduction mechanisms in organic materials.

| Conduction Mechanism | Characteristic Behavior | Temperature Dependence | Voltage Dependence |
|------------------------------------|---|---|---|
| Direct Tunneling (Low Bias) | $I = V \frac{q^2 \sqrt{2mq\Phi_B}}{4\pi\hbar^2 d} e^{\frac{-2d}{\hbar} \sqrt{2mq\Phi_B}}$ | None | $I \propto V$ |
| Fowler-Nordheim Tunneling | $I = \frac{q^3}{16\pi^2 \hbar (q\Phi_B)} V^2 e^{\frac{4\sqrt{2m^*} (q\Phi_B)^{3/2}}{3qhV}}$ | None | $\ln\left(\frac{I}{V^2}\right) \propto \frac{1}{V}$ |
| Thermionic Emission | $I = \frac{qm^*}{2\pi^2 \hbar^3} (k_B T)^2 e^{\frac{-\Phi_B}{k_B T}} e^{\frac{q\sqrt{\frac{qV}{4\pi\epsilon d}}}{k_B T}}$ | $\ln\left(\frac{I}{T^2}\right) \propto \frac{1}{T}$ | $\ln(I) \propto C_1 V^{1/2} - C_2$ |
| Schottky Emission | $I = \frac{4\pi qm^*}{\hbar^3} (k_B T)^2 e^{\frac{-\Phi_{eff}}{k_B T}} e^{\frac{q\sqrt{\frac{qV}{4\pi\epsilon d}}}{k_B T}}$ | $\ln\left(\frac{I}{T^2}\right) \propto \frac{1}{T}$ | $\ln(I) \propto V^{1/2}$ |
| Poole-Frenkel Emission | $I = V \sqrt{N_{eff}} \sqrt{N_D} q \mu e^{\frac{E_t}{2k_B T}} e^{\frac{\sqrt{\frac{q^3 V}{4\pi\epsilon}}}{k_B T}}$ | $\ln\left(\frac{I}{V}\right) \propto \frac{1}{T}$ | $\ln\left(\frac{I}{V}\right) \propto V^{1/2}$ |
| Hopping Conduction | $I = V A e^{-\left(\frac{B}{T^{1+d}}\right)}$ | $\ln\left(\frac{I}{V}\right) \propto \frac{1}{T}$ | $I \propto V$ |

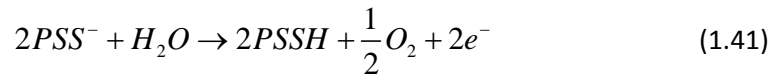
1.3.1.2 Organic Memory Mechanisms

Redox Reaction for Organic Memory Devices

Now we describe the mechanisms responsible for the memory effect in organic materials. Currently there are three types of mechanisms used to store information in organic memories. The first method developed by Möller et al and later improved by Smith et al relies on a redox reaction of the organic layer (Figure 1-14) [47, 69]. The devices consist of a 50 nm film of polyethylene dioxythiophene:polystyrene sulfonic acid (PEDOT:PSS) sandwiched between a top Au contact and an n-type Si substrate (Figure 1-14). During a high voltage pulse of 10V, injected electrons cause a reduction of the oxidized PEDOT chains.



Concurrently, the injected holes permit oxidation in the PSS⁻ chains. In addition, the PSS⁻ strands also react with water to form PSSH.



The formation of PSSH occurs due to the localized heating up to 100-200°C from high currents during the write pulses. After completion of the write pulse, the neutralized PEDOT:PSS film can no longer effectively conduct holes through the PEDOT chains giving the films significantly higher impedance, as demonstrated in Figure 1-14. The current at 1.5V is five orders of magnitude larger before the 10V write pulse. With the PSSH and oxidized PSS chains, the reduced PEDOT⁰ chains cannot re-oxidize back to PEDOT⁺, making the physical changes in the PEDOT:PSS layer permanent. Thus the device can be written once but read many times, hence the name Write-Once-Read-Many times (WORM). [47, 69, 70]

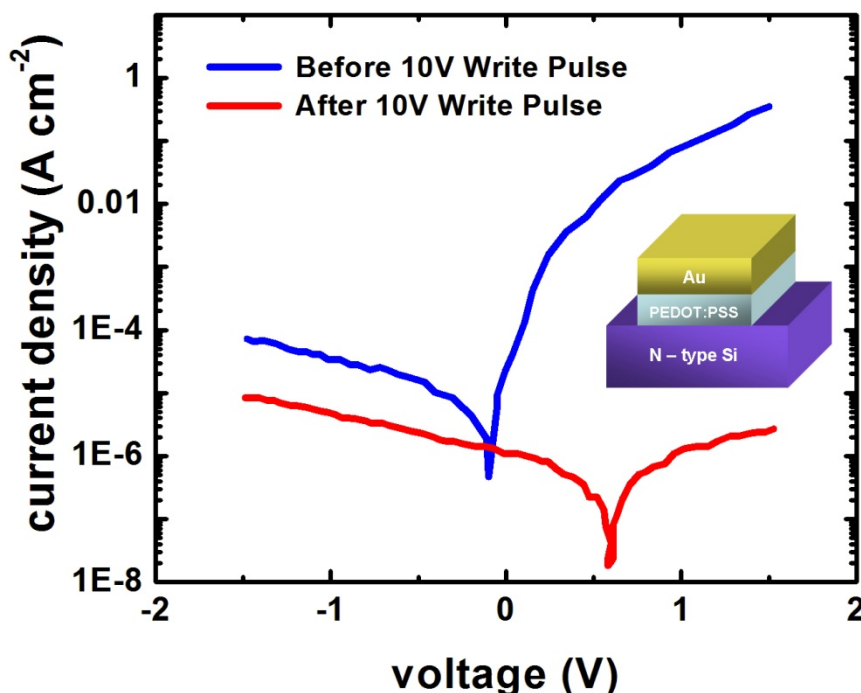


Figure 1-14 – WORM device reported by Möller *et al* [47] and Smith *et al* [69]. The PEDOT:PSS acts as a polymer fuse by developing a larger resistance after a 10V write pulse. Schematic of device shown in insert. [69].

Charge Storage for Organic Memory Devices

The second type of mechanism, on which some organic memory devices are based on, is charge storage. This mechanism relies on stored charges screening out the applied voltage, resulting in a higher impedance state as compared to the neutral state. The mechanism was first developed and proposed by Simmons and Verderber [71] for an inorganic Metal-Insulator-Metal (MIM) devices. The original MIM devices consisted of SiO₂ sandwiched between two Al contacts. Charges were stored in traps in the SiO₂ layer, which were created during the fabrication process [71]. This model, extrapolated to organic memory devices by Bozano *et al* (Figure 1-15) consists of a triple layer system with a discontinuous 5nm film of Al (nanoparticles) sandwiched between 50 nm layers of aluminum tris(8-hydroxyquinoline) (Alq₃), with Al

electrodes. Typical I-V curves of such a device are shown in Figure 1-15 in which it can be seen that the device is initially in the low impedance (ON state) state as the voltage is applied up to 6V (blue curve in Figure 1-15). Between 3 and 6V, the current exhibits negative differential resistance (NDR). Due to the fact that as the carriers generated by the applied voltage, charges become trapped in the 5nm Al film. As the voltage is swept down, the trapped carriers remain in the discontinuous Al film of nanoparticles as long as the voltage sweep is sufficiently fast. Thus, the downward sweep follows the red curve in Figure 1-15, operating in a high impedance state (OFF state). The stored charges in the Al layer generate an opposing electrical field that screens the applied field. The resulting field across the Al layer can be calculated by first deriving the induced electric field across the interfaces of the discontinues Al and Alq₃ as: [71]

$$E = \frac{-Q_0}{\varepsilon} \quad (1.42)$$

Where E is the electric field, Q_0 is the induced charge at the interface between the Al and Alq₃, and ε is the dielectric constant of Alq₃. Thus the new screened field will be the based on the sum of the original induced charges and the stored charges. [71]

$$E^* = \frac{-(Q_0 - eN_s)}{\varepsilon} \quad (1.43)$$

Where E^* is the new electric field, e is the fundamental charge, and N_s is the number of stored charges. Based on Equation (1.43), the resulting electric field and hence the voltage drop across the Al film will be reduced (even during an applied voltage), producing the high impedance state. If the voltage is raised to 3V, the stored charges are able to tunnel out and bring the device back to its low impedance state. The device will remain in the low impedance state as long as the voltage reduced slowly, allowing enough time to prevent any new charges

from being trapped. The presence of the hysteresis provides the opportunity to perform memory operations by charging and discharging nanoparticles in the Al layer. [44, 71]

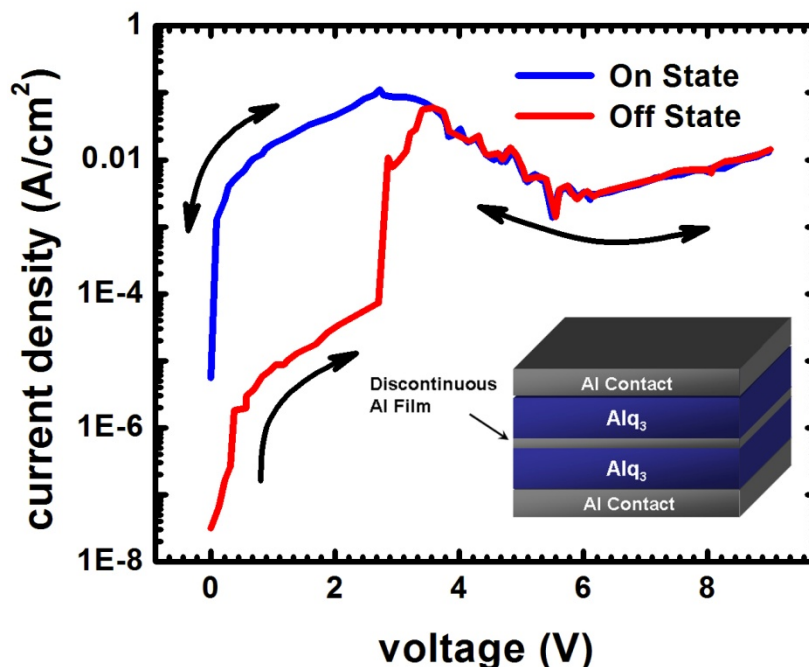


Figure 1-15 – Organic memory device using charge storage. The device uses a triple layer of 50nm of Alq₃ and 5nm of Al. Writing occurs at 6V in the NDR regime, allowing the Al film to store charges. Erasing occurs with an application of 3V, allowing the stored charges to tunnel out. Schematic of device shown in the insert. [44]

Charge Transfer for Organic Memory Devices

The third mechanism similar to charge storage is charge transfer utilized in memory devices. The difference being that, the stored electrons do not originate from the contacts, but are transferred from a donor within the device. This results in partially filled Highest Occupied Molecular Orbital (HOMO), analogous to the valence bands for inorganic semiconductors, in the organic donors. The impedance of the device therefore is reduced by allowing more carriers to conduct through the unfilled HOMO level. In the absence of an external field, the transferred electrons are stored and cannot escape, as the acceptors are surrounded by an insulator. The

application of a negative voltage transfers the electrons back to the donors and restores the high impedance state [72-74]. Yang Yang and his group at UCLA have done significant work in this area and were the first to demonstrate an organic device utilizing the charge transfer mechanism (Figure 1-16a)[42, 43, 48, 50, 51, 72-77]. The device consists of a blend of Polystyrene, 8-hydroxyquinoline (8HQ), and 1-dodecanethiol-protected gold nanoparticles (Au-DT NPs), sandwiched between two Al contacts. As a voltage is applied, the device remains in the OFF state until a threshold is reached when the electrons from the 8HQ (organic donor) can tunnel into the Au-DT nanoparticles (Figure 1-16b). The band diagram is shown in Figure 1-16 b(ii), where 'd' is the barrier width, E_F is the gold nanoparticle's Fermi level, E_{vac} is the vacuum level, Ψ_M is the work function of the gold, and Φ_B is the barrier height between the gold and the DT. The LUMO (Lowest unoccupied Molecular Level) is analogous to the conduction bands for inorganic semiconductors. The donated electrons leave vacancies in the HOMO of the 8HQ, reducing the impedance of the device. The device can then be returned to the high impedance state by applying a negative voltage to remove the electrons from Au -DT NPs and transfer them back to the 8HQ, thus refilling the HOMO levels [50].

a)

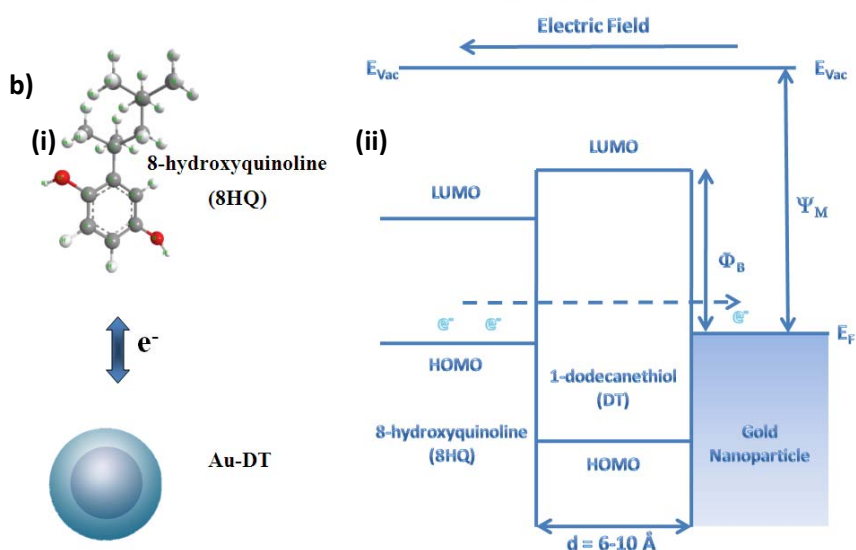
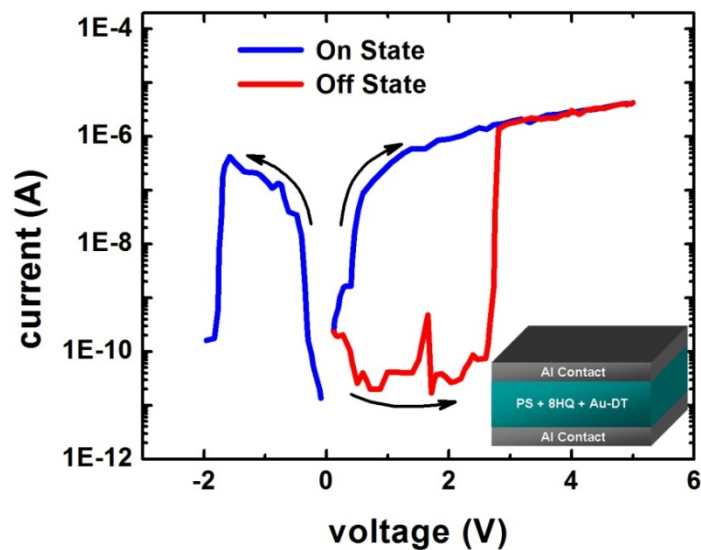


Figure 1-16 – a) Organic memory device using charge transfer. The device uses 8-hydroxyquinoline (8HQ) as the electron donor and 1-dodecanethiol-protected gold Nanoparticles (Au-DT NPs) as the acceptor. Polystyrene (PS) is used a host material. Writing occurs at 2.83V by transfer electron from 8HQ to Au-DT NPs. Erasing occur with an application of -1.8V, transferring the electrons back to the 8HQ. Schematic of device shown in insert. b) (i) Electron transfer between 8HQ molecules and the nano sized gold particles, coated with 1-dodconethiol. (ii) Band diagram of the charge transfer, where 'd' is the barrier width, E_F is the gold nanoparticle's Fermi level, E_{Vac} is the vacuum level, Ψ_M is the work function of the gold, and Φ_B is the barrier height between the gold and the DT. With a strong enough electric field electrons from the HOMO level of the 8HQ can tunnel through the DT and transfer to the gold nanoparticle. When the field is removed the charges become trapped, leaving the HOMO level free to conduct holes between network of 8HQ molecules in the device.[50]

1.4 Objective of Work

The objective of this thesis is to fabricate and understand the charge transport in an all-organic memory device that combines the advantages of molecular and organic electronics. Specifically, non-volatile memory devices using C_{60} fullerene molecules dispersed in an insulating polymer. C_{60} molecules are chosen over inorganic nano-particles such as Au because of the low synthesis costs of C_{60} and its precise diameter (0.72nm). Inorganic nano-particles generally cost significantly more to synthesize and vary in size, requiring additional processing to narrow the size distribution. The C_{60} polymer memory devices exhibit high and low conductance states, rapid switching, low power consumption, long term cycling stability and data retention. The devices can be fabricated at room temperature using spin coating, thus are easily scalable for mass production. Our aim is to perform preliminary investigation of the fundamental mechanisms, which will provide insight into the development of new device structures that may bring the organic memory technology closer to market.

1.5 Materials

The all-organic memory system being developed in this system relies on a charge storage mechanism. The basic design is a dispersion of organic molecules for storing the charges, within a host polymer. C_{60} is chosen for the organic storage molecules. The host polymer used is poly (4 vinyl phenol) (PVP). In addition, polystyrene (PS) is also analyzed as a capping layer, which will be described in chapter 3. Hence, a brief description and background of these materials is presented here.

1.5.1 C₆₀

C₆₀ is a closed caged molecule belonging to a class of carbon materials known as fullerenes. C₆₀ is composed of 12 pentagonal and 20 hexagonal faces with sixty carbon atoms located at each vertex, as depicted in Figure 1-17. It is icosahedral shaped [78], much like a soccer ball, with a precise diameter of 0.72nm. C₆₀ has a very high electron affinity (2.8eV [78-80]) making it attractive for electronic applications. The potential applications range from organic diodes[81], single-electron transistors[21, 82], superconductors[83-85], and more extensively in organic photovoltaics [86, 87]. Organic photovoltaics utilize C₆₀'s high electron affinity to transfer charge and effectively break up photogenerated excitons to generate power. The charge transfer of C₆₀ has been well studied using sub femto-second laser pulses and measured to be around 100's of femto-second [88, 89]. The high electron affinity, ultra fast charge transfer, and consistent diameter make C₆₀ ideal for use in the all-organic memory device, such as the ones thoroughly characterized in this thesis.

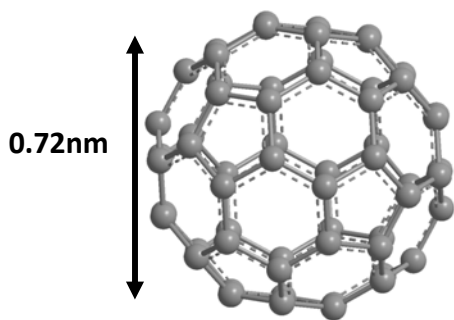


Figure 1-17 – Schematic of a C₆₀ molecule

1.5.2 Polymers

The polymers chosen for this thesis are Poly (4-vinyl phenol) (PVP) and Polystyrene (PS), both are amorphous and insulating. PVP consists of a benzene ring with a hydrogen atom replaced with an OH group and connected with a standard carbon-to-carbon backbone chain, in a atactic configuration. A schematic of its structure is shown in Figure 1-18a. PS has a similar

structure to that of PVP, with the exception of a complete benzene ring, as depicted in Figure 1-18b. PVP and PS are compatible with solution based processing, making them ideal for use in organic electronics. For example, PVP is often used for the gate insulator in organic transistors [90-97]. A solution of PVP and solvent (usually isopropanol) is spin coated onto either the semiconducting layer or a conducting gate, depending on whether the transistor is top or bottom gated. Typically, the PVP thickness ranges from 300nm to 1 μ m's to ensure very low gate leakage, which is essential to the transistors operation. PVP can also be cross-linked when mixed with a cross-linker [such as poly(melamine-coformaldehyde) (MMF)] and thermally annealed up to 200°C. When cross-linked, PVP's leakage currents significantly drop, allowing the gate insulator thickness to be scaled down to 25nm. The uncross-linked version of PVP is ideal for hosting the charge storing C₆₀ molecules. C₆₀ can co-dissolve with PVP in isopropanol allowing for solution based processing of thin films (sub 100nm thickness) of PVP and C₆₀ blends. Unlike previous organic memories, the use of C₆₀ avoids the distribution of sizes of inorganic nanoparticles while still maintaining fast charging times. In addition, by dispersing them with insulating polymers such as PVP, the use of low cost fabrication techniques can be maintained. When combined with a thin layer of PS, an all-organic memory device can be fabricated.

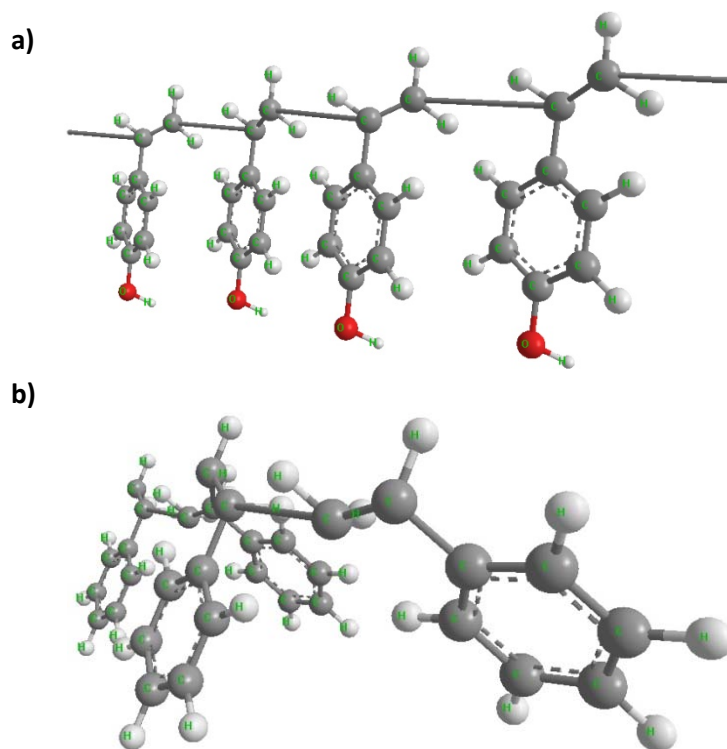


Figure 1-18 – a) Structure of PVP. Benzene rings with a hydrogen atom replaced with an OH groups are connected atactically to a standard carbon-to-carbon backbone chain. b) Structure of PS. Unlike PVP, PS has complete benzene rings.

1.6 Motivation and Outline of the Work

Organic memory devices have the potential for becoming a universal memory technology. However, before the case of organic memory devices is considered for practical application, their fundamental properties must be understood. Our motivation for understanding this research is to thoroughly investigate the structure, transport, and device characteristics of organic memory devices fabricated from C_{60} molecules incorporated into insulating polymers. Toward this end, we have carried out detailed studies of charge storage, transfer, and transport. Specifically in Chapter 2, we describe the results of electrical measurements from single layer devices consisting of C_{60} molecules embedded in PVP matrix. These simple metal-organic-metal (MOM) devices were used to model the charge storage and transport mechanism. In the single layer devices, we show that the I-V characteristics can be

fitted with a combination of conduction mechanisms depending on the voltage. Furthermore, basic memory functions along with fast switching and nanoscale operations are shown to be possible with MOM devices.

In Chapter 3, a more sophisticated multi-layer layered memory device structure is introduced in order to overcome the limitations of the single layer devices described in Chapter 2. The multi-layer devices exhibit a completely different asymmetric hysteresis in comparison to the MOM devices. Furthermore, the difference between the 'ON' and 'OFF' states is several orders of magnitude, allowing easier differentiation between the two states. Based on the device characteristics, it is also possible to extract the energy required to charge the C_{60} molecules. In this chapter, we also describe our unsuccessful efforts to transfer electrodes onto the multi-layer devices.

In Chapter 4, we report a detailed study of the conduction mechanisms in organic memory devices. Specifically, we expand on our work from Chapter 2 by incorporating measurements from different temperatures, ranging from 4K to 298K. These measurements have been correlated with the conduction mechanisms described in this Chapter. Our study reveals that tunneling from the contact into the polymer is dominant. Various measurements from single and multi-layer devices are presented in order to understand the mechanism.

In Chapter 5, the main conclusions from this work are summarized. In addition, some recommendations for future work are provided.

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Chapter 2 Single Layer Memory Devices

2.1 Introduction

In this Chapter, single layer C_{60} in insulating polymer blend devices which demonstrate a memory effect are described. Structural and electrical measurements have been carried out to help in understanding the charge storage and transport within the blend films. Here, we concentrate on single layer devices to characterize their fundamental properties. Specifically, structural characterization using Raman spectroscopy, atomic force microscopy, and scanning electron microscopy have been carried out. More importantly, detailed electrical characterization of the blends is described. The objective of this work was to understand the fundamental properties of single layer blend devices and apply the concepts to more complicated structures described later. The single layer devices exhibited symmetrical current vs. voltage (I-V) curves with a discernable hysteresis, demonstrating the potential for information storage. The symmetrical hysteresis has been translated into basic memory functions along with the demonstration of fast switching and nanoscale operations. Later in Chapter 3, the knowledge regarding charge transport, storage and transfer obtained from single layer devices will be extrapolated into more commercially viable memory technology using a multi-layer structure.

2.2 Experimental Setups

2.2.1 Structural Characterization

Structural characterization on thin films of the Poly (4-vinyl phenol) (PVP) polymer and C_{60} blends has been performed primarily using three techniques: Raman Spectroscopy, Atomic Force Microscopy (AFM), and Scanning Electron Microscopy (SEM). Raman spectroscopy was used to confirm the presence of C_{60} within the blends, and prove charge storage within the C_{60} molecules. SEM and AFM measurements provided an understanding of the thin film surface characteristics. In order to effectively interpret the results from each of these techniques, their principles of operation and application is discussed in the following sections.

2.2.1.1 Raman Spectroscopy

Raman spectroscopy is a powerful tool used to identify and characterize materials. The process involves shining a monochromatic laser onto the surface and monitoring the wavelengths of the scattered light. Figure 2-1a depicts three different scattering events that occur during illumination. The strongest type is the Rayleigh scattering which involves elastic collisions between the incident photons of the laser light and the phonons within the material. Thus, in this case, the scattered photons have the same energy as the incident photons. This elastic scattering results in a change in the dipole moment of the molecule that is infrared (IR) active but not Raman active. Stokes and Anti-Stokes scattering are inelastic events involving incident photons and phonons in the material. Unlike Rayleigh scattering, the scattered photons do not have the same energy as the incident photons. The inelastic events that result in a change in the polarizability of the molecules are Raman active. The energy level diagram for the inelastic scattering is shown in Figure 2-1b. Stokes scattering occurs when the incoming photon is absorbed by the molecules in the ground state, which excites an electron to a higher energy

virtual state. Concurrently, some electrons decay back down but into an excited vibrational state, emitting a photon with a lower energy compared to the initial photon. Anti-Stokes on the other hand involves absorption of the incoming photon by excited electrons already in a higher energy state that excites into an even higher energy virtual state and decays back down to the ground energy state. The excess energy is transferred to the emitted photon giving it higher energy than the initial photon. Based on the Boltzmann equation, the number of molecules initially in the ground state is significantly larger than in the excited state. As a result, Stokes scattering is stronger than the Anti-Stokes scattering. The resulting change in energy of the photons during either Stokes or Anti-Stokes scattering is called a Raman Shift, ν (cm^{-1}), and is calculated in wave numbers by: [1-3]

$$\nu = \frac{1}{\lambda_{\text{Incident}}} - \frac{1}{\lambda_{\text{Scattered}}} \quad (2.1)$$

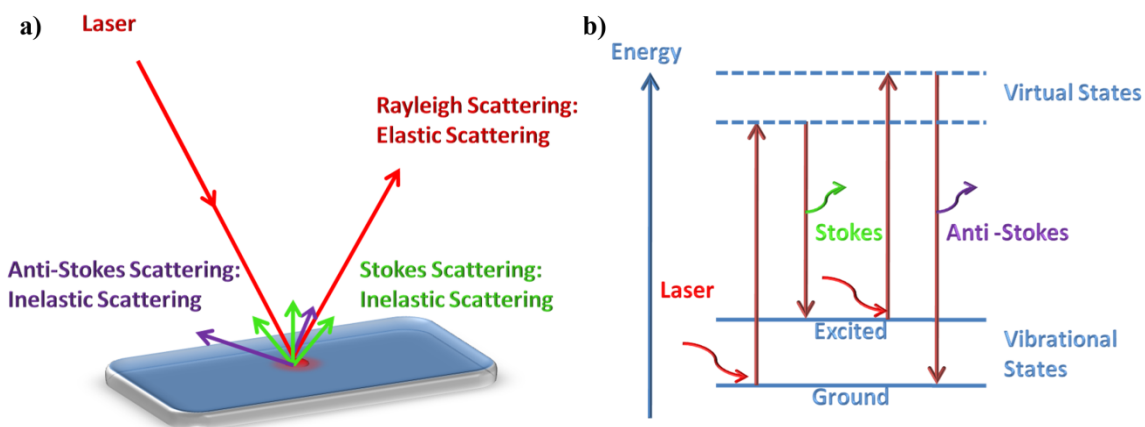


Figure 2-1 – a) Three types of scattering of an incident laser. Rayleigh scattering is an elastic form, producing photons with the same energy as the laser light. Stokes and Anti-Stokes scattering are inelastic forms of scattering, changing the scattered photon's energy as compared to the incident photon. b) Energy level diagram showing the difference between Stokes and anti-stokes scattering. Stokes produces photons with lower energy and Anti-Stokes produce photons with higher energy. [1-3]

In Raman systems, the scattered light is collected and the Rayleigh components are filtered out. A Charge Coupled Device (CCD) records the spectrum of both the Stokes and Anti-Stokes scattered light. The data is plotted as intensity vs. wave number. A typical Raman spectrum for C_{60} is shown in Figure 2-2. Specific peaks, such as the tangential A_{1g} peak (located at 1469 cm^{-1}) are fingerprints for the C_{60} molecules.

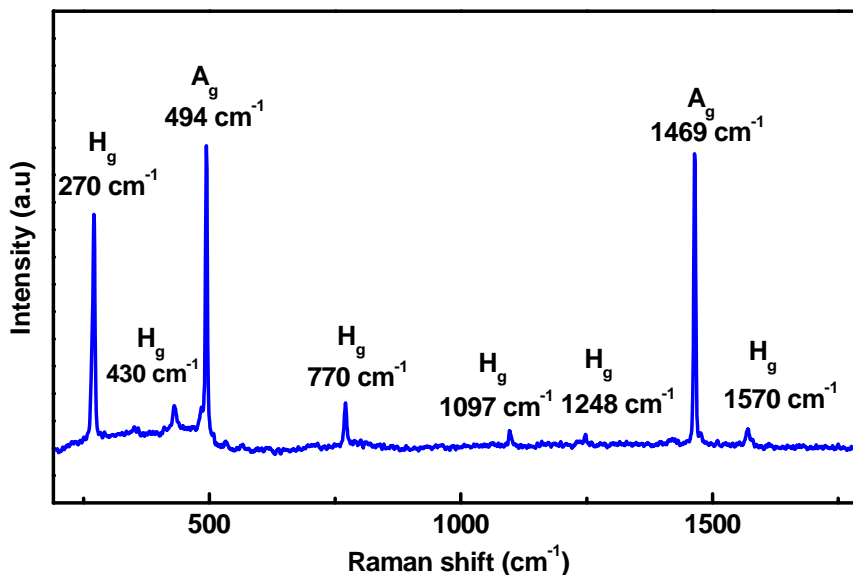


Figure 2-2 – Raman spectrum of C_{60} . The characteristic peaks are labeled. [4-6]

2.2.1.2 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is used to characterize the surface topography of various nano materials and nano devices. The basic principle behind AFM is to monitor the forces between a very sharp tip (typically made of silicon nitride with a radius in nanometers) and the surface of the sample while rastering the tip, giving a topographic image of the surface. Figure 2-3 illustrates the principles behind AFM. Typically, rastering of the tip occurs by using piezoelectric materials, such as PZT, to move the sample in 3 dimensional space. Two of the

most common modes of operation of AFM are contact and non-contact. Contact mode relies on touching the tip with the surface and dragging the tip across it. The measured deflections of the tip by the laser are used to generate an image of the surface. In addition, the deflections are used in conjunction with a feedback loop to ensure the tip remains in contact with the surface by moving the sample by an appropriate amount in the z-direction. The physical contact with the surface wears down the tip, making it blunt, reducing spatial resolution. Damage could potentially occur on the surface of the sample as well. For these reasons, non-contact mode is used more frequently. Unlike contact mode, non-contact mode does not touch the tip to the surface, instead it operates by oscillating the tip (at its resonant frequency) in the z-direction and monitoring the changes in the amplitude of the oscillations caused by the attractive forces existing between the surface and the tip. A feedback loop is used to try to minimize the change in amplitude by moving the sample in the z-direction, creating an image of the surface. By preventing direct contact of the tip and surface, the lifetime of the tip is increased and the surface is better preserved, making non-contact mode ideal for soft samples.[7] AFM could also be used for conductivity measurements at the nanoscale, known as Conducting AFM (c-AFM).[8] A conducting tip is used in contact mode and a DC bias is applied to the tip while keeping the sample at ground. The resulting current vs. voltage is recorded, with an effective device area in the nanometers.

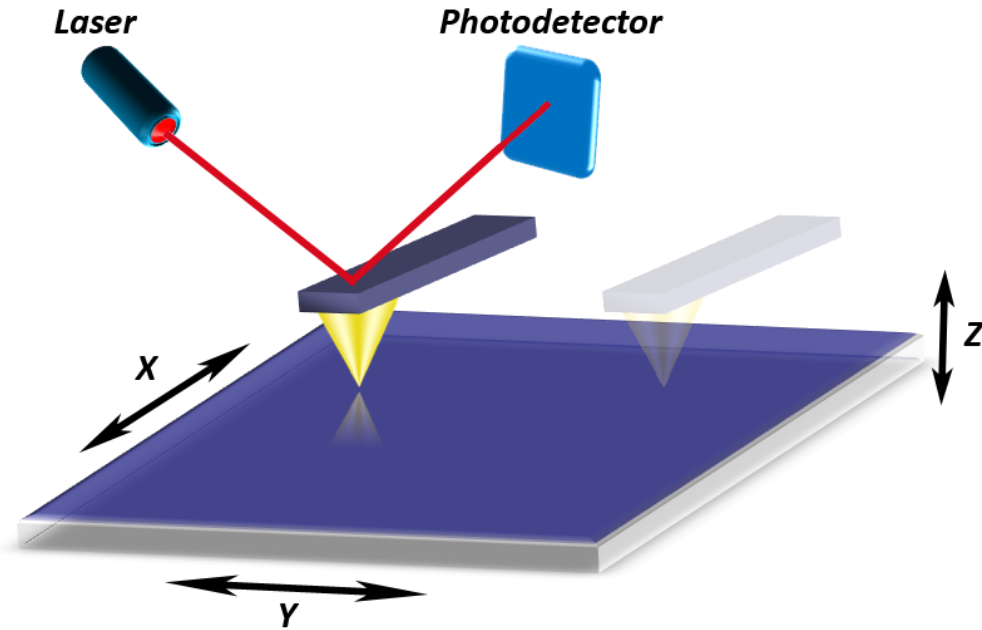


Figure 2-3 – Schematic of AFM in operation. The tip is rastered across the sample's surface and the deflection of the tip is monitored by the reflection of a laser beam.

2.2.1.3 Scanning Electron Microscopy

Scanning Electron Microscopy (SEM) is a relatively high-resolution technique for imaging structures down to nanometers. SEM functions similarly to an optical microscope. Instead of using photons, SEM relies on electrons emitted by a field emission (FE) gun to illuminate the sample. The beam of electrons is focused using electromagnets, and its energy can be varied from 1-100keV. When the beam interacts with the sample, two types of electron are emitted as shown in Figure 2-4. The first is called secondary electrons (SE) which have energies less than 50eV. These electrons originate from the first few nanometers from the surface of the sample and are generated by the high-energy electrons in the incident beam exciting conduction band electrons (valence band electrons for insulators and large band gap semiconductors) to the vacuum level, allowing them to be ejected into the vacuum ($<10^{-6}$ Torr). The SEs are then collected and converted to photons and digitally processed to form an image of the sample

surface. The second type is called backscatter electrons (BSE), which are the result of elastic scattering of the incident beam electrons with the positive nuclei of sample atoms. This process is a classic example of Rutherford scattering. As a result, BSE originates much deeper in the sample than the SE and are close to the energy of the electron beam. BSE are excellent for imaging samples whose atomic compositions varies in atomic number, since heavier atoms will appear brighter. The higher intensity occurs due to the larger cross-sectional area from the more positive nuclei associated with increasing atomic numbers. [9]

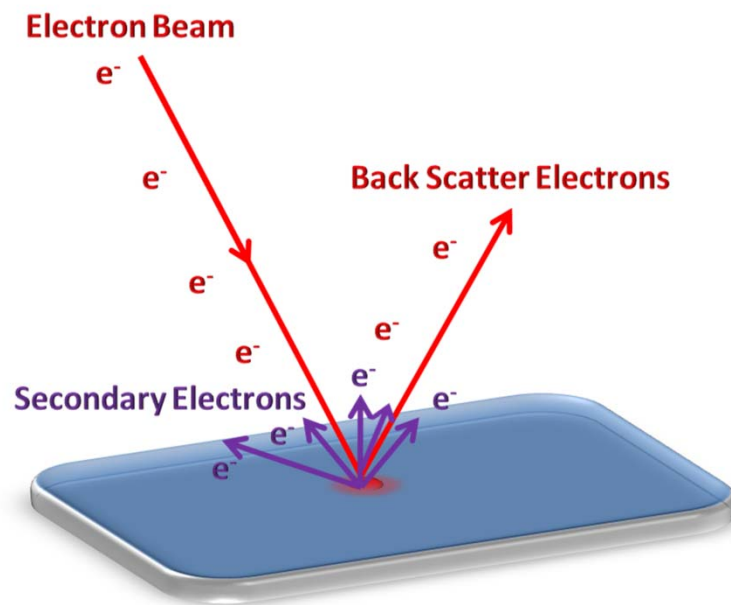


Figure 2-4 – Interaction of electron beam with the sample. Two types of electron are emitted, secondary (SE) and back scattered electrons (BSE).

2.2.2 Electrical Characterization

Electrical characterization of organic material is the primary thrust of this thesis. The types of characterization methods used were simple current vs. voltage (I-V), capacitance vs. voltage (C-V), low and high frequency dynamic response, and current vs. voltage vs. temperature (I-V-T) measurements. Measurements were performed using a specially commissioned probe station with micro manipulated probes with radius of 25 μ m. The probes were positioned with the help of an optical microscope with a wide field lens. Due to the use of insulating polymers in the devices, careful consideration to reduce noise levels in the testing apparatus was needed to achieve the high current resolutions of pico amps (pA). The probe station was placed within a grounded aluminum enclosure, called a dark box. The dark box acts like a faraday cage blocking out any stray electromagnetic radiation such as the induced fields from power lines within the building. To further reduce noise, such as from leakage currents associated with the testing apparatus, the ground connection of the dark box was connected to a guard connection to the measurement unit. The guard connection isolates the actual device current by acting as a sink for any leakage or noise currents and preventing them from reaching the measurement unit. [10, 11] All of the electrical characterization reported in this chapter was performed at room temperature using the probe station housed in the Faraday case. I-V versus temperature were performed using a special thermally controlled probe station and will be discussed in detail in Chapter 4. I-V measurements were obtained using an HP 4140B picoammeter controlled by the Agilent VEE software through standard IEEE-488 protocols with GPIB connections. It should be noted that, virtually all of the electrical measurement techniques utilized in this thesis were setup from scratch by the author. Photographs of the electrical measurement station and programs written in VEE to control the electrical measurement instruments are provided in the Appendix of this thesis. C-V measurements were performed using an Agilent 4156C semiconductor parameter analyzer, which was also controlled with the

Agilent VEE software. Low and high frequency dynamic response measurements were carried out using a 2020 Data Precision Arbitrary Function Generator to generate varying pulse patterns and an Agilent oscilloscope (Agilent 54622A 100MHz) was used to read both the voltage pulse applied to the device and its voltage response. A circuit diagram of the setup is shown in Figure 2-5. The voltage response was converted to device current through the use of a 1 Mega Ohm resistor and applying Ohms Law: $I = \frac{V}{R}$.

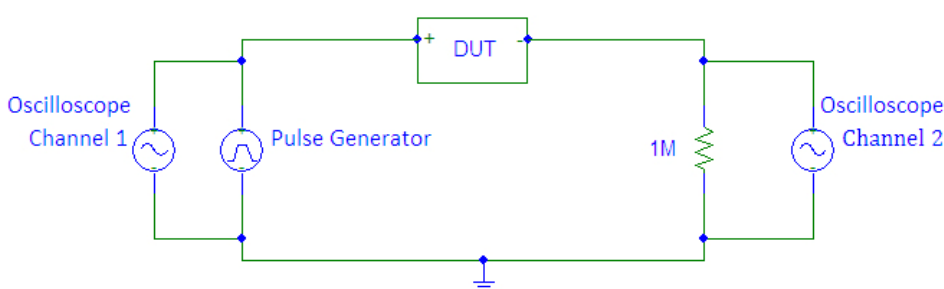


Figure 2-5 – Circuit diagram for both high and low frequency dynamic response measurements. The device current is calculated using Ohms law with a 1 Mega Ohm resistor.

2.3 PVP & C₆₀ Memory Devices

Now we describe the operation of single-layer organic memory devices. First we demonstrate that insulating polymer and C₆₀ molecule blends can act as non-volatile memory devices. Electrical measurements were performed at the macroscale to observe the bi-stability in the devices by monitoring and characterizing the presence of a hysteresis. To help in understanding the conduction process, the resulting I-V data were fitted to conduction mechanisms discussed in Chapter 1. The memory device operations and characteristics, such as data retention and response times were carefully studied. In the second part of the study, we demonstrate the scalability of the memory effect down to the nanoscale. Conducting AFM (c-AFM) measurements on nanoscale regions indicate that the blends were capable of operating at

very small dimensions, allowing the possibility of high storage densities. Nano devices using electron beam lithography were also fabricated to confirm the c-AFM measurements. Both nanoscale measurements were fitted using the method previously described. In all cases, the conduction mechanisms are similar and result from tunneling as in the case of the macroscale devices.

2.3.1 Macroscopic Devices

2.3.1.1 Device Fabrication

Macroscopic memory devices (Figure 2-6), with an area of 4mm^2 , were fabricated by first thermally evaporating $2\text{mm} \times 1\text{cm} \times 100\text{nm}$ Al strips (bottom contacts) onto a clean glass slide at a base pressure of 1×10^{-6} Torr. The glass slides were cleaned by ultrasonicing in an acetone bath for 15 minutes, followed by 10-minute sonication in an isopropanol bath, and next for 10 minutes in a deionized water bath. Finally, the glass slides were rinsed with fresh deionized water and blow-dried with dry nitrogen gas. After evaporation, a solution of 25mg of PVP and 0.5mg of C_{60} dissolved (giving weight percent ratio of 2%) in 1ml of isopropanol was spun on to the electrodes at 7400 RPM and allowed to dry. A C_{60} concentration of 2% was chosen because it is well below the percolation limit of C_{60} (see calculation provided later). The resulting PVP + C_{60} film thicknesses were measured at 30nm using a combination of high-resolution field emission scanning electron microscope (FESEM) and interferometry. Finally, 2mm strips of Al (top contacts perpendicular to the bottom contacts) were thermally evaporated. The result is a MIM (metal-insulator-metal) structure, utilizing a cross-point array architecture. Pure PVP devices for comparison were fabricated using the same procedure, except with solution of 25 mg PVP in 1ml isopropanol.

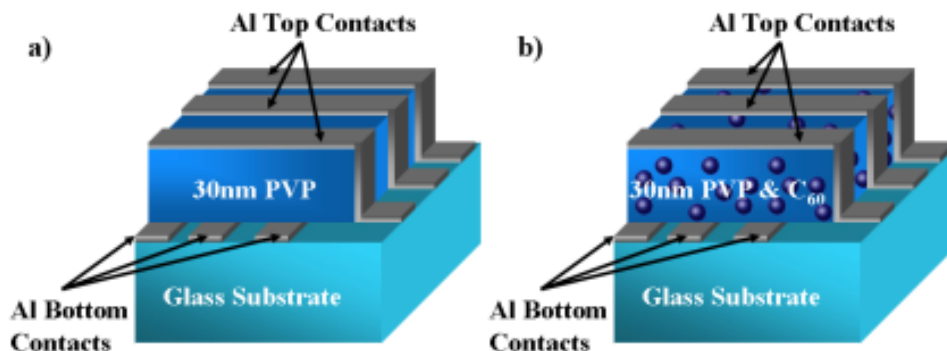


Figure 2-6 – Macroscopic device structures of pure PVP (a) and PVP + C₆₀ device (b).

2.3.1.2 Structural Characterization

Atomic Force Microscopy

The spin coated organic films were found to be well adhered and smoothed with an average roughness ranging from 3 – 5 nm as determined by an atomic force microscope (AFM). Pure PVP or the blend films do not show any surface texture and appear uniform and flat throughout as shown in Figure 2-7a and Figure 2-7b, respectively. In addition, the blend films showed no evidence of pinholes or large aggregates of C₆₀, indicating that the blend is homogeneous. Aggregates or pinholes, if present could potentially produce shorts either through thinner regions of PVP or through clusters of C₆₀ that could extend across the top and bottom contacts.

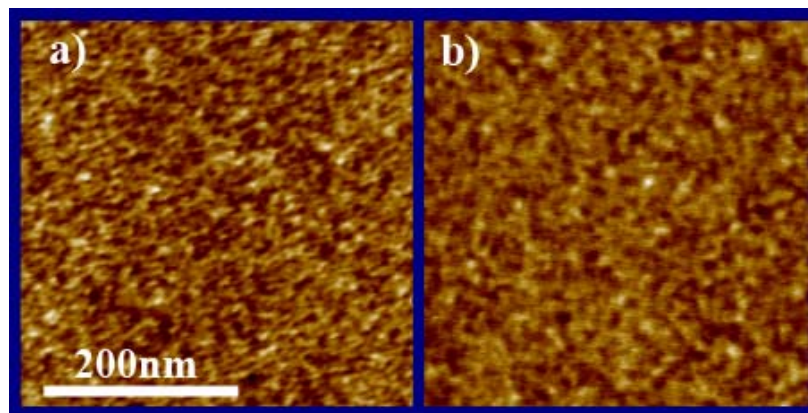


Figure 2-7 – Atomic force microscopy (AFM) images of (a) PVP polymer and (b) PVP + C₆₀ blend layer surfaces. Images were obtained using a Digital Instruments Nanoscope AFM in tapping mode at a frequency of 0.3 kHz. The root mean square roughness extracted from AFM of the pure PVP and blend layers was ~3 – 5 nm.

Raman Spectroscopy

Raman spectroscopy was used to confirm the incorporation of C₆₀ in our blend films by monitoring the A_{1g} tangential Raman mode for C₆₀ near 1469 cm⁻¹ (Figure 2-8) [4, 5]. Three films were analyzed, pure C₆₀, pure PVP and the PVP + C₆₀ blends. The pure PVP contains small peaks at low wave-numbers but the 1469 cm⁻¹ tangential mode peak is absent while the blend material exhibits a combination of PVP and C₆₀ peaks. The uniformity of the C₆₀ distribution was verified by taking Raman spectra at multiple places across the films.

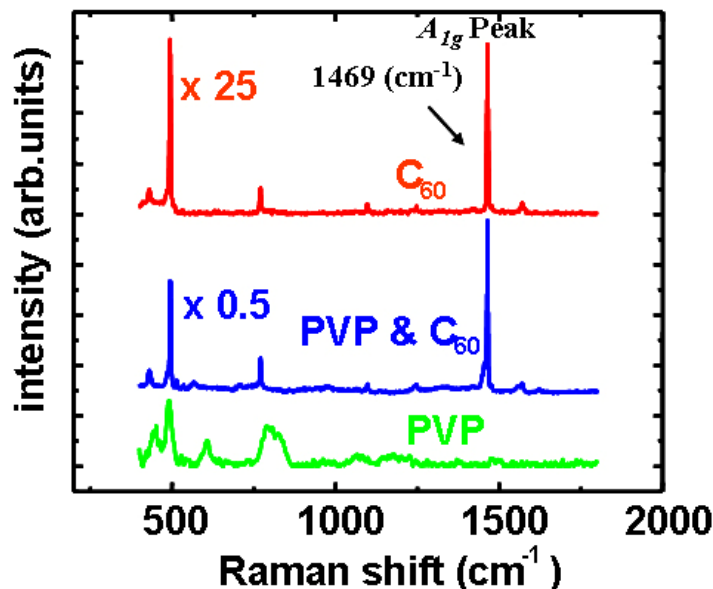


Figure 2-8 – Raman spectra of pure PVP, pure C_{60} and PVP + C_{60} blend thin films on quartz substrate. The tangential mode peak of the C_{60} molecules is clearly present in the blend films and is absent in pure PVP, indicating that they have been incorporated into the material. Spectra were obtained with a Renishaw System 1000 instrument using a Peltier cooled CCD. The measurements were carried out with a 785 nm laser with a $2\mu\text{m}$ spatial resolution. The resulting data was analyzed utilizing the software package called Wire version 2.0 with a grading set to 1200 lines per millimeter.

2.3.1.3 Electrical Measurements

Current vs. Voltage

Typical current-voltage (I-V) measurements of the macroscopic pure PVP and PVP + C_{60} devices exhibit symmetrical characteristics for negative and positive applied voltages, shown in Figure 2-9a and Figure 2-9b. The PVP only devices show negligible hysteresis (Figure 2-9a) while a clear hysteresis can be seen in the PVP + C_{60} devices (Figure 2-9b), indicating that C_{60} is responsible for the hysteresis. Although no clear threshold voltage is observed in contrast to results of Bozano et al [12] and Ouyang et al [13], the hysteresis in the PVP + C_{60} devices is sufficiently large (the maximum difference between the current levels, being approximately 50 –

75nA at +1.0V) to allow definitive write (+2.5V), read (+1V) and erase (-2.5V) states. A short circuit current at 0V is clearly observed in the I–V characteristics of the PVP + C₆₀ devices, as shown in Figure 2-9b. This is related to the fact that application of the initial negative voltage leads to the injection of electrons into the C₆₀ molecules, which begin to screen the applied voltage. The actual voltage across the device will be different from the applied voltage. Zero current is in fact measured at + 1.35V and – 1.35V in the upward and downward sweeps, respectively. These voltages are consistent with the threshold voltage in the capacitance vs. voltage measurements, which will be discussed later, indicating the voltage induced is due to the storage of charge in the C₆₀ molecules.

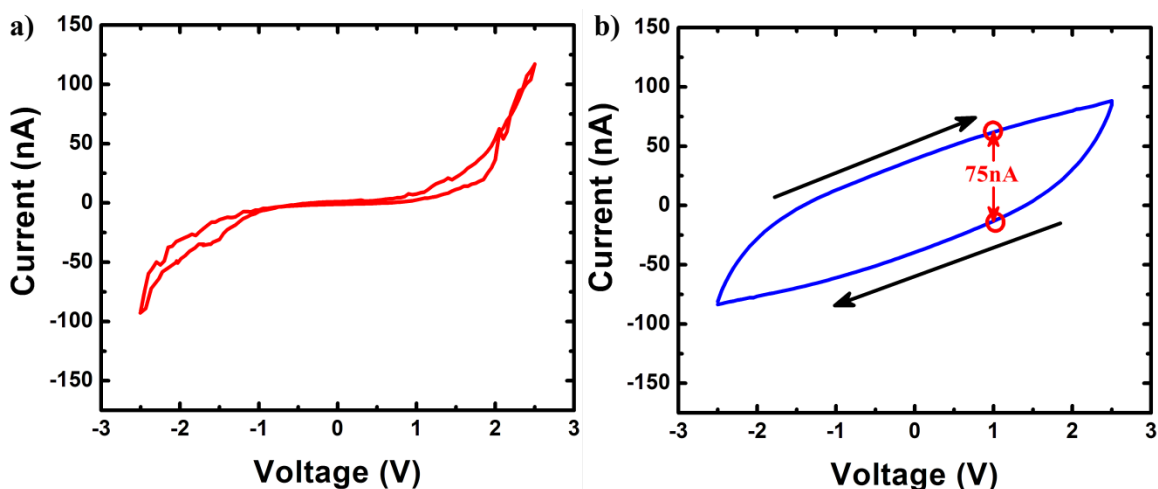


Figure 2-9 – Current versus Voltage characteristics of pure PVP and PVP containing C₆₀ devices on glass substrates. (a) The pure PVP MOM devices exhibit negligible hysteresis as the voltage is swept from negative to positive. (b) In contrast, the PVP + C₆₀ devices exhibit a distinct hysteresis with a current difference of approximately 50 – 75nA between the high and low conduction states. The arrows indicate the direction of the sweep. The measurements were performed at room temperature with an Agilent 4140B pico-ammeter at a sweep rate of 10ms/V.

Sweep Rate

I-V measurements were performed at varying sweep rates to determine if the hysteresis is due to artifacts or traps in the polymer. Pure PVP and PVP + C₆₀ devices were measured with sweep rates varying from 100 μ s/V to 100ms/V (Figure 2-10). PVP + C₆₀ devices maintain their observed hysteresis throughout the various sweep rates. In addition, the pure PVP devices do not show a presence of a hysteresis. The lack of hysteresis in the pure PVP devices and the stable hysteresis in the PVP + C₆₀ devices confirm that the hysteresis unlikely to be from traps or artifacts that could be associated with the polymer. There is a relative decrease in conductivity in the pure PVP devices as the sweep rate is slowed. This can be attributed to a relaxation in the polymer during the measurement. However, this effect is overpowered by the screening of the charged C₆₀ molecules. This is evident from the relatively small drop in overall conductivity at slower sweep rates until 100ms/V for the PVP + C₆₀ devices.

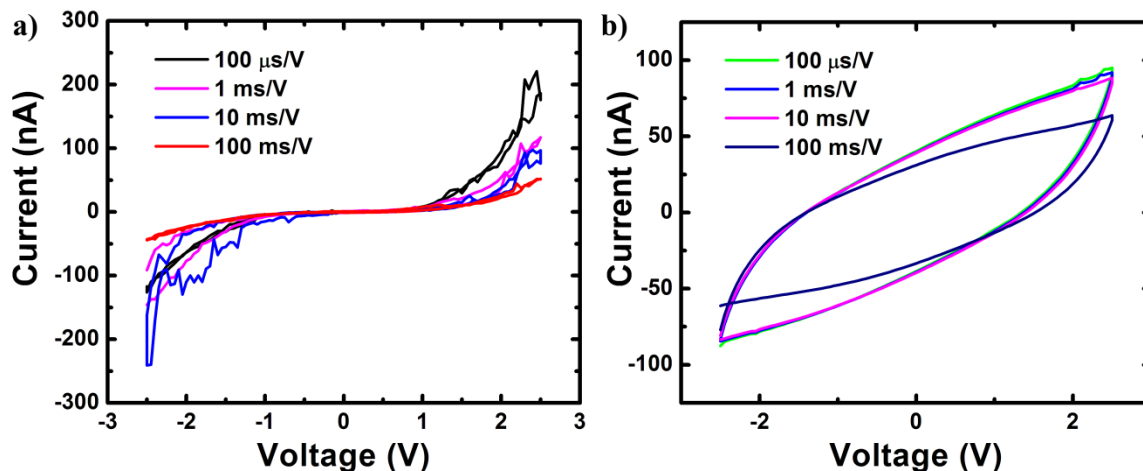


Figure 2-10 – Current versus Voltage characteristics at varying sweep rates of 100 μ s/V to 100ms/V of (a) pure PVP and (b) PVP containing C₆₀ devices on glass substrates. (a) The pure PVP MOM devices exhibit negligible hysteresis as the voltage at varying sweep rate. (b) In contrast, the PVP + C₆₀ devices exhibit a distinct hysteresis throughout the various sweep rates.

Varying Film Thickness

Thickness vs. I-V measurements were performed on both pure PVP and PVP + C₆₀ devices to optimize device performance. Thicknesses were varied by varying the RPMs during the spin coating stage of the device fabrication process while concentration and other factors were kept constant. Figure 2-11a shows the relationship between the spin speed and the thickness of the films. Varying the thickness in the pure PVP devices provided information on the breakdown voltages and the expected operating voltage for a given thickness (Figure 2-11b). The breakdown goes through two phases. The first is called a soft breakdown in which conducting filaments form creating paths for larger amounts of electrons to flow through. With continued increase in voltage, the filaments collect and change the physical structure to point where the second phase, called hard breakdown occurs. The filaments during the soft breakdown are detrimental to the storage of charge in the C₆₀ molecules because they essentially reduce the barriers that maintain the electrons in the C₆₀, allowing them to escape. Thus, devices must operate below the point of soft breakdown. Based on Figure 2-11b, an increase in the thickness results in a non-proportional increase in the operating voltage. This is because the thicker films are capable of supporting more conducting filaments. Thus, 30 nm film thicknesses were chosen as the optimal thickness since any conducting filaments that are produced would lead to a hard breakdown. By operating close to the hard breakdown point, the devices can withstand a larger current level without producing any filaments. This means that the device will be more sensitive to charging of C₆₀ molecules and provide a large hysteresis.

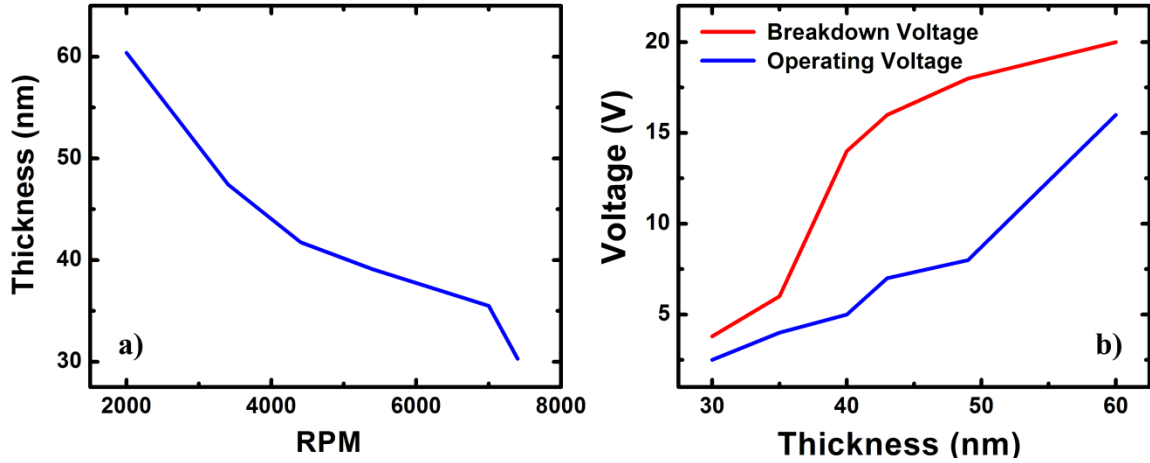


Figure 2-11 – (a) Film thickness vs. spin speed. (b) Breakdown and operating voltage vs. film thickness.

Percolation Limit

The percentage of C_{60} to polymer is important to ensure that electrons remain trapped in the C_{60} molecules and do not tunnel out on their own. The threshold percentage of C_{60} where tunneling or other interactions between the C_{60} molecules in PVP can occur is called the percolation threshold. To obtain the optimal concentration of C_{60} for memory devices, it is important to utilize a concentration well below the percolation threshold. To derive the threshold, we first assume that the C_{60} molecules are perfect spheres and therefore their volume is given by:

$$V_{C_{60}} = \frac{4}{3}\pi r^3 \quad (2.2)$$

Where $V_{C_{60}}$ is the C_{60} molecule volume and r is its radius. Next, we need to consider both the volume of the sphere and the volume around it that is not accessible to another C_{60} molecule.

The combined volume is known as the excluded volume and can be derived by first considering the excluded volume of a cylinder capped with two hemispheres [14, 15]:

$$V_{Ex} = \frac{32}{3}\pi r^3 + 8\pi l r^2 + 4l^2 r \langle \sin \theta \rangle \quad (2.3)$$

Where V_{Ex} is the excluded volume, r is the radius of the cylinder, l is its length, and $\langle \sin \theta \rangle$ is the degree of alignment of the cylinders. Taking the limit of Equation (2.3) as l approaches zero, we get the equation for the excluded volume for C_{60} molecules, depicted in Figure 2-12a:

$$V_{Ex} = \frac{32}{3}\pi r^3 \quad (2.4)$$

Where V_{Ex} is the excluded volume and r is the radius of the C_{60} molecule. The percolation threshold, in terms of volume, is defined as the volume fraction (ϕ_{V_c}) of the C_{60} molecule and the excluded volume: [14, 15]

$$\phi_{V_c} = \frac{V_{C_{60}}}{V_{Ex}} = \frac{\frac{4}{3}\pi r^3}{\frac{32}{3}\pi r^3} = \frac{1}{8} \quad (2.5)$$

To find the percolation threshold in terms of the weight percentage of C_{60} and PVP, we need to multiply Equation (2.5) by the ratio of the densities of PVP and C_{60} .

$$\phi_{W_c} = \frac{\rho_{C_{60}}}{\rho_{PVP}} \phi_{V_c} = \frac{1.47 \text{ g/cm}^3}{1.16 \text{ g/cm}^3} \left(\frac{1}{8} \right) = 16\% \quad (2.6)$$

Where ϕ_{W_C} is the percolation threshold in terms of the weight percentage, $\rho_{C_{60}}$ is the density of C_{60} , and ρ_{PVP} is the density of PVP. Therefore, the percolation threshold for C_{60} in PVP is 16%. In order to test whether this weight percent for achieving the percolation threshold is accurate, we performed measurements as 2% and 16% C_{60} concentrations in PVP. Figure 2-12b (i-ii) shows the difference in I-V behavior of a blend film at 2% C_{60} and 16% C_{60} . It can be seen in Figure 2-12bii that near the percolation threshold, the hysteresis in the I-V curve is almost entirely absent. Since the distribution of C_{60} in the PVP is completely random, around 16%, the number of isolated C_{60} molecules is significantly reduced and charges are able to tunnel from one C_{60} molecules into nearby ones. This reduces the charge storing capability and effectively eliminates the hysteresis in the I-V curve. In addition, a conducting path can develop through which electrons can be transported via the C_{60} molecules, as shown in Figure 2-12c, increasing the overall current of the device. Although any concentration below the percolation threshold yields a hysteresis in the I-V characteristics, we found that 2% is the optimal concentration in terms of achieving a uniform blend, sufficiently large current values, and ease of processing.

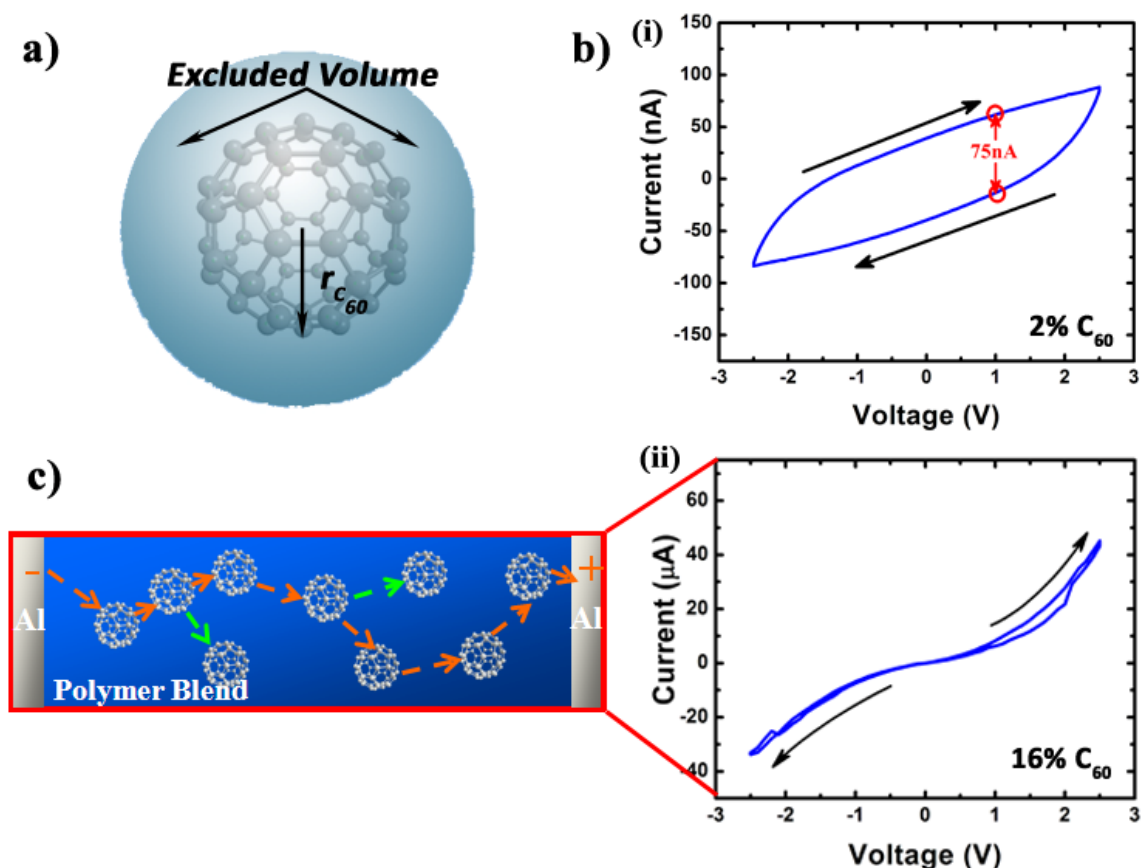


Figure 2-12 – a) The excluded volume of a C₆₀ molecule, with $r_{C_{60}}$ as the radius. b) (i) I-V plot of a PVP + C₆₀ blend at 2 weight percent. (ii) I-V plot of a PVP + C₆₀ blend at 16 weight percent. Conducting paths start forming preventing charge storage and increasing device current. c) Diagrams depicting percolation at high weight percent of C₆₀.

Capacitance vs. Voltage

In order to confirm that charge injection and retention is indeed occurring in the C₆₀ molecules and not in the polymer, capacitance vs. voltage (C-V) measurements were carried out. Two types of devices were investigated; one of pure PVP and the other of PVP + C₆₀ blend (Figure 2-13a). Both devices were constructed with a standard metal-insulator-semiconductor (MIS) architecture. The semiconductor portions of the MIS structure allows for the generation of charges, which are capable of being stored within the insulating layer, creating a hysteresis in

the C-V curve. The hysteresis is the result of a threshold shift in the voltage required to switch the device from inversion (high concentration of minority carriers at the interface of the semiconductor and the insulator) to accumulation (high concentration of majority carriers the interface) caused by any stored charges within the insulator. Our MIS devices consisted of a p-type silicon (Si) semiconductor, dictating that any charging of the C_{60} molecules in the blend layer would occur during the inversion region (positive voltage) due to the accumulation of electrons. Discharging would occur during the accumulation region (negative voltage) due to the accumulation of holes. Both pure PVP and blend devices were fabricated by first cleaning the p-type Si chips in a piranha solution (consisting of 30% H_2O_2 , and 70% H_2SO_4) for 20 minutes, followed by rinsing in deionized water and blow-drying with dry nitrogen. This cleaning process removes organic materials from the surface, which could potentially create shorts, or act as charging centers. In addition, the cleaning process also allows for the formation of an ohmic back contact. The ohmic contact ensures charge injection of the minority carriers (electron for p-type Si) so accumulation and inversion can occur. With the native oxide removed from the back of the silicon, aluminum (Al) was thermally evaporated onto the back of the p-type Si substrates and annealed at 490°C in a nitrogen atmosphere to form the ohmic back contact. For pure PVP devices, PVP was spin coated on top of the 1-2 nm native oxide (formed due to exposure in air after the formation of the ohmic back contact) at a thickness of 65 nm. Al was then thermally evaporated to form the top contacts. The 65nm thickness of the PVP layer was chosen to ensure the leakage current across the MIS device would be on the order of pico-amps. The PVP + C_{60} device were fabricated in a similar fashion, except that a 30 nm layer of PVP + C_{60} was spin coated, between the 65 nm PVP and native oxide. The final C-V device structures are schematically shown in Figure 2-13a(i-ii).

C-V curves for the pure PVP devices [Figure 2-13b(i)] show the usual accumulation/depletion/inversion characteristics associated with MIS structures. The absolute value of the accumulation capacitance ($\approx 290\text{pF}$) is consistent with that estimated from the PVP film (thickness = 65 nm) on top of the 2 nm SiO_2 layer. The C-V measurements on MIS structures containing C_{60} show significant hysteresis, suggesting charge storage in the C_{60} layer (Figure 2-13c). The direction of hysteresis indicates that the charging of C_{60} takes place from the semiconductor side by electron tunneling through the thin oxide layer. Based on the C-V behavior of these devices the hysteresis in the I-V characteristics is attributed to charge injection and retention in the C_{60} molecules.

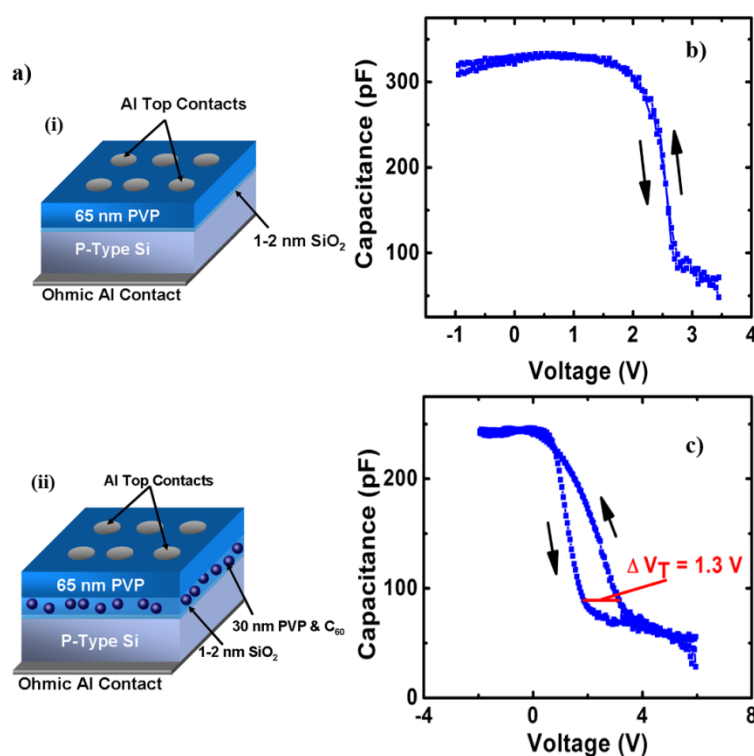


Figure 2-13 – (a) Metal-insulator-semiconductor (MIS) structures consisting of ohmic bottom Al contact, p-type Si with a 1 – 2 nm SiO_2 layer, organic layer (thickness = 65 nm to prevent leakage current) and top Al electrodes. (b) The pure PVP device does not show any hysteresis while the (c) MIS device with PVP + C_{60} shows a hysteresis with a threshold voltage of 1.3V, indicating that charge storage occurs in the C_{60} molecules.

Charge Transfer observation with Raman Spectroscopy

Although the C-V measurements provide indirect evidence of charge injection and retention in C_{60} molecules, Raman analysis can provide a more direct evidence by monitoring the A_{1g} Raman mode of a device, immediately after fabrication and after application of +2.5V and -2.5V. The application of +2.5V and -2.5V corresponds to the write and erase steps in the I-V plot, respectively. The Raman A_{1g} mode downshifts (compared to the as-synthesized device) by a few wave numbers after the write step (even after the Raman measurements taken up to 24 hours after the memory operation) but appears at the expected 1469 cm^{-1} peak position after the erase operation, as shown in Figure 2-14. The downward shift of the C_{60} A_{1g} peak is a strong indication that charge injection into C_{60} occurs after the write operation [16-19]. The shift in the Raman peak does not imply that all the C_{60} molecules are charged to the same state. The downshift is attributed to the stimulated transversal vibration of the charged C_{60} molecules, due to the red excitation laser. The disappearance of the A_{1g} peak is due to the summing of the signals from the different charged C_{60} molecules, including the uncharged ones. Since the amount of charged C_{60} molecules is greater than the neutral molecules, the A_{1g} peak is suppressed and absorbed in the observed downshifted peak. The appearance of the A_{1g} peak at 1469 cm^{-1} after the erase operation also indicates that the injected charges have been discharged. Thus C-V and Raman analysis provide strong evidence that C_{60} molecules are responsible for the hysteresis (and thus the memory effect) in our devices.

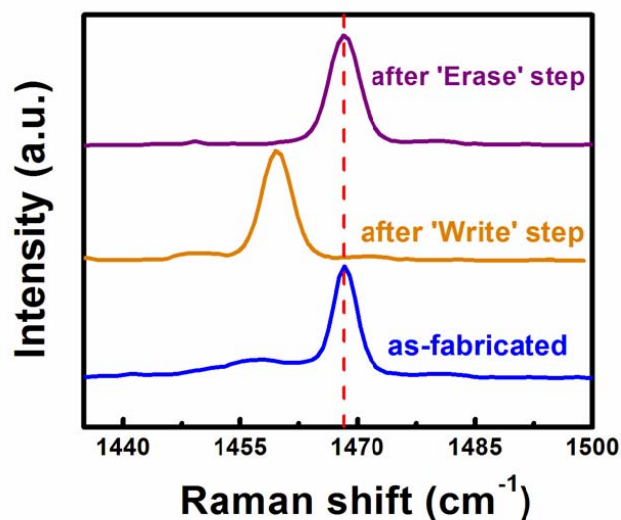


Figure 2-14 – Raman spectra near the A_{1g} C_{60} peak of a device after three memory operations. The as-fabricated device shows the C_{60} A_{1g} mode at the expected 1469 cm^{-1} peak position (indicated by the vertical line) which shifts downward after the application of 2.5V pulse (write step), indicating that charge injection into C_{60} molecules has occurred. The discharging of carriers from the C_{60} after the application of -2.5 V (erase operation) is clearly indicated by the fact that the A_{1g} appears at the expected 1469 cm^{-1} peak position.

Waveform – Read-Write-Erase-Cycles

High frequency

In order to translate the I–V hysteresis into memory operations, multiple read-write-erase cycles measurements were carried out on the PVP+ C_{60} devices at high frequency (Figure 2-15a) using an arbitrary wave function generator. It can be seen at point 1 in Figure 2-15a that the device can be turned from high ('0' ON state) to low ('1' OFF state) conductivity states by applying +2.5 V to negatively charge the C_{60} molecules, this could be registered as the 'write' step. The write step corresponds to point 1 of the hysteresis loop in Figure 2-15b. Next, the device is brought down to 0V, corresponding to point 2 in hysteresis loop. Then by applying

+1.0V, a low current can be recorded (read step) to register a '1' state, as in point 3 in the loop. The device is brought back to point 2. The device can then be fully erased by applying -2.5V to return it to its original OFF state, corresponding to point 4 in the hysteresis loop. The device state is next moved to position 5 in the hysteresis loop by applying 0V. The OFF state can be read by applying +1.0V pulse, corresponding to point 6 on the hysteresis loop, providing a higher current than the ON state. Finally, the device is brought back to point 5 with a 0V pulse. The noticeable decrease in the current during each memory operation is attributed to a continuous decrease in the effective applied voltage due to screening from charge injection into the blend layer. The high frequency memory operation measurements in Figure 2-15a show a persistent offset in the 0V current. This is because the device does not reach equilibrium during the high frequency pulses. Figure 2-15c shows that the device takes 1 to 2 seconds before reaching equilibrium, with a consistent difference in current for both the '0' and '1' states. Thus, for any set frequencies of operation the '0' and '1' states will remain distinguishable. This is important since any memory device will operate at a single defined frequency that is chosen during the design process. Therefore, during the high frequency operations, the offset zero voltage current would not be a factor in the devices performance, since the two states would remain distinguishable at the end of the short read operation.

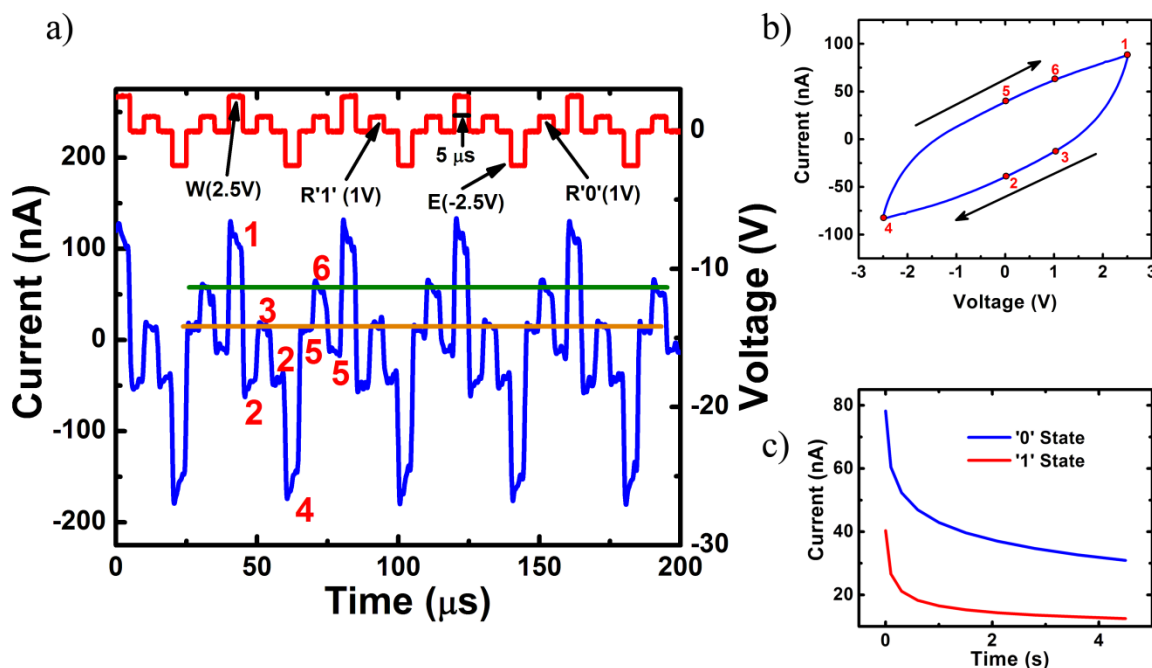


Figure 2-15 – (a) Current versus voltage response of the memory devices during high frequency write-read-erase-read voltage cycles. Initially a voltage pulse of +2.5V is used for writing (W) which can be read (R) by applying +1 V ('1' bit, low conductance). This information can be erased (E) by applying a voltage pulse of -2.5 V. The fact that the original data has been erased can be confirmed by applying +1 V to read ('0' bit, high conductance). The ON and OFF states can be clearly distinguished by the large current difference indicated by the two horizontal lines. (b) I-V plot with corresponding states labeled. (c) Current decay during reading operation for both '0' and '1' states. The two states remain distinguishable.

Low Frequency

Low frequency read-write-erase cycle measurements were performed to allow the device to operate at equilibrium (Figure 2-16). Pulse widths of 4 seconds were used, longer than the time needed for the devices to reach equilibrium. Despite the long time scale, the '0' and '1' states remain distinguishable. The difference in currents for both the states is smaller than the high frequency operation as expected from the current decay graph in Figure 2-15c. However,

this does not present a significant problem since these low frequency operations would not be used; instead, the devices are required to operate at the higher frequencies.

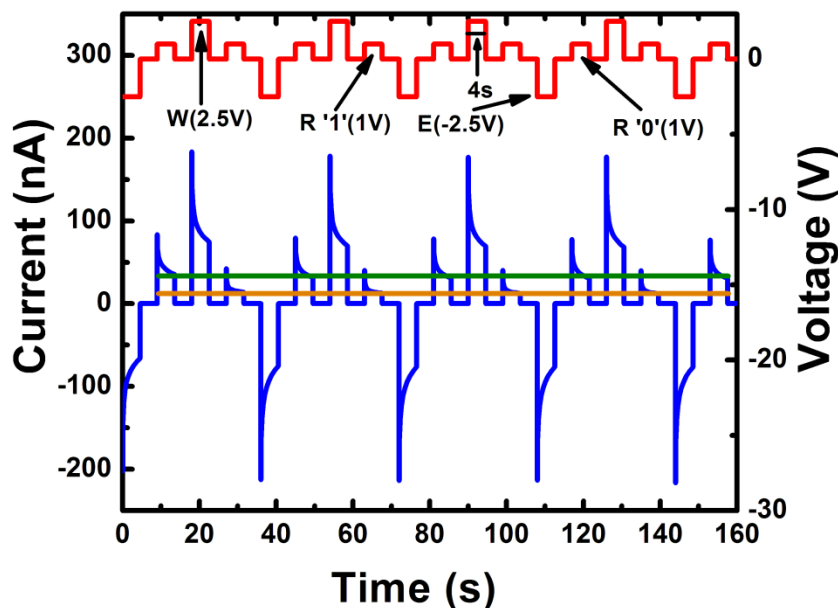


Figure 2-16 – Current versus voltage response of the memory devices during low frequency write-read-erase-read voltage cycles. The '0' and '1' States remain discernable.

Response time

The response time of the devices is important because it dictates how fast they can operate. In order to measure the response time, a 2.5V pulse (representing the write operation) is applied to the device and the delay time measured. A typical result demonstrating switching times of nano-seconds is shown in Figure 2-17. The average response time of 10ns is comparable to a typical DRAM chip, which is designed to operate at 70ns. This suggests that the PVP + C₆₀ memory device are capable of performing memory operations at high speeds that are required in the main memory of computer systems.

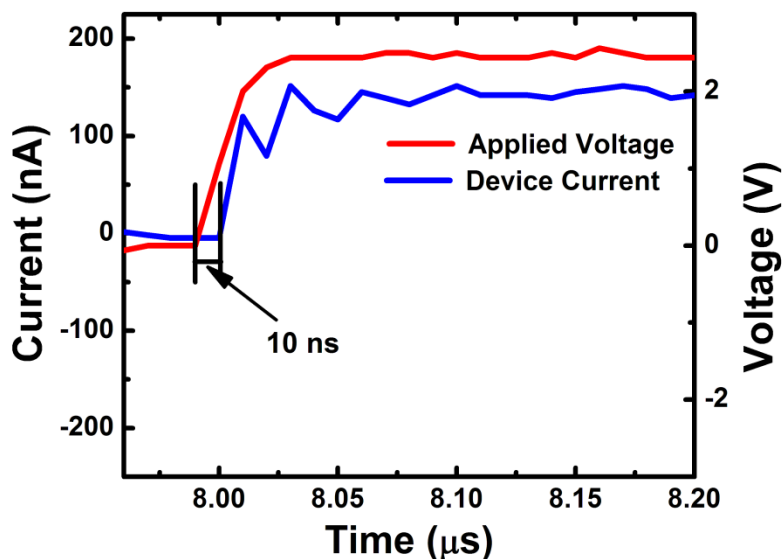


Figure 2-17 – Measured response time of 10ns for PVP + C₆₀ devices

Data Retention

In order to investigate the non-volatile nature of the memory devices, devices were read for 2 hrs to monitor both the OFF ('0' bit) and ON ('1' bit) states. The results are shown in Figure 2-18. The devices were tested by initially applying a -2.5 V pulse to erase any retained data. The ON state was obtained by applying a pulse of +2.5 V and then bringing the voltage down to +1V where it was held for 2 hours and the current monitored. The OFF state was obtained by applying a -2.5 V pulse and then bringing the voltage up to +1V where it was held for 2 hours and the current monitored. No deterioration of the performance was observed for up to 1 hour, after which a slight decline in both ON and OFF states currents were observed for the next hour. However, the difference between the ON and OFF states always remained constant, indicating data retention. The decline in current after 1 hour could be attributed to the degradation in the polymer from the constant application of 1V. This should not pose a problem in a real world application since the continuous two-hour testing of the ON and OFF states

translates into substantially long time as compared to a single read-write-erase cycle, which is only a few tens of nanoseconds.

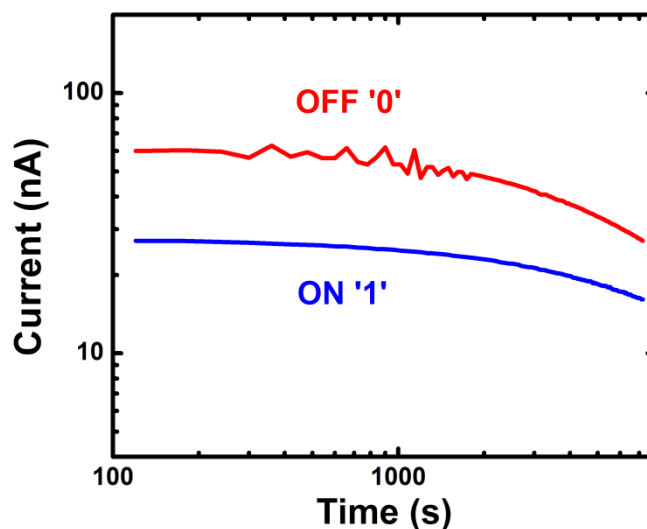


Figure 2-18 – Data retention graph showing a consistently higher current value for the OFF state than for the ON state.

Conduction Mechanism

Standard conduction mechanisms for organic devices (as discussed in Chapter 1) were fitted for both the high and low conduction states located in the positive region of the I-V curves for the PVP + C₆₀ devices (Figure 2-9) in order to understand the mechanisms responsible for conduction. Differences in the conduction mechanisms should become apparent by fitting the two states independently. The high conducting state ('0' state) is analyzed first. No single model was found to adequately fit the entire curve, instead two mechanisms in the low (0-1.3V) and high voltage (1.3-2.5V) regimes were needed (Figure 2-19). From 0 to 1.3V direct tunneling was found to be most appropriate mechanism, in which electrons tunnel through a square barrier. After 1.3V, the applied voltage is enough to change the shape of the barrier into a triangular

one, thus allowing Fowler-Nordheim tunneling to occur. Fits from other models were found to be unsuitable for explaining the data in either regimes of the curve.

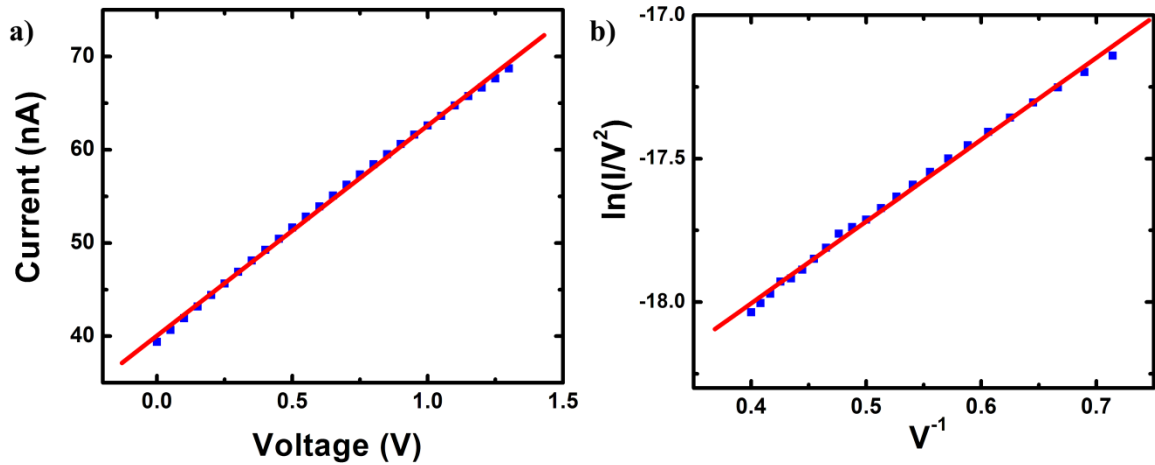


Figure 2-19 – Fits for the high conducting state in the positive region of the upward sweep of Figure 2-9b (a) Fit for direct tunneling from 0 to 1.3V. (b) Fit for Fowler-Nordheim tunneling from 1.4 to 2.5V. The blue squares represent the experimental data and the red line represents the fit.

After +2.5V, the voltage is swept downwards. Where, the device operates in a low conducting state. Similar to the high conducting state, a threshold exists where the conduction mechanisms switches between Fowler-Nordheim and direct tunneling. Above 1.8V Fowler-Nordheim is the dominant mechanism, shown in Figure 2-20a. Below 1.8V direct tunneling takes over, as shown in Figure 2-20b. However, closer examination of the data in Figure 2-20b shows that there does exist a 'kink' in the data at +1.35V as the voltage is swept down from 1.8V to 0V.

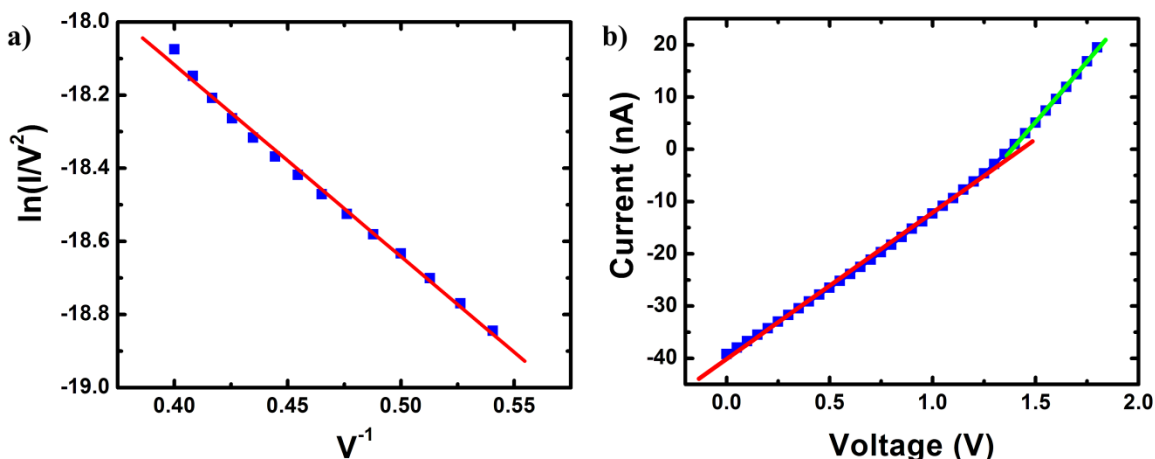


Figure 2-20 – Fits for the low conducting state in the positive region of the downward sweep of Figure 2-9b (a) Fit for Fowler-Nordheim tunneling from 2.5V to 1.8V. The blue squares represent the experimental data and the red line represents the fit. (b) Fit for direct tunneling from 1.8V to 0V. The green line represents a direct tunneling fit from the region of 1.8V to 1.35V and the red line the direct tunneling fit for the region of 1.35V to 0V.

We explain the appearance of this change in slope using Figure 2-21. The ‘kink’ in the downward sweep arises from a change in the direction of current at +1.35V. Initially, as the voltage is swept to +2.5V, the electrons are injected from the bottom electrode and trapped by the C_{60} molecules. As the voltage is decreased from +2.5V in the downward sweep, the total screening voltage ($\sim 1.3V$) due to C_{60} charging is not sufficient to block injection of carriers from the bottom contact. However, when the voltage is decreased down to $\sim 1.35V$, the applied and screening voltages are equal and the effective voltage is zero. A further decrease in voltage results in the top contact experiencing a more negative potential than the bottom contact. Thus, injection of carriers from the top contact starts to occur as schematically indicated in the right panel of Figure 2-21. However, the C_{60} molecules close to the metal-polymer interface are still neutral and do not effect charge injection from top contact into the polymer, as opposed to injection from the bottom contact where charged C_{60} molecules alter the injection of electrons.

Therefore, barriers are different when charge injection occurs from the top contact vs. the bottom contact during the low conducting region. This difference in barriers leads to a 'kink' at 1.35V in the fit for direct tunneling.

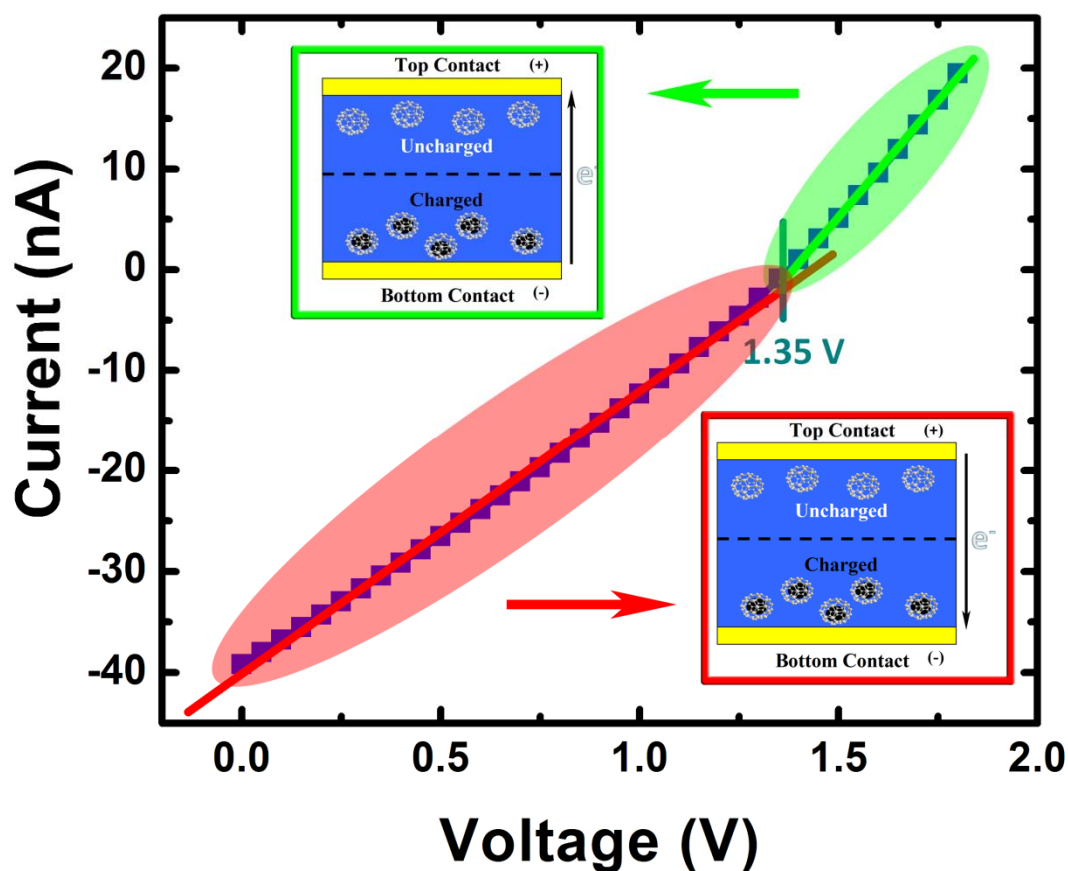


Figure 2-21 – Two direct tunneling regions during the low conducting state. Direct tunneling starts after 1.8V and continues through 0V. However at 1.35V the stored charges near the bottom contact cancel the applied 1.35V, giving zero current. When the voltage drops below 1.35V the current switches direction and electrons inject from the top contact, where the C_{60} are still neutral. As a result the slope of the fit line changes.

The difference in conduction mechanisms for the high and low conducting states is expected due to the charged C_{60} molecules associated with low conduction state. The charged C_{60} molecules screen out part of the applied voltage, shifting the threshold for switching from Fowler-Nordheim tunneling to direct tunneling. In addition, the semi charged layer of C_{60} molecules creates a 'kink' in the direct tunneling fit.

2.3.2 Nanoscale Operation

The macroscopic devices clearly demonstrate that the blend structure of an insulating polymer and C_{60} is capable of performing fast non-volatile memory operations. However, it is unclear if the devices can work at the nanoscale. Conducting AFM (c-AFM) measurements were performed along with nanoscale gap cells to demonstrate operation of the devices at the nanoscale. Both experiments independently show similar characteristics to the macroscale devices.

2.3.2.1 Conducting AFM

Conducting AFM measurements were first utilized since it does not require any type of lithography. Instead, it relies on a conducting AFM tip, which is brought in contact with the blend film. Thus, the device area is defined roughly by the contact area of the AFM tip, allowing for a quick nanoscale measurement.

The c-AFM measurements were performed on a 30 nm PVP + C_{60} blend films deposited on glass substrates coated with a conducting indium tin oxide (ITO). ITO is a transparent and conducting oxide, typically deposited as a thin film and is used extensively in application requiring transparent and conducting electrodes [20]; such as touch screens, LCD monitors,

organic solar cells, and organic light emitting diodes (OLED) [21-23]. The ITO substrates were used for the Raman study so that Raman with device operation could be studied. The results of the Raman study were successful, showing that ITO is a suitable electrode material. The top contact in c-AFM is formed after the platinum-coated AFM tip is contacted to the film, giving a device area of approximately 50nm^2 . The device area is a rough approximation since force separation data is required for determining the contact area and could not be obtained due to limited access to the instrument. I-V measurements were performed at four positions (i – iv) in a square array as indicated in Figure 2-22.

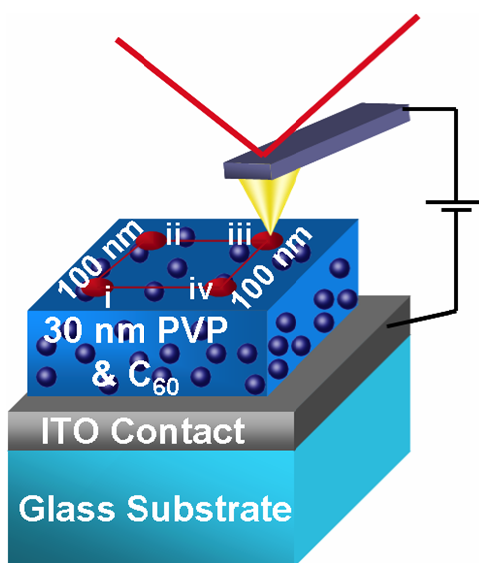


Figure 2-22 – Schematic of c-AFM device. Four measurements at the shown positions were taken. The AFM tip was platinum coated in order to make it conducting.

Comparison to Macroscale Devices

Typical I-V results from the c-AFM measurements are shown in Figure 2-23a. The I-V curves from the c-AFM measurements are very similar to the macroscopic devices (Figure 2-23b). As observed in the macroscopic devices, the c-AFM exhibits a large hysteresis, despite a drop in overall current. The current values unexpectedly do not scale with the electrode area from the macroscopic (100nA) to the nanoscale (200pA). This is attributed to the field enhancement occurring from the c-AFM tip. The relatively sharp tip, as compared to the flat sheet of the ITO, causes the electric field to concentrate at the AFM tip (top contact) causing the barrier between the AFM tip and the polymer film to bend more than expected. The smaller barrier allows for an increase in the number of electrons that can tunnel through the barrier and flow through the device, effectively providing a higher current than expected from simply scaling of the contacts. The finite short circuit current from the macroscale devices is also present in the c-AFM measurements. Similar to the macroscale devices, the write step can be performed by applying +2.5V, the erase step with -2.5V and the read state can be observed with +1V.

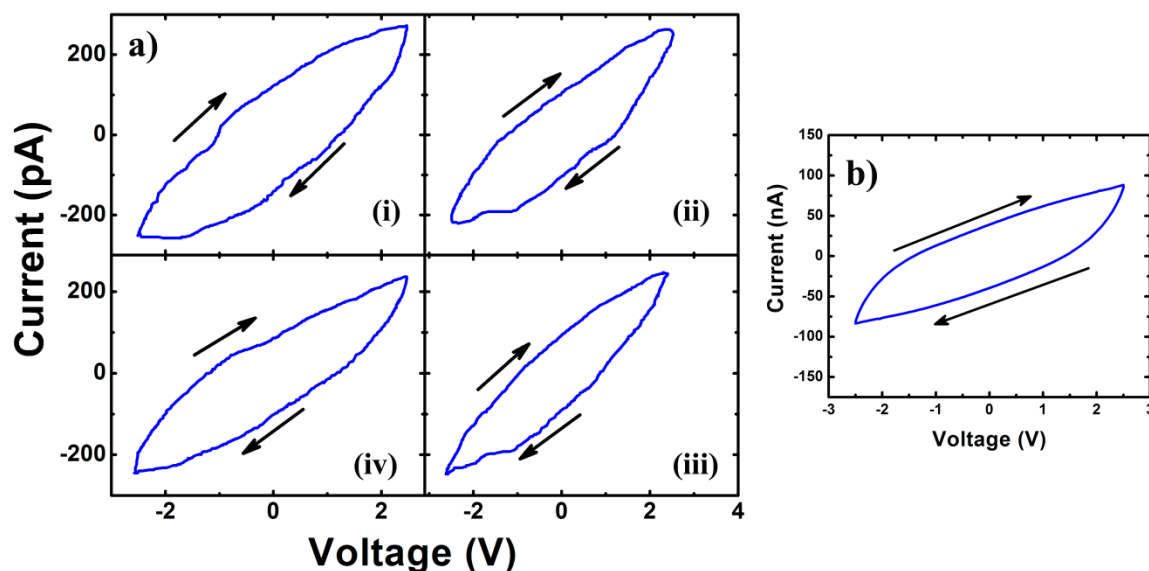


Figure 2-23 – (a) Current vs. Voltage characteristic as measured with the c-AFM. 4 points were measured at the corners of a 100nm by 100nm square. (b) Current vs. Voltage characteristic of macroscale devices.

The conduction models for the c-AFM measurements are similar to the macroscale devices. The high and low conduction states need to be analyzed separately. Just like the macroscale devices, the high conduction state has a threshold of 1.1V, in which the conduction mechanism switches (Figure 2-24). Direct tunneling occurs below 1.1V. After 1.1V, the barrier changes into a triangular shape, switching the mechanism to Fowler-Nordheim tunneling. In this stage of operation, the electrons are capable of tunneling into the C_{60} molecules.

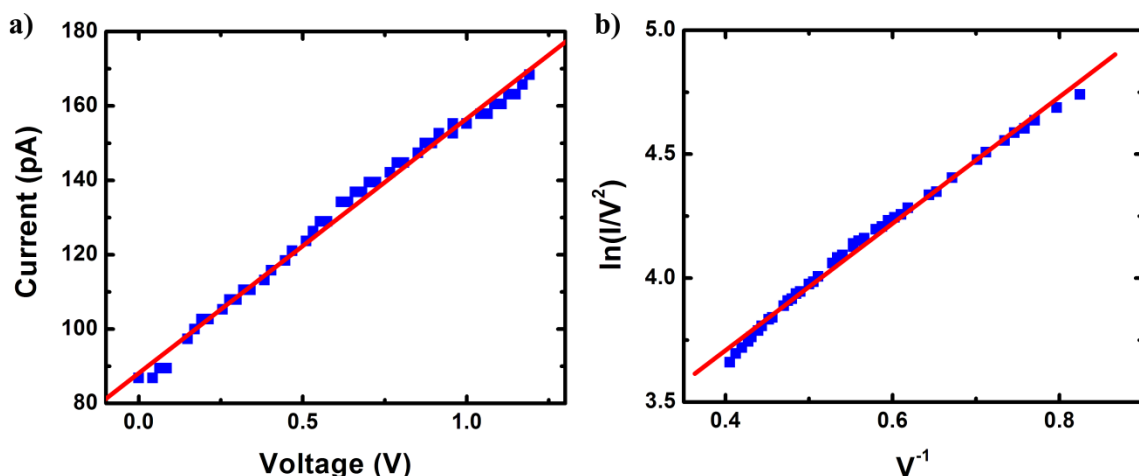


Figure 2-24 – (a) Fit for direct tunneling from 0 to 1.1V. (b) Fit for Fowler-Nordheim tunneling from 1.2 to 2.5V. The blue squares represent the experimental data and the red line represents the fit.

Also similar to the macroscopic devices the low conducting state is divided into two regions: above +1.6V Fowler-Nordheim is the dominant mechanism and below +1.6V, direct tunneling is dominant with a 'kink' at +1.15V (Figure 2-25). Just as with the macroscopic devices, the 'kink' is associated with charging of C_{60} near the ITO contact (bottom contact) during the applied voltage of +2.5V.

The lack of scaling due to field enhancement from the AFM tip is supported by the conduction models in both the high and low conducting states. In the high conducting state, the threshold needed to switch the conduction from direct to Fowler-Nordheim tunneling occurs at a lower voltage than for the macroscopic devices (1.15V vs. 1.3V). This suggests that the barrier is smaller for the c-AFM measurements due to the field enhancement, supporting our argument the low conductivity state lower threshold voltage for switching between Fowler-Nordheim and direct tunneling (1.15V vs. 1.3V); along with the reduction in the 'kink' voltage for the direct tunneling fit (1.15V vs. 1.35V). Despite the lack of scaling, the c-AFM measurement suggests that

the C₆₀ and insulating polymer composite memory devices function at the nanoscale very similarly to the macroscopic devices.

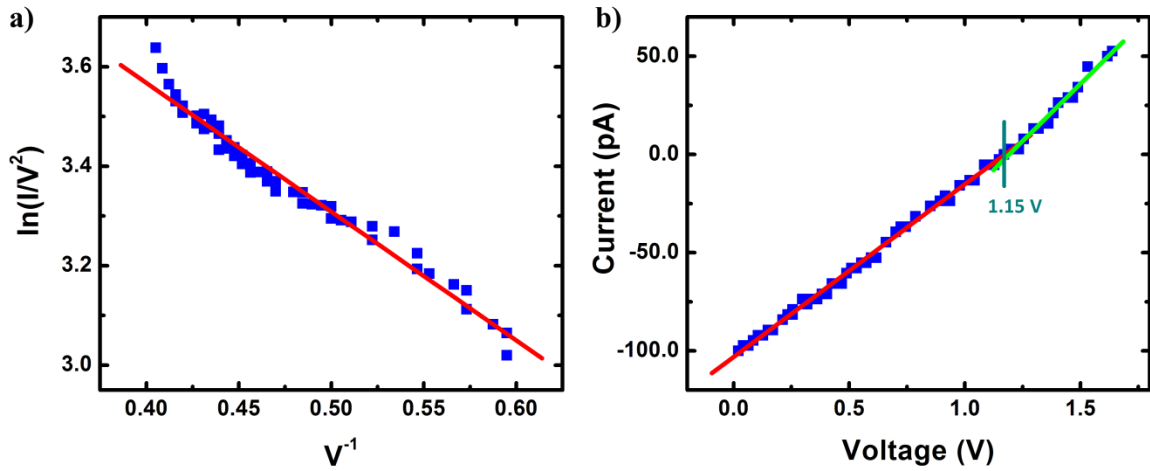


Figure 2-25 – Fits for the low conducting state in the positive region of the downward sweep of Figure 2-23a (a) Fit for Fowler-Nordheim tunneling from 2.5V to 1.6V. The blue squares represent the experimental data and the red line represents the fit. (b) Fit for direct tunneling from 1.6V to 0V. The green line represents a direct tunneling fit from the region of 1.6V to 1.15V and the red line the direct tunneling fit for the region of 1.15V to 0V.

2.3.2.2 *Nanoscale Gap Cells*

Device Fabrication

Nanoscale gap cells were fabricated with electron beam (e-beam) lithography onto a silicon substrate with 400nm thermally grown oxide for confirmation of the c-AFM measurements. The devices were fabricated by first cleaning the substrate using a piranha solution. Polymentyl methacrylate (PMMA) was then spin coated onto the substrate and annealed at 190°C for 30 minutes. The annealing step ensures the film is dry to prevent out gassing. The substrate is then placed in an SEM and the pattern is written by rastering the electron beam. The exposed PMMA undergoes a chemical reaction that effectively cuts the polymer chains in the exposed regions. Next, the substrate is submerged in developer called methyl isobutyl kentone (MIBK) which is diluted at a ratio of 1 to 3 with isopropanol (IPA) and agitated. The developer dissolves the modified polymer from the exposed regions, leaving the written pattern as holes in the PMMA film. The substrate is then rinsed with IPA and blow-dried with dry nitrogen. The patterned PMMA functions as a mask for evaporating titanium (Ti) though. After evaporation, a process called lift-off is performed by dissolving the remaining PMMA with a solvent such as a commercial remover from MicroChem called: Nano Remover PG. Dissolving the remaining PMMA removes excess Ti, leaving an array of nanoscale patterns. After the nanoscale contacts were patterned, 30nm of PVP + C₆₀ film was spin coated onto the contacts. Figure 2-26 shows a scanning electron microscope (SEM) image of the fabricated gap cells before spin coating. The gap size was 30 nm, similar to the thickness of the macroscopic devices. The resulting contact area was calculated to be 900 nm².

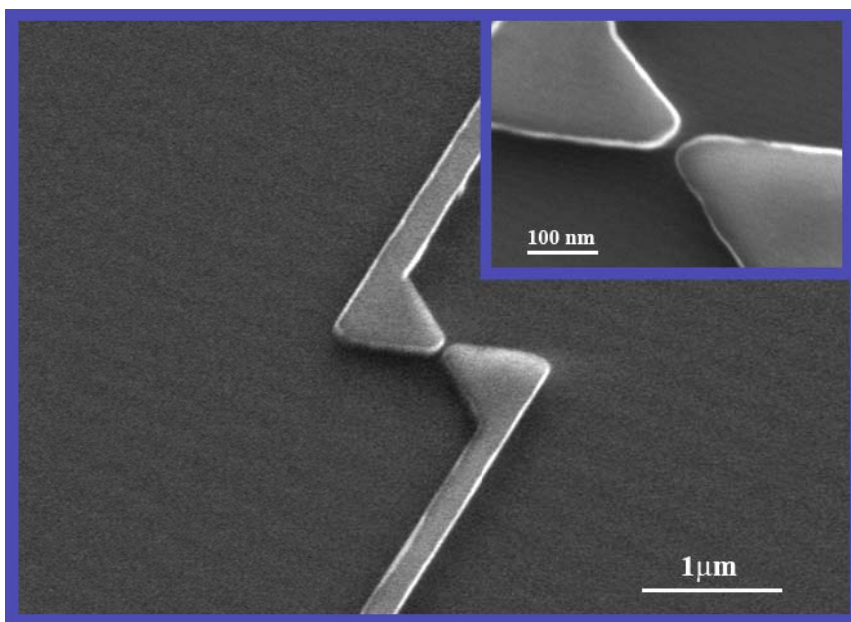


Figure 2-26 – SEM image of the contacts for the nanoscale gap cells, before spin coating.

Comparison to Macroscale Devices

Typical I-V results from the nanoscale gap cells are shown in Figure 2-27a. The I-V curves from the nanoscale gap cell measurements are very similar to both the macroscopic devices (Figure 2-27b) and the c-AFM measurements (Figure 2-27c). As observed in the other two types of devices, the nanoscale gap cells exhibits a large hysteresis, despite a drop in overall current. Similar to the c-AFM measurements, the current values do not scale with the electrode area from the macroscopic to the nanoscale. However, unlike the c-AFM, where field enhancement caused the increase in current, the scaling issue arises from conduction across a larger area than anticipated (see insert in Figure 2-27a). It can be seen from the schematic in the insert that the electric field (E-field) is not completely confined within the gap of the device. Instead, some field lines extend around the gap because the contact's dimensions are comparable to the gap. Hence, the contact area is larger than expected producing larger currents. By approximating the

extra contact area, the current can scale up to the macroscale devices. The current generated by the nanoscale gap cells is smaller than the c-AFM measurements because the field enhancement from the AFM tip has larger effect on the current than an increase of the contact area.

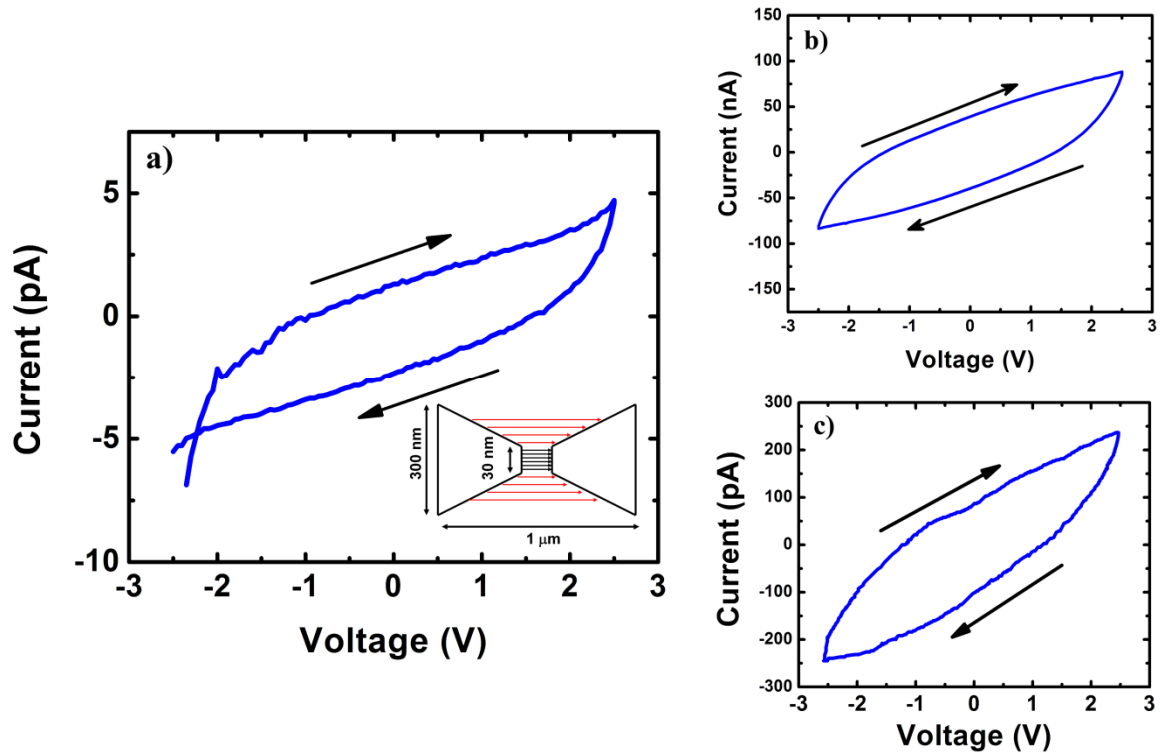


Figure 2-27 – (a) Current vs. Voltage characteristic of the nanoscale gap cells. A schematic of electric field across the gap cell, note the schematic is not drawn to scale. (b) Current vs. Voltage characteristic of macroscale devices. (c) Current vs. Voltage characteristic as measured with the c-AFM.

The conduction models for the nanoscale gap cells measurements are similar to both the macroscopic devices and the c-AFM measurements. The high and low conduction states need to be analyzed separately. Similar to the macroscale devices, the high conduction state has a threshold of 1.3V, where the conduction mechanism switches (Figure 2-28). Similar voltage thresholds between the nano gap cells and macroscopic devices indicate a lack of field enhancement that was present in the c-AFM measurements. After 1.3V, the barrier changes into

a triangular shape, switching the mechanism to Fowler-Nordheim tunneling. In this stage of operation the electrons are capable of tunneling into the C_{60} molecules.

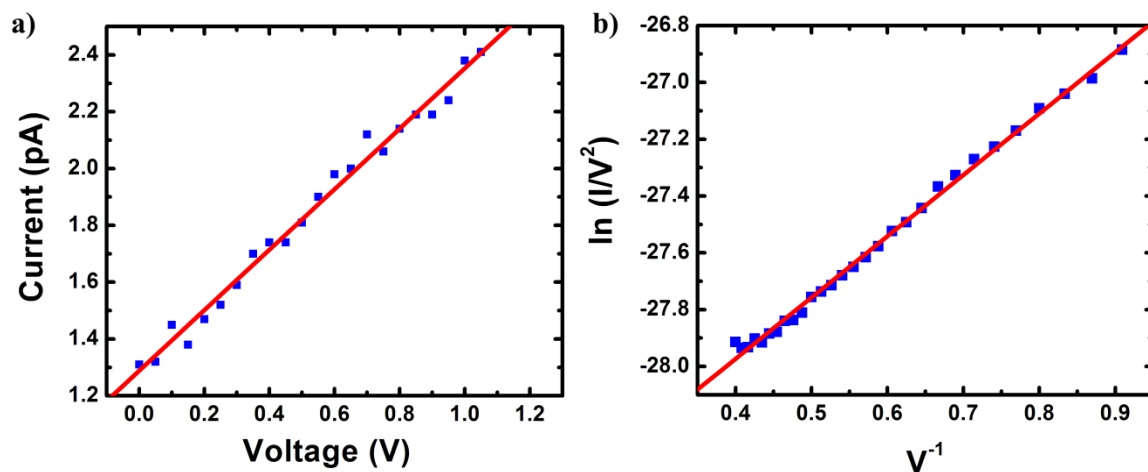


Figure 2-28 – (a) Fit for direct tunneling from 0 to 1.3V. (b) Fit for Fowler-Nordheim tunneling from 1.3 to 2.5V. The blue squares represent the experimental data and the red line represents the fit.

Similar to both the macroscopic devices and the c-AFM measurements, the low conducting state conduction is divided into two regions. Above +1.8V, Fowler-Nordheim is the dominant mechanism and below +1.8V direct tunneling is dominant with a ‘kink’ at +1.5V (Figure 2-29). Just as with both the macroscopic devices and c-AFM measurements, the ‘kink’ is associated with charging of only C_{60} near the negative contact (identical to the bottom contacts for both the macroscale devices and c-AFM measurements) during the applied +2.5V.

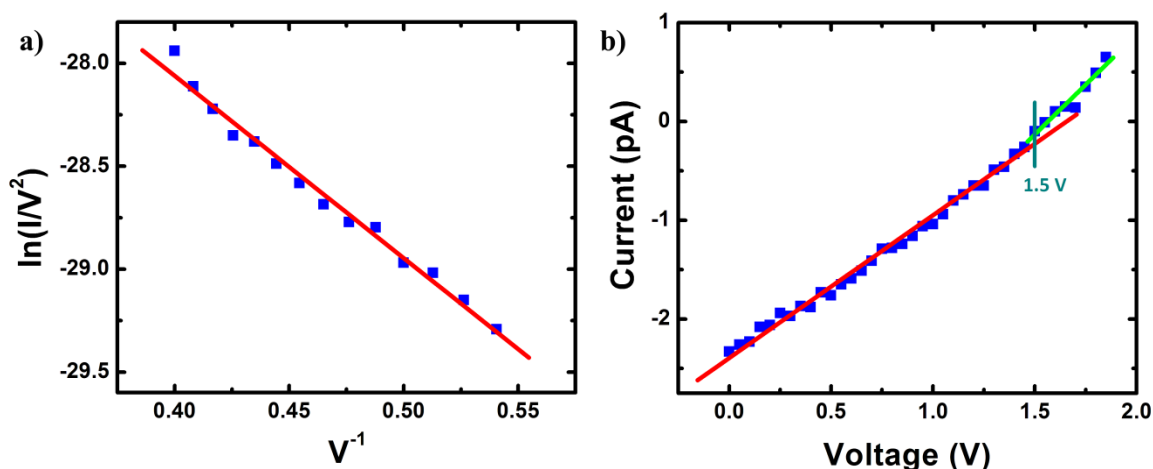


Figure 2-29 – Fits for the low conducting state in the positive region of the downward sweep of Figure 2-27a. (a) Fit for Fowler-Nordheim tunneling from 2.5V to 1.8V. The blue squares represent the experimental data and the red line represents the fit. (b) Fit for direct tunneling from 1.8V to 0V. The green line represents a direct tunneling fit from the region of 1.8V to 1.5V and the red line the direct tunneling fit for the region of 1.5V to 0V.

The lack of scaling from the distribution of electric field is supported by the conduction model in low conducting state. Based on the fits for the low conductivity state, the ‘kink’ voltage is higher than the macroscale devices due to charging of C_{60} outside the nano gap, contributing to larger screening voltages than expected. Unlike the c-AFM measurements, there is no field enhancement or other phenomena that could increase the current or lower the threshold voltage for switching from Fowler-Nordheim tunneling to direct tunneling. Thus, the increase in current could only arise from a larger contact area than expected. In conjunction with the c-AFM measurements, the nanoscale gap cells demonstrate that the C_{60} and insulating polymer composite memory devices can function at the nanoscale.

Both the nanoscale and macroscale measurements exhibit similar symmetrical I-V curves with a discernable hysteresis, indicating screening of applied voltage from charge storage within the C_{60} molecules. In addition, the transport mechanisms remained same when the

memory devices were scaled down from the macroscale to the nanoscale, as summarized in Figure 2-30. In the high conducting state, the devices exhibited direct tunneling below a voltage threshold of +1.3V for both the macroscale device and the nano gap cells and +1.1V for the c-AFM measurements. Above the threshold, Fowler-Nordheim tunneling occurs, allowing the C_{60} molecules to charge. The difference in the c-AFM measurement threshold is attributed to field enhancement from the c-AFM tip. In the low conducting state, Fowler-Nordheim dominates above +1.8V for both the macroscale devices and the nanoscale gap cells, and +1.16V for the c-AFM measurements. Direct tunneling is the primary mechanism below +1.8V for both the macroscale devices and the nanoscale gap cells, and +1.16V for the c-AFM measurements. A 'kink' is present in the fits for the direct tunneling model for the macroscale and nanoscale measurements. The macroscale devices had a 'kink' at +1.35V, while c-AFM measurement showed a 'kink' at 1.15V and the nanoscale gap cells had a 'kink' at 1.5V. The differences in 'kink' voltages are attributed to different device geometries.

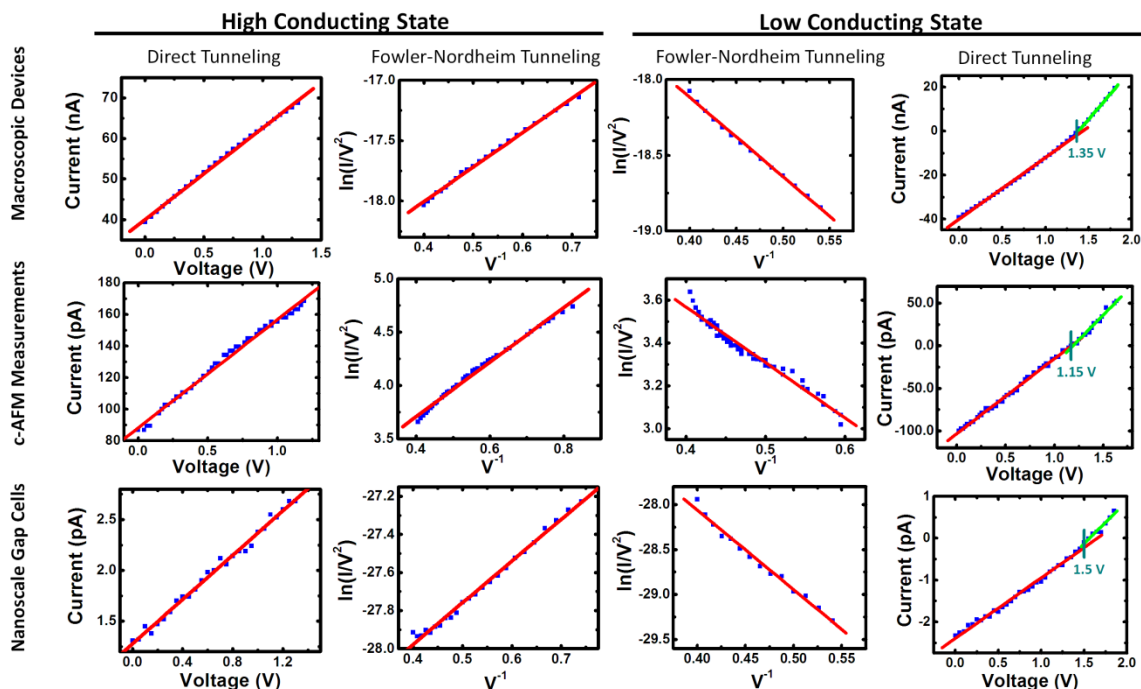


Figure 2-30 – A summary of the fits for both the high and low conducting states for (a) macroscopic devices, (b) c-AFM measurements, (c) nanoscale gap cells. The high conducting state has a threshold above which the conduction mechanism switches from (i) direct tunneling (ii) to Fowler-Nordheim tunneling. The low conducting has a threshold which the conduction mechanism switches from (iii) Fowler-Nordheim tunneling (iv) to direct tunneling. During direct tunneling another threshold exists where the current flips direction for the macroscopic devices (1.35V), c-AFM measurements (1.15V), and nanoscale gap cells (1.5V).

2.4 Conclusion

We have demonstrated a memory effect in the form of a high and low conduction states in the single layer PVP + C₆₀ devices. The use of C₆₀ molecules as the charge storage medium and the ability to disperse them uniformly in an insulating polymer matrix using a solution-based technique is promising for high storage density, large area devices. Memory operations at high and low frequencies have been demonstrated and reveal that read-write-erase operations are possible. The Raman and C-V measurements also indicate that C₆₀ molecules store the charge and not the polymer. Conducting AFM and nanoscale gap cells analysis also indicate that the memory effect persists at the nano-scale. In addition, the conduction mechanisms translate

across scaling from the macroscale to the nanoscale. The tunneling mechanisms are independent of temperature and thus it is important to observe any temperature dependence on the operation of our devices. We will go back to the conduction mechanisms and look at the device operation with respect to temperature, and try to confirm temperature independence in Chapter 4.

While the single layer devices exhibited a distinguishable hysteresis and capability to store information, the 75nA difference between the two states is expensive, in terms of both real estate and power consumption, to differentiate in a microchip configuration. The relatively small 75nA hysteresis is due to uniformly distributed C_{60} molecules, which also store charge uniformly throughout the film thickness. Therefore during an erase (-2.5V) operation, the C_{60} molecules near the negative polarity contact neutralize but the molecules near the positive polarity charge which leads to continued screening. As a result, the single layer devices are only useful for demonstrating the memory effect from charge storage in C_{60} molecules. Instead, a multi-layer device structure introduced in Chapter 3 where a capping layer prevents charge injection from the top electrode can yield hysteresis with μA instead of nA by ensuring that the entire PVP + C_{60} layer is charged or discharged. This effectively gives a 10^3 difference in the current associated with each state. The larger hysteresis allows for cheaper and easier differentiation between the state and therefore significantly closer to a commercially viable universal memory technology.

2.5 References

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Chapter 3 Multi-Layer Organic Memory Devices

3.1 Introduction

In Chapter 2, a memory effect in organic materials, fabricated using C_{60} fullerene molecules dispersed in an insulating polymer, was demonstrated. The memory effect was measured by sandwiching the polymer/ C_{60} layer between two Al electrodes. It was demonstrated that the hysteresis in the I-V sweep was due to charge storage and retention in C_{60} molecules at room temperature. Unfortunately, the current values between the high and low conducting states were low (~ 75 nA), making it difficult to distinguish between the two states. Furthermore, information regarding the stability of the polymer/ C_{60} memory devices was not reported. As such, the single layer memory devices are only useful for demonstrating the proof of principle that such devices are feasible.

In this Chapter, we demonstrate that it is possible to improve the difference between high (few micro-amps) and low (less than few pA) conduction states in our C_{60} /insulating polymer memory devices by adopting a three layer device structure. Our inspiration for the multi-layer structure comes from flash memory technologies as described in Chapter 1 [1-5]. In flash memories, a floating gate is isolated by two insulating layers, with one layer thin enough to allow for hot carrier injection and Fowler-Nordheim tunneling. We adapt this structure by incorporating a thin (~ 5 nm) polystyrene capping layer between the polymer/ C_{60} (also referred to as nanocomposite throughout this Chapter) and the top electrode. Just as in the flash memories, the storage medium (C_{60} in our case) is physically isolated from the metal contacts while the matrix retains the ability for current to flow and allow charging/discharging of the isolated C_{60} molecules. We found that the multi-layered devices possess significantly larger hystereses as compared to the single-layer devices while also enhancing the stability of the devices. Specifically, the hystereses in the multi-layer devices are on the order of 10^3 and can be

preserved up to 85°C. Furthermore, memory retention tests show that it is possible to preserve a state even after annealing at 85°C for 30 minutes.

3.2 Device Fabrication

The three layer memory devices were fabricated in the cross-point architecture as shown in Figure 3-1. The Al electrode width and thickness were 2 mm and 90 nm, respectively. Two types of devices were fabricated in order to investigate the role of C₆₀ molecules in charge storage, one with pure PVP (Figure 3-1a) and the other with PVP+ C₆₀ nanocomposite (Figure 3-1b). Initially, the bottom electrode Al strips were thermally evaporated through a shadow mask at a base pressure of 1×10^{-6} Torr onto clean glass substrates. Subsequent to Al evaporation, a ~30nm of poly (4-vinyl phenol) (PVP) for the pure polymer layer and ~30nm thick layer of PVP+ C₆₀ nanocomposite were spin coated (7400 rpm) on top. The concentration of C₆₀, PVP and solvent was 0.5mg of C₆₀ in 25mg of PVP in 1 ml of isopropyl alcohol (concentration of C₆₀ in solution is 2% by weight). As shown in Chapter 2, our calculations and measurements demonstrate that the percolation threshold of C₆₀ in PVP is ~16%. Therefore, at 2%, we expect the C₆₀ molecules to be completely isolated from each other. Finally, the PS capping layer (thickness ~5nm) was deposited on top by dissolving 10 mg of PS in 1 ml of toluene and spin coating the solution at 7000 rpm. The thickness of the PS layer was confirmed by spectroscopic ellipsometry. After the deposition of the three layers, the substrates were replaced in the thermal evaporator and gold electrodes (90 nm thick and 2 mm wide) perpendicular to the bottom electrodes were deposited on top, completing the cross point architecture. The motivation for using Au electrodes on top was to limit the possible effects of Al oxidation at the interface or surface from exposure to atmosphere.

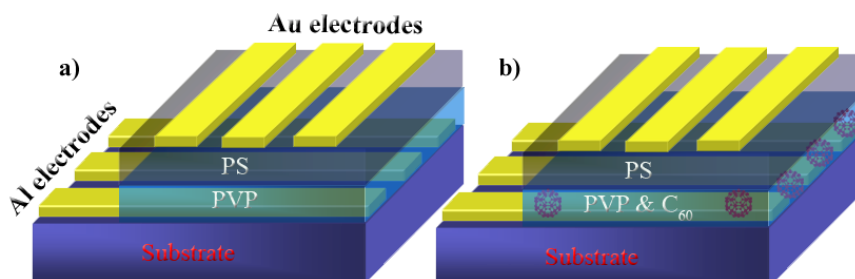


Figure 3-1 – Multi-layer device structure for (a) pure PVP and (b) PVP + C₆₀ nanocomposite

3.3 Structural Characterization

3.3.1 Scanning Electron Microscopy

The interface between the PS and PVP + C₆₀ nanocomposite can greatly affect the current flow through the device. For example, if the polymer layers do not adhere well to each other, then voids could be created between them, which could severely retard the current flow. Analyzing the interface between two polymers is challenging but some basic information about the adhesion of the polymers can be obtained from cross-sectional SEM (x-SEM). x-SEM involves cleaving a cryogenically cooled sample and mounting it perpendicular to the electron beam. However, because both PS and PVP are insulating polymers, charging of the sample leads to washout, limiting the spatial resolution. To help minimize this, gold was thermally evaporated on both sides of the polymer sample, as depicted in Figure 3-2. The sample was prepared by first evaporating 300nm of gold onto a Si substrate. Next, the PVP + C₆₀ nanocomposite was spin coated at 1000 RPM from a concentrated solution (100mg PVP in 1ml of isopropanol) followed by spin coating (1000 RPM) of the PS layer, also from a concentrated solution (100mg PS in 1ml of toluene). The low spin speeds and concentrated solutions ensured that polymer layers were microns thick to allow observation in the SEM. The samples were then allowed to dry overnight in an oven at 70°C to ensure complete evaporation of the solvent. Gold was subsequently thermally evaporated onto of the PS layer. The sample was then carefully submerged in liquid

nitrogen (LN_2). The thermal mismatch between the gold and the Si causes, the sample to lift off the substrate. The film is then cleaved and mounted vertically on an SEM stud. Carbon tape was wrapped around the sample to enhance discharging of electrons from the beam.

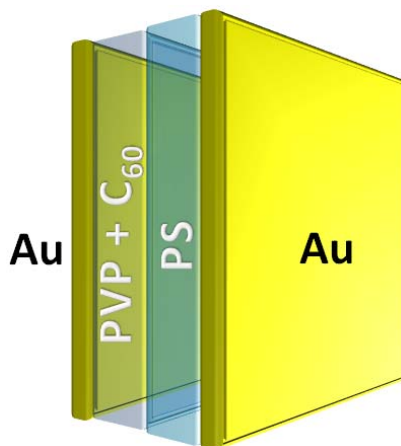


Figure 3-2 – Schematic of x-SEM sample, the two gold layers help minimize charging.

The x-SEM images obtained from the multi-layer samples are shown in Figure 3-3. In Figure 3-3a, the polymer interface is clearly visible using the secondary electron (SE) detector. To confirm the boundary of the gold and polymer, the back scattered electron (BSE) detector is used in Figure 3-3b. Since gold is heavier than carbon, Au atoms have a larger cross sectional area allowing for increased number of electrons to be elastically scattered towards the BSE detector. This creates a strong contrast between the gold (bright regions) and the polymer layers (dark regions). This advantage is highlighted on the PS side in Figure 3-3b where some gold had flaked off during the cleaving process in LN_2 and is clearly visible as bright region. An enlarged image of the interface is shown in Figure 3-3c. The image was taken with a combination of the SE detector and the BSE detector, mixed at a ratio of 75% SE and 25% BSE. By overlaying the images for both detectors, the proposed interface can be confirmed to be from the two polymers. This was additionally confirmed by the BSE image in Figure 3-3d where

the interface appears to be continuous without any obvious voids or defects. Thus, from this rather low resolution imaging analysis, it is possible to conclude that there is reasonably good adhesion between the two polymers, allowing for efficient current flow between the polymer layers. However, a more careful analysis using transmission electron microscopy (TEM) analysis is needed for obtaining detailed information regarding the interface. Although the focus of this work is to understand the electronic properties of the organic memory devices, better structural analysis using a TEM could be one of the topics for future work.

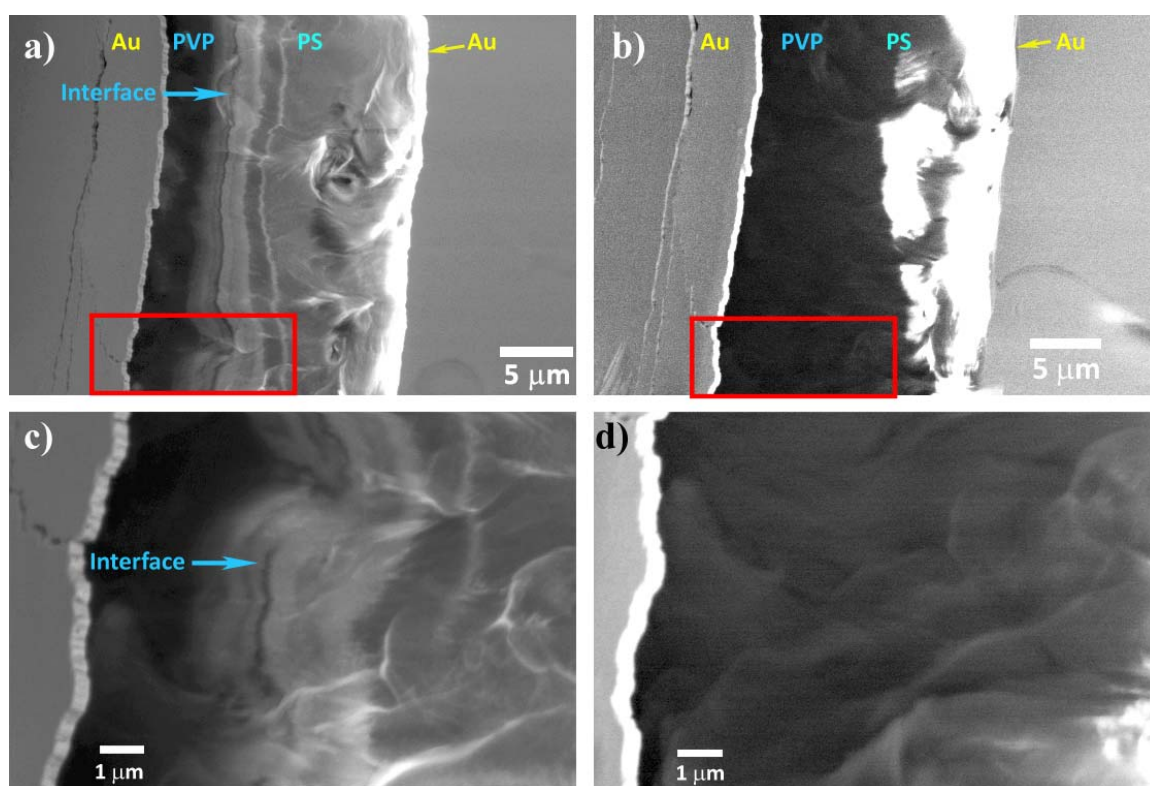


Figure 3-3 – Cross sectional SEM images of the multi-layer polymer interface. (a) Image using secondary electron (SE) detector. (b) Image using backscatter electron detector (BSE). (c) Zoomed image of figure (a) (outlined in red) and taken with a mixture of SE and BSE images at ratio of 75:25. (d) Zoomed image of figure (b) using the BSE detector.

3.3.2 Atomic Force Microscopy

In Chapter 2, atomic force microscopy (AFM) was used to show the relative smoothness of the single layer- PVP + C₆₀ blend film. Similarly, AFM is used to determine if the inclusion of the PS capping layer in the multi-layer devices introduces any additional roughness. As in the case for the single layer, the multi-layer organic films are well adhered and smooth with an average roughness ranging from 3–5 nm as determined by the AFM. The multi-layer film did not show any surface texture and appear relatively uniform and flat throughout as shown in Figure 3-4. In addition, the film showed no evidence of pinholes, indicating that it is homogeneous. This suggests that spin coating PS on top of the PVP + C₆₀ blend film does affect the film. This is expected since the solvent used for spin coating PS is toluene and does not dissolve or affect PVP polymer.

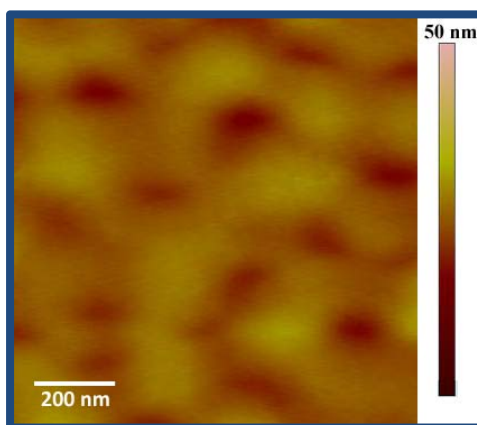


Figure 3-4 – Atomic force microscopy (AFM) image of the top surface of a multi-layer film consisting of PS polymer on top of PVP + C₆₀ blend layer. Images were obtained using a Digital Instruments Nanoscope AFM in tapping mode at a frequency of 0.3 kHz. The root mean square roughness extracted from AFM was ~3 – 5 nm.

3.4 Electrical Characterization

3.4.1 Current vs. Voltage

Having deposited uniform thin films, the next step was to characterize their electrical properties. We began by measuring the current – voltage (I–V) characteristics of the multi-layered devices. The I–V characteristics from the layered cross-point devices are shown in Figure 3-5. The bottom electrode is grounded and voltage on the top electrode was swept from + 3V to –3 V. Typical I–V characteristic from the pure Al/PVP/PS/Au devices is also shown in Figure 3-5 where it can be clearly observed that in the absence of C_{60} molecules, no hysteresis is found. In contrast, for the multi-layer device with the PVP + C_{60} nanocomposite layer, a distinct hysteresis at negative voltages can be observed. It can also be observed that the current increases at positive voltages for the polymer only devices, in contrast to the devices containing C_{60} molecules. Based on our analysis of the single-layer memory devices in Chapter 2, charge injection from the Al electrode into the polymer can be described by direct tunneling at low fields and by Fowler-Nordheim tunneling at high fields. It should be mentioned that in the polymer only devices, hystereses can be measured initially but disappears after the first 2–3 voltage sweeps. This is attributed to the presence of electronegative OH molecules in the benzene rings of the PVP, which act as traps for electrons. However, in contrast to C_{60} , the OH molecules are relatively unstable and not as electronegative so that repeatable charge storage and discharge is not possible.

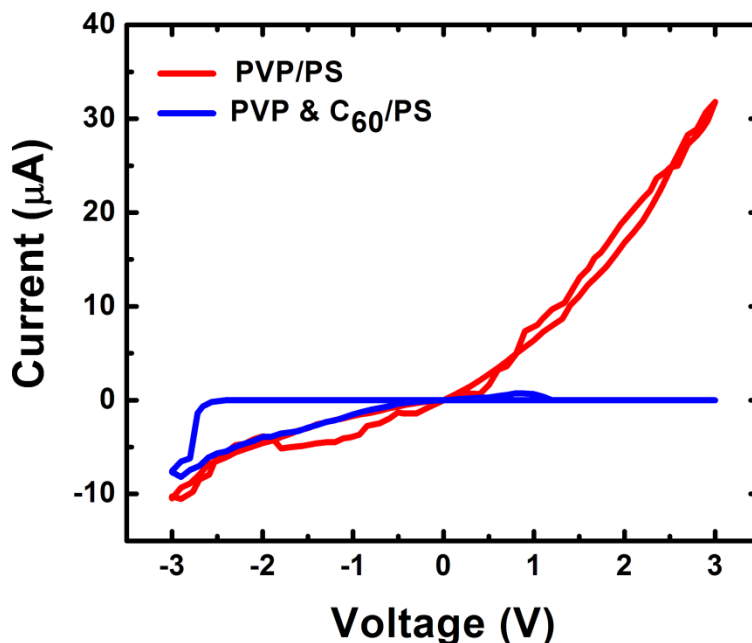


Figure 3-5 – Current vs. voltage plot of both multi-layer devices with one containing pure PVP and the other containing the PVP + C₆₀ nanocomposite.

In order to demonstrate the hysteresis in devices containing C₆₀ molecules more clearly, the I-V curve is replotted in Figure 3-6. The shape of the hysteretic I-V curve is similar to other organic memory devices [6-8]. The appearance of the hysteresis can be described in the following manner with the aid of Figure 3-6. Initially, in the off state at point 1 in Figure 3-6, the measured current value is less than 1 pA (the sensitivity of our measurement unit). As the voltage is increased, electrons are injected from the bottom Al contact into the nanocomposite layer via tunneling through the very thin insulating layer and the measured current increases. The thin insulating layer is from the PVP in which C₆₀ molecules are dispersed. While it is possible that a few C₆₀ molecules are in direct contact with the Al electrodes, these molecules would not be able to store charge or aid in conduction. Instead, we will focus on the C₆₀ molecules that are embedded in the polymer matrix and not in direct contact with the Al electrodes. Thus, in order for charge to reach the C₆₀ molecules it must be transported through

the insulating matrix first. Some electrons maybe injected directly into the C_{60} molecules where they are essentially trapped due to the high electronegativity of the fullerenes. Other electrons may reach the C_{60} molecules via tunneling through localized states in the PVP. We will discuss this in more detail in Chapter 4. As sufficiently large amounts of electrons are trapped by the C_{60} molecules, the current through the sandwich structure begins to decrease as indicated by point 2 in Figure 3-6. The negative differential resistance in the current at point 2 is attributed to the screening of the applied electric field due to storage of charge in the nanocomposite layer. As the voltage is further increased up to +3V, more of the isolated C_{60} molecules become charged which increases the screening so that the device remains in the low conduction state, as indicated by point 3. In contrast, the absence of charging and therefore screening in the polymer only devices leads to an increase in current at high positive voltages, as indicated by the red curve in Figure 3-5. As the voltage on the multi-layer device containing C_{60} is decreased, the device remains in the low conduction state (shown blown up in the inset of Figure 3-6) until a critical voltage (< -2.5 V) is reached where the C_{60} molecules are discharged, point 4 in Figure 3-6. The discharge of trapped carriers leads to a large increase in the current and the device goes into a high conduction state mode, point 5. Once the device is fully discharged, increasing the voltage leads to a steady decrease in current, which follows a different path back towards point 1, as indicated by the arrows in Figure 3-6, giving rise to a hysteresis.

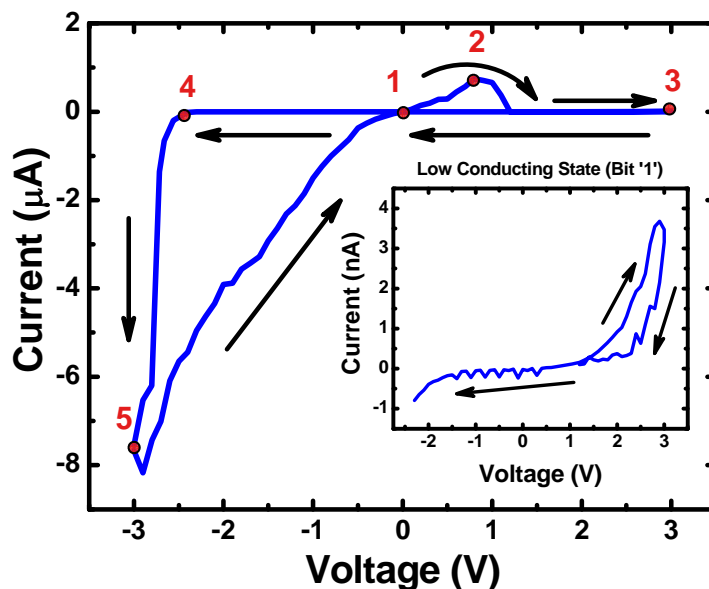


Figure 3-6 – I-V plot of the PVP + C₆₀ nanocomposite multi-layer memory device. The curve starts at point 1 at zero volts. At point 2 the voltage is high enough to allow for charging of C₆₀ molecules and the current begins to drop as a result. By point 3, all the C₆₀ molecules are charged and the device is operating in a low conducting state. At point 4 the reverse bias is large enough to allow the charged C₆₀ molecules to discharge, bringing the device into a high conducting state, point 5. The low conducting state showing very low current values in the off state is given in the inset.

3.4.2 C₆₀ Charging Levels

Since the charging of the C₆₀ molecules is determined by the maximum positive voltage applied, it should be possible to vary the characteristics of the observed hysteresis because the discharge voltage depends on the amount of screening. This is useful in memory devices for writing multiple bits per cell. That is, by applying different threshold voltages, it is possible to monitor the different states of the same memory cell. This is one of the main tricks used in flash memory technology to increase the storage capacity [1]. The variation of the hysteresis as a function of the maximum positive voltage applied is shown in Figure 3-7a. Although there are

some fluctuations in the data, the trend of increasing discharge voltage (Erase V_T) with write voltage can be clearly observed in Figure 3-7b. It can be seen from the Figure 3-7a that for maximum positive voltages above + 1.6V, hysteresis in the I–V characteristics can be observed. Furthermore, the discharge voltage also depends on the maximum positive voltage applied. At a maximum applied voltage of + 1.4 V, no hysteresis is observed. It is interesting to note that the overall current through the device in all the measurements is similar, indicating that carrier injection and transport through the polymer is unaffected. If however, the number of carriers injected into the polymer is the same, then the amount charged C_{60} molecules should be the same in all measurements. This is clearly not what is observed in Figure 3-7. The fact that the C_{60} molecules are not charged at + 1.4 V indicates that there is an energy barrier (β) between the PVP polymer and the fullerenes which is between $1.4 \text{ eV} < \beta < 1.6 \text{ eV}$. The charging energy is consistent with values obtained from spectroscopy for C_{60} molecules [9].

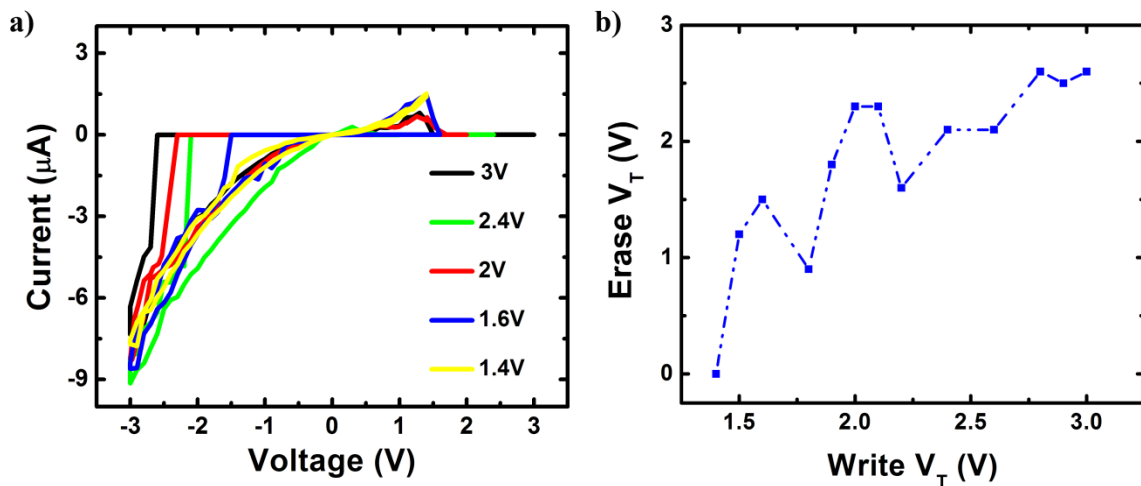


Figure 3-7 – (a) The variation of discharge voltage with maximum positive voltage applied. The listed voltages are the maximum positive voltages applied. No hysteresis is observed when the maximum applied positive voltage is + 1.4 V, indicating no C_{60} molecules are charged. (b) The variation of the erase threshold voltage (V_T) varies with the maximum write voltage.

3.5 Memory Operation, Switching, and Stability Properties of Multi-Layer Devices

3.5.1 Waveform – Read-Write-Erase-Cycles

In order to translate the hysteresis into memory device operations, read-write-erase functions were performed. The behavior of a device during the programming of the various states is plotted in Figure 3-8. Relatively slow voltage pulses of 4 ms were used to program the different functions. A voltage of -1V was chosen to read the '0' or '1' states. At this voltage, the difference between the on and off states (on/off ratio) is greater than three orders of magnitude, making them easily distinguishable. More importantly, the read current is in the micro-amps, which allows it to be read without requiring additional amplification. Initially, a $+2.5\text{V}$ pulse was applied in order to write the '1' state. After the voltage pulse, the device was disconnected for 5s when a read pulse of -1V was applied. It can be seen from Figure 3-8 that the device after the read step remains in the low conduction state. In order to erase the charge from the write step, a -3V pulse was applied which switches the device into the high conduction state, as demonstrated by the large current measured during this step. The erasure of the device was confirmed by applying a voltage pulse of -1V which shows that the device is in the high conduction state ('0' state) with a current value of $-1 (\pm 0.5) \mu\text{A}$, as shown in Figure 3-8. The characteristics in Figure 3-8 indicate that the device is programmable.

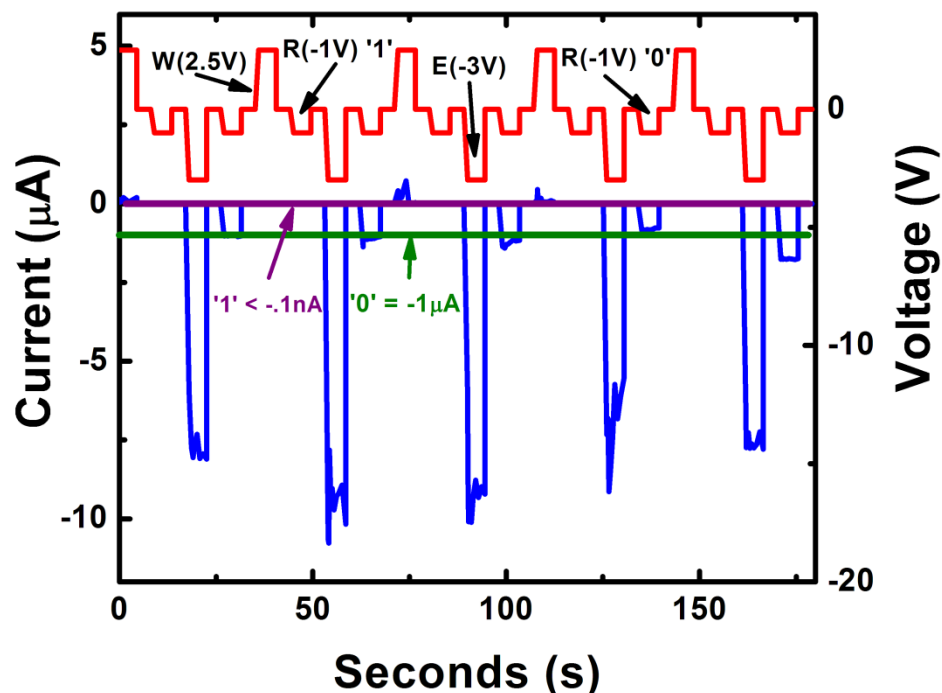


Figure 3-8 – Current versus voltage response of the memory devices during write-read-erase-read voltage cycles. Initially a voltage pulse of + 2.5V was used for writing (W) which can be read (R) by applying -1 V ('1' bit, low conductance). This information can be erased (E) by applying a voltage pulse of -2.5 V. The fact that the original data has been erased can be confirmed by applying -1 V to read ('0' bit, high conductance). The ON and OFF states can be clearly distinguished by the large current difference indicated by the two horizontal lines.

3.5.2 Response time

In order to demonstrate that the devices can switch at high speeds, we also performed nanoscale time measurements by applying a -2.5V pulse (representing the Erase operation) to the device and measuring the delay time. A typical result is shown in Figure 3-9. In agreement with the results of the single layer devices in Chapter 2, we find switching time of the order of 10ns, indicating that fast switching is also possible in the multi-layer devices. The capability of operating at high frequencies suggest that the PVP + C₆₀ memory devices may perform well, even in applications with demanding speed consternates, such as replacing the DRAM in a computers main memory.

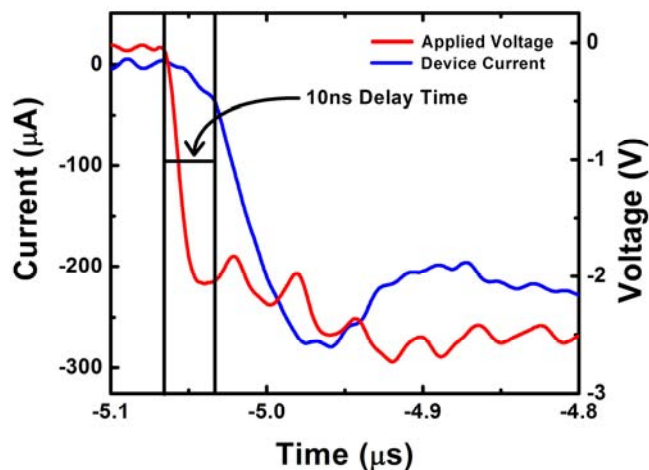


Figure 3-9 – Measured response time of 10ns for the Au/PS/PVP+C₆₀/Al multi-layer memory devices.

3.5.3 Data Retention

In order to investigate the non-volatile nature of the memory devices, devices were read for 2 hours at every minute to monitor both the OFF ('0' bit) and ON ('1' bit) states. The result is shown in Figure 3-10. The devices were tested by initially applying a -2.5V pulse for 10ms to erase all the data. The ON state was obtained by applying a 10ms pulse of +2.5V and then read by applying a 10ms pulse of -1V every minute and simultaneously monitoring the current. The OFF state was obtained by applying a -2.5V pulse for 10ms. The device was then read by applying a 10ms pulse of -1V every minute for 2 hours and simultaneously monitoring the current. After each read pulse in both states, the power to the device was removed by disabling the voltage input. No deterioration in the performance of the memory device was observed. The difference between the ON and OFF states remained relatively constant at 10^3 , indicating data retention. The time trend is in agreement with the single layer devices in Chapter 2. However, the off to on ratio is three orders of magnitude higher than the single-layer device.

The high on/off ratio makes the multi-layer memory device easier to read, bringing the PVP + C₆₀ memory devices closer to commercialization.

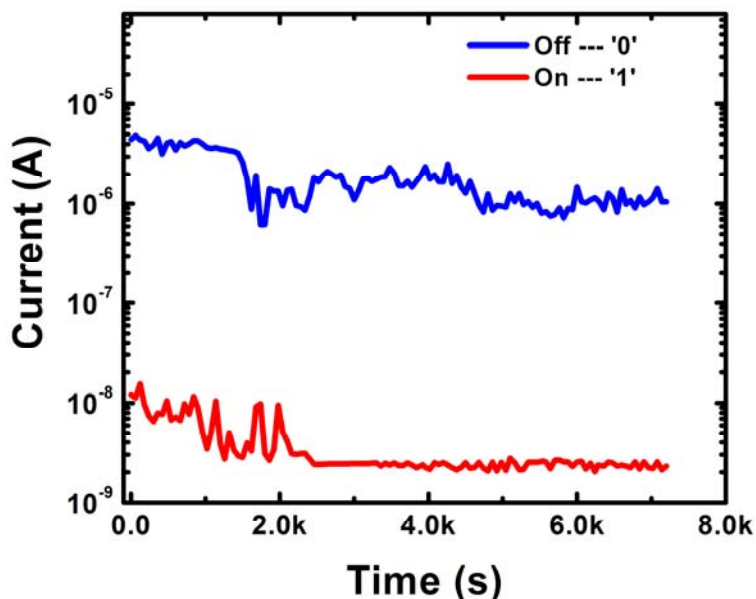


Figure 3-10 – Data retention graph for two hours. The difference between the '0' bit and '1' bit is consistent at 10³.

3.5.4 Thermal Stability

Now we discuss the stability of our devices, an issue with all organic devices. In addition to concerns about environmental stability, there is also a question whether the devices can operate at temperatures near the glass transition temperature of PS (~ 100°C). The I–V curves measured at three different temperatures are shown in Figure 3-11a. It can be seen that the hysteresis is preserved up to 85°C, which is remarkable because the PS begins to soften at this temperature. In addition to stability, we also demonstrate that the multi-layer devices are able to retain data after annealing at 85°C. In order to demonstrate the retention capabilities of these devices, we performed write and erase functions on the device, annealed it at 85°C for 30

minutes and measured the hysteresis. The results of this test are plotted in Figure 3-11b. It can be observed that the device remains in the low conducting state subsequent to annealing at 85°C for 30 minutes after the write step. Similarly, for the erase step, the device remains in the high conducting state after annealing at 85°C for 30 minutes. Longer annealing times could not be tested in this study due to the degradation of contacts. However, this will be one of our focuses in future work. We have also investigated the environmental stability of the devices by storing them at room temperature in ambient conditions without additional protection. We found that the devices are stable even after 5 days and retain their charge over that time (Figure 3-11c and d). This was tested by taking an I-V curve of a device first (depicted in the inset of Figure 3-11c) and performing a write operation afterwards. The device was then stored in ambient conditions for 5 days without additional protection. After 5 days, I-V measurements were taken, the result of which are as shown in Figure 3-11c. The curve starts at 0V and is swept from 3V to -3V. From 0 to 3V, no threshold representing the charging of C₆₀ molecules is observed, because the molecules have retained their charge from 5 days ago and cannot be charged further. As a result, the device starts out in the low conducting state in the I-V curve and does not enter the high conducting state until the erase threshold. Afterwards, the device operates in the high conducting state and recreates the expected hysteresis. When the I-V plot is repeated (Figure 3-11d), the write threshold voltage reappears because the C₆₀ molecules were discharged from the previous I-V sweep. This indicates that the device performance and operation is preserved during the 5 days. In addition, we recently tested devices fabricated over 16 months ago and found that the I-V curves of the multi-layer devices are preserved over that time. Indeed, these devices have been used to carry out the temperature dependence study reported in Chapter 4. The improved environmental stability is attributed to the PS capping layer, which essentially acts as prevention barrier.

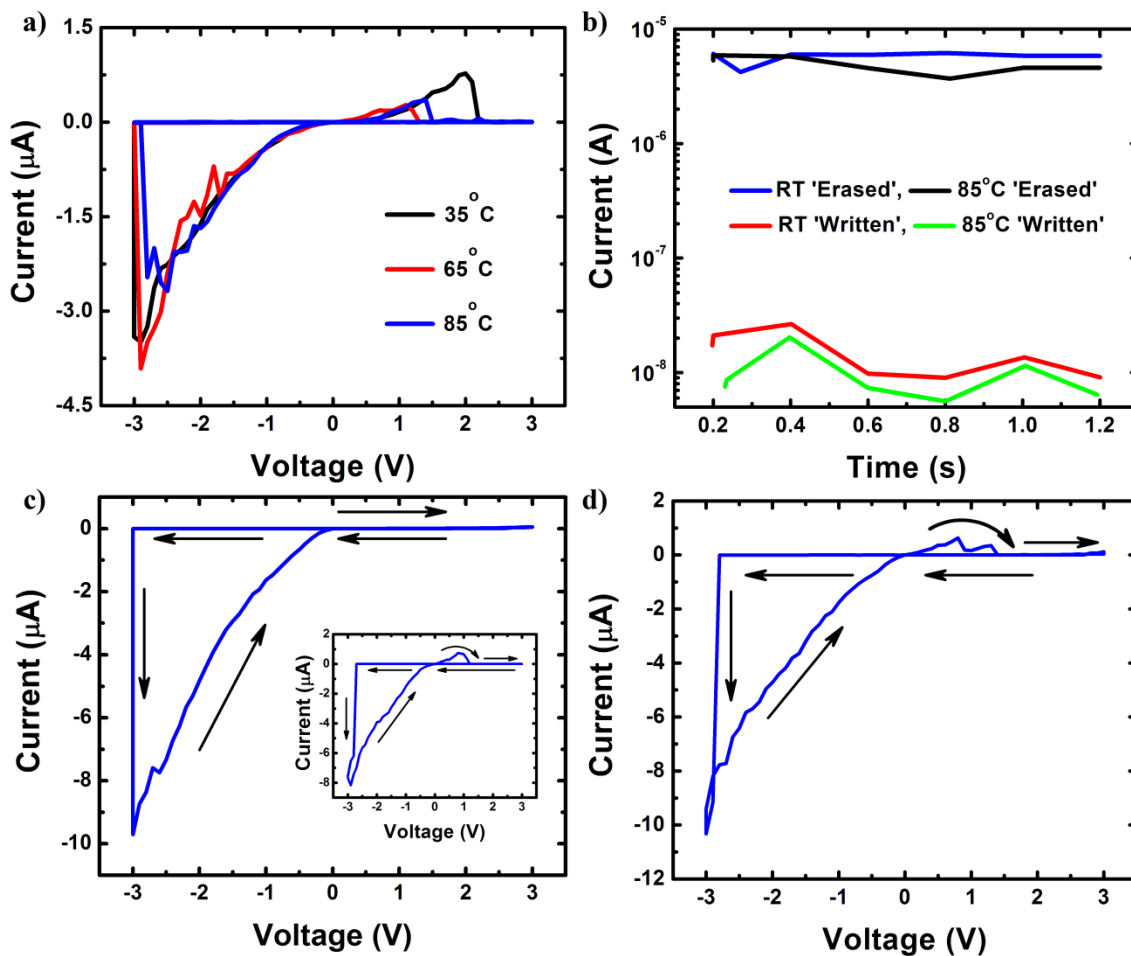


Figure 3-11 – Demonstration of stability and retention in our memory devices. (a) Measurement of the hysteresis at three different temperatures. (b) This graph shows that the device remains in the same state (either written or erased state at room temperature [RT]) after annealing at 85°C. (c) I-V plot of a written device after 5 days, the lack of a writing threshold indicates that the device retained its charge during the 5 days. The inset shows the I-V behavior before being written. (d) I-V plot repeated after 5 days measurement. Writing threshold is present because the device is now in the high conducting state.

3.6 Nano Transfer Printing

The multi-layer memory devices have the potential for commercialization because of their large hysteresis and stability. As a result, they have generated significant interest from venture capitalists to help test the commercial viability of the memory devices. The ideal architecture for a commercial viability memory device is the cross-point architecture [10],

schematically depicted in Figure 3-12. A single bit is stored in a device defined by the crossing of the top and bottom contacts. This design allows for the optimal storage density while minimizing the complexity of accessing each device [10]. The cross-point architecture is identical to the test chips developed for this thesis to study both the single-layer and multi-layer memory devices. However, the devices tested in our study are at the macroscale, and need to be scaled directly down to the nanoscale in order to demonstrate the storage densities needed for commercial viability.

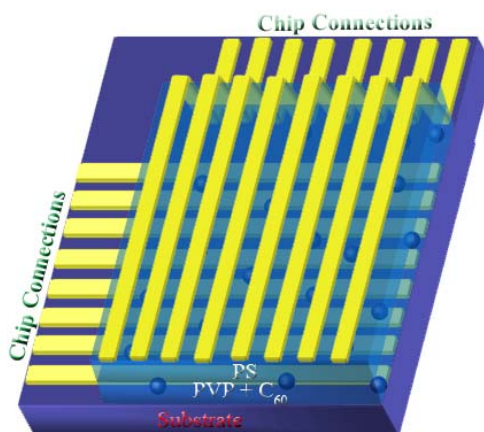


Figure 3-12 – Schematic of the multilayer memory device in the cross point architecture where an actual devices used to store a bit is defined by the intersection of the top and bottom electrode lines.

Development of the cross-point architecture at the nanoscale typically involves some form of nanolithography. However, any type of traditional lithography is difficult on organic materials, especially when involving thin films of polymers. These techniques, such as photolithography or electron beam lithography (E-Beam), utilize a sacrificial layer called a resist to create patterns for use as a mask to deposit the pattern structures. The resist is removed using organic solvents as usually the last step in the process. The removal step can destroy the organic components in the electronic device. For this reason, a purely additive technique such as

nano transfer printing (nTP) is needed for organic electronics [11]. nTP utilizes an elastomeric stamp to transfer patterned metal regions through the use of van der Waals forces on to the surface of a polymer layer, as opposed to using solvents to strip away a resist layer. In order to attempt to make nanoscale devices, we investigated the possibility of using transfer printing for electrodes. The results of our study are reported below. It should be noted that we were largely unsuccessful in this endeavor. However, the knowledge from the failures has been useful in determining alternative paths for deposition of nanoscale electrodes.

3.6.1 Transfer Failures

Before attempting nanoscale transfer, we decided to work with macroscale patterns to understand the stamping process without the added complexity associated with nanoscale patterns. The test pattern used for the macroscale work is shown in Figure 3-13. The pattern was written in photo resist through photolithography on top of a silicon wafer. The pattern was then transferred onto a poly (dimethylsiloxane) (PDMS) elastomer (Sylgard 184 from Dow Corning) by casting and curing against a patterned resist on a silicon wafer (called a master) [12, 13]. The use of an elastomer versus a rigid stamp ensures intimate contact between stamp and the PS surface. The raised pattern on the silicon wafer create patterns on the PDMS stamp.

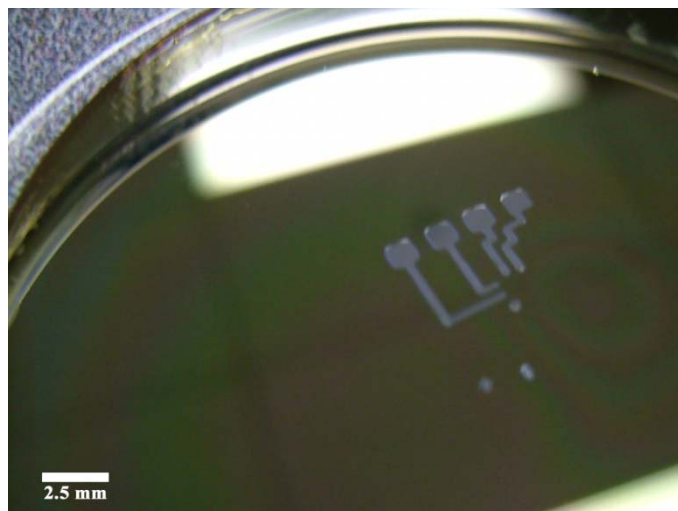


Figure 3-13 – Test pattern used for transfer printing. The pattern is designed to act as macroscale contacts for nanoscale devices. The pattern was written in photo resist on top of a silicon wafer.

Initially, we followed procedures outlined by Rogers et al and others, that involved either using a self assembled monolayer (SAM) layer called 1,8-octanedithiol or oxides to bind with hydroxyl (–OH) groups on the substrate (polymer in our case) surface [14-26]. The use of the SAM layer is motivated by the fact that it contains sulfur groups that bind with gold, transferring the patterned gold from the stamp to the polymer surface. However, solvents used to remove excess 1,8-octanedithiol molecules also attack both PS and PVP layers. As such, we started with the hydroxyl group method. A simple method to determine if OH groups are present, is to investigate the wettability of the surface. The presence of OH groups induces hydrophilicity on the surface. However, since PS is already hydrophilic without any additional treatment, we attempted to transfer gold pattern directly on the PS layer using the oxide-hydroxyl group method. Since gold is a noble metal and does not form an oxide, a thin layer (<5nm) of Al or Ti was evaporated on top of the gold to form the necessary oxide to facilitate binding to the OH groups. Upon exposure of the thin oxide to air, a layer of OH groups should form on the oxide

surface, which could be useful for bonding the gold layer to the hydrophilic PS layer. However, attempts to transfer print without any treatment to the PS layer were unsuccessful as the entire gold layer remained on the PDMS stamp.

In order to create preferential adhesion of the gold to PS as opposed to the stamp, oxygen plasma treatments were used on both the PS layer and the surface of the PDMS stamp (before gold deposition). Oxygen plasma treatment of PS is known to activate its surface and improve wettability [27], creating a stronger bond with the thin oxide layer that is attached to the gold layer. For PDMS, oxygen plasma exposure also creates OH groups [28], however they actually decrease the surface energy between the gold and PDMS, making it more favorable to transfer the gold from the PDMS to the PS layer. Mild success was achieved using oxygen plasma treatment, as can be seen in Figure 3-14. Figure 3-14a is a typical result of a partial transfer and Figure 3-14b shows the stamp after printing. To understand the reason for the partial transfer, optical images were taken before and after printing of the PDMS stamp. Figure 3-14c is a 2.5x magnification image of a PDMS stamp with gold. The gold layer is clearly continuous, as confirmed by the 10x magnification in the inset. However, after transfer, the gold was found to be discontinuous, with some gold remaining on the stamp, as shown in Figure 3-14d. If we zoom in to 10x magnification [inset (i)] and even 50x [inset (ii)] the gold flaking is clearly evident. This is attributed to the surface energy of the PS layer being still just slightly higher than the PDMS stamp and not uniform along the surface, despite attempts to increase it with oxygen plasma treatment.

We then moved to another method using “kinetics” as described by Meitl et al [11]. Meitl uses the kinetics of removing the stamp to determine if a stamp will pick up a layer or transfer a layer to a substrate. That is, if the stamp is peeled quickly then the metal layer is unlikely to stick to the stamp and if peeled slowly the metal is likely to be transferred to the substrate. We adapted this method by rolling the stamp very slowly over the PS layer. However, as before, only partial transfers resulted, similar to Figure 3-14. Finally, we adapted an annealing method described by Wang et al and Hur et al [29, 30]. The annealing method is simply to heat the PDMS above the glass transition temperature of the polymer substrate to enhance adhesion of the electrodes (see description below). We have initiated a collaboration with Dr. Guo’s group at University of Michigan to adapt the annealing method to our process. Our initial results were very positive in that we were able to achieve complete transfer by annealing the stamp while it was in contact with the PS layer, see below.

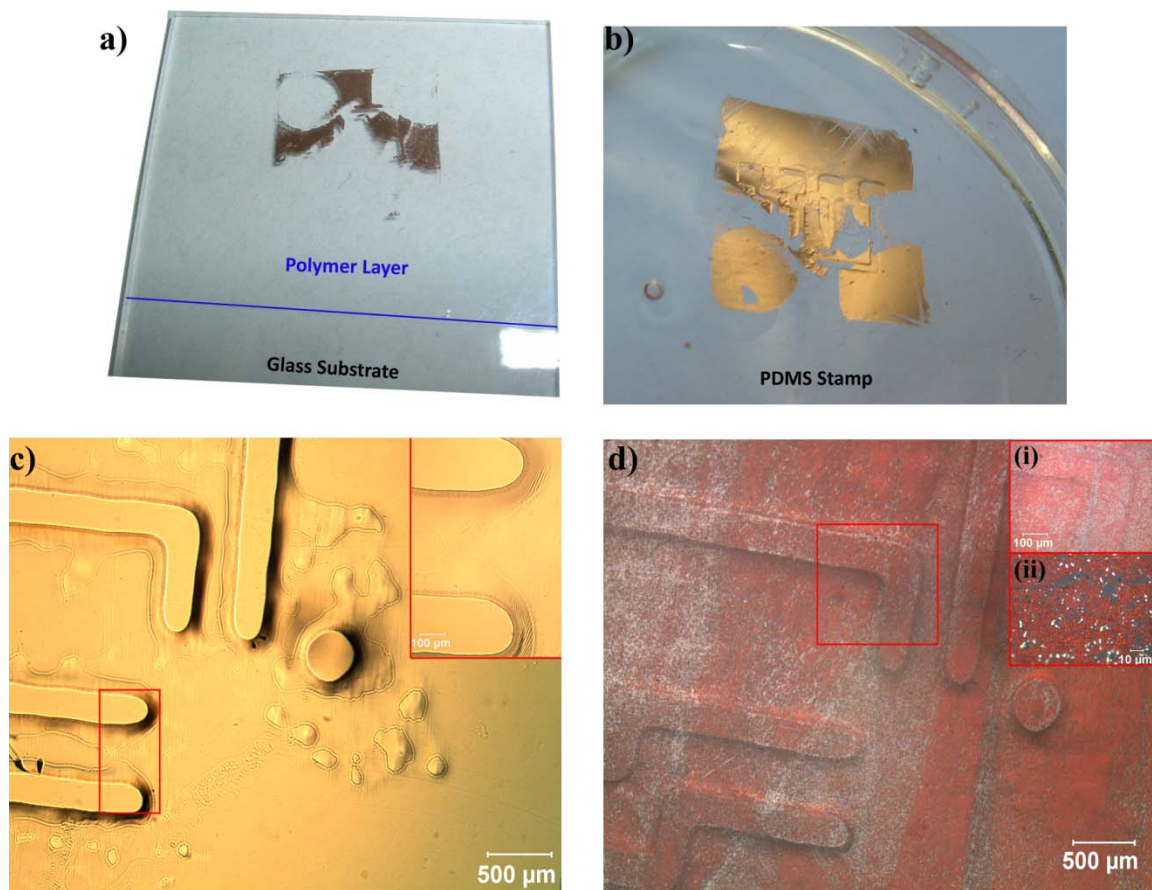


Figure 3-14 – (a) Partial transfer of gold pattern onto PS layer. (b) PDMS stamp after partial transfer. (c) 2.5x magnification of PDMS stamp before transfer with gold evaporated on top. Inset is magnified at 10x. (d) 2.5x magnification of PDMS stamp after transfer. Gold flakes appear. (i) 10x magnification of PDMS stamp after transfer. (ii) 50x magnification after transfer.

3.6.2 Transfer of Electrodes by Annealing Method

The annealing method procedure for successful transfer of electrodes starts with fabrication of the PDMS stamp by casting and curing (60°C for 3 hours). The transfer of top contacts was obtained by following the procedure in Figure 3-15. After removing the stamp from the master, gold was evaporated on the patterned side of the stamp (step ii in Figure 3-15). Next, the stamp was brought into contact with the PS layer and heated to 120°C for 5 minutes. 120°C is above the glass transition temperature (T_g) of PS (100°C). T_g is the threshold

temperature where a polymer softens, becoming elastic and therefore can be deformed easily. The T_g is different and lower than the melting temperature (T_m), where a polymer will essentially melt and flow like ice melting into water but with a higher viscosity. Here, the advantage of using PS as the capping layer is further highlighted, as 120°C is still below the T_g of PVP (130-185°C). This way, the top contacts can be transferred without disturbing the distribution of the C_{60} within the PVP layer. The softened PS layer behaves as glue, increasing the adhesion of the gold layer. Thus, when the stamp is removed (step iv in Figure 3-15), the gold on the raised regions should remain on the PS layer forming the top contacts, completing the device (step v in Figure 3-15).

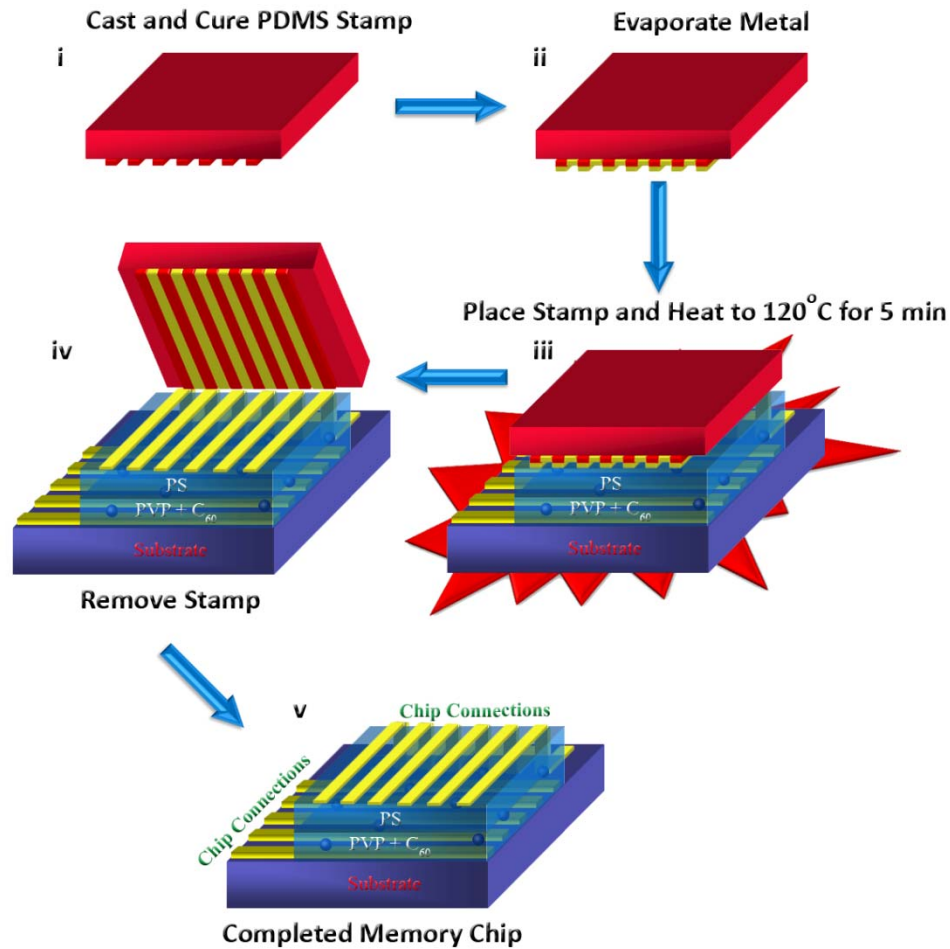


Figure 3-15 – Procedure for stamping on top contacts for the multi-layer memory devices using the annealing method in collaboration with Prof. Guo's group at the University of Michigan.

A macroscale pattern was attempted with the annealing transfer method. The results of the transfer are shown in Figure 3-16. By following the procedure outlined in the previous section, we were successful in transferring the entire gold layer that was evaporated onto the stamp. Gold that was not part of the patterned lines was also transferred because the trenches (space between the lines) were too large. As a result, the region within the trenches also made contact with the PS layer. We do not foresee this to be a major problem in the future when transferring nanoscale lines, because the trenches will be sufficiently small to prevent bowing of

the PDMS stamp so that only the raised regions of the pattern in contact with the PS layer will transfer. This is highlighted by the presence of lines, where the edges did not transfer completely, creating an outline of the patterned lines in the gold layer, as indicated by the arrows in Figure 3-16. Despite the transferring of gold from the trenches, we observed that the gold layer was continuous, ensuring good metal contacts and preventing any open circuits in the top electrodes. While we currently lack the infrastructure to align a nano-pattern, the group at University of Michigan is capable of alignment. As part of ongoing and future work, we will create the nano-pattern masters that are used for casting the PDMS and fabricate the bottom contacts using e-beam lithography. In addition, we will spin on the PVP + C₆₀ blend layers and the PS layers. The University of Michigan group will align and stamp on the nano-pattern of gold. The completed chip will then be used to test the nanoscale operation viability of the multi-layer memory devices.

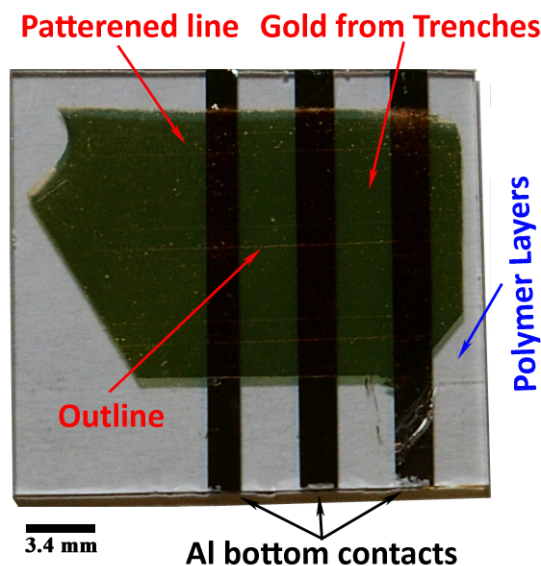


Figure 3-16 – 30 nm gold lines transferred by PDMS stamping. The entire gold are is transferred because the trench (spaces between the lines) were too large.

3.7 Summary

In conclusion, we have described a multi-layer organic memory device based on insulating polymers and C_{60} molecules. The large hysteresis in the I–V curves is attributed to the screening of voltage due to charging of C_{60} molecules. We demonstrated that the hysteresis can be used to perform read-write-erase functions. The hysteresis characteristics can be modified by varying the maximum positive voltage applied. This allows the control of the number of C_{60} molecules that are charged and therefore the screening voltage. This manifests as a variation of the discharge voltage, which could be used to write multiple bits per cell. We also demonstrated that the addition of the PS capping layer in the multi-layer devices leads to enhanced stability and information retention up to 85°C. Finally, we developed a procedure for transferring metal contacts onto the PS layer, which can also be used to scale the memory devices down to the nanoscale.

3.8 References

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Chapter 4 Conduction Mechanism in Organic Memory Devices as a Function of Temperature

4.1 Introduction

In Chapter 2, we introduced the single-layer memory device which allowed us to demonstrate and characterize the hysteresis associated with the Poly (4-vinyl phenol) (PVP) polymer and C_{60} thin film blend. In addition, we were able to fit the conduction models discussed in Chapter 1 to the current-voltage (I-V) characteristics of the single-layer devices. It was found that the devices operated via direct tunneling until a threshold voltage above which, the transport switched to Fowler-Nordheim tunneling. However, the differences in current values between the on and off states in the single layer devices was approximately 75nA, too small to be technologically feasible. In order to overcome this limitation, in Chapter 3, we described the development of a multi-structured memory device, which exhibited a current difference of approximately three orders of magnitude between the two states. Furthermore, the current in the on state was of the order of micro-Amps, making detection and differentiation between the two states more technologically viable. The primary novelty of the multi-layered device structure was the introduction of a capping layer (pure PS with a thickness of ~ 5 nm), which allowed the entire PVP + C_{60} film (the active layer) to charge as opposed to the partial charging associated with the single layer. The ability to charge the entire active layer gives rise to a significantly larger hysteresis, allowing for easier detection of the memory states. In addition, the capping layer helps to increase the stability of the multi-layer devices because it acts as a diffusion barrier protecting the blend layer. Although the conduction mechanisms reported in Chapter 2 and 3 were elucidated from measurements performed at room temperature or above, they describe the salient features of the memory devices. However, some of the conduction models described in detail require a low temperature study to eliminate them as contributing to conduction in our devices. Therefore, in order to confirm that the

tunneling is the only mechanism responsible for transport in our organic devices as described in Chapters 2 and 3, we have measured the current versus voltage characteristics as a function of temperature (ranging from 4.2K to 298K) of our devices. Specifically, in order to study the mechanisms of transport in each individual component of the multi-layer device, we have made measurements on pure PS, pure PVP and PVP + C₆₀ layers. Transport analysis through the pure polymer films allowed us to distinguish any effects on transport induced from introducing C₆₀ molecules. Since the multi-layered device in Chapter 3 utilized Al contacts at the bottom and Au on top, we have also investigated the influence of transport as a function of contact electrodes on the relevant polymers. Finally, in order to summarize the salient features of the transport through the various components of the multi-layered device that give rise to the hysteresis and allow memory operations to be performed, at the end of this Chapter, we have developed a working model for the conduction processes in our devices.

4.2 Experimental Setup

The I-V measurements as a function of temperature (I-V-T) were performed using a Janus ST-500-2-4LF cryogenic probe station, which was commissioned from scratch by the author. The probe station is electrically isolated and grounded to the measurement system to reduce the noise and achieve pico Amps level current measurements. The station was pumped down to 10⁻⁵ Torr via a turbo-molecular pump in order to make measurements at cryogenic temperatures. Liquid Helium (LHe) was used to cool both the station and the device down to 4.2 Kelvin. The temperature was controlled via a scientific instrument 9700 temperature controller, which uses a feedback loop to maintain the devices temperature to within 0.05 Kelvin. Resistors controlled by the feedback loop are used to heat the device to the appropriate temperature. I-V measurements were performed using a HP 4140B picoammeter using the set up described in

the previous Chapters. Both the temperature controller and picoammeter were computer controlled via the Agilent VEE software through standard IEEE-488 protocols with GPIB connections. The VEE program written by the author is shown in the Appendix.

4.3 Capping Layer

As described in Chapter 3, a thin layer ($\sim 5\text{nm}$) of Polystyrene (PS) was used to cap the top of the multi-layer memory devices. The top gold electrode was deposited on top of this PS layer and therefore it is important to understand the junction between Au and PS. Therefore, we first describe the transport through the PS layer. Metal-insulator-metal (MIM) devices were fabricated with Au electrodes sandwiching the PS thin film to investigate transport through the pure polymers. Schematic of the MIM structure is shown in Figure 4-1. The device was fabricated by first thermally evaporating the bottom contacts through a shadow mask, followed by spin coating (7000 RPM) the PS layer from a solution of 10mg of PS and 1ml toluene. Then the top contacts were thermally evaporated through a shadow mask. Devices with Al and Au contacts were fabricated in the same fashion, with the exception that additional Au was evaporated on top of the Al contact pads for Al/polymer/Al devices. The addition of Au on top for the Al devices was found to be necessary to help ensure proper electrical contact throughout the I-V-T measurement, especially at low temperatures. We also found that the absence of the Au layer on top of the Al electrodes leads to oxidation, which leads to degradation of the contact with time.

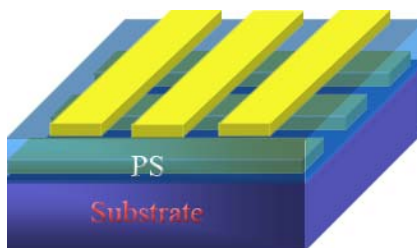


Figure 4-1 – Metal-insulator-metal structure for I-V-T measurements on PS. Similar MIM structure was also used for I-V-T measurements on pure PVP.

4.3.1 Pure PS MIM Devices with Aluminum Contacts

I-V-T measurements were performed from 4.2 K to 294 K with a step of 10 K. I-V curves at various temperatures for the pure PS MIM device are shown in Figure 4-2. It should be noted that the I-V curves for some temperatures were removed from the plot for clarity but raw data is available, if required for further discussion. In addition, many erroneous points that were deemed noise were also removed. The source of the noise was attributed to the difficulty of maintaining proper contact with the probe tips, especially at low temperatures. The inclusion of gold on top of the Al pads was helpful in reducing the noise to an acceptable level. Based on the plot in Figure 4-2, it appears that there is no significant temperature dependence of the I-V characteristics for the pure PS MIM devices. In addition, no apparent hysteresis is present throughout the temperature measurements as highlighted by Figure 4-2b where the ratio of the two conducting states versus temperature is plotted at 0.2V. The curve is relatively flat showing no significant difference. Also, the ratio between the high and low conducting states is small (same order of magnitude), indicating no significant hysteresis in the pure polymer, as expected. Similar results have been found to occur at different voltages.

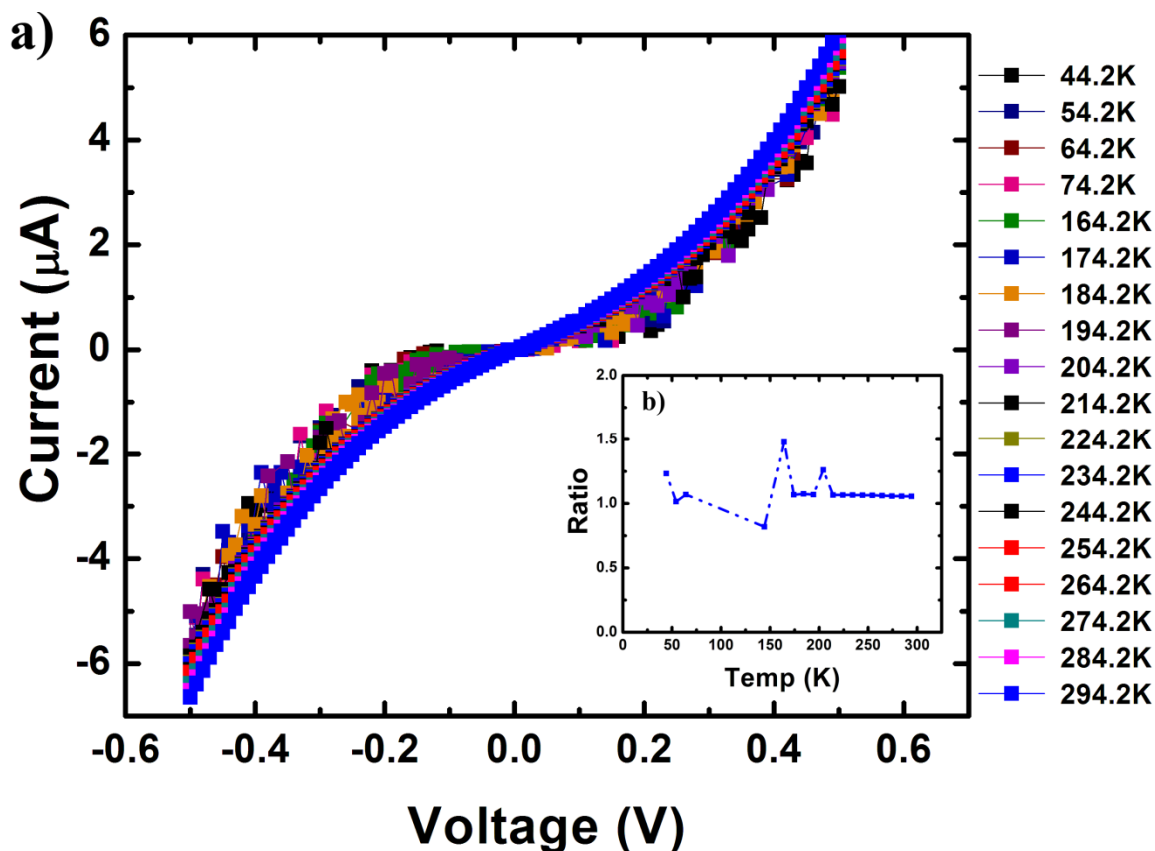


Figure 4-2 – (a) Current versus Voltage measurements of pure PS MIM devices taken at various temperatures. Some temperatures were excluded from the graph for clarity. (b) Current ratio versus temperature at 0.2V, demonstrating the absence of a hysteresis

To confirm the weak temperature dependence, Current versus Temperature (I-T) data was plotted at various voltages, as shown in Figure 4-3. The upward (0V to 0.5V) and the downward sweep (0.5V to 0V) of the I-V-T curve in Figure 4-2a were analyzed separately. Figure 4-3a is the upwards sweep and Figure 4-3b is the downward sweep. The relatively flat slopes of the I-T curves at the different voltages indicate that there is very little temperature dependence on the conduction. Based on the mechanisms described in Chapter 1, only the temperature independent models, direct and Fowler-Nordheim tunneling are plausible [1-4]. The other mechanisms such as Poole-Frenkel, variable-range hopping, or thermionic emission result in a

large temperature dependences [5-9] of the current that is not observed here. In addition, the difference in current level from 0.1V to 0.2V is larger than the rest of the voltages, suggesting a change in the conduction mechanism that is voltage dependent. This will be discussed next in detail.

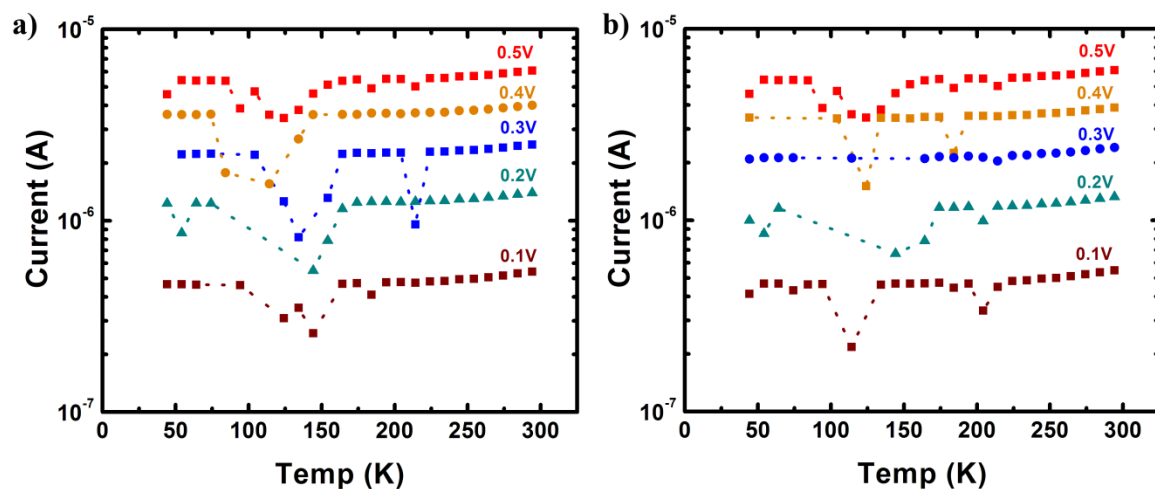


Figure 4-3 – Current versus Temperature (I-T) for various Voltages. Figure (a) is during the upward sweep from 0V to 0.5V. Figure (b) is the downwards sweep from 0.5V to 0V.

The relative temperature independence indicates that direct or Fowler-Nordheim tunneling are the dominant mechanisms. To confirm this, the theoretical tunneling models are fitted to the I-V curve at 292 K. The choice of temperature associated with the I-V curve is arbitrary due to the temperature independence. Figure 4-4 shows the resulting fits. As in Chapter 2, for the PVP + C₆₀ blend films, neither of the two models fit the curve completely. Rather, a threshold exists below which direct tunneling is dominant and above which Fowler-Nordheim is dominant. Figure 4-4a shows the direct tunneling region, located at 0 to 0.2V, and Figure 4-4b shows the Fowler-Nordheim region, located at 0.2V to 0.5V.

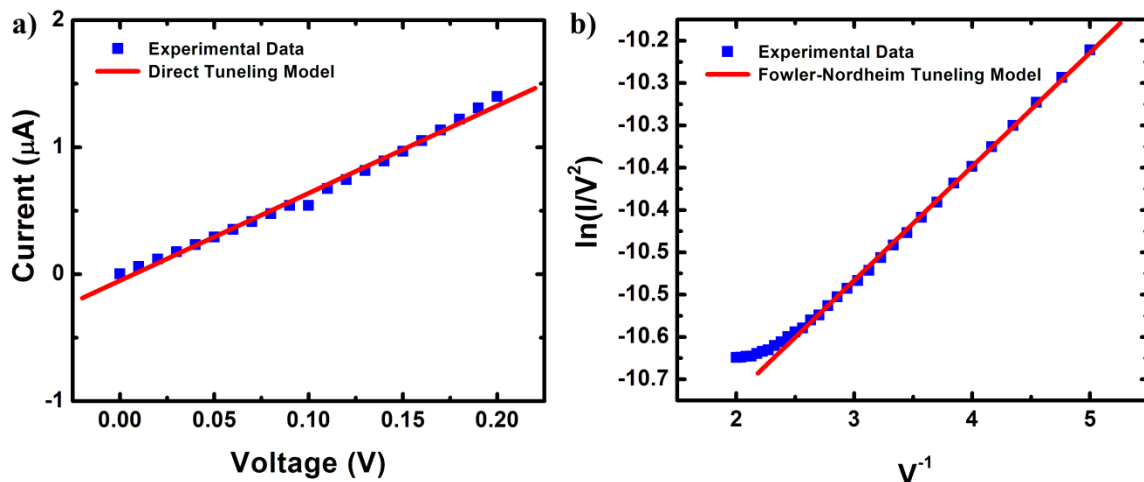


Figure 4-4 – Fits for PS with Al contacts MIM device in the positive region of the upward sweep of the data in Figure 4-2a (a) Fit for direct tunneling from 0 to 0.2V. (b) Fit for Fowler-Nordheim tunneling from 0.2 to 0.5V. The blue squares represent the experimental data and the red line represents the fit.

4.3.2 Pure PS MIM Devices with Gold Contacts

I-V-T measurements were performed in a similar manner to Al devices described above except that the temperature range was limited from 78 K to 298 K in order to conserve LHe by using liquid nitrogen (LN_2). I-V curves at various temperatures in this study are shown in Figure 4-5a. Some temperature measurements and noise were removed once again for clarity. The data in Figure 4-5 is dramatically different from those obtained using Al contacts (Figure 4-2). Firstly, it can be seen that the I-V characteristics are linear and the amount of current through the device is very high. Indeed, the current is high enough to reach the maximum capability of our HP4140B picoammeter, which has a limit of 10mA. The very large currents through the Au/PS/Au are reproducible and not related to the breakdown of the polymer. Instead, the data analysis shows that in these devices direct tunneling in absence of Fowler-Nordheim tunneling is the mechanism for conduction, leading to the higher measured current values. We also believe that the high currents are more likely due to a smaller barrier between the Au electrodes and PS layer, compared to the barrier between Al and PS. We will discuss this in more detail towards

the end of this chapter. Based on the plot in Figure 4-5a, it appears that there is no significant temperature dependence on the I-V characteristics. In addition, no apparent hysteresis is present throughout the temperature measurements. This is highlighted by Figure 4-5b where the ratio of the two conducting states versus temperature is plotted at 0.2V. The curve is relatively flat showing that the ratio between the high and low conducting states is small (same order of magnitude), indicating no significant hysteresis.

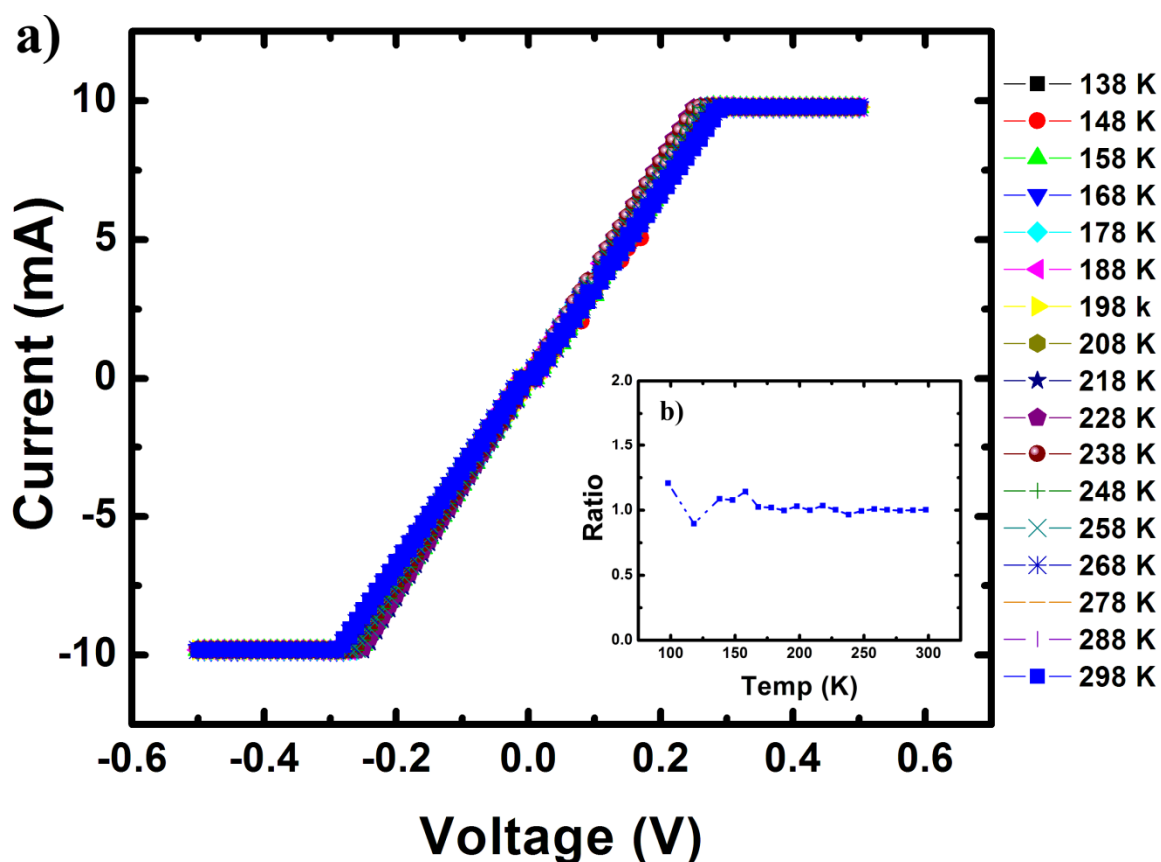


Figure 4-5 – (a) Current versus Voltage for varying temperatures. Some temperatures were excluded from the graph for clarity. (b) Current ratio versus temperature at 0.2V

To confirm the weak temperature dependence, I-T data was plotted, as shown in Figure 4-6. The analysis is limited to 0.25V, where the current is 10mA, which is the maximum capability of our meter. As before, the upward sweep (0V to 0.25V) and the downward sweep (0.25V to 0V) of the I-V-T curve in Figure 4-5a were analyzed separately as shown in Figure 4-6a and Figure 4-6b, respectively. No temperature dependence was found and no switching from direct to Fowler-Nordheim tunneling was found for the voltage range that could be measured. This is different from the Al contacts where a threshold exists at 0.2V to switch from direct tunneling to Fowler-Nordheim tunneling, causing a difference in the current levels between 0.1V to 0.2V. This suggests that there is a difference in the barrier heights and electron injection energy from the back contact between Al and Au electrodes.

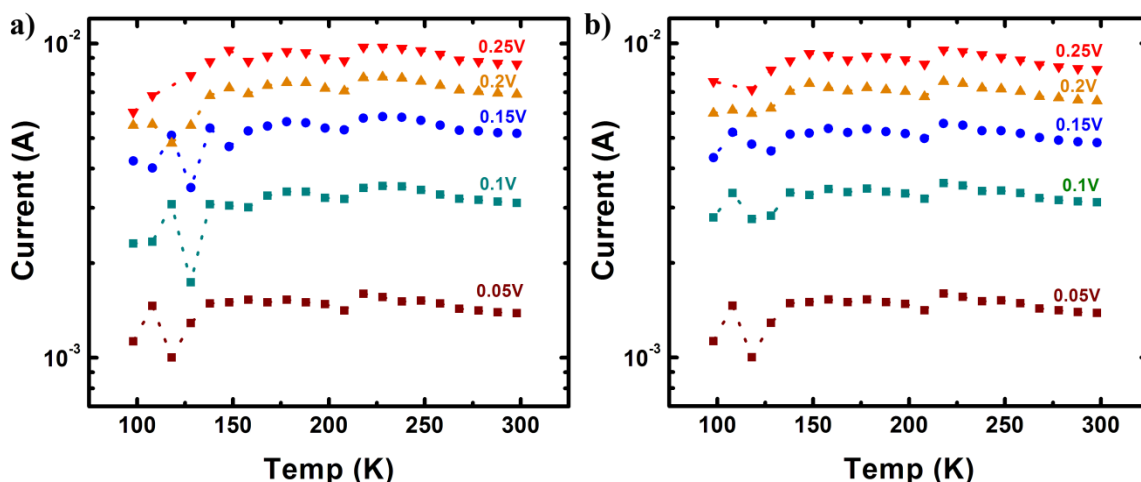


Figure 4-6 –I-T for Au/PS/Au MIM devices at various voltages. Figure (a) is during the upward sweep from 0V to 0.25V. Figure (b) is the downwards sweep from 0.25V to 0V.

We fit the I-V data at 298K (but results of the fits are the same at all temperatures) to confirm the tunneling mechanism, as shown in Figure 4-7. The direct tunneling relationship fits the experimental data in the Figure convincingly for the voltage range presented. The direct tunneling mechanism can also explain the linear I-V output shown in Figure 4-5a

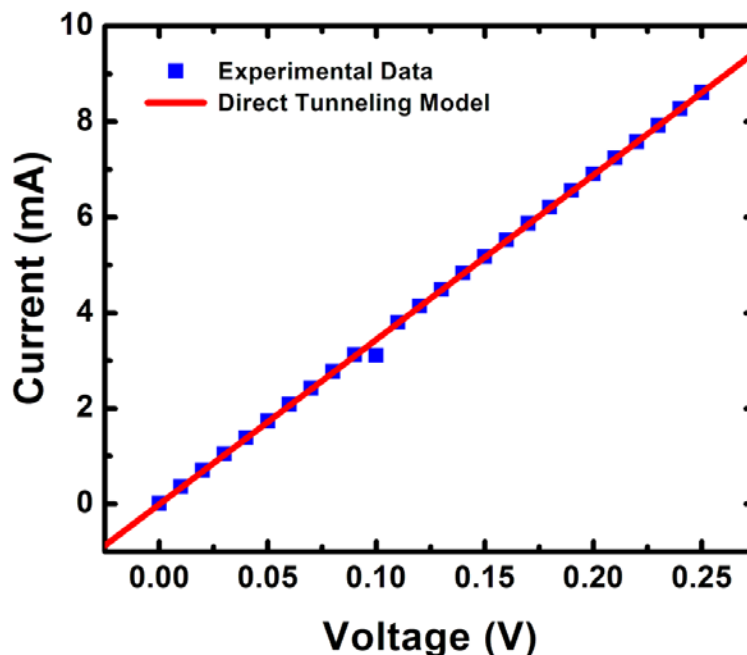


Figure 4-7 – Direct tunneling fit for PS MIM devices with Au electrodes in the positive region of the upward sweep (0V to 0.25V) of Figure 4-5a. The blue squares represent the experimental data and the red line represents the fit.

4.4 Pure Poly (4-vinyl phenol) MIM Devices with Al Electrodes

Since PVP is the host insulating polymer in which the C_{60} molecules are dispersed, the transport through the polymer as a function of temperature as well as the junction characteristics when contacted to Al are important to understand. We therefore carried out a detailed transport study with temperature on MIM devices consisting of pure PVP polymer sandwiched between Al electrodes. The PVP MIM devices were fabricated in the same manner as the pure PS devices with Al electrodes. Specifically, the PVP was deposited by spin coating (7400 RPM) from a solution of 25mg of PVP and 1ml Isopropanol giving a film thickness of approximately 30nm, onto patterned Al electrodes, followed by evaporating the top Al contacts.

I-V-T measurements were performed as before from 4.2K to 294K in 10K steps and are shown in Figure 4-8. Once again, no temperature dependence was found but the current values are substantially lower than any of the previous pure polymer devices tested. In addition, Figure 4-8b shows that the ratio of the two conducting states with temperature does not exceed 4, which indicates that no significant dependence of hysteresis with temperature exists.

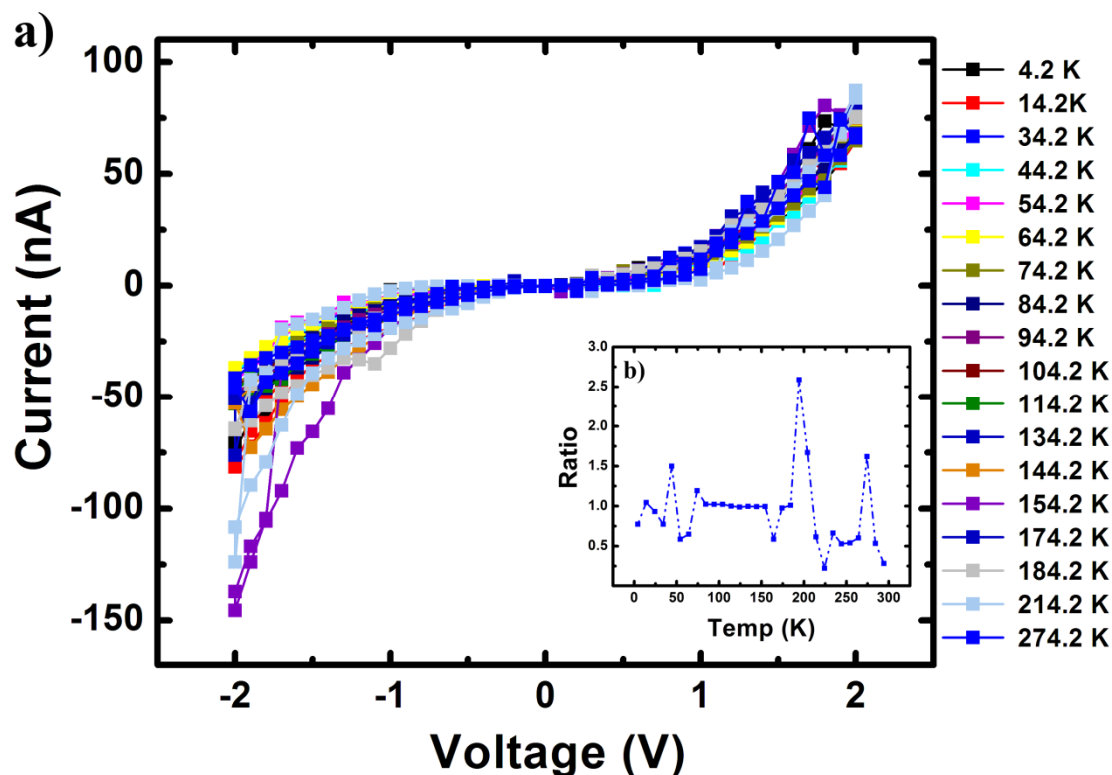


Figure 4-8 – a) I-V of Al/PVP/Al MIM structures at varying temperatures. Some temperatures were excluded from the graph for clarity. (b) Current ratio between the two states versus temperature at 1V are shown.

The weak temperature dependence was confirmed by I-V-T measurements plotted in Figure 4-9. As in the PS system, the upward sweep (0V to 2V), represented in Figure 4-9a, and the downward sweep (2V to 0V), represented in Figure 4-9b, were analyzed separately. Just as in the PS case, the resulting I-T curves indicate that there is very little temperature dependence on the conduction in both sweep directions. As such, we believe that the mechanism is based on both direct and Fowler-Nordheim tunneling.

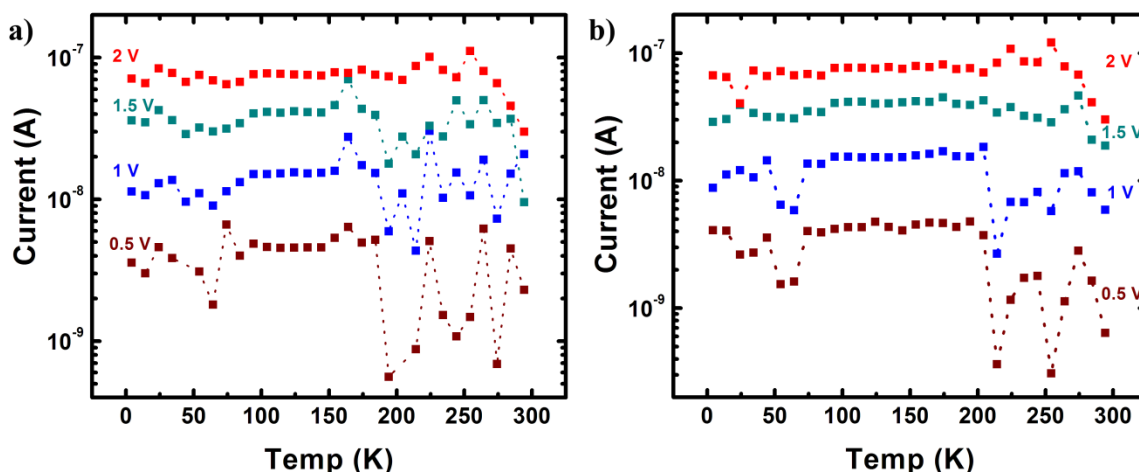


Figure 4-9 – I-T of Al/PVP/Al for various Voltages. Figure (a) is during the upward sweep from 0V to 2V. Figure (b) is the downwards sweep from 2V to 0V.

4.5 Multi-Layer Memory Devices

Having established the temperature dependence of the I-V characteristics and confirming the absence of hysteresis at all investigated temperatures for pure polymer devices with the two electrode metals used for the multi-layered devices, we launched similar measurements on the blend devices. Since the I-V-T measurements of the multi-layered devices are essentially dominated by the blend (PVP+C₆₀) layer, it would be redundant to present the results from the blend layer alone. For this reason, we report the I-V-T measurements and analysis from the multi-layered devices only. The I-V characteristic of the multi-layered devices

is dominated by the charge transport through the PVP+C₆₀ layer (charging and discharging of the fullerene molecules) with temperature. The device structure used for the temperature study was identical to that used in Chapter 3 and shown in Figure 3-1b. The fabrication steps are briefly summarized here to refresh the reader. The device was constructed by first thermally evaporating Al electrodes for the bottom contact followed by spin coating a ~30nm thick PVP & C₆₀ blend film from a solution of 25mg of PVP, 0.5mg of C₆₀ and 1 ml of isopropyl alcohol. Next, the PS capping layer (thickness ~5nm as measured by spectroscopic ellipsometry) was deposited on top by dissolving 10 mg of PS in 1 ml of toluene and spin coating the solution at 7000 rpm. Finally, the top contacts were deposited by thermally evaporating Au through a shadow mask.

I-V curves at various temperatures of the multi-layered structure are shown in Figure 4-10. It can be seen from the Figure that in contrast to the pure polymer devices, a clear hysteresis, as expected, can be clearly observed at all temperatures. Furthermore, the negative differential resistance above approximately 1.4V due to electric field screening from charging of fullerene molecules can also be clearly seen. Thus, it can be concluded that the charging and discharging of the fullerene molecules within the PVP matrix is not dramatically affected by temperature. Although the hysteresis in the multi-layered devices is clearly observed, no clear change in the I-V characteristics and therefore the ratio between the on and off states can be seen with temperature, as shown in Figure 4-10b where the ratio of the two conducting states versus temperature is plotted at -1V. Based on Figure 4-10b, there is no apparent relationship between temperature and the amount of hysteresis, instead the variation in the ratio can be attributed to the inherent noise during measurement of the low conducting state. The lack of temperature dependence in combination with the absence of hystereses in the pure polymer cases confirms that the hystereses in the multi-layered devices are a result of charge storage

within the C_{60} molecules. A closer observation of Figure 4-10a reveals that the threshold voltage to charge and discharge the C_{60} molecules varies from measurement to measurement. However, no specific correlation with temperature could be found, indicating that the variability is due to system variations. The variation is not detrimental since the memory devices perform write operations at 3V, ensuring the C_{60} molecules are charged to store the information. The variation in the discharge threshold ranged from -2.2V to -2.9V, which is well beyond the read voltage of -1V. In addition, an erase voltage of -3V or higher should ensure complete discharging of the C_{60} molecules. Further, read pulses of -1V is not large enough to disturb the charged C_{60} molecules. However, the variation in the threshold voltages could be a sign of degradation within the polymer matrix, since the extended I-V sweeps at the various temperatures can produce significant electrical stress on the polymers, possibly the first signs of an accelerated aging. Future work is required to understand this behavior and its possible relationship to aging of the memory devices.

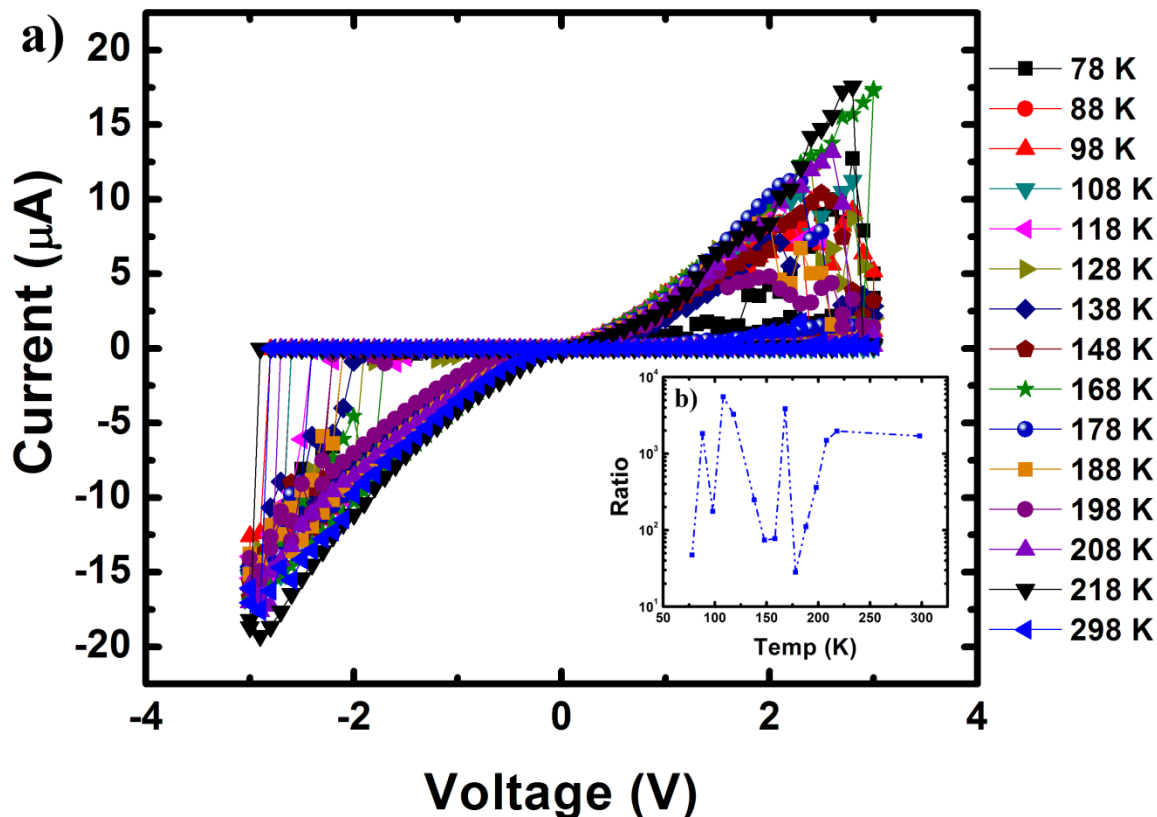


Figure 4-10 – (a) I-V characteristics at for varying temperatures for multi-layered (Al/PVP+C₆₀/PS/Au) devices. Some temperatures were excluded from the graph for clarity. (b) Current ratio between on and off states versus temperature at -1V.

The I-T data for the multi-layered devices plotted in Figure 4-11 confirm the weak temperature dependence, similar to the pure polymer cases. The currents in the low conducting state defined as the upward sweep from 0V to -3V as a function temperature are plotted in Figure 4-11a. The low conducting state in the device occurs due to the charged C₆₀ molecules screening the applied voltage, as described in Chapters 2 and 3. The noise level is significant in this regime due to the very low current values associated with this conducting state. Despite the noise, no significant dependence of the current on the temperature can be observed. The high conducting state occurs during the downward sweep from -3V to 0V and the corresponding I-T

data is plotted in Figure 4-11b. The high conducting state occurs because at sufficiently large voltages, the charged C_{60} molecules discharge, preventing any voltage screening and allowing current to flow. The high currents make any noise in the system negligible, giving the relatively flat curves in Figure 4-11b. As in the low conducting state, only a weak temperature dependence is observed. As was the case for the pure polymers, only direct and Fowler-Nordheim tunneling are capable of describing the temperature behavior of the conductance in both high and low conducting states of Figure 4-11.

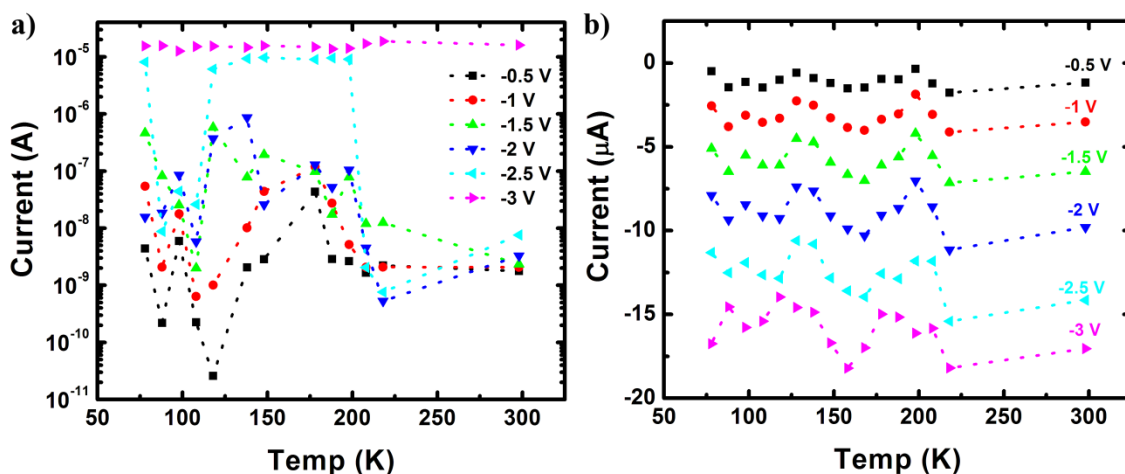


Figure 4-11 – I-T data of the multi-layer memory device for various voltages. Figure (a) is during the upward sweep from 0V to -3V, operating in the low conducting state. Figure (b) is the downwards sweep from -3V to 0V, operating in the high conducting state.

Direct and Fowler-Nordheim tunneling models were fitted to the I-V curve at 298 K, as the lower temperature measurements were noisier. As was the case in Chapter 2, for the single-layer PVP + C₆₀ blend films, neither of the two tunneling models were found to fit the curve completely in either conduction states. Instead a threshold voltage of -1.3V exists where the tunneling mechanism switches from direct to Fowler-Nordheim. It should be noted that a similar switch was also observed in the pure PVP MIM devices with Al electrodes (Figure 4-4b). However, the switch from direct to Fowler-Nordheim tunneling in the Al/PVP/Al devices occurred at threshold voltages between 0.2V – 0.5V. Therefore, it is likely that the switch between direct and Fowler-Nordheim tunneling in the multi-layered devices occurs due to the combination of charge injection at the Al/PVP interface, transport through the PVP, as well as the presence of C₆₀ molecules in the matrix. Below the threshold voltage of -1.3V, direct tunneling was found to be the dominant mechanism in terms of magnitude. Figure 4-12a shows the direct tunneling fit for the low conducting state between 0V to -1.3V while Figure 4-12b shows the fit for the high conducting state at voltages ranging from -1.3V to 0V.

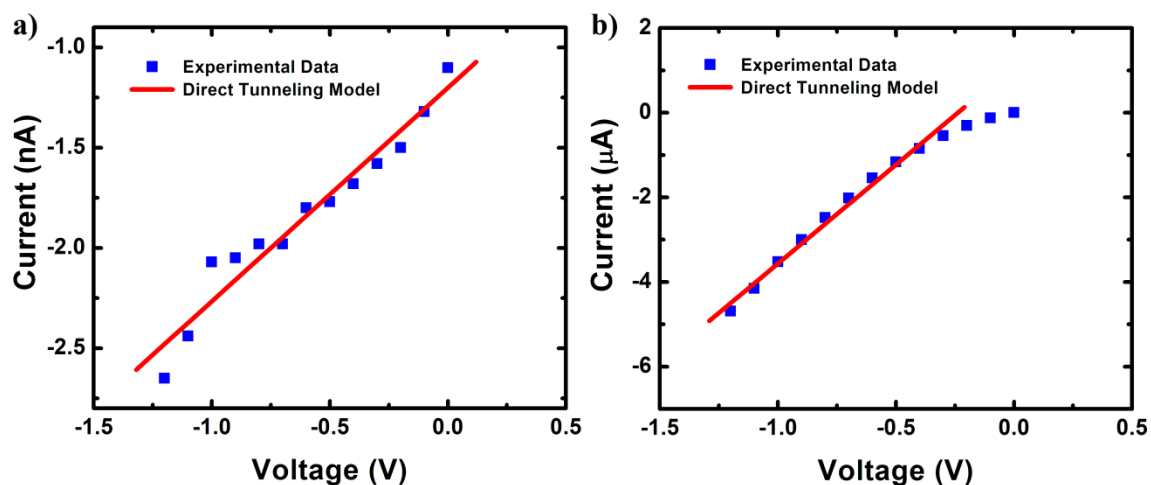


Figure 4-12 – Direct tunneling fits for the multi-layer devices in the negative region for both the (a) low conducting state (upward sweep from 0V to -1.3V) and the (b) high conducting state (downward sweep from -1.3V to 0V) of Figure 4-10a.

The application of negative potentials greater than -1.3V leads to the onset of the Fowler-Nordheim conduction mechanism in the multi-layered devices. Fits for both conduction states in this voltage regime are shown in Figure 4-13. Both the high and low conducting states are linear in the Fowler-Nordheim plot, confirming Fowler-Nordheim conduction. Insets (i) and (ii) in the Figure show an enlarged view of the low and high conducting states, respectively. The insets show that noise within the measurement can cause points along the I-V curve to deviate from the Fowler-Nordheim model slightly, however, the overall current trends follows the model well.

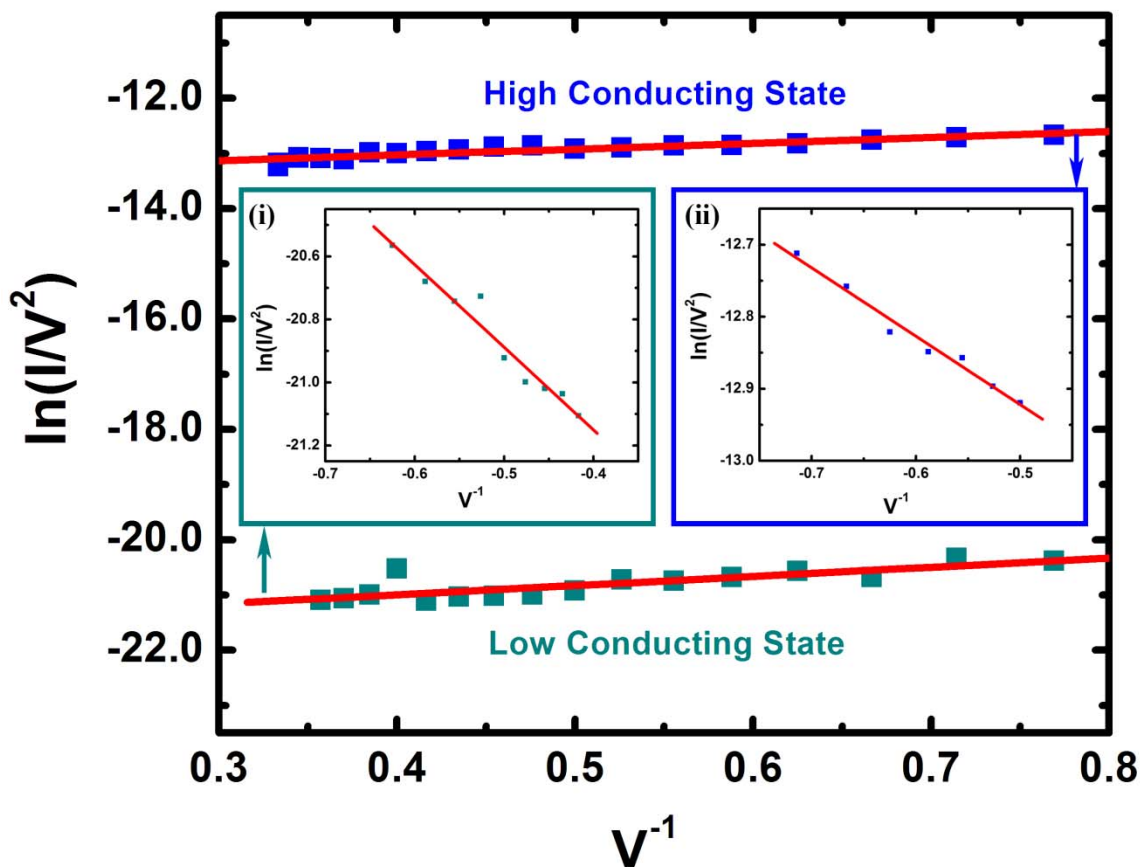


Figure 4-13 – Fowler-Nordheim tunneling fits for the multi-layer devices at negative voltages greater than -1.3V for both low and high conducting states of Figure 4-10a. (i) Enlarged view of the Fowler-Nordheim fit for the low conducting state. (ii) Enlarged view of the high conducting state fit.

Based on the tunneling models for the operation of the multi-layer devices, we can confirm that the blend memory devices operate using the fitted tunneling models presented in Chapter 2. The conduction through the PS layer with the top gold contacts was demonstrated to be based on direct tunneling. Therefore, the conduction in the multi-layered devices is limited by the active layer, giving rise to the hystereses and the two distinct conduction states. The PS capping layer merely acts as a tunneling layer separating the C_{60} molecules from the top contact to allow for complete charging and discharging of the C_{60} molecules dispersed in the PVP layer.

Thus, any temperature dependence that would have occurred through the active layer would manifest itself in the conduction through the entire multi-layer device. In addition, in Chapter 2 we showed that the tunneling models were the only ones from Chapter 1 that were capable of describing the observed I-V data for the single -layer memory devices. Based on the temperature study reported here, it can be confirmed that the conduction through the single-layer devices is also dominated by direct and Fowler-Nordheim tunneling and that other mechanisms do not play a significant role in the transport. This is further confirmed by the similar thresholds required to switch from direct to Fowler-Nordheim tunneling between the multi and single-layer devices. For the single-layer devices, the threshold was found to be 1.3V in the positive region. However, because of the symmetry of the I-V curve, 1.3V directly translates to -1.3V in the negative region. This is identical to the observed threshold for the multi-layer devices. Thus, we can rule out the contribution from C_{60} on the electrical conduction through the device. Instead, the primary role of the C_{60} molecules is to screen the applied voltage based on how much charge is stored, leading to high and low conducting states.

4.6 Model for Conduction and Memory Effect

Although we have not carried out detailed spectroscopic investigation of the device structures, our basic I-V-T measurements provide sufficient insight to devise energy diagrams for charge transport. Based on the I-V-T measurements and tunneling mechanisms we have constructed a rough model of the band diagram for the multi-layer devices to help illustrate the operation and transport mechanism through the structure. It is important to note that the derivation of the band diagram for the multi-layered device from diagrams of individual components are approximations based on the I-V data presented throughout this thesis and should not be considered as the final structure. A more accurate band diagram will require

detailed studies including ultraviolet photoemission spectroscopy (UPS) and inverse photoemission spectroscopy (IPES) to determine the exact position of the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) levels of both PVP and PS polymers when contacted to Al and Au electrodes [10-14]. In addition, an analysis of the density of defect states within PVP is needed to better understand their role in the conduction through this layer. These issues will need to be addressed as future work.

Nevertheless, keeping these points in mind, we begin by constructing the band diagram for the individual components of the multi-layer devices during zero bias. The large variation in the current range of the I-V measurements for the Au/PS/Au, Al/PS/Al, and Al/PVP/Al devices indicate that the barrier height between the metal electrode and the polymers varies as presented in Figure 4-14. Since both PVP and PS are amorphous polymers with defect densities roughly similar to each other, the variations in current can be, at least as a zeroth order approximation, attributed to the differences in the barrier heights between the electrode and polymer. Based on this assumption, first looking at the band diagrams for PS, the higher current for the Au electrodes compared to Al suggest that the barrier height between PS and Au is smaller than that of Al, shown in Figure 4-14a and Figure 4-14b, respectively. The incorporation of C₆₀ molecules in the PVP matrix leads to a slightly more complex band diagram as depicted in Figure 4-14c. This diagram shows the fullerene HOMO and LUMO energy levels are within the insulating polymer. In addition, localized states near the Fermi level are also shown within the polymer, well below the LUMO of the C₆₀ molecules. The localized states are incorporated into the diagram to explain the tunneling mechanism obtained from the fits of the experimental data. Specifically, since the tunneling probability decreases exponentially with material thickness, transport mechanisms for relatively thick (~ 30nm) PVP must be mediated through states within the band gap. The presence of mid-gap energy levels allows tunneling to occur

between these states across the entire width of the PVP layer [15]. If the PVP layer is cross-linked then the number of localized states drop, reducing the current through the layer [16-19]. In the presence of mid-gap states, charge injection from the back electrode can occur by direct tunneling and if the energy of the carrier is sufficiently large (i.e. 'hot electron' injection), then it is possible for the carrier to be transported through a relatively thick layer without losing all of its energy [20]. The output I-V characteristics of such a transport model would be a combination of direct and Fowler-Nordheim tunneling similar to what we observe for the multi-layer devices. Returning to Figure 4-14c, the LUMO of C_{60} is located approximately between 2.8-3.76eV [21-24] and is shown at 3.76eV which is significantly higher than the localized states within the PVP polymer. The motivation for this is to convey that discharging of the fullerene molecules into defect states cannot occur. The HOMO level of C_{60} is located approximately between 6.36-7.6eV [21-24] and is not involved in the conduction or memory operation in either the single-layer or the multi-layer memory devices. The band diagram for the multi-layer device was derived by summing the Au/PS/Au and Al/PVP+ C_{60} /Al diagrams to obtain the energy levels in Figure 4-14d. The difference in the work functions of Al and Au causes a slight bending of the bands, facilitating transport of the injected carriers. We will next look at the band diagram of the multi-layer memory device with respect to the memory operation.

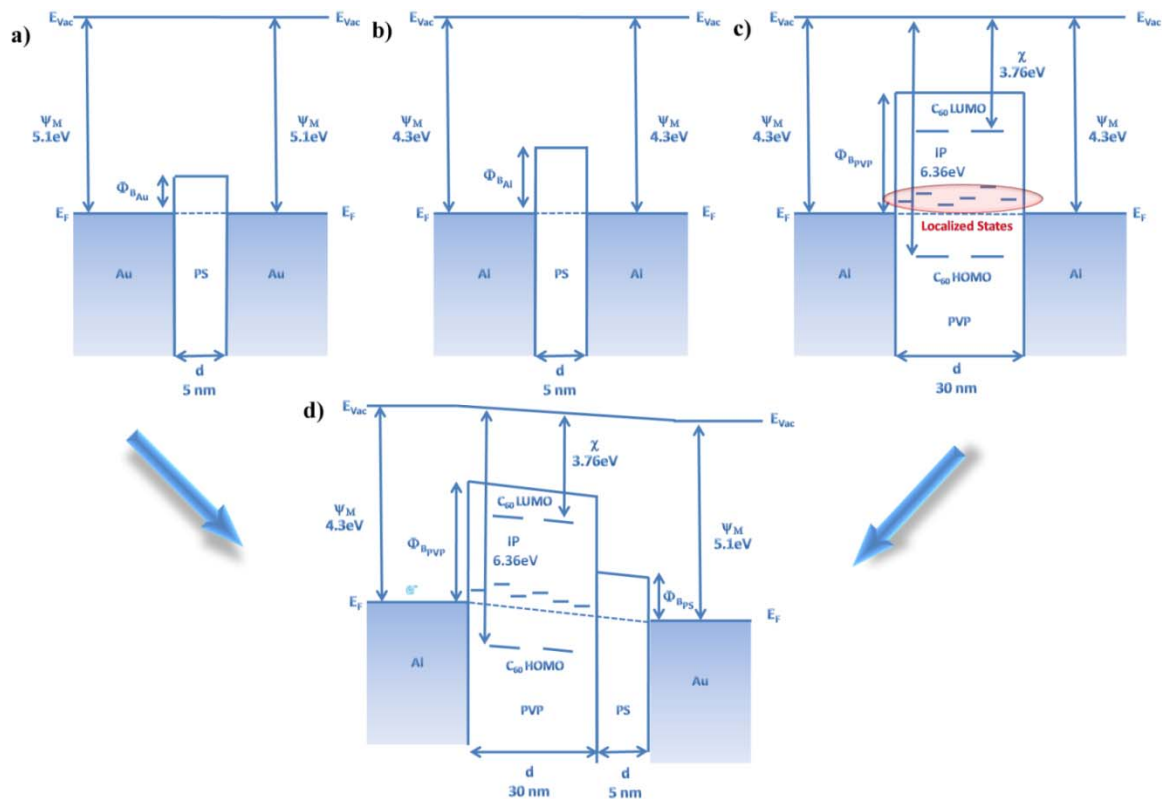


Figure 4-14 – Band diagrams for (a) PS with Au contacts, (b) PS with Al contacts, (c) PVP+C₆₀ with Al contacts, and (d) the multi-layer memory device. In the schematics above ‘d’ is the barrier width, E_F is the Fermi level of the metal contacts, E_{Vac} is the vacuum level, Ψ_M is the work function of the metals, χ and IP are the electron affinity and ionization potential of C₆₀ respectively. $\Phi_{B_{Au}}$, $\Phi_{B_{Al}}$, and $\Phi_{B_{PVP}}$ are the barrier height between the metal contacts and the polymers. $\Phi_{B_{PVP}}$ is the barrier height between Au and PS in the multi-layer case, which is equal to $\Phi_{B_{Au}}$. The barrier height in (a) is smaller than that of (b) based on the lower currents that the Al contacts produce in Figure 4-2. The multi-layer band diagram is a combination of both PS with Au and PVP+C₆₀ with Al diagrams

Using the band diagram in Figure 4-14d, we can also derive the diagram of the multi-layer memory device under read, write, and erase conditions. We will start with read operation conditions, which occur at an applied voltage of -1V. Reading a ‘0’ bit occurs during operation of the device in the high conducting state, resulting in the band diagram of Figure 4-15a. Electrons are capable of tunneling through both the PS layer and the localized states in the PVP+C₆₀ layer

from the Au to the Al contacts. The C_{60} molecules remain uncharged because the barrier between the local states and the LUMO level of C_{60} remain large enough to prevent tunneling. When the device reads a '1' bit (Figure 4-15b) the stored electrons in the LUMO level of the isolated C_{60} molecules prevent the bands from bending as much as they normally would by screening part of the applied voltage of -1V. As a result, the number of electrons tunneling through the two polymer layers is reduced allowing the device to operate in the low conducting state. As before, the LUMO levels of C_{60} are sufficiently separated from the localized states in the PVP layer to prevent the stored electrons from tunneling out of the LUMO level.

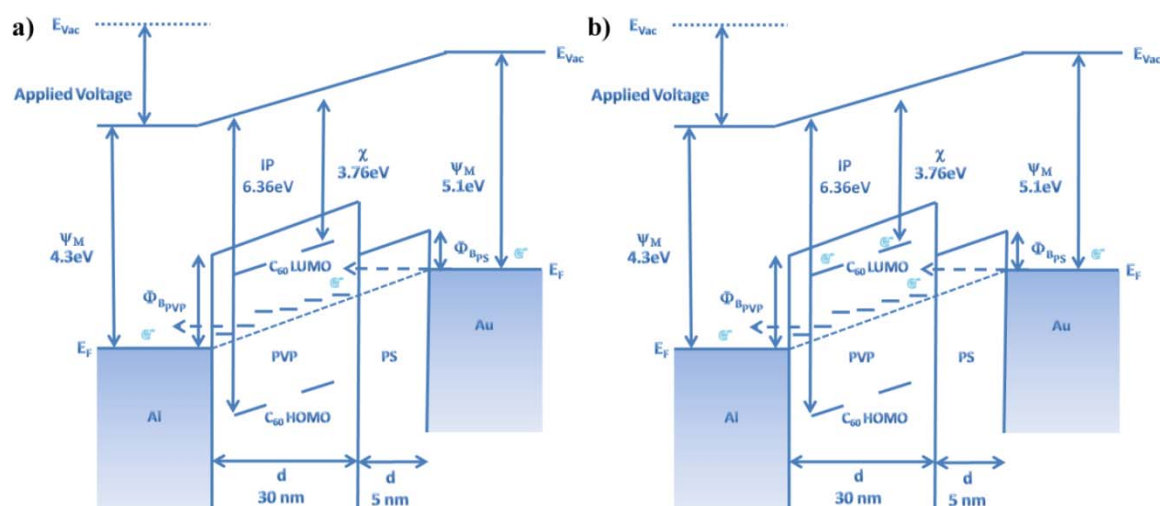


Figure 4-15 – Band diagram of the multi-layer memory device during read operations, (a) high conducting state ('0' bit) and (b) low conducting state ('1' bit).

When a write operation is performed, the bands bend significantly in the opposite direction compared to the read case, as shown in Figure 4-16a. The application of a +3V pulse causes the bands to bend far enough to allow Fowler-Nordheim tunneling to occur across the device to allow for tunneling between the localized states in the PVP layer and the LUMO level of the isolated C_{60} molecules. Electrons are injected from the Al electrode into both the localized states

and the LUMO level of some C_{60} molecules near the Al electrode. It should be remembered from Chapter 3 that the initial energy of the injected energy must be greater than at least 1.5eV for charging of the C_{60} molecules. Other C_{60} molecules in the PVP matrix may also be charged by electrons tunneling from the distributed localized states across the PVP layer. The remaining electrons in the local states tunnel down the energy potential and eventually through the PS layer into the Au electrode. When the +3V is removed the electrons in the LUMO levels are trapped until an erase operation is performed by an application of a -3V pulse. The application of -3V alters the band diagram to that of Figure 4-16b. The large negative applied bias causes the bands to bend enough to allow for Fowler-Nordheim tunneling to occur from the Au to Al electrodes. Electrons tunnel from the Au and through the PS layer into the localized states in the PVP layer, where they continue down the energy potential to the Al contact. The electrons that were stored in the LUMO level of the C_{60} molecules during the write operation are now capable of tunneling into the localized states, while the electrons in C_{60} molecules near the electrode tunnel directly into the Al. When the voltage is removed, the C_{60} molecules remain discharged and the device operates in the high conducting state during reading operations. The writing and erase process of the multi-layer device differs slightly from the single-layer device because the C_{60} molecules are separated from the Au contact. The isolation prevents electrons from tunneling directly into the LUMO level of C_{60} molecules near the Au electrode during erase operation, where they could be trapped and decrease hysteresis during read operations as is the case of the single-layer devices reported in Chapter 2. Therefore, based on the transport measurements without additional knowledge from spectroscopy, the suggested band diagrams presented here might be good starting points for understanding the complex behavior of charge storage and transport through the multi-layered devices.

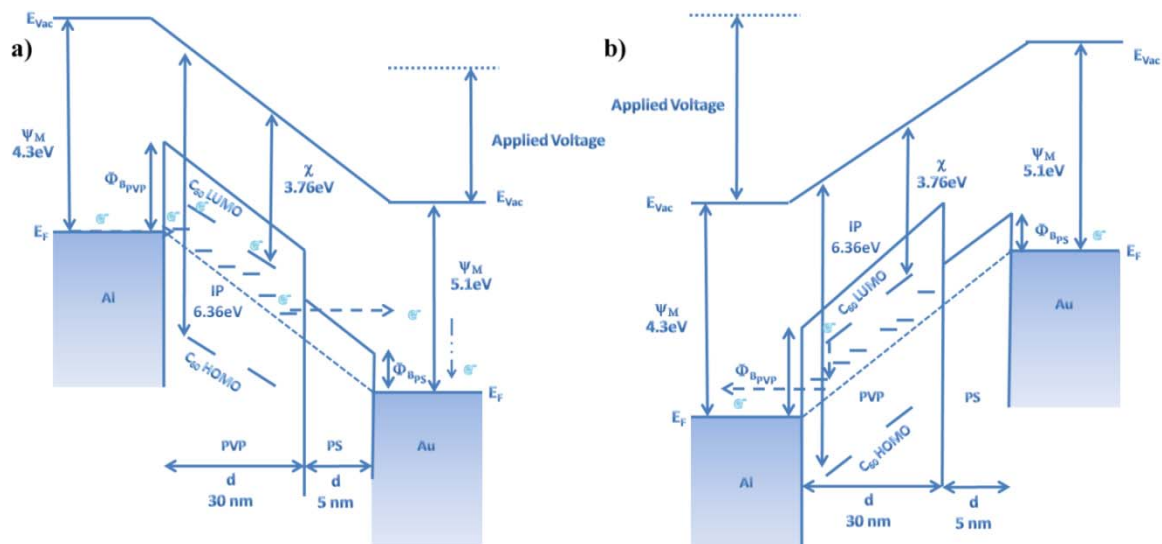


Figure 4-16 – Band diagrams for the multi-layer devices during (a) write (+3V pulse application) and (b) erase (-3V pulse application) operations.

4.7 Summary

In this Chapter, we have utilized I-V-T analysis to obtain insight into the conduction through the multi-layer memory devices described in Chapter 3. We first analyzed the capping layer, composed of pure PS, with both Al and Au contacts. I-V curves with both types of metal contacts were shown to be symmetrical and temperature independent. However, the Al devices exhibited both direct and Fowler-Nordheim tunneling characteristics, and was governed by a threshold voltage of 0.2V, while Au devices conducted purely based on the direct tunneling model. With a measured thickness of 5nm, Au was shown to be the ideal top contact in the multi-layer structure to ensure that the PS layer acts purely as a tunneling layer to isolate the PVP+C₆₀ active layer from the top contact. Thus, the PVP+C₆₀ layer dictates the conduction through the multi-layer devices, allowing for the complete charging and discharging of the C₆₀ molecules. In addition, the current through the multi-layer device remains sensitive to the conductive state of the active layer, which is directly related to the charged states of the C₆₀ molecules. Pure PVP was also analyzed to understand its role in the charge storage within the

C₆₀ molecules and transport. The resulting I-V curves from devices with Al contacts showed symmetrical and temperature independent characteristics, confirming dominant role played by the tunneling mechanism in the conduction through the PVP polymer. This suggested that electrons are capable of tunneling through the PVP from the Al contact and C₆₀ molecules to charge and retain the charge, as was shown in Chapter 2 with the Capacitance versus Voltage and Raman measurements. However, the question of how tunneling can occur in a relatively thick (~ 30 nm) polymers arises. We believe that the conduction occurs not by tunneling through the entire layer as is the case for PS, but instead by tunneling between localized states within the polymer. Charging of the C₆₀ molecules can occur either by direct injection of 'hot electrons' that have sufficient energy or by band bending to allow the electrons to tunnel between the localized states within the PVP polymer to access the energy levels of the C₆₀ molecules. Without significant band bending, the C₆₀ levels are inaccessible to the tunneling electrons that are not injected with sufficiently large initial energy. By combining the information obtained for both pure polymers with the I-V-T data for the multi-layer devices, we can elucidate first order model for both the conduction and the memory mechanisms in the multi-layer devices. The I-V-T data for the multi-layer was asymmetric and temperature independent. The asymmetry arose from the charging of the C₆₀ molecules within the PVP layer, which was responsible for the memory effect. The measured temperature independence of the current suggests that tunneling mechanisms are responsible for conduction through the entire device. This also suggests that the conduction through the PVP+C₆₀ layer, and hence through the single-layer memory devices in Chapter 2, are temperature independent. The resulting tunneling fits for the multi-layer devices are very similar to the fits presented in Chapter 2 for the single-layer devices, confirming the dominant role of PVP+C₆₀ in the measured conduction. The two conducting states that arise from charging the C₆₀ molecules exhibited similar behavior in terms of

temperature independence and tunneling behavior. Combined with the large ratio between the two states, the role of C_{60} was confirmed to operate only as a voltage screener and not related to the conduction through the memory device, similar to Simmons *et. al* [25] and Bozano *et al* [26].

4.8 References

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Chapter 5 Conclusions & Future Work

5.1 Conclusions

The continued convergence of different applications into a single mobile device such as Apple's iPhone has put considerable constraints on the current memory technology. As a result, the need for a universal memory technology has never been greater. New types of memory technologies such as Phase Changing, Ferroelectric, and Magnetic Random Access Memories have been developed to try to satisfy the new needs. However, as discussed in the beginning of Chapter 1, they lack some critical properties and performance to satisfy the new demands. Here, we have investigated a new memory technology that could have the potential to be a universal memory. Based on our initial discovery of charge storage within C_{60} molecules dispersed in insulating polymers at room temperature, we first developed a single-layer memory device to probe and understand the potential memory capability of the C_{60} /polymer system. The single-layer devices showed promise with a distinguishable difference in conduction states of approximately 75nA, which can be used for memory operations. While not technologically feasible, they did allow us to develop a conduction model, based on tunneling mechanisms, to understand the memory effect. However, the models require measurements at cryogenic temperatures. We setup a cryogenic probe station to make measurements rising from 4.2 K to 298 K. We utilized the knowledge gained from the single-layer devices to develop a multi-layer device that possessed superior performance in terms of difference in conduction states (a ratio of 10^3) and stability. The larger difference in states makes the multi-layer device technologically feasible, along with its memory retention, stability, and high-speed operation. Using the cryo-probe station, we were able to develop an early theoretical model for the conduction and memory storage mechanisms in the new multi-layer structure. The most important conclusions from each of the chapters in this thesis are summarized below.

Chapter 1 – Introduction

The status of both the current and future memory technologies, including the advantages and disadvantages, were briefly discussed. The motivation for the work and status of organic memory technology was also presented. Specifically, the possible conduction mechanisms for organic materials in general were presented in detail. These mechanisms included direct and Fowler-Nordheim tunneling, thermionic emission, Schottky emission, Poole-Frenkel emission, and variable range hopping. Each mechanism and its characteristic relationship with both voltage and temperature were derived from fundamental principles. We later fitted these models to our data to elucidate the underlying physics involved with the C₆₀/polymer memory. We also presented three main mechanisms utilized widely for organic memories to date; redox reactions, charge transfer, and charge storage. The last one is the mechanism for memory operation in our C₆₀/polymer system. The motivation for using the polymers in the system was also briefly explained by providing the structure of Poly (4-vinyl phenol) (PVP) and Polystyrene (PS).

Chapter 2 – Single-Layer Memory Devices

Analysis of the single-layer devices was started by characterizing the physical structure of the PVP+C₆₀ thin films using Atomic Force Microscopy (AFM) and Raman Spectroscopy. AFM measurements showed the films to be relatively smooth with an average roughness of a few nanometers. In addition, there were no pinholes, which could lead to short circuits. Raman analysis confirmed the presence of C₆₀ within the PVP layer by the presence of the characteristic

peaks, such as the A_{1g} peak, in the films of the PVP+C₆₀ blend. Electrical analysis of the single-layer memory devices was divided up into two sections, macroscale and nanoscale devices.

The macroscale devices were used to demonstrate a hysteresis in the current versus voltage (I-V) curves, which is vital for memory operation. A difference of 75nA was measured, enough to represent distinguishable states in laboratory conditions. The film thickness of ~30nm was found to be the optimal based on an analysis of breakdown voltage. The I-V curves were also plotted versus the sweep speed of the voltage to help determine if the conduction of hysteresis was based on traps within the thin film. The I-V was found to have very little dependence on the sweep rate, indicating traps were not involved. The optimum amount of C₆₀ was studied by calculating the percolation limit of C₆₀ in PVP, which was derived to be 16%. At 16% or above, the hysteresis disappeared and the current level increased to micro-Amps, due to conducting paths formed between the C₆₀. Below the percolation limit, 2% was found to be the optimal concentration in terms of film characteristics, hysteresis amount, and ease of processing. Charging of C₆₀ was confirmed indirectly with capacitance versus voltage (C-V) and directly with Raman analysis. For the C-V measurements, metal-insulator–semiconductor (MIS) devices were fabricated with p-type silicon. The insulator was varied between pure PVP and PVP+C₆₀ blend. Only the blend devices displayed a significant hysteresis, indicating charge injection into the C₆₀. Raman measurements were made on the standard memory device with ITO as the bottom electrode. By monitoring the A_{1g} peak, we could confirm charging and discharging of the C₆₀ molecules. After the write operation, the peak shifted due to the charging of C₆₀ molecules, confirming charge storage during the 24-hour period, and the peak returned by to its original position after the erase pulse, confirming discharging of the molecules. The hysteresis was translated into memory operations by performing read-write-erase (RWE) cycles at both low and high frequency. The device successfully followed the applied voltage pulses,

showing the two states during both frequencies. The delay time of the device was confirmed to be approximately 10ns. Memory retention was also confirmed by performing read operation for two hours after both write and erase operations. The two resulting states were found to be distinguishable throughout the two-hour period, however degradation was found in the current after the first hour for both states. This is attributed to possible deterioration in the polymer matrix. Conduction mechanisms discussed in Chapter 2 were fitted at room temperature to the I-V curve for the PVP+C₆₀ memory devices. It was found that below 1.3V the conduction occurred according to the direct tunneling model and above 1.3V, Fowler-Nordheim was dominant. This occurred for both conduction states, indicating that C₆₀ was not directly involved with conduction through the blend film. In addition, charging\discharging of the C₆₀ molecules only occurs during Fowler-Nordheim tunneling, when the band bending is sufficiently large to make the C₆₀ energy levels accessible, allowing write or erase operations. During direct tunneling, charge storage occurs due to a lack of band bending, making the read operation possible.

Nanoscale measurements were performed with both conducting atomic force microscopy (c-AFM) and nanoscale gap cells. Both measurements exhibited the characteristic hysteresis shown with the macroscale devices. In addition, we showed that the conduction model followed the macroscale devices. However, it was discovered that the current levels in both measurements did not scale properly. This anomaly was associated with device structure, resulting in field enhancement from the AFM tip in the c-AFM measurements and delocalized electric field across the nanoscale gap for the gap cells. Despite this, the presence of the hysteresis in both measurements confirmed the potential for the memory devices to operate at the nanoscale.

Chapter 3 – Multi-Layer Organic Memory Devices

The single-layer memory devices were useful for proof of principle, but not technologically viable due to the relatively low current difference between on and off states. We developed a multi-layer structure by introducing a capping layer (PS) on top of the active layer (PVP+C₆₀) to increase the current levels in the hysteresis. The single-layer devices suffered from partial charging of the C₆₀ within the film due to the symmetry in the device structure. Thus, discharging the C₆₀ molecules on the positive electrode meant that the C₆₀ near the negative electrode would also charge. By adding the capping layer, the symmetry is broken, allowing the charging of the C₆₀ molecules through the bottom contacts only. This enabled us to achieve an on/off ratio of 10³. Adhesion between the capping and active layer was confirmed by cross sectional scanning electron microscopy (x-SEM) and the roughness of the multi-layers was measured to be a few nanometers, as determined by AFM. The multi-layer devices exhibited asymmetrical I-V curves with a large hysteresis occurring only on the negative region. Based on the I-V curve, it was determined that the device can be written at +3V, erased at -3V, and read at -1V. The threshold voltage to erase information depended on the maximum voltage to perform the write operation. A minimum voltage of +1.4V, corresponding to the charging energy for C₆₀, was required to achieve a hysteresis. RWE operations could be easily performed due to the 10³ on/off ratio. We also measured the switching time to be on the order of 10 ns, as was the case with the single-layer devices. In addition, the multi-layer device exhibited data retention over two hours without any significant degradation in the current, in contrast to the single-layer devices. This suggests that the multi-layer devices are more stable. We confirmed the enhanced stability through high temperature (85°C) I-V measurements and data retention

tests. In addition, we observed retention after 5 days and preservation of the I-V curves after 16 months. We also attempted nTP to fabricate nano sized cross-point devices, following different procedures from the literature. It was found that the annealing method worked best and currently work is ongoing to produce devices using this procedure.

Chapter 4 – Conduction Mechanism in Organic Memory Devices as a Function of Temperature

To develop a model for both the conduction and memory mechanism associated with the multi-layer devices, we performed I-V measurements with respect to temperature (I-V-T) down to 4.2 K, using the Janis cryogenic probe station. Measurements were taken for metal-insulator-metal (MIM) device structures for both pure PS and PVP with both Au and Al contacts. The three devices, Al/PS/Al, Au/PS/Au, and Al/PVP/Al exhibited symmetrical I-V curves with very little temperature dependence. All three devices operate with direct tunneling under low bias and Fowler-Nordheim tunneling at high bias. The hysteresis in all three devices was small and showed very little temperature dependence. I-V-T data was also taken for the multi layer devices (Al/PVP+C₆₀/PS/Au). The multi-layer devices also showed very little temperature dependence. The I-V curves with respect to temperature were very similar I-V curves in Chapter 3, however the threshold voltage varied somewhat for both the write and erase thresholds. This could be a sign of accelerated aging and will need further analysis during future work. Both conduction mechanisms can be described by direct tunneling below a threshold voltage of -1.3V, and by Fowler-Nordheim tunneling at higher biases. The threshold is similar to the single-layer devices (-1.3V versus +1.3V), suggesting that the active layer is the controlling layer while the capping layer is passive. The ratio of hysteresis was temperature independent.

Based on the I-V-T data for all three devices we derived a rough band diagram to help explain the model for conduction and memory effect. However, without a detailed understanding of the electronic structure of both PVP and PS, the band diagrams are speculative, and measurements such as ultraviolet photoemission spectroscopy (UPS) and inverse photoemission spectroscopy (IPES) are needed to understand the band structure and will need to be performed in the future. Despite this, our model is a good starting point for now to help us understand the underlying physics within the memory devices. We also derived band diagrams for each memory operation. The key point is the presence of localized states that allow tunneling across the relatively thick (~ 30 nm thick) PVP layer. They also allow for tunneling in and out of the lowest unoccupied molecular orbital (LUMO) of the C_{60} molecules during both write and erase operations, where Fowler-Nordheim tunneling occurs to lower the barrier between the localized states and C_{60} and the barrier between the C_{60} and the Al electrode.

5.2 Recommendations for Future Work

I. Nanoscale Cross-Point Devices

In Chapter 2, we successfully demonstrated the characteristic hysteresis at the nanoscale using both c-AFM and nanoscale gap-cells. However, nanoscale cross-point devices are needed for direct proof of nanoscale operation. Currently, nTP is the only viable technique to fabricate the nano cross-point devices from organic materials. In Chapter 3, we made attempts to transfer print electrodes onto the PS layer of the multi-layer devices. These attempts lead to the transfer printing during annealing as the method which ultimately proved to be successful for our devices. The next step is to translate the annealing method to the nanoscale and fabricate the nano cross-point devices to investigate whether memory operations

can be translated to small dimensions. Information, such as stability, yield, variations, and fabrication methodology is needed to bring these devices closer to realization.

In addition to nanoscale devices with printing, stacked structures should also be considered to improve the storage densities. Since the solvents used for PVP and PS do not attack the other polymer, numerous multi-layered devices could be stacked vertically to achieve high storage densities without the need for nanodevices.

II. Long Term Stability

In Chapter 3, we showed that the multi-layer devices are stable up to 85°C and in ambient conditions. However, the variations in threshold voltages observed in Chapter 4 suggest there are likely to be issues in terms of stability with time. To understand this, long-term stability and memory retention tests must be performed. This could be done by measuring device characteristics over an extended period of time at high temperatures and humidity levels (the so called 85°C and 85% humidity test). These accelerated tests should provide detailed knowledge of device degradation in realistic operation conditions. In addition, long-term endurance tests are needed to see the memory cycle life. For example, how many write or erase cycles can the device operate, until charging of the C₆₀ becomes impossible due to some aging effects. Also, how long C₆₀ molecules can store charge should also be investigated with realistic conditions. These tests are important since the current and new memory technologies have data showing memory retention and operation well into several decades and endurance tests up to 10¹⁰ cycles [1].

III. Measuring the Electronic Band Structure of PVP and PS

Detailed information regarding the band gaps and band alignments with electrodes for PVP and PS is lacking. This information is crucial for accurately determining the positions of the various energy levels in the multi-layer devices. A thorough investigation of band alignment using ultraviolet photoemission spectroscopy (UPS) and inverse photoemission spectroscopy (IPES) measurements should improve the preliminary band schematics presented in Chapter 4. A better understanding will allow for further optimization of the C₆₀/polymer memory system. In addition, the challenges associated with the development of the technology can be understood and overcome with a better grasp of the underlying physics.

IV. Transmission Electron Microscopy

Although TEM analysis on organic materials is challenging due to beam damage, dedicated investigation of the multi-layer device could yield valuable information. Specifically, knowledge regarding the distribution of the C₆₀ molecules in the PVP matrix can be obtained. Indeed TEM studies have been performed on C₆₀ contained in conjugated polymers used in organic solar cells. Such investigations have elucidated the operating mechanism. Similar knowledge could be obtained in these devices if careful TEM analysis could be performed.

5.3 References

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Appendix A. Device Fabrication

Here we describe the cleaning and fabrication of the various devices used in this dissertation. The fabrication techniques discussed, are for the macroscale single and multi-layer devices for current versus voltage (I-V) measurements. In addition, fabrication of devices for capacitance versus voltage (C-V) measurements is explained. Also, the electron beam (E-beam) lithography steps are outlined here. We will now outline the procedure for each of the sections, beginning with macroscale devices.

A.1 Macroscale Devices

Devices were fabricated on standard microscope glass slides as the substrate. The slides were cut, using a diamond scribe, into 2.5cm-by-2.5cm square pieces. The substrates were then cleaned prior to fabrication. We will outline the cleaning procedure prior to the fabrication procedure.

Substrate Cleaning Procedure

1. Place glass substrates into a clean glass Petri dish. Make sure substrate lie flat and are not on top of each other
2. Pour HPLC grade acetone into the Petri dish until the acetone level is slightly higher than the height of the glass slides
3. Cover the Petri dish with parafilm to prevent contamination during sonication
4. Place the Petri dish in a bath ultrasonicator, allowing it to float on top of the water
5. Sonicate for 15 minutes
6. Remove the Petri dish from the bath and drain the acetone into the appropriate hazardous waste receptacle

7. While draining squirt isopropanol (HPLC grade) onto the substrates to prevent the acetone from drying on the surface
8. Rinse the substrate with isopropanol by filling a small amount of isopropanol and swirling the Petri dish. (Repeat 2 times).
9. Repeat steps 2-6 with isopropanol instead of acetone
10. Repeat steps 7-8 with deionized water
11. Fill the Petri dish with just enough deionized water to cover the glass slides. Be sure not to over fill as it will sink in the sonicator.
12. Repeat steps 4-5 except for 10 minutes.
13. Remove Petri dish from sonicator
14. Using a clean pair of tweezers remove each glass substrate and rinse with fresh deionized water and blow dry with pure dry Nitrogen (N_2)
15. Place each of the dry substrates into a clean plastic Petri dish for storage and transport.

Fabrication Procedure

Deposition of Bottom Contacts

1. Open thermal evaporate and prepare it for the appropriate metal (Al for the bottom contact) for both single and multi-layer devices
2. Setup appropriate shadow mask
3. Place clean glass slides (face down) on to the shadow mask
4. Pump down the evaporator
5. Evaporate 80 nm of the metal at a rate no greater than 1nm/s to ensure a smooth film
6. Remove samples from the evaporator and store them into a clean plastic Petri dish

Polymer Solution Preparation

Poly (4-vinyl phenol) and C₆₀

1. Using a clean spatula, weight 50 mg of Poly (4-vinyl phenol) (PVP) in a 3 ml vial
2. Weigh 1mg of C₆₀, using weighing paper, and place in same vial holding the PVP
3. Measure out 2ml of isopropanol and pour into the vial
4. Cap the vial and wrap with parafilm to seal the vial
5. Sonicate for 1 hour

Polystyrene

1. Using clean tweezers weight 100mg of Polystyrene pellets and place in a 25 ml vial with a foil lined cap
2. Measure 10ml of toluene and pour into the vial.
3. Cap the vial and wrap with parafilm to seal the vial
4. Sonicate for 30 minutes

Spin Coating

Single-Layer Devices

1. Using 6 mm wide Kapton tape (Polyimide based tape that is inert and developed by DuPont), tape on edge of the substrate, covering part of the evaporated Al track. Also, tape the adjacent edge where the top contact pads would lie.
2. Using dry N₂, blow the surface of the substrate to remove any dust contaminates
3. Place masked substrate on the chuck in the spin coater and turn on the vacuum to hold the substrate.
4. Set the RPMs to 7400 RPMs, the spin time to 120 seconds, and a slow ramp speed
5. Spin the substrate to test it is being held by the vacuum chuck
6. Restart the spin coater and wait until it reaches 7400 RPMs
7. Dispense a stream of the PVP+C₆₀ solution using a pipette

8. After the spin coater is finished transfer to a clean Petri dish

Multi-Layer Devices

1. Follow steps 1-7 for the single-layer device procedure
2. Reset the spin coater to 7000RPMs, while preserving the other parameters
3. Start the spin coater and wait until it reaches 7000RPMs
4. Dispense a stream of PS solution using a pipette on top of the PVP+C₆₀ layer
5. When finished, remove substrate and place in a clean Petri dish for transportation

Deposition of Bottom Contacts

Single-Layer Devices

1. Open up the evaporator and prep it for Al deposition
2. Place shadow mask
3. Remove the Kapton tape from the polymer deposited substrates
4. Position substrate so that the evaporated line are perpendicular to the bottom contacts
5. Startup the evaporator
6. When fully pumped down, evaporate 80 nm of the Al, at a slow rate (~0.5nm/Sec)
7. Remove completed single-layer memory devices

Multi-Layer Devices

1. Repeat steps 1 -7 of the single-layer devices, using Au instead of Al

A.2 Devices for C-V Measurements

Devices were fabricated for C-V measurements to demonstrate capability of charging the C_{60} molecules at room temperature. These devices were based on a Metal-Insulator-Semiconductor (MIS) design with p-type Silicon (Si) as the substrate. The Si was purchased from University Wafer without any grown oxide. The substrate was cleaved, using a diamond scribe and tweezers, along the crystalline plane into 1cmx1cm substrates. The substrates are cleaned using a piranha solution, as outlined below followed by the fabrication procedure.

Si Substrate Cleaning Procedure

1. Create a piranha solution by mixing sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) at a ratio of 70% H_2SO_4 and 30% H_2O_2
2. Carefully place substrates in solution while ensuring that do not over lap
3. Wait 20 minutes and remove them
4. Immediately rinse with deionized water and blow-dry with dry N_2
5. Place in a clean Petri dish for transport.

Fabrication Procedure

Deposition of Ohmic Back Contact

1. Immediately following the cleaning procedure, open evaporator and setup for Al deposition
2. Load Si substrates top side up, leaving the back side exposed for evaporation
3. Close and pump down the evaporator
4. Evaporate 250nm of Al
5. Remove samples and transfer to an oven capable of heating in an inert environment (such as N_2)
6. Anneal the samples at 490°C for 10 minutes to form the ohmic Al contacts to the back of the Si substrates

Solution Preparation

Pure PVP

1. Weigh 50 mg PVP in a 3 ml vial
2. Measure 2 ml of isopropanol and pour into the vial
3. Cap and seal with parafilm
4. Sonicate for 1 hour

PVP+C₆₀

1. Follow procedure outlined in the solution preparation section for PVP+C₆₀ in the Macroscale Device section

Spin Coating

Pure PVP

1. Blow the surface with dry N₂ to remove any contaminants
2. Set spin coater to 7400 RPMs, 120 seconds, a slow ramping rate
3. Place sample on to the chuck and engage the vacuum
4. Start spin coater and wait until it reaches 2000 RPMs
5. Using a pipette, dispense a stream of the PVP solution on the sample
6. Remove and place in a Petri dish for transportation

PVP+C₆₀

1. Repeat the pure PVP procedure but with the PVP+C₆₀ solution at 7400 RPMs
2. When finished, reset the spin coater for 2000 RPMs
3. Repeat steps 4 and 5 with the PVP solution
4. Remove and place in a Petri dish for transportation

Deposition of Top Contacts

1. Setup evaporator for Al deposition
2. Setup a shadow mask with patterned 1mm diameter holes
3. Place the samples upside down on to the shadow mask
4. Pump down and evaporate 100nm Al
5. Remove completed C-V devices

A.3 Electron Beam Lithography

E-beam lithography was used to fabricate nano-scale gap cells to demonstrate the hysteresis of the PVP+C₆₀ system at the nanoscale. The procedure involves three main steps patterning a resist, deposition of a metal, and lift-off of the resist. Each step is summarized below. The substrates used were Si substrates with 400 nm of thermally grown oxide to prevent shorting. The substrate was cleaved into 1.5cm-by-1.5cm samples. Prior to the E-Beam, the Si substrates were cleaned using the procedure outlined in the substrate cleaning procedure section for the macroscale devices.

Patterning of Resist

1. Design the desired pattern in AutoCAD
2. Program a spin coater to perform two steps. The first step spins the substrate at 500 RPMs for 5 sec to remove excess resist. The second step revs up the speed to 3000 RPMs for 30 seconds.
3. Setup a hot plate for 190°
4. Load a substrate into the spin coater and engage the vacuum
5. Using a plastic pipette, transfer enough solution of Polymethyl methacrylate (PMMA) to cover the entire substrate.
6. Start the spin coater and allow it to run through the two step program
7. Transfer the substrate to the hot plate and anneal the sample for 30 minutes

8. Load sample into the Scanning Electron Microscope (SEM) used for E-beam lithography
9. Load pattern into the computer and run a simulation
10. Optimize pattern to minimize time
11. Set the parameters based on the simulation, such as dosage and dwell time
12. Run the program to write the pattern into the resist
13. Remove the sample and submerge in methyl isobutyl ketone (MIBK) which is diluted at a ratio of 1 to 3 with isopropanol to develop the pattern
14. Agitate for 30 seconds
15. Rinse with isopropanol and blow-dry with dry N₂
16. Place samples into a Petri dish for transportation

Metal Deposition

1. Open evaporator and prepare it for the appropriate metal required for deposition.
2. Load samples face down to evaporate onto the patterned resist.
3. Pump down and evaporate 50-100 nm of the desired metal
4. Remove sample and store in a clean Petri dish when finished

Lift-Off

1. Fill a beaker half way with a commercial remover called Nano Remover PG
2. Submerge the sample
3. Allow to soak, while gently agitating every couple of minutes, until the resist is removed
4. Once removed, the metal pattern should be clearly visible
5. Rinse thoroughly with deionized water and blow-dry with dry N₂
6. Store device in a clean Petri dish for further processing

Appendix B. Instruments and Programs

B.1 Introduction

The instruments and equipment used in this thesis were commissioned and maintained by the author. The instruments were computer controlled through the standard IEEE 488 GPIB interface. The programs were also written by the author in Agilent's VEE Pro and are presented in the second section. Both the equipment and programs were instrumental to other research projects as well such as organic photovoltaics and transistors. The programs for these applications are not shown here for brevity.

B.2 Instruments and Equipment

Here we present photographs of the most commonly used equipment.

Electrical Probe Station Setup

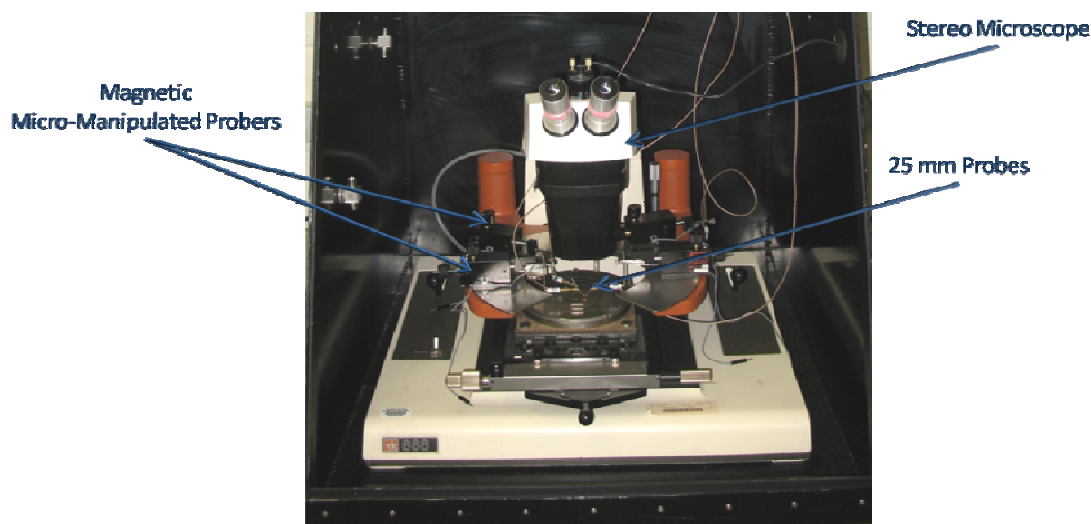


Figure B-1 – Electrical probe station housed inside a dark box to reduce noise, allowing for pA resolution. Connections were made using standard BNC cables as described in Chapter 2.

Current Meter and Voltage Source

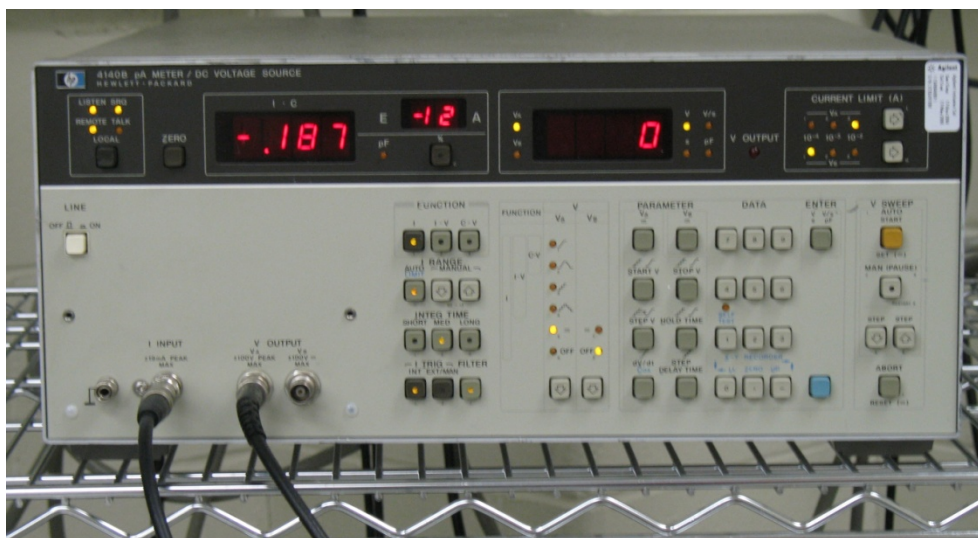


Figure B-2 – The HP 4140B pA Meter/DC voltage source, capable of measuring I-V and C-V.

Arbitrary Waveform Generator



Figure B-3 – Digital Precision 2020 Polynomial Waveform Synthesizer, used to generate high frequency Read-Write-Erase used in Chapter 2

I-V-T Station

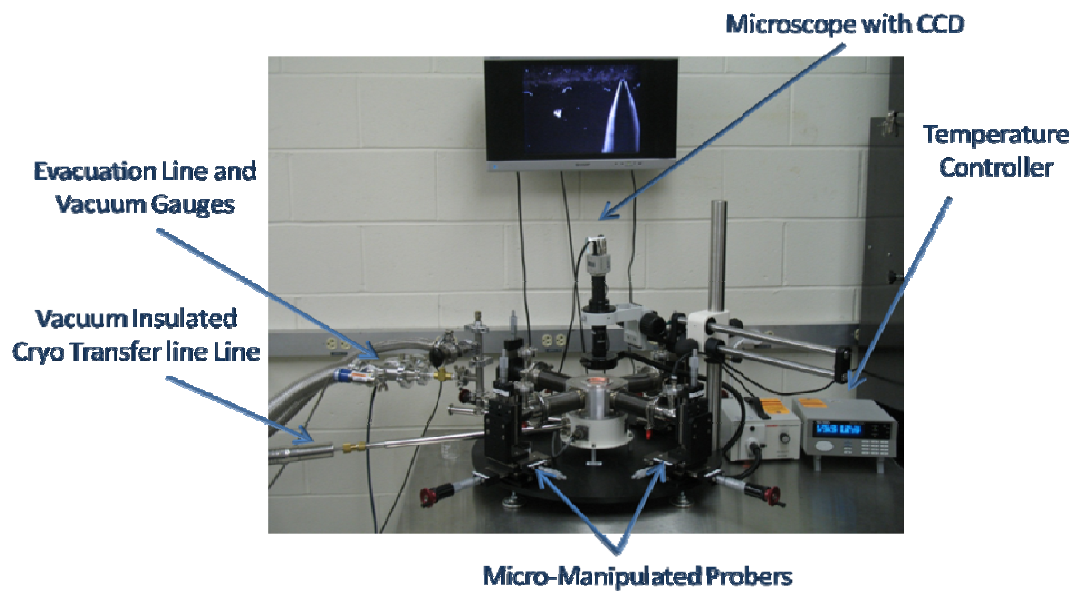


Figure B-4 – I-V-T station used to make I-V measurements with temperature down to 4.2K. LHe is pressurized through the cryo transfer line and the temperature controller uses a resistive heater to control the temperature to an accuracy ± 0.5 K

Pumping Station for the I-V-T Probe Station

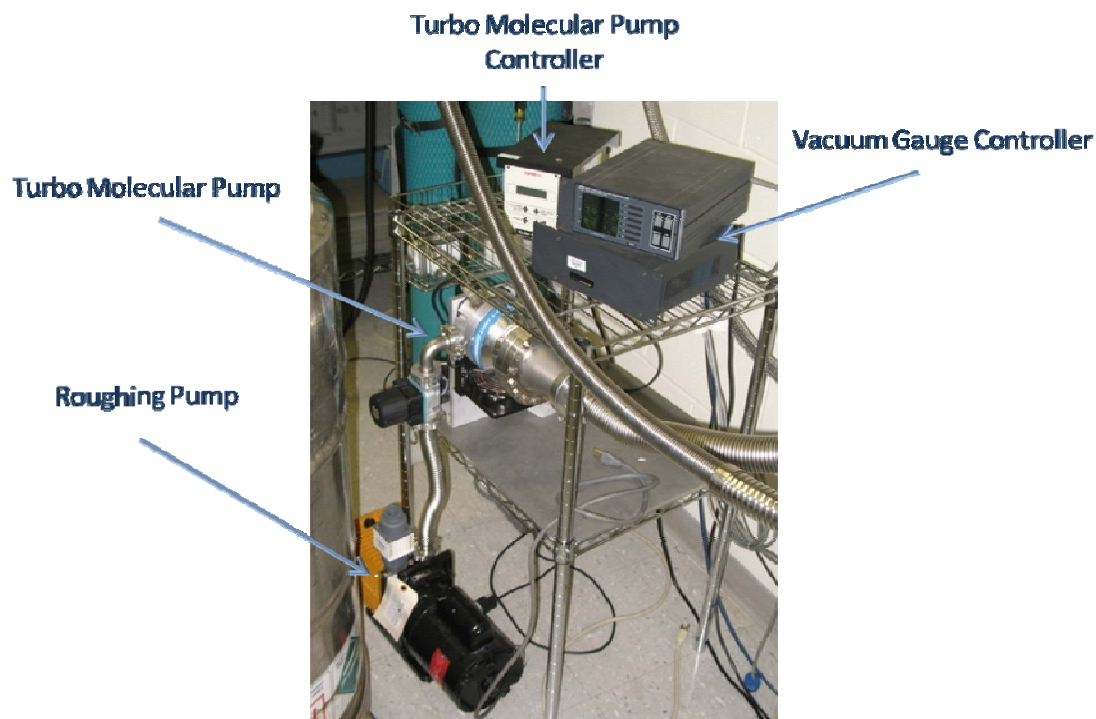


Figure B-5 – Pumping station used to pump down the I-V-T chamber to 8×10^{-5} Torr, required to achieve cryogenic temperatures without significant icing.

B.3 Programs

Memory I-V Sweep Rate

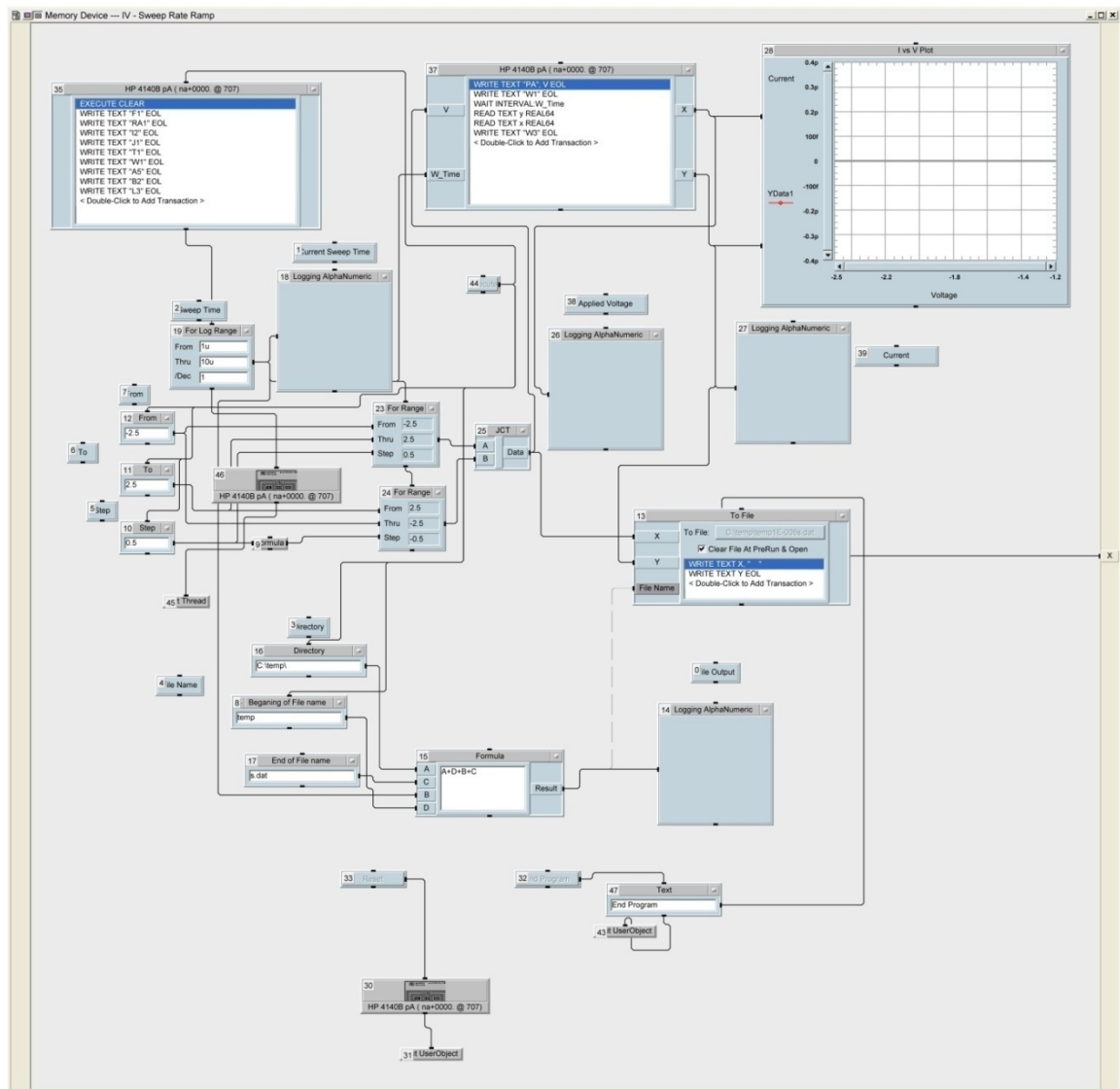


Figure B-7 – Program for performing I-V measurements at varying sweep rates.

Memory Waveform — Long Pulses

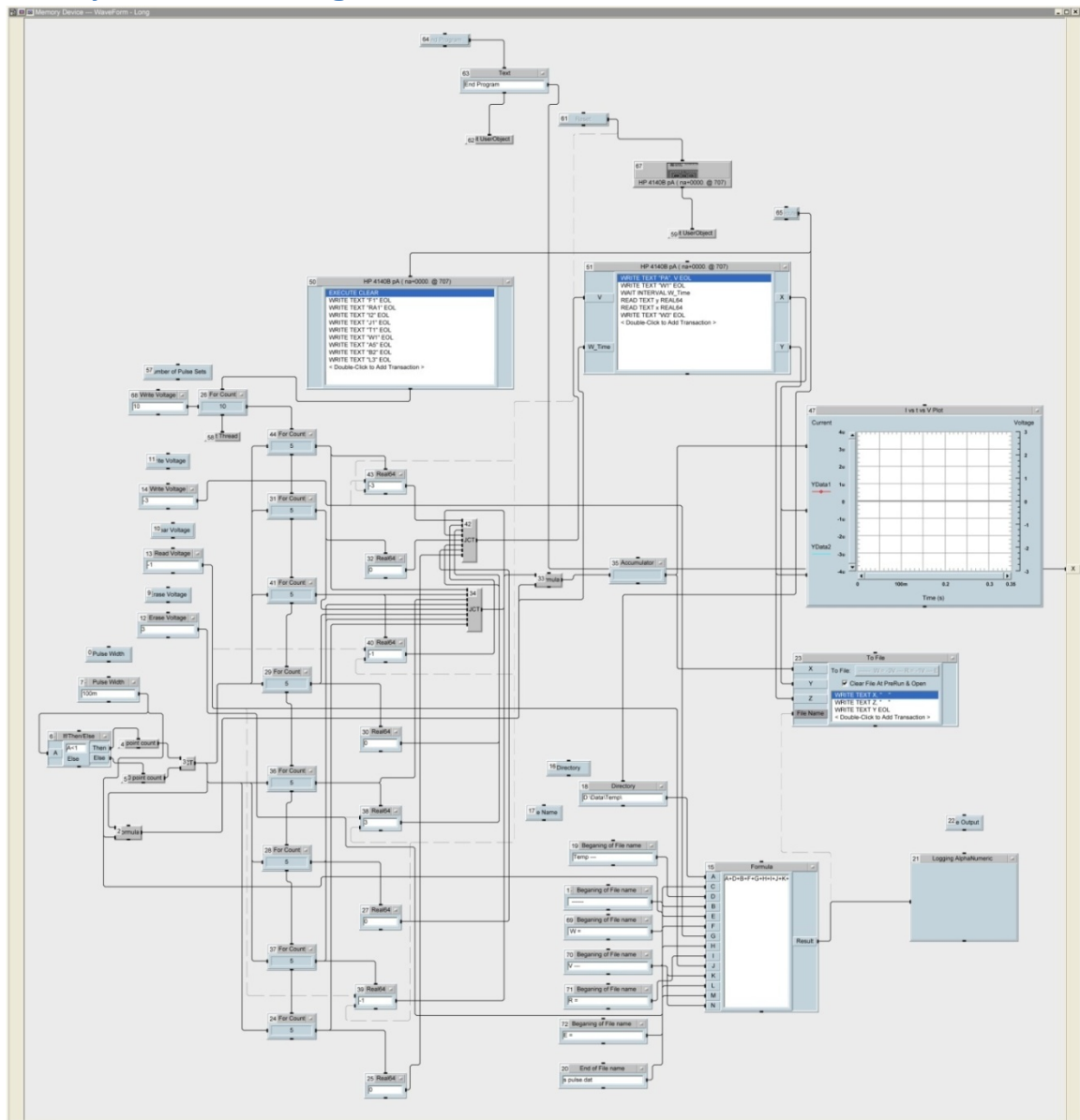


Figure B-8 – Performs multiple memory operation at time scales greater than 100µs.

Memory Retention

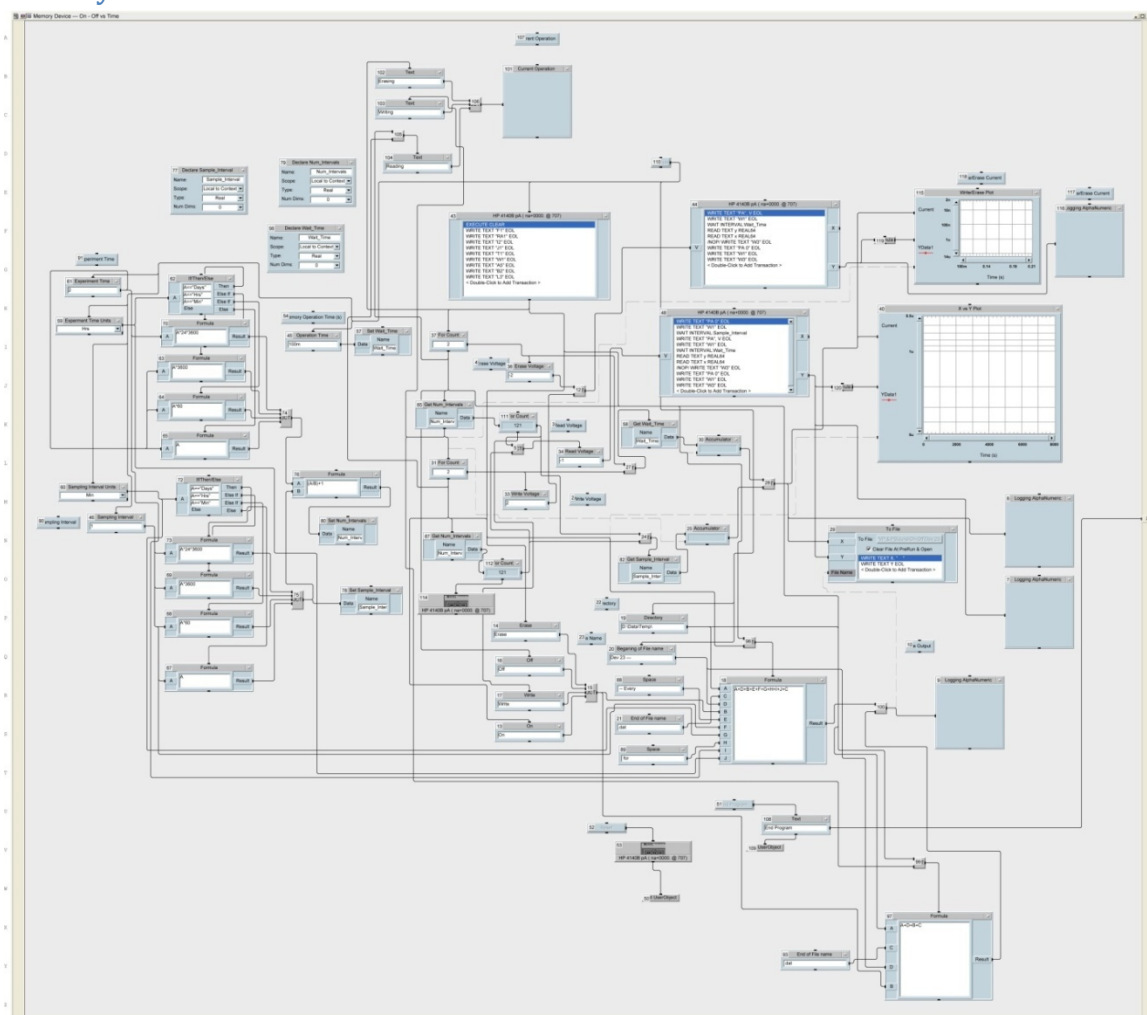


Figure B-9 – Program to test non-volatile memory retention for extended periods of time using the HP4140B.

I-V versus T

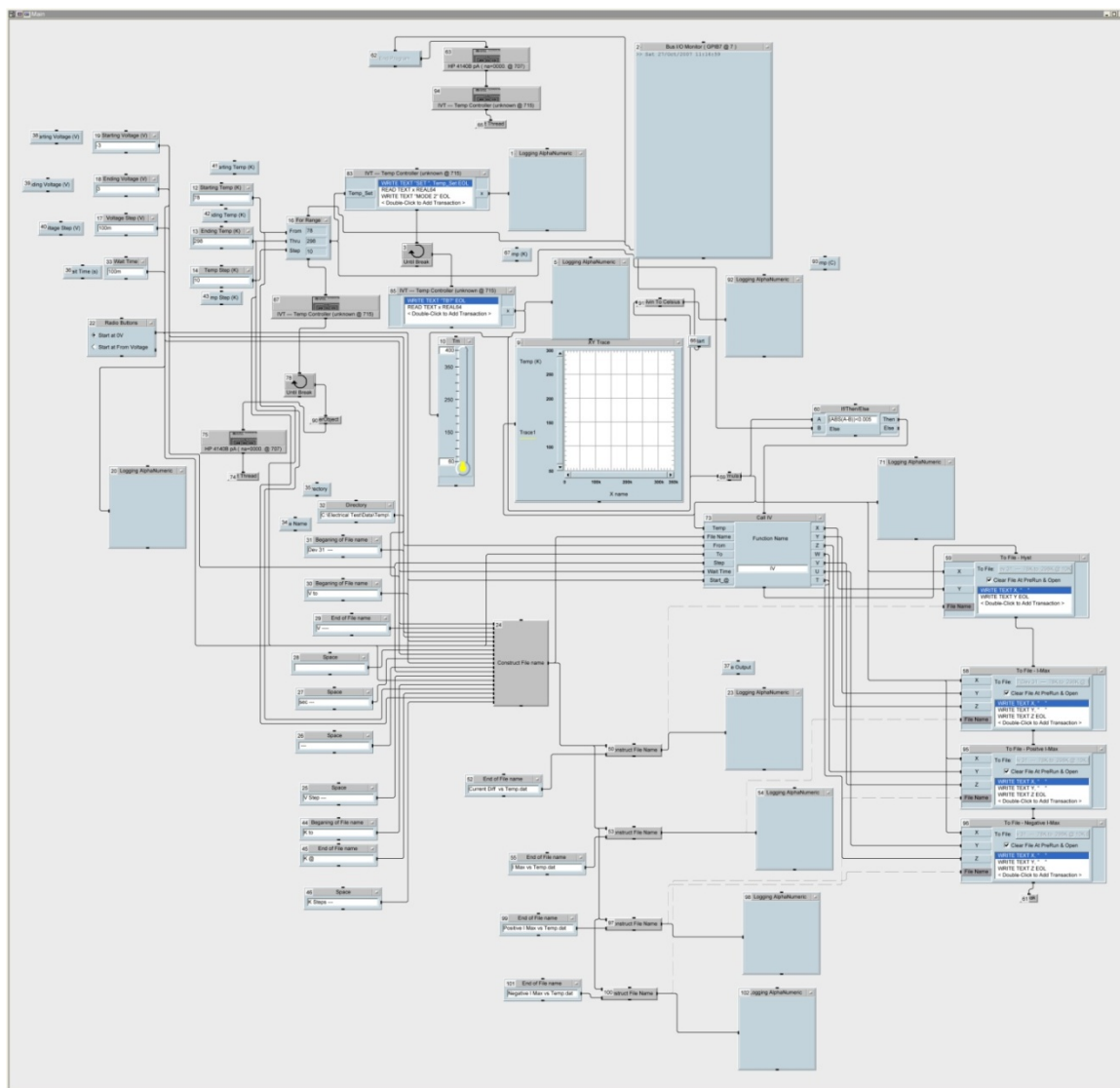


Figure B-10 – Main program for I-V-T measurements. This program reads and controls the temperature of the sample in the I-V-T probe station, using the temperature controller. Once the temperature is reached, the program holds it and activates a subprogram to perform the I-V at the given temperature.

Sub I-V Program

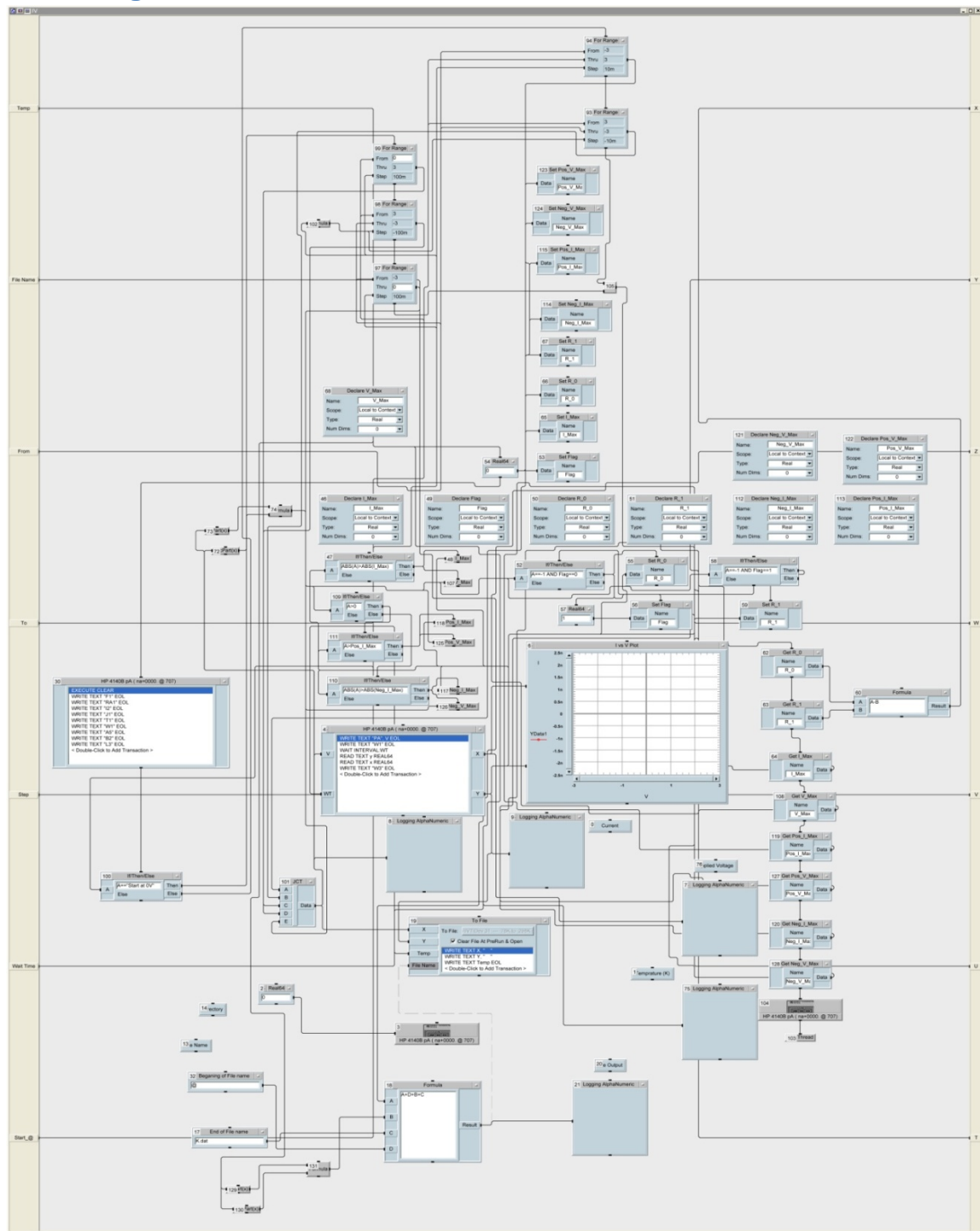


Figure B-11 – Sub program to perform I-V measurements at a given temperature. Once finished it calculates the hysteresis at a given voltage and the maximum current per temperature.

Curriculum Vita

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Education:

| | | | |
|-----------|-------|--------------------|---|
| 2006-2008 | Ph.D. | Rutgers University | Materials Science and Engineering |
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| 2004-2007 | Graduate Research Assistant | Rutgers University | Materials Science and Engineering |
| 2004-2007 | Teaching Assistant | Rutgers University | Materials Science and Engineering |

Publications:

- 2007 G. Eda, G. Fanchini, A. Kanwal, M. Chhowalla, "Bundling dynamics of single walled carbon nanotubes in aqueous suspensions", Submitted
- 2006 A. Kanwal and M Chhowalla, "Stable, three layered organic memory devices from C₆₀ molecules and insulating polymers", Applied Physics Letters, 89 203103
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- 2006 S. Paul, A. Kanwal, and M. Chhowalla, "Memory effect in thin films of insulating polymer and C₆₀ nanocomposites" Nanotechnology, 17 145-151
- 2006 A. Kanwal and M Chhowalla, "Nanoscale Measurements in Organic Memory Devices from C₆₀ in Insulating Polymers" ," Mater. Res. Soc. Symp. Proc. Vol. 905E © Materials Research Society DD6.3

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- 2005 A. Kanwal, S. Paul, and M. Chhowalla, "Organic Memory Devices Using C₆₀ and Insulating Polymer," *Mater. Res. Soc. Symp. Proc. Vol. 830* © Materials Research Society D7.2