

DEVELOPMENT OF 4H SILICON CARBIDE JFET-BASED POWER
INTEGRATED CIRCUITS

by

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ABSTRACT OF THE DISSERTATION

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4H-Silicon Carbide (4H-SiC) is a promising semiconductor for the next generation of high power, high frequency, and high temperature applications. Significant progresses have been made on SiC technologies since 1990's. Superior device performance demonstrated by SiC discrete power devices is leading to the commercialization of SiC diodes and transistors targeting mid and high power level applications. As compared to the vertical power devices, the lateral device technology promises to fulfill the monolithic integration of both power devices and control circuits. SiC power integrated circuits (PICs) share similar advantages as Si PICs while providing a much higher power handling capability at higher frequency. In addition, SiC power junction field transistor (JFET) is promising for high temperature, reliable operation without suffering from the reliability problems faced by metal-oxide-semiconductor junction field transistors (MOSFETs) and bipolar junction transistors (BJTs). Therefore, the lateral JFET technology is investigated under this research.

This thesis describes design, fabrication, characterization, and further optimization and analysis of a novel vertical channel lateral JFET (VC-LJFET) technology in 4H-SiC and the demonstration of the world's first SiC power Integrated circuit. A double reduced surface electric field (RESURF) structure is applied to achieve higher voltage and lower on-resistance for the power lateral JFET (LJFET). A 4-stage buffer circuit based on the resistive-load n-type JFET inverter is designed and integrated with the power LJFET to form a monolithic power integrated circuit. Important fabrication procedures are presented. The fabricated power LJFET demonstrates a blocking voltage of 1028 V and a specific on-resistance of $9.1 \text{ m}\Omega\cdot\text{cm}^2$, resulting in a record-high $V_{BR}^2/R_{ON,SP}$ figure-of-merit (FOM) of $116 \text{ MW}/\text{cm}^2$ for lateral power devices. The optimized RESURF structure demonstrates blocking capability of $120 \text{ V}/\mu\text{m}$ in 4H-SiC. The temperature dependences of important device parameters, such as threshold voltage, transconductance, and electron mobility, are also discussed. Based on the technology, the integration of a high performance lateral power JFET with buffer circuits has been demonstrated for the first time. The SiC LJFET power IC chips demonstrate a record high power level at frequencies up to a few MHz. An on-chip temperature sensing diode is implemented to monitor the chip junction temperature. The rise time and fall time around 20 ns for the SiC power LJFET are observed and remains unchanged even at a junction temperature as high as 250°C when driven by a Si MOS gate driver. The demonstration of SiC power integration technology points to the robust integrated power electronics applications in the harsh environment and boosts the power level of single-chip power electronic system from 100 W to 1000 W.

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1. INTRODUCTION

1.1 SiC Material and Process Technology Overview

Silicon Carbide (SiC) is one of the earliest few materials that are recognized as semiconductors and even the first Light Emitting Diode (LED) was first demonstrated by using SiC in 1907. Although SiC was named “the perfect semiconductor” by William Shockley back in 1950s, the difficulties of growing large size single crystals of SiC seriously delayed the development of SiC electronics. Till early 1990s, Cree started commercialization of SiC single crystal wafers, and since then significant research efforts have been spent in SiC growth and process technologies, power device engineering, and high temperature electronics. Continuous technology breakthroughs on the development of high quality SiC substrates and epilayers, SiC process technologies, and high voltage power devices and ICs, over the past twenty years, lead to the “Christmas Eve” of the SiC applications in high temperature power electronics.

Compared with Si and Gallium Arsenide (GaAs), wide bandgap (WBG) materials (energy bandgap larger than 2 eV) are necessary for high temperature electronics to avoid the excessive junction leakage current at temperatures higher than 200 °C. Generally, wide bandgap materials, such as SiC and Gallium Nitride (GaN), have good chemical stability and mechanical properties, high breakdown fields, and high saturation velocities, which make WBG semiconductors the promising materials for the next generation of high power, high frequency, and high temperature electronics. Table 1.1 lists the electrical parameters for selected semiconductor materials [1, 2].

Table 1.1 Material properties of the well-known semiconductors

	E_g (eV)	n_i (cm^{-3})	ϵ_r	μ_n ($\text{cm}^2/\text{V}\cdot\text{s}$)	μ_p ($\text{cm}^2/\text{V}\cdot\text{s}$)	E_C (MV/cm)	v_{sat} (10^7cm/s)	λ (W/cm·K)
Si	1.12	1.5×10^{10}	11.8	1350	450	0.3	1.0	1.5
Ge	0.66	2.4×10^{13}	16.0	3900	1900	0.1	0.5	0.6
GaAs	1.42	1.8×10^6	12.8	8500	400	0.4	2.0	0.5
GaN	3.39	1.9×10^{-10}	9.0	900	200	3.3	2.5	1.3
3C-SiC	2.36	6.9	9.6	800	320	2.0	2.0	4.9
4H-SiC	3.23	8.2×10^{-9}	9.7	960($\parallel c$), 800($\perp c$)	120	3.0	2.0	4.9
6H-SiC	3.0	2.3×10^{-6}	9.7	400($\parallel c$), 85($\perp c$)	90	3.0	2.0	4.9
Diamond	5.5	1.6×10^{-27}	5.5	2200	1800	5.6	2.7	20.0

Table 1.2 Figures-of-Merit (FOM) normalized to Si

	JFOM	KFOM	BFOM	BHFFOM	HMFOM	HCAFOM	HTFOM
Si	1	1	1	1	1	1	1
Ge	0.028	0.24	0.15	0.32	0.57	0.26	0.9
GaAs	7	0.45	16	11	3.3	4.8	0.2
GaN	756	1.6	677	81	9.0	75	0.1
3C-SiC	178	5.1	143	26	5.1	28	0.6
4H-SiC	400	5.1	585	71	8.4	69	0.4
6H-SiC	400	5.1	244	30	5.4	45	0.4
Diamond	2540	32	4940	568	23.8	207	1.5

Johnson FOM = $(E_C v_{sat} / 2\pi)^2$ for high frequency signal amplifiers [3];

Keyes FOM = $\lambda \sqrt{v_{sat} / \epsilon_r}$ for high speed switches [4];

Baliga FOM = $\varepsilon_r \mu E_C^3$ for unipolar low frequency power devices [5];

Baliga high frequency FOM = μE_C^2 for unipolar high frequency power switches [6];

Huang Material FOM = $E_C \sqrt{\mu}$; Huang Chip Area FOM = $\varepsilon_r E_C^2 \sqrt{\mu}$; Huang Temperature FOM = $\lambda / (\varepsilon_r E_C)$; [7].

Figures-of-Merit (FOM) based on material properties are used to evaluate the device performance and semiconductor materials targeting different applications. Among the FOMs listed in Table 1.2, BFOM is widely used for the evaluation of a unipolar power device when the conduction loss dominates its total power loss. Another regularly quoted FOM, V_{BR}^2 / R_{ON_SP} , is related with BFOM by

$$BFOM = \varepsilon_r \mu_n E_C^3 = \frac{1}{\varepsilon_0} \frac{V_{BR}^2}{R_{ON_SP}}, \quad (\text{Eq. 1.1})$$

and it is widely quoted to compare the DC performance of power transistors. Reported in 2004, HFOMs are more indicative from the application point of view [7]. HFOMs include HMFOM for evaluation of both conduction and switching losses, HCAFOM (chip area FOM) for comparison of chip areas, and HTFOM for the junction temperature variation. All HFOMs are based on the assumption of balanced conduction loss and switching loss, similar power rating, and identical gate driving currents. According to Table 1.2, 4H-SiC devices have 8.4 times lower power losses than Si, 69 times smaller chip area, and about 1.5 times higher temperature rise if both are designed to operate under similar voltage and current conditions. Note that the FOM number may be different because of diversified references. As illustrated in Table 1.1 and 1.2, GaN shows comparable mobility, breakdown field, and saturation velocity as SiC but only 1/3 of

thermal conductivity of SiC that indicates worse FOMs related with thermal conductivity. Furthermore, GaN is a direct bandgap semiconductor resulting in a short minority carrier life time which is undesirable for bipolar device operation. In the mean time, defect density of GaN materials are still several orders higher than SiC although huge progress is making on the material growth of GaN. Among the three regular polytypes of SiC materials, 4H-SiC has the best FOMs for power switching applications.

With the commercialization of micropipe-free 4 inch SiC wafers in 2007, it almost hits the right time to start the cost-effective, large scale SiC unipolar FET device fabrication. In ICSCRM2007, Japan, Toyota claims that SiC technologies could be used in power electronics for its hybrid vehicles as early as 2010 [8].

In order to develop superior devices, SiC process technology has received intensive efforts over the past twenty years. Thanks for the Si technology developed in a half century, SiC technology follows similar technical traditions and shares most of the process modules from Si technology. Furthermore, specialized process technologies for SiC etching, selective doping and dopant activation, and ohmic and Schottky contact structures, etc. have also been well developed leading to commercialization of 4H-SiC Schottky Barrier Diode (SBD) [9, 10] and demonstration of other rectifiers and switches with superior performance. The comprehensive review of SiC process technology development has been summarized in several books published over the past few years [11-14].

In addition to the process modules descended from Si technology, such as lithography, dielectric and metal deposition and patterning, oxidation and passivation, and packaging, etc., the processes involving physical (implantation and annealing) and chemical

reactions (plasma etching, oxidation, and ohmic contact formation) with SiC need specialized technical efforts. SiC dry etching can be carried out by either Reactive Ion Etching (RIE) or Inductively Coupled Plasma (ICP) etching in the carbon fluoride (CF₄), chlorine, or sulfur hexafluoride (SF₆) based oxygen plasma. Further efforts need to be focused on reducing the roughness on the etched mesa or trench sidewalls, which is critical for the gate or base-emitter performances of trench devices, as well as high field, etching created termination regions.

Selective doping is a key technology for device engineering. Because of their extremely low diffusion coefficients of dopants in SiC, the diffusion process is practically unfeasible for selective doping in SiC. The widely accepted dopants, both implanted and grown-doped in SiC, are nitrogen (N) for the n-type and aluminum (Al) for the p-type because of their lower ionization energy and reasonable solid solubility in SiC. Compared to the nitrogen as n-type dopant, phosphor has higher activation efficiency at high concentration resulting in lower sheet resistance [15] which is desirable for n⁺ ohmic contact formation. However, lighter atomic weight of nitrogen is preferable to form relatively deep structures, such as well, tub, buried layer, etc., in SiC, and the reduced implantation lattice damage is expected for nitrogen compared to phosphor. Boron (B), a p-type dopant for Group IV semiconductors, has smaller atomic mass compared to aluminum. Unfortunately, 0.285 eV of ionization energy in 4H-SiC [16] is too high and the out-diffusion of boron atoms in 4H-SiC at high annealing temperature introduces extra difficulties on doping redistribution control [17, 18]. Al has an ionization energy of 0.19 eV [19], therefore even the electrically active Al dopants cannot be completely ionized at room temperature. Both implanted dopants need to be thermally activated to

form the electrically active dopants by replacing either Si or C atoms in SiC crystal structure. Much higher post implantation annealing temperature than that needed in Si technology, e.g. at least 1500 °C, is necessary for the activation of both n-type and p-type dopants in SiC. Even temperatures as high as 1700 °C are needed to fully activate the high concentration Al implanted p⁺⁺ region. At such high temperature, SiC starts to dissolve and form very rough surface. Different annealing technologies are therefore developed to fully activate implanted dopants while maintaining good surface quality. Among the annealing techniques, such as dummy wafer capping with SiC powder to supply an additional vapor pressure [20], Aluminum Nitride (AlN) capping [21], and high temperature rapid temperature annealing (RTA) [22], the graphite film capping converted from a layer of photo resist (PR) achieves the excellent annealing results [23] with relatively low cost and convenience. Another category of selective doping techniques includes the etch-and-regrowth [24] and selective-epitaxial growth technologies [25]. These techniques offer better quality layers and the doping profile could be tailored for specific device requirements. However, high growth temperature (>1500 °C) is required and tough process control for the growth is expected.

Compared with n-type dopants in SiC, the p-type ohmic contacts to SiC are more challenging because of the higher ionization energy of p-type dopants and the lower activation efficiency at high doping concentration. Among the diversified ohmic contact studies, nickel (Ni) based ohmic contacts to both n-type and p-type SiC are widely implemented in device fabrication. The specific contact resistance of Ni contacts could be as low as $6 \times 10^{-6} \Omega \cdot \text{cm}^{-2}$ and $1.5 \times 10^{-4} \Omega \cdot \text{cm}^{-2}$ for n and p type 4H-SiC with implanted doping concentrations of $1 \times 10^{19} \text{ cm}^{-3}$ and $1 \times 10^{21} \text{ cm}^{-3}$ respectively [26]. With the

addition of other metal layers, the Ni/Ti/Al and Ni/AlTi/Ni contacts to p-type 4H-SiC could be both reduced into $10^{-5} \Omega \cdot \text{cm}^{-2}$ range. In comparison, titanium silicide (TiSi_2) in the modern CMOS technology gives contact resistance in the order of 10^{-6} to $10^{-7} \Omega \cdot \text{cm}^{-2}$ for both n+ and p+ Si [27], which is almost an order higher than that of the best n-type contacts to SiC. As for the high power unipolar device implementations, the contact resistance of $10^{-5} \Omega \cdot \text{cm}^{-2}$ is usually negligible compared to the drift region resistance. However, detailed discussion on the device on-resistance will be presented in chapter 4 to address the more stringent contact resistance requirement of lateral power device than the vertical device. By considering the benefit of extremely simplified ohmic contact process, Ni silicide is chosen for both n and p contacts to 4H-SiC in this study.

In summary, there are no major technical obstacles at current stage for SiC to penetrate into Si power electronics market except its prohibitive material cost. However, it is also interesting to note that some benefits resulted from SiC technology could offset part of total cost for the SiC power electronics system where SiC power switches are implemented. First of all, the fabrication cost of SiC device and integrated circuit (IC) could be lower or at least no more than Si technology. With the exception of the specialized high temperature ($>1700^\circ\text{C}$) furnace for post implantation annealing, almost all other tools that have been well developed for Si Fab could be readily used. Of course, those specialized technologies for SiC need to be addressed in the SiC Fab as well. Most process modules from Si and even specialized process modules for SiC can be tailored to be compatible with Si technology and with a lower running cost in the “outdated” 4-inch or 6-inch Fabs. In addition, the stringent contamination control in a Si CMOS Fab, especially between the front end and back end process modules, could be relieved in the

SiC Fab. Those fast diffusion metal ions in Si cannot diffuse inside SiC even at very high temperatures ($>1000\text{ }^{\circ}\text{C}$). Secondly, compared to Si power chips, SiC counterparts have smaller die sizes for the same power rating, which would enhance the probing yield by relieving the effects of device killer defects in the process. In addition, the line yield of SiC wafers would be higher because of their lower scrap probabilities due to its tougher physical properties. Finally, while most importantly, the overall system cost saving by implementing SiC power devices and ICs is always the impetus for the advanced SiC research. Specifically, SiC power devices can enable substantially higher switching frequencies in a power electronics system and/or significantly higher system efficiency. This serves to reduce the sizes of capacitors, inductors and heatsinks. Considering the rapidly-rising raw material cost, such benefits will become increasingly attractive in the years to come.

1.2 SiC Power Devices

1.2.1 Unipolar or Bipolar Power Devices

In contrast to unipolar power devices, bipolar ones have smaller on-resistance while larger switching power loss because of the conductivity modulation caused by the minority carrier injection. Therefore, bipolar power switches are usually used at higher power rating but lower switching frequency. As shown in Fig. 1.1, the power dissipation for the device safe operation limits different types of devices into specific applications. The traditional Si bipolar junction field transistor (BJT) was replaced by power MOSFET in applications where the operating voltages are below 200 volts and by the insulated gate bipolar transistor (IGBT) in applications where the operating voltages range from 200 volts to 1500 volts [28]. Power thyristors are still dominating high power and low frequency applications. The application boundary shown in Fig. 1.1 could not be clearly defined and are dynamically changing because new device structures and semiconductor materials are actively developing into practical applications. Si super junction power MOSFET developed over the past 10 years is pushing its voltage rating up to at least 600 volts while offers high frequency operation at the same time [29-31]. With the introducing SiC, not only the power-frequency boundary needs to be redefined but also the traditionally-obsolete power device types, e.g. JFET and BJT, are reviving and will be discussed in more details later. The theoretical study on the SiC super junction power device also predicts breaking through the theoretical unipolar SiC limit in the future[32].

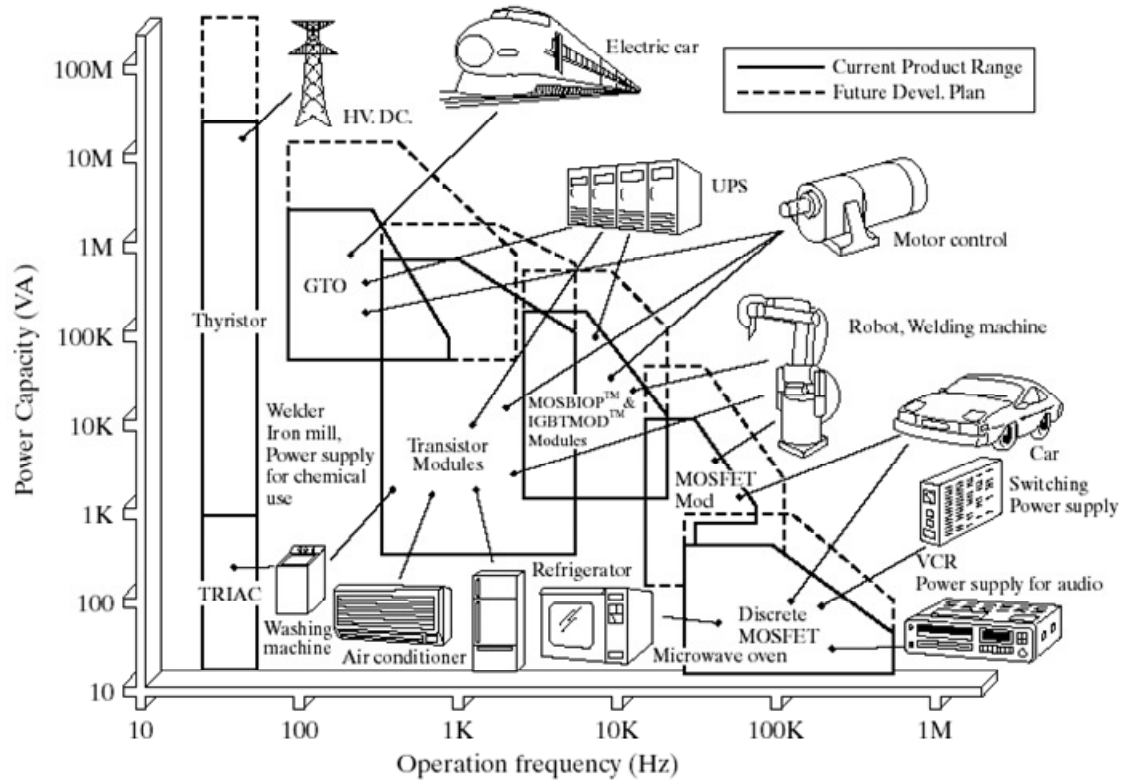


Fig. 1.1 Applications of power electronics and the power-frequency boundaries for different Si power devices.

There is no such illustration as that in Fig. 1.1 for SiC power device yet. However, several theoretical studies have been published to compare SiC unipolar and bipolar power devices. Huang, *et al* [33] concludes that SiC NPN transistors for the 4.5-kV applications have comparable switching loss as that of the SiC MOSFETs, but have lower conduction loss especially at higher current level. Tamaki, *et al* [34] has concluded that SiC unipolar power switches are advantageous in comparison to bipolar power switches at voltages up to as high as 20 kV when switching frequency is above 800 Hz for a device junction temperature of 175 °C. Das, *et al* [35] compared SiC power MOSFET and SiC n-IGBT and concluded that the SiC MOSFET remains the device of choice up to 10 kV

while the SiC n-IGBT becomes more attractive at higher voltage and higher temperature. Therefore it is reasonable to predict the better performance of SiC unipolar FETs in applications where the operating voltages rates at least up to 2000 volts, as compared to bipolar parts, by simply expansion 10-fold of 200 volts, the upper limit for traditional Si power MOSFETs.

1.2.2 SiC Bipolar Junction Transistor (BJT)

Conductivity modulation resulted from minority carrier injection in bipolar devices is widely used to reduce the on-state resistance of thick drift layer in high power Si devices, such as power bipolar junction transistors (BJTs), insulated gate bipolar transistors (IGBTs), and P-i-N power diodes, etc. Due to the 10 times higher electrical critical field of SiC, thinner base width is achievable and enables the higher current gain for the SiC power BJT as compared to the Si counterpart. Furthermore, the much higher critical second breakdown current density, defined by

$$J_{C,crit} = qnv_s = \frac{v_s \epsilon_s E_c^2}{2BV}, \quad (\text{Eq. 1.2})$$

makes the SiC power BJT almost free of second breakdown problem [36]. Therefore, the power BJT, silenced in Si, regains attraction in SiC. Multiple teams have demonstrated SiC power BJTs with reduced on-resistance and improved current gain over the past few years. And commercial sampling SiC BJTs are already available from some startups [37, 38].

In 2001, Bergman et al. [39] reported a correlation between the forward voltage shift and the expansion of stacking faults coming from the basal plane dislocations (BPDs) in substrates when SiC bipolar devices operate under high current density conditions. In

2005, Cree reported the new etch-and-grow techniques to reduce the BPD density to less than 10 cm^{-2} [40] and confirmed the improved the forward voltage shift resistance by the PiN diode evaluation [41]. Although the reduced BPD density is achieved, the recent stress test for a SiC BJT without BPDs still showed the 21% current gain degradation [42]. In addition to the material growth techniques, the implantation-free 4H-SiC BJTs with double base epilayers were also fabricated and demonstrated improved forward voltage shift performance under the 24-hour, 100-A/cm^2 stress test [43].

As a normally-off device, the SiC power BJT is still a device of choice in the power switching applications since much higher current gain is achievable compared to the single-digit current gain of its Si counterpart. However, the complex and expensive base drive circuits are necessary due to its current driven character. Also the forward voltage drift problem for the BJTs built in the non-zero BPD substrates still cast reliability concern for the high current, high temperature and long term operations.

1.2.3 SiC Power MOSFET

Si power metal-oxide-semiconductor field-effect-transistor (MOSFET) dominates the high frequency power switch and power integrated circuit applications at both mid and low power levels. Thanks for the native oxide on SiC; the SiC MOSFET has attracted much attention over the past twenty years. The demonstrated devices extend the blocking voltage of MOSFET to as high as 10 kV [44] and reduce the specific on-resistance to as low as $5.7 \text{ m}\Omega\cdot\text{cm}^2$ with a blocking voltage over 1.4 kV [45] and $1.8 \text{ m}\Omega\cdot\text{cm}^2$ with a blocking voltage of 680V [46]. The SiC power MOSFET therefore is promising to extend the unipolar device into the mid and high power level applications. However, SiC

MOSFETs are still facing three major challenges. First, the MOS gate channel suffers low electron mobility because of the carrier scattering by interface and near interface charges. Second, the threshold voltage is instable for the trapping and releasing of carriers in gate oxide and interface under high gate field stress. Because of these two reasons, the resulted negative temperature coefficient of on-resistance for the SiC MOSFET becomes a serious concern for parallel operation of power MOSFETs [47]. Finally the SiC MOS gate has the intrinsically reliability problem under high temperature and high gate voltage stress which is caused by the higher field of gate oxide, and 0.5 eV smaller conduction band offset for the SiC-oxide interface as compared to Si-oxide [48, 49].

1.2.4 SiC Junction Field Effect Transistor (JFET)

As a unipolar device, the power JFET has been completely outperformed by the power MOSFET in Si. However, like the SiC power BJT, the JFET has attracted huge research efforts as well and demonstrated excellent devices in both recorded academic performance and practical applications. In contrast to the MOSFET in SiC, JFET is promising to offer high temperature, high frequency, and high power, reliable operation without suffering from the challenges facing the MOSFET. Furthermore, the much larger built-in voltage (V_{bi}) of SiC p-n junction than that of Si enables the normally-off power JFET with reasonable gate over drive capability ($V_{bi} - V_{TH}$). In addition, the extremely low diffusion coefficients of dopants in SiC enable good junction profile control created by implantation, which therefore makes the normally-off SiC JFET with submicron channels manufacturable.

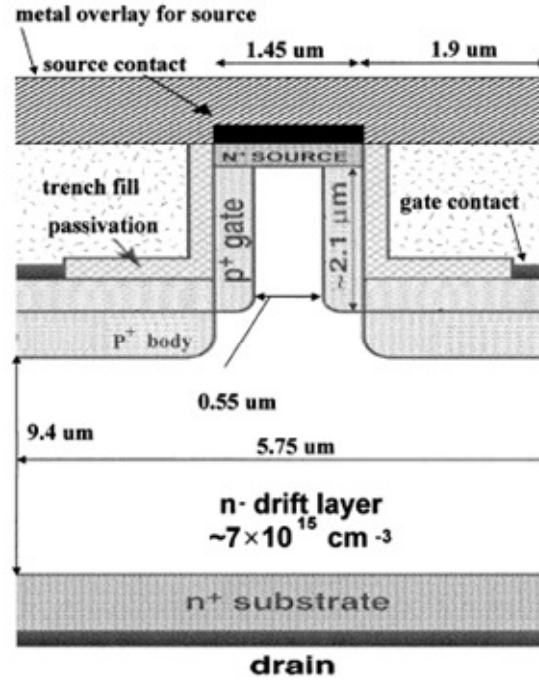


Fig. 1.2 Cross-sectional view of TIVJFET [50].

Among all proposed JFET structures, the double-gated vertical-channel structure, also known as the static induction transistor (SIT), has been implemented in the demonstration of multiple SiC power JFETs with the best performances among all SiC power transistors. Two approaches, implanted Gate and buried Gate, were proposed to develop SITs. As the first approach shown in Fig. 1.2, the trench-implanted vertical JFET (TIVJFET) has been demonstrated with a normally-off performance showing the best FOMs among the SiC power transistors with the blocking voltages ranging from 400 V to 10 kV [50, 51]. The buried Gate approach, as shown in Fig. 1.3, achieves the record low specific on-resistances of $1 \text{ m}\Omega\cdot\text{cm}^2$ for 700-V device [24] and $1.2 \text{ m}\Omega\cdot\text{cm}^2$ for 1.2-kV device [52]. However, the normally-off buried Gate SIT (BGSIT) has not been demonstrated probably due to the process difficulty of submicron channel regrowth. In contrast, the submicron

channel of TIVJFET is realized by tilted implantation without the stringent requirement of submicron facilities.

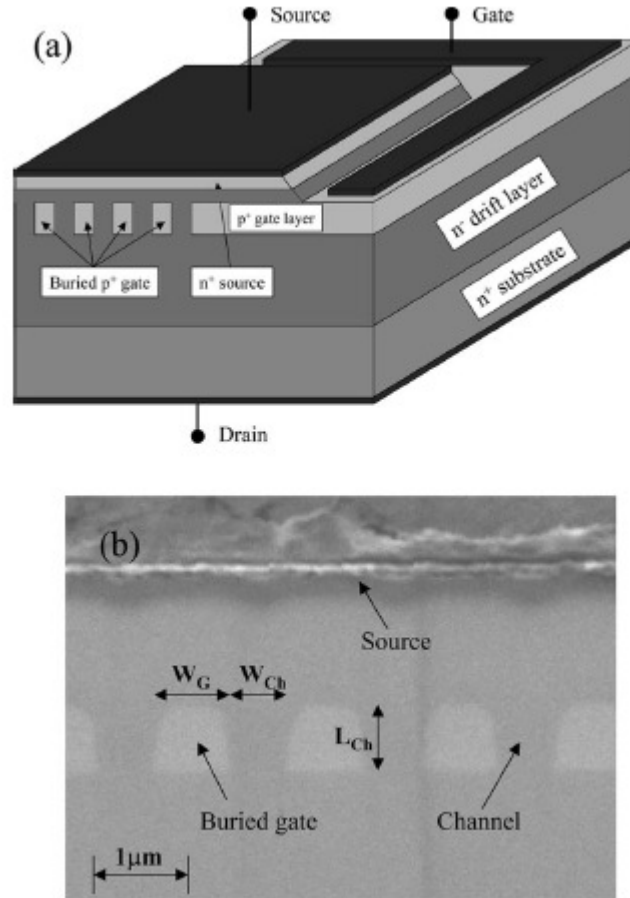


Fig. 1.3 Cross-sectional view of buried gate SIT: (a) 3D schematics; (b) SEM cross-sectional view [24].

The most recent research efforts have been focus on the high current switching applications. Veliadis, et al [53] reported 1200-V, 50-A 4H-SiC vertical JFETs (VJFETs) for power switching applications. Cheng, et al [54] concluded the reliable operation of 600-V 4H-SiC VJFETs at temperatures up to 250 °C for over thousands hours. In conclusion, SiC power JFETs are the most mature SiC power transistors with the least reliability concerns up to date.

1.3 High Temperature Electronics

Due to its wide bandgap property, SiC is promising to build high temperature electronic systems. “High temperature electronics” is defined as electronics operating at temperatures in excess of those normally encountered by conventional, silicon-based semiconductors or their auxiliary components [55]pp.2. While conventional Si devices can be used up to 200 °C and sufficiently reliable operation has been obtained for 200 °C-300 °C silicon-on-insulator (SOI) integrated circuits (ICs) [55, 56], the junction temperatures of Si power devices in the power electronic system are usually limited up to 175 °C. Since low-power SOI ICs are able to be used at temperatures up to 300 °C, it is unlikely that WBG semiconductors will find much use in low-power ICs until the ambient applications temperature exceeds 300 °C [56]. However, in the mid and high power applications, SOI technology is out of the field and SiC or GaN power devices will take the applications at ambient temperatures higher than 175 °C. Table 1.3 [56] lists some selected high temperature electronics applications in which SiC power electronics might play a key role in the near future.

Table 1.3 Semiconductor technologies for some selected high-temperature electronics applications [56].

High Temperature Electronics Application	Peak Ambient	Chip Power	Current Technology	Future Technology
Automotive				
Engine Control Electronics	150 °C	< 1 kW	BS & SOI	BS & SOI
On-cylinder & Exhaust Pipe	600 °C	< 1 kW	NA	WBG
Electric Suspension & Brakes	250 °C	> 10 kW	BS	WBG
Electric/Hybrid Vehicle PMAD	150 °C	> 10 kW	BS	WBG
Turbine Engine				
Sensors, Telemetry, Control	300 °C	< 1 kW	BS & SOI	SOI & WBG
	600 °C	< 1 kW	NA	WBG
Electric Actuation	150 °C	> 10 kW	BS & SOI	WBG
	600 °C	> 10 kW	NA	WBG
Spacecraft				
Power Management	150 °C	> 1 kW	BS & SOI	WBG
	300 °C	> 10 kW	NA	WBG
Venus & Mercury Exploration	550 °C	~ 1 kW	NA	WBG
Industrial				
High Temperature Processing	300 °C	< 1 kW	SOI	SOI
	600 °C	< 1 kW	NA	WBG
Deep-Well Drilling Telemetry				
Oil and Gas	300 °C	< 1 kW	SOI	SOI & WBG
Geothermal	600 °C	< 1 kW	NA	WBG

BS = bulk silicon, SOI = SOI, NA = not presently available, WBG = wide bandgap.

It is very challenging to develop a reliable high temperature electronic system which requires innovative device design, fabrication, electrical connections, and packaging. However, all the semiconductor components are still sharing the same device physics. The fundamental device physics in terms of temperature dependence will be revisited and summarized below, which will be used in subsequent chapters of this thesis. The intrinsic carrier density, n_i , of a semiconductor depends on temperature and its energy bandgap, as given by equation below [57] pp. 19,

$$n_i = \sqrt{N_C N_V} e^{-E_g/(2kT)} = \left(\frac{2\pi kT}{h^2} \right)^{3/2} \left(\frac{m_{dh} m_{de}}{m_0^2} \right)^{3/4} e^{-E_g/(2kT)} = AT^{3/2} e^{-E_g/(2kT)}, \quad (\text{Eq. 1.3})$$

where N_C is the effective density of states in the conduction band, N_V is the effective density of states in the valence band, h and k are Planck's and Boltzmann's constants, T is the absolute temperature, m_{de} and m_{dh} are the density-of-state electron and hole effective masses, m_0 is the free-electron mass, E_g is the bandgap, and A is a constant with a weak temperature dependence. The temperature dependence of energy bandgap, E_g , for Si [57]pp.15 and 4H-SiC [2] are given by,

$$\text{Si: } E_g = 1.17 - 4.73e^{-4} \frac{T^2}{T + 636} (\text{eV}) \quad (\text{Eq. 1.4})$$

$$\text{4H-SiC: } E_g = 3.265 - 6.5e^{-4} \frac{T^2}{T + 1300} (\text{eV}) \quad (\text{Eq. 1.5})$$

where the energy bandgap is in electron volt (eV). The p-n junction built-in potential, V_{bi} , and its derivative of temperature are defined by

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{np}{n_i^2}\right) = \frac{E_g(T)}{q} + \frac{kT}{q} \ln\left(\frac{np}{A^2 T^3}\right), \quad (\text{Eq. 1.6})$$

$$\frac{\partial V_{bi}}{\partial T} = \frac{V_{bi}}{T} - \frac{E_g}{qT} - \frac{3k}{q} + \frac{1}{q} \frac{dE_g}{dT}, \quad (\text{Eq. 1.7})$$

where n and p are the electron and hole concentration in the p-n junction, A is the one defined in equation 1. The p-n junction saturation current, J_s , is given by

$$J_s \equiv \frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n} = qA^2 T^3 \left(\frac{L_p}{\tau_p n_{n0}} + \frac{L_n}{\tau_n p_{p0}} \right) e^{-E_g/kT} \propto T^{(3+\gamma/2)} e^{-E_g/kT}, \quad (\text{Eq. 1.8})$$

where $\frac{D}{\tau} \propto T^\gamma$. As for the ideal forward biased p-n junction, the generation current can be neglected. Therefore, the junction forward current and its derivative of temperature are given by

$$J_F = J_s \left(e^{qV/kT} - 1 \right), \quad (\text{Eq. 1.9})$$

$$\frac{\partial J_F}{\partial T} = \left(\frac{3}{T} + \frac{E_g - qV}{kT^2} \right) J_F. \quad (\text{Eq. 1.10})$$

1.4 Power Integration Technology: from Si to SiC

Since the first integrated circuit (IC) chip was demonstrated in 1953, multi billion transistors have been successfully integrated on a single Si chip by the state-of-the-art 45 nm complementary metal oxide semiconductor (CMOS) technology to realize complex logic functions required by the information technology. In the mean time, the evolution of the new generation power MOSFET from early 1970's to 1980's and the invention of the insulated gate bipolar transistor (IGBT) in early 1980's [58] linked power device with integrated circuits technology [59]. The introduction of MOS technology in power electronics paved the way for power integration as the technology of power devices and integrated circuits has become compatible [59]. The power integration brings not only advantages of lower cost, but also improved reliability, reduced electromagnetic interference (EMI), and the reduction of space and weight [60, 61]. Power integration technologies are generally categorized into monolithic or hybrid types depending on the application power levels. Similarly, the first monolithic approach, with the lowest power level requirements, is the integration of lateral power or high voltage devices with low voltage analog/digital control circuits based on the bipolar-CMOS-DMOS (BCD) technology. The second monolithic approach, providing higher power capabilities, is the integration of one vertical power device with relatively simpler control and protection circuits, which is also called intelligent discrete power device [59]. The third approach is defined as the functional integration which is based on the vertical power devices, such as diodes, thyristors, and MOS devices, *et al.* to realize application specific functions like protection and current or voltage bidirectional functions [59]. The first and second

monolithic approaches are also called the smart power technologies [59]. Fig. 1.4 illustrates the application areas of the different integration modes in Si.

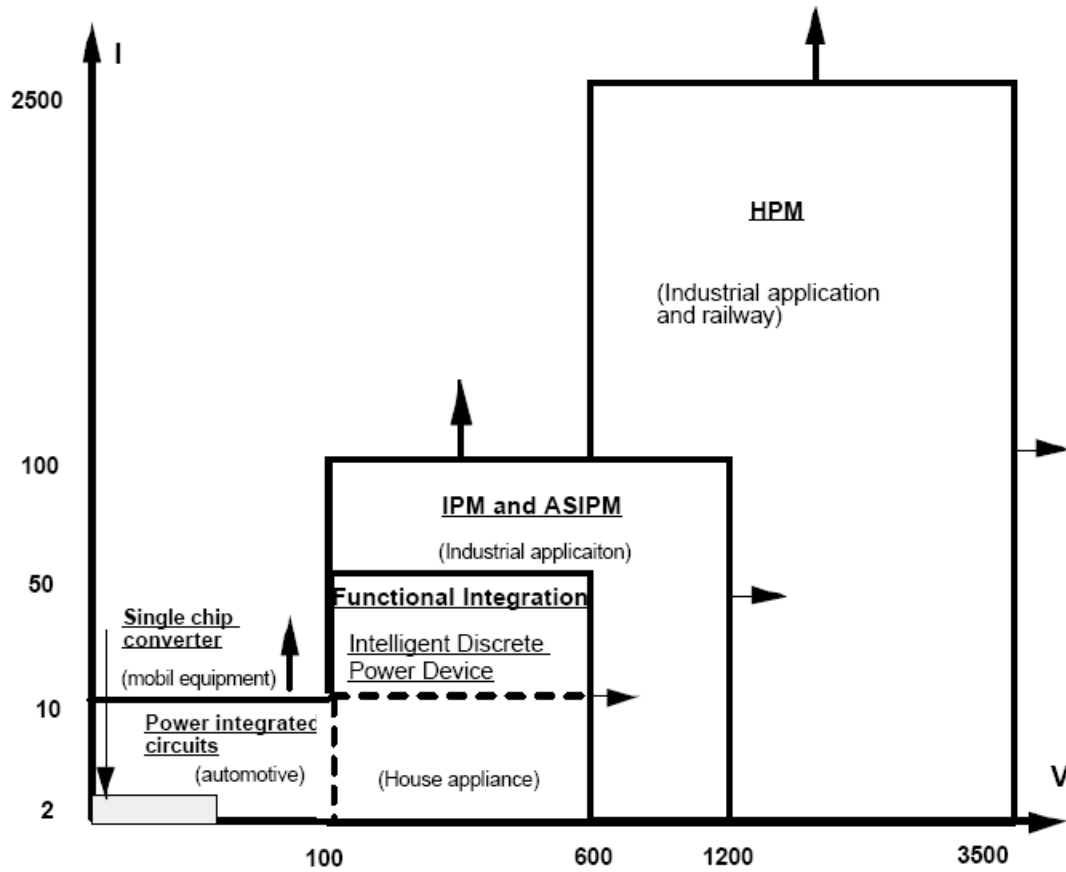


Fig. 1.4 Application areas of different integration modes in Si [59].

The monolithic power integration based on the Si BCD technology has been widely implemented to realize the system-on-a-chip (SOC) and all kinds of smart power IC chips, in which both the signal processing part (analog and/or digital), and the power delivery and conversion part are integrated on a single Si chip. One of the latest technology nodes is called BCD9 from NXP Semiconductors offering V_{BR} of 100 V, $R_{ON,SP}$ of $3 \text{ m}\Omega \cdot \text{cm}^2$, and the logic gate density of 10^7 cm^{-2} , which is only two or three generations behind the most advanced CMOS technology [62]. As shown in Fig. 1.4, the lateral power device is not so efficient as the vertical one once the application voltage

goes above 100 V, and therefore the intelligent power switch and/or the hybrid integration take the place in the applications. In these applications, the BCD technology is still used to build the high voltage integrated circuits (HVIC) for the gate drive, protection, and sensing functions, which can be co-packaged with power IGBT or super-junction DMOS [63]. It is expected that the application boundaries of different integration modes will be expanded, blurred or even disappeared with the evolution of novel technologies not only in Si.

The benefits of SiC power switches have been well known for very long time in the high power applications [64]. As stated in section 1.1, SiC power switches are able to operate at higher frequency and power rating compared to the Si counterpart. The reduced specific-on resistance and the drift layer thickness or length enable faster switching of SiC power switches driven by similar drivers. When introducing SiC in the power integration technology, either the voltage rating at the similar switching frequency or the switching frequency at the same voltage rating, or even both voltage and frequency, could be boosted roughly one order of magnitude. The application boundaries in Fig. 1.1 and 1.4 definitely need to be redefined for SiC power electronics. With the elevation of voltage, frequency, or power level, in the power electronic applications, the EMI is also exacerbated and therefore the power integration is needed to restrain EMI and protect the control and driving signal integrity by reducing the parasitic components. Similar as the Si power integration, either SiC hybrid or monolithic integration could be practical targeting different power levels while monolithic integration is necessary at higher frequencies. In addition, a SiC temperature sensing diode can be integrated on the chip to provide overheating protection for the power switches. Most importantly, the SiC power

IC chip can be implemented in a harsh environment, usually with a high temperature or radiation, while without compromise of using Si drivers. Finally, the added value of integration of a driving circuitry with SiC power devices would help SiC penetrating the Si applications, in which significant space and weight saving of inductors and capacitors in high frequency DC-DC converters and switching mode power supplies could be realized by using SiC devices.

1.5 Current Status of SiC Lateral Power Transistors and Low Voltage ICs

In order to develop a power IC chip, a lateral power device platform needs to be addressed, in which the source, gate and drain electrodes are sitting on the top surface requiring more challenging device termination, isolation and layout technologies to ensure successful integration of both high voltage (HV) and low voltage (LV) devices. Although significant progress has been achieved on SiC vertical power JFETs [50] and MOSFETs [45], progress on lateral power devices is relatively limited. In recent years, an increasing amount of research interest is being focused on this promising field. Multiple lateral MOSFETs with reduced surface electric field (RESURF) structures have been demonstrated covering the voltage range from 460 V to 2700 V [65-72]. A lateral MOSFET with a “two-zone” double RESURF structure was reported to have $V_B = 1550$ V, $R_{ON_SP} = 54 \text{ m}\Omega\cdot\text{cm}^2$ and the corresponding V_{BR}^2 / R_{ON_SP} figure-of-merit (FOM) is $44 \text{ MW}/\text{cm}^2$ [72]. However, challenges similar to those of the vertical MOSFETs, such as large channel resistance and poor gate oxide reliability, are also found in the lateral MOSFETs. On the contrary, lateral SiC power JFETs promise to offer smaller channel resistance and more reliable operation under high temperature. A 600V normally-OFF lateral JFET with the on-state resistance of $160 \text{ m}\Omega\cdot\text{cm}^2$ in 4H-SiC was reported in 2004 [73]. Subsequently, a normally-on device with better performance was reported with blocking voltage pushed up to 794 V and R_{SP_ON} lowered to $50 \text{ m}\Omega\cdot\text{cm}^2$ [74]. A theoretical study of the normally-off vertical channel lateral JFET is reported in 2005 [75], as shown in Fig. 1.5. The simulated normally-off device with optimized RESURF and channel structures has the potential of blocking 1535 V with a specific on-resistance of $3.24 \text{ m}\Omega\cdot\text{cm}^2$, resulting in a theoretical figure of merit of $727 \text{ MW}/\text{cm}^2$ that is

comparable with the best experimentally demonstrated vertical power JFET [50]. This device concept founds the proposed research in this thesis and will be further detailed in the later chapters.

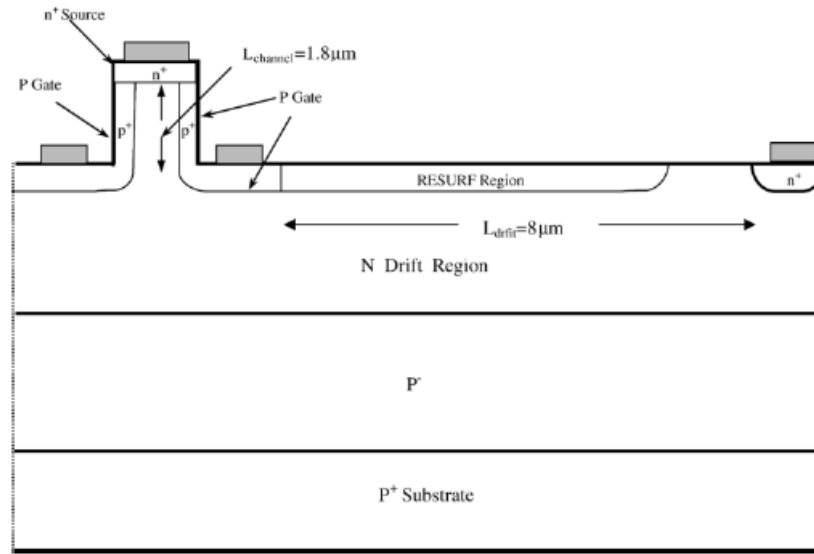


Fig. 1.5 Structure of VC-LJFET with an uniform doped RESURF region[75].

In addition to the lateral power devices, low voltage digital and analog circuits are also important to develop power IC chips. In 1994, the first monolithic digital SiC integrated circuit was demonstrated based on an NMOS technology in 6H-SiC [76]. And in 1996 and 1997 two teams reported CMOS based operational amplifier [77] and digital integrated circuits [78, 79] respectively in 6H-SiC. In 2006, a 4H-SiC based CMOS inverter was first demonstrated which was fabricated in the process flow of a 4H-SiC power DMOS [80]. As for the SiC JFET technology, 600°C operation capability [81] and radiation hardness [82] of 6H-SiC JFETs were reported in 1994 and 1992 respectively. More recently, 3000-hour stable operation of a differential amplifier at a temperature as high as 500 °C has been demonstrated based on a low voltage lateral JFET technology in 6H-SiC [83].

In summary, SiC lateral power devices and integrated circuits have been demonstrated separately, however monolithic integration of HV and LV devices on a single chip is not demonstrated yet.

1.6 Objectives of the Thesis Research

The objective of the research is to develop a monolithic 4H-SiC power IC chip based on the conjectured structure, vertical-channel lateral JFET (VC-LJFET), in 2005 [75]. By the experimentally demonstration and characterizations of the 4H-SiC lateral JFETs and power integrated circuits, the research would lead to a novel SiC power integration technology for high temperature, high frequency, and high voltage applications, which cannot be met by Si electronics. In order to demonstrate the JFET based 4H-SiC power IC technology, critical issues on device and circuits design, mask and layout design, robust fabrication flow, and later on understanding of device characteristics, will be addressed. Specifically, the objectives include:

- (1) Design of the chip: device, circuitry, mask and layout;
- (2) Develop a robust fabrication process flow: address of critical process issues;
- (3) Device characterizations: temperature dependence of both low voltage and high voltage JFET characterizations;
- (4) IC chip switching test;
- (5) RESURF experimentally optimization;
- (6) Metallization spreading resistance modeling;
- (7) Temperature sensing diode technology for chip junction temperature monitoring;
- (8) Demonstrate operation of 600 V, 4A at $V_F = 4V$, at room temperature, and the stable operation at 250 °C is required;
- (9) MHz switching results with integrated driving circuits need to be demonstrated to show functionality of the power IC chip.

2. DESIGN

2.1 Device Concept and Technology Overview

It is critical to design a process compatible technology for the integration of both power and low voltage devices. Based on the TIVJFET process flow, the fabrication-compatible device structure, VC-LJFET, for both HV and LV devices were proposed and the simulation study on the HV VC-LJFET [75] predicted its excellent performance. Therefore, a 4H-SiC JFET based power integration technology platform is proposed and illustrated in Fig. 2.1. The VC-LJFET based technology provides integration of high voltage (HV) and low voltage (LV) lateral JFETs, N-type SiC resistors, and implanted trench isolations. The technology also features vertical channels with double gates for each channel, and a double **reduced surface electric field** (RESURF) structure for high voltage devices. Compared to the planar single gate JFET, the VC-LJFET offers higher transconductance, hence better current handling capability for the low voltage devices. The double-gate structure also relieves the difficulty to make normally-off high voltage JFETs that is desirable in power electronic circuits for the fail-safe purpose. The double-RESURF effect helps flatten the electric field in the drift region along the lateral direction and hence improve the device blocking voltage for the same drift length. In other words, doping concentration of the drift region can be substantially increased with the drift region length reduced for a given blocking voltage. It is also known that RESURF-based devices possess similar advantages as a super-junction structure for having a much lower output capacitance (C_{oss}) than a traditional device structure. The lower R_{ON} and C_{oss}

resulting from the RESURF effect yield a better figure of merit $R_{ON} \cdot C_{OSS}$, which is important in resonant switching [84, 85].

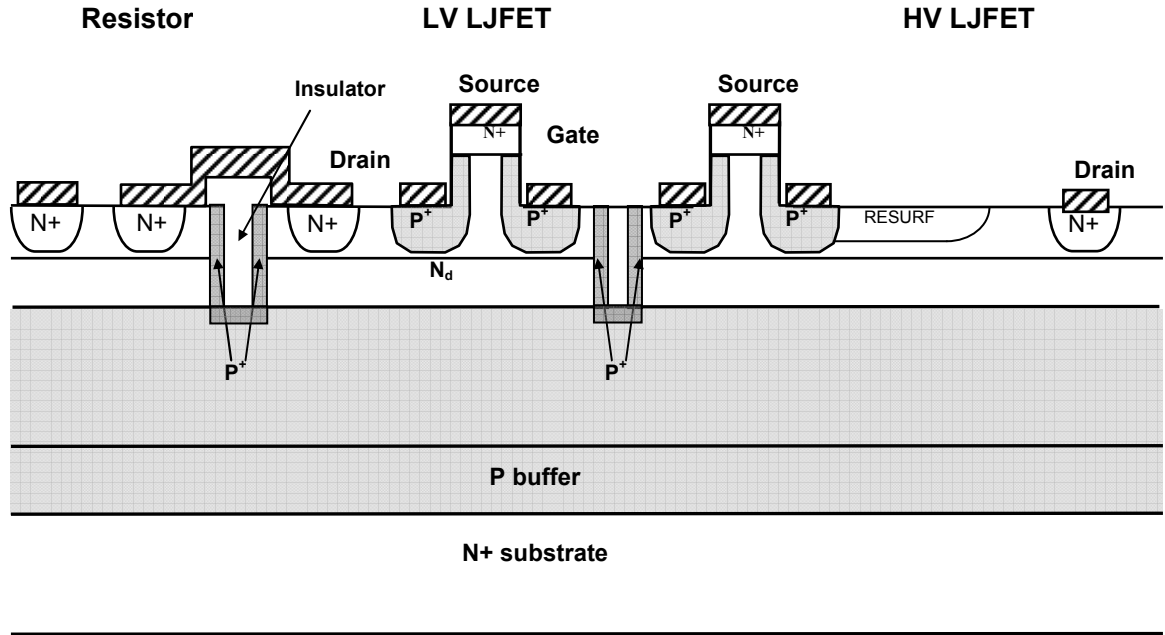


Fig. 2.1 Schematic structure of the VC-LJFET technology platform: integration of HV and LV JFETs, N-type SiC resistors, and implanted trench isolations.

The vertical channel formed by tilted implantations on mesa sidewalls enables the submicron channel control for the normally-off JFET [50]. The mesa structure offers multiple self-aligned process steps without the need of photo masks, as well as the photo resist (PR) etch back planarization process [50]. In this technology, HV JFET and low-voltage buffers can be easily integrated due to their structural similarity. And comparing with the planar JFET technology, the vertical channel design provides a feasible approach to realize both the normally-off JFET operation and a better current handling capability. In addition, the technology can be scaled down to further reduce the channel resistance

for the HV JFETs, integrate more compact logic gates, and provide higher performance analog circuits. The scaling down of the VC-LJFET to a level that requires deep submicron technology will be discussed briefly in Chapter 6.

2.2 Design of the Normally-Off Vertical Channel Lateral JFET (VC-LJFET)

2.2.1 HV VC-LJFET Unit Cell Design

The high voltage device unit cell is shown in Fig. 2.2. The mesa pitch size is fixed at $3.7\ \mu\text{m}$ and the etched mesa height is $4\ \mu\text{m}$. The drift region is defined by the gate and drain implantation, and its actual drift length (L_{drift}) is between 7 and $9\ \mu\text{m}$ depending on the misalignment and different implantation masking materials. The channel layer is nitrogen doped to $5 \times 10^{16}\ \text{cm}^{-3}$ with a vertical channel length of $1.8\ \mu\text{m}$. The p^+ gate of the lateral side is implanted to be $0.5\ \mu\text{m}$ thick with an Al concentration of $1 \times 10^{19}\ \text{cm}^{-3}$. The p^+ sidewall gate has an Al concentration of $1 \times 10^{18}\ \text{cm}^{-3}$ and a depth of $0.35\ \mu\text{m}$ that leaves the channel width (W_{ch}) $0.4\ \mu\text{m}$. The n-type drift layer for voltage blocking constitutes the major part of the on-resistance and is doped to $1 \times 10^{17}\ \text{cm}^{-3}$ with a thickness of $1\ \mu\text{m}$. Although the best simulation results are achieved with a $4\ \mu\text{m}$ thick, $3 \times 10^{16}\ \text{cm}^{-3}$ doped drift layer [75], the $1\ \mu\text{m}$ thick design is however selected to make sure the isolation trench reaches the bottom p RESURF. The two p-type layers below the drift layer are designed to serve as the bottom RESURF structure to support the vertical voltage drop. All the epilayers are grown on the n-type 4H-SiC substrate for better wafer quality.

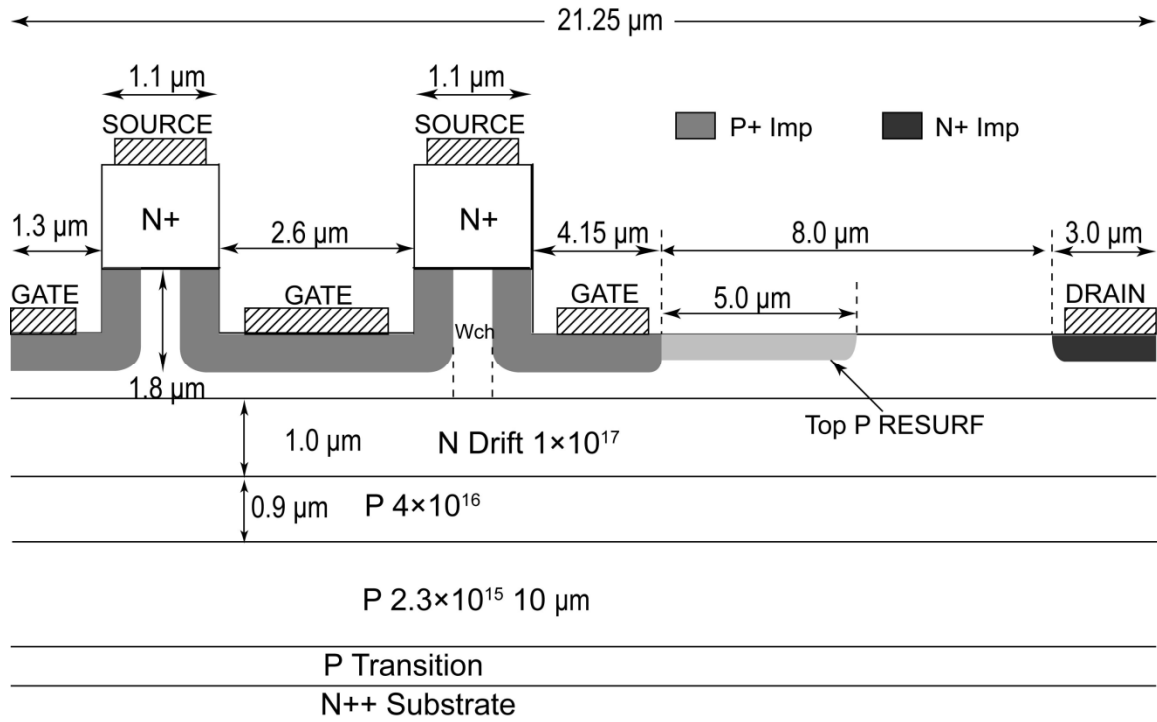


Fig. 2.2 The cross-sectional view of HV VC-LJFET unit cell.

2.2.2 RESURF Design

The RESURF structure was developed in early 1970s [86] and is widely applied in Si power IC technologies [62]. The RESURF effect helps flatten the electric field along the lateral direction and hence improve the device blocking voltage for the same drift length. In other words, doping concentration of the drift region can be substantially increased with the drift region length reduced for a given blocking voltage. It is also known that RESURF-based devices possess similar advantages as a super-junction structure for having a much lower output capacitance (C_{oss}) than a normal device. However, super-junction SiC devices have not yet been demonstrated because of processing difficulties. Therefore, RESURF structures are an especially attractive choice for lateral power devices in SiC.

The utilization of RESURF effect requires that the n-type drift layer be completely depleted before the lateral junction breaks down. The vertical depletion of the n drift layer places a dose limitation of the drift layer by

$$Q_{drift} = n_{drift} \cdot t_{drift} \leq \frac{\epsilon_s E_C}{q} = Q_M, \quad (\text{Eq. 2.1})$$

where q is the single electron charge, ϵ_s is the permittivity of the semiconductor, E_C is the critical breakdown field, Q_M is the maximum dose of the semiconductor material, n_{drift} is the drift layer doping, and t_{drift} is the drift layer thickness. Q_M of 4H-SiC is calculated to be $1.61 \times 10^{13} \text{ cm}^{-2}$ which is 8 times as high as that of Si ($1.94 \times 10^{12} \text{ cm}^{-2}$). Furthermore, by considering both vertical and lateral directions, the optimal drift layer dose ($Q_{drift} = n_{drift} \cdot t_{drift}$) for a single-RESURF structure is estimated by [30]

$$Q_{drift} = n_{drift} \cdot t_{drift} \leq \frac{\epsilon_s E_C}{q} \sqrt{\frac{p_{sub}}{n_{drift} + p_{sub}}} = Q_M \sqrt{\frac{p_{sub}}{n_{drift} + p_{sub}}} < Q_M (n_{drift} > 0), \quad (\text{Eq. 2.2})$$

where p_{sub} is doping of bottom RESURF, usually the substrate doping.

The specific on-resistance of the drift layer calculated by equation 3

$$R_{ON,SP} = R_{ON} A_{drift} = \frac{1}{q \mu_n n_{drift}} \frac{L_{drift}}{t_{drift} W} \cdot (L_{drift} W) = \frac{L_{drift}^2}{q \mu_n Q_{drift}} = R_{sh} \cdot L_{drift}^2, \quad (\text{Eq. 2.3})$$

shows that higher Q_{drift} leads to lower $R_{ON,SP}$ of the drift region, where A_{drift} is the drift region area, μ_n is the electron mobility, L_{drift} is the drift length, R_{sh} is the sheet resistance of the n-type drift layer, and W is the device unit cell width. For a fixed Q_{drift} , higher n doping yields higher on-resistance because of the degradation of electron mobility. Compared to the single-RESURF structure, double-RESURF structure yields a Q_{drift} twice as high, leading to a lower on-resistance [75, 87]. The doping concentration and thickness of the epilayers are fixed parameters as we start the device fabrication. As for

the 1 μm thick drift layer [75], the optimal Q_{drift} is around $1.3 \times 10^{13} \text{ cm}^{-2}$ corresponding to the doping level of $1.3 \times 10^{17} \text{ cm}^{-3}$, and the optimal top p-RESURF dose (Q_{top}) is around $0.95 \times 10^{13} \text{ cm}^{-2}$ corresponding to the p-doping level of $1.9 \times 10^{17} \text{ cm}^{-3}$ (p depth is 0.5 μm). Both optimal doses are obtained by device simulation. For a shallower p-RESURF implantation with less surface damages, a doping concentration between $3 \times 10^{17} \text{ cm}^{-3}$ (p depth of 0.3 μm) and $4.8 \times 10^{17} \text{ cm}^{-3}$ (p depth of 0.2 μm) can be used as the optimum. However, the implantation concentration is finally designed at $6.5 \times 10^{17} \text{ cm}^{-3}$ by considering the incomplete activation of aluminum (Al) ions in 4H-SiC during post-implantation annealing at 1550 $^{\circ}\text{C}$. A series device simulations were carried out to find the optimal RESURF length (L_r) by setting p-RESURF concentration of $6.5 \times 10^{17} \text{ cm}^{-3}$ and depth of 0.2 μm , and $L_{drift} = 7.5 \mu\text{m}$. Fig. 3 shows the impact ionization generation rate (IIGR) distributions at the breakdown voltages for different RESURF lengths. With the extension of top RESURF region, the breakdown point moves from the junction of p+ Gate and n drift to that of n drift and bottom RESURF. It can be seen that when L_r equals to 5 μm , the breakdown reaches a peak of 1056 V. The simulated breakdown voltages at different L_r are also plotted in Fig. 2.4.

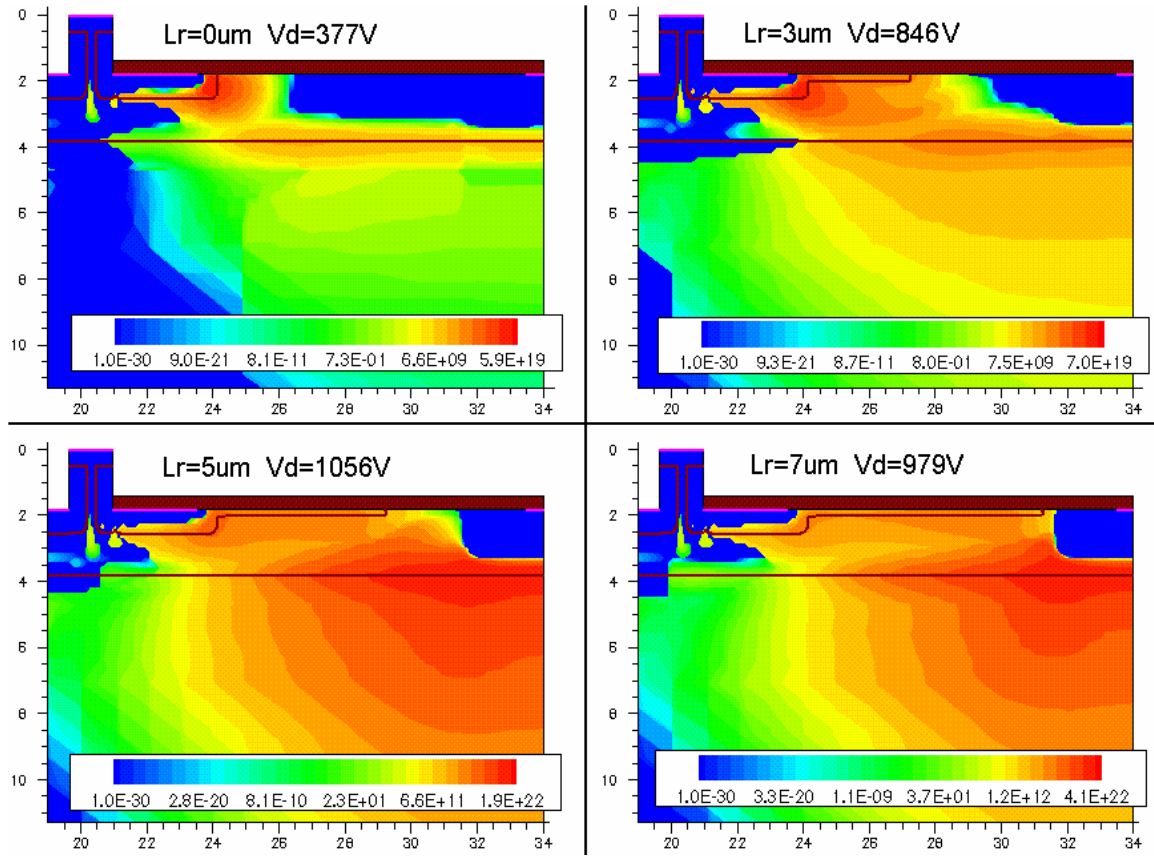


Fig. 2.3 The impact ionization generation rate (cm⁻³s⁻¹) distributions at breakdown voltages.

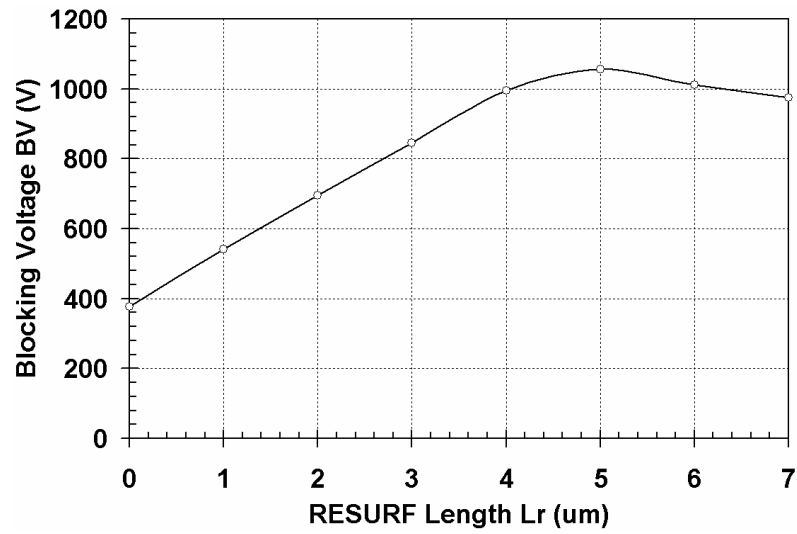
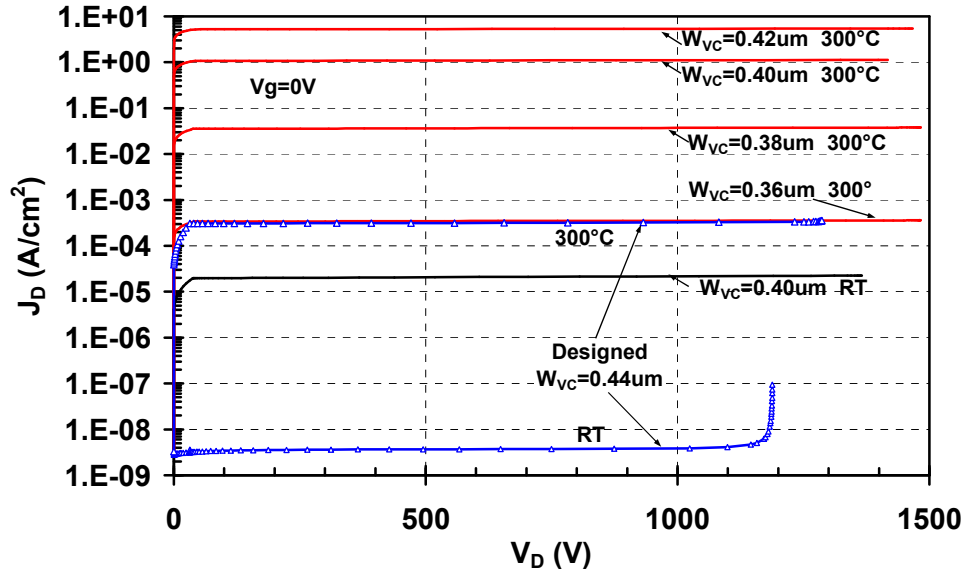


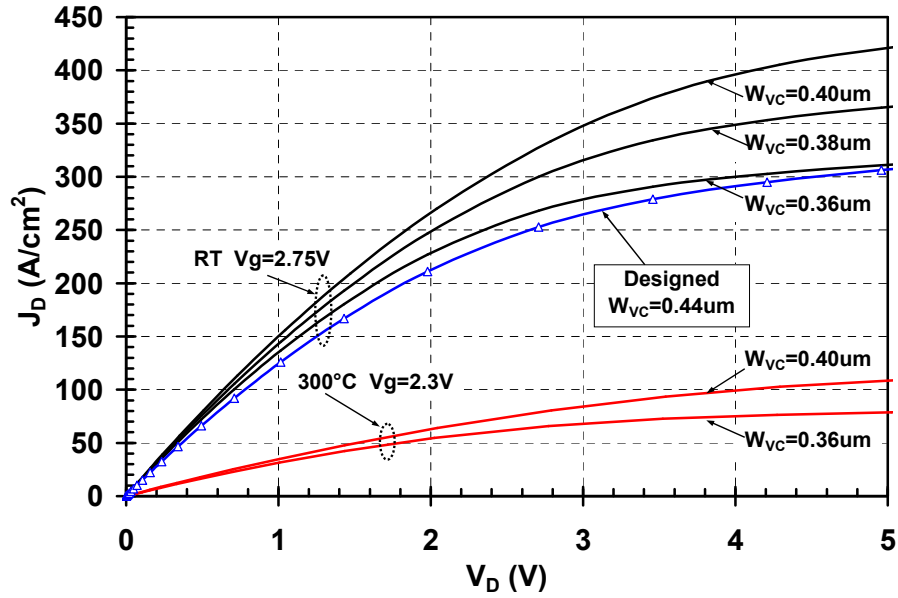
Fig. 2.4 Breakdown voltages at different top RESURF lengths.

2.2.3 Vertical Channel Design

Similar as the TIVJFET, the vertical channel of the VC-LJFET determines threshold voltage, channel on-resistance, and even the blocking performance. Multiple simulations are performed to fine-tune the submicron channel width. The original n-type channel doping was designed to be $3 \times 10^{16} \text{ cm}^{-3}$; however, the ended channel doping of the epilayer is $5 \times 10^{16} \text{ cm}^{-3}$ which further tightens the optimal channel width. As shown in Fig. 2.5, breakdown simulation results for the doping level of $5 \times 10^{16} \text{ cm}^{-3}$ show that $0.4 \text{ }\mu\text{m}$ is the upper boundary of the channel width for the room temperature (RT) normally-off operation, while this number goes down to $0.36 \text{ }\mu\text{m}$ for $300 \text{ }^{\circ}\text{C}$. Note that the device with a channel width of $0.44 \text{ }\mu\text{m}$ is still normally-off at $300 \text{ }^{\circ}\text{C}$ for the channel doping of $3 \times 10^{16} \text{ cm}^{-3}$, as shown by the blue lines in Fig. 2.5(a). The corresponded forward I-V curves are shown in Fig. 2.5(b). The specific on-resistances of the HV VC-LJFET ($L_{\text{drift}} = 9 \text{ }\mu\text{m}$) at room temperature are $7.4 \text{ m}\Omega\cdot\text{cm}^{-2}$ for $W_{\text{ch}} = 0.36 \text{ }\mu\text{m}$ and $6.7 \text{ m}\Omega\cdot\text{cm}^{-2}$ for $W_{\text{ch}} = 0.40 \text{ }\mu\text{m}$, for $V_{\text{DS}} = 1 \text{ V}$ and $V_{\text{GS}} = 2.75 \text{ V}$. In order to obtain the proper channel width, three types of small test HV VC-LJFETs are designed with different mesa widths at mask level, i.e. standard size and the sizes with $\pm 0.15 \text{ }\mu\text{m}$ deviations.



(a) The simulated blocking I-V curves



(b) The simulated forward I-V curves

Fig. 2.5 The TCAD simulation results for the VC-LJFETs with different channel width: $L_{drift} = 9 \mu\text{m}$, the designed channel doping is $3 \times 10^{16} \text{ cm}^{-3}$ while the actual channel doping is $5 \times 10^{16} \text{ cm}^{-3}$.

2.2.4 LV VC-LJFET Design

The unit cell of the low voltage (LV) VC-LJFET is very similar to the HV JFET, as shown in Fig. 2.2, except that the L_{drift} is reduced to 2 μm and the top RESURF is removed. The unit cell length is 6 μm shorter than the HV VC-LJFET. Multiple simulations for different channel widths show the same results as HV JFETs that 0.4 μm and 0.36 μm are the upper limits of the channel width for the normally-off operation at RT and 300 $^{\circ}\text{C}$ respectively. The $R_{DS,ON}$ of LV JFETs is also a key parameter for the buffer design, which will be discussed on the following section. Fig. 2.6 shows the specific $R_{DS,ON}$ versus different channel widths at both RT and 300 $^{\circ}\text{C}$.

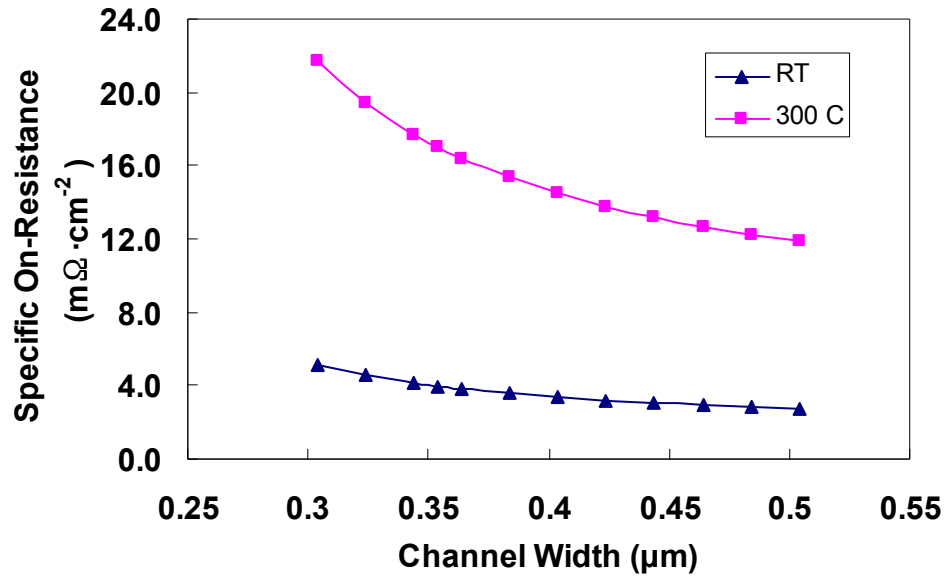


Fig. 2.6 The simulated specific $R_{DS,ON}$ of LV VC-LJFET as a function of channel widths.

2.3 Design of the Gate Drive Buffer and Power Integrated Circuits

The purpose of a power integration technology is to create smart power IC (SPIC) chips that may eventually lead to a system-on-a-chip (SOC) with higher performance and lower cost. A smart power IC can include power devices, gate drive and control circuits, and the circuits with load monitoring, diagnostic and self-protection functions [79]. Among them, the gate drive buffer, along with the power devices, is the core of a PIC. With the interface of a gate buffer, small signals can be used to switch the power devices effectively with the proper DC biases. The widely used buffer stages in operational amplifiers or power amplifiers are typically based on complementary device pairs, specifically, either as NPN and PNP bipolar transistor pairs or N-channel and P-channel MOS transistor pairs. In the VC-LJFET technology proposed, however, only n-type JFETs and resistors are available for the buffer design. Based on the resistive-load NJFET inverter, a four-stage super buffer is designed to drive the integrated power JFET, as shown in Fig. 2.7.

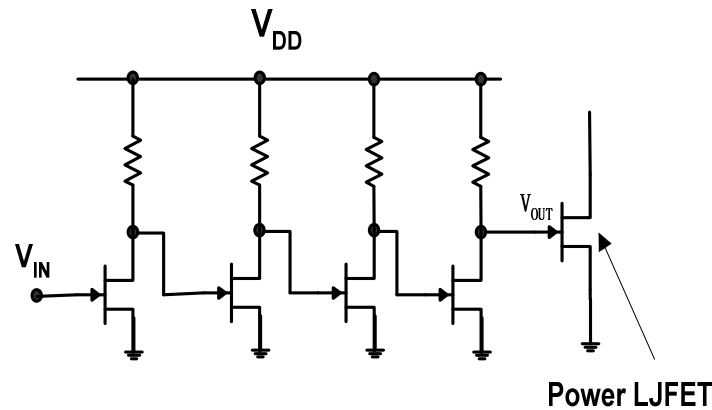


Fig. 2.7 The SiC power integrated circuit comprising a high-voltage power LJFET and its driving buffer circuitry

For each stage of the resistive-load inverter, the minimum HIGH output voltage (V_{OH}) is equal to the DC power supply voltage (V_{DD}), but the maximum LOW output voltage (V_{OL}) is always larger than zero and can be formulated as $R_{ON}/(R_L+R_{ON})\cdot V_{DD}$, where R_L is the load resistance and R_{ON} is the on-resistance of the JFET. To ensure proper buffer functionality, V_{OL} of previous stage needs to be less than threshold voltage (V_{TH}) of the JFET. This requires R_{ON}/R_L to be as small as possible. However, with a given device area constraint, a smaller R_{ON} , requires V_{TH} to be reduced, making the $V_{OL}<V_{TH}$ condition harder to satisfy. As a result, threshold voltage of the JFET needs to be controlled within a certain range to ensure the appropriate cascading of multiple inverter stages. To obtain a good balance between the propagation delay and the overall circuit size, an area ratio of 5 is selected between neighboring inverter stages.

Test structures and circuits have also been designed and incorporated for for evaluation of various processing steps. Table 2.1 summarizes some of the designed devices and test structures.

Table 2.1 Summary of VC-LJFETS and some test structures.

VC-LJFET	Active Area (cm ²)	Comments
HVJFET (Large)	1.59×10^{-2}	Large power device targeting 4A current handling capability at RT
HVJFET (Medium)	4.01×10^{-3}	Medium power device targeting 1A current handling capability at RT
HV Lateral Diode	420 μm of p+ peripheral	For blocking voltage testing

HVJFET L mesa (+0.15 μm)	1.53×10^{-4}	HV JFET with wider channel, actual layer out as large HV JFETs
HVJFET M mesa (0.0 μm)	1.53×10^{-4}	HV JFET with nominal channel, actual layer out as large HV JFETs
HVJFET S mesa (-0.15 μm)	1.53×10^{-4}	HV JFET with narrower channel, actual layer out as large HV JFETs
LVJFET T1	1.60×10^{-5}	For low voltage device modeling
LVJFET T2	1.63×10^{-4}	For low voltage device modeling
Resistor RT1, RT2		Form a logic inverter combined with LVJFET T1, T2

2.4 Layout and Mask Design

In order to achieve a practical current capability, a large power device with a footprint about $2\text{mm} \times 1.5\text{mm}$ and an active area of $1.59 \times 10^{-2} \text{ cm}^2$ is designed, as illustrated in Fig. 2.8. To reduce the spreading resistance of the metal overlay, mesa groups are limited to around $500 \mu\text{m}$ in length. And the drain pad is split into four separate ones sitting along a middle line which divides the large device into two symmetry halves. Two identical buffer circuits are designed to drive the upper and down side of the large power device. Two types of chip blocks, A and B, both include a large power JFET, two buffer circuits, and other testing devices. Block B contains identical devices except the buffer output is not electrically connected to the Gate pads of the power device. Besides, a medium size power JFET which is $\frac{1}{4}$ of the large one is also designed with a single but larger Drain bonding pad, as shown in Fig. 2.9. Only one buffer is needed to drive the medium JFET. Similarly, two blocks, C and D, are designed to hold the power JFET, buffer, and testing devices. Block D differs C from the disconnection between output of buffer and Gate of power JFET. Block E only includes test devices serving as the process monitor. Please refer to Table 2.2 for the block size summary.

TABLE 2.1 Block size summary for the designed power IC chips.

	Block A	Block B	Block C	Block D	Block E
Width (μm)	2350	2385	1480	1500	1030
Length (μm)	2040	2040	1400	1400	950

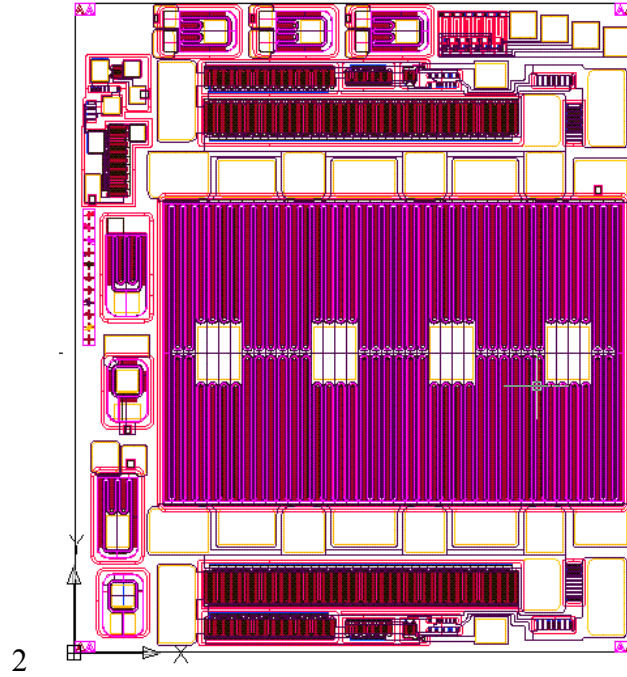


Fig. 2.8 The footprint layouts of SiC power IC chips: Block A, $2.04\text{mm} \times 2.35\text{ mm}$.

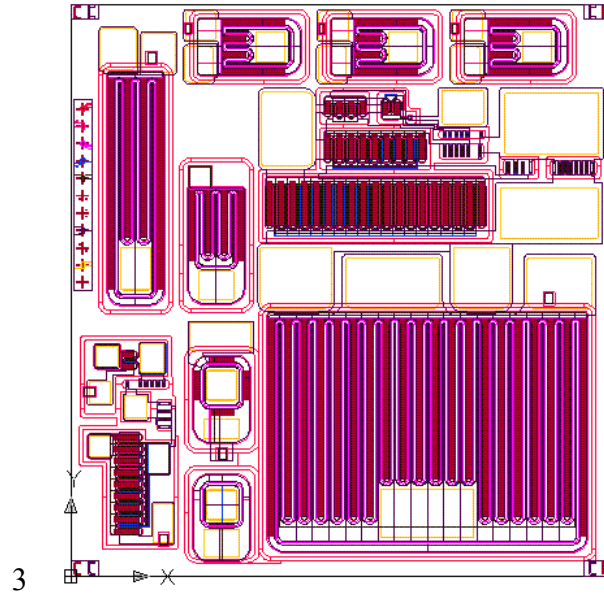


Fig. 2.9 The footprint layouts of SiC power IC chips: Block C, $1.4\text{ mm} \times 1.48\text{ mm}$.

Fig. 2.10 shows the device unit cell details of different mask layers. It is noted that the sharp end of Drain region is carefully designed by reducing the RESURF length from $4.5\text{ }\mu\text{m}$ to $2.5\text{ }\mu\text{m}$ since the electrical field peak at the turning edge of p+ Gate is relieved

by the geometry and then less RESURF charge is needed. Table 2.3 summarizes the masks for the technology platform.

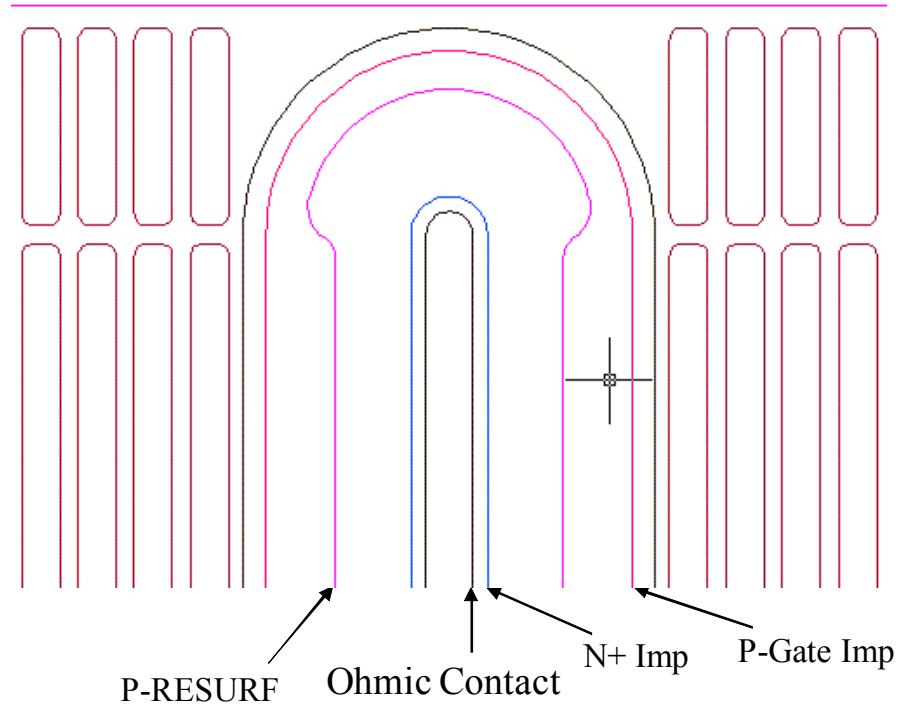


Fig. 2.10 Device unit cell details of different mask layers

TABLE 2.3 Mask summary for the power IC development.

Number	Layers	Description	Mask Tone	Alignment Requirement
Mask #1	Mesa Etching	2.5 μm of PR line width, 1.2 μm white	black	good contact is needed
Mask #2	Isolation	for both isolation etching and implantation	white	not critical
Mask #3	Gate Implantation	for Gate sidewall and contact implantation	white	less than 1 μm misalignment
Mask #4	Drain Implantation	for Drain n++ implantation	white	less than 1 μm misalignment
Mask #5	RESURF	form HV device only	white	less than 0.5 μm

	Implantation			misalignment
Mask #6	Ohmic Contact	for ohmic contact window opening and Gate overlay patterning	white	less than 0.5 μm misalignment
Mask #7	Via	open windows for overlay contact	white	less than 1 μm misalignment
Mask #8	Overlay	connect devices to form circuits	black	less than 1 μm misalignment
Mask #9	Bonding Pad	open bonding pad window and Au lift-off	white	not critical

One group of small area HV VC-LJFETs with standard size, $+0.15\ \mu\text{m}$, and $-0.15\ \mu\text{m}$ mesas serve the purpose of both the channel width and V_{TH} control. Another HV LJFET without sharp turning corner, together with an identical-shaped diode, are also designed to monitor the blocking voltage. Two LV JFETs and two load resistors form the inverters and also serve for the device modeling and parameter analysis. Other test structures, Gate-Source shorting test structure, ring oscillator, device isolation test pattern, RESURF length optimization diodes, and TLM patterns for ohmic contact, are also designed in different blocks. Please refer to Table 2.1 for the device summary.

3. FABRICATION

3.1 Device Engineering

3.1.1 Wafer Structure

The started 4H-SiC wafer from Cree, Inc. includes seven epilayers grown on an n-type substrate, as shown in Fig. 3.1. Right above the n-type substrate, a p-type transition/field-stopping layer is grown and followed by the 10- μm , $2.3\text{e}15\text{ cm}^{-3}$ doped p-epilayer that is designed to support most of the blocking voltage in the vertical direction. A 0.9- μm , $4\text{e}16\text{ cm}^{-3}$ p doped layer is additionally grown on the p- layer. The p layers serve as the bottom RESURF structure for the high voltage VC-LJFET. On the top of p layers, an n-type, 1- μm , $1\text{e}17\text{ cm}^{-3}$ doped layer is the drift layer providing current flow and followed by another n-type, 2- μm , 5 to $5.5\text{e}16\text{ cm}^{-3}$ doped layer in which the vertical channel is formed. The 2- μm , $6\text{e}18\text{ cm}^{-3}$ n+ layer is to provide enough vertical distance for the planarization process to prevent the possible Source-Gate shorting problem. The top n++ layer is designed to be at least 0.7 μm for the Source ohmic contact; however the actual thickness is only about 0.55 μm . Fig. 3.1 shows the SIMS analysis for the actual wafer doping and thickness.

0.7 μm	N++ 1.1E19
2.0 μm	N+ 6E18
2.0 μm	N 5.5E16
1.0 μm	N 1E17
0.9 μm	P 4E16
10.0 μm	P- 2.3E15
P transition	
N+ 4H-SiC Substrate	

Fig. 3.1 (a) Schematic of the wafer structure.

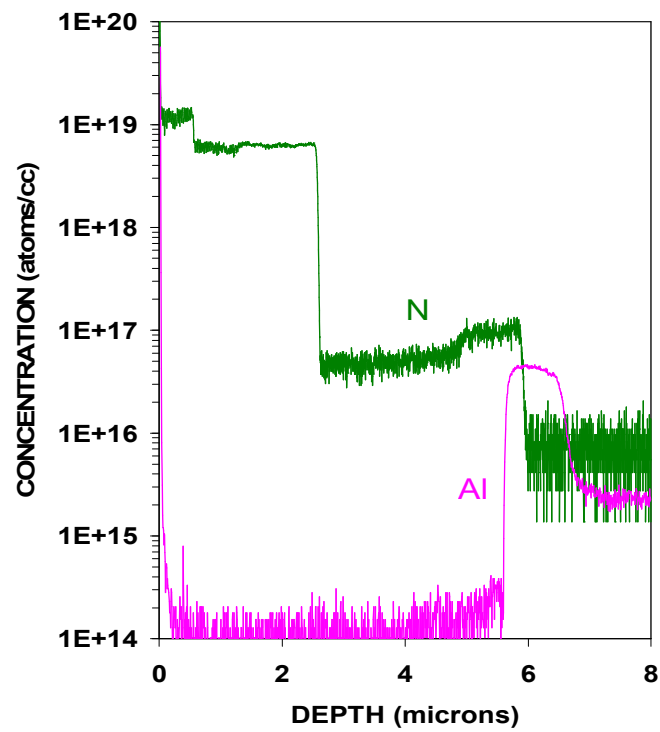


Fig. 3.1 (b) SIMS analysis for the dopants

3.1.2 Mesa Formation

To prepare a SiC dry etching mask, a 280 nm AlTi (3.5%wt of Ti) layer is sputtered and patterned by lithography and wet etching. The AlTi line width is around 1.8 μm with a reduction of 0.7 μm compared with the lithography mask line width (the 3.7 μm pitch size with a 2.5 μm line width). Then a 4- μm deep trench etching is carried out by $\text{CF}_2\text{-O}_2$ and C_4F_8 based Bosch process in an inductively-coupled plasma (ICP) etcher [8]. The etched mesa line width is further shrunk to about 1.1 to 1.2 μm . Please refer to Fig. 3.2 for the schematic and the SEM photo for the etched mesa profile.

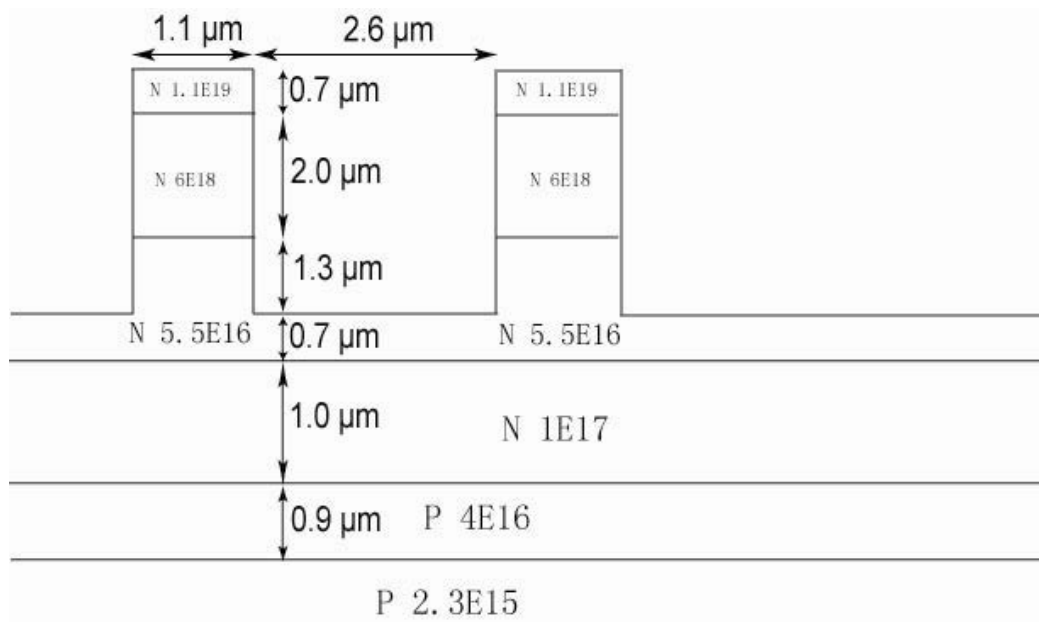


Fig. 3.2 (a) Schematic of the mesa cross section;

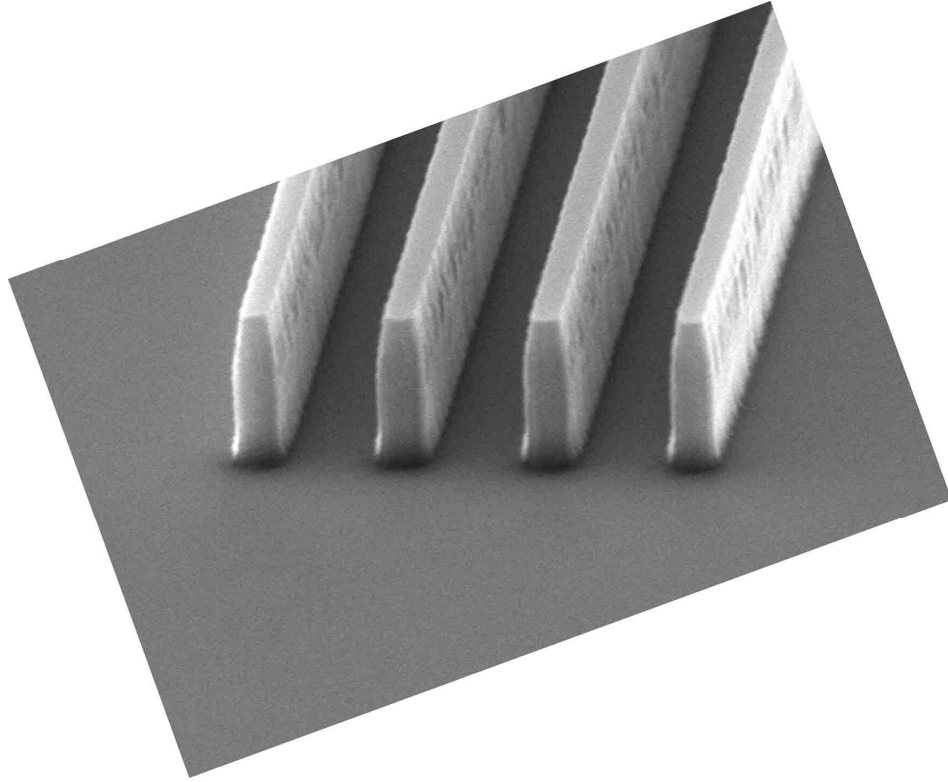


Fig. 3.2 (b) SEM photo for a group of mesas after ICP etching

3.1.3 Isolation Trench

Device isolation is created by the trench etching and the subsequent ion implantation to assure the buried p layers electrically grounded. A 700-nm thick AlTi mask is prepared by wet etching. The thicker AlTi compared with the mesa etching is to protect mesas from isolation trench etching. A regular $\text{CF}_2\text{-O}_2$ ICP etching is done to create 1.7- μm deep isolation trenches, as shown in Fig.3.3.

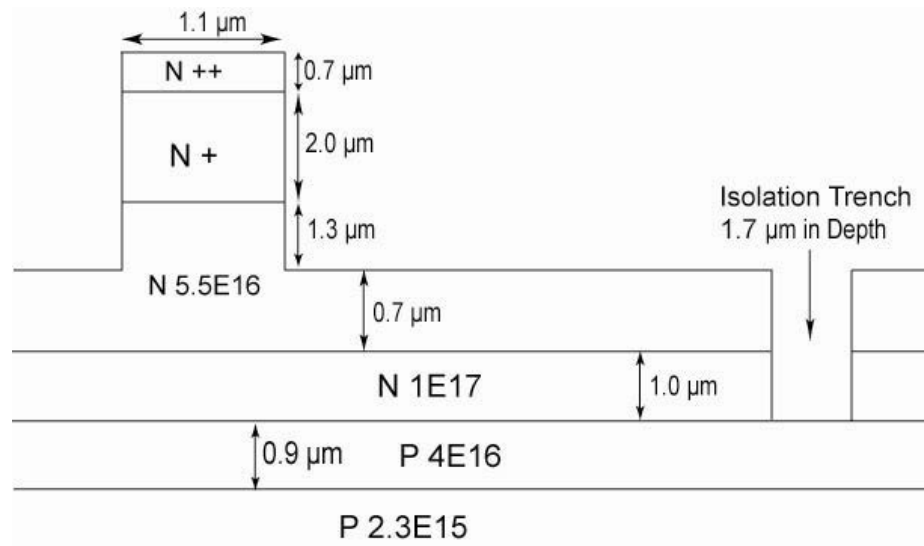


Fig. 3.3 (a) Schematic of the isolation trench

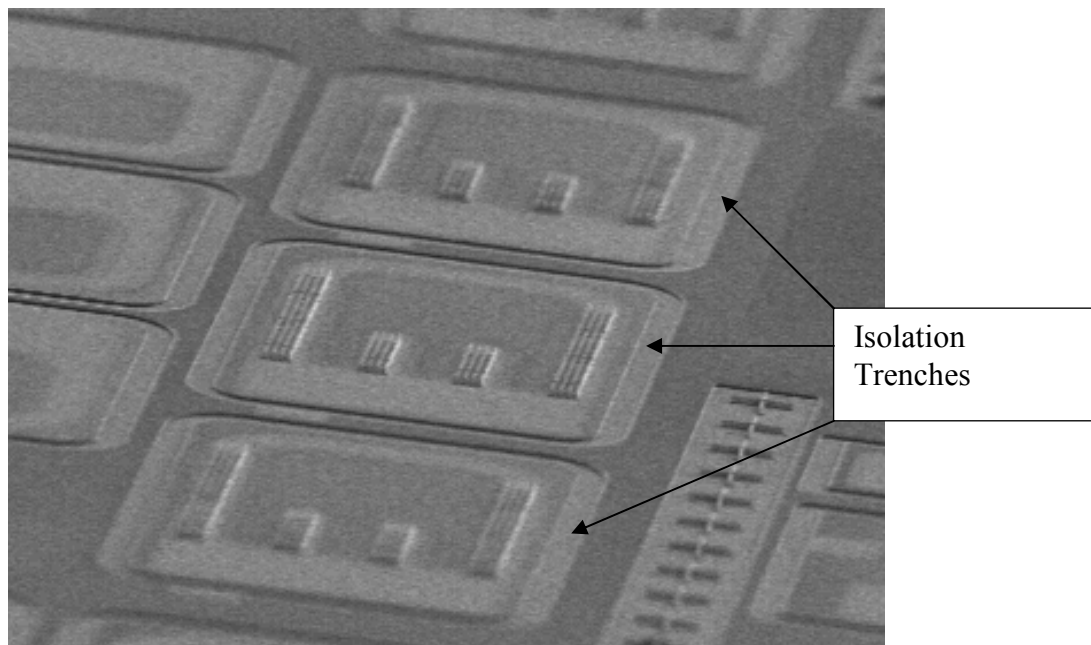


Fig. 3.3 (b) SEM photo for the isolation trenches

3.1.4 Mesa Size Control and Implantation Design

In order to fabricate the normally-off JFETs, the channel width needs to be well controlled below $0.4\ \mu\text{m}$, as chapter 2.2.3 designed. The sidewall implantation depth is limited by the implantation energy and the maximal tilt angle set by the pitch size and trench width. Therefore, the mesa size is targeted at $1.1 \pm 0.1\ \mu\text{m}$ and the corresponded trench width is $2.6\ \mu\text{m}$, as shown in Fig. 2.2. However, the mesa sizes are usually wider than the target after etching. An isotropic mesa trimming process was developed to cut the mesa size down into the $1.1\text{-}\mu\text{m}$ range. The zero bias, $\text{CF}_4\text{-O}_2$ plasma based ICP etching can not only trim the mesa size but also improve the etched SiC surface. Fig. 3.4 shows the SEM photos of a group of mesas before and after 40 min trimming.

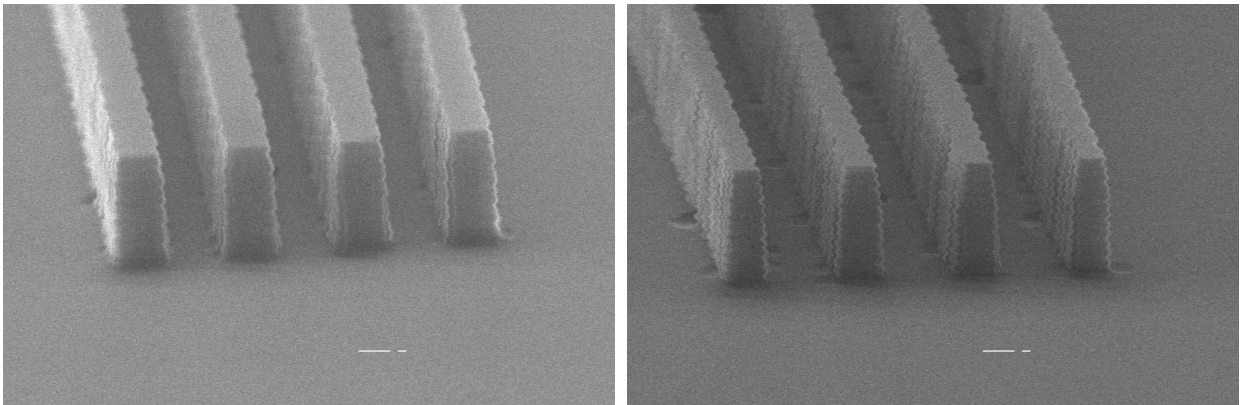


Fig. 3.4 The SEM cross-sectional view photos for a group of mesas: (a) before trimming; (b) after 40min trimming.

The implantation simulation is carried out by Profile Code with Person IV distribution assumption [88]. The tail of aluminum (Al) ion implantation profile in the sidewall is modeled by a linear degradation of $100\ \text{nm}$ per decade on a semi-log plot, as

shown in Fig. 3.5. The implantation depth is defined by the intersection of implantation tail and the channel doping.

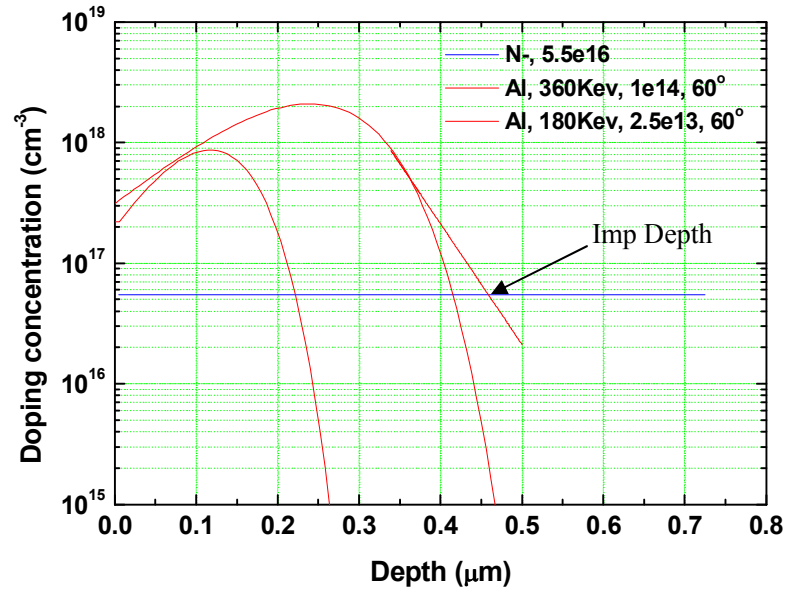


Fig. 3.5 Channel doping profile of the Gate sidewall implantation: the peak doping concentration is $2e18 \text{ cm}^{-3}$.

3.1.5 Gate and Isolation Implantation

To create the Al ion implantation mask, 1- μm thick molybdenum (Mo) is sputtered and patterned by the lithography with two exposures of Gate and Isolation masks respectively, and then by the following wet etching. The e-beam cured, 3- μm thick photo resist (PR) was actually used to replace the Mo implantation mask for other samples, which defines a 1- μm longer drift length than the Mo mask. The schematics of the implantation mask are plotted in Fig. 3.6. A vertical Al ion implantation is done to form p++ layer for better ohmic contacts. Then, four groups of tilt Al ion implantations are

carried out to create the submicron channels in the range between 0.25 to 0.45 μm that are extremely critical to form the normally-off VC-LJFETs [51, 88-90]. The four groups of implantations from the four directions with the same tilt angle guarantee the full conversion of mesa sidewalls and mesa ends into the p Gate with a concentration of $2 \times 10^{18} \text{ cm}^{-3}$, as shown in Fig. 3.5. The submicron channel definition follows exactly what TIVJFET does [51, 88], however the exposure of the whole mesa region during implantation relieves the process difficulty to define a Mo mask on the mesa top. The exposed mesa top n++ layer are also partially compensated by the p-Gate implantation, as shown in Fig. 3.7, and therefore needs to be removed. Isolation trenches are also implanted in this step to form a p++ layer for ohmic contact.

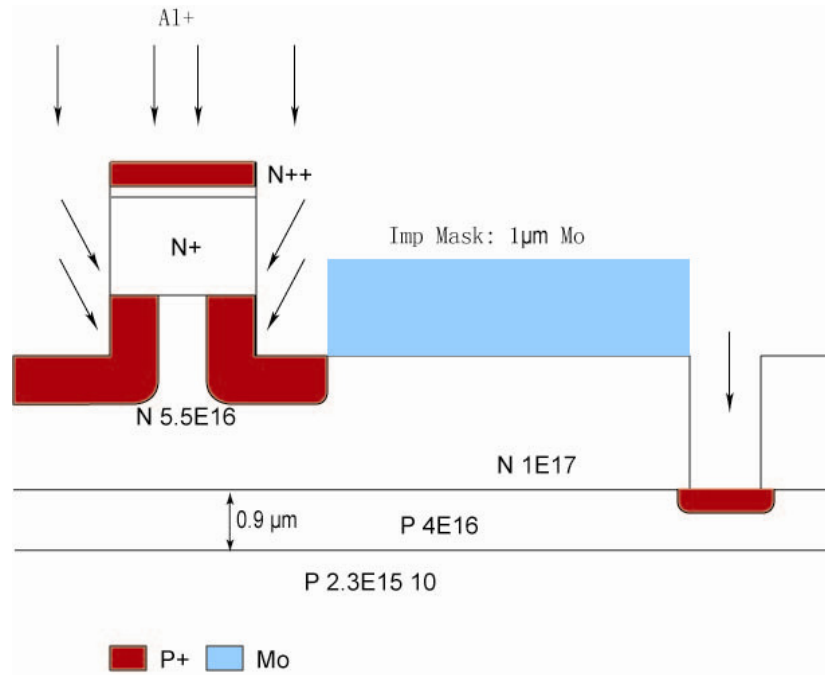


Fig. 3.6 Schematics of Gate and Isolation implantation mask

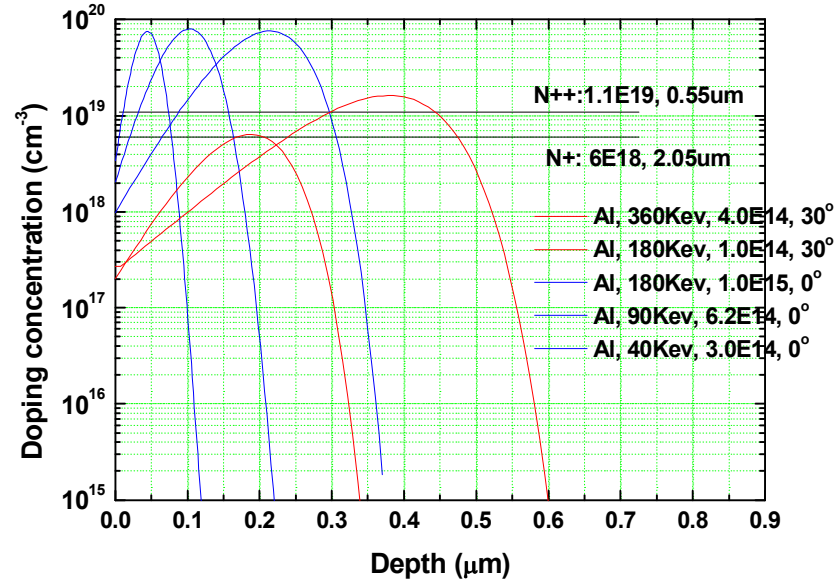


Fig. 3.7 Vertical doping profiles after p-Gate implantation

3.1.6 Drain and RESURF Implantation

After the Gate implantation, a nitrogen ion implantation of a box profile with the concentration of $1\text{e}19\text{ cm}^{-3}$ and the depth of $0.2\text{ }\mu\text{m}$ is done to form the n++ Drain. The top p-RESURF is formed by Al ion implantation with a resulting concentration of $6.5\text{e}17\text{ cm}^{-3}$ and a depth of $0.2\text{ }\mu\text{m}$. Note that only high voltage devices need RESURF implantation. The whole p-Gate and mesa region is exposed during the RESURF implantation. The sample is then annealed at 1550°C in Ar ambient for 30 minutes to activate the implanted Al and N. Fig. 3.8 shows the implanted device structure.

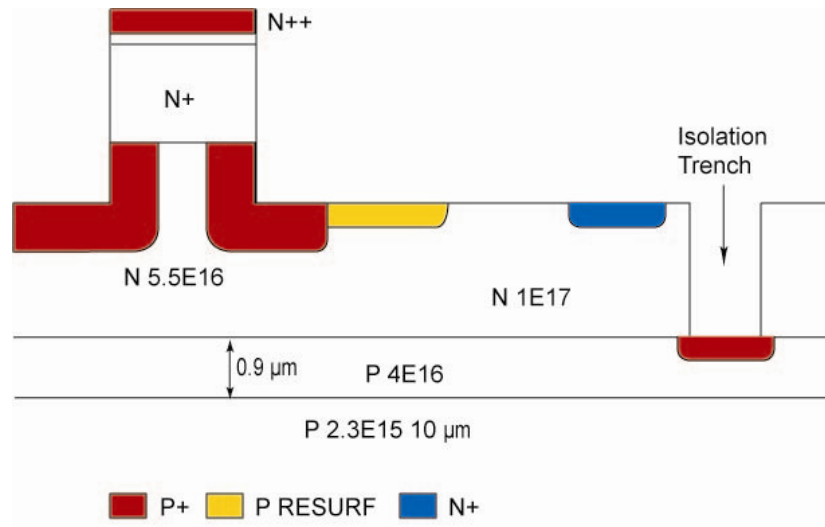
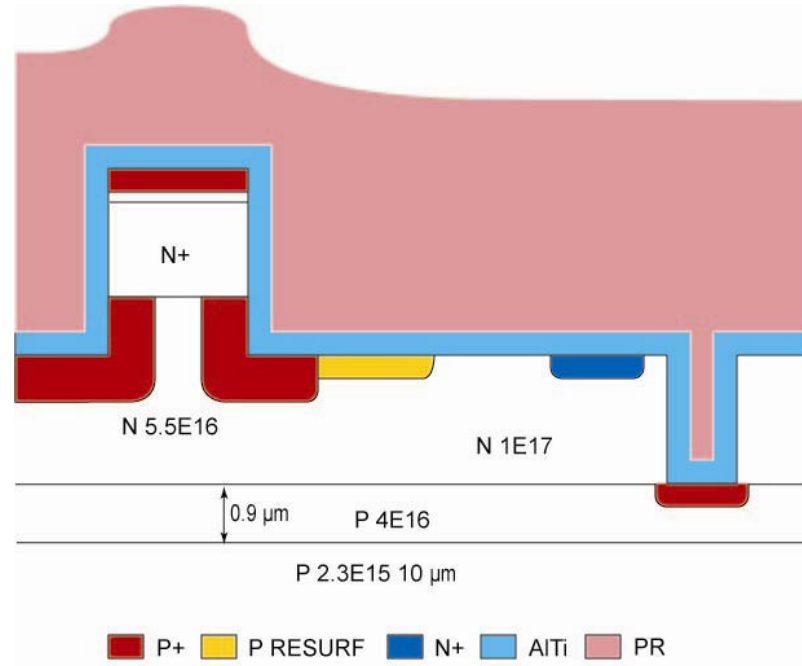


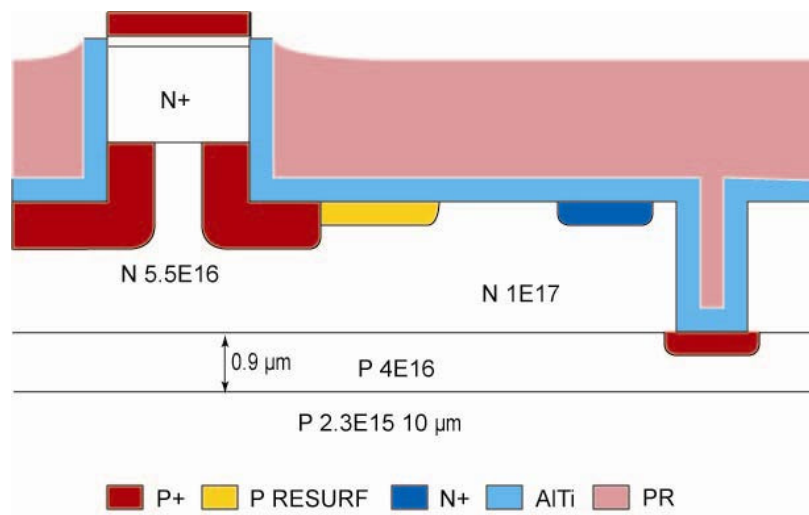
Fig. 3.8 Schematic of the device structure after all implantations

3.1.7 Mesa Top Removal

The mesa top n^{++} region ($1e19 \text{ cm}^{-3}$) is compensated by p^{++} implantation ($2e19$ to $1e20 \text{ cm}^{-3}$), as shown in Fig. 3.7, and hence must be removed to avoid deteriorated Source ohmic contact. A so called self-aligned process assisted by the PR etch back is used to define the SiC mesa etching mask without lithography requirement. The PR assisted self-aligned process, mainly inherited from TIVJFET fabrication, is repeatedly used in multiple following process steps as well. A 500 nm AlTi is sputtered and then a layer of PR coating is spun on AlTi surface, as shown in Fig. 3.6 (a). PR is etched back by O_2 plasma to expose the AlTi on the mesa top, and then AlTi is removed by wet etching from mesa top, as illustrated in Fig. 3.6 (b). After PR removal from the surface, the AlTi mask for the mesa top removal is well defined. Then about 0.5 to 0.6 μm SiC is removed from the mesa top by CF_4 - O_2 plasma in ICP etcher.



(a)

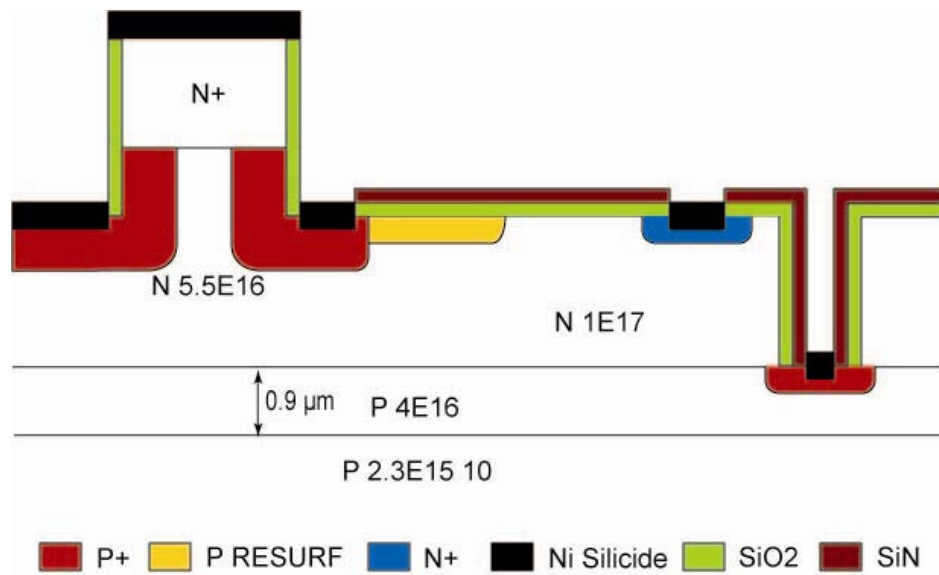


(b)

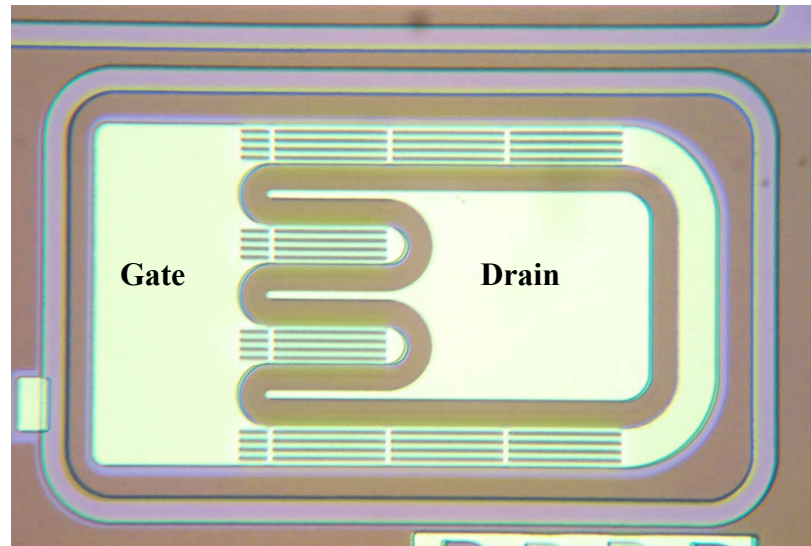
Fig. 3.9 Schematics of the mesa top removal procedures: (a) PR profile after planarization spinning; (b) after PR etch back and AlTi wet etching.

3.2 Oxidation and Ohmic Contact

The surface passivation is accomplished by a 2-hour oxide growth in wet O_2 at 1100°C , followed by a 200nm-thick plasma-enhanced chemical vapor deposition (PECVD) silicon nitride. Source, Gate, Drain, Isolation, and resistor ohmic contacts are then formed by nickel (Ni) annealing at 1000°C in 5% H_2 and 95%Ar forming gas. Fig. 3.10 (a) shows the schematic cross section view of the device after ohmic contact formation, and Fig. 3.10 (b) shows an optical photo for a small HV testing VC-LJFET.



(a)



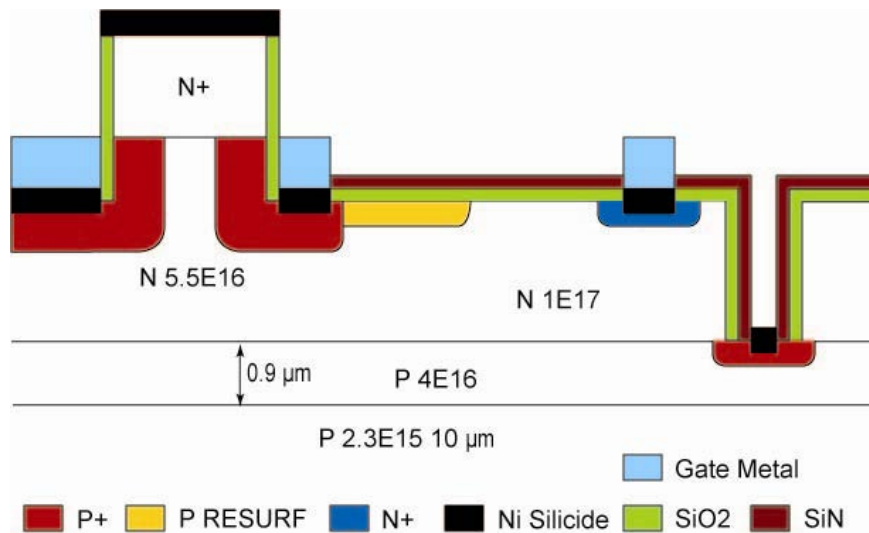
(b)

Fig. 3.10 after oxidation and ohmic contact formation: (a) Schematic of the device cross section; (b) An optical photo of a small testing HV JFET.

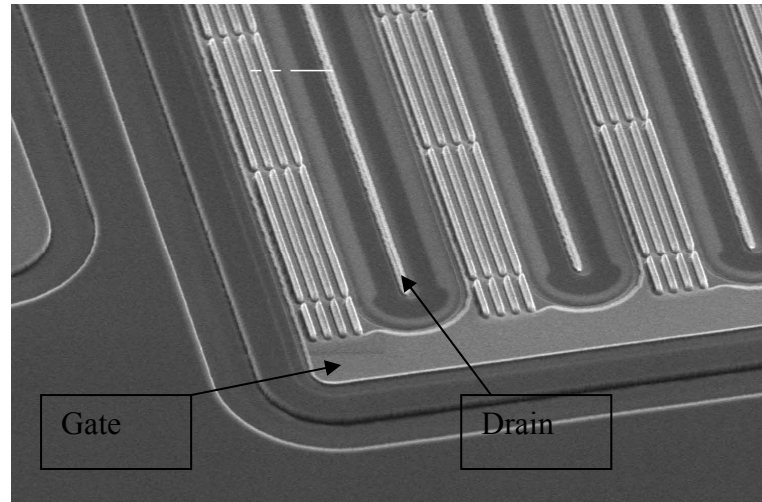
3.3 Metallization

3.3.1 Gate and Drain Metal Thickening

In order to reduce the Gate series resistance, 1- μm Mo is sputtered and patterned by the Gate overlay lithography followed by wet etching. The Mo in the mesa-trench region is unable to be defined by the lithography and wet etching because of the limited trench width (2 μm wide only). To solve the process difficulty, a similar self-aligned process, as shown in section 2.6, is developed. PR etch back level needs to be much lower than the case in Fig. 3.9 (b) to expose the metal on the mesa top and sidewall. Then Mo is removed from mesa top and sidewall by wet etching with precisely controlled over etch time. In the meantime, Drain metal is also thickened. Please refer to Fig. 3.11.



(a)



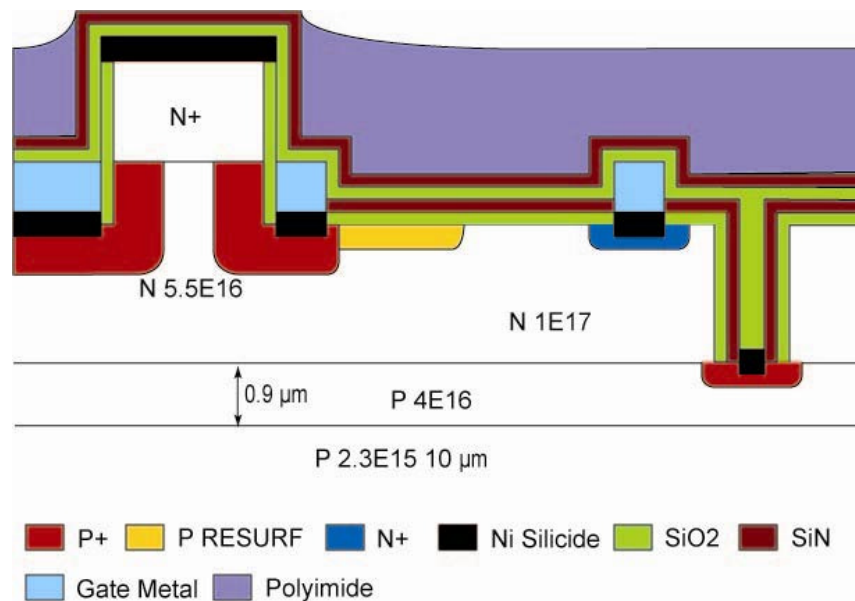
(b)

Fig. 3.11 Gate overlay: (a) Schematic of the device cross section; (b) SEM photo of a large device corner.

However, there are some process difficulties for the Gate overlay process. In this design, the patterning of the Gate metal shares the same ohmic contact window mask and therefore the Drain metal line after the Mo wet etching becomes so thin that would be easily peeled off. The process window for the Mo removal from the mesa top and sidewall is too small to succeed each time. And the adhesion of Mo to Ni silicide is not well studied and even the large area Mo peeling off was also observed in the fabrication. In order to evaluate the necessity or the benefit of Gate metal, another sample without Mo Gate metal was also fabricated and the Gate resistance comparison will be discussed in next chapter.

3.3.2 Interlayer Dielectric (ILD) and Planarization

The interlayer dielectric is composed of 200 nm SiO₂, 200 nm SiN, both by PECVD, and followed by a 2- μ m Polyimide to fill up the trenches. Then PR/Polyimide etch back is carried to expose the dielectric layer on the mesa top, as shown in Fig. 3.12 (a). Dielectric layer is removed by CF₄ plasma in ICP etcher from the mesa top, and then Vias for Gate, Drain, Isolation, and resistor contacts are also opened by CF₄ plasma, as shown in Fig. 3.12 (b).



(a)

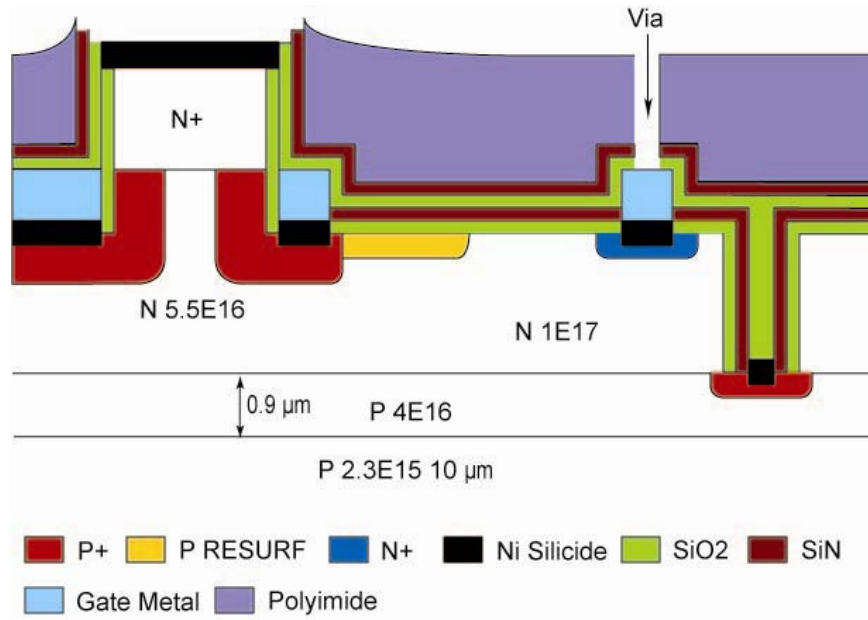


Fig. 3.12 Schematic of the device cross section for the IDL and Via formation: (a) after Polyimide/PR etch back; (b) after Via opening.

Another approach to fill the trenches by PECVD SiO_2/SiN is also developed to avoid using polyimide for the purpose of improving higher temperature performance of the VC-LJFETs. The etching of silicon dioxide and silicon nitride by CF_4 plasma is tougher as compared with the O_2 plasma etching of polyimide. While oxide and nitride enhance the temperature performance to above 300°C , the polyimide can fill trenches much more effectively than the dielectrics. Both approaches can be tailored for applications at different temperatures.

3.3.3 Metal Overlay

1.3- μm Al is sputtered and patterned by overlay lithography and wet etching to form electrical connections for all FETs and resistors, as shown in Fig. 3.13. Wafer level testing is done at this stage to determine the device forward and reverse properties, and digital inverter performance, resistor values are characterized. Fig. 3.14 shows two optical photos for a fabricated HV VC-LJFET (medium size, $4.01 \times 10^{-3} \text{ cm}^2$) and the super buffer circuitry to drive the power JFET. It is ready for preliminary on-chip characterizations.

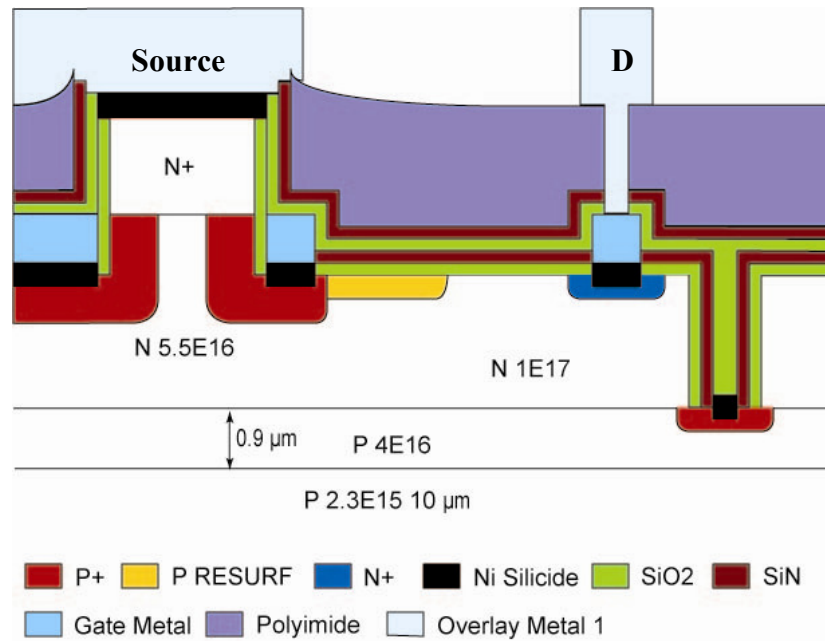
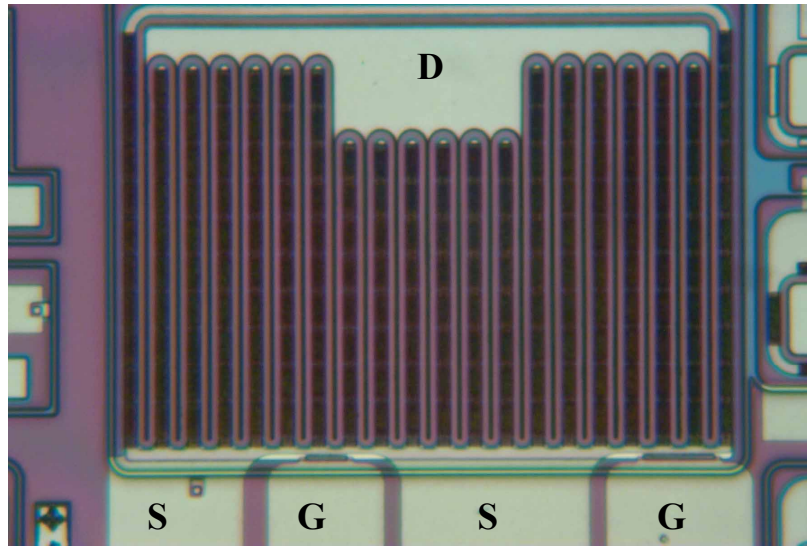
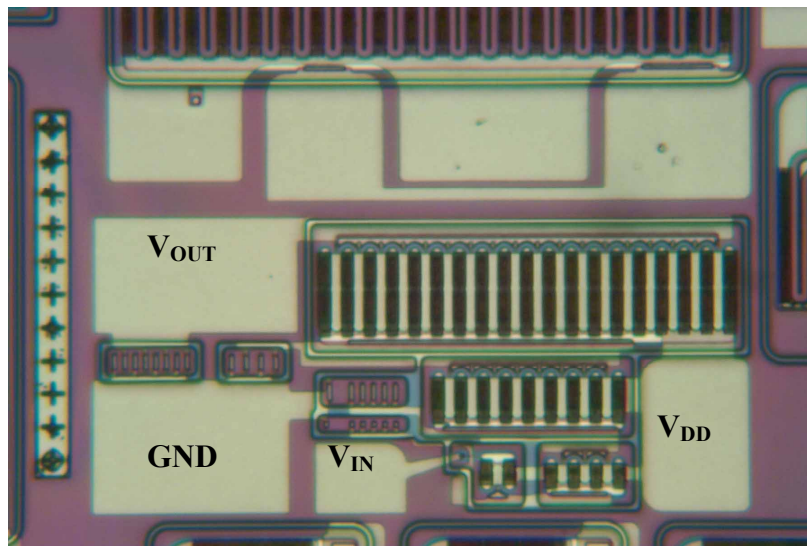


Fig. 3.13 Schematic of the device cross section view after overlay formation



(a)



(b)

Fig. 3.14 Optical photos for the 4H-SiC power integrated circuits after Al overlay: (a) the medium size power JFET, $4.01 \times 10^{-3} \text{ cm}^2$; (b) the buffer driver circuits.

3.3.4 Final Passivation and Bonding Pad

After preliminary test, 2- μm additional Polyimide is deposited to seal all devices. Subsequently, a 1.5- μm Au layer is defined by lift-off process to form the pad region for wire bonding. Fig. 3.16 shows the photo of a large HV VC-LJFET ($1.59 \times 10^{-2} \text{ cm}^2$) and its double buffer circuitries after bonding pad formation.

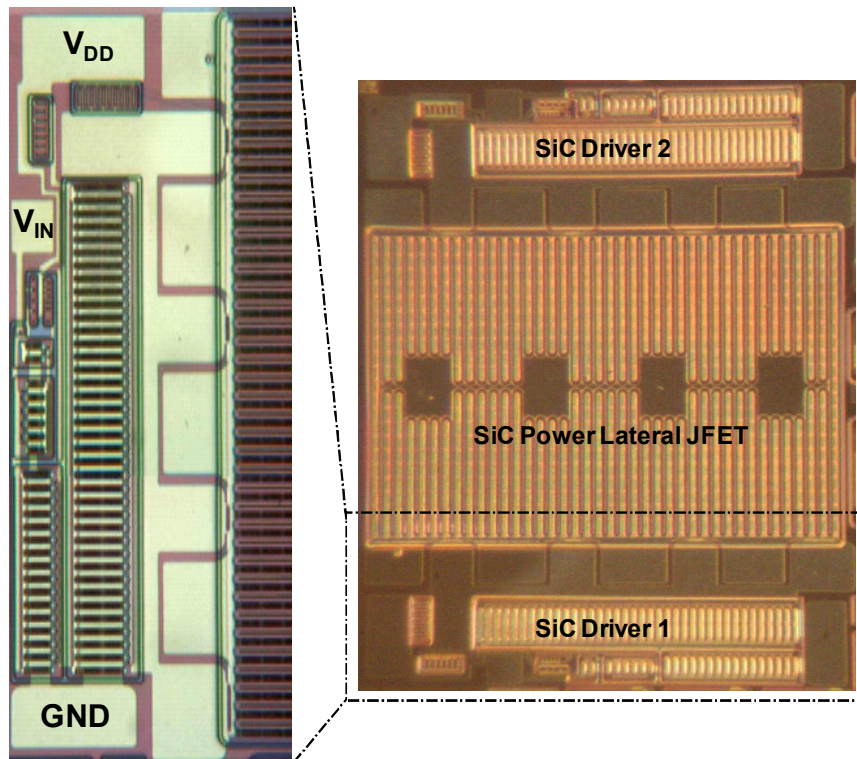


Fig. 3.16 Optical photo for the first monolithic 4H-SiC power integrated circuits: A large power JFET with two buffer circuitries.

3.4 Packaging

After gold overlay on the bonding pads is completed, functional chips are cut from the sample by a dicing saw. The chip is then mounted on a hermetic package by silver nano paste [91] followed by 325 °C curing for 1.5 hour. Then 1-mil thick gold wires are used for bonding. Refer Fig. 3.17 for a packaged SiC power IC chip.

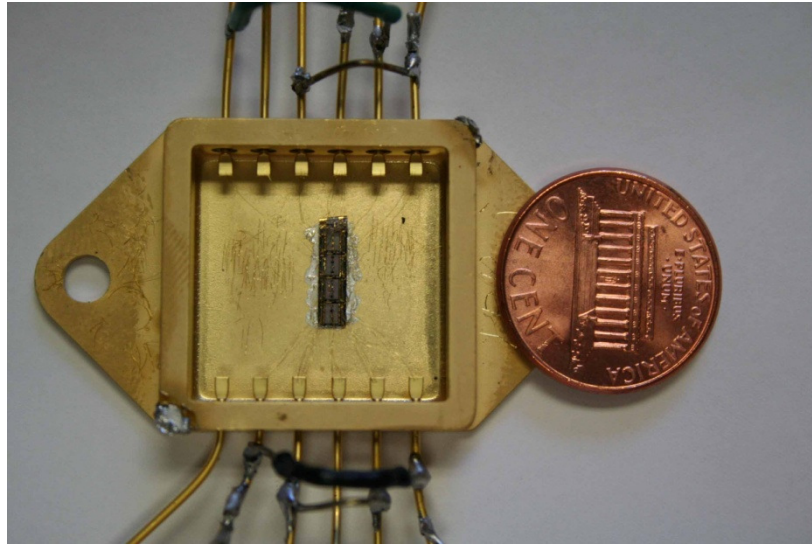


Fig. 3.17 An optical photo for the 4H-SiC power integrated circuits after packaging.

3.5 Fabrication Summary

Five different samples from two 2-inch 4H-SiC wafers were fabricated and summarizes in Table 3.1. Among them, the sample PWIC-1PR and PWIC-2PL were successfully fabricated and packaged, and all the packaged device characterizations were from these two sample batches. The fabrication procedures described above are mainly for sample PWIC-1PR. By replacing polyimide by dielectrics ($\text{SiO}_2/\text{Si}_3\text{N}_4$), the fabricated devices might be able to operate at temperatures as high as 500 °C. The planarization process for trench fill is well established in Si Fab either by using polyimide or oxide and nitride. However, it is relatively more troublesome for the dielectric planarization process because of the limited university facilities. The process steps to define Mo Gate metal is also removed from the PWIC-2PL batch. In order to achieve the high temperature reliable operation, the Al metallization needs to be replaced by other high temperature metals. The new metallization requires further process development to enable the patterning, good adhesion and coefficient of thermal expansion (CTE) matching between layers, and the process compatibility with the final Au layer for wire bonding purpose.

Table 3.1 Summary of fabricated power IC samples.

Wafer ID	Sample ID	Channel Length	Implantation Mask	Gate Metal	Trench Fill	Drift Length	Comment
CY0796-25	PWIC-1PL	1.8 μm	PR	1 μm Mo	Polyimide	7 to 9 μm	failed after on-chip test
	PWIC-1PR	1.8 μm	PR for n ⁺ , Mo for p ⁺	1 μm Mo	Polyimide	6 to 8 μm	successful
	PWIC-1PD	1.8 μm	PR for n ⁺ , Mo for p ⁺				testing purpose
JC0006-01	PWIC-2PL	2.1 μm	PR	no metal	SiO_2 and Si_3N_4	7 to 9 μm	successful
	PWIC-2PR	2.3 μm	PR				stopped before oxidation

4. CHARACTERIZATION

4.1 Device and Resistor Characterizations

4.1.1 Diode Blocking Test during Fabrication

The lateral diode listed in Table II is used for blocking voltage tests during the fabrication. The tests are carried out at different stages, i.e. before RESURF, after RESURF, and after ohmic contact formation. At least five diodes are tested across the whole sample. As an example, the blocking voltages of a lateral diode at different stages are shown in Fig. 4.1. The blocking test results after gate and drain implantation without the top RESURF region show the breakdown voltage in the range of 400 V to 600 V. They improved significantly to the range between 900 V and 1000 V after the RESURF regions are formed with a depth between 0.2 μm and 0.3 μm and a doping level at $6.5 \times 10^{17} \text{ cm}^{-3}$. PECVD SiO_2 with the thickness of 60 nm or 100 nm is used on different regions of the wafer as the shielding mask during RESURF implantation to reduce the surface damage and introduce varied RESURF doses purposely. Another control sample consisting regions of 100 nm, 50 nm, and zero SiO_2 shielding layer is also implanted at the same time. However, no conclusion about the optimal SiO_2 thickness is made because the breakdown voltage differences among devices with different masking oxide thicknesses are insignificant when compared to that caused by the variation of the drift length L_{drift} across the whole sample. On the other hand, the consistent breakdown voltages between 900 V and 1000 V from the actual sample indicate that the designed RESURF dose probably hit the optimum or is very close to it. The test results after the ohmic contact annealing show similar breakdown voltages but at higher reverse leakage levels. Higher leakage currents may be due to charges introduced during oxidation and

ohmic contact annealing. Nevertheless, the absence of significant breakdown voltage degradation indicates that the dose of charges introduced is not sufficient to affect the RESURF effectiveness. More results regarding the optimization of RESURF structure will be further discussed in chapter 5.

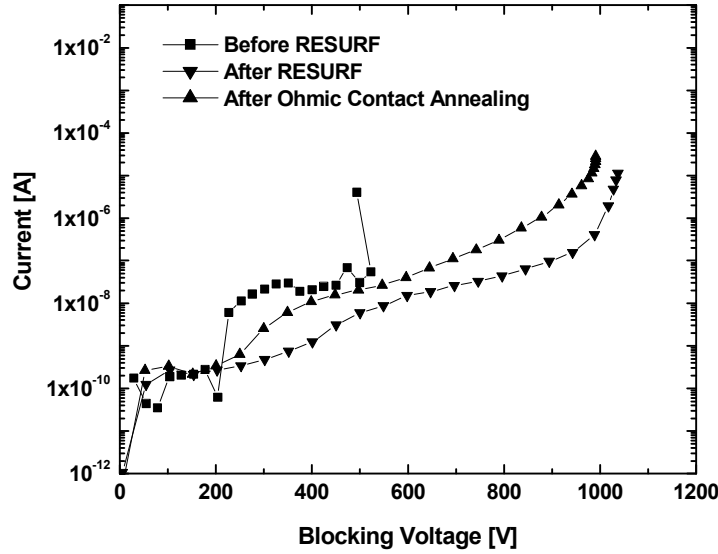


Fig. 4.1 The breakdown performance of a lateral diode during fabrication.

4.1.2 Basic Theory for the JFET Characterization

The purpose of this section is to revisit the well-established basic JFET theories [57] that will be used for the device characterizations. The detailed compact modeling of the VC-LJFET is beyond the scope of this thesis. As for a uniformly doped channel, the Drain current of the n-type JFET, I_{DS} , can be calculated by [57]

$$I_{DS} = I_P \left[3(u_2^2 - u_1^2) - 2(u_2^3 - u_1^3) \right], \quad (\text{Eq. 4.1})$$

where $I_p = \frac{Z\mu_n q^2 n^2 a^3}{6\epsilon_s L_{CH}}$ (Eq. 4.2), is the pinch-off current,

$$u_1 = [(V_{bi} - V_{GS})/V_p]^{1/2}, \quad (\text{Eq. 4.3})$$

$$u_2 = [(V_{DS} - V_{GS} + V_{bi})/V_p]^{1/2}, \quad (\text{Eq. 4.4})$$

$$V_p = \frac{qna^2}{2\epsilon_s} \quad (\text{Eq. 4.5}), \text{ is the pinch-off voltage,}$$

n is the channel doping, a is the half channel width (W_{CH}), Z is the device unit cell width, and L_{CH} is the channel length. The threshold voltage of a JFET is defined by

$$V_{TH} = V_{bi} - V_p. \quad (\text{Eq. 4.6})$$

In the saturation region, the Drain current expression can be simplified using Taylor's expansion around $V_{GS} = V_{TH}$ from Eq. 4.1 to be

$$I_{DS} = \frac{\mu_n \epsilon_s}{W_{CH}} \frac{Z}{L_{CH}} (V_{GS} - V_{TH})^2 = \beta (V_{GS} - V_{TH})^2, \quad (\text{Eq. 4.7})$$

which is very similar to the square law of the MOSFET. Considering the channel length modulation effect, the Drain current needs to be modified by

$$I_{DS} = \beta (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}), \quad (\text{Eq. 4.8})$$

where λ is the channel length modulation coefficient. In the linear region, when $V_{DS} \ll V_{GS}$ and $V_{DS} \ll V_{bi}$, Eq. 4.1 reduced to [92]

$$I_{DS} = 4\beta V_p \left(1 - \sqrt{\frac{V_{bi} - V_{GS}}{V_p}} \right) V_{DS}. \quad (\text{Eq. 4.9})$$

Eq. 4.9 can be further simplified by Taylor's expansion around $V_{GS} = V_{TH}$ to

$$I_{DS} \approx 2\beta (V_{GS} - V_{TH}) V_{DS}, \text{ when } V_{GS} \approx V_{TH}. \quad (\text{Eq. 4.10})$$

There are two ways to extract threshold voltages of FETs from transfer I-V curves. The first method is to force the FET working in the saturation region by setting large V_{DS} while scanning V_{GS} ($V_{GS} < V_{DS}$). The square root of the Drain current is proportional to the V_{GS} , which can be derived simply from Eq. 4.7. Another way is to set very small V_{DS} and scan V_{GS} . In this case the Drain current is linearly dependent on the V_{GS} when V_{GS} is around V_{TH} , as shown by Eq. (4.10).

4.1.3 Characterizations of High Voltage VC-LJFETs

4.1.3.1 DC Characterizations

Fig. 4.2 combines both forward and reverse characteristics of a normally-off 4d-mesa VC-LJFET with a device active area of $8.37 \times 10^{-5} \text{ cm}^2$. The gate currents at different gate biases are also recorded when the forward I-V curve is measured. The N^+ substrate and the P isolation region are grounded during these measurements. The device on-resistance measured at $V_{GS}=3.0 \text{ V}$ and $V_{DS}=1 \text{ V}$ is $107 \text{ } \Omega$. At the same condition the gate current is found to be only $64 \text{ } \mu\text{A}$ corresponding to the gate leakage current density of 0.8 A/cm^2 when the drain current is 9.17 mA that leads to the Drain-to-Gate (DG) current ratio of 143. At $V_{GS}=2.5 \text{ V}$ and $V_{DS}=1 \text{ V}$, the drain current is 8.64 mA while the gate current is only $3.7 \text{ } \mu\text{A}$ which gives a DG current ratio of 2335. The exponential increase of gate current when $V_{GS} > 2.5 \text{ V}$ requires a careful design of the voltage swing and level for the gate driver circuits used to switch the power VC-LJFET. The device has a specific on-resistance of $9.1 \text{ m}\Omega \cdot \text{cm}^2$ with a blocking voltage of 1028 V at $26 \text{ } \mu\text{A}$, giving a FOM of 116 MW/cm^2 . The threshold voltage of this device is found to be around 0.2 V . Other normally-off devices of the same type show similar blocking performance. Variations in

device specific on-resistance between 9 and 15 $\text{m}\Omega\cdot\text{cm}^2$ and in device threshold voltage between 0.2 V to 1.5 V are observed. One reason for such variations can be attributed to the epitaxial doping variation for the n-layer across the wafer. A lower doping can lead to a narrower effective channel opening and a higher device specific on-resistance. The channel width variation resulted from the mesa line width variation across the wafer can also contribute to the threshold voltage spreading.

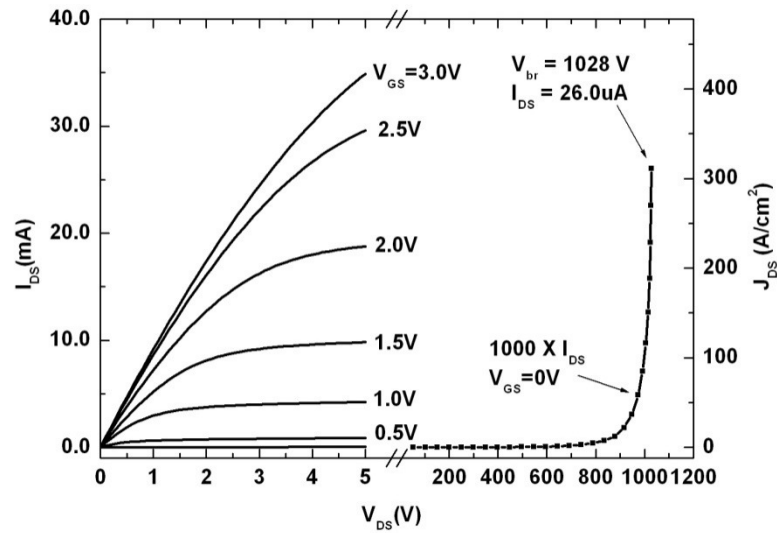


Fig. 4.2 Drain current I_{DS} versus drain voltage V_{DS} characteristics of the fabricated 4H-SiC normally-off VC-LJFET. The device active area is $8.37 \times 10^{-5} \text{ cm}^2$.

Fig. 4.3 shows on-chip performance of the medium size HV VC-LJFET with an active area of $4.01 \times 10^{-3} \text{ cm}^2$ that can handle current close to 1A. The device has a specific on-resistance of $12.9 \text{ m}\Omega\cdot\text{cm}^2$ at $V_{GS}=3.5 \text{ V}$ and $V_{DS}=1 \text{ V}$ that is about 40% higher than the small 4d-mesa device. This is partly due to a higher threshold voltage (1 V) caused possibly by a lower channel doping in this region of the wafer or a smaller mesa line width, as explained above. At a drain bias of 1V, the gate leakage current densities are measured to be 2.5 A/cm^2 and 0.75 A/cm^2 at gate voltages of 3.5V and 3.0V, respectively.

This is consistent with the gate current density of the smaller device described above. Performances of these large devices indicate that the VC-LJFET structure can be readily scaled up by a proper layout and process design to handle power levels useful for practical power applications.

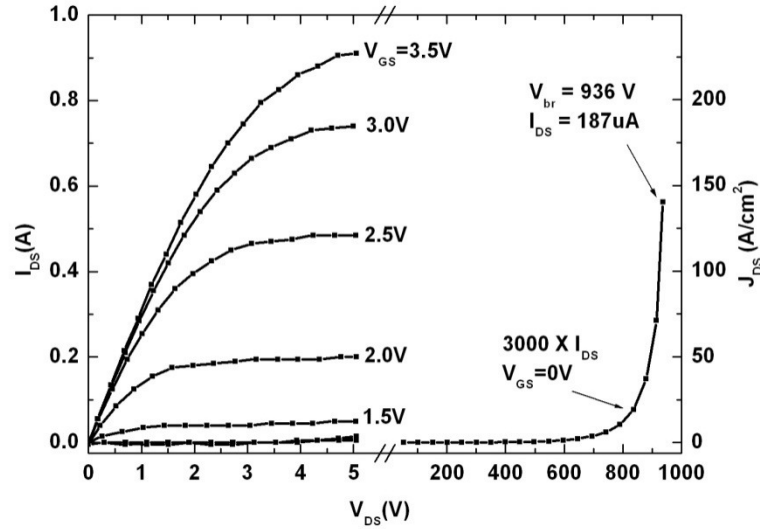


Fig. 4.3 Drain current I_{DS} versus drain voltage V_{DS} characteristics of the fabricated 4H-SiC normally-off VC-LJFET. The device active area is $4.01 \times 10^{-3} \text{ cm}^2$.

Fig. 4.4 plots the specific on-resistance versus breakdown voltage for the most notable SiC lateral power devices reported in the voltage range between 400 V and 3000 V. Lateral devices higher than 3000 V have not been reported for either Si or SiC. Lateral silicon super-junction DMOS are also included for comparison together with the theoretical 1-D silicon limit. It is evident that the device reported in this paper presents by far the lowest specific on-resistance as well as the highest FOM.

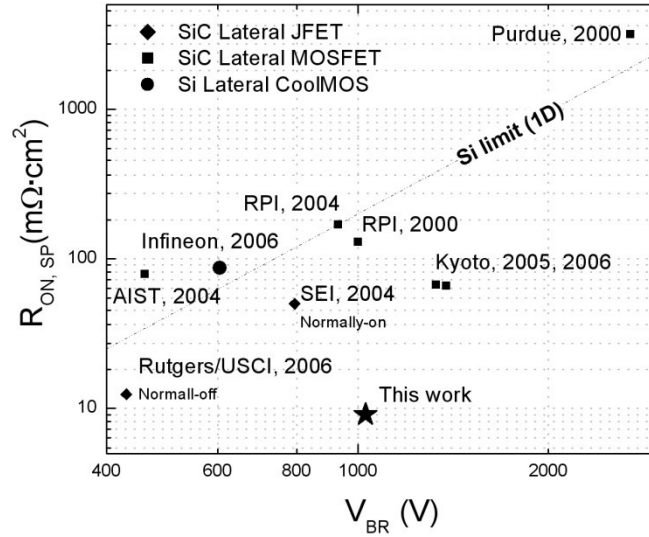
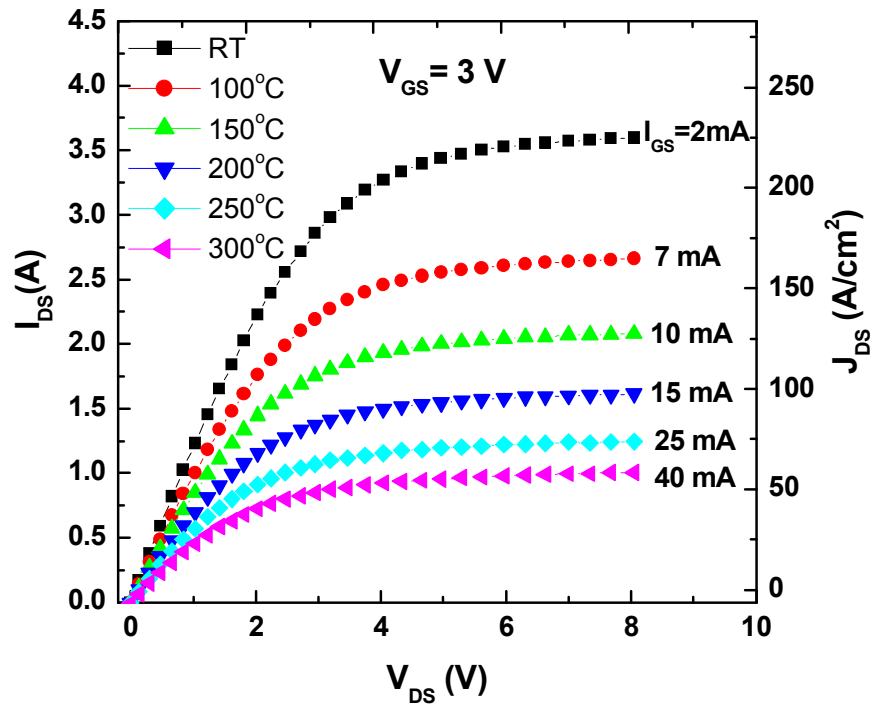


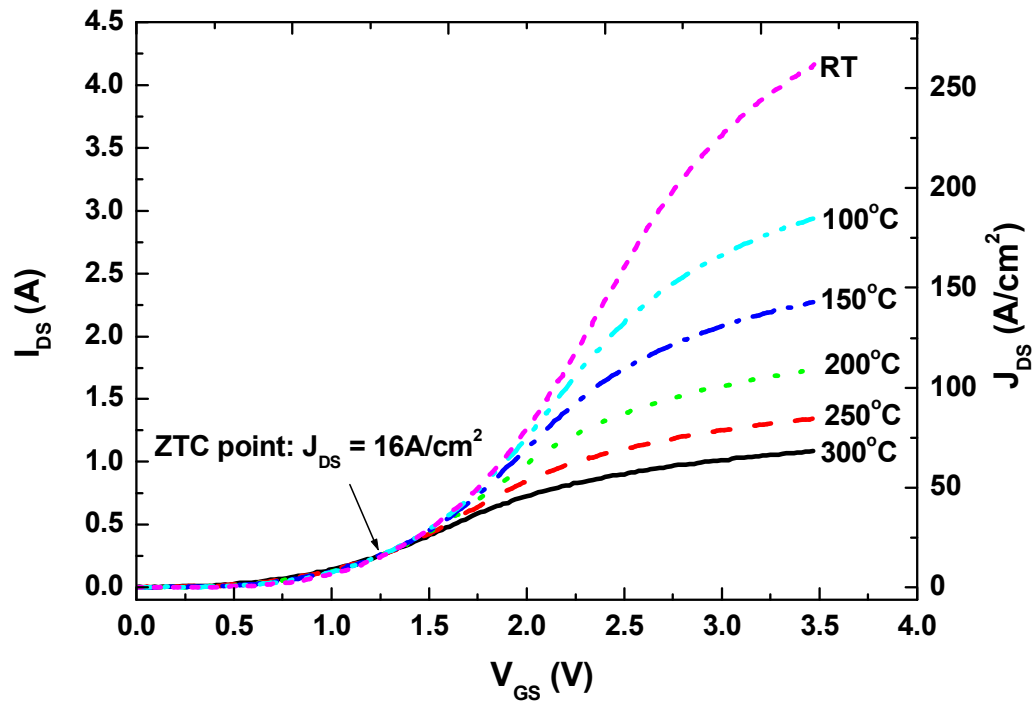
Fig. 4.4 Specific on-resistances versus breakdown voltages for SiC lateral power devices. The state-of-the-art lateral silicon device is also included for comparison.

The forward performance of a packaged large HV VC-LJFET with an active area of $1.59 \times 10^{-2} \text{ cm}^2$ is characterized at room temperature, and at temperatures from 100 °C to 300 °C with 50 °C steps. The output I-V curves at different temperatures are shown in Fig. 12(a) with a constant V_{GS} of 3 V. The corresponding gate currents are also estimated based on the current driven measurement results, and are listed in Fig. 4.5 (a). By assuming the on-state $V_{DS} = 2 \text{ V}$, the Drain-Gate current ratio of 1100 at room temperature decreases to 18 at 300 °C. The voltage transfer curves are measured and I_{DS} versus temperature at different V_{GS} is extracted and shown in Fig. 4.5 (b). The threshold voltage extracted from transfer curves is 0.6 V at room temperature and decreases to around 0.1 V at 300 °C. As illustrated in Fig. 4.5 (b), the zero temperature coefficient (ZTC) is observed at $V_{DS} = 1.25 \text{ V}$ with a current density of 16.5 A/cm^2 . Avalanche breakdown voltages vary between 800 V and 1000 V on small HV VC-LJFETs; and the

highest blocking voltage observed (1028 V) is comparable to the numerical prediction [26]. Voltage blocking capabilities of large area devices have been measured and confirmed to be >600V. The real device avalanche breakdown voltages for these large area devices have not been tested due to the possible destructive nature of such measurements and the limited number of functional devices of this size.



(a)



(b)

Fig. 4.5 Output and transfer characteristics for a large HV VC-LJFET: (a) output; (b) transfer.

4.1.3.2 C-V Characterizations for Packaged Devices

In addition to DC characterizations, the device capacitance is characterized on a packaged medium VC-LJFET with an active area of $4.01 \times 10^{-3} \text{ cm}^2$ by C-V measurements. Fig. 4.6 shows the output capacitance C_{OSS} - V_{DS} curve that clearly indicates a capacitance drop around V_{DS} of 30 V when the drift layer is depleted. In the mean time, the device C-V simulation fits the experimental data well except the transition region. The specific C_{OSS} decreases from 44 nF/cm² to 1.75 nF/cm² while V_{DS} increases

from 0 V to 100 V. The specific input capacitance (C_{ISS}) for the packaged device is found to be 55 nF/cm².

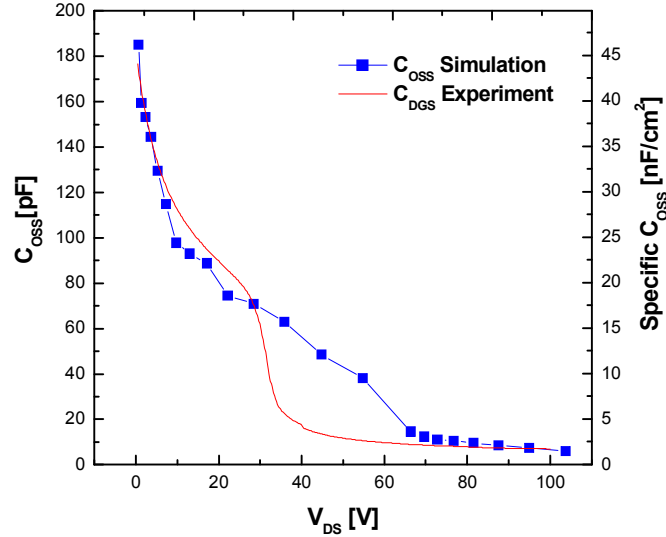


Fig. 4.6 C_{OSS} versus Drain voltage for a packaged medium HV VC-LJFET.

Considering both static and dynamic characteristics, $R_{ON,SP} \cdot C_{OSS,SP}$, a figure of merit (FOM) for high frequency resonant switching [84, 85], is calculated as 17.5 pF for the VC-LJFET technology by assuming the specific on-resistance of 10 m Ω ·cm². For comparison, specifications of two commercial Si RF LDMOS FETs [85] and a vertical power MOSFET [84] are listed in Table 4.1. It is noted that current VC-LJFET is comparable to the Si RF LDMOS (ST PD57018) in terms of the RC FOM while having an order of magnitude higher blocking voltage. It is also comparable to the state-of-the-art Si vertical CoolMOS in both FOM and breakdown voltage terms. Moreover, an improved design of the SiC VC-LJFET with a narrower P+ gate extension (4.15 μ m in Fig. 2) and a semi-insulating substrate has been simulated (details will be reported elsewhere). Comparison of the results against the devices mentioned above reveals that it

has the potential to match the RC FOM of the best Si RF LDMOS while at the same time achieving the breakdown voltage of the Si vertical CoolMOS.

TABLE 4.1

RC FOM and Blocking Voltage comparisons: Si LDMOS, Si Vertical Super Junction MOSFET (CoolMOS), and HV VC-LJFET

	$R_{ON,SP} \cdot C_{OSS,SP} (\Omega pF)$	$V_{BR} (V)$	Year	Device Type
ST PD57018	15.1@ $V_D=28V$	60-70	2003	Si RF LDMOS
Agere AGR09180EF	2.8@ $V_D=28V$	60-70	2005	Si RF LDMOS
Infineon SPP06N80C3	19.8@ $V_D=100V$	800	2003	Si CoolMOS
VC-LJFET	17.5@ $V_D=100V$	800-1000	2007	SiC LJFET
VC-LJFET Improved	4.4@ $V_D=100V$	1200	N/A	SiC LJFET

4.1.3.3 Switching Characterizations for Packaged Devices

The switching performance of a packaged large HV VC-LJFET has been characterized by using an external Si MOS gate driver. Fig. 4.7 shows the drive circuitry setup. The R-C filter between the Si MOS Gate driver and the SiC HV-LJFET serves several purposes. First it creates a temporary short for the high-frequency AC component of the input signal and hence obtaining a strong negative bias for a rapid turn-off of the

HV-LJFET. The negative gate bias is also necessary to turn the device completely off during the fast switching operation, when large dV/dt is applied and the charge/discharge current of the Gate-Drain capacitance may turn on the power FET [14]pp.395, especially for the low threshold voltage devices. Furthermore, the filter limits the current fed into the HV-LJFET gate during forward biasing duration by choosing an appropriate R value and provides compatibility to a standard MOS driver with output voltages of 15V or higher.

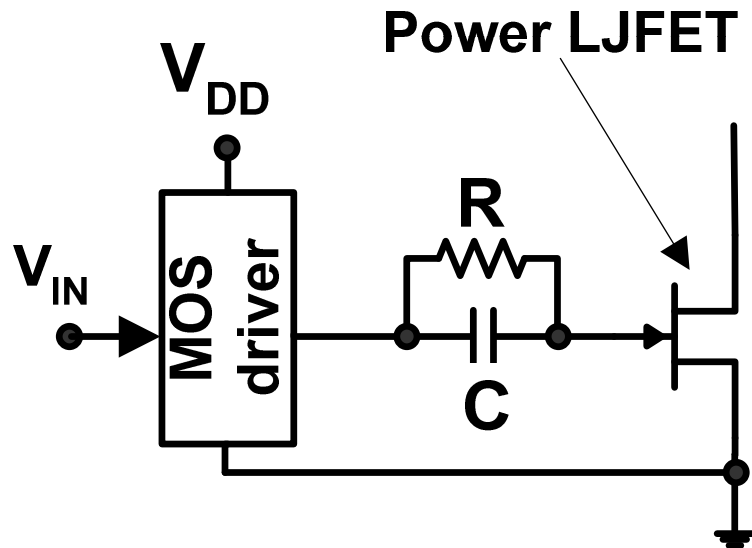
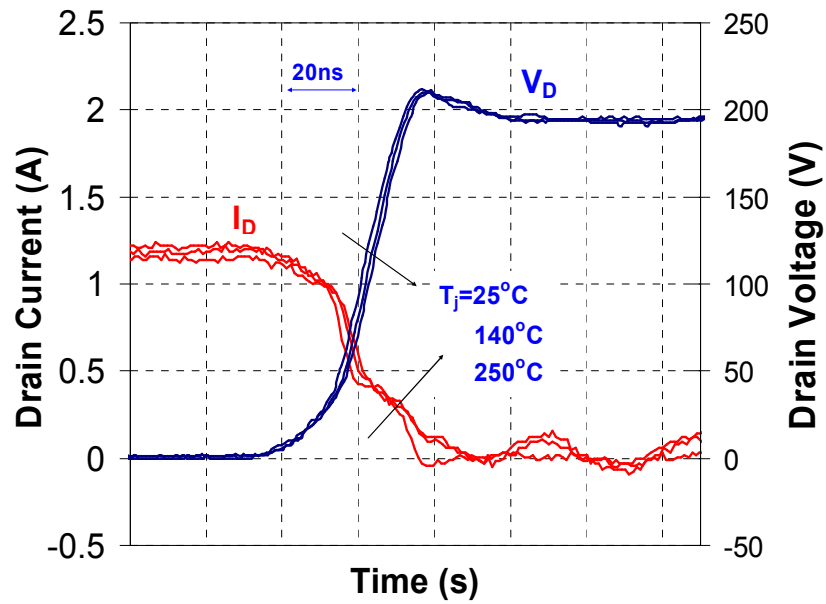


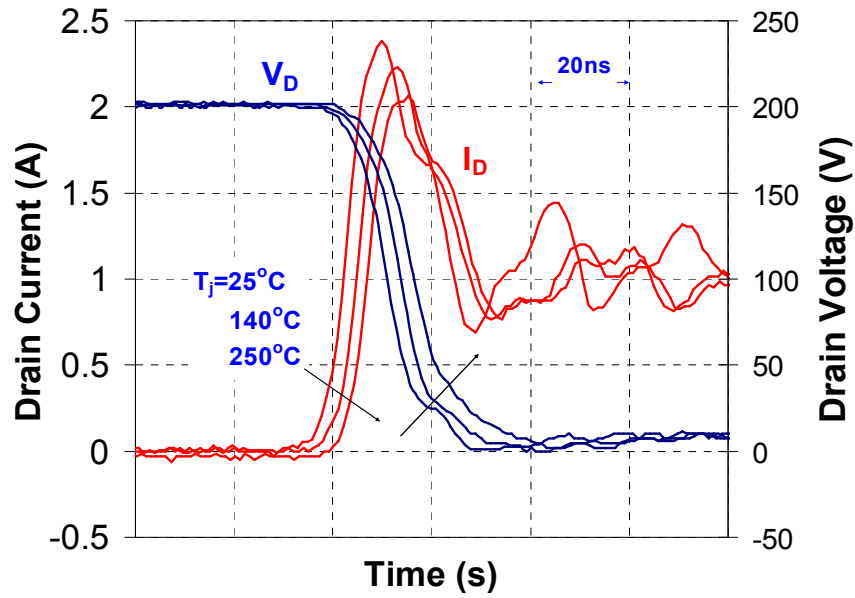
Fig. 4.7 A gate driver for SiC LJFET with an R-C filter and a normal MOS driver (TC1411). Note that a negative power supply is not required.

Inductive switching of the HV VC-LJFET with a SiC free-wheeling diode at 200V, 1.2A is evaluated at various temperatures by the gate-driving circuit with a standard double-pulse input signal. The results are shown in Fig. 4.8. Total turn-on and turn-off times of 20~30ns have been observed in the whole temperature range tested. As a

unipolar device, the switching speed of the HV-LJFET is virtually unchanged at temperatures as high as 250°C. The device turn-on current waveforms indicate that while the SiC Schottky Barrier Diode does not have any storage charge, its junction depletion capacitance lead to a reverse-recovery time of ~20ns and a significant current overshoot when the power SiC LJFET turns on with the internal driver. On the other hand, when the switch turns off, this same SiC SBD junction capacitance acts like a small turn-off snubber capacitor, reducing the transient device current when its voltage rises. This effectively reduces the turn-off loss, compensating the additional turn-on loss incurred from the SiC SBD depletion capacitance. It should also be noted that this reverse-recovery process does not result in net switching loss in the SiC SBD because it only involves displacement current.



(a)



(b)

Fig. 4.8 Inductive turn-off of the SiC power LJJFET at 200V, 1.2A at various temperatures. Device rise/fall times remains virtually unchanged at $\sim 20\text{ns}$. (a) turn-off and (b) turn-on.

4.1.3.4 DC Characterizations for Packaged Power JFETs in Parallel

The positive temperature coefficient of FET on-resistance leads to the parallel operation of multiple FETs, by which the power level can be scaled up. Three large size HV LJJFETs have been successfully co-packaged in one metal package, as shown in Fig. 4.9. Fig. 4.10 shows the forward I-V performance of three large power JFETs in parallel. The specific on-resistance of the packaged device is $30.3 \text{ m}\Omega\cdot\text{cm}^2$ when both V_{DS} and V_{GS} are equal to 4 V. It can be seen from Fig. 4.10 (b) that the gate current of 10 mA can obtain the Drain current close to 6 A.

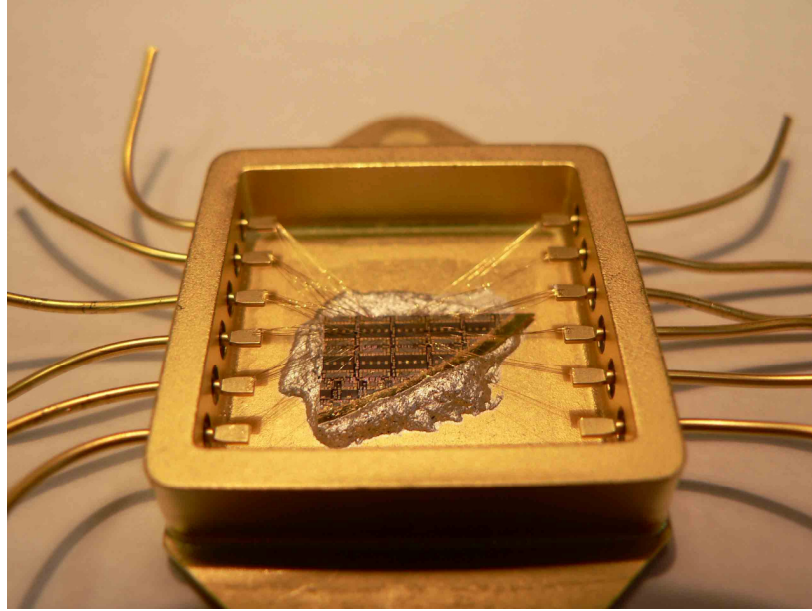
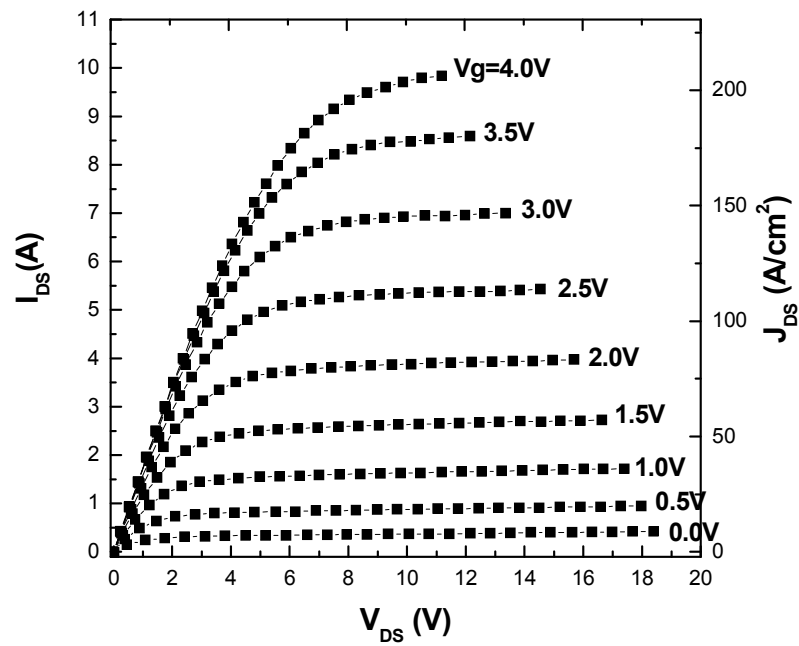


Fig. 4.9 Photograph of a packaged power JFET which co-packages 3 HV VC-LJFETs from sample PWIC-2PL.



(a)

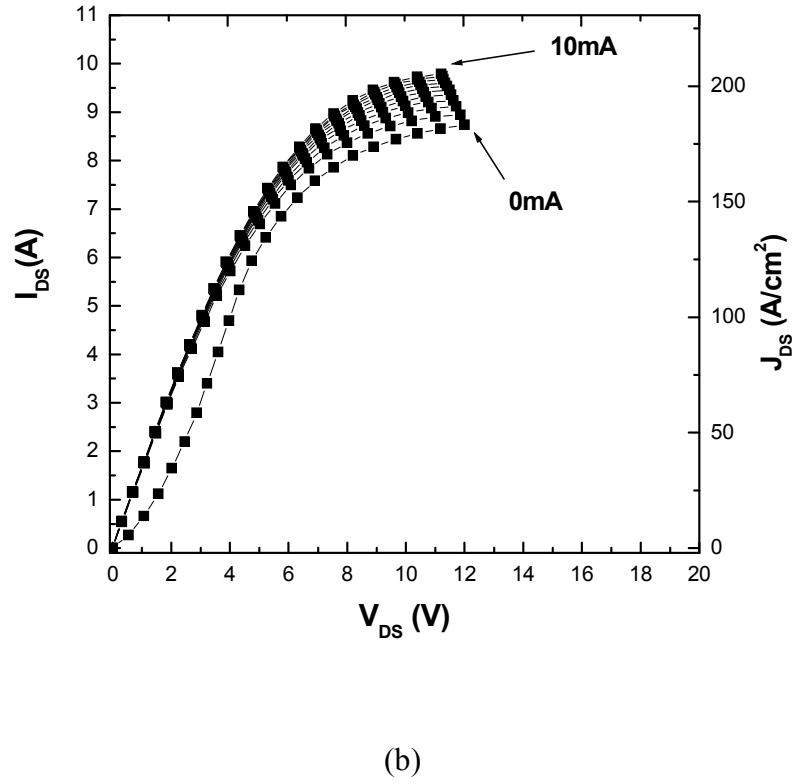
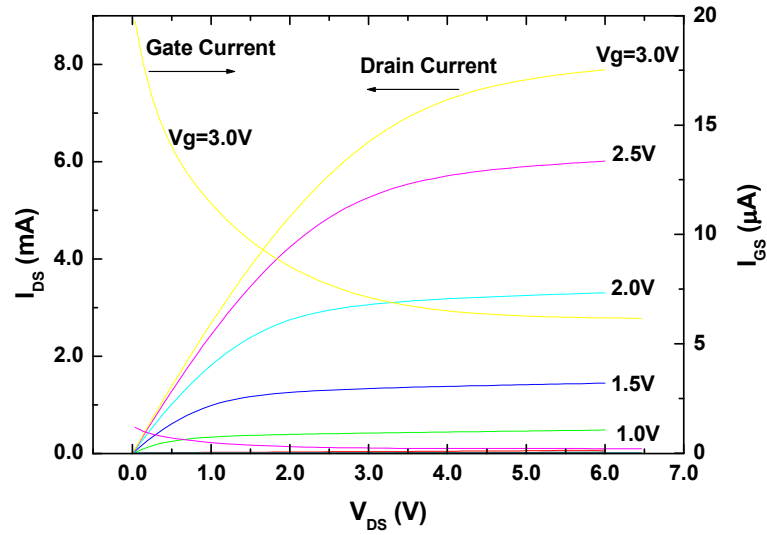


Fig. 4.10 Forward I-V characteristics of the co-packaged HV VC-LJFET: three large power JFETs in parallel, (a) voltage mode, (b) current mode.

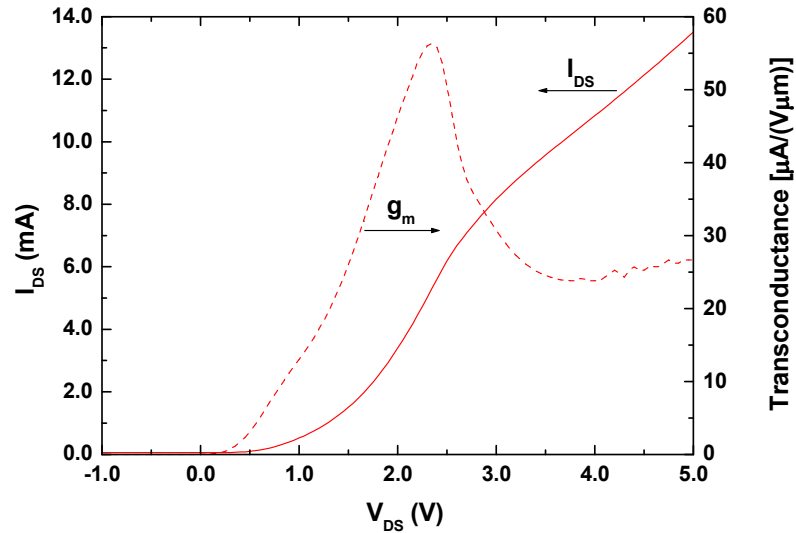
4.1.4 LV VC-LJFET

Multiple low voltage VC-LJFETs have been selected across the sample for the output and transfer characterizations. Fig. 4.11 (a) and (b) show a typical output and transfer curve respectively. Gate current is also measured at corresponding V_{GS} . As shown in Fig. 3.15 (a), a DG current ratio of 243 is still achieved when $V_{GS} = 3$ V and $V_{DS} = 1$ V. The transfer curve is measured at a constant $V_{DS} = 8$ V forcing the JFET working in the saturation region while V_{GS} scanning from -3 V to 5 V. Fig. 3.15 (b) also plots the

normalized transconductance as a function of the gate voltage, which is the derivative of the transfer curve. The peak transconductance is $56 \mu\text{A}/(\text{V}\cdot\mu\text{m})$ at V_{GS} of 2.35 V.



(a)



(b)

Fig. 4.11 DC characteristics of a LV VC-LJFET T1: (a) output curve; (b) transfer curve.

To investigate the effect of channel opening on the threshold voltage and specific on-resistance of the LV VC-LJFET, devices have been mapped across the sample. The specific on-resistances of LV LJFET T2 at room temperature, measured at $V_{DS} = 1$ V and $V_{GS} = 3$ V, are plotted against threshold voltage in Fig. 4.12. Clearly, as expected, a narrower channel opening leads to a high threshold voltage as well as a high device resistance while the device will become normally-on if the channel is too wide. R_{DS-ON} is composed of two parts of resistance, i.e. channel resistance and drift resistance. The channel resistance is controlled by the gate overdrive voltage and can be well predicted by the classic double-gate JFET theory [57]. The drift resistance (R_{Drift}) is a constant resistance resulting from the lateral drift region. Therefore the total specific on-resistance of VC-LJFET can be predicted by equation below,

$$R_{DS-ON,SP} = R_{Drift,SP} + V_{DS} \left(3 \frac{L_{CH}W}{\mu_n} \right) \left(\frac{1}{\sqrt{2qn\epsilon_s}} \right) (V_{bi} - V_{TH})^{-3/2} [3(u_2^2 - u_1^2) - 2(u_2^3 - u_1^3)],$$

where W is the unit cell length (15.25 μm for the LV JFET), u_1 and u_2 are given by Eq. 4.3 and 4.4 respectively, V_{bi} is determined by the n-channel and p-Gate doping to be 3.02 V, and V_{GS} is assumed to be 2.75 V for the direct junction voltage drop instead of the applied Gate voltage of 3 V. A curve for $R_{DS-ON, SP}$ vs. V_{TH} is plotted in Fig. 4.12 that shows a good agreement between the model and the measured data, where the $R_{Drift,SP}$ is fitted to be $3.11 \text{ m}\Omega\cdot\text{cm}^2$.

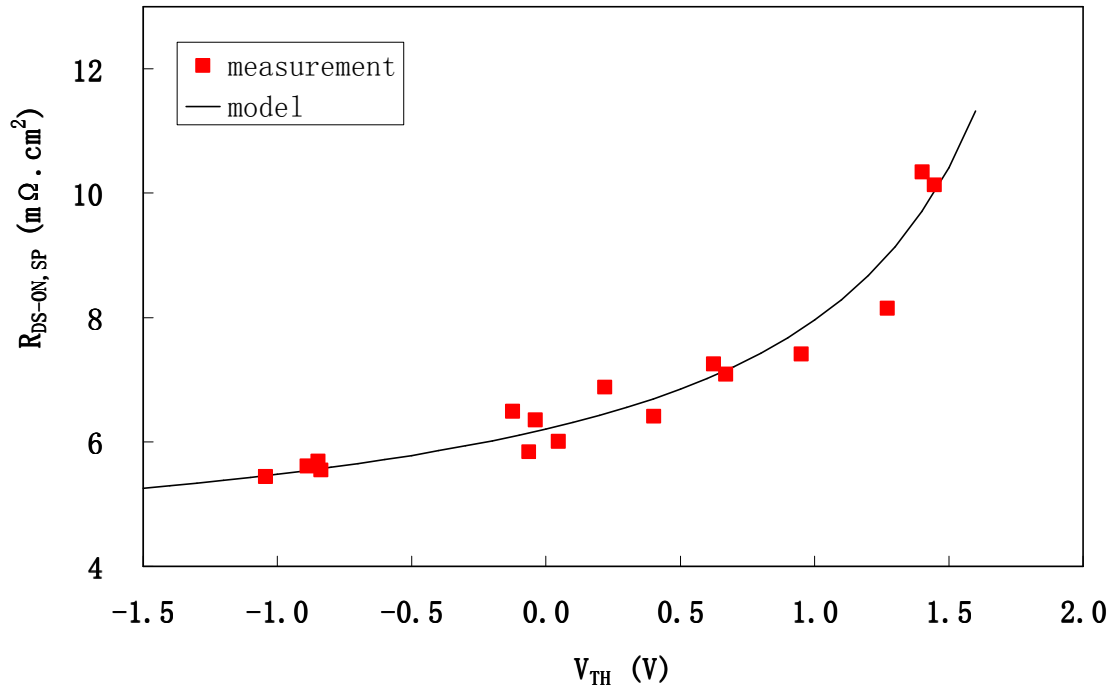


Fig. 4.12 Specific-on resistance vs. threshold voltage for LV VC-LJFETs. Symbol: measurement, line: model.

In order to obtain the channel length modulation coefficient λ and the output resistance of the JFET, the output I-V curves are measured up to 50 V for LVJFET T1 ($1.60 \times 10^{-5} \text{ cm}^2$), as shown in Fig. 4.13. All measured LVJFETs show a similar I_{DS} step around $V_{DS} = 32 \text{ V}$ that has not been reported in any devices. One possible explanation for this is that the lateral channel below the lateral p-gate is pinched off around $V_{DS} = 32 \text{ V}$, relieving the pinch-off of the vertical channel and leading to an increase in the drain current.

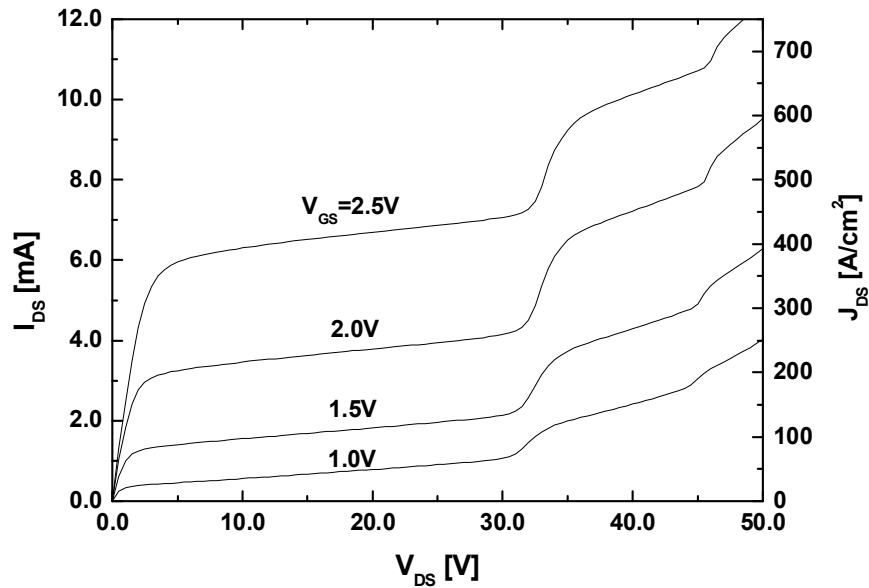


Fig. 4.13 Output I-V curves of LVJFET T1.

Temperature dependence of the LV VC-LJFET is characterized by transfer I-V curves with the variation of V_{GS} from -3 V to 5 V and a constant V_{DS} of 8V to force the saturation of devices. Some evidences of channel conductivity modulation have been observed [93]. The zero temperature coefficient (ZTC), an important device parameter for high temperature FET circuits design, is observed at the drain current of 3.4 mA corresponding to the current density of 21 A/cm² when $V_{DS} = 1.1$ V. Fig. 4.14 shows the transconductance of the LVJFET T2 versus V_{GS} at different temperatures. It should be noted that the transconductance has been normalized to a unit device width. Similar temperature dependence of threshold voltages for both LV and HV JFETs are also demonstrated [93].

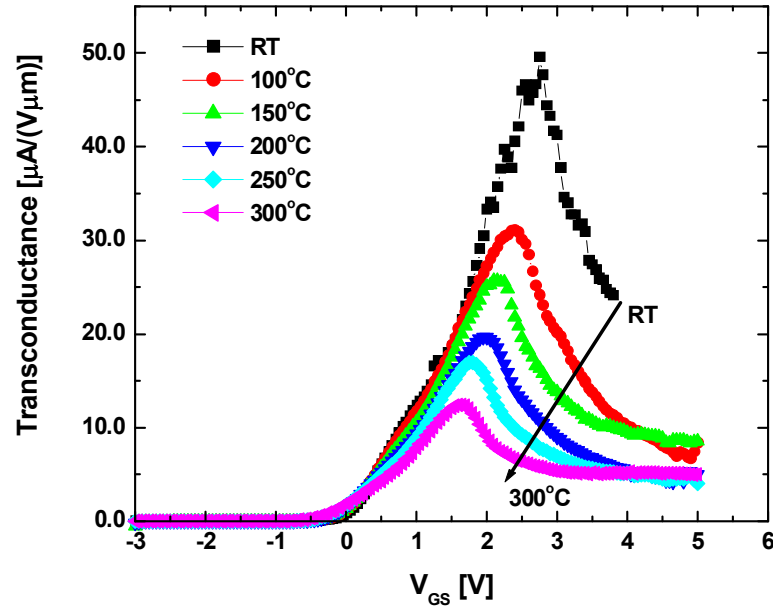


Fig. 4.14 Temperature dependence of the transconductance of LV VC-LJFET T2.

4.1.5 Resistor

The resistances of the test resistor RT1 and RT2 are measured at room temperature across the whole sample. The less than 20% variation of resistance is achieved. The total 17 samples are measured for RT1 and RT2 respectively with the results of $RT1 = 2288 \pm 326 \, \Omega$ and $RT2 = 227 \pm 41 \, \Omega$. Stable operation of the load resistor at a power density of a few thousand watts per cm^2 has been observed at ambient. The temperature dependences of RT1 and the extracted electron mobility are plotted in Fig. 4.15. The resistors are formed on the channel layer ($5 \times 10^{16} \text{ cm}^{-3}$, $0.7 \, \mu\text{m}$) and the drift layer ($1 \times 10^{17} \text{ cm}^{-3}$, $1.0 \, \mu\text{m}$). The extracted mobility from the resistance varies from $498 \text{ cm}^2 / \text{V-s}$ at room temperature to $103 \text{ cm}^2 / \text{V-s}$ at $300 \, ^\circ\text{C}$ with the consideration of the temperature

effect on the ionization of nitrogen in 4H-SiC. The temperature dependence of the extracted mobility can be best fitted to $T^{-2.3}$, as shown in Fig. 4.15.

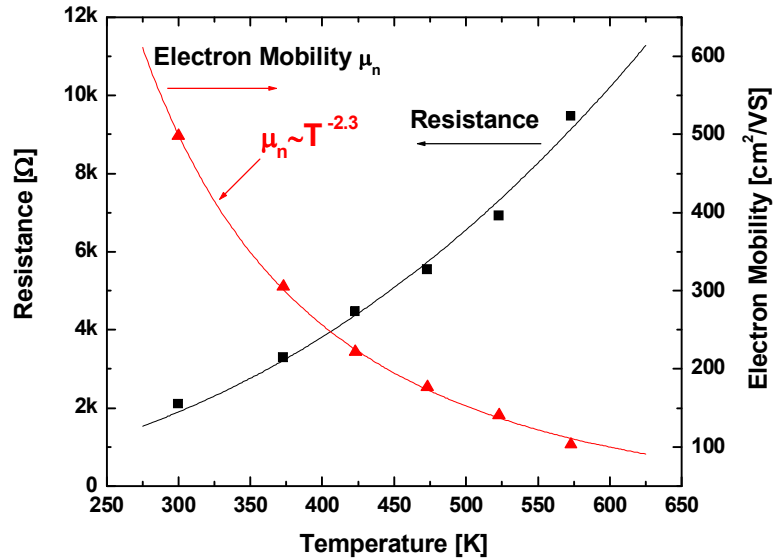


Fig. 4.15 Temperature dependences of n-type SiC resistance and the corresponding electron mobility.

4.1.6 Discussion

4.1.6.1 Temperature Dependence of Threshold Voltage

Because of the challenging submicron channel control, the threshold voltages extracted from the transfer I-V curves are scattered from -0.6 V to 1.5 V. However, the threshold voltages of different type JFETs within one block show the variation less than 0.5 V, which indicates good local mesa uniformity. The three types of HV VC-LJFETs with 0.15 μm difference at mask level yield an average V_{TH} difference of 1.4 V. Since the three HV JFETs are grouped together, the local uniformity of mesas is verified by the

consistent V_{TH} difference among the three JFETs. It is also worth noting that, compared with the planar device technologies, the VC-LJFET offers circuit designers a unique benefit that multiple devices with different threshold voltages can be conveniently applied in the circuit design. The threshold voltages as a function of temperature are plotted in Fig. 4.16. Results from three types of devices show consistent threshold voltage dependence on temperature between 1.6 mV/K and 2 mV/K. Such a consistency resulting from the identical channel structures reflects the more robust characteristics of the VC-LJFET technology as compared to the SiC CMOS approach [80]. The temperature dependence of $R_{ON,SP}$ for HV VC-LJFETs follows similar tendency of SiC resistors.

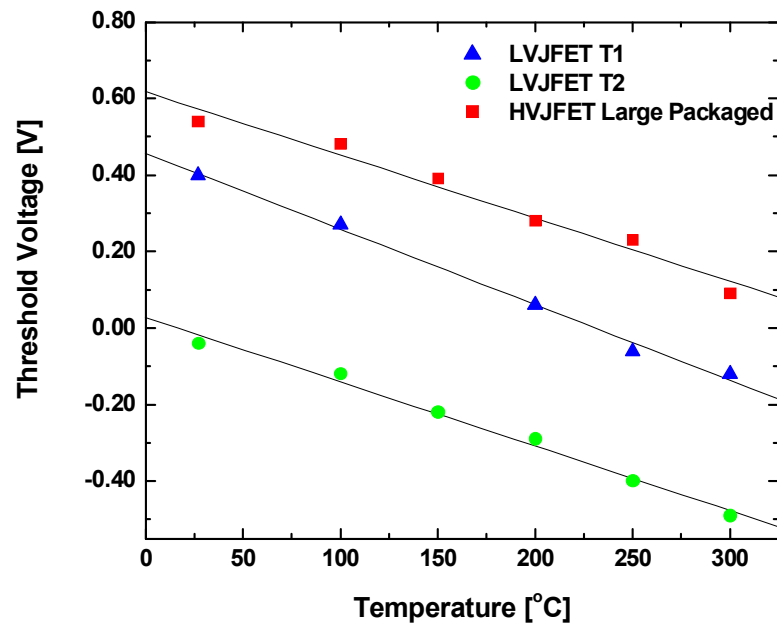


Fig. 4.16 Temperature dependence of threshold voltage: from PWIC-1PR.

4.1.6.2 Specific On-Resistance Analysis

The specific on-resistance of power FETs includes drift region, channel region, ohmic contact, and metallization resistance. As illustrated in Fig. 2.2, the VC-LJFET has a lateral channel region below the p-Gate, which also contributes to the total on-resistance since its length is comparable with the drift length. The total specific on-resistance of the VC-LJFET can be estimated and shown below. The electron mobility of $480 \text{ cm}^2/\text{Vs}$ in 4H-SiC for the n-dopings of $1 \times 10^{17} \text{ cm}^{-3}$ and $5 \times 10^{16} \text{ cm}^{-3}$ are used and we assume 100% ionization of N dopants. The ratio of vertical channel length versus channel width is fixed at 5. Z is the device unit cell width that is equal to the active area (A) divided by the unit cell width (U).

(1) Vertical Channel Resistance

$$n = 5 \times 10^{16} \text{ cm}^{-3}, \rho = 0.26 \Omega \cdot \text{cm}$$

$$R_{CH} = \rho \frac{L_{CH} / W_{CH}}{2Z} = \frac{0.65}{Z} (\Omega), \text{ where 2 is due to the effect of two mesas in parallel.}$$

(2) Drift Region and Lateral Channel Region Resistance

$$n = 1 \times 10^{17} \text{ cm}^{-3}, \rho = 0.13 \Omega \cdot \text{cm}, t = 1 \mu\text{m} \text{ is the drift layer thickness, } L_{drift} = 9 \mu\text{m},$$

$L_{LC} = 6 \mu\text{m}$ is the lateral channel region length which assumes to be the average effect of the two mesas.

$$R_{drift_LC} = \rho \frac{(L_{drift} + L_{LC}) / t}{Z} = \frac{1.95}{Z} (\Omega)$$

(3) Ohmic Contact Resistance

$$R_{C,SP} = 5 \times 10^{-5} \Omega \cdot \text{cm}^2 = 0.05 \text{ m}\Omega \cdot \text{cm}^2 \text{ is assumed to be the ohmic contact resistance of}$$

Ni silicide to etched and/or implanted n+ 4H-SiC.

$$R_{Cont} = \frac{0.05m}{Z \times 2.4\mu m} + \frac{0.05m}{Z \times 1.5\mu m}$$

$$= \frac{0.208}{Z} + \frac{0.333}{Z} (\Omega)$$

where the first item denotes the Source contact and the second item indicates the Drain contact, and Z is in centimeter.

(4) Specific On-Resistance

$$R_{ON,SP} = (R_{CH} + R_{drift_LC} + R_{Cont}) \cdot A = \left(\frac{0.65}{Z} + \frac{1.95}{Z} + \frac{0.208}{Z} + \frac{0.333}{Z} \right) (Z \cdot U) (\Omega).$$

As for the HV VC-LJFET,

$$R_{ON,SP}(HV) = \left(\frac{0.65}{Z} + \frac{1.95}{Z} + \frac{0.208}{Z} + \frac{0.333}{Z} \right) (Z \cdot 21.25\mu m)$$

$$= 1.38 + 4.144 + 0.442 + 0.708 = 6.674 (m\Omega \cdot cm^2)$$

where vertical channel takes 21%, and ohmic contact resistance contributes 17%.

As for LV VC-LJFET,

$$R_{ON,SP}(LV) = \left(\frac{0.65}{Z} + \frac{1.17}{Z} + \frac{0.208}{Z} + \frac{0.333}{Z} \right) (Z \cdot 15.25\mu m)$$

$$= 0.991 + 1.784 + 0.317 + 0.508 = 3.60 (m\Omega \cdot cm^2)$$

where vertical channel takes 28%, and ohmic contact resistance contributes 23%.

It is expected that the vertical channel and ohmic contact resistance constitute a higher percentage of the total resistance for the HV FET than that of the LV FET. It is worth noting that the spreading resistance of metallization will be discussed in chapter 5.2.

Table 4.2 shows the specific on-resistance summary of a Block D region and the specific on-resistances of several packaged HV LJFETs are also listed as comparison. The on-resistances are measured at the Gate voltage of 3 V and the Drain voltage of 1 V except otherwise commented in the table. The $0.93 \text{ m}\Omega \cdot \text{cm}^2$ smaller specific on-

resistance of the 4d-mesa HV FET than the M-mesa FET is due to the four mesas included in the unit cell instead of two in the standardized FETs, which reduces the vertical channel resistance. The $0.66 \text{ m}\Omega\cdot\text{cm}^2$ larger specific on-resistance of the medium size power FET than the small M-mesa FET is partially from the spreading resistance of metallization when device area scales up. This conclusion is further justified by comparing specific on-resistances between the medium power FET (Block C and D) and the large power FET (Block A and B). Of course the larger device area results in higher channel resistance because of the variation of channel width across the large device area, as discussed in section 4.1.4.1 and 4.1.4.

Table 4.2 Specific on-resistances of different VC-LJFETs from sample PWIC-1PR

1PR Dv8h4	R_{ON} (Ω)	Active Area (cm^2)	R_{On,SP} ($\text{m}\Omega\cdot\text{cm}^2$)	Comment
HVJFET 4d mesa	107.6	8.37E-05	9.01	
HVJFET L mesa (+0.15μm)	66.1	1.53E-04	10.11	V _g = 2V, V _{ds} = 1V
HVJFET M mesa (0.0 μm)	65.0	1.53E-04	9.94	
HVJFET S mesa (-0.15μm)	83.1	1.53E-04	12.72	
HVJFET Block D (medium)	2.64	4.01E-03	10.60	V _g = 3.5V
LVJFET T1	372	1.60E-05	5.93	
LVJFET T2	36.9	1.63E-04	6.01	
HVJFET Block AB (Large)	0.899	1.59E-02	14.29	Bv2h9 V _g = 3.5V
	0.838	1.59E-02	13.33	Av2h9 V _g = 3.5V
	0.786	1.59E-02	12.49	Av5h7 V _g = 3.5V
	0.777	1.59E-02	12.35	Av5h5 V _g = 3.5V

By comparing specific on-resistances between HV and LV VC-LJFETs, the resistivity of the drift region can be calculated. Since the drift length difference is 6 μm between HV and LV devices, the resistance of the 6 μm drift region can be calculated by

$$R_{ON}(6\mu m) = \frac{R_{ON,SP}(HV)}{Z \cdot 21.25\mu m} - \frac{R_{ON,SP}(LV)}{Z \cdot 15.25\mu m} = \frac{10m\Omega \cdot cm^2}{Z \cdot 21.25\mu m} - \frac{6m\Omega \cdot cm^2}{Z \cdot 15.25\mu m} = \frac{0.771}{Z}(\Omega).$$

And because $R_{ON}(6\mu m) = \rho \frac{6\mu m / t}{Z}(\Omega)$, ρ is calculated to be $0.1286 \Omega \cdot cm$ which is very close to $0.13 \Omega \cdot cm$ estimated by assuming the electron mobility of $480 cm^2/Vs$ and the n-doping of $1 \times 10^{17} cm^{-3}$. However, the $9.94 m\Omega \cdot cm^2$ of $R_{ON,SP}$ for the HV FET is still around 50% higher than the estimated value of $6.67 m\Omega \cdot cm^2$. The extra $R_{ON,SP}$ could be resulted from the ohmic contact resistance and the over-estimated vertical-channel electron mobility.

4.2 Temperature Sensing Diode

4.2.1 SiC P-i-N diode calibration for temperature sensing

Electronic device junction temperature is a key device parameter that can be used to characterize the thermal resistances and impedances of junction-to-case, junction-to-heatsink and junction-to-ambient for packaged power devices or high density IC chips [94]. In addition, the temperature sensing technology can be applied for the overheating protection of smart power ICs. For chips without encapsulation infrared or other sensing techniques could be applied to measure the junction temperature directly. However, such direct junction temperature measurements cannot be applied to the packaged chips. Instead, an electrical measurement method that uses pre-calibrated temperature sensitive parameters (TSPs) as an indirect temperature indicator was used. TSPs for silicon semiconductor devices have been fully developed and some different TSPs such as forward junction voltage drop, reverse leakage current of junction, transistor saturation voltage or gate turn on voltage etc. have previously been used in experimental measurements [95, 96]. The forward voltage drop is widely used for electrical junction temperature measurement of a chip with an integrated diode. For a Si diode, the sensing temperature range is limited by its narrow bandgap. In contrast, SiC diode can be used to monitor a much larger temperature scope. Therefore, the testing diode on the power IC chip can serve as a temperature sensor to monitor the actual chip temperature during the high power, high frequency switching operation. Preliminary results are presented on a packaged SiC P-i-N diode.

As shown in Fig. 4.17, the junction temperature calibration was carried out by the combination of a Tektronix 371A high current curve tracer, a Delta 9039 temperature

chamber and a temperature meter. With the environment (Delta 9039) temperature setting changed from 50 °C to 250°C at increments of 10°C, the device I-V curve and actual device temperature are recorded by the Tektronix 371A and the temperature meter. At each temperature setting, measurement results are taken after a thermal stabilization time of 10 minutes. Device self-heating during measurement is negligible since the pulse duration of Tektronix 371A is only 250µs and the current is measured only up to 2.5 A or 62.5 A/cm². Hence the case temperature read by the thermal couple should be representative of the real junction temperature. Fig. 4.18 lists some of forward I-V curves of the packaged SiC P-i-N diode at different temperatures.

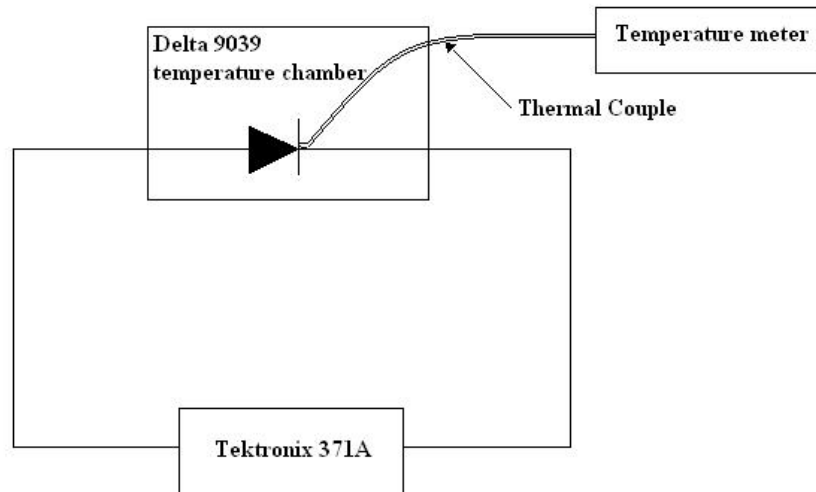


Fig. 4.17 Junction temperature calibration setup for a diode in package.

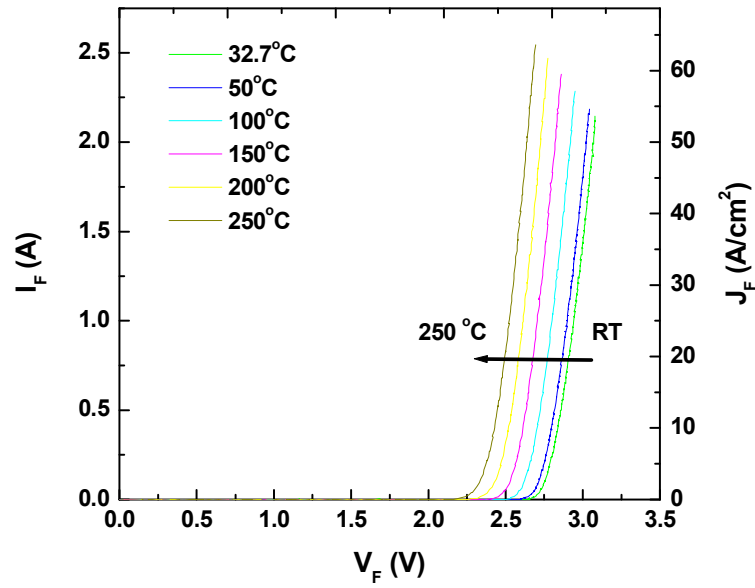


Fig. 4.18 Forward I-V performance of a packaged SiC diode at different temperatures.

The results of calibration are shown in Fig. 4.19 where the forward voltages of the P-i-N diode are plotted against the device junction temperature at different current levels. For a given current, the p-n junction forward voltage decreases linearly with the increase of junction temperature. The relationship between the forward voltage (V_j) and the junction temperature (T_j) can be fitted by the equation below [94]:

$$V_j = V_0 + T_j \times \text{slope}$$

where the slope and V_0 can be obtained by the linear fitting of V_j vs. T_j from the group of I-V curves recorded at different temperature. Very good linearity is achieved in the Fig. 4.17 indicating the excellent temperature sensing capability of SiC p-n junctions.

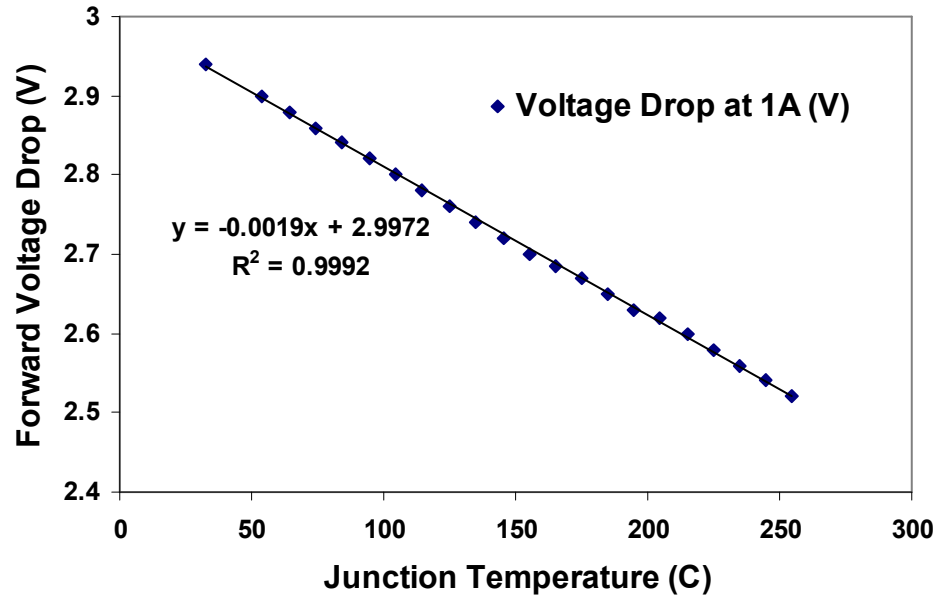


Fig. 4.19 Temperature calibration of a SiC PiN diode: forward voltage drop versus junction temperature.

4.2.2 Temperature Calibration for the SiC p-n Junctions

The Gate and Drain pads of two small power FETs in separate packages have been electrically connected to pins of power IC chip packages by wire bonding. The temperature calibrations were carried out by following the procedures in previous section, where the HP4145B replaced the Tectronix 371A since the junction area is much smaller than the P-i-N diode shown previously. Table 4.2 (a) and (b) show the calibration results for the two G-D junctions. Four different sensing current levels, 10 μA , 50 μA , 100 μA , and 500 μA , were used for the temperature measurement. The reason for the more than 3 mV/ $^{\circ}\text{C}$ of voltage drop rate for the 1PR-m G-D junction is not clear yet. However, the package 1PR-m which contains a large power JFET has demonstrated high temperature switching driven by the external MOS gate driver. The device junction temperature was

sensed by the G-D junction forward voltage drop to be 235 °C with a heat sink temperature of 219 °C when the device was switching at 2 MHz, 200 V, and 1.15 A.

Table 4.3 The calibration results for the junction temperature sensing parameters

Table 4.3 (a) G-D junction close to a large power JFET

1PR-m, G-D	$V_j = A + B \cdot T$		
Fixed Current	Intersect (A) (V)	Slope (B) (V/°C)	R
10uA	2.56189	-0.00345	-0.99988
50uA	2.78356	-0.00344	-0.99992
100uA	2.89645	-0.00335	-0.99984
500uA	3.23592	-0.00303	-0.99985

Table 4.3 (b) G-D junction close to a medium power JFET

1PR-e, G-D	$V_j = A + B \cdot T$		
Fixed Current	Intersect (A) (V)	Slope (B) (V/°C)	R
10uA	2.31536	-0.0022	-0.99032
50uA	2.37215	-0.00182	-0.99061
100uA	2.41524	-0.00173	-0.98999
500uA	2.56136	-0.00157	-0.98149

4.3 Circuit Characterizations

4.3.1 Digital Inverter

Two voltage transfer curves of digital inverters composed of LVJFET T1 and resistor RT1 are shown in Fig. 4.20. Proper logic function is demonstrated. Both inverters show the identical V_{OH} of 5 V and V_{OL} of 0.5 V. The condition of V_{OL} smaller than V_{TH} is the key to make the super buffer functioning. However, smaller V_{OL} requires larger load resistor and smaller $R_{DS,ON}$ of the LV JFET corresponding to a lower V_{TH} which in turn requests lower V_{OL} of pervious buffer stage. Therefore, the threshold voltage spreading and the matching of load resistors determine the functionality of the integrated super buffer.

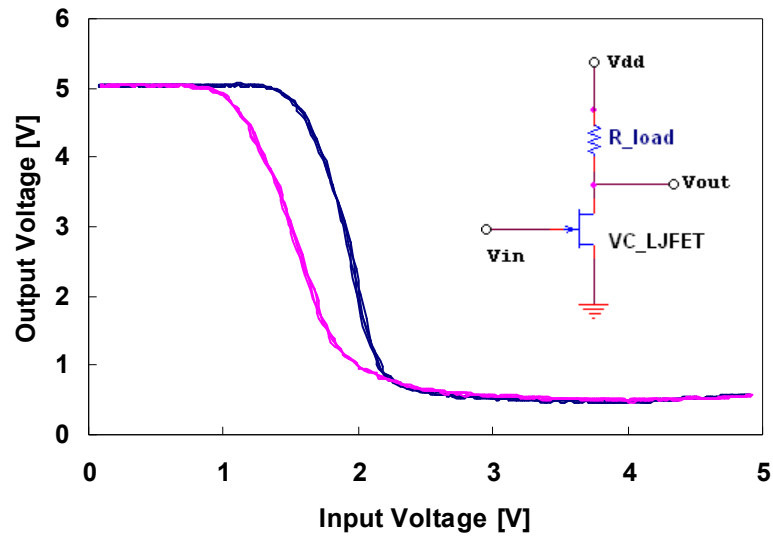


Fig. 4.20 Voltage transfer curves of two resistive load n-type VC-LJFET logic inverters.

4.3.2 Buffer

Input and output waveforms of the 4-stage super buffer are shown in Fig. 4.21. The output voltage swings between 1V and 5V, with the rise and fall times close to the detection limit of the measurement setup ($<10\text{ns}$). A delay time of around 25~35ns between the output and the input signals is attributed to the internal propagation time of the logic inverter stages.

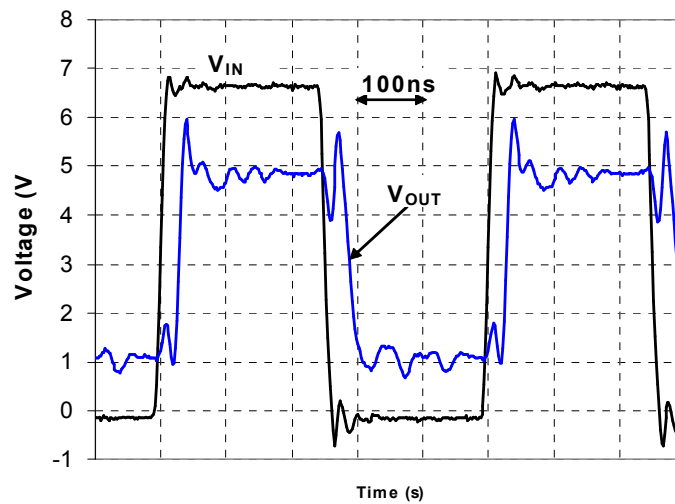


Fig. 4.21 Switching of the integrated buffer driver at 2MHz. The output voltage swings between 1V and 5V.

4.3.3 Power IC

A packaged SiC power IC composed of a medium size HV JFET and a super buffer driver demonstrates the capability of MHz switching at much higher power density than the Si PICs, as shown in Fig. 4.22 [93]. With the interface of an integrated buffer, the HV LJFET is controlled by the input signal, and demonstrates room temperature switching at the condition of 200 V, 0.4 A, and 5 MHz. The input signal has a voltage swing from -2

V to 3.6 V and a duty cycle of around 40%. The fast switching characteristics of the SiC VC-LJFET with a rise and fall time of 34 and 30 ns respectively is visualized with this input waveform present for comparison. Another packaged power IC chip, containing one large HV LJFET and two super buffers, demonstrates power switching at 3 MHz, 275 V, and a load current as high as 2 A. As shown in Fig. 4.23, the buffer output signal provides a voltage swing from -2 V to 4 V. Since power JFET has a threshold voltage near zero, a negative gate bias is needed to turn the device off quickly..

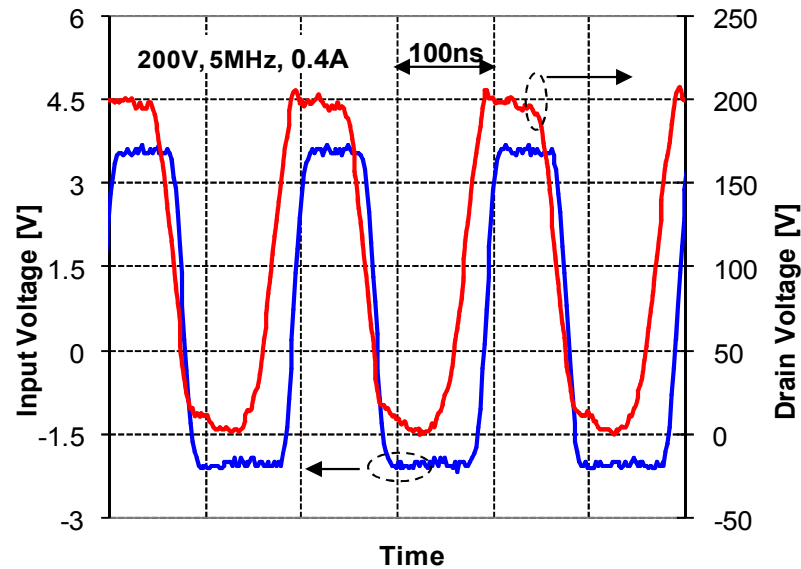


Fig. 4.22 Switching wave forms of a SiC power IC at room temperature: Medium HV LJFET, 5 MHz, 200 V and 0.4 A with a duty cycle of 40% for the input signal. The driver has a propagation delay somewhat less than 100ns.

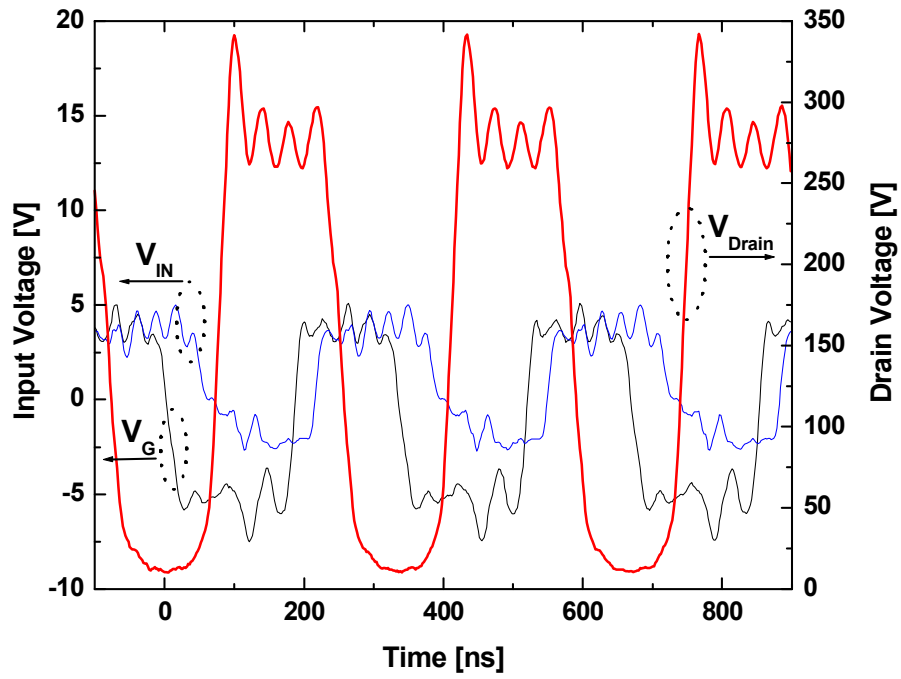


Fig. 4.23 Switching wave forms of a SiC power IC at room temperature: Large HV LJFET, 3 MHz, 275 V, and 2 A with a duty cycle of 45% for the input signal.

5. FURTHER OPTIMIZATION AND ANALYSIS

5.1 Experimental Optimization of the RESURF Structure

Because of the inefficient activation of Al ions in SiC at 1550 °C and the deviation of the TCAD model from the reality, the RESURF structure needs to be carefully optimized experimentally to gain the highest breakdown performance for the given drift length design. As stated in chapter 4, the thickness variation of PECVD SiO₂ as an implantation shielding layer could not verify the optimal dose of the top p-RESURF because of the drift length variation across the shielding regions. In this chapter, two different approaches have been proposed to optimize the RESURF structure. One approach is to etch the drift region down gradually by the “ohmic contact” mask on the small sample PWIC-1PD with the E blocks, and measure the blocking voltage on the testing diodes. Another one is to etch the drift region down by an extra “RESURF etch” mask, and test the breakdown performance of diodes as well. Meaningful results from both approaches will be discussed in the following two sections.

5.1.1 A Novel Structure to Increase the Blocking Voltage to 1.4 kV

The three types of diodes with different RESURF lengths (1 μm , 3 μm , and 4.5 μm) in block E contained in sample PWIC-1PD are used for this study. The sample 1PD was implanted and activated together with 1PR and then stopped without oxidation. The blocking performance is tested with the AlTi patterned by the ohmic contact mask, as shown in Fig. 5.1. The drift region length determined by p-Gate implantation and n+ Drain implantation is 9.5 μm at mask level. However, the drift length is shrunk to be around 7.5 μm due to the misalignment and the lateral etching of Mo mask for p-Gate implantation. The ohmic contact distance between cathode and anode is 11.5 μm at the

mask level while actual distance is around $12\text{ }\mu\text{m}$ due to the side etching of AlTi metal. A series of etch-and-test steps were carried out with etching depths between 30 nm to 55nm for each step. The AlTi metal serves as both etching mask and contact metal, and hence this self-aligned process enables fixed blocking distance between different etching steps. The average blocking voltages versus the etching depths are plotted in Fig. 5.2. At least three diodes for each type were measured to get the statistical blocking voltage shown in the figure. Apparently the diode blocking characteristics can be divided into two parts, before 200 nm and after 200 nm, depending on the etching depth.

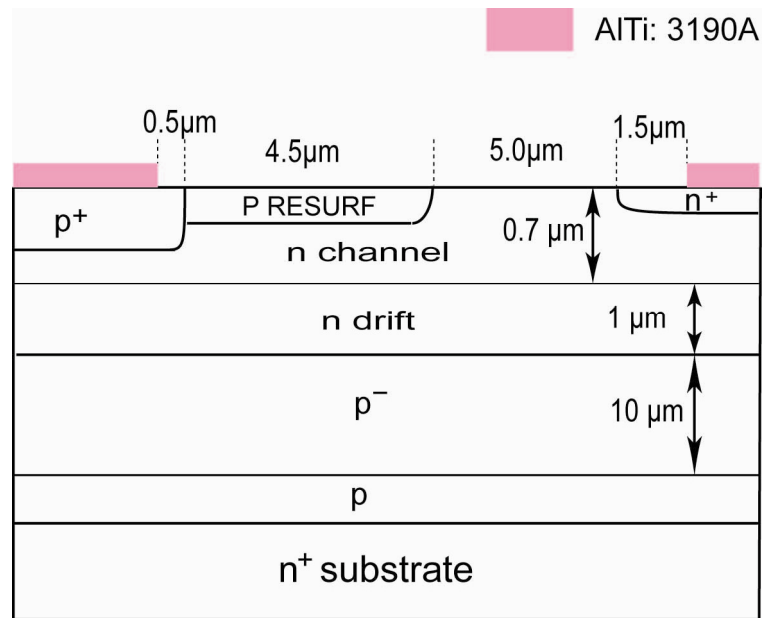


Fig. 5.1 Cross-sectional view of the 4.5- μm RESURF lateral diode with the AlTi contact metal: the lateral dimensions are from the mask design.

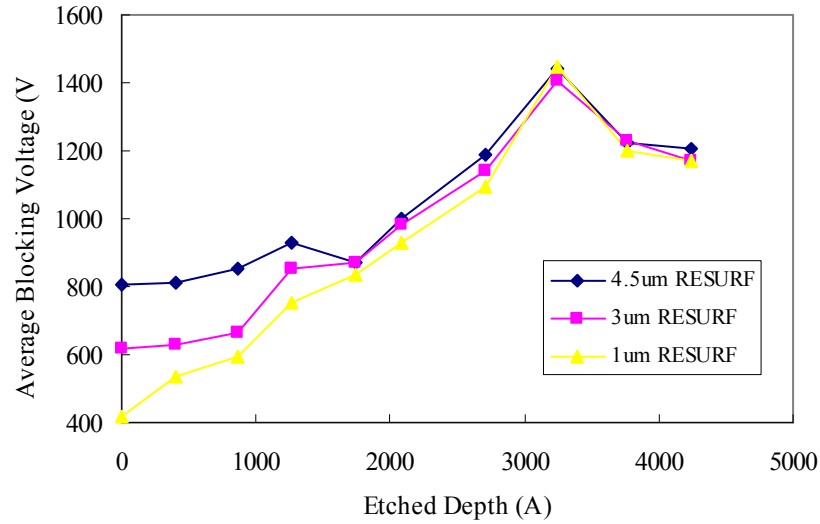


Fig. 5.2 Blocking performance of test diodes at different etching depths.

For the diodes before the etching, longer RESURF length leads to high breakdown voltage, which is consistent with the simulation results in Fig. 2.4. With the deeper etching, all diodes show the increased breakdown voltages, which indicate that the RESURF dose is getting optimized. When the etching depth reaches 1265 Å, the 4.5-μm RESURF diode blocks 927 V, and the 1-μm RESURF diode blocks 751 V with an increase of 80% as compared with the 417 V before etching. It is clear that the 4.5-μm RESURF diode achieves the optimal blocking at the depth between 1200 and 1300 Å, as shown in Fig. 5.3, since further etching reduces its breakdown voltage. The maximal blocking and optimal depths for the 3-μm and 1-μm RESURF diodes, which are expected to happen at deeper depths resulting in the lower RESURF dose, are not clearly observed. Shorter RESURF length leads to smaller optimal windows for both dose and blocking.

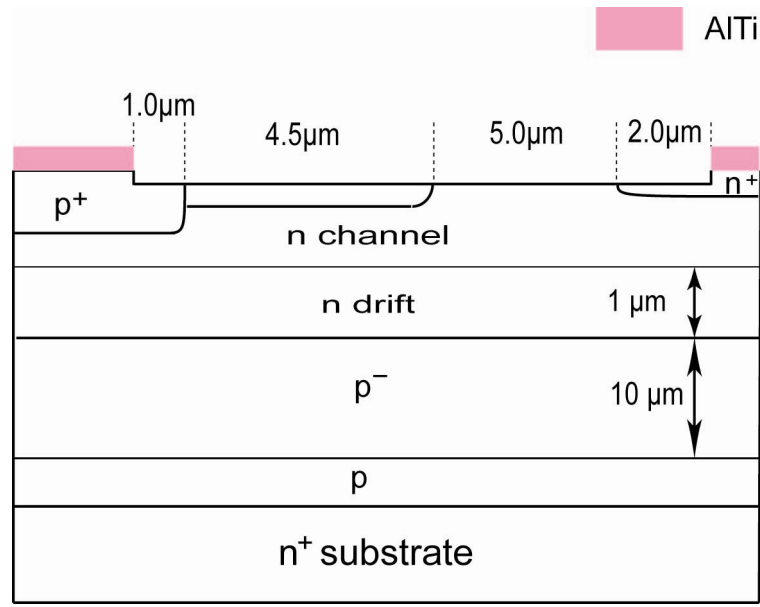


Fig. 5.3 Cross-sectional view of the 4.5- μm RESURF lateral diode with the optimal etching depth of 1265 Å: the etching window is expanded by 1 μm because of the side etching of AlTi.

When the etching depth increases to above 2000 Å, the further increase of blocking voltage for all the diodes is observed and they all achieve the average breakdown voltage larger than 1.4 kV around the depth of 3240 Å, as shown in Fig. 5.2. The nice and non-destructive breakdown I-V curves for a group of diodes at the optimized etching depth are plotted in Fig. 5.4 as well. This increasing of blocking voltages for all diodes is due to the etching away of part of n+ Drain region as illustrated in Fig. 5.3 and 5.5 which results in the 2- μm extension of drift length. The n+ Drain implantation profile in Fig. 5.6 shows the junction depth of 2500 Å. Furthermore, all three diodes show similar breakdown performance which indicates that the top p-RESURF is less effective in determining the blocking voltages and is almost removed when reaching the maximal breakdown performance. The junction depth of p-RESURF is 3500 Å, as shown in Fig. 5.7. While the top p-RESURF is gone at the highest blocking voltage, two possible top RESURF

structures, together with the bottom p-RESURF, are present after etching to achieve the optimal breakdown. The first top RESURF structure resulting from etching is the corner step around the n⁺ Drain, as shown in Fig. 5.5, which relieves the peak electrical field on the n⁺ Drain to n channel high-low junction. Another possible top RESURF structure is the remaining p-Gate region after etching, as shown in the left and up part of Fig. 5.5. The actual length of the new RESURF region is around 2 μm because of the side etching of Mo p-Gate implantation mask instead of the 1 μm illustrated in the figure. The dose in this region integrated from 3220 Å to 7000 Å is $2.58 \times 10^{14} \text{ cm}^{-2}$ which is more than 10 times of the maximal dose $1.61 \times 10^{13} \text{ cm}^{-2}$ (Q_M) discussed in chapter 2.2.2. However, considering the extremely low activation efficiency of high concentration Al ions in SiC, such as 10%, the new top p-RESURF dose is close to the optimal dose $0.95 \times 10^{13} \text{ cm}^{-2}$ or at least in the same order. If the new p-RESURF does take effect, the drift length in the Fig. 5.5 will extend to the left edge of the etching window resulting in the length of 12.5 μm , but the actual length was measured to be 13 μm for the 1450-V diodes.

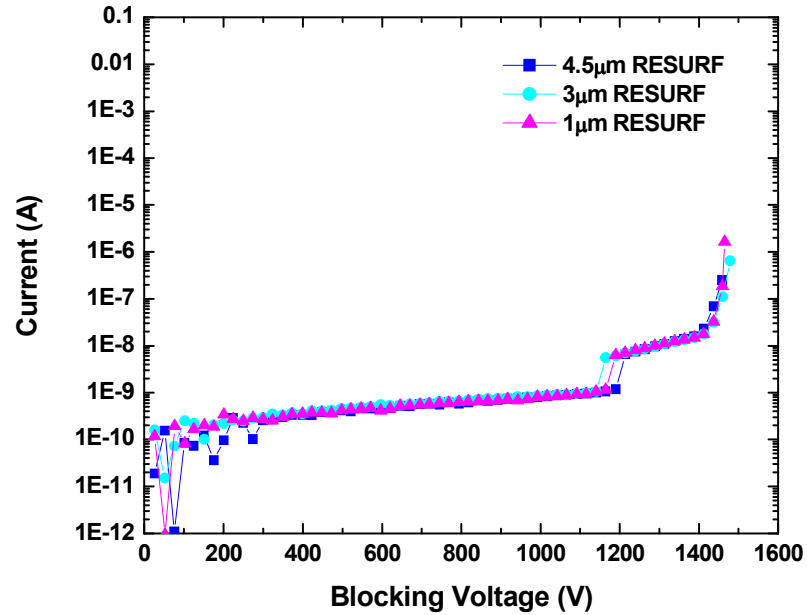


Fig. 5.4 Blocking I-V curves for a group of diodes on PWIC-1PD after the 3240-Å etching: the optimized breakdown voltages are not destructive.

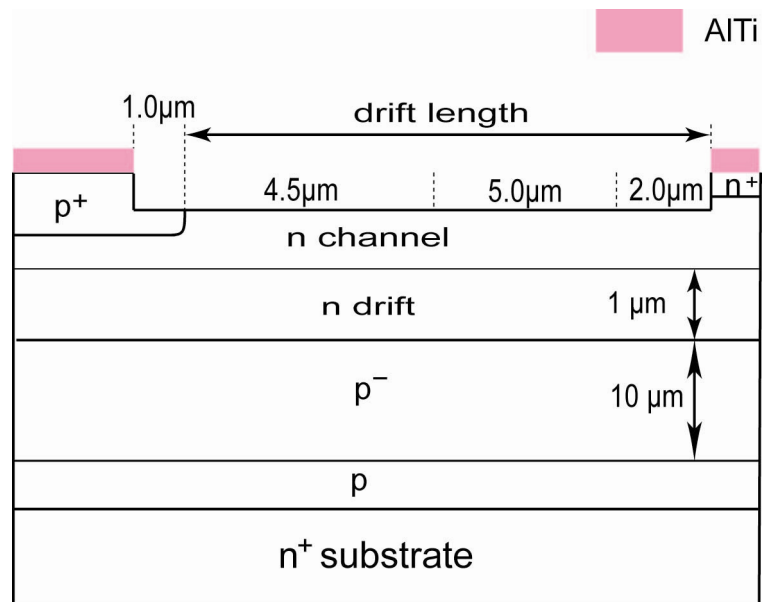


Fig. 5.5 Cross-sectional view of the lateral diode with the etching depth of 3240 Å: the top p-RESURF is almost etched completely.

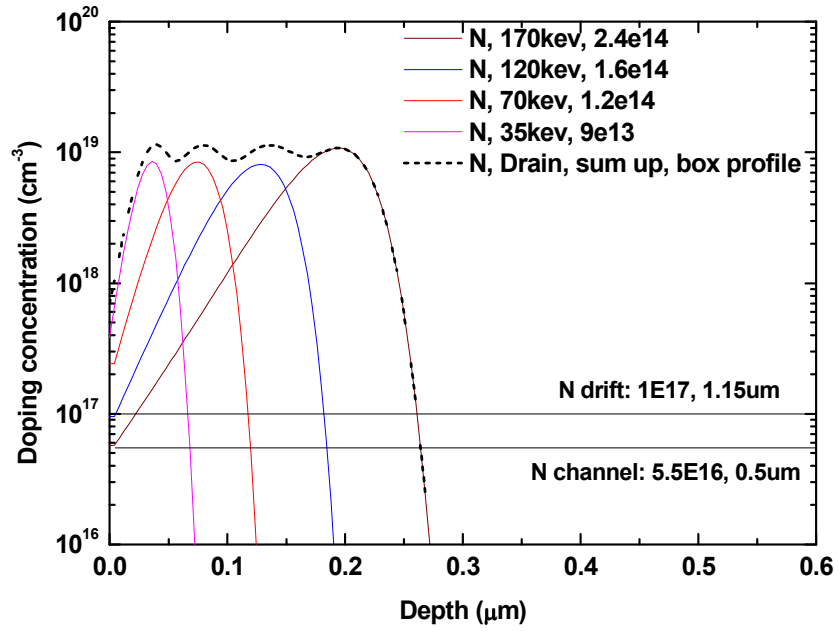


Fig. 5.6 The n+ Drain implantation profile.

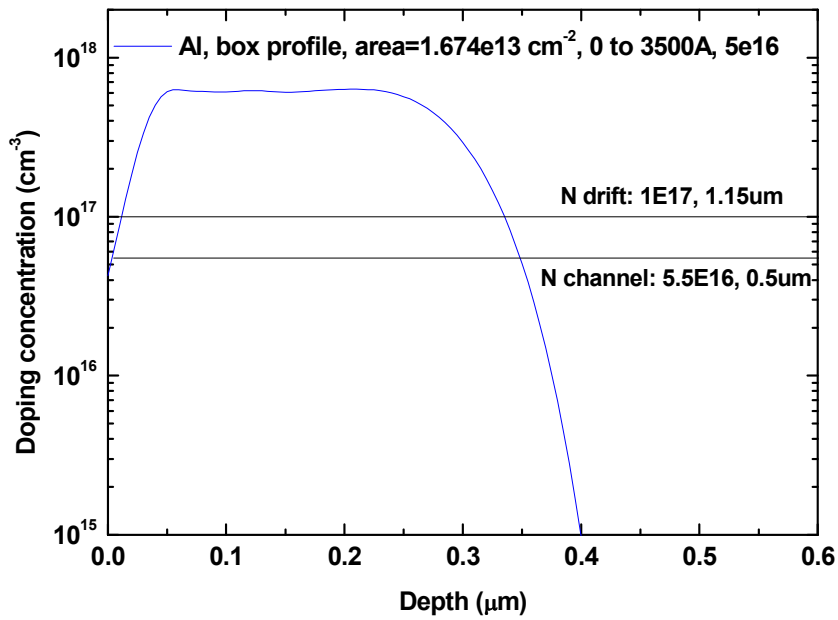


Fig. 5.7 The top p-RESURF implantation profile for PWIC-1P batch.

5.1.2 RESURF Dose Optimization to Refrain the Leakage Current

It is hard to experimentally implement the previous approach in the VC-LJFET fabrication. Therefore, a new mask to open an etching window in the drift region was designed, as shown in Fig. 5.8. Then a series of etch-and-test steps were also done on the actual sample PWIC-2PL to catch the optimal RESURF dose. The etch window opening is $6\mu\text{m}$ at mask level while the actual etch window is $7\mu\text{m}$ due to the side etching of AlTi. In addition, another layer of contact metal needs to be patterned for the blocking test after each etching step since this is not the self-aligned approach as shown in section 5.1.1.

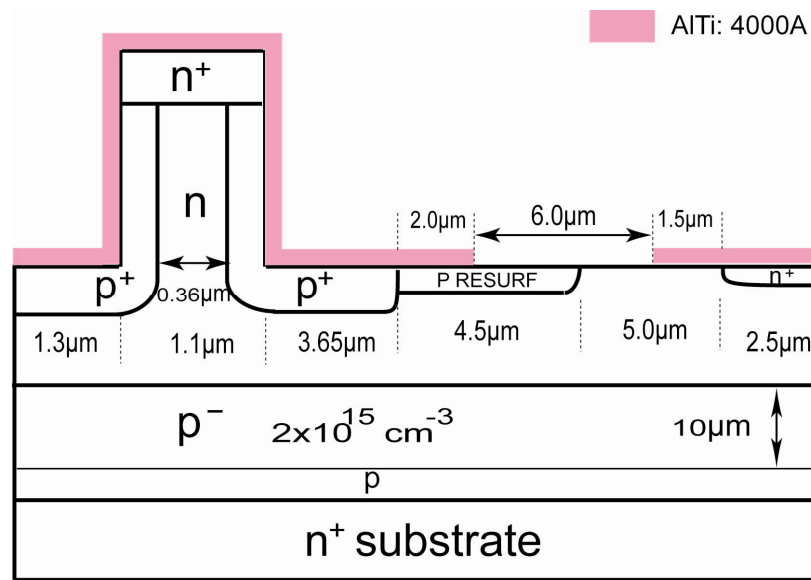


Fig. 5.8 Cross-sectional view of the VC-LJFET with an RESURF etching window: the lateral dimensions are from the mask design.

The starting RESURF dose of PWIC-2PL is designed to be higher than that of the PWIC-1P batch, as shown by the solid line in Fig. 5.9. Groups of devices including the LM, MM, SM, and 4d JFETs, and diode in each group are characterized after every

etching step. The decreased leakage current and increased breakdown voltages are generally observed. Fig. 5.10 (a) and (b) show the breakdown I-V performance of a group of test structures before and after the 4th etching with a total depth of 1500 Å. The over-dosed RESURF devices show some burning traces after blocking measurement, as shown in Fig. 5.11. The traces are exactly along the Drain and RESURF boundaries where the high electric field presents for the over-dosed RESURF design. In contrast, there are no observable measurement traces after the 4th etching, which indicates less non-uniformity of electric field distribution in the drift region. The LM, MM, and SM JFETs show lower breakdown voltages than those of both the 4d JFET and diode, which are due to the field crowding at the corner region of the VC-LJFET with a linear layout. Further etching down may reduce the leakage current and catch the optimal RESURF dose. However, some margin is left for the consumption of SiC during oxidation and the charge resided in the dielectrics.

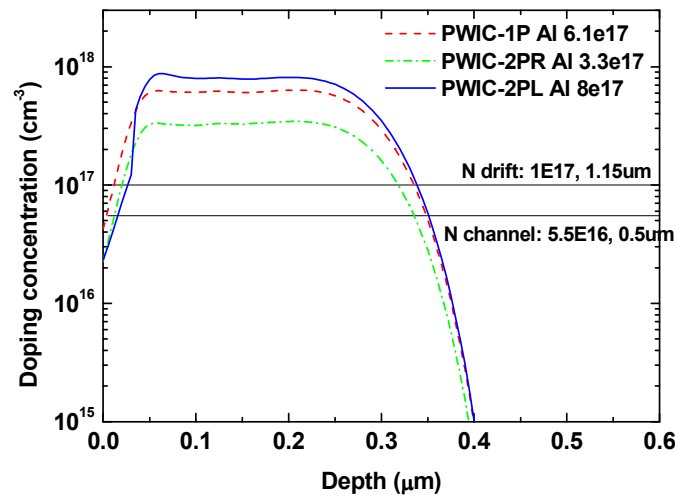
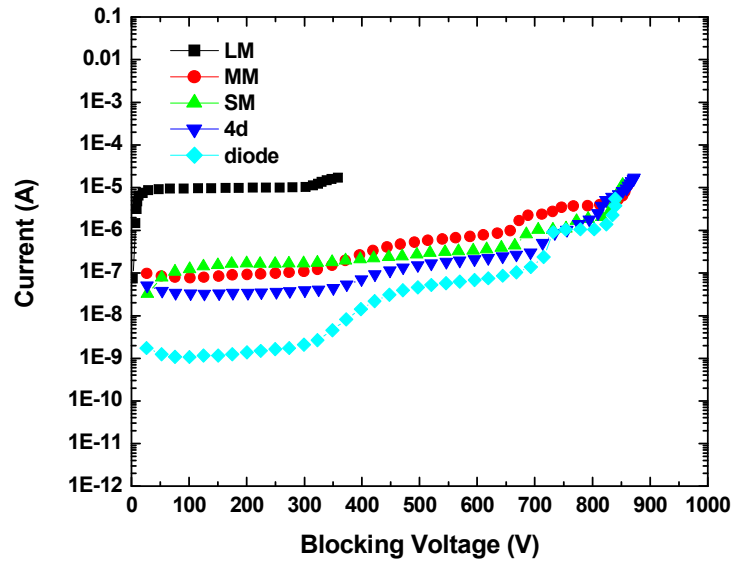
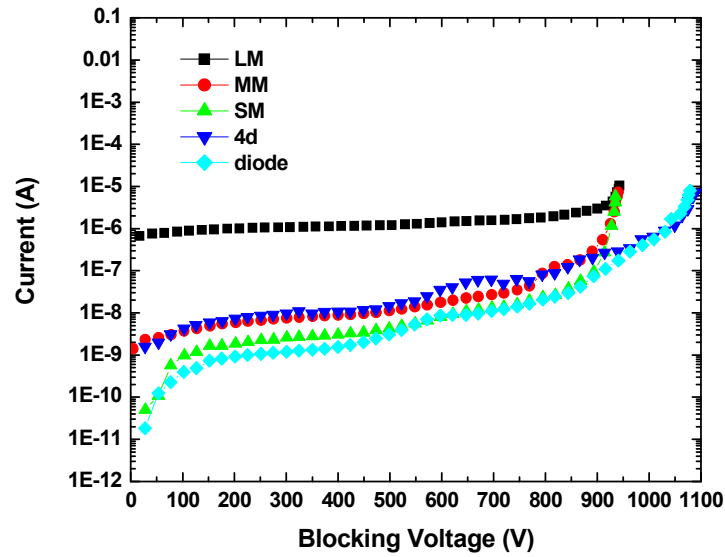


Fig. 5.9 The top p-RESURF implantation profile for PWIC batches.



(a)



(b)

Fig. 5.10 Blocking performance of a group of test structures in PWIC-2PL: (a) before etching; (b) after 4th etching with a total depth of 1500 Å.

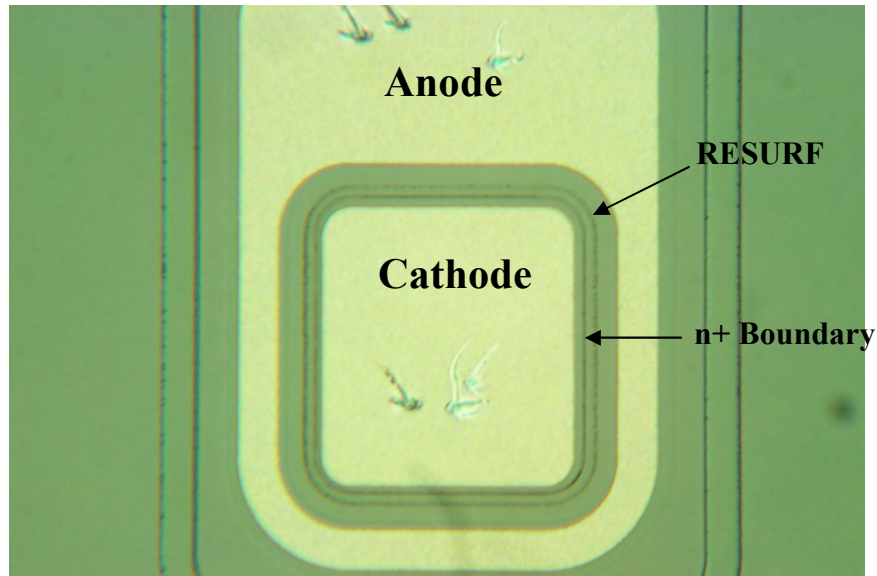


Fig. 5.11 Optical photo of a lateral diode on PWIC-2PL with the over-dosed RESURF: the traces appeared as a result of electrical burning after the blocking measurement.

The breakdown voltages of the exactly same group of devices in Fig. 5.10 are characterized after oxidation and the ohmic contact formation, as plotted in Fig. 5.12. When compared to the case before oxidation, the leakage current is further reduced while the blocking voltage decreases a little as well. Both decreased leakage current and deteriorated breakdown indicate that the RESURF is a little bit under dosed after the ohmic contact formation since the overdosed structures have been tested before the RESURF etching. Therefore, the introduced extra charge is positive resulting in the partial compensation of the negative fixed ions in the depleted p-RESURF region. Further degradation of breakdown performance is observed after the metallization in PWIC-2PL which introduces the 2.2 μm of PECVD oxide and nitride layers to fill trenches and cover drift regions for the high temperature operation purpose. Fig. 5.13 shows the blocking performance migration of the same diode at different process stages.

The destructive breakdown after metallization is attributed to the under dose of RESURF compensated by the positive charges in the passivation dielectrics. In contrast, the PWIC-1PR batch does not show obvious blocking degradation of breakdown after metallization in which 2- μm polyimide is used to fill trenches. Apparently higher quality dielectrics with lower charges are needed to meet the high temperature operation requirement.

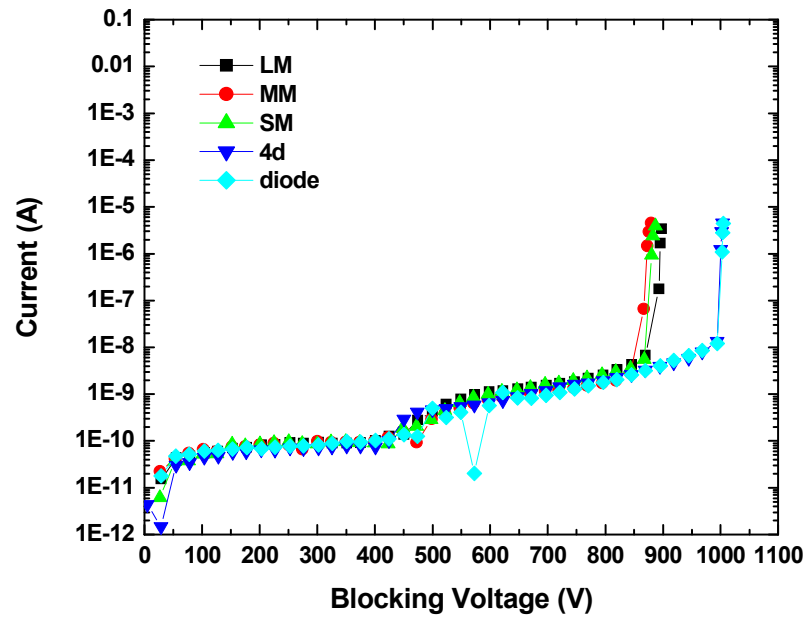


Fig. 5.12 Blocking performance of a group of test structures in PWIC-2PL after oxidation and ohmic contact formation.

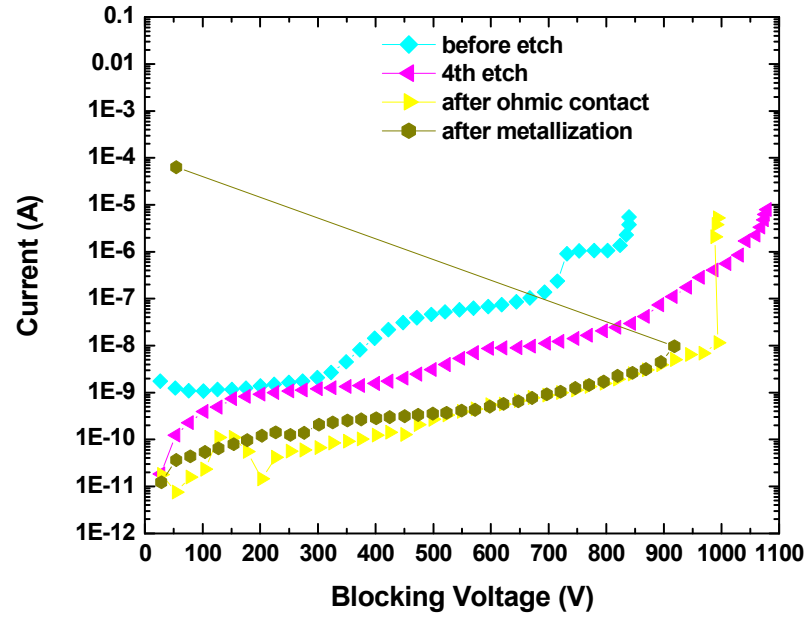


Fig. 5.13 Blocking performance of a lateral diode in PWIC-2PL at different process stages.

5.2 An Analytical Model for the Metallization Voltage Debiasing of Power Devices

The spreading resistance of metallization in the Si LDMOS technology has come into picture when the technology scales down to the submicron range [97, 98]. The voltage debiasing due to metallization could be as high as 36% for the 40-V device in the double-metal 300-m Ω switch design, where the double-metal specific resistance is around 0.299 m Ωcm^2 [98]. Because of its superior material properties, the SiC power devices rated at 1000 V have specific-on resistances in the m Ωcm^2 range where the metal spreading resistance is not negligible anymore especially for the lateral power devices. In addition, the voltage debiasing on the Base metal for BJTs, and the series resistance of Gate metal for FETs are critical in determining the overall device performance.

The resistance of metallization in the multi-metal Si technologies has been modeled as different resistance networks and implemented in the SPICE model for circuit design [97-99]. Analytical expressions for the debiasing resistors can be derived by solving Kirchoff's current law for the appropriate boundary conditions [99]. In this section, detailed modeling to calculate the debiasing resistance of metallization in the linear layout design will be presented. Two sets of differential equations have been derived based on the resistive current shunt and exponential current shunt respectively.

5.2.1 Resistive Current Shunt

As for the lateral power device with an inter-digitate linear layout design, the current flow from Drain to Source in n-type FETs is resistive or linear assuming the constant Gate bias. A simplified model shown in Fig. 5.14 is used in this study. The Source and Drain metal fingers with different metal width, W_S and W_D , are sitting on a piece of semiconductor with the drift length of L and the width of W . The metal and

semiconductor thicknesses are denoted by d_M and d_S respectively. The current flows from the Drain pad into Drain metal bus, through the drift region, into Source metal bus, and then flow out into the Source pad. The x-axis is along the finger direction and y-axis is the lateral direction. In this model, the electrical potential in the metal is assumed to only depend on the x and the perpendicular plane inside metal is equal potential. Therefore, the problem can be simplified into the 1D question.

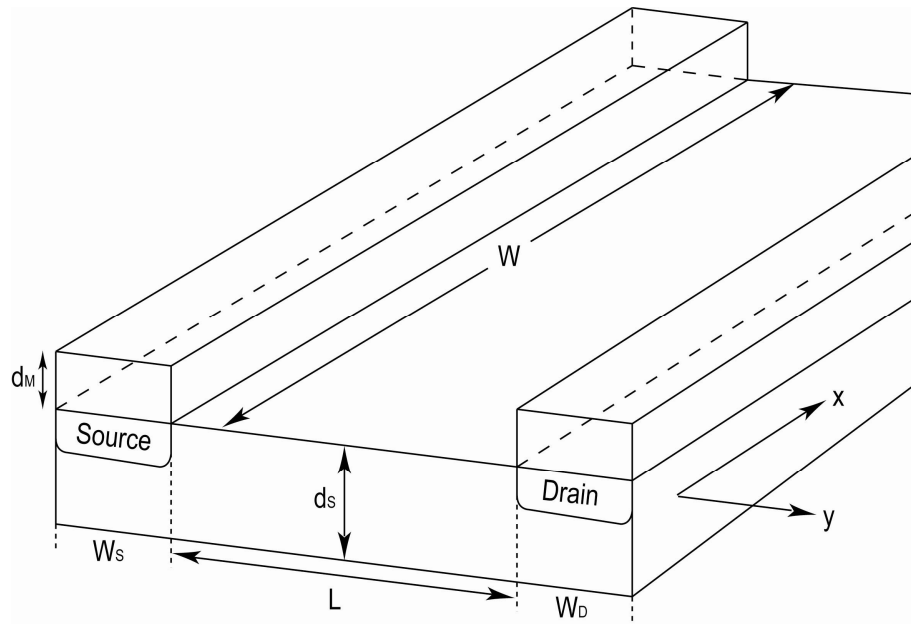


Fig. 5.14 A schematic 3D viewgraph for the simplified linear layout in lateral FETs.

Let's discuss the current flow in the Drain bus finger first. The Drain current flow, I_D , inside metal is schematically shown in Fig. 5.15(a). At each x point, the current in the metal contains two components. One flows into the semiconductor, named as I_{DS} , and another one is still the current flow in the metal. This relation is expressed by

$$I_D(x) = I_D(x + \Delta x) + I_{DS}(x). \quad (\text{Eq. 5.1})$$

By replacing the current by the current density, and considering $I_{DS} = J_{DS}d_S\Delta x$ due to the current continuity shown in Fig. 5.15 (b), Eq. 5.1 becomes

$$J_D(x)W_Dd_M = J_D(x + \Delta x)W_Dd_M + J_{DS}(x)d_S\Delta x. \quad (\text{Eq. 5.2})$$

Furthermore, Eq. 5.2 can be converted into a differential equation below

$$\frac{dJ_D(x)}{dx} + \frac{d_S}{W_Dd_M}J_{DS}(x) = 0. \quad (\text{Eq. 5.3})$$

Assuming the voltage distributions on the Drain and Source metal are $V_D(x)$ and $V_S(x)$, then we have

$$J_{DS}(x) = \frac{V_D(x) - V_S(x)}{R_S \cdot W \cdot d_S}, \quad (\text{Eq. 5.4})$$

where R_S is the drift region resistance along the lateral direction. According to Ohm's law, there is

$$J_D(x) = -\sigma_M \frac{dV_D(x)}{dx}, \quad (\text{Eq. 5.5})$$

where σ_M is the electrical conductivity of metal. By combining Eq. 5.3 to 5.5, a 2nd order differentiation for the voltage distribution along the metal finger is expressed by

$$\frac{d^2V_D(x)}{dx^2} - \frac{1}{\sigma_M \cdot R_S \cdot W \cdot W_D \cdot d_M} [V_D(x) - V_S(x)] = 0. \quad (\text{Eq. 5.6})$$

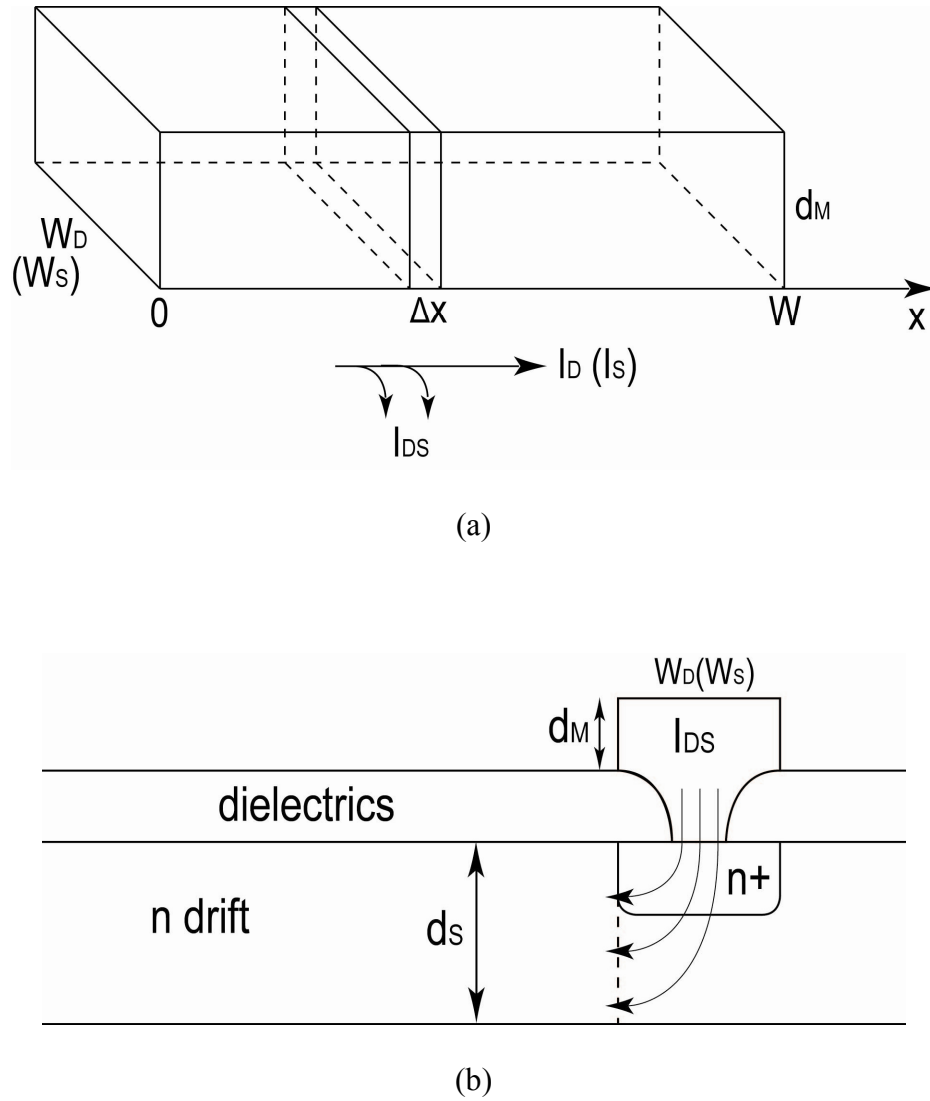


Fig. 5.15 Schematics of 1D current flow model in metal and semiconductor: (a) current flow in metal but; (b) current flow from metal into semiconductor.

Similarly, the current flow and voltage distribution in the Source metal can be modeled by

$$\frac{d^2 V_s(x)}{dx^2} + \frac{1}{\sigma_M \cdot R_S \cdot W \cdot W_S \cdot d_M} [V_D(x) - V_s(x)] = 0. \quad (\text{Eq. 5.7})$$

Let's introduce $r = \frac{R_{sh-M}}{R_{sh-S}}$ (Eq. 5.8) as the ratio between sheet resistances of metal (R_{sh-M})

and semiconductor (R_{sh-S}). Then Eq. 5.6 and 5.7 can be further simplified to be

$$\begin{cases} \frac{d^2 V_D(x)}{dx^2} - \frac{r}{L \cdot W_D} [V_D(x) - V_S(x)] = 0 \\ \frac{d^2 V_S(x)}{dx^2} + \frac{r}{L \cdot W_S} [V_D(x) - V_S(x)] = 0 \end{cases} \quad (\text{Eq. 5.9a and b})$$

As for the inter-digitate layout, the boundary conditions of Eq. 5.9 as illustrated in Fig.5.16 are expressed below

$$\text{B.C. I: } \begin{cases} V_D(0) = V_{DD} \\ V_S(W) = 0 \end{cases}, \text{ and}$$

$$\text{B.C. II: } \begin{cases} J_D(W) = 0 \\ J_S(0) = 0 \end{cases} \Rightarrow \begin{cases} \left. \frac{dV_D(x)}{dx} \right|_{x=W} = 0 \\ \left. \frac{dV_S(x)}{dx} \right|_{x=0} = 0 \end{cases}.$$

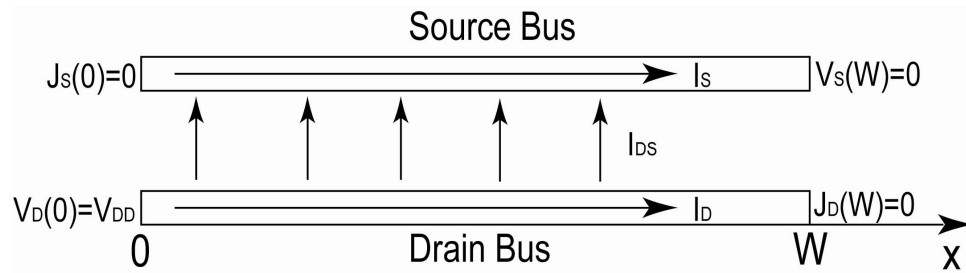


Fig. 5.16 Boundary conditions for the linear layout.

By take the actual parameters below,

$$\left. \begin{aligned} R_{sh-S} &\approx 10^3 \Omega / \square \\ R_{sh-M} &\approx 10^{-1} \Omega / \square \end{aligned} \right\} \Rightarrow r = 10^{-4},$$

$$d_s = 1 \mu m \text{ (Semiconductor thickness),}$$

$$L = 8 \mu m \text{ (Drift layer length),}$$

$$W_D = 4 \mu m \text{ (Drain metal width),}$$

$$W_S = 14.5 \mu m \text{ (Source metal width),}$$

$$W = 500 \mu m \text{ (Finger length),}$$

$$V_{DD} = 2V \text{ (Drain voltage for the on-resistance evaluation),}$$

the voltage distributions on the Drain and Source metal bus are solved in Mathematica from Eq. 5.9 and the corresponded boundary conditions. Fig. 5.17 plots the voltage distributions against distance along the metal bus fingers. It is noted that the lowest voltage drop across the drift region is 1.4 V at $x = 360 \mu m$.

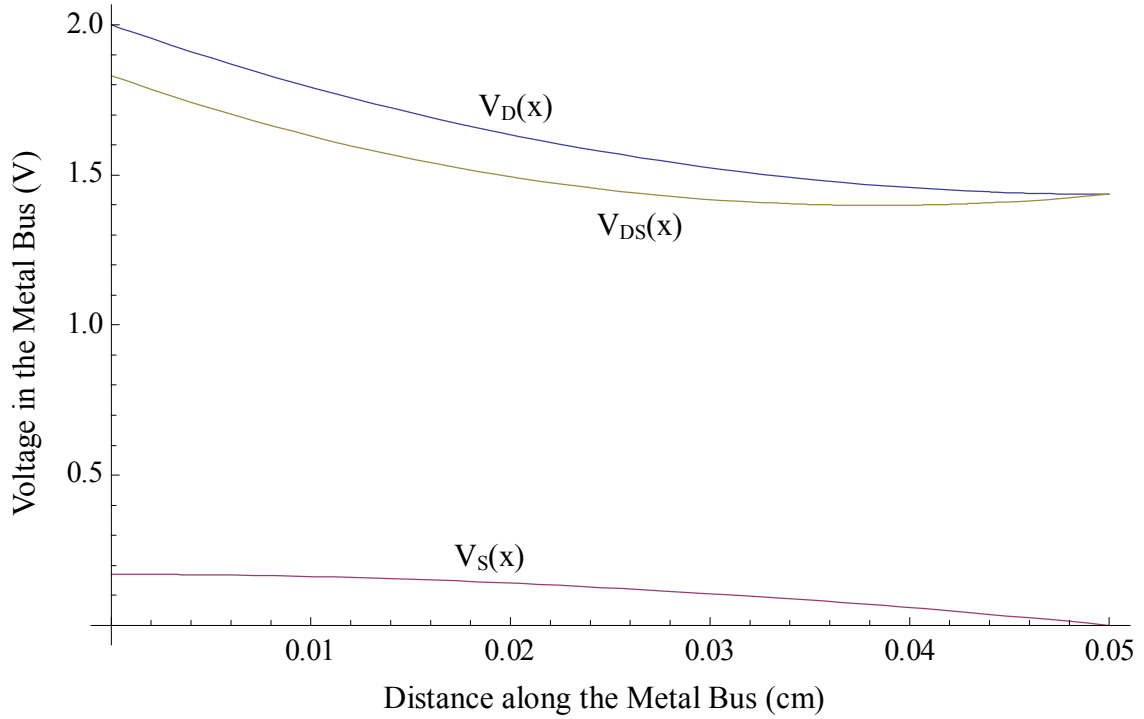


Fig. 5.17 The voltage distributions along the metal finger bus.

Once the voltage distribution is solved, the specific on-resistance of the device considering the voltage debiasing effect can be calculated by

$$R_{ON,sp} = \frac{[V_D(0) - V_S(W)]}{\int_0^W [V_D(0) - V_S(W)] dx} \cdot R_{sh-S} \cdot L \cdot A, \quad (\text{Eq. 5.10})$$

where $A = W \cdot (L + L_{D,S})$ is the device active area and $L_{D,S}$ is the width occupied by Drain and Source, which is $13.25 \mu\text{m}$ in the VC-LJFET design. Note that the resistance calculated here only counts on the drift region resistance. As a comparison, the apparent specific on-resistance is calculated by

$$R_{ON,sp,ideal} = R_{sh-S} \cdot \frac{L}{W} \cdot A = R_{sh-S} \cdot L(L + L_{D,S}). \quad (\text{Eq. 5.11})$$

Therefore, the apparent specific resistance is calculated to be $1.7 \text{ m}\Omega\text{cm}^2$ as compared to the $2.25 \text{ m}\Omega\text{cm}^2$ considering the voltage debiasing effect. It is worth noting that the

voltage debiasing on the Source metal results in the reduction of V_{GS} and so the channel resistance will be affected as well. Better prediction of actual device performance is expected by implementation of the voltage debiasing model into the device compact model.

5.2.2 Exponential Current Shunt

When considering the voltage debiasing in the Gate metal of JFET or the Base metal of BJT, the resistive or linear current shunt shown by Eq. 5.4 needs to be replaced by the p-n junction current shunt which is exponentially dependant on the voltage variation across the p-n junction. Let's still consider the JFET case. Similarly, the Eq. 5.3 converted to

$$\frac{dJ_G(x)}{dx} + \frac{W_{p-n}}{W_G d_M} J_{GS}(x) = 0, \quad (\text{Eq. 5.12})$$

where W_{p-n} is the cross-sectional junction width providing the Gate current flow. And the current shunt is expressed by

$$J_{GS}(x) = J_S \exp([V_G(x) - V_S(x)]/V_T), \quad (\text{Eq. 5.13})$$

where J_S is the saturation current of Gate-Source junction, $V_T = kT/q$ is the thermal voltage. And there is

$$J_G(x) = -\sigma_M \frac{dV_G(x)}{dx}. \quad (\text{Eq. 5.14})$$

Finally, the voltage distribution along the Gate finger can be solved by the differential equation below

$$\frac{d^2 V_G(x)}{dx^2} - \frac{J_S \cdot W_{p-n}}{\sigma_M \cdot W_G \cdot d_M} \exp\{[V_G(x) - V_S(x)]/V_T\} = 0. \quad (\text{Eq. 5.15})$$

And the voltage distribution in the Source metal can also be derived as shown below

$$\frac{d^2 V_S(x)}{dx^2} + \frac{J_S \cdot W_{p-n}}{\sigma_M \cdot W_S \cdot d_M} \exp\{[V_G(x) - V_S(x)]/V_T\} = 0. \quad (\text{Eq. 5.16})$$

It is hard to solve the coupled non-linear differential equations. However, if assume the Source metal is well grounded, the two equations can be simplified to be one equation containing only the Gate voltage,

$$\frac{d^2 V_G(x)}{dx^2} - \frac{J_S \cdot W_{p-n}}{\sigma_M \cdot W_G \cdot d_M} \exp\{V_G(x)/V_T\} = 0. \quad (\text{Eq. 5.17})$$

The Eq. 5.15, 5.16, and 5.17 can be used, by applied appropriate boundary conditions, to predict the Gate or Base metal voltage debiasing effect prevailing in power JFETs and BJTs. However, continuous study is needed to implement these equations in actual device design.

6. CONCLUSIONS AND SUGGESTIONS

6.1 Conclusions

A 4H-SiC JFET based power integration technology has been successfully developed. The technology platform yields the first demonstration in the world of a monolithic SiC power integrated circuit that combines both the high voltage power device and low voltage driving circuitry. The high voltage device in the technology also achieves the best $BV^2/R_{ON,SP}$ figure-of-merit among all Si and SiC lateral power devices up to date. The fabricated power IC chips demonstrate the capability of megahertz switching at a power level as high as 270 W, leading to the potential applications in high-efficiency integrated power electronic systems. The temperature dependence study on the integrable components and the temperature sensing technology demonstrated in SiC show the potential applications of high temperature smart power ICs built in SiC. The work in this SiC power integration study boosts the power level of the single-chip system, expands the application boundaries of today's Si power integration technology, and views the future of ultra compact SiC power converters.

The detailed contributions of this study are summarized below.

- (1) A 4H-SiC VC-LJFET based technology is developed to provide integration of HV and LV lateral JFETs, n-type SiC resistors, and the implanted trench isolations. The process flow originally designed for the vertical JFET has been tailored to fit in the IC fabrication.
- (2) The fabricated HV VC-LJFET realizes a record low specific on-resistance of 9.1 $\text{m}\Omega\cdot\text{cm}^2$ at a blocking voltage of 1028 V. The V_{br}^2/R_{on-sp} figure-of-merit (FOM) of

this device has been calculated as 116 MW/cm^2 which surpasses that of the best reported lateral SiC power device [72] by a factor of three.

- (3) Both theoretical and experimental optimizations of RESURF structure lead to the devices with the blocking voltage between 800 V to 1100 V at the drift lengths between $6.5 \mu\text{m}$ and $9 \mu\text{m}$. The further optimization by forming an etching step near the Drain side extends the blocking voltage to more than 1400 V at the drift length between $12 \mu\text{m}$ and $13 \mu\text{m}$. As compared with the results from other research teams in Table 6.1, the $120 \text{ V}/\mu\text{m}$ blocking performance of this technology is 50% higher than the best results from other teams which are around $80 \text{ V}/\mu\text{m}$.

Table 6.1 The device performance list for the most notable lateral SiC power FETs

BV (V)	$R_{on,sp}$ ($\text{m}\Omega\cdot\text{cm}^2$)	Drift length (μm)	BV/Ld ($\text{V}/\mu\text{m}$)	Affiliation
1028	9.1	8.5	121	Rutgers/USCI 2007
430	12.4	6	72	Rutgers/USCI 2006
794	50	10	79	SEI, 2004
600	160	15	40	SEI, 2004
1300	160	20	65	RPI, 2002
1000	130	20	50	RPI, 2002
460	79	10	46	AIST, 2004
930	170	20	47	RPI, 2004
2700	3180	100	27	Purdue, 2000
1330	67	20	67	Kyoto Univ, 2005
1380	66	20	69	Kyoto Univ, 2006
1550	54	20	78	Kyoto Univ, 2008

- (4) An analytical model for the metallization voltage debiasing is derived to predict the metallization resistance and the corresponded voltage debiasing.

- (5) C-V characterizations for both medium and large packaged HV VC-LJFETs show the predicted small C_{OSS} at high Drain voltage, which is desirable for the high frequency resonant switching applications. Switching characterizations for the HV JFETs show the turn-on and turn-off time around 20 ns and the fast switching characteristics do not degrade with increase of temperature up to 250 °C.
- (6) Full characterizations for the HV, LV FETs and resistors have been carried out at both room temperature and high temperature as high as 300 °C. The temperature dependences of all the components agree with the theoretical prediction.
- (7) The temperature sensing by SiC p-n junctions is proposed and demonstrated in the chip temperature measurement.
- (8) Room temperature switching of packaged power IC demonstrates both high power level of 270 W at 3 MHz, 275 V, and 2 A for a large power JFET, and higher frequency of 5 MHz at 200V and 0.4 A.

6.2 Future Work Suggestions

In order to further reduce the specific on-resistance, scaling down of mesa size into the submicron range resulting in the deep submicron of vertical channel width can make the contribution of channel resistance to the total on-resistance to be negligible. According to the successful batches, a fixed channel length to width ratio of 5 could be used as guidance while the fine adjustment could be assisted by the TCAD simulation. However, the most challenging part of the scaling down is the requirement of deep submicron process techniques which usually are not well established in the university cleanroom facility. In addition to the scaling down, the reduction of channel length is probably worth trial by paying for the price of lower chance to get the normally-off JFETs and the deteriorated channel length modulation property for the LV JFETs.

There is still large room to improve the breakdown performance of lateral power devices since the current performance of $120 \text{ V}/\mu\text{m}$ is still far smaller than the SiC material limit. The field plate can be applied either from the Gate side or Drain side to further flatten the electrical field in the drift region. The field plate technique is also helpful to reduce the Gate-Drain miller capacitance and hence improve switching performance. However, the high electric field in the dielectrics needs to be paid enough attention to avoid reliability problem. Special design should be done to refrain the corner breakdown in the large power devices with linear layout. One straight forward way is to extend the drift length at the corner region to increase the overall device blocking capability.

Higher temperature post implantation annealing process needs to be developed to get more accurate control on the RESURF dose. Higher activation efficiency at higher

annealing temperature for Al ions in SiC is critical to develop p-type JFET which is useful to form the complementary pairs with n-type JFET as the basic building block in the wide circuit applications. Of course the p-type ohmic contact needs further improvement to at least low $10^{-4} \Omega \cdot \text{cm}^2$ range. In order to develop high temperature JFET for reliable operation, the Al should be got rid of from the metallization schemes. The high temperature metals such as Mo, W, and Cu could be used for metallization while the metal patterning, adhesion and CTE mismatch between layers should be addressed.

It is very valuable to construct the compact model for both HV and LV VC-LJFETs. Only based on the well established model, development of more complicated SiC power IC chips can be feasible. The analytical model for the metallization debiasing derived in this thesis could be implemented with the JFET compact model to show more accurate prediction for the power LJFET performance.

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