DESIGN AND FABRICATION OF 4H SILICON CARBIDE MOSFETS

by

JIAN WU

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ABSTRACT OF THE DISSERTATION

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By JIAN WU

Dissertation Director:

Professor Jian H.Zhao

The 4H-SiC power MOSFET is an excellent candidate for power applications. Major technical difficulties in the development of 4H-SiC power MOSFET have been low MOS channel mobility and gate oxide reliability. In this dissertation, a novel 4H-SiC power MOSFET structure has been presented with the aim of solving these problems.

The research started from the study and improvement of the channel mobility of lateral trench-gate MOSFET that features an accumulation channel for high channel mobility. The design, fabrication and characterization of lateral trench-gate MOSFET are presented. The fabricated lateral trench-gate MOSFET with an accumulation channel of 0.15 μm exhibited a high peak channel mobility of 95 cm^2/Vs at room temperature and 255 cm^2/Vs at 200°C with stable normally-off operation.

Based on the successful demonstration of high channel mobility, a vertical trench-gate power MOSFET structure has been designed and developed. This structure also features an epitaxial N-type accumulation channel to take advantage of high channel mobility. Moreover, this structure introduces a submicron N-type vertical channel by counter-doping the P base region via a low-dose nitrogen ion implantation. The implanted vertical channel provides effective shielding for gate oxide from high electric field.

A process using the oxidation of polysilicon was developed to achieve self-alignment between the submicron vertical channel and the gate trench. A "sandwich" process, including nitric oxide growth, dry oxygen growth and nitric oxide annealing, was incorporated to grow high-quality gate oxide.

The fabricated single-gate vertical MOSFET can block up to 890 V at zero gate bias. The device exhibited a low specific on-resistance of 9.3 $m\Omega cm^2$ at V_{GS}=70 V, resulting in an improved FOM (V_B^2 / R_{ON}) of 85 MW/cm^2. A large-area MOSFET with an active area of $4.26x10^{-2}$ cm^2 can block up to 810V with a low leakage current of 21 μA and conducted a high on-current of 1 A at V_{DS}=3 V and V_{GS}=50 V. The fabricated devices all exhibited the stable normally-off operation with threshold voltages of 5~6 V. Their subthreshold characteristics with high on/off ratios of 3~5 indicates that the MOSFETs are capable of operating stably as switching devices.

ACKNOWLEDGEMENT

To my parents, my wife and my son

and

To the memory of my grandparents

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Chapter 1   Introduction

1.1 Material Advantage of 4H-SiC for Power Electronics

The increasing dependence of power electornics in modern society has motivated great advances in power electronics technology. These advances are significantly dependent on the enhancements in the performance of power devices that have been widely used in power generation, power distribution and power management.

An ideal power device should exhibit the following features: carrying any amount of current with zero on-state voltage drop in the forwad conduction mode, holding off any value of voltage with zero leakage current in the blocking mode, and switching between the on-state and off-state with zero switching time. Practical power devices, however, always exhibit a finite resistance when carrying current in the on-state as well as a finite leakage curent while operating in the off-state under certain breakdown voltage, both of which lead to power losses. Hence, in reality, the research work on power devices focuses on utilizing advanced materials as well as innovative device structures, or processing techniques to improve the on-resistance, blocking capability and switching time.

Silicon power devices have served the industry over a long time and they currently dominate power electronics market. Due to the inherent limitations

of silicon material properties, such as narrow bandgap, low thermal conductivity and low breakdown voltage, silicon power devices are approaching theoretical limits in terms of higher power and higher temperature operations, offering no significant improvement in device performances with further investment.

With the development of high quality substrates and processing technologies, 4H-SiC power devices are expected to outperform their Si counterparts in high-power and high-temperature applications, due to the inherent material advantages of 4H-SiC. The material properties of 4H-SiC are listed and compared with other important semiconductor materials in Table 1-1 [1, 2, 3]. In comparison to Si, 4H-SiC has the following advantages:

(a) The breakdown field of 4H-SiC is 10 times as high as that of Si. For the same voltage rating, 4H-SiC devices can be designed using a much thinner drift region and higher drift layer doping than that required for their Si counterparts. Thus the specific-on resistance could be significantly reduced, resulting in the much lower conduction power loss and improved power efficiency.

(b) As a wide bandgap material, 4H-SiC has a bandgap 3 times as wide as that of Si, which means the current increase due to thermal generation is much lower than in silicon. In other words, the intrinsic temperature, at

which the intrinsic carrier concentration becomes comparable to the doping concentration, is extremely high for SiC devices. Hence SiC power devices are capable to operate at much higher temperatures, enabling compact power systems with reduced cooling needs. In addition, the wide bandgap of 4H-SiC keeps its power devices from the degradation of electronic properties under high radiation environment such as aerospace.

(c) The electron saturation velocity of 4H-SiC is two times that of Si. During the switching of a diode, the higher electron saturation velocity of 4H-SiC can offer shorter reverse recovery time, as charges stored in the depletion region can be removed faster. Hence 4H-SiC power devices can be switched at higher frequencies than their Si counterparts.

(d) The thermal conductivity of 4H-SiC is three times as high as that of Si. As an excellent thermal conductor, 4H-SiC power devices have stronger thermal stability, allowing the heat generated in the power devices to be transmitted to a heatsink and the ambient more easily.

Among the wide bandgap semiconductor materials, SiC materials are by far the most developed for power devices in terms of substrate quality and device processing. According to Table 1-1, diamond is theoretically the best candidate for power devices as it has the highest electric beakdown field, the

largest bandgap and the highest thermal conducitivity. However, its material quality and device fabrication technology are still in its infancy. From Table 1-1, it is seen that GaN may perform slightly better than SiC in terms of physical proerties for those power devices that do not require conductivity modulation. However, the wafer quality and manurfactuing technology of GaN are less mature than that of SiC. Another important advantage of SiC over GaN is the fact that SiC, like silicon, has SiO_2 as its stable and native oxide, which is the key to opporunities for high-performance MOSFET fabrication. Hence, due to the availability of high-quality bulk wafers and custom epitaxial layers and the increasing advances on device fabrication technology, SiC has been a very promising candidate for high-power devices.

Among over 150 polytypes of SiC, only the 6H- and 4H- polytypes are commerically available. According to Table 1-1, the carrier mobility of 4H-SiC is substantially higher compared to 6H-SiC. Furthermore, the more isotropic nature of its electrical properites is particularly favor 4H-SiC for power devices [4].

In the past ten years, the SiC growth techniques have been advancing sufficiently for the material to be used in the development of power semiconductor devices. Previously, micropipes, which are crystalline defects in SiC, had been present in nearly all commercially produced SiC wafers.

Recently, however, 100-mm, n-type 4H-SiC substrates with zero micropipe (ZMP) density have been commerically released by Cree, Inc. [5]. The advent of ZMP 4H-SiC substrates is an important step for SiC as the material of choice to be adopted in wide-scale industry of high-power devices.

Table 1-1. Properties of some important semiconductor [1, 2, 3].

Materials	Si	GaAs	Wide Bandgap Semiconductors				
			GaN	3C-SiC	4H-SiC	6H-SiC	Diamond
Bandgap E_g (eV)	1.1	1.4	3.39	2.2	3.26	3	5.45
n_i (cm^{-3})	1.5×10^{10}	1.8×10^{6}	1.9×10^{-10}	6.9	8.2×10^{-9}	2.3×10^{-6}	1.6×10^{-27}
Dielectric constant ε_r	11.8	12.8	9	9.6	10	9.7	5.5
Electron mobility u_n (cm^2/V-S)	1350	8500	900	900	1140//c	370//c	1900
Breakdown Field E_c (MV/cm)	0.3	0.4	3.3	1.2	3	2.4	5.6
Electron saturation Velocity V_{sat} (10^7 cm/s)	1	2	2.5	2	2	2	2.7
Thermal conductivity K (W/cm-K)	1.5	0.5	1.3	4.9	4.9	4.9	20
Direct/Indirect	Indirect	Direct	Direct	Indirect	Indirect	Indirect	Indirect

1.2 4H-SiC Power Devices

Power switching devices are essential components of all the power electronic systems. The major types of power switching devices for low and medium power applications are BJTs, MESFETs, JFETs and MOSFETs.

The BJT is attractive for high power applications because conductivity modulation in the collector layer may lead to a significantly reduced specific on-resistance. Recently some high-voltage BJTs with low sepcific on-resistance have been reported [6, 7, 8]. However, low current gain delays the progress of the development of power BJTs. Since the BJT is fundamentally a current controlled device, it requires the complex and expensive gate drive circuits to deal with the low current gain. Moremore, at the operation of relatively high current density, the high level injection in the base region causes the further fall-off in current gain. Although the current gain can be improved by using the Darlington pair configuration [9], the disadvantage of this structure is a considerable increase in the on-state voltage drop.

MESFETs, JFETs and MOSFETs are all voltage-controlled devices except for the different gate types. Among these devices, SiC MESFETs have been well explored [10]. However, since the gate of a MESFET is a Schottky

contact with a much smaller barrier height than SiC bandgap, its use in high-voltage and high-temperature power switching applications are limited.

For silicon power devices, the interest in JFET structures is limited due to the availability of well-developed silicon MOSFETs. For SiC power devices, however, the problems currently encourtered with the quality and realiability of the SiC/SiO$_2$ interface have brought renewed interest in SiC JFETs for power applications. In terms of device structure, JFETs can be designed to be either lateral [11] or vertical structure. Lateral JFETs have the intrinsic advantage of realizing power integrated circuits but at the cost of lower cell-packing density and consequently a higher specific on-resistance. In contrast, vertical JFETs are preferred in high-power applications due to the higher cell-packng density, and consequently a lower specific on-resistance. In terms of operation behavior, vertical JFETs are of two different types: normally-on [12], and normally-off. In principle, normally-on structure allows higher current density, and lower specific on-resistance. However, since a normally-on device conducts even when no gate voltage is applied, a gate voltage has to be applied for it to stop conduction. Hence it requires a more complex gate drive and additional protection circuits to prevent a DC bus short if the gate signals fail. Usually the normally-off JFETs are more desirable for power electronics. The normally-off design can be realized in

different ways: integrating a normally-off, low-voltage lateral JFET with a normally-on, high-voltage vertical JFET monolithically [13] or by packaging [14], or directly using a purely vertical structure by removing the lateral JFET region for reduced on-resistance, which was first demonstrated on a TIVJFET structure with Ron_sp of 3.6 mΩcm^2 and a blocking voltage of 1726 V [15].

As with their Si counterparts, SiC power MOSFETs are inherently advantageous over other power devices for low and medium power applications.

First, even compared to JFETs, power MOSFETs still have the advantage of extremely low gate current because of the insulating oxide between gate and channel. The very high input impedance due to its MOS gate structure greatly simplifies the gate driver circuits. In applications, the inversion or accumulation layers under the MOS channel can be directly controlled using integrated circuits, as only a small gate current is required to charge and discharge the high-impedance gate capacitance.

Second, as a majority carrier device, power MOSFET is capable of operating at much higher frequencies than that of power BJT, due to the absence of minority carrier injection invloved in its operation. The switching time of power MOSFET is dertermined only by the time of charging and

discharging the input capacitance. No delays are encountered due to storage or recombination of minority carriers.

Third, power MOSFETs are expected to have a stable positive temperature coefficent of the on-resistance because of the unipolar operation and thus the thermal runaway behaior is avoided in power MOSFETs. By taking advantage of this thermal behavior, many individual power MOSFET cells can be parallelly combined or packaged. With a good thermal path, the positive temperature coefficient reduces the current in the hottest device and forces more to flow in the cooler device.

Therefore, due to attractive features of low on-resistance, high blocking capability, high switching speed and simplified gate drive, power MOSFETs are expected to be widely used in a variety of power applications.

1.3 Channel Mobility in 4H-SiC MOSFETs

Although the 4H-SiC MOSFET is considered to be significantly advantageous as compared to other types of power devices, some technical difficulties need to be overcomed before it can achieve its full potential. These issues include the notoriously low channel mobility and consequently high specific on-resistance, and gate oxide reliability under high temperature and high electric field.

The major reason for low channel mobility is believed to be due to the presence of the exponentially increased interface states towards the conduction band edge, resulting in substantial electron trapping and Coulomb scattering at the SiO_2/SiC interface [16]. The origin of these traps is linked to the imperfect nature of the SiO_2/SiC interface, like the presence of carbon clusters [17] and dangling Si and C bonds. Moreover, interface surface roughness may also play a major role in affecting channel mobility through interface roughness scattering of the electrons. It has been shown that p-type implantation into 4H-SiC followed by high temperature activation annealing $(1700 \sim 1750^oC)$ can cause a surface roughness phenomenon called "step bunching" due to loss of silicon from the surface [18,19]. This surface degradation can lead to extremely low channel mobility in 4H-SiC MOSFETs.

Meanwhile, the issue of gate oxide reliability is also linked to the high density of interface states as well as interface surface roughness. The fact that gate oxide needs to be formed on the source region, which usually has a substantial surface roughness due to the heavy dose nitrogen implantation and high-temperature annealing, gives rise to the concerns of gate oxide reliability. In addition, one of the commonly cited intrinsic oxide degradation mechanism in SiC is Fowler-Nordheim (FN) tunneling [20], which is

observed to be exponentially dependent on the electric field and proportional to the square of temperature. It has been experimentally shown that the interface states act as the primary source of FN tunneling into the oxide [21].

Recently, various approaches have been employed to improve the quality of the MOS interface for higher channel mobility.

The use of Nitric Oxide (NO) for either direct oxide growth or for a subsequent annelaing has been demonstrated to improve the peak inversion channel mobilities of 4H-SiC MOSFETs to 50~70 cm^2/Vs [22, 23]. Some research has indicated that this nitridation process of the gate oxide could remove residual carbon from the interface [24], resulting in the reduced density of interface states. Even higher inversion channel mobility up to 150 cm^2/Vs has been achieved by the use of a contaminated alumina environment for gate oxidation [25]. However, there are problems associated with this special process: substantial mobile ions may have been introduced into gate oxide under the contaminated alumina environment [25]; rapid thermal annealing for ohmic contacts has to be avoided to attain the above results, or the channel mobility would be degraded by a factor of about two [26].

Forming MOS channels on alternative crystal faces has also been considered for high MOS channel mobility. A peak mobility of 95.9 cm^2/Vs has been observed in MOS channel mobility by using the $(11\bar{2}0)$ crystal face

(Fig.1-1) as compared to the more commonly used (0001) Si-face [27]. The carbon-face (000$\bar{1}$) was also used to achieve a high channel mobility of 127 cm^2/Vs [28]. Recently a much higher channel mobility of 244 cm^2/Vs on the carbon-face obtained by wet oxidation and nitrogen annealing has been presented in ICSCRM 2007 [29].

One of the promising solutions to the low inversion channel mobility is to introduce an accumulation channel, as it provides a continuous conductive path around the potential barriers and keeps the conduction channel electrons away from the inferior SiO$_2$/SiC surface. Some researchers have utilized a buried channel structure formed by ion implantation to improve the channel mobility in 4H-SiC MOSFETs to up to 140 cm^2/Vs [30]. Similar to [25], however, this high mobility was only obtained without high-temperature ohmic contact annealing, which is an inevitable processing step needed for MOSFET fabrication. In this structure, the thickness and doping of the N-type channel layer need to be carefully chosen so that the channel region is completely depleted from the depletion regions of the P-type base and the gate.
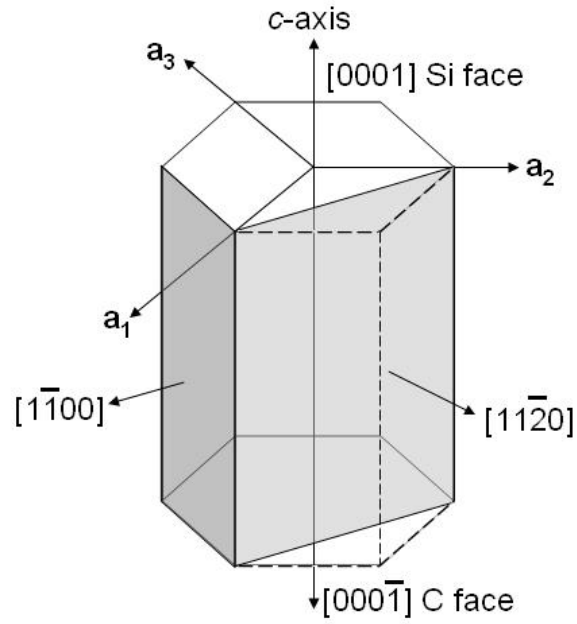
Fig.1-1. Crystal faces of 4H-SiC.
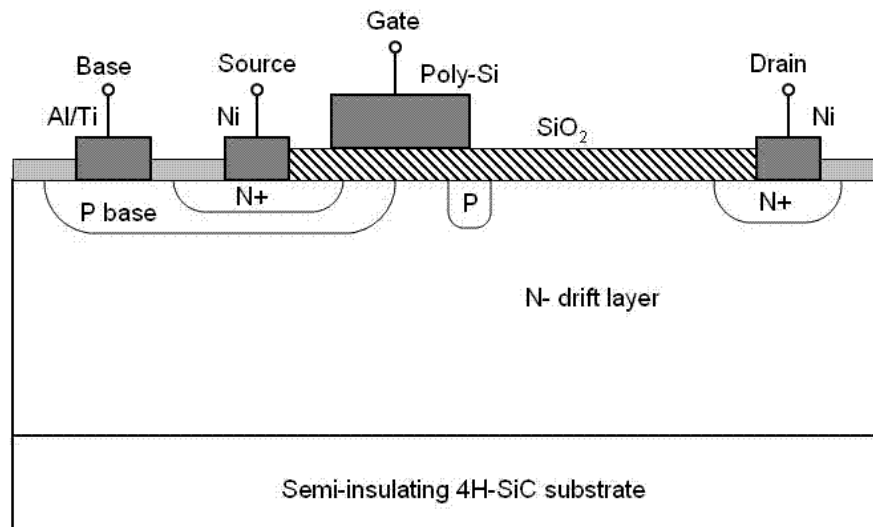
Fig.1-2. Cross-sectional view of a lateral 4H-SiC power MOSFET from [32].

1.4 Trends in 4H-SiC Power MOSFETs

Since the first SiC power MOSFET was reported in 1994 [31], a lot of effort has been devoted to the development of SiC power MOSFETs, and different structures have been employed to achieve the full potential of SiC MOSFETs.

In terms of device structure, MOSFETs can be designed to be either lateral structure (source and drain terminals are all on the front-side of the wafer) or vertical structure (drain terminal is on the backside of the wafer). Initially SiC lateral MOSFETs were introduced in an attempt to increase the theoretical blocking voltage limit imposed by the thickness of the epilayers available at that time. The device exhibited a blocking voltage of 2600 V but with a high specific on-resistance (Fig.1-2) [32]. Then another SiC lateral MOFET with reduced-surface-field (RESURF) design was demonstrated to reduce the specific on-resistance. The device had a specific on resistance of 66 mΩcm^2 with a blocking voltage of 1380V [33]. Although the lateral JFETs is suitable for monolithic integration of power integrated circuits, they have a higher specific on-resistance due to the lower cell-packing density. Intrisiclly vertical MOSFETs are preferred in high-power applications due to the higher cell-packing density and consequently low specific on-resistance.

The first reported power MOSFET was in the form of a vertical trench-gate structure (UMOSFET). The UMOSFET structure contains a gate region that can be fabricated by the trench-etching process, and a P-base region, which can be formed by epitaxial growth over the N-type drift layer. With this process, the UMOSFET cell size can be made relatively small due to the absence of the JFET region in a regular DMOSFET structure, thus resulting in the increased channel density and the elimination of resistance components from the JFET regions. In addition, since both source and base regions can be formed epitaxially, the fabrication process of UMOSFETs can be free of ion-implantation and the associated high-temperature annealing, preventing the device from surface degradation. The first demonstrated 4H-SiC UMOSFET had a blocking voltage of 150 V and a specific on-resistance of 33 mΩcm^2. The results were then greatly improved by other groups (Fig.1-3) [34, 35, 36]. One of the best results were reported by Khan *et al* (Purdue Univ.) with a blocking voltage of 5,050 V and a specific on-resistance of 105 mΩcm^2 [36]. The device introduced a P-bottom layer under the gate trench by a self-aligned ion-implantation to protect the oxide at the bottom of the gate trench from high electric fields in the blocking state. However, SiC UMOSFET suffers from some disadvantages. First, the dry etching technique used to form the deep trench results in a roughened side

wall. The inversion channel mobility on the dry-etched sidewalls of the gate trenches is much lower compared to planar inversion mobility. Second, high electric field stress that occurs at the sharp trench corners may lead to the failure of the gate oxide at these corners. At the MOS interface, the electric field strength in the oxide exceeds the semiconductor field strength by the ratio of the dielectric constants, a factor of 2.5, resulting in a high field in the oxide up to around 5 MV/cm. The field crowding at the trench corner further increases the oxide field to certain value close to or higher than oxide breakdown.

To eliminate the drawbacks in SiC UMOSFET structure, a planar double-implanted MOSFET structure (DMOSFET) was first proposed and fabricated on 6H-SiC [37]. The fabricated DMOSFET could sustain a blocking voltage of 760V, but with a high specific on-resistance of 125 mΩcm^2. Different from Si DMOSFETs, the base and source regions in SiC DMOSFETs can only be formed by successive ion implantation using aluminum or boron for P-base and nitrogen for the N$^+$ source, since impurity diffusion is impractical in SiC. In addition, because P-type implantation activation needs high-temprature anneal (>1550°C), self-aligned implant processes using polysilicon gates can not directly utilized in SiC MOSFETs and realignment must be conducted. Matin *et al* proposed a novel

self-alignment process using poly-Si oxidation for the fabrication of

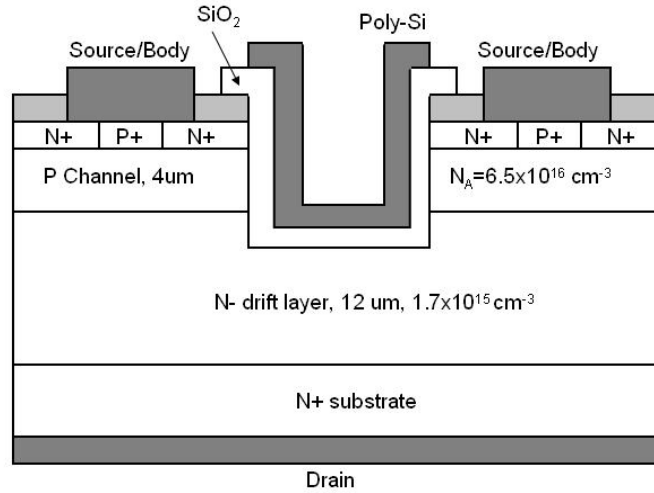short-channel SiC DMOSFETs [38].

Fig.1-3. Cross-sectional view of a 4H-SiC UMOSFET from [34].
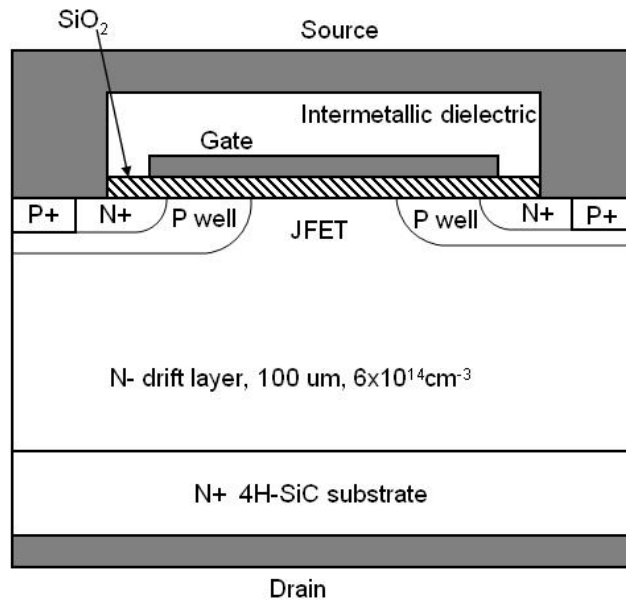
Fig.1-4. Cross-sectional view of a 4H-SiC DMOSFET from [41].

The devices have shown a low specific on-resistance of 9.95 mΩcm^2. Recently, Cree Inc. has demonstrated a series of high-voltage SiC DMOSFETs [39, 40, 41]. One of the best fabricated device was a 10kV , 5A 4H-SiC Power DMOSFET utilizing a 100 μm-thick N-type epilayer with a doping concentration of 6x10^{14}cm^{-3} as drift layer [41]. This is the highest blocking voltage reported for SiC MOSFET. The device showed a specific on-resistance of 111 mΩcm^2 with a gate voltage of 15V at room temperature and a leakage current density of 11μA/cm^2 at 10kV. The effective channel mobility was estimated to be 13 cm^2/Vs. It is seen again that the primary problem in DMOSFET is very low channel mobility. As stated previously, P-base implantation into 4H-SiC followed by high-temperature activation annealing can cause a surface degradation, resulting in extremely low channel mobility in SiC DMOSFETs. In addition, the JFET region between the implanted P-base regions introduces the additional JFET resistance, and also increases the cell pitch.

As the typical UMOSFETs and DMOSFETs suffer from the low inversion channel mobility, accumulation-mode MOSFETs (ACCUFETs) have been emerging as a possible solution for power MOSFETs on SiC. The carriers in accumulation layer are distributed further away from the SiO$_2$/SiC interface than in the case of inversion layer. Hence the effective mobility in an

accumulation layer can be expected to be higher than in an inversion layer because surface roughness scattering is not as severe as in inversion layer [51]. The ACCUFET structure features an N-type accumulation channel. The thickness and doping of this N-type layer is carefully chosen such that it is completely depleted by the built-in potentials of the P/N junction and the MOS gate under zero gate bias, resulting in a normally-off operation. When a positive bias is applied to the gate, an accumulation electron channel is formed under the SiO_2/SiC interface for forward conduction.

A number of attempts have been made to develop UMOS ACCUFETs and DMOS ACCUFETs by either N-type epilayer growth or nitrogen ion implantation for accumulation channel. The first UMOS ACCUFET reported by Denso Corp. (Japan) incorporated an N-type epilayer grown subsequent to trench etch, and exhibited a blocking voltage of 450V and specific resistance of 10.9 mΩcm^2 [42]. The structure also utilized rounded trench corners to alleviate the field crowding problem. Later on Purdue University reported a SiC accumulation-channel UMOSFET with a blocking voltage of 1400V and a specific on-resistance of 15.7 mΩcm^2 [43]. A P-type implanted layer under gate trench by self-alignment was used to protect the oxide at trench corners from the high field in the blocking state.

A few significant progresses have also been made on DMOS ACCUFETs. The first DMOS ACCUFET was demonstrated in 6H-SiC [44], which achieved a blocking voltage of 350V and a specific on-resistance of 18 $m\Omega cm^2$. A subsurface P^+ implant was used in the device to create a thin N-layer below the gate oxide. Recently, Harada *et al* (PERC-AIST, Japan) has reported an accumulation-mode DMOS with an extremely low on-resistance of 1.8 $m\Omega cm^2$ with a blocking voltage of 660 V [45]. The buried N-type accumulation channel was introduced by ion-implantation. However, this device was fabricated on an unusual carbon-face substrate rather than on a regular silicon-face, in order to take advantage of higher channel mobility. Currently the best performing DMOS ACCUFET reported up to date is demonstrated by Miura *et al* (Mitsubish) on the regular Si-face substrate[46]. A specific on-resistance of 5 $m\Omega cm^2$ with a stable avalanche breakdown of 1.35 kV was recorded. The specific on-resistance was still a low value of 8.5 $m\Omega cm^2$ at 150^0C. The accumulation channel was introduced by epitaxial growth and patterned by dry etching. The devices were designed to have a small unit cell pitch of 14 µm and a channel length of 1.0 µm. It is seen that the ACCUFET structure shows a much promising result in terms of its specific on-resistance. Recently, more results on accumulation-mode MOSFETs have been presented in ICSCRM 2007. The SiC Delta-doped Accumulation

Channel MOSFET (DACFET) by Kitabatake *et al* (Matsushita) can block

1400 V with a low specific on-resistance of 6.7 mΩcm^2 [47]. Okuno *et al*

(Denso) demonstrated a (11$\bar{2}$0) face accumulation-channel DMOSFET with

a breakdown voltage of 1100 V and a low on-resistance of 5.7 mΩcm^2 [48].

Table 1-2 summarizes the best reported performances for power 4H-SiC
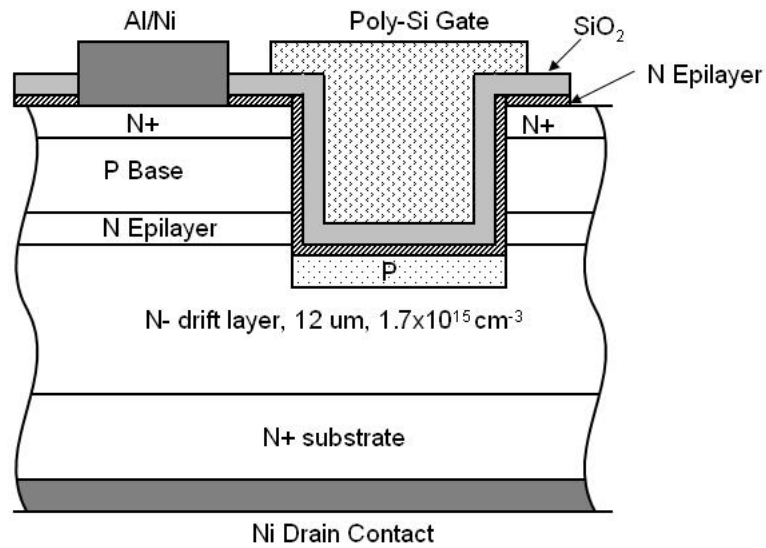
MOSFETs.

Fig.1-5. Cross-sectional view of a 4H-SiC UMOS ACCUFET from [43].
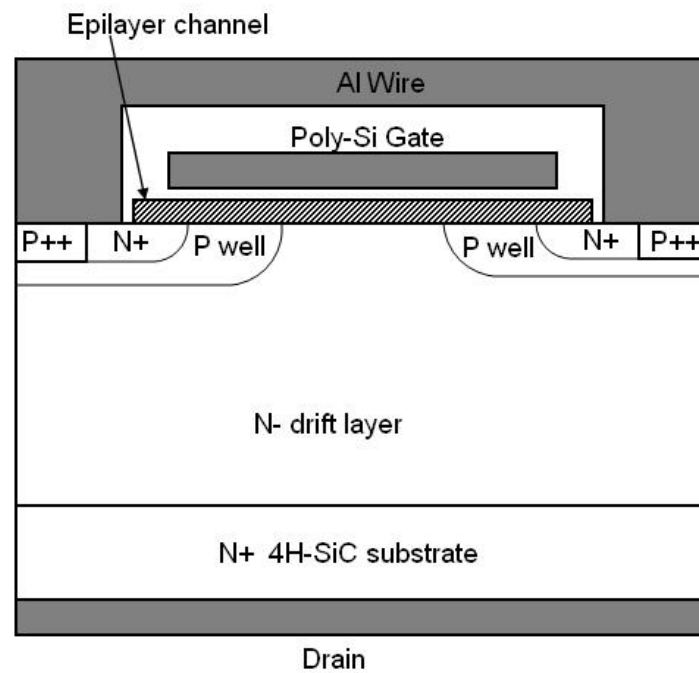
Fig.1-6. Cross-sectional view of a 4H-SiC DMOS ACCUFET from [46].

Table 1-2. Best reported performances for power 4H-SiC MOSFETs.

Device	Blocking voltage (kV)	Sepcific On-Resistance (mΩcm²)	$\dfrac{V_B^2}{R_{ON}}$ (MW/cm²)	Group
DMOSFET	10	111	901	Cree
DMOSFET	10	123	813	Cree
DACFET	1.4	6.7	292	Matsushita
DMOS ACCUFET	1.2	5	288	Mitsubishi
SEMOSFET	5.0	88	284	Kansai EP / Cree
UMOSFET	5.05	105	243	Purdue Univ.
IEMOSFET (C-face)	0.66	1.8	242	PERC-AIST
DMOS ACCUFET (C-face)	1.1	5.7	212	Denso Corp
DMOSFET	2	27	148	Purdue Univ.
DMOSFET	2.4	42	137	Cree, Inc.
UMOS ACCUFET	1.4	15.7	125	Purdue Univ.
UMOSFET	5	228	110	Purdue Univ.
UMOSFET	3.06	121	77	Purdue Univ.
SIAFET	4.58	387	54	Kansai EP / Cree
SIAFET	6.1	732	50.8	Kansai EP / Cree
UMOS ACCUFET	0.45	10.9	18.6	Denso Corp

1.5 Thesis Outline

The 4H-SiC power MOSFET is an excellent candidate for power applications. However, some technical difficulties in the development of 4H-SiC power MOSFET, including low MOS channel mobility linked with high density of SiO_2/SiC interface states and interface surface roughness, need to be solved before it can achieve its full potential.

The goals of this thesis research are to design a novel MOSFET structure and process to improve MOS channel mobility, to develop new processing technology for vertical trench-gate power MOSFET with submicron implanted vertical channels and to demonstrate normally-off 4H-SiC power MOSFETs.

Chapter 2 describes the device design, photomask layout and fabrication process overview of lateral trench-gate MOSFET structure aiming for the improvement of MOS channel mobility. The characteristics of normally-off lateral trench-gate MOSFETs with very high channel mobility are presented in Chapter 3. The dependence of channel mobility and threshold voltage on the accumulation channel thickness is also analyzed. Chapter 4 describes the device design, optimization and photomask layout of the vertical trench-gate power MOSFET structure. Chapter 5 deals with the development of a modified self-alignment process for submicron vertical channels and gate

trenches. Device fabrication challenges and process optimization are also discussed. Chapter 6 presents the fabrication details of vertical trench-gate power MOSFETs and Chapter 7 discusses the experimental results of the fabricated normally-off single-gate MOSFETs and the large-area MOSFETs. The conclusions of this research are given in Chapter 9 along with some recommendations for future works.

Chapter 2   Design and Fabrication of Lateral Trench-Gate MOSFET

2.1 Motivation for Lateral Trench-Gate MOSFET

Compared to other types of the devices, 4H-SiC MOSFET is considered to be an excellent candidate for power switching applications. However, conventional 4H-SiC MOSFETs suffer from high specific on-resistance due to extremely low inversion channel mobility. According to the research reported to date, two factors are believed to be the major reasons contributing to low MOS channel mobility. One is the inferior SiO_2/SiC interface, where the presence of the exponentially increased interface states towards the conduction band edge result in substantial electron trapping and Coulomb scattering. The other one is interface surface roughness due to the high temperature activation annealing ($\geq 1550^0$C). Specifically, in conventional 4H-SiC DMOSFET structure, P-type base implantation requires a subsequent annealing for activation performed at 1700^0C. This high-temperature annealing creates significant surface roughness and drastically affects the MOS channel mobility by scattering of the electrons.

The improvement of MOS channel mobility is consequently concentrated on enhancing the quality of the SiO_2/SiC interface, reducing

surface roughness, and preventing the conduction electrons from the inferior MOS interface. All these goals can be achieved by innovative device structure design and process design. This section describes the design of an innovative lateral trench-gate MOSFET structure and its fabrication process. The study of this lateral MOSFET structure is specifially aming for the improvement of MOS channel mobility. Furthermore, the research on the lateral trench-gate MOSFET is part of the development of vertical trench-gate power MOSFET and the lateral trench-gate structure can be readily transformed into the vertical trench-gate structure.

2.2 Device Design and Simulation

The cross-sectional view of a 4H-SiC lateral trench-gate MOSFET is shown in Fig.2-1. As shown, if the dotted P-type region is converted into N-type by a low dose ion implantation, the lateral structure can be readily transformed into a vertical power MOSFET, which can be fabricated without high-temperature, surface-degrading annealing because of the low dose nitrogen implantation [49, 50].
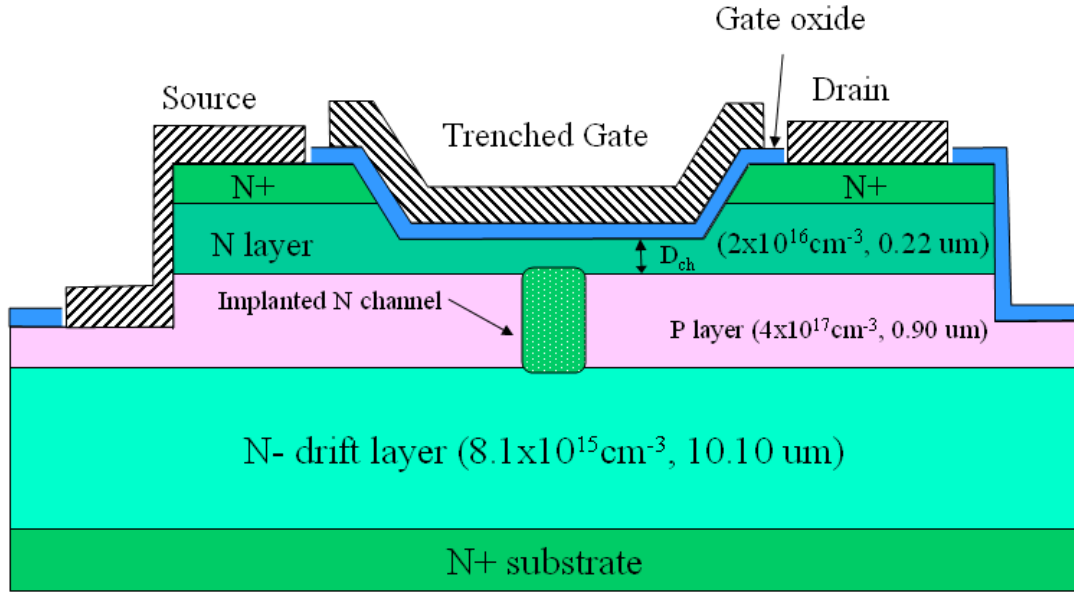
Fig.2-1. Cross-sectional view of lateral 4H-SiC trench-gate MOSFET.
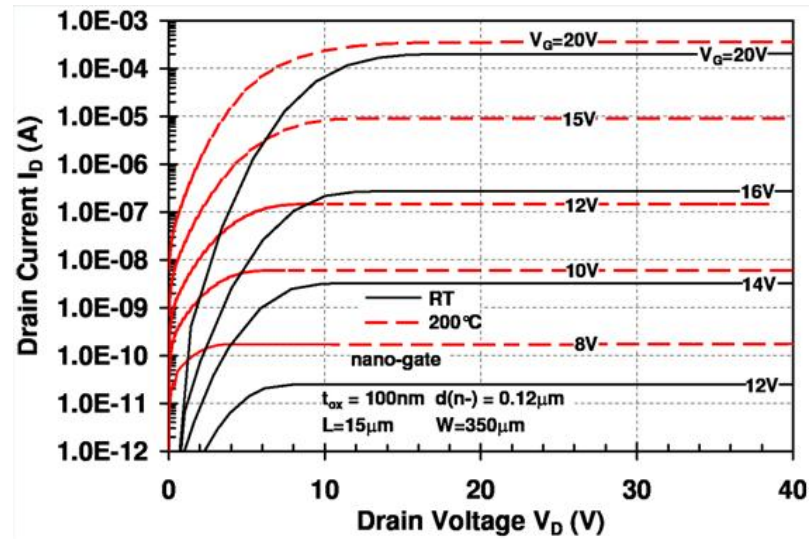

Fig.2-2. Forward I-V curves of lateral MOSFETs at RT and 200°C.

The new lateral MOSFET structure features a buried layer as accumulation channel, which may keep the conduction channel of electrons away from the inferior SiO_2/SiC surface in order to reduce the interfacial trap effect on carrier mobility and the electron scattering by surface roughness. Moreover, this accumulation channel is formed by epitaxial layer. Neither epitaxial regrowth nor ion implantation is needed for channel formation in order to better preserve the surface.

It is also seen in the cross-sectional view, in Fig. 2-1, that this innovative structure design has eliminated the ion implantations in the fabrication for source N+ regions and P base regions. Both regions in this structure are formed by epitaxial layers instead of ion-implantations used in the conventional SiC MOSFET structures, like DMOSFETs. Consequently high temperature annealing ($\geq 1550^{\circ}$C) is not required in the fabrication for activation. Compared to the rough surface created by high-temperature annealing, the preserved SiC surface in gate regions would directly favor the improvement of channel mobility and gate oxide reliability. Although additional low dose implantation will be introduced in the fabrication of vertical trench-gate power MOSFETs, only a lower temperature activation annealing ($< 1550^{\circ}$C) is used.

In addition, the special process using nitric oxide is employed for gate oxidation. A number of researchers have demonstrated that the use of nitric oxide for either direct oxide growth or for a subsequent annelaing improves the peak inversion channel mobilities. In the fabrication process of this lateral trench-gate MOSFET structure, a furthur optimized gate oxidation process with nitric oxide will be used for the nitridation of SiO_2/SiC interface to significantly suppress the interface states.

The above descriptions of the structure design and process design have shown that the introduction of an epitaxial accumulation channel, an epitaxial source N^+ region and a P base region free of ion implantation, and improved gate oxidation process are all aiming for the improvement of MOS channel mobility.

In the device design, the thickness and doping of the N-type accumulation channel needs to be carefully chosen such that it is completely depleted by the built-in potentials of the P/N junction and the MOS gate under zero gate bias, resulting in a normally-off operation. When a positive bias is applied to the gate, an accumulation channel of electrons is formed under the SiO_2/SiC interface for forward conduction. Since the thickness of the epitaxial layer is fixed in the original wafer, the control and adjustment of the thickness of accumulation channel is realized in the fabrication by shallow ICP

dry-etching with varied etching time. Accumulation channels with varied thicknesses can be formed in the different trench-gate regions to explore the optimum thickness range.

Computer simulations in ISE-TCAD simulator have been performed to describe the output characteristics of the lateral MOSFETs. The forward I-V curves of a lateral trench-gate MOSFET at RT (25°C) and 200°C are shown in Fig.2-2, where the phenomena that the output I_{DS} is higher at 200°C than at 25°C is predicted. The simulation is based on the wafer structure shown in Fig.2-1. The wafer has an initial 0.22 μm thick N-type epilayer with a doping concentration of 2×10^{16} cm^{-3} as the buried channel on top of a 0.90 μm, 4×10^{17} cm^{-3} doped P-type epilayer and a highly doped N^{+} cap epilayer (0.15 μm, $N_d =$ 2×10^{19} cm^{-3}) for an implant-free source ohmic contact. The channel width and length are 350 μm and 15 μm respectively. The accumulation channel thickness is chosen as 0.12 μm and the gate oxide thickness is specified as 100 nm.

2.3 Mask Layout

The mask layout of a group of lateral trench-gate MOSFETs is shown in Fig.2-3. The group consists of five MOSFETs with different gate channel lengths, 3 μm, 6 μm, 9 μm, 12 μm and 15 μm respectively. These MOSFETs

have a uniform channel width of 350 μm. The die is then repeated across the mask. The lateral trench-gate MOSFET process consists of four mask levels described in Table 2-1. Meanwhile, the gate trench mask and gate contact mask have dual uses for fabrication. They can be combined to serve as mesa isolation masks during photolithography.

For each MOSFET in the group, a gate contact mask defines the gate metal area with 2 μm overlap on both source and drain regions, in addition to a pad area (100 x 60 μm^2) for probing. Source and drain contact masks define metal source and drain regions with 3 μm spacing to the gate contacts, plus a pad area (138 x 60 μm^2) on each side.

Table 2-1. Photomask set of lateral trench-gate MOSFET process.

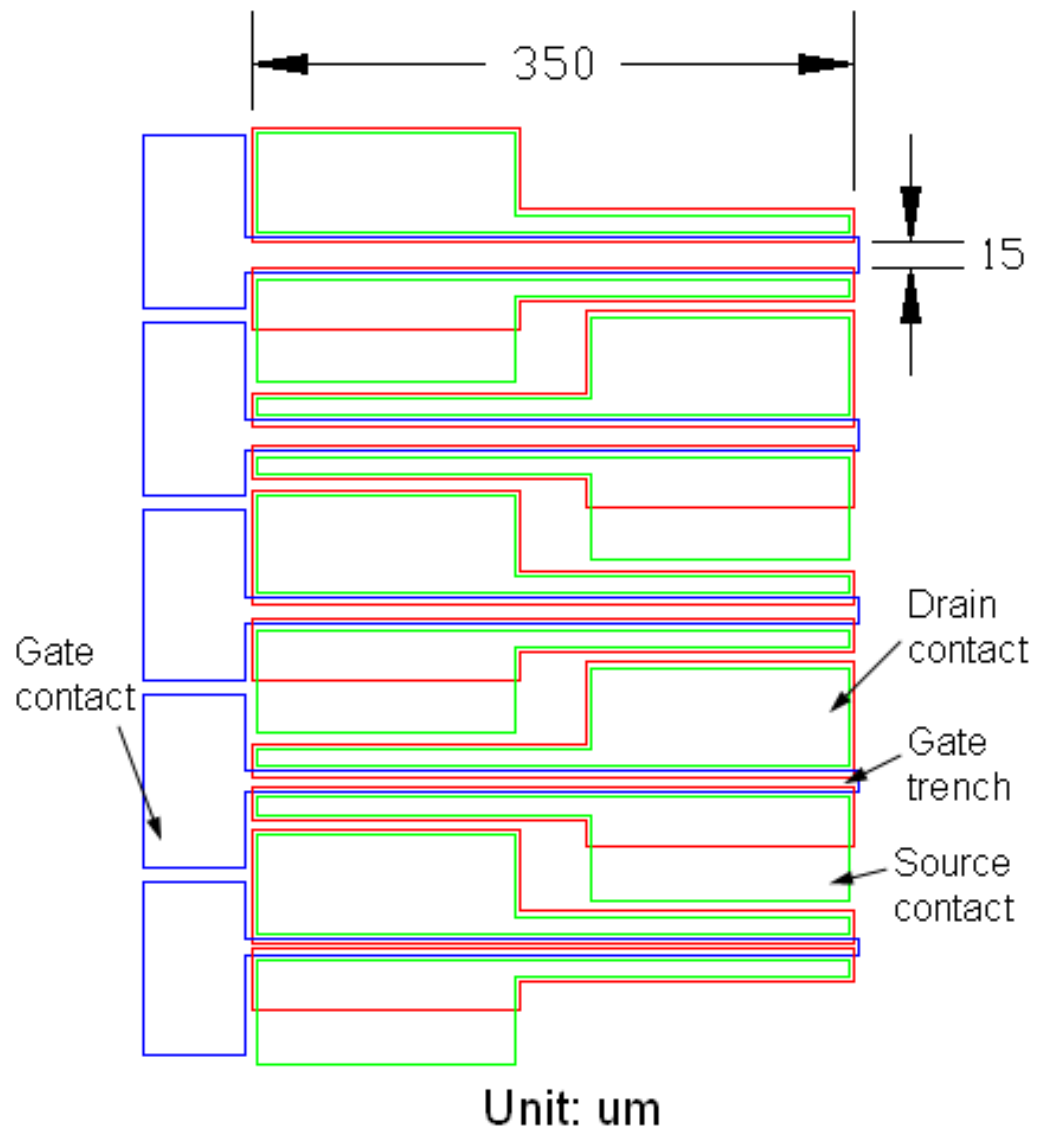| Mask	Uses for Fabrication
Alignment Mask	Alignment marks formation
Gate Trench Mask	Gate trench formation and mesa isolation
Gate Contact Mask	Gate contact formation and mesa isolation
Source and Drain Contact Mask	Oxide windows formation, and source and drain contact formation

Fig.2-3. Mask layout of a group of lateral trench-gate MOSFETs.

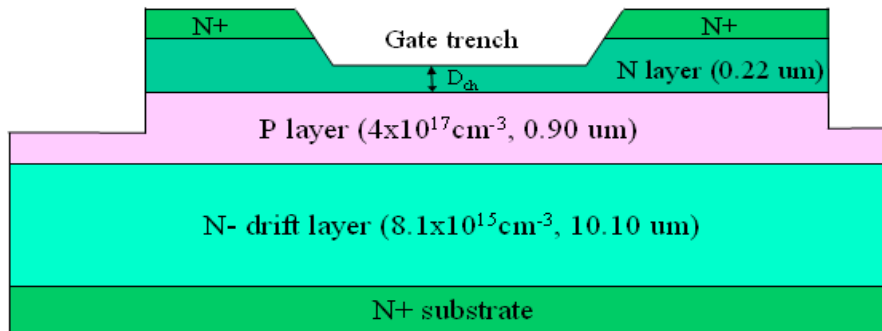## 2.4 Process Flow of Lateral Trench-Gate MOSFET

The process flow of major steps in the fabrication of lateral trench-gate MOSFET is shown in Fig. 2-4. The starting 4H-SiC wafer has an initial 0.22 μm thick N-type epilayer with a doping concentration of 2×10^{16} cm^{-3} as the buried channel on top of a 0.90 μm 4×10^{17} cm^{-3} doped P-type epilayer, and a highly doped N$^+$ cap epilayer (0.15 μm, $N_d = 2 \times 10^{19}$ cm^{-3}) for implant-free source ohmic contact. The mesa isolation can be formed by ICP etching deep into the P layer for mesa isolation. The trench-gate region is formed by shallow ICP etching with varied etching time, resulting in the accumulation channels with different depths to achieve the optimum results. A special oxidation process with nitric oxide and dry O_2 is used to grow 100 nm thick gate oxide of high quality. Rapid thermal annealing is performed for Ni ohmic contacts at relatively low temperature (~900°C), which may prevent the SiO_2/SiC interface from degradation. Molybdenum is finally deposited as gate contacts.
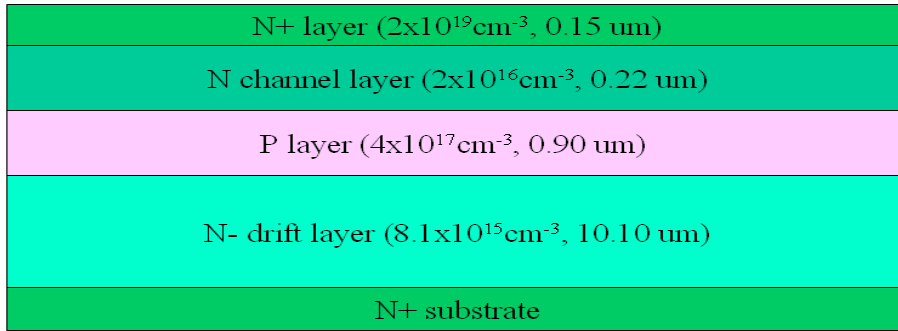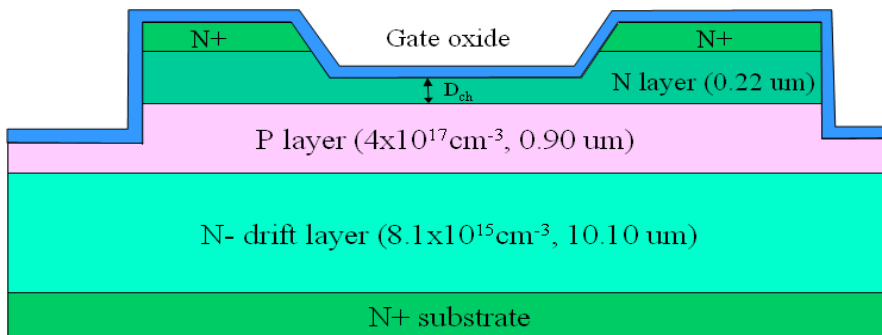
(a) Starting wafer structure
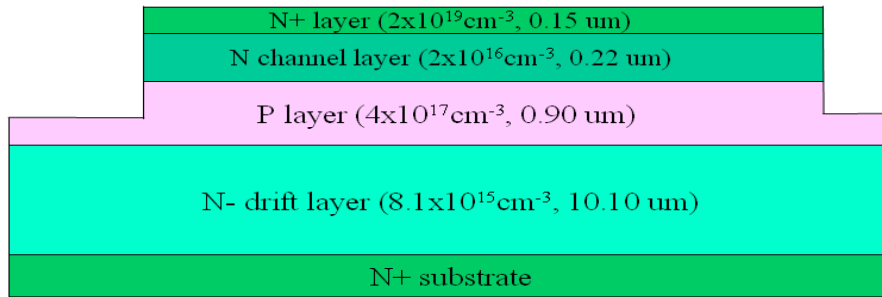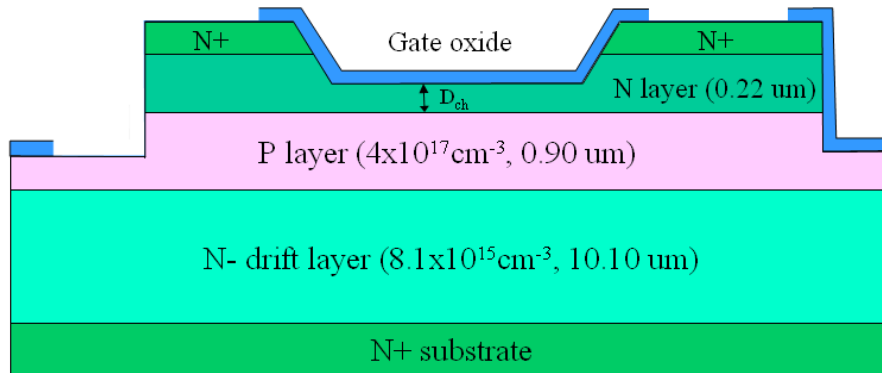

(b) Mesa isolation by ICP etching
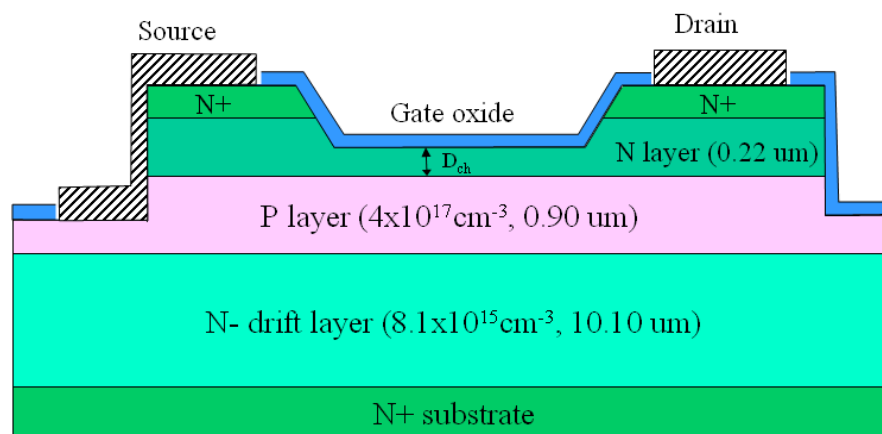

(c) Gate trench by ICP etching
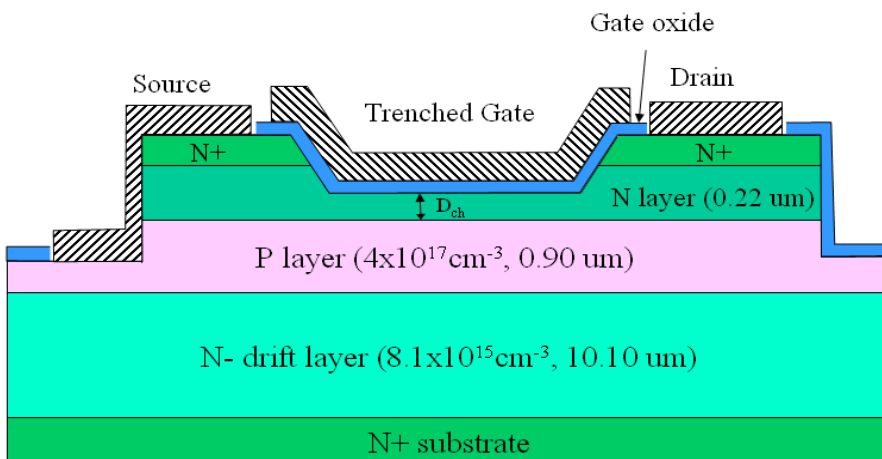

(d) Gate oxidation
Fig.2-4. Process flow of lateral trench-gate MOSFET.

(e) Open contact windows by wet-etching

(f) Source and drain contact

(g) Gate contact

Fig.2-4. Process flow of lateral trench-gate MOSFET (continued).

2.5 Fabrication of Lateral Trench-Gate MOSFET

2.5.1 Wafer specifications

The starting 4H-SiC 8° off-axis Si face commercial wafer, purchased from Cree, Inc., has an initial 0.22 μm thick N-type epilayer with a doping concentration of $2x10^{16}$ cm^{-3} as the buried channel on top of a 0.90 μm $4x10^{17}$ cm^{-3} doped P-type epilayer and a highly doped N^{+} cap epilayer (0.15 μm, $N_d=2x10^{19}$ cm^{-3}) for implant-free source ohmic contact (Fig. 2-1).

2.5.2 Alignment mark formation

This step is intended to form cross-like patterns distributed between devices for the alignment in the following photolithography processes. Alignment mark patterns were formed by ICP etching using double metal layers as dry etching masks.

A full wafer cleaning was conducted on the wafer to remove any possible residuals or particles on the wafer surface. The first metal layer composed of 20 nm AlTi and 150 nm Ni was patterned by photolithography, metal deposition by sputtering and lift-off. The second layer of 300 nm AlTi was deposited to cover possible pinholes in the first metal layer and then patterned with a photolithography and a wet-etching using phosphoric acid and diluted hydrofluoric acid. After removing the photoresist by photoresist stripper, the

exposed SiC surface was etched by ICP in CF_4/O_2 mixture to a depth of 0.5 μm. After ICP etching, the metal masks were all removed by RCA acid.

2.5.3 Mesa isolation

This step is intended to make a deep etching into the middle P layer for mesa isolation. Since no specific mesa isolation mask is available, the gate trench mask and the gate contact mask are incorporated at this step to serve as mesa isolation masks.

One part of the dry etching mask used to protect source and drain regions was formed by 300 nm pure Ni layer, which was patterned by photolithography using the gate trench mask, metal sputtering and subsequent lift-off. The other part of the dry etching mask used to protect gate regions was formed by 300 nm sputtered AlTi, which was patterned by a photolithography using gate contact mask and a wet etching using phosphoric acid. Since this etchant does not attack the bottom Ni layer, the selective etching of AlTi can be realized. After removing the photoresist by photoresist stripper, the exposed SiC surface was etched by ICP in CF_4/O_2 mixture to a depth of 0.7 μm, followed by the wet etching with RCA acid to remove all the metal layers.

2.5.4 Gate trench formation

Formation of gate trenches is one of the critical steps in devices fabrication. In order to compare and identify the optimum thickness of n-layer for high mobility and reasonable threshold voltage, three different thicknesses of N-type channel layer, namely 0.15 μm, 0.12 μm, 0.09 μm, need to be formed in different regions. Prior to the dry etching performed on the actual sample, a small SiC piece cut from the initial wafer served as control sample to determine the accurate ICP etching time needed to achieve the designated depth.

The dry etching mask was formed by 30 nm AlTi. The metal layer was sputtered over the wafer, part of which was patterned by photolithography, followed by wet-etching using a specific AlTi etchant (Al Etch II with surficant) to achieve a smooth etching boundary. The gate trenches with specified accumulation channel thickness of 0.15 μm were then formed on this exposed SiC surface by a timed shallow ICP dry-etching. The entire process has repeated on other two regions to form the gate trenches with accumulation channel thicknesses of 0.12 μm and 0.09 μm.

2.5.5   Gate oxidation

Gate oxidation is another critical step in the fabrication of 4H-SiC lateral MOSFETs. A new oxidation process was used in this step to form a gate oxide of high quality for the improvement of MOS channel mobility.

The gate oxidation procedure started from a thorough cleaning of the samples. Then a standard RCA cleaning process followed by a diluted HF dip was used to clean the samples prior to the sacrificial oxidation. A shallow sacrificial oxide was grown at $1100^{o}C$ in wet O_2 (O_2+H_2O) ambient for 5 min, in order to expose fresh SiC for subsequent gate oxidation. Then the samples were taken out of the furnace, and the sacrificial oxide layer was removed by diluted hydrofluoric acid (15%) with ultrasonic agitation for 20 min. A long-time sandwich oxidation process, composed of the slow growth by nitric oxide, the fast growth by dry O_2, and the nitric oxide annealing, was then employed to grow a 100 nm gate oxide. Fig.2-5 shows the microphotograph of a group of lateral trench-gate MOSFETs after gate oxidation.

2.5.6   Source and drain contacts and rapid thermal annealing

This step is intended to form source and drain contacts concurrently and perform rapid thermal annealing for ohmic contacts.

Prior to metal contact deposition, the windows of source and drain contacts were opened in the oxide by wet-etching with BOE 7:1 (buffered oxide etch). After photolithography defined the source and drain contact regions, a Ni layer of 300 nm was sputtered as source and drain contact metal, followed by a lift-off using the photoresist stripper. It is worth pointing out that prior to loading the sample into the sputtering chamber, a dilute hydrofluoric acid dip was used to effectively remove any unintentional interfacial oxide layer for better ohmic contacts. Source and drain contacts were annealed concurrently by Rapid Thermal Annealing (RTA) at relatively low temperature ($\sim 900^{\circ}$C) in nitrogen forming gas (5% H_2 in 95% N_2), which may prevent the SiO_2/SiC interface from degradation.

2.5.7 Gate contacts formation

Gate contacts were formed by a lift-off process. The photolithography with image reversal was first conducted to define gate contact regions. Subsequently a molybdenum layer of 300 nm was sputtered, followed by a lift-off using the photoresist stripper. Fig.2-6 shows a microphotograph of the fabricated lateral trench-gate MOSFETs after all of the contact formations.
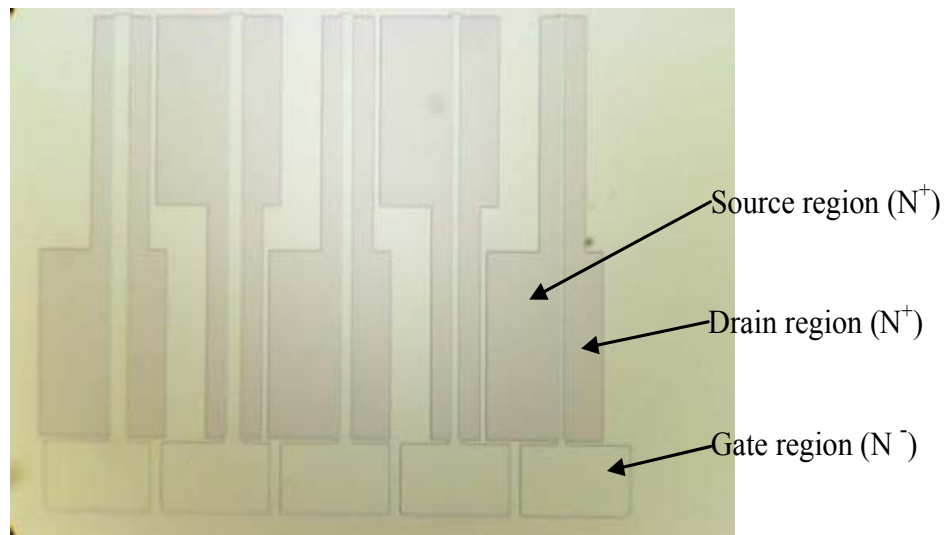
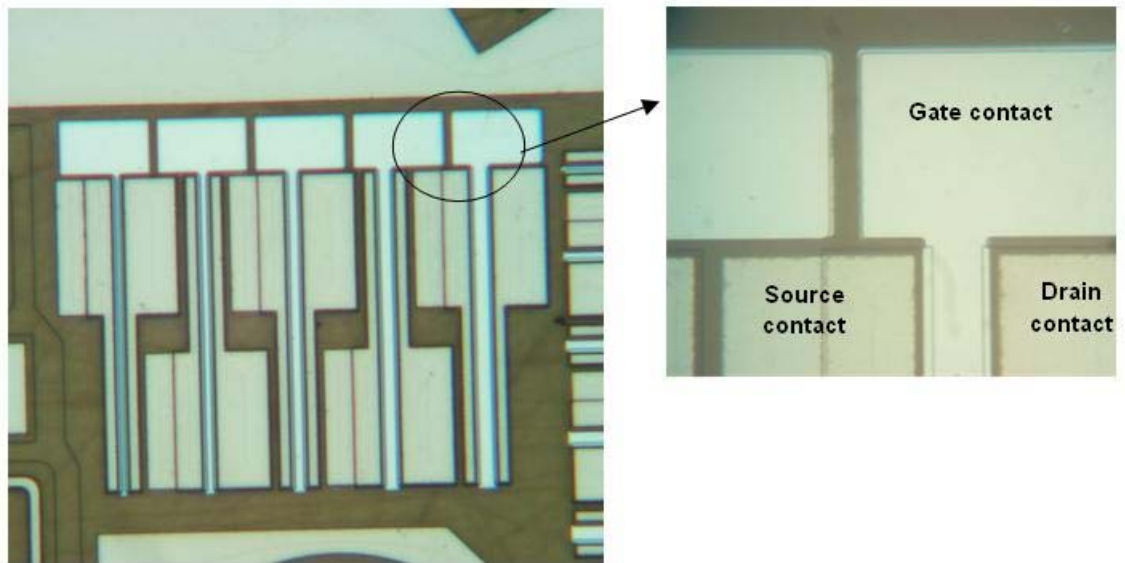Fig.2-5. Microphotograph of a group of lateral MOSFETs after gate oxidation.

Fig.2-6. Microphotographs of the fabricated lateral trench-gate MOSFETs.

Chapter 3   Characterization of Lateral Trench-Gate MOSFET

The on-state measurements of the lateral trench-gate MOSFETs were performed using an HP4145B semiconductor parameter analyzer. All of the devices were tested at chip level using a standard probe station. With the source contacts grounded, the output I_{DS}-V_{DS} characteristics were obtained by applying positive voltages to the drain and gate. The transfer I_{DS}-V_{GS} characteristics were measured with the source grounded and applying a constant voltage of 50 mV to the drain. The gate-drain leakage was first measured, and was confirmed to be of the order of 100 pA.

3.1 Output and Transfer Characeristics

The output I_{DS}-V_{DS} characteristics of a lateral trench-gate MOSFET with an accumulation channel thickness of 0.15 at room temperature ($25^{o}C$) and $200^{o}C$ are shown in Fig.3-1a and Fig.3-1b, respectively. The maximum voltage applied on the gate is 40 V, which limits the maximum oxide field strength to approximately 4 MV/cm. It is seen that the drain currents at $200^{o}C$

are drastically higher than those at room temperature, indicating a substantially increase in the channel mobility at 200°C.

Fig.3-2a and Fig.3-2b show the I_{DS}-V_{GS} transfer characteristics of a device at room temperature and 200°C when V_{DS}=50 mV. The corresponding field-effect mobility μ_{FE} is extracted from the I_{DS}-V_{GS} transfer curve using Eq. (3-1) and also is plotted in Fig.3-2a and Fig.3-2b.

$$\mu_{FE} = \frac{\partial I_{DS}}{\partial V_{GS}} \frac{1}{C_{OX} V_{DS}} \left(\frac{L}{W} \right)$$

(3-1)

where C_{OX} is the oxide capacitance, and L and W are the channel length (L=15 μm) and width (W=350 μm) respectively. At room temperature, the field-effect mobility μ_{FE} reaches a peak value as high as 95 cm^2/Vs at the oxide field around 1 MV/cm, representing a significant improvement in the channel mobility compared to the results in [22, 23], which were subjected to similar high-temperature ohmic contact rapid thermal annealing. It is worth pointing out that this result is more meaningful for the fabrication of MOSFETs than those higher mobilities of 140~150 cm^2/Vs in [25, 26, 30], because those results were only obtained without high-temperature ohmic contact annealing. The field-effect mobility μ_{FE} at 200°C as shown in Fig.3-2b exhibits a substantially higher peak value of 255 cm^2/Vs at low oxide field strength of 1 MV/cm than the peak value at room temperature. The increase in the channel mobility with increasing temperature, which was also reported in

[22], is believed to be attributed to the thermal detrapping of electrons. The reduced Coulomb scattering and the reduced density of trapped electrons due to the detrapping leads to higher channel mobility. Revisiting both Fig. 3-2a and Fig.3-2b, it is seen that μ_{FE} gradually decreases from the peak value as the gate oxide electric field strength increases towards 4 MV/cm. The variation of the effective mobility with increasing electric field normal to the surface results from the enhancement of surface scattering by the higher electric fields applied normal to the SiO$_2$/SiC interface [51], where the interface traps as well as surface roughness are responsible for the increased surface scattering.

In general, the threshold voltage (V_{th}) is extracted from the I_{DS}-V_{GS} transfer characteristics by linear extrapolation. The drain current in the linear region can be written as [52]

$$I_{DS} = \frac{W}{L}\mu_{FE}C_{ox}[V_{DS}(V_{GS}-V_{TH})-\frac{V_{DS}^2}{2}] \tag{3-2}$$

For very small drain voltages, (3-2) can be rewritten as

$$I_{DS} \approx \frac{W}{L}\mu_{FE}C_{ox}V_{DS}(V_{GS}-V_{TH}) \qquad \text{for } V_D << (V_G-V_T) \tag{3-3}$$

Based on Eq. (3-3), since the I_{DS}-V_{GS} transfer characteristics in Fig.3-2a and Fig.3-2b were measured at a very small V_{DS} of 50 mV, V_{th} can be extracted from the intercept on the V_{GS} axis of a linear fit. The V_{th} is found to be 5.6V and 5.3V at room temperature and 200°C, respectively.

One more practical approach for determining V_{th} is the Transconductance (g_m) Extraction (GME) method based on the following derived equation for the linear region:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W}{L} \frac{2\alpha}{q} C_{OX}^2 V_{DS} (V_{GS} - V_{TH})$$ (3-4)

where α is the coefficient dependent on the impurity concentration [53]. Hence the threshold voltage can be determined by extrapolating the g_m-V_G relation to g_m=0. Since μ_{FE} is proportional to g_m, based on Eq.(3-3) and (3-4), the GME method is virtually extrapolating the μ_{FE}-V_G relation.

For comparison purpose, threshold voltage V_{th} is also extracted by GME method. By fitting and extrapolating the curve of μ_{FE} versus V_{GS}, as shown in Fig.3-2a and 3-2b, the threshold voltages are evaluated to be still as high as 3.0V and 2.8V at room temperature (25^oC)and 200°C, respectively, indicating the device is able to operate in normally-off mode for temperature up to 200°C. The normally-off operation of the MOSFETs is attributed to the pinch-off of the accumulation channel of 0.15 μm by the MOS gate and the depletion from the P/N junction.

In summary, the fabricated device with an accumulation channel of 0.15 μm, which has been subjected to ohmic contact rapid thermal annealing, has exhibited a high peak channel mobility of 95 cm^2/Vs at 25^oC and 255 cm^2/Vs

at 200ºC with stable normally-off operation from 25ºC to 200ºC, thus

demonstrating the advantages of the lateral trench-gate MOSFET structure.
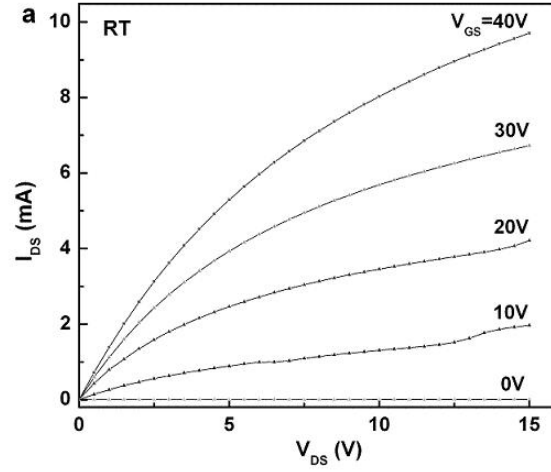
(a)
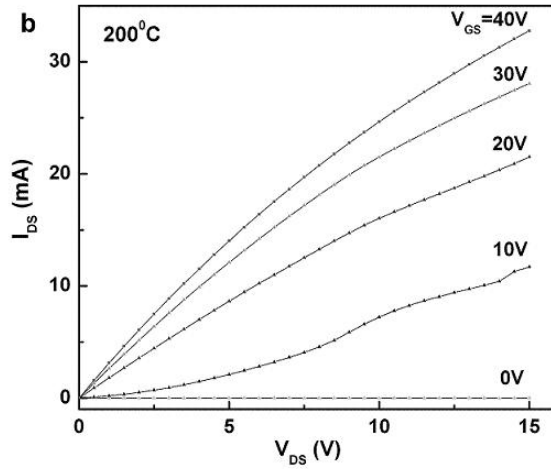
(b)

Fig.3-1. Output characteristics of the lateral 4H-SiC trench-gate MOSFET

with accumulation channel thickness of 0.15μm (Forward I_{DS} vs. V_{DS} at

different V_{GS}) (a) at room temperature (25ºC); (b) at 200ºC.
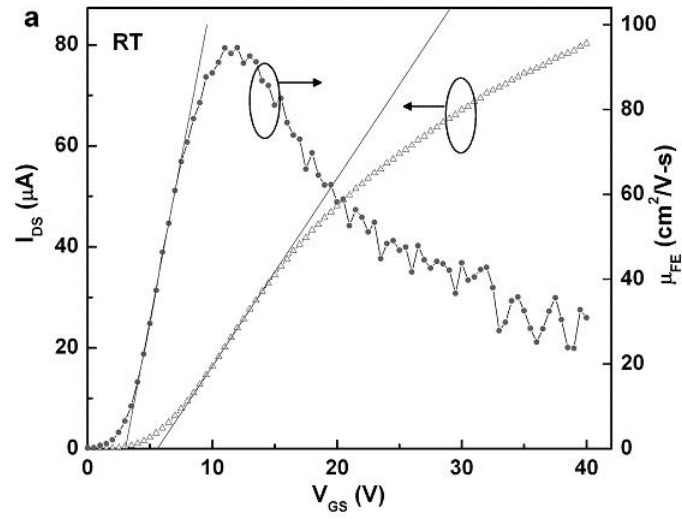
(a)
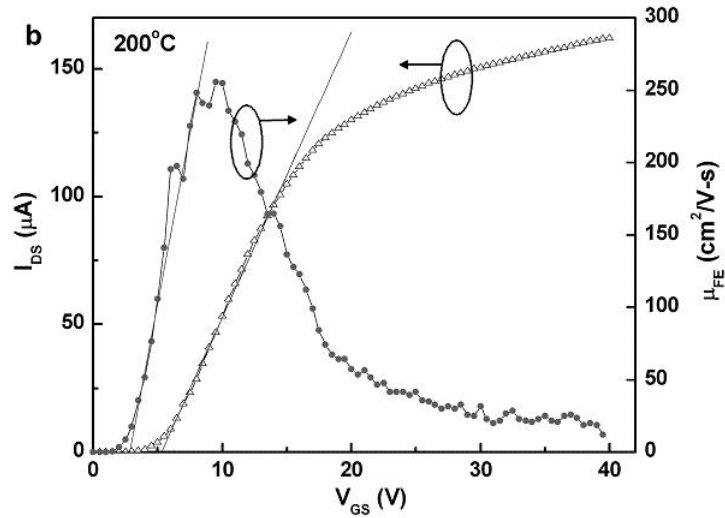
(b)

Fig.3-2. Transfer characteristics (I_{DS} vs V_{GS}) of the lateral 4H-SiC trench-gate

MOSFET with an accumulation channel thickness of 0.15 μm at a V_{DS} of 50

mV, and field-effect mobility as a function of gate voltage (a) at room

temperature (25°C); (b) at 200°C.

3.2 Channel Thickness Dependence of Peak Field-Effect

Mobility and Threshold Voltage

The depth of the epitaxial buried channel (D_{ch}) is a critical design parameter for trench-gate MOSFETs, which affects the channel mobility as well as the threshold voltage. In addition to the devices with a channel depth of 0.15 μm, the devices with channel depths of 0.12μm and 0.09 μm were also fabricated on the same chip and tested using the same procedure described in Section 3.1. Fig.3-3 shows the dependence of the peak μ_{FE} on the buried channel depth at room temperature and 200^oC. For the channel depth of 0.09, 0.12, and 0.15 μm, the peak μ_{FE} values are 59, 81, and 95 cm^2/Vs at room temperature, respectively. The significant improvement of channel mobility with the increase of channel depth is also found at the device temperature of 200^oC, i.e., 160, 190, and 255 cm^2/Vs for the channel depths of 0.09, 0.12, and 0.15 μm, respectively. This tendency can be interpreted to reflect that, as channel depth increases, more electrons can flow in the deep position away from the SiO_2/SiC interface with less scattering by interface traps and surface roughness.

The dependence of the threshold voltage on the buried channel depth at room temperature and 200^oC are compared in Fig.3-4. Fig.3-4a shows the results of V_{th} by extrapolating from transfer curves. It is seen that the threshold

voltage decreases due to the increase of channel depth. For the channel depths of 0.09, 0.12, and 0.15 μm, the threshold voltages are 25.3, 14.6, and 5.6 V, respectively, at room temperature, and 14, 10.4, and 5.3 V, respectively, at 200$^{\mathrm{o}}$C. Fig.3-4 also shows that V_{th} is lower at 200$^{\mathrm{o}}$C than at room temperature, which is consistent with the detrapping of negative electrons at the channel interface. However, the devices with different channel depths, D_{ch}, show substantial discrepancy in the variation of V_{th} when the temperature changes from room temperature to 200$^{\mathrm{o}}$C. The device with D_{ch} of 0.15 μm only shows a shift of V_{th} as small as 0.3 V, whereas the device with D_{ch} of 0.09 μm exhibits a large shift of 11.3 V. These observations indicate that in thicker buried channels, the thermal detrapping of electrons has a weak influence on V_{th}. For comparison, V_{th} values are also extracted by extrapolating from the curve of μ_{FE} vs. V_{GS}, and are shown in Fig.3-4b. It is seen that the dependence of V_{th} on D_{ch} in Fig.3-4b is similar to Fig. 3-4a, in spite of the different V_{th} values due to different extraction methods. From the analysis of Fig. 3-3 and Fig. 3-4, it can be concluded that the best channel depth is 0.15μm, which gives the device the highest mobility at both room temperature and 200$^{\mathrm{o}}$C, and also the smallest shift in $V_{\mathrm{th.}}$
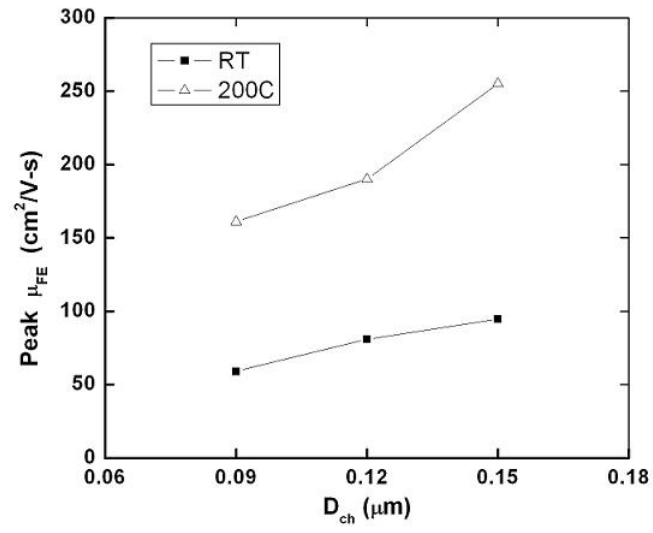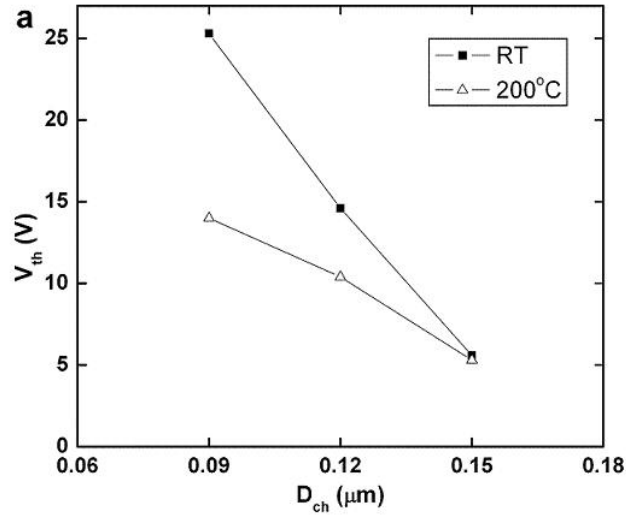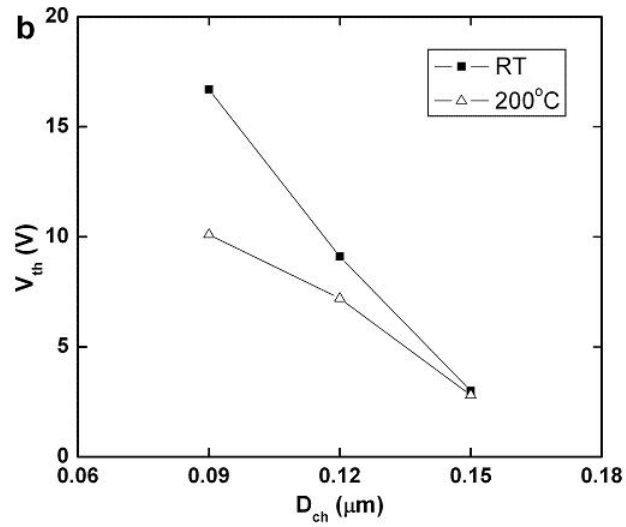
Fig. 3-3. Peak field effect mobility μ_{FE} as a function of buried channel depth D_{ch} at room temperature and 200°C.

(a)

(b)

Fig. 3-4. Threshold voltage V_{th} as a function of the buried channel depth D_{ch} at room temperature and $200^{o}C$ (a) by extrapolating from the transfer curve; (b) by extrapolating from the curve of μ_{FE} vs. $V_{GS.}$

Chapter 4   Normally-Off Vertical Trench-Gate Power MOSFET Structure

4.1 Motivation for Vertical Trench-Gate MOSFET

Although the 4H-SiC MOSFET is considered to be a very promsing structure for power switching devices, its development has been hindered by poor inversion channel mobility and consequently high specific on-resistance. The inferior SiO_2/SiC interface and surface roughness are believed to be the major reasons resulting in low MOS channel mobility. At the inferior SiO_2/SiC interface, substantial electron trapping and Coulomb scattering degrade the channel mobility due to the presence of the exponentially increased interface states towards the conduction band edge. The surface roughness is usually created by high temperature activation annealing ($\geq 1550^0$C). Specifiically, in conventional 4H-SiC DMOSFET structure, a activation annealing at as high as 1700^0C is required after P-type base implantation. Such high-temperature annealing creates significant surface roughness and drastically affects the MOS channel mobility by scattering of the electrons.

In an effort to to improve the MOS channel mobility, a lateral trench-gate MOSFET structure has been designed, fabricated and characterized. Through an innovative device structure design and process design, this lateral trench-gate MOSFET structure may enhance the quality of the SiO_2/SiC interface, reduce surface roughness, and prevent the conduction electrons from the inferior MOS interface and surface roughness, all aiming for the improvement of the MOS channel mobility.

Based on the successful demonstration of normally-off lateral MOSFETs with high mobilities at both room temperature and high temperature, a normally-off vertical trench-gate power MOSFET structure is proposed. The section describes the design and simulation of an innovative vertical trench-gate MOSFET structure. The mask layout and fabrication process flow are also presented.

4.2 Advantages of the Device Structure

As described previously, a lateral trench-gate power MOSFET can be readily transformed into a vertical power MOSFET, if the partial P-type region is converted into N-type by a low dose ion implantation. The cross-sectional view of a vertical trench-gate power MOSFET is shown in

Fig.4-1. The vertical trench-gate power MOSFET structure inherits the advantages of lateral trench-gate MOSFET, aiming for high channel mobility.
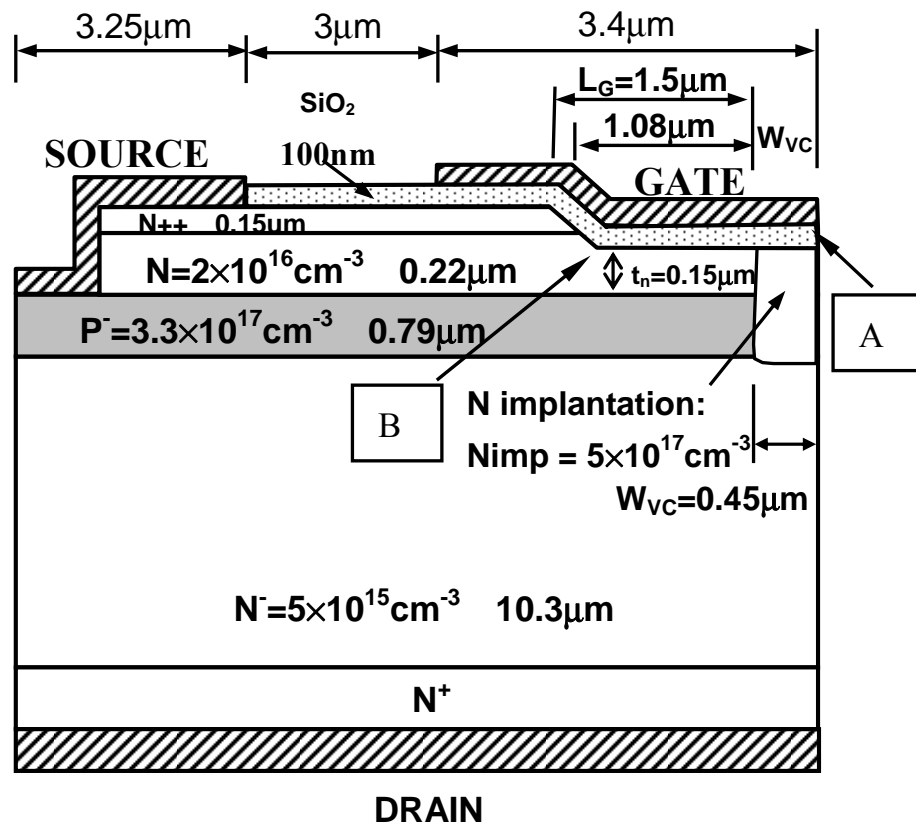

Fig.4-1. Cross-sectional view of 4H-SiC vertical trench-gate power MOSFET.

First, the vertical trench-gate power MOSFET has a horizontal buried layer as an accumulation MOS channel for much improved channel mobility, which has been demonstrated in the study of lateral trench-gate MOSFETs. It is worth pointing out that this accumulation layer is formed by an N-type epitaxial layer. Therefore, neither epitaxial regrowth nor channel implantation is required. Not only does it reduce the fabrication complexity, but it also offers the superior quality of epitaxial channel instead of implanted channel. This accumulation channel formed by epitaxial layer results in a low resistance path for the electron flow by keeping the conduction channel away from the SiO_2/SiC surface, where electron trapping and Coulomb scattering by interface states and electron scattering by surface roughness may degrade channel mobility.

Second, the source N^+ region and P base region are formed by epitaxial layers instead of heavy-dose ion implantations that are used for the convertional SiC MOSFET structures. Consequently, the high temperature activation annealing (≥ 1550 ^oC) that results in surface degradation and consequent low channel mobility is eliminated from the fabrication. Hence the smooth SiC surface in the gate regions would be preserved for the improvement of channel mobility and gate oxide reliability. Although an additional low dose nitrogen implantation will be introduced to form vertical

conductive channels as shown in Fig. 4-1, only a lower temperature activation annealing (<1550 ^{o}C) is required.

In addition, a "sandwich" oxidation process comprised of nitric oxide growth, dry oxidation and nitric oxide annealing will be used for gate oxidation. This optimized gate oxidation process involving nitric oxide may significantly suppress the interface states in the SiO_2/SiC interface.

Since vertical trench-gate power MOSFET is required to sustain a high voltage in the off-state, it also gives rise to the concern of the gate oxide breakdown under a high electric field. As illustrated in Fig. 4-1, Point A is expected to be subjected to the highest electric field in the oxide. The electric field in the oxide is related to the elctric field in SiC, which is inferred from Gauss's Law as

$$E_{OX} = \frac{\varepsilon_{SiC}}{\varepsilon_{OX}} E_{SiC} \approx 2.5 E_{SiC} \qquad (4\text{-}1)$$

Without any shielding structure, the electric field in the oxide would easily exceed its breakdown strength. Usually the threshold of the field for reliable operation is considered to be 4 MV/cm. Moreover, since it is a trench-gate structure, electric field crowding resulting in gate oxide breakdown as in UMOSFETs is another concern for the vertical trench-gate MOSFET structure, specifically at Point B in Fig. 4-2.

These concerns, however, have been significantly alleviated in the vertical trench-gate MOSFET structure. As stated previously, the vertical trench-gate power MOSFET structure is evolved from the lateral trench-gate structure by converting the dotted P-type region into N-type via a low dose ion implantation. When the trench-gate power MOSFET is operating in the forward blocking mode, the implanted vertical N-type channels are pinched-off and the high voltage is mostly supported by the depletion region formed at the P base/N drift junction. The voltage drop across the horizontal epitaxial N channel is very small. Hence the gate oxide is effectively shielded from the high electric field during the blocking mode. The simulation of the vertical trench-gate MOSFET structure has verified that with this effective shielding the electrical field at Point A in the gate oxide is around 4 MV/cm at the designed device breakdown.

The potential problem of electric field crowding at Point B has also been solved by taking the following measures. The effective shielding by the vertical implanted channel has already substantially reduced the electric field along the horizonal epitaxial channel, including the corner at Point B. Moreover, in the preliminary fabrication of the vertical trench-gate power MOSFET, the side wall of the gate trench has been found to be actually a tapering wall at an angle of 25 degrees, instead of a side wall with a sharp

corner. In addition, a wide trench design is utilized in the structure with a small trench depth/width ratio of 0.22μm/3.3μm, rather than the large ratio of 4μm/ 6μm in a typical 4H-SiC UMOSFET [34]. These factors may soften the potential lines curvature at the trench corner and reduce the electric field crowding.

In summary, the vertical trench-gate power MOSFET has novel features all aiming at improving channel mobility and gate oxide reliability: (i) epitaxial accumulation channel for improved channel mobility, with no MOS channel implantation involved, (ii) no high-dose ion implantation, (iii) no high-temperature ($\geq 1550^{o}$C) surface-degrading activation annealing, (iv) no N^{+} source implantation and hence no gate oxide on top of the heavily implanted source region, (v) no epitaxial regrowth, and (vi) an effective shielding structure to prevent the gate oxide and the trench corners from high electric field and electrical field crowding.

4.3 Device Operation and Design Optimization by Simulation

The vertical trench-gate power MOSFET features a horizontal MOS accumulation channel formed by epitaxial layer and a vertical conductive channel formed by nitrogen ion implantation. The thickness of the N epitaxial layer is carefully chosen such that it is completely depleted by the built-in

potentials of the P/N juction and MOS gate at zero bias, resulting in a normally-off device. The channel potential barrier does not have to have a large magnitude, because the depletion of the P base/N drift junction supports most of drain voltage and screens the horizontal epitaxial channel from the drain bias with the vertical channels pinched-off. The implanted vertical N channels are normally-on conduction channels in the on-state. When a positive bias is applied to the gate, an accumulation channel is created at the SiO_2/SiC interface for the forward conduction. Consequently a low resistance path for electron flow is generated from the source to drain via the conductive vertical N channels and horizontal acuumulation N channels.

The accumulation N channel thickness is one of the key important design parameters to determine the normally-off behavior of the device. It needs to be thin enough to be completely depleted by the built-in potentials of the P/N junction and the MOS gate under zero gate bias. On the other hand, if the lateral channel is too narrow, it may increase the on-resistance and affect the threshold voltage. The optimum thickness of N-type MOS channel has been identified from the results of the lateral trench-gate MOSFETs. The epitaxial accumulation channel of 0.15 μm may achieve the highest channel mobility with a stable normally-off operation.

The vertical channel opening and doping are also critical parameters in the device design. Ideally, the vertical channel needs to be conductive during the on-state, whearas it is effectively pinched off during the off-state to shield the gate oxide from the high electrical field. For a given vertical channel doping, the optimum channel opening must be optimized not only to obtain the low specific on-resistance, but also to control the electrical field at the gate oxide interface and achieve high blocking voltage. The narrower the vertical channel opening, the less is the electrical field at the gate oxide and the higher is the blocking voltage. However, these benefits are gained at the cost of higher vertical channel resistance.

Using computer simulations in ISE-TCAD simulator, the influence of the vertical channel opening and doping concentration on blocking voltage, oxide field and specific on-resistance has been depicted in Table 4-1.

At the given doping concentration of $N_{imp}=5.5 \times 10^{17} cm^{-3}$, when the half channel opening W_{vc} varies from 0.35 to 0.7 μm, the specific on-resistance is improved from 9.32 to 7.40 $m\Omega cm^2$, while the breakdwon voltage decreases from 1918 to 1896 V and the corresponding electric field in the oxide increases significantly from 3.85 to 7.68 MV/cm, far beyond the value for the reliable device operation. Fixing W_{vc} at 0.45 μm, when N_{imp} varies from $5.5 \times 10^{17} cm^{-3}$ to $4.5 \times 10^{17} cm^{-3}$, the electric field in the oxide reduces from 5.14

to 3.61 MV/cm while the specific on-resistance increases from 8.75 to 9.19

$m\Omega cm^2$. It is seen that a good trade-off between forward current density and

blocking performance can be achieved by introducing the vertical implanted

channel with $N_{imp}=5.0 \times 10^{17} cm^{-3}$ and $W_{vc}=0.45\mu m$, where the oxide field is

limited around 4MV/cm to prevent premature oxide breakdown.

Table 4-1. Summary of simulation results of the vertical trench-gate power
MOSFET structure.

| W_{vc} (μm)	N_{imp} (cm^{-3})	Breakdown Voltage (V) at RT	Field in SiO_2 at Breakdown E_{ox} (MV/cm)	Threshold Voltage V_T (V) at RT	Rsp,on ($m\Omega cm^2$) at RT
0.35	5.5×10^{17}	1918	3.85	-	9.82
0.45		1916	5.14	5.03	8.75
0.55		1911	6.26	-	8.08
0.70		1896	7.68	-	7.40
0.45	5.5×10^{17}	1916	5.14	5.03	8.75
	5.0×10^{17}	1908	4.35	5.00	8.91
	4.5×10^{17}	1908	3.61	-	9.19

4.4 Mask Layout

The devices designed in the mask layout consist of large-area devices with active area of 1.03×10^{-2} cm^2, medium-area devices with active area of 1.03×10^{-2} cm^2, small-area devices with active area of 9.357×10^{-4} cm^2. A set of test structures are designed as well, and are distributed in different regions to control the process. These structures include including single-gate vertical power MOSFETs, MJET P-N diodes to identify the optimum JTE depth, rectangular TLM patterns to verify contact resistance of source P contacts and source N contacts, MOS capacitors, and lateral MOSFETs to test channel mobility. The detailed mask set information is listed in Table 4-2. The mask layout of small, medium and large MOSFETs, and test structures are shown in Fig.4-3.

Table 4-2. Photomask set for vertical power nano-gate MOSFET process.

| Mask	Uses for Fabrication
Alignment and Mesa Mask	Alignment mark formation and mesa isolation
JTE-3 Mask	JTE-3 formation (outermost step)
JTE-2 Mask	JTE-2 formation (intermediate step)
JTE-1 Mask	JTE-1 formation (innermost step)
Source Trench Mask	Source trench formation
1.2 μm Gate Trench Mask	Gate trench formation
Gate Contact Mask	Gate contact formation
Source P Contact Mask	Source contact on P base
Source N Contact Mask	Source contact formation on N-type source
Overlay-1 Mask	Connection for source fingers and gate fingers
Overlay-2 Mask	Contact pads of the second overlay
Overlay-3 Mask	Bonding pads formation
Overlay Window Mask	Open oxide window for new overlay
New Overlay Mask	New overlay formation
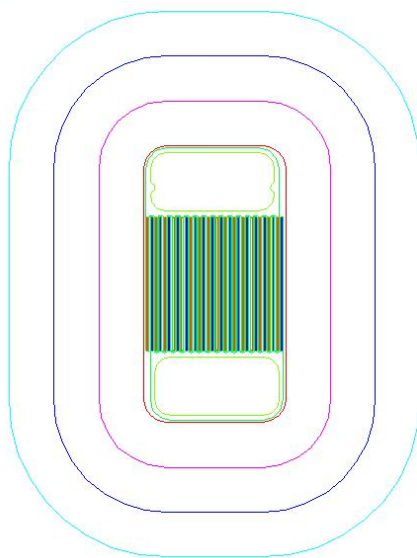
(a)
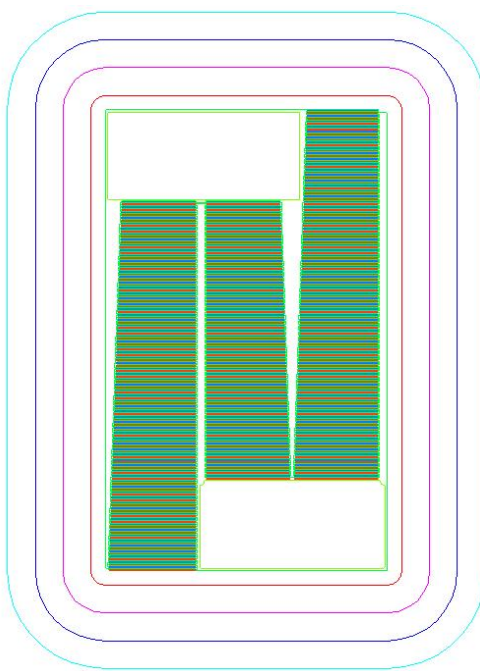
(b)

Fig. 4-3. Mask layout of (a) small-area MOSFET (b) medium-area MOSFET.
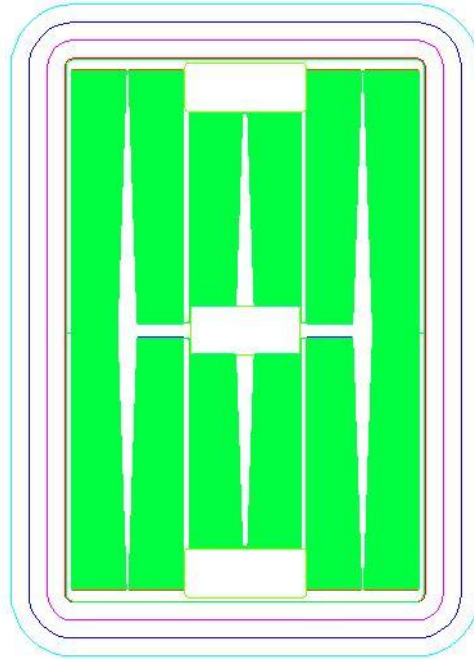
(c)
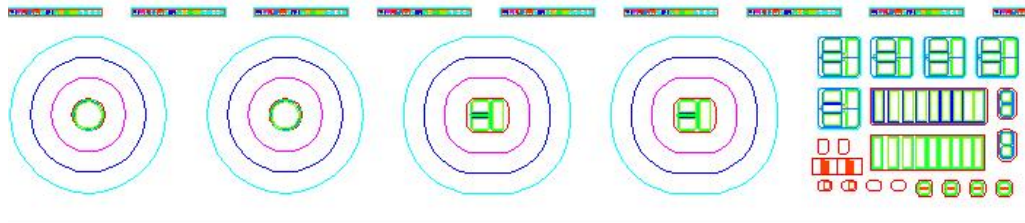
(d)

Fig. 4-3. Mask layout of (c) large-area MOSFET (d) test structures (continued).

Chapter 5   Process Development of Vertical Trench-Gate Power MOSFET

## 5.1 A Process for Self-Alinged Trench Gate and Submicron Vertical Implanted Channel

The advantageous vertical trench-gate power MOSFET structure features a horizontal epitaxial N channel as an accumulation channel and a vertical N channel. The horizontal epitaxial channel can keep the conduction channel of electrons away from the inferior SiO_2/SiC surface, and its thickness of the N epitaxial layer is carefully chosen such that it is completely depleted by the built-in potentials of the P/N juction and MOS gate at zero bias for normally-off operation. In fabrication, the thickness of the accumulation channel is determined by shallow ICP etching to form the trench gate structre. The vertical N channel is formed by nitrogen ion implantation. It needs to be conductive during the on-state, whereras it is effectively pinched off during the off-state to shield the gate oxide from the high electric field. According to the device simulation, the optimum vertical channel doping concentration is $5.0 \times 10^{17} cm^{-3}$ and channel opening is 0.9 μm.

The biggest challenge faced in the fabrication process is the creation of implantation mask for submicron vertical channel and the alignment of the mask to the gate trench. The best optical lithography system available at the Microelectronics Research Laboratory (MERL) of our department is Karl Suss MJB3 mask aligner. The minimum linewidth it can generate in the appropriate photoresist is 1.5 µm for dense patterns and 0.8 µm for sparse patterns [54]. Apparently standard lithography with this mask aligner is unable to directly pattern thick photoresist or metals to form implantation mask for submicron vertical channels.

A modified self-aligned process using polysilicon oxidation, which is modified from [38], may enable us to obtain the submicron vertical N channel and align it to gate trench. The process steps are outlined below and are shown in Fig. 5-1.

(1). First a 3 µm thick polysilicon layer is deposited and patterned with a metal mask by dry-etching.

(2). With the patterned polysilicon layer as dry etching mask, the gate trench is formed by shallow ICP etching. The gate trench width is controlled to be approximately 2.8 µm. Determination of etching depth takes into account the SiC consumption in the subsequent polysilicon oxidation and gate oxidation.

(3). The polysilicon is thermally oxidized. As the oxide expands on the polysilicon trench sidewall, the polysilicon trench width is reduced. By controlling the oxidation time, the polysilicon trench opening of 0.6~0.8 μm can be obtained.

(4). With the oxidized polysilicon trench as implantation mask, deep nitrogen ion implantation is performed to convert a path in the P base layer to a vertical N channel.
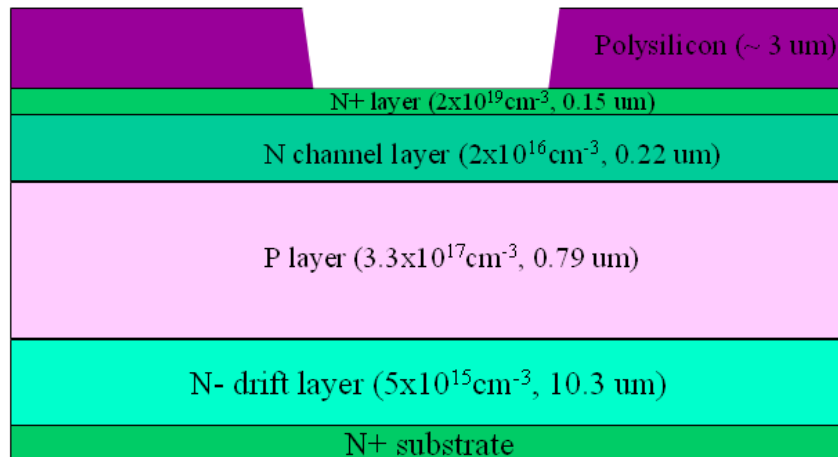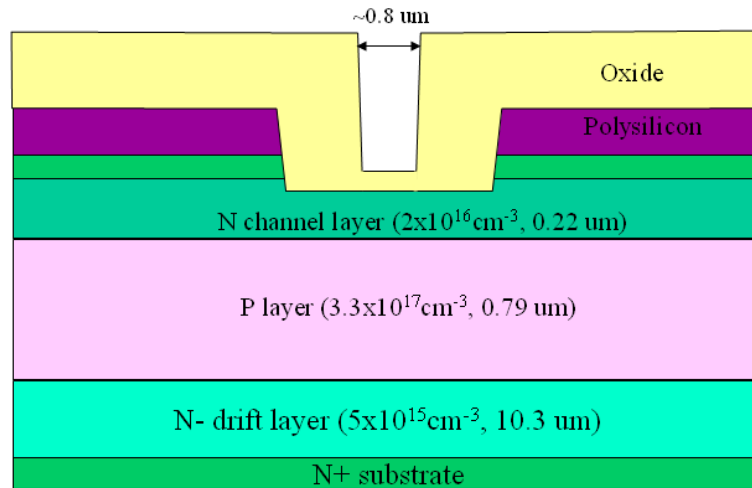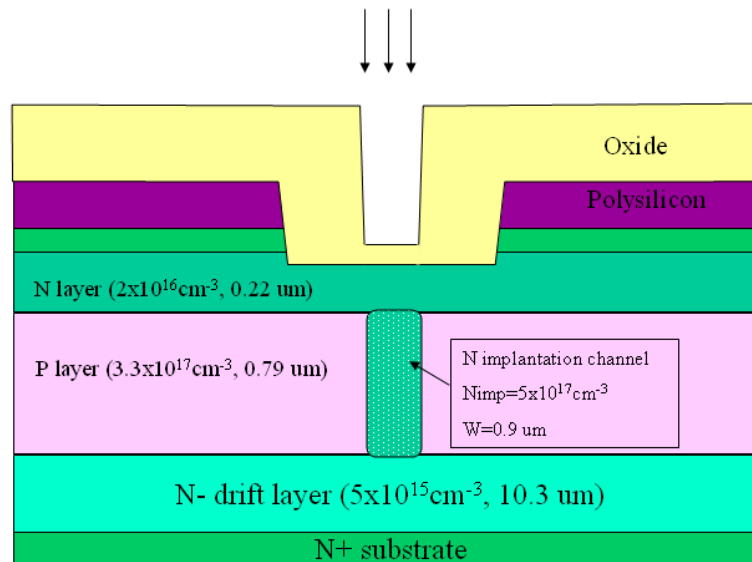
(a) Poly-Si trench formed by dry etching
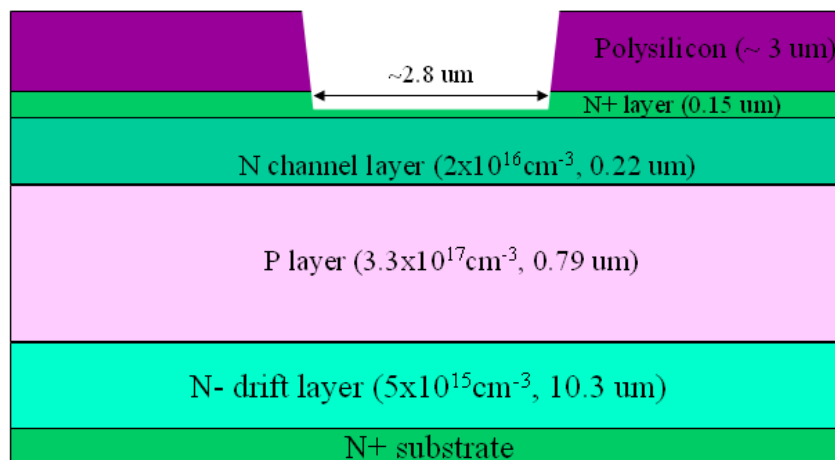
(b) Gate trench etching with polysilcion as dry etching mask.

Fig. 5-1. Process steps of self-aligned gate trench and submicron vertical N channel.

(c) Polysilicon oxidation to form implantation mask

(d) Nitrogen ion implantation to form vertical N channel

Fig. 5-1. Process steps of self-aligned gate trench and submicron vertical N channel (continued).

5.2 Fabrication Challenges of Vertical Trench-Gate Power MOSFETs

Polysilicon etching

Not only does polysilicon serve as the dry etch mask for gate trenches, but it is also used as a self-aligned implantation mask for vertical channels after thermal oxidation oxidation. Based on an implantation profile simulation, a polysilicon layer of 3 μm thick is required to block ion implants. Such thick polysilicon causes considerable difficulties in forming polysilicon trenches with uniform width and depth by Reactive Ion Etching (RIE). An appropriate metal scheme is needed to serve as dry etching mask to form a qualified poly-Si trench profile.

Gate trench etching

The thickness of the accumulation channel is a key parameter to achieve normally-off operation. In an effort to determine etch depth, Secondary Ion Mass Spectrometry (SIMS) analysis has to be performed first to extract the accurate wafer structure. Moreover, plasma-etching conditions should be optimized for the accurate control of etching depth and the qualified etched surface.

Thermal oxidation of polysilicon for submicron vertical channels

Oxidized polysilicon serves as the self-aligned implantation mask for vertical N channels. The width of the polysilicon trench before oxidation is required to be around 2.8 μm for gate trench etching. Since the optimum vertical channel opening is around 0.9 μm, the width of polysilicon after oxidation has to be around 0.8 μm. Consequently the major difficulties in forming the self-aligned implantation mask lie in the optimization of the oxidation process to reduce the polysilicon trench width to the required submicron dimension value and to obtain an ideal vertical trench profile for ion implantation.

Deep nitrogen implantation and activation annealing

Deep nitrogen implantation with appropriate dose and depth is required to counter-dope the P layer and to form vertical N channels.

Underdose implantation is unable to counter-dope the P layer and result in non-conductive channels during the on-state, while overdose implantation may deteriorate the blocking performance, as the vertical channels with high nitrogen doping may cause less pinch-off and increased leakage current during off-state. Appropriate implantation depth is also required to penetrate the P layer to form a conductive N layer. The implantation depth therefore needs to be carefully controlled as well. If the implantation depth is less than P epilayer thickness, no conductive vertical channels are formed and

consequently no forward currents occur, whereas deeper nitrogen implantation may introduce the high dose nitrogen implants into the N drift layer, resulting in premature breakdown under reverse bias. In addition, the activation annealing process at a lower temperature ($<1550^0$C) needs to be developed to activate nitrogen implants without surface degrading.

MJTE edge termination by ICP etching

Device edge termination is of vital importance to achieve high blocking voltage. Multi-step Junction Termination Extension (MJTE) has been proved to be an effective method for device termination [55]. ICP etching is used to form MJFET steps. The heights of these steps are to be determined by applying some etching trials on small-area defect-free test diodes, and then reproduced on the real devices.

Gate oxidation

High-quality gate oxide is the key to significantly reduce the density of interface states. An appropriate oxidation process is therefore needed to be identified to achieve high-quality gate oxide.

5.3 Development of Self-Aligned Process Using Polysilicon

The polysilicon process is an efficient method for self-alignment of gate trench and submicron vertical N channel. However, the thick polysilicon layer gives rise to a few difficulties during polysilicon etching and polysilicon oxidation. This polysilicon process needs to be developed and optimized to produce the uniformity of the width and depth of polysilicon trenches and the width of oxidized polysilicon trenches.

5.3.1   Uniformity improvement of polysilicon trench width

The uniformity of polysilicon trench width deals with the following issues: selecting an appropriate material as etching mask for polysilicon RIE etching, patterning the etching mask to obtain the uniform linewidth of ~2.2 μm, and dry etching on polysilicon trenches to obtain uniform width of ~2.6 μm for gate trench etching.

Polysilicon dry etching is performed in BCl_3/Cl_2 mixture by MEMS and Nanotechnology Exchange. A series of experiments have been conducted to find out the appropriate material for dry etching mask. Metal masks such as Ni and AlTi have been found to be suitable to serve as dry masks for the qualified profile of vertical trench, while regular thick photoresist produces to the rounded trench profile.

However, neither AlTi nor Ni can be used individually as a reliable dry etching mask. After a series of experiments, a new metal scheme involving both Ni and AlTi has been developed in order to define the fine patterns and effectively prevent pinholes. A 100 nm thick Ni layer is first deposited on the polysilicon as protective layer to prevent pinholes and is patterned by a standard photolithography using gate trench mask with 1.2 μm patterns and a wet etching. Due to large undercut during the wet etching, usually the width of resultant patterns on Ni layer is over 3μm, beyond the required range to define the polysilicon trench. After removing photoresist and cleaning the surface, a 200 nm thick AlTi layer is deposited on the Ni layer and will be used to define polysilicon gate trench. After strictly controlled photolithography and wet-etching, the resultant width of AlTi patterns is around 2.2 μm, which is qualified to form polysilicon trenches by etching. Fig. 5-2 shows the microphotograph of the double metal layer (Ni/AlTi) as the RIE etching mask.
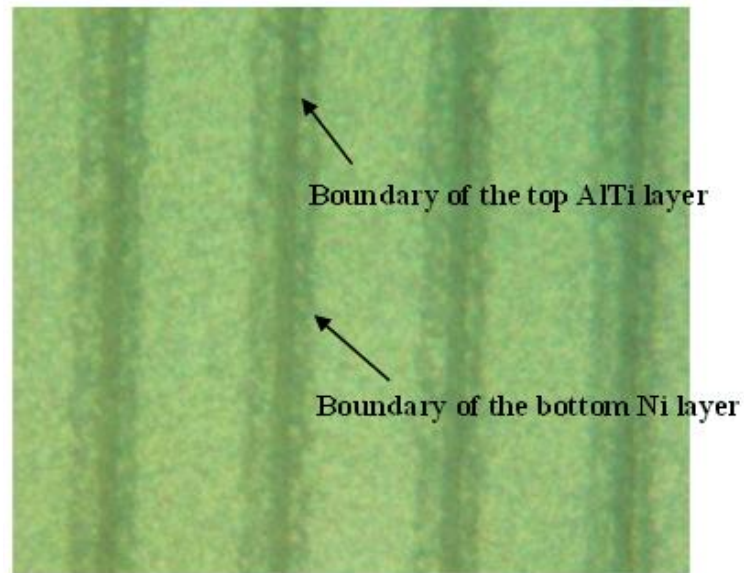
Fig. 5-2 Microphotograph of double metal layer (Ni/AlTi) as RIE etching mask for polysilicon trench formation.

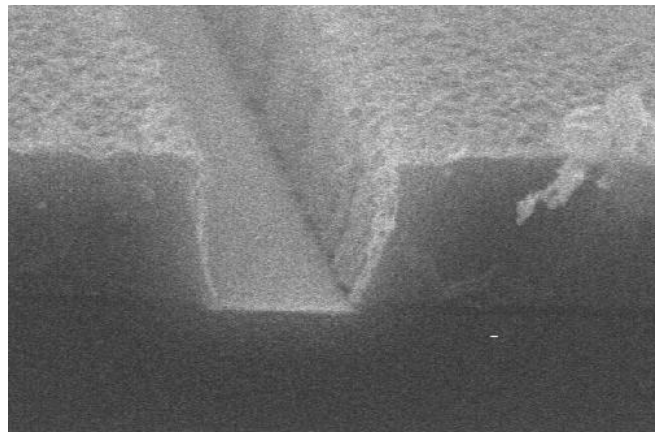## 5.3.2 Uniformity improvement of polysilicon trench depth

RIE etching rate on polysilicon is usually not uniform across the wafer. Consequently it is difficult to determine a uniform stopping time of RIE etching.

A good solution is to place an etch stop underneath the polysilicon layer. Due to the high etching selectivity of polysilicon over SiO_2 in BCl_3/Cl_2 mixture, a process with a thin sacrificial oxide layer as the etching stop has been developed for etch depth uniformity. A thin polysilicon layer (~100 nm) is first deposited on the SiC wafer surface prior to thick polysilicon deposition, followed by a short-time oxidation to completely oxidize the thin polysilicon

layer, creating a ~200 nm thick oxide layer to serve as an etch stop for polysilicon etching. In the RIE process, slight over-etching is allowed to complete the dry etching for all the polysilicon trenches. Meanwhile, the over-etching is stopped by the oxide layer underneath to keep the SiC surface intact (Fig. 5-3a). Eventually, the remaining oxide etch stop at the bottom of the polysilicon trench is readily removed using short-time wet etching by BOE (7:1). The fresh SiC surface is exposed for gate trench etching (Fig. 5-3b).
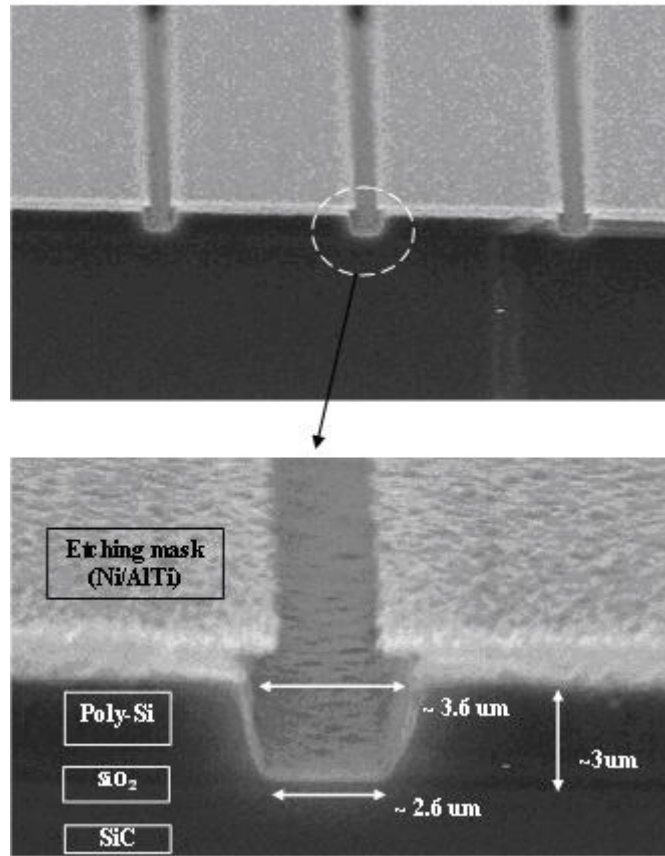
(a) Polysilicon trenches with the oxide at the trench bottom after RIE.

(b) Polysilicon trench with SiC surface at the trench bottom after BOE etching

Fig. 5-3 SEM photo of polysilicon trench after RIE etching and after BOE

etching to remove the oxide etch stop at the trench bottom.

5.3.3   Uniformity improvement of oxidized polysilicon trench width

A long time thermal oxidation is used to oxidize polysilicon trenches and reduce the trench width from 2.6 μm to 0.8 μm for the implantation of submicron vertical channels. The oxidation temperature and time are key parameters to optimize the process.

The polysilicon oxidation is usually conducted at 1100°C to complete the process in a reasonably short time. According to the experimental results, however, many black dots appear after polysilicon oxidation (Fig. 5-4). Due to the concern that this phenomenon might be related to possible crystal damage in this specific process, the oxidation temperature is reduced to 1000°C to eliminate the generation of black dots on the polysilicon surface. The desirable width of the oxidized polysilicon trench was obtained after long-time oxidation of total 39 hrs. No black dots were observed on the polysilicon surface (Fig. 5-5).

As shown in Fig. 5-5, however, the existing problem is that the polysilicon trenches after long-time thermal oxidation seem to be somewhat rounded profile instead of the expected vertical profile. It seems that in the oxidation rate in the polysilicon trench is not uniform along the sidewall. With this polysilicon trench as an implantation mask, the resultant implanted N

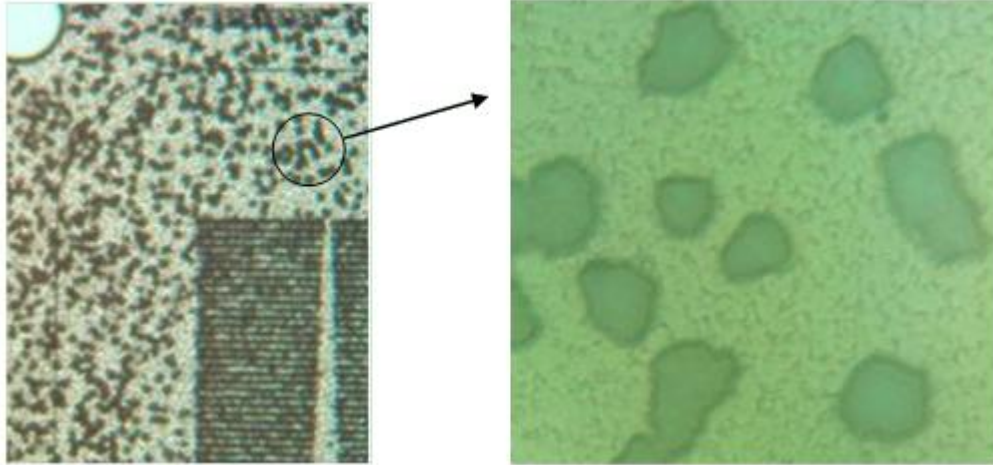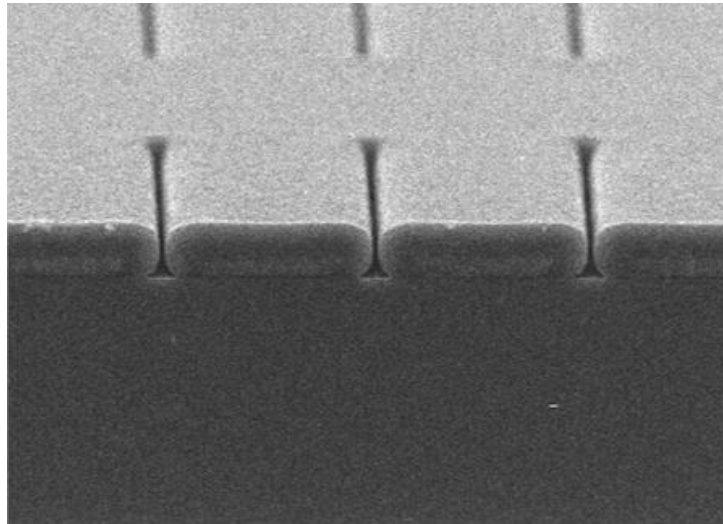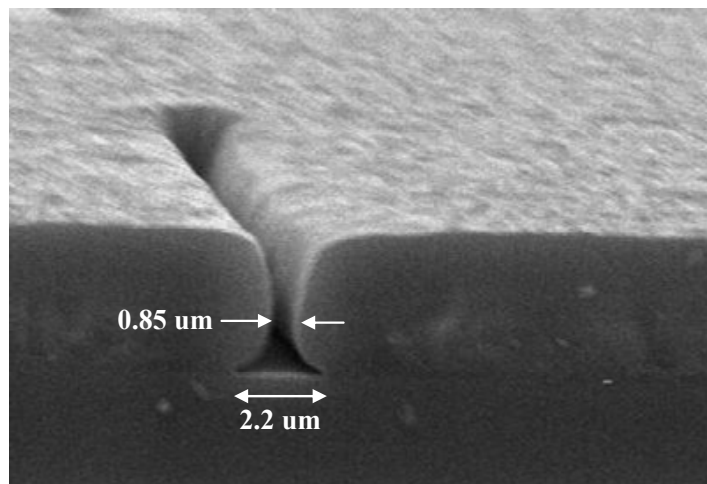channel might be a vertical channel with tapering width instead of uniform width.

Fig.5-4. Microphotographs of polysilicon surface after thermal oxidation at 1100°C.

(a) An array of polysilicon trenches

0.85 um

2.2 um

(b) Magnified polysilicon trench

Fig.5-5. SEM photos of polysilicon trenches after thermal oxidation at $1000^{0}C$ for 39 hrs.

5.4 Process Flow of Vertical Trench-Gate Power MOSFET

The fabrication of vertical trench-gate power MOSFET includes various semiconductor processing techniques including photolithography, metal deposition, plasma etching, RIE, wet etching, ion implantation, oxide growth, polysilicon deposition and insulator deposition. An overview of the fabrication steps are described below and some of the major steps are illustrated in Fig. 5-6.

(a) Formation of alignment marks and mesa (Fig. 5-6(a))

With a metal layer as the etching mask, the alignment marks and mesa are etched by ICP.

(b) Polysilicon deposition (Fig. 5-6(b)).

A thin layer of polysilicon is deposited by LPCVD on the wafer, followed by thermal oxidation to convert the polysilicon into the oxide as the etch stop. Then a 3 μm thick polysilicon layer is deposited.

(c) Polysilicon etching for gate trench mask (Fig. 5-6(c)).

The polysilicon is etched by RIE etching in BCl_3/Cl_2 mixture with a double-layer metal as etching mask.

(d) Gate trench formation for accumulation channel with specified thickness (Fig. 5-6(d)).

Gate trench is etched by ICP with polysilicon trenches as etching mask.

(e) Thermal oxidation of polysilicon trenches for implantation mask (Fig. 5-6(e)).

The oxide expands on the polysilicon trench sidewalls in the long-time thermal oxidation and reduces the polysilicon trench width to submicron dimensions for implantation mask.

(f) Deep nitrogen implantation for vertical channels (Fig. 5-6(f)).

High-energy to low-energy implantation with the mask made of oxidized polysilicon trenches.

(g) Post-implantation annealing (Fig. 5-6(g)).

It is used to activate the implanted ions.

(h) Source trench formation for P body contact and N source contact (Fig. 5-6(h))

Source trenches are created by ICP etching with a double-metal layer as etching mask.

(i) Formation of junction termination extension (Fig. 5-6(i)).

Three-step JTE is formed by ICP etching with photoresist or metal as etching masks.

(j) Thermal oxidation for gate oxide (Fig. 5-6(j)).

Gate oxidation is performed using a "sandwich" process including nitric oxide growth, dry O_2 growth, and nitric oxide annealing.

(k) Open windows in the oxide for source and body contact (Fig. 5-6(k)).

Windows are opened in the oxide with hardbaked photoresist as wet-etching mask.

(l) P body contact formation (Fig. 5-6(l)).

P body contact is formed by AlTi/Ni deposition and a lift-off process.

(m) Source contact formation (Fig. 5-6(m)).

Source contact is formed by Ni/TiW deposition and a lift-off process.

(n) Drain contact formation and RTA (Fig. 5-6(n)).

Drain contact is formed by a full-area deposition of AlTi/Ni, followed by RTA for ohmic contacts

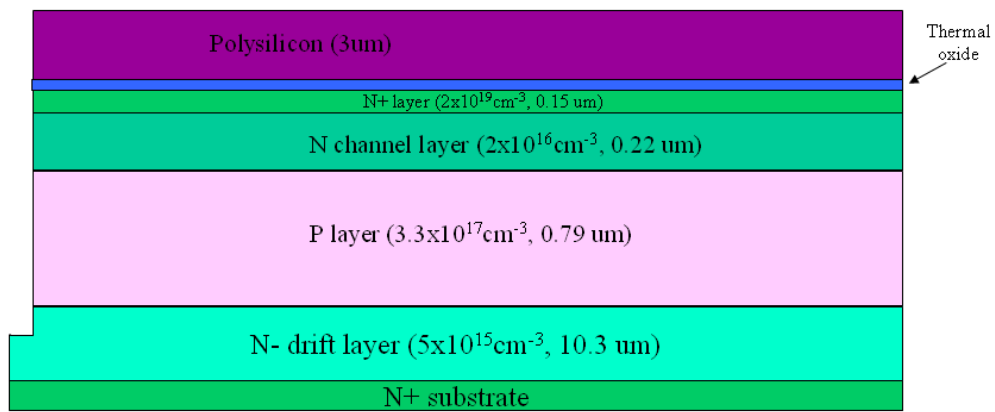(o) Gate contact formation (Fig. 5-6(o))

Gate contact is formed by deposition of Mo and subsequent wet etching.
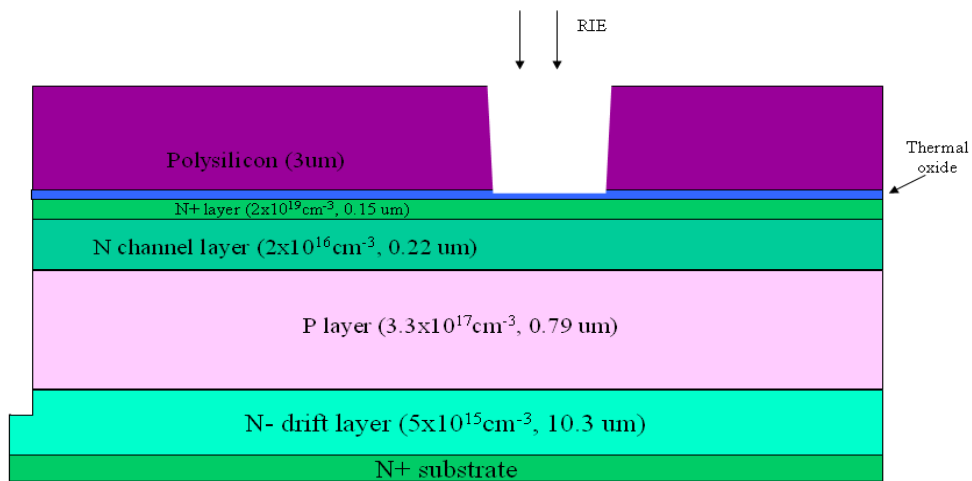
(p) Metal overlay formation (Fig. 5-6(p))

The individual source or gate contacts are connected by metal overlay.
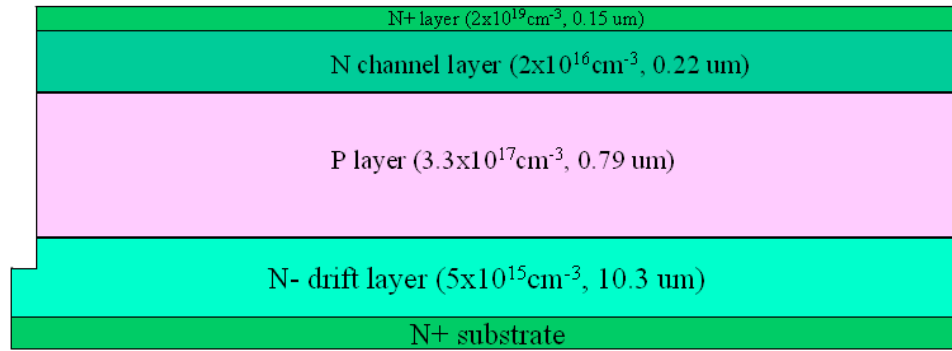
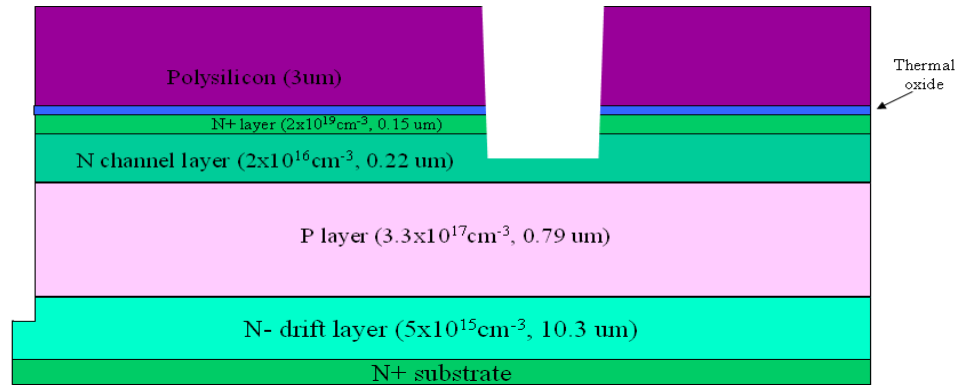
(a) Formation of alignment marks and mesa.
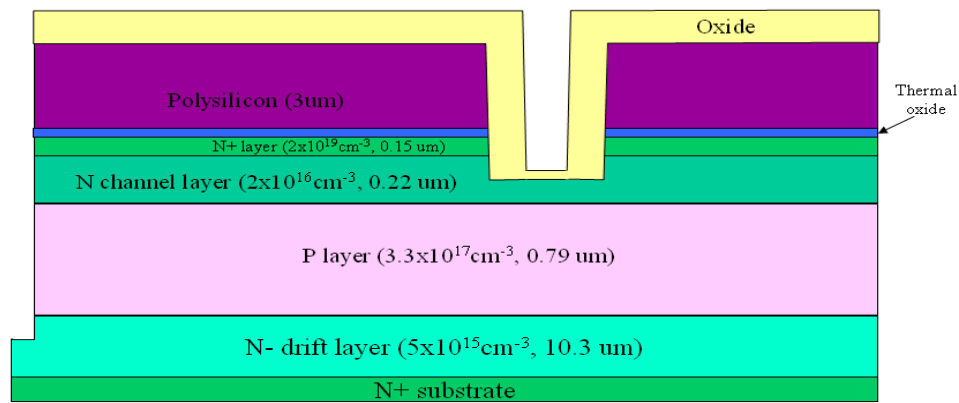

(b) Polysilicon deposition.

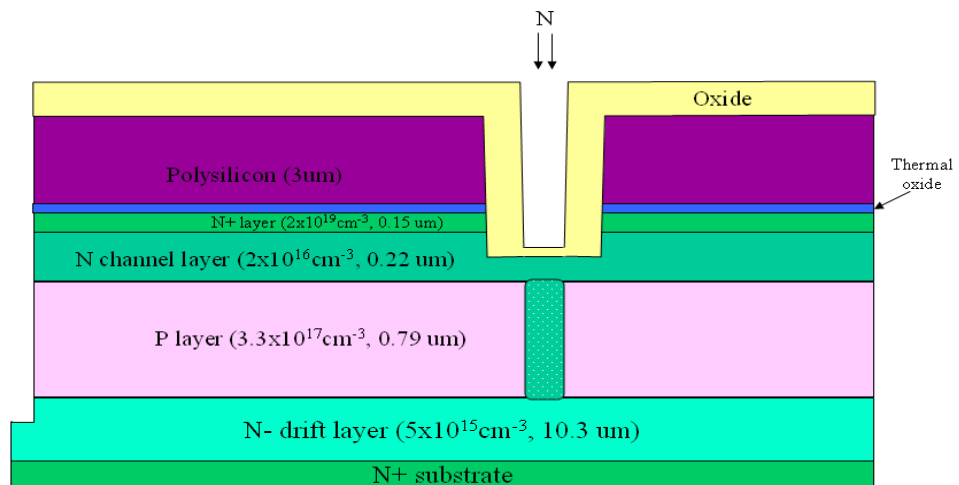(c) Polysilicon etching for gate trench mask.

Fig.5-6. Process flow of vertical trench-gate power MOSFET.

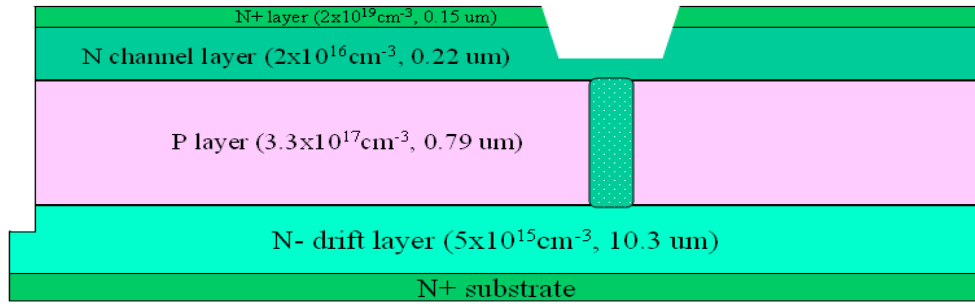(d) Gate trench formation for accumulation channel.

(e) Thermal oxidation of polysilicon trenches for implantation mask.
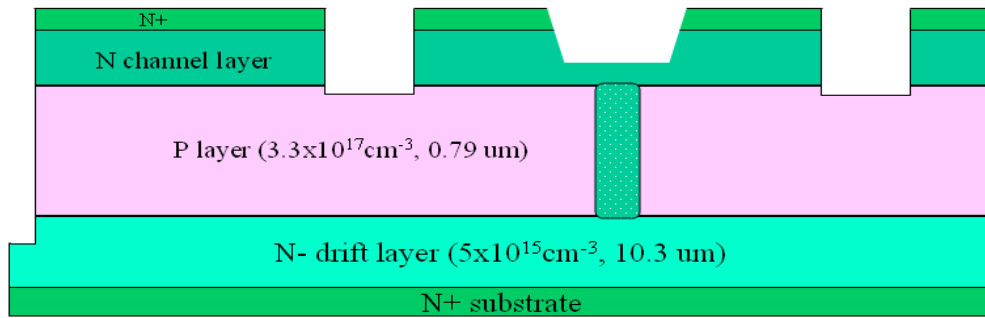

(f) Deep nitrogen implantation for vertical channels.
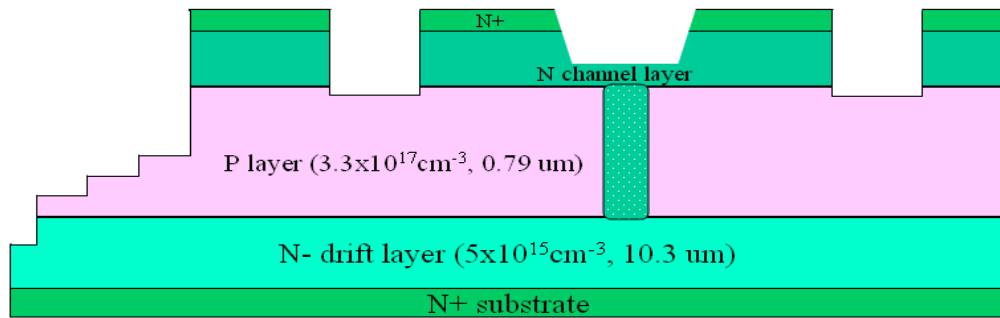
Fig.5-6. Process flow of vertical trench-gate power MOSFET (continued).

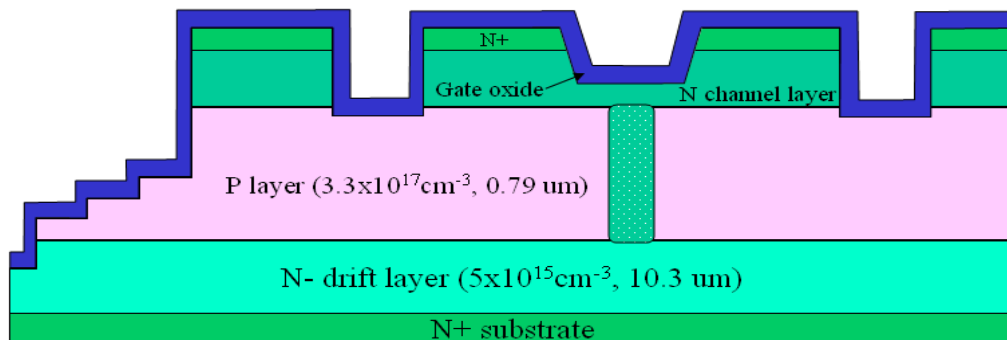(g) Post-implantation annealing.

(h) Source trench formation.

(i) Formation of junction termination extension.

(j) Gate oxidation.

Fig.5-6. Process flow of vertical trench-gate power MOSFET (continued).
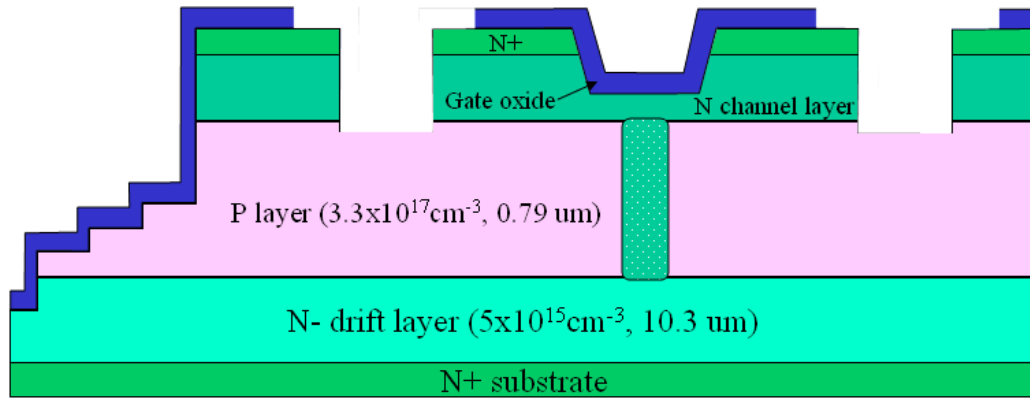
(k) Open windows in the oxide for source and body contact.
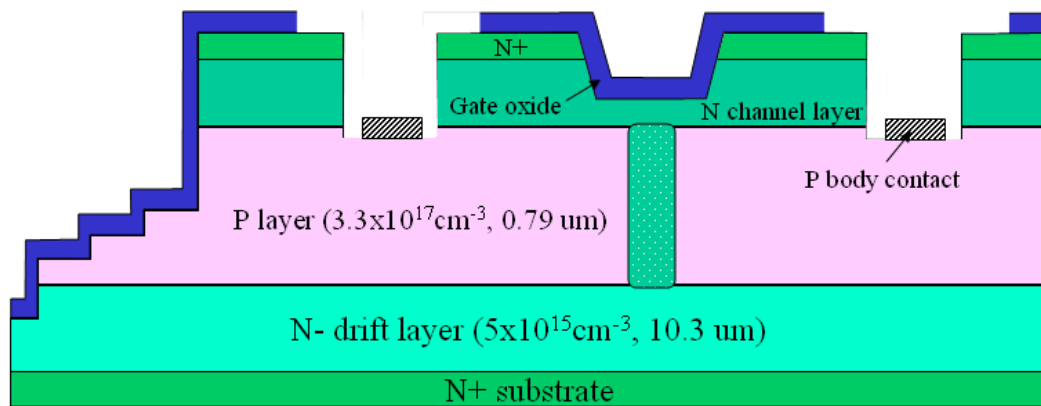
(l) P body contact formation.
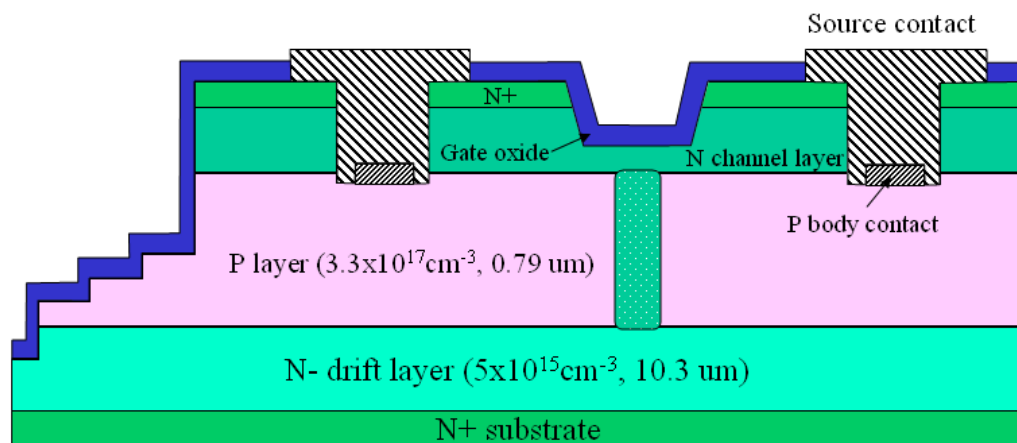
(m) Source contact formation.

Fig.5-6. Process flow of vertical trench-gate power MOSFET (continued).

(n) Drain contact formation and RTA annealing.

(o) Drain contact formation and RTA annealing.
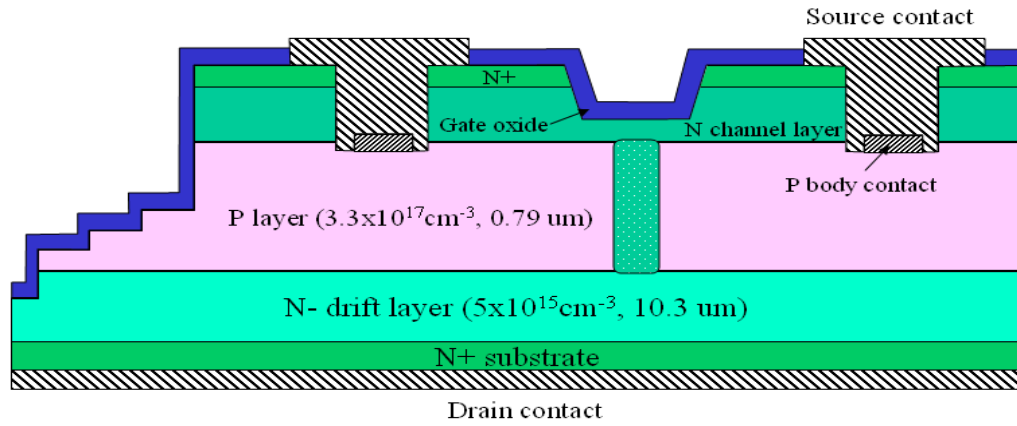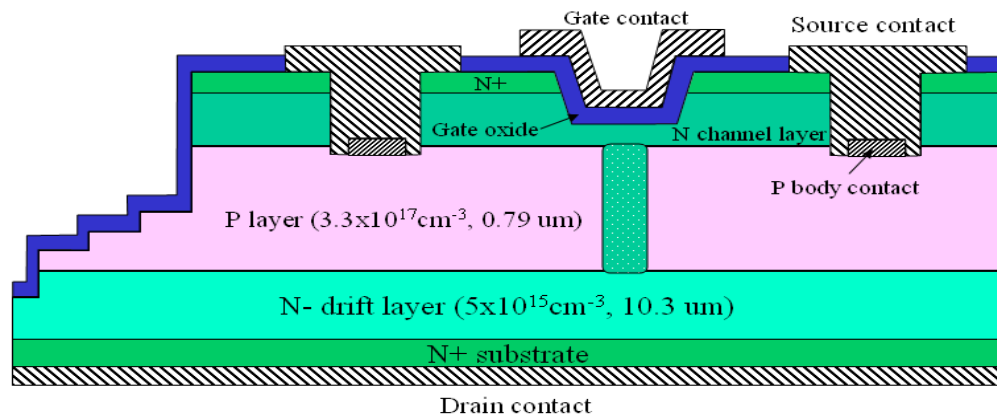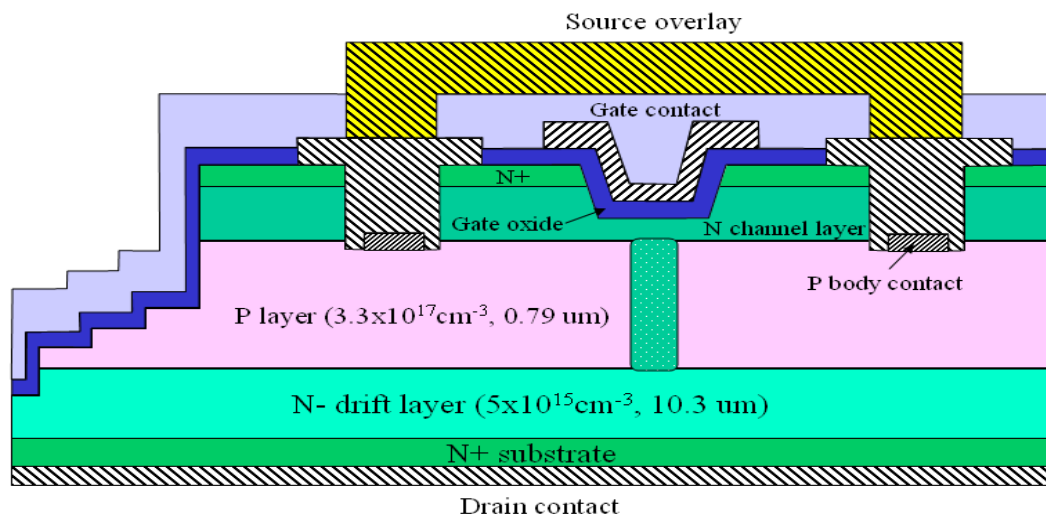

(p) Metal overlay formation.

Fig.5-6. Process flow of vertical trench-gate power MOSFET (continued).

Chapter 6   Fabrication of Vertical Trench-Gate Power MOSFET

6.1 Wafer Specifications

Two 4H-SiC 2-inch 8° off-axis Si face wafers, purchased from Cree, Inc., were processed to fabricate the vertical trench-gate power MOSFETs.

The starting wafer MV1 has an initial 0.22 μm thick N-type epilayer with a doping concentration of $2x10^{16}$ cm^{-3} as the buried channel on top of a 0.79 μm $3.3x10^{17}$ cm^{-3} doped P-type epilayer and a highly doped N$^+$ cap epilayer (0.15 μm, $N_d=2x10^{19}$ cm^{-3}).

The wafer structure is important to determine the etching depth of gate trenches, the implantation depth of vertical channels, and the etching depth of source trenches. To confirm the wafer structure, SIMS analysis was performed at a spot on the wafer MV1, where aluminum impurities were analyzed to a depth of 1.5 μm with detection limits of $2x10^{13}$cm^{-3} (Fig. 6-1(a)). The total thickness of N$^+$ and N layers was found to be slightly thicker than the wafer specifications provided by Cree, Inc., and a P-type epilayer has a lower doping than the specification (Table 6-1).

Similarly, SIMS analysis was also performed on the other wafer for both nitrogen and aluminum impurities (Fig. 6-1(b)), and is compared to the original specification in Table 6-2.

Table 6-1. Comparison of wafer specifications by Cree Inc. and SIMS (MV1).

	Layer1	Layer2	Layer3	Layer4	Layer5 (top layer)
Original Specification	N-type 1e18 cm^{-3} 0.5u	N-type 5e15 cm^{-3} 10.30u	P-type 3.3e17 cm^{-3} 0.79u	N-type 2e16 cm^{-3} 0.22u	N-type 2e19 cm^{-3} 0.15u
SIMS	N/A	N/A	P-type 1.49e17 cm^{-3}	N-type 0.40u	

Table 6-2. Comparison of wafer specifications by Cree Inc. and SIMS (MV2).

	Layer1	Layer2	Layer3	Layer4	Layer5 (top layer)
Original Specification	N-type 2e18 cm^{-3} 0.5u	N-type 7.1e15 cm^{-3} 11.0u	P-type 3e17 cm^{-3} 0.8u	N-type 2e16 cm^{-3} 0.2u	N-type 2e19 cm^{-3} 0.15u
SIMS	N/A	N-type 1e16 cm^{-3}	P-type 4e17 cm^{-3} 0.8u	N-type 1.6e16 cm^{-3} 0.19u	N-type 2.4e19 cm^{-3} 0.13u
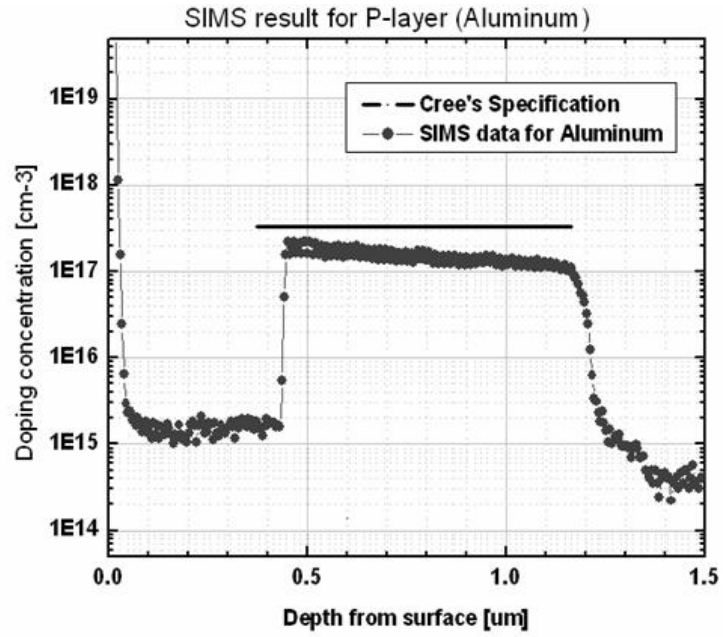
(a) Aluminum doping profile in wafer MV1.
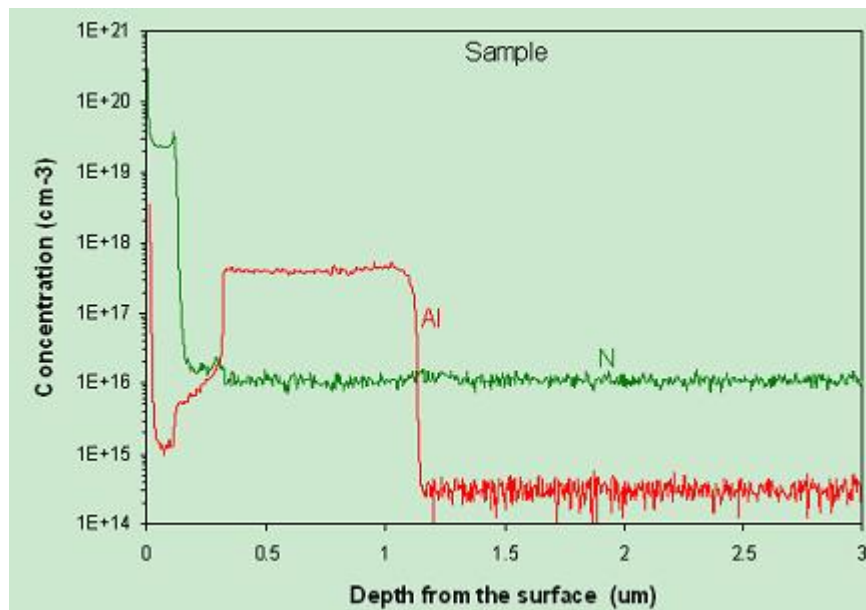
(b) Nitrogen and aluminum doping profile in wafer MV2.

Fig.6-1. Impurities profiles by SIMS.

6.2 Formation of Alignment Marks and Mesas

This step is intended to form cross-like patterns distributed between devices for the alignment in the later photolithography processes and create the mesas for isolation between devices. In order to effectively prevent pinholes, a double-layer metal scheme was used to form dry etching mask. Alignment mark patterns were formed by ICP etching.

A full wafer cleaning process was conducted to remove any possible residuals or particles on the wafer surface.

The first metal layer of 20 nm AlTi and 150 nm Ni was deposited by sputtering, and then patterned by photolithography and lift-off. The thin layer of AlTi serves as a buffer layer to improve adhesion of the Ni etching mask to the SiC surface. The second layer of 300 nm AlTi was deposited to cover possible pinholes in the first metal layer and then patterned with photolithography and wet etching using phosphoric acid and diluted hydrofluoric acid. After removing the photoresist using photoresist stripper, the exposed SiC surface was etched by ICP in CF_4/O_2 mixture to a depth of 1.5 μm. After ICP etching, the metal masks were all removed by RCA acid. The alignment marks that were formed are shown in Fig. 6-2.
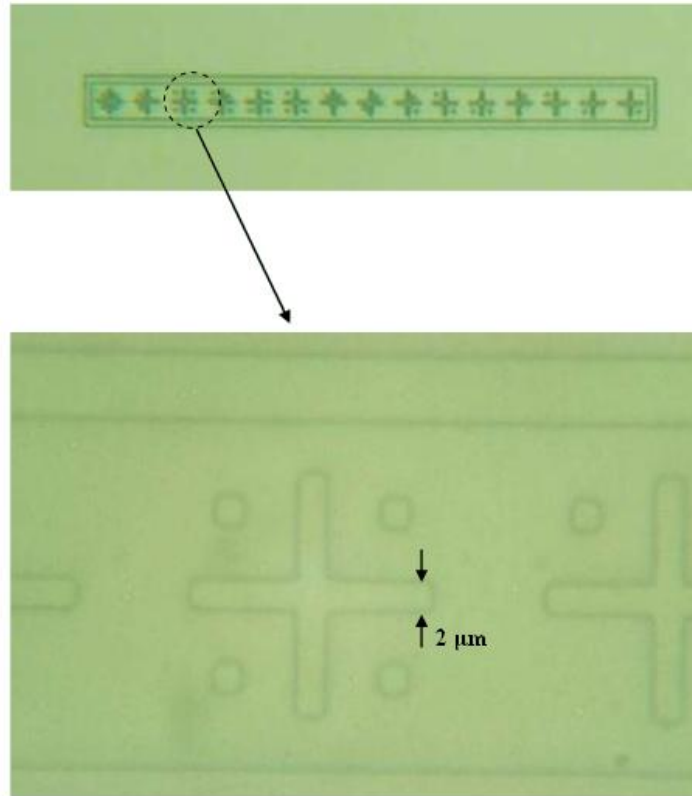
Fig. 6-2. Microphotograph of alignment marks on the SiC wafer.
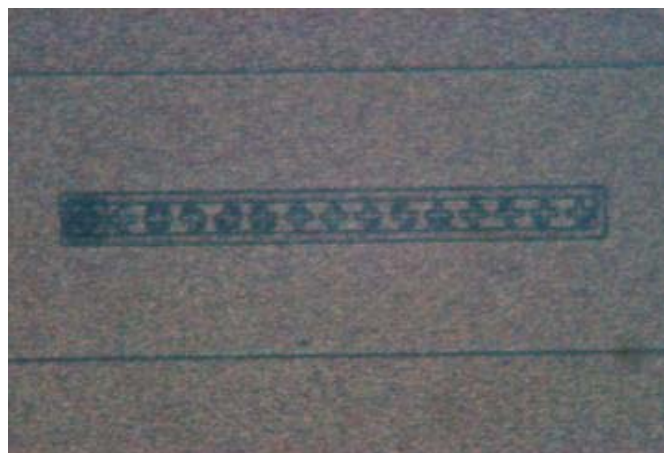
Fig. 6-3. Microphotograph of thick polysilicon deposited on the SiC wafer.

6.3 Polysilicon Deposition

A thick polysilicon layer serves as the dry etch mask for gate trench formation as well as the self-aligned implantation mask for vertical channels after the treatment of oxidation. Based on implantation simulation, the polysilicon layer of 3 μm thick is required to block the dopants. In addition, a thin layer of thermal oxide underneath the polysilicon is needed as an etch stop in the RIE of polysilicon due to the high etching selectivity of polysilicon over thermal oxide.

The process completed in MEMS and Nanotechnology Exchange are as follows: 100 nm thick undoped polycrystalline silicon was first deposited by LPCVD, following a thermal wet-oxidation at 1000°C for 3 hours to completely convert the initially deposited polysilicon into approximately 200 nm thick oxide as the etch stop. Finally, a thick layer of undoped polysilicon of 3 μm was deposited by LPCVD as the implantation mask. Fig. 6-3 shows the rough surface of the thick polysilicon deposited on the SiC wafer.

6.4 Polysilicon Etching

Polysilicon was etched in BCl_3/Cl_2 mixture by MEMS and Nanotechnology Exchange. According to the series of experiments stated in Chapter 5, the double-metal layer (Ni/AlTi) was formed first as drying

etching mask to obtain the vertical polysilicon trench and effectively prevent pinholes (Fig. 6-4 (a)). Due to the high etching selectivity of polysilicon over oxide, the dry etching is expected to be stopped in the middle of the sacrificial oxide layer. After removing the metal mask by RCA acid, the oxide etch stop at the bottom of polysilicon trench was removed using short-time wet etching by BOE, and the fresh SiC surface was exposed (Fig. 6-4 (b)).

The etching process of polysilicon was divided into several runs to check the etching status. Fig. 6-5 (a)(b) show the microphotographs of the circular windows across the wafer after the last etching run. It is seen that the etching was not uniform and polysilicon residuals can still be observed. During the wet etching of the oxide, however, all these polysilicon residuals appearing on top of the oxide were completely removed so that the fresh SiC surface was exposed for next processing.
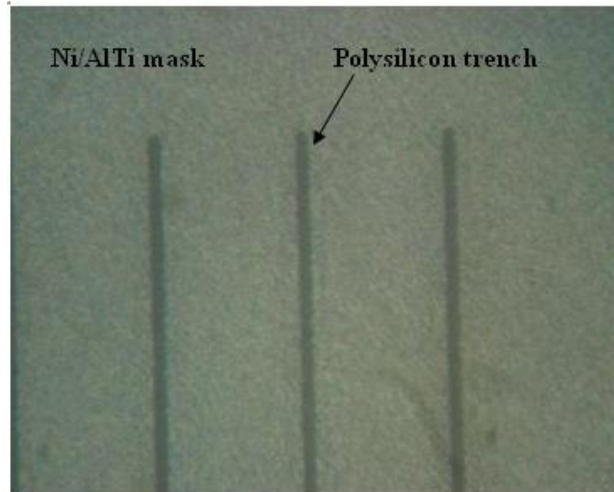
(a) Before RIE etching of polysilicon with Ni/AlTi mask.
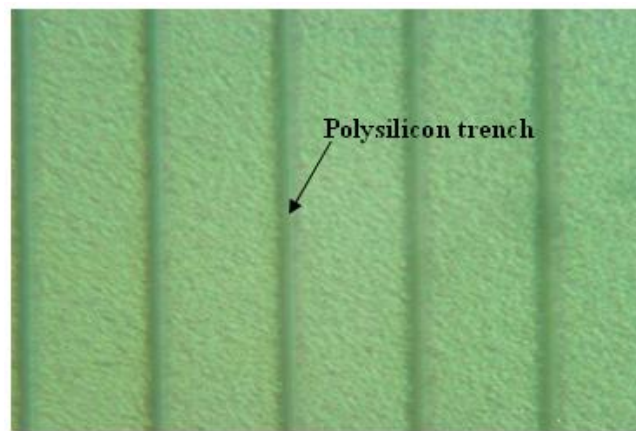
(b) After RIE etching of polysilicon (Ni/AlTi mask and sacrificial oxide at the

trench bottom have been removed).

Fig. 6-4. Microphotograph of polysilicon trenches.

(a) Alignment circle close to wafer edge

(b) Alignment circle close to wafer center

(c) Alignment circle after removing metal mask and sacrificial SiO$_2$
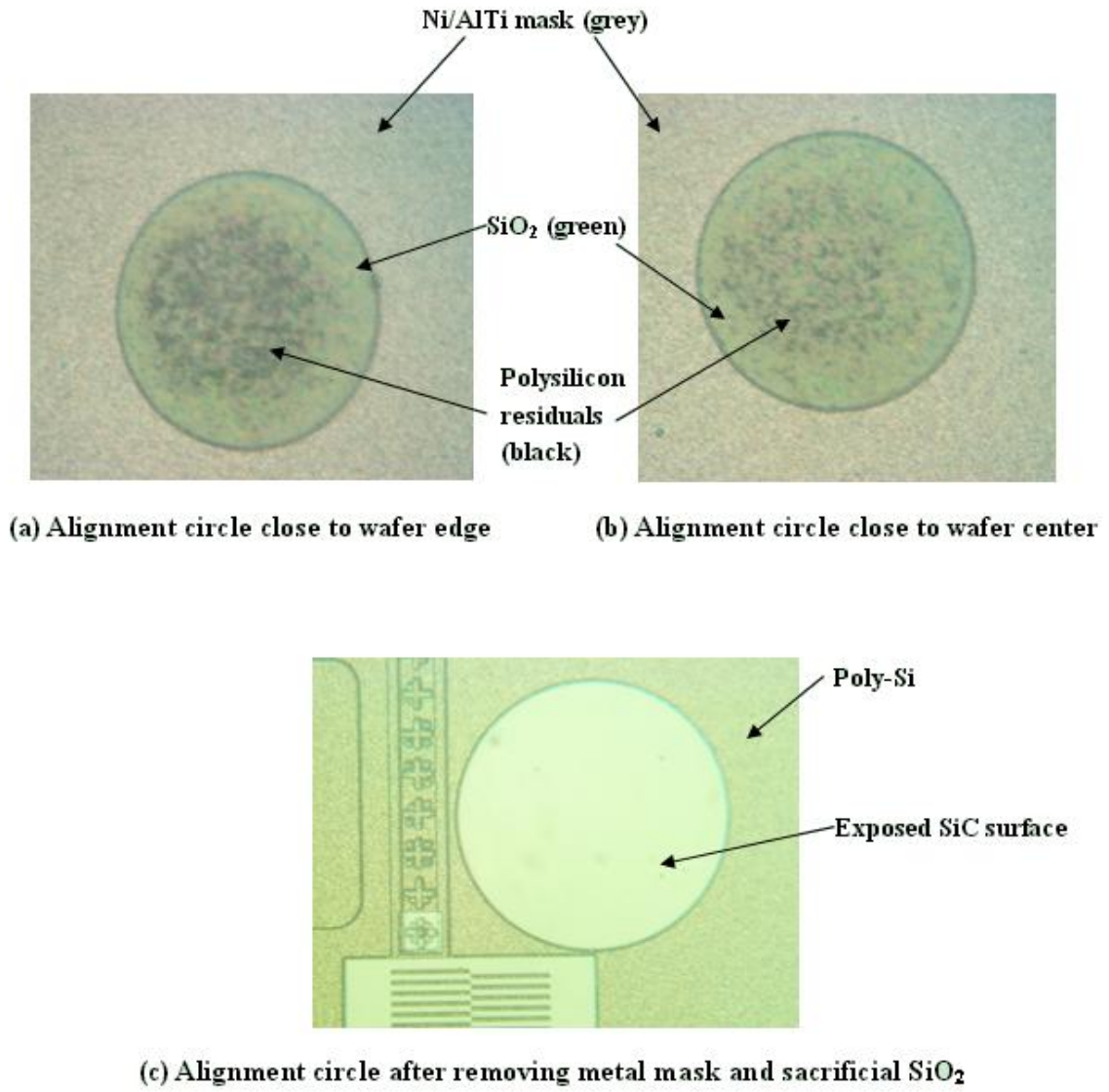
Fig. 6-5. Microphotographs of polysilicon residuals and exposed fresh SiC surface after wet etching of sacrificial oxide.

6.5 Gate Trench Formation

This step is intended to form gate trenches and accumulation channels with specified thicknesses.

With the polysilicon trenches as etching mask, gate trenches can be formed by ICP etching. The wafer was divided into three regions to apply different etching times for different accumulation channel thicknesses of 0.09 μm, 0.12μm, 0.15 μm. The accurate etching depth on each region was determined from the SIMS data of the wafer. In addition, the consumption of SiC in polysilicon oxidation and gate oxidation had to be taken into account, which were estimated to be 100 nm and 50 nm respectively based on the experiments. Hence a total 150 nm of SiC consumption had to be deducted from the expected etching depth. Three different etching times were applied to three different regions for gate etching. When one of the regions was exposed to the etching plasma, other regions were protected by a patterned thick AlTi layer.

6.6 Thermal Oxidation of Polysilicon for Implantation Mask

This step is intended to make a self-aligned implantation mask for vertical N channels through P base layer. The vertical channel width is one of the key parameters strongly affecting forward on-resistance as well as the

electric field in the gate oxide when reverse biased. According to the device simulation results, the vertical implanted channel with $N_{imp}=5.0 \times 10^{17} cm^{-3}$ and $W_{vc}=0.90$ μm will make a good trade-off between forward current density and blocking performance and limit the oxide field to around 4MV/cm. Considering the lateral spread of ion implants, the target channel opening is conservatively set as 0.6~0.8 μm.

Following the gate trench etching, the wafer was cleaned by RCA acid, and then was placed in the oxidation tube for thermal oxidation. With the oxide expanding on the polysilicon trench sidewall, the width of polysilicon trench was reduced. Since the polysilicon trench was as wide as 3.6 μm after RIE etching, it took a long time of 39 hours to obtain the required width to serve as self-aligned implantation mask.

After the long-time oxidation, the wafer was taken out and inspected by SEM. It is seen that the trench width is not uniform even along the same trench (Fig.6-6 (a)(b)). For wafer MV1, the widest trench opening is ~0.85 μm and the narrowest trench opening is ~0.6μm, which fall in the required range. However, the trench openings on wafer MV2 show more deviation on in Fig. 6-6(b), where the widest trench opening is ~0.6 μm and the narrowest trench opening is ~0.2μm. Although the smaller width of vertical channels may further reduce the electrical field in the gate oxide and favor the blocking

performance, it might result in the increased on-resistance and even pinched-off channels at some locations. Moreover, the other problem is that the oxidized poly-Si trenches had a rounded profile (Fig.5-5) instead of a vertical profile. Consequently the vertical channels formed by nitrogen ion implantation could have a tapering width with respect to the channel depth, which might affect the blocking performance of the devices.
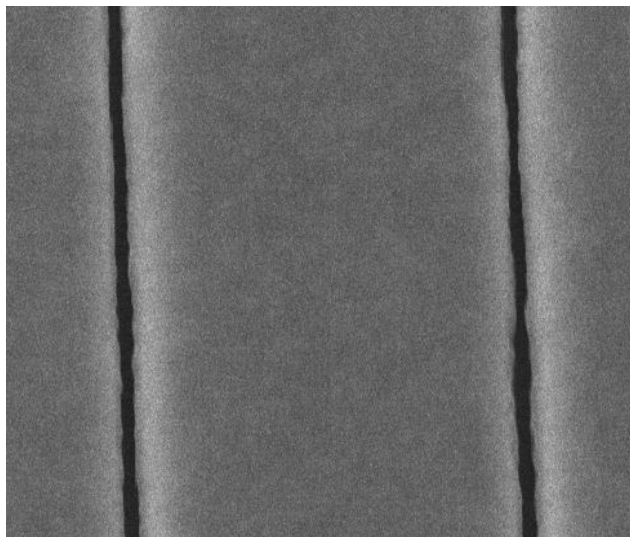
(a) Polysilicon trenches on wafer MV1.
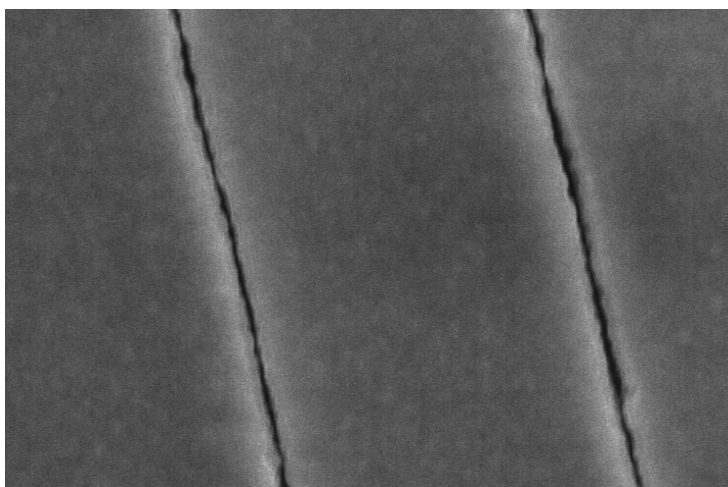
(b) Polysilicon trenches on wafer MV2.

Fig. 6-6. Top view of polysilicon trenches after the long-time oxidation.

6.7 Deep Nitrogen Implantation for Vertical Channels

The deep nitrogen implantation creates N-type conductive vertical channels through the P-type epilayer. SIMS results were used in design implantation profiles for the wafers. The deep nitrogen ion implantation was performed at the University of Western Ontario in Canada.

The implantation profile was designed and simulated using ProfileCode^{TM}. The simulated implantation profile is shown in Fig.6-7. Ten successive nitrogen implants, with the maximum energy of as high as 1.99 MeV, created the resultant vertical N channel with an average doping of 7.22×10^{17} cm^{-3} (N_d-N_a = 5.22×10^{17} cm^{-3}). The detailed nitrogen dose and energies are listed in Table 6-3. The nitrogen ion implantation was conducted at room temperature with normal incidence.

The implantation depth was determined by SIMS results along with the thickness of the oxide grown on the SiC wafer at the trench bottom, which was measured to be 270 nm in test structures. If the implantation depth is too small to penetrate the P layer, the resultant vertical channels would not be conductive, and hence no forward currents would be possible. On the other hand, implantation much deeper than the P epilayer thickness would introduce nitrogen implants of high dose into the N drift layer of low doping, resulting in premature breakdown in the blocking mode. Thus the

implantation depth needs to be accurately designed to penetrate the P epilayer. The simulation has shown that a sufficient depth of 1450 nm can penetrate the top oxide, accumulation channel layer and P-type epilayer to form the required vertical N channels.

Table 6-3. Deep nitrogen ion implantation for vertical channels.

	Energy (keV)	Dose (cm^{-2})
Nitrogen ion implantation	1990	9.2e12
	1850	8.8e12
	1510	7.7e12
	1220	7.2e12
	960	6.8e12
	760	6.2e12
	590	5.9e12
	460	5.9e12
	350	6.0e12
	250	5.1e12

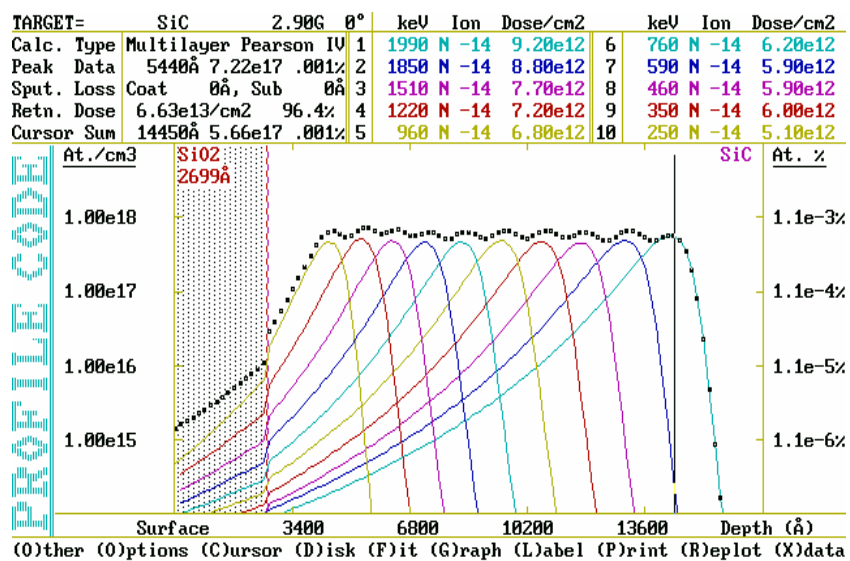| TARGET=		SiC	2.90G	0°	keV	Ion	Dose/cm2		keV	Ion	Dose/cm2
Calc. Type	Multilayer Pearson IV			1	1990 N	-14	9.20e12	6	760 N	-14	6.20e12
Peak Data	5440Å 7.22e17 .001%			2	1850 N	-14	8.80e12	7	590 N	-14	5.90e12
Sput. Loss	Coat 0Å, Sub 0Å			3	1510 N	-14	7.70e12	8	460 N	-14	5.90e12
Retn. Dose	6.63e13/cm2 96.4%			4	1220 N	-14	7.20e12	9	350 N	-14	6.00e12
Cursor Sum	14450Å 5.66e17 .001%			5	960 N	-14	6.80e12	10	250 N	-14	5.10e12

Fig.6-7. Box profile of the deep nitrogen implantation for vertical channels.

6.8 Post-Implantation Annealing

Post implantation annealing is intended to activate ion implants and repair radiation damage.

A complete cleaning process prior to the activation annealing is required to remove the oxide and thick polysilicon layer on the top of the wafer. The wafer was soaked in the BOE (7:1) solution for 6 hours to remove the oxide grown on the sidewalls and the bottom of the polysilicon trenches (Fig. 6-8a).

Subsequently the thick polysilicon layer on the wafer frontside and the polysilicon stains on the wafer backside were completely removed by the wet etching using KOH solution. It is seen in Fig. 6-8b that the side wall of the gate trench is actually tapering at an angle of about 25 degrees, instead of having a sharp corner. This tapering sidewall may help soften the potential lines curvature at the trench corner and reduce the electric field crowding.

After a standard RCA cleaning, the wafer was placed face down on a polished 4H-SiC substrate and loaded into a graphite crucible, the inner of which was filled with pure SiC powder. The annealing was performed in a high-temperature box oven in ultra-high purity argon ambient. In an effort to prevent surface degradation due to high-temperature annealing, the annealing temperature was chosen to be 1450°C. The wafer surface was checked under microscope before and after nitrogen implantation for comparison (Fig.6-9(a)

and (b)). It is seen that the implant shadows have vanished after activation, indicating the damaged crystal lattice has been restored.

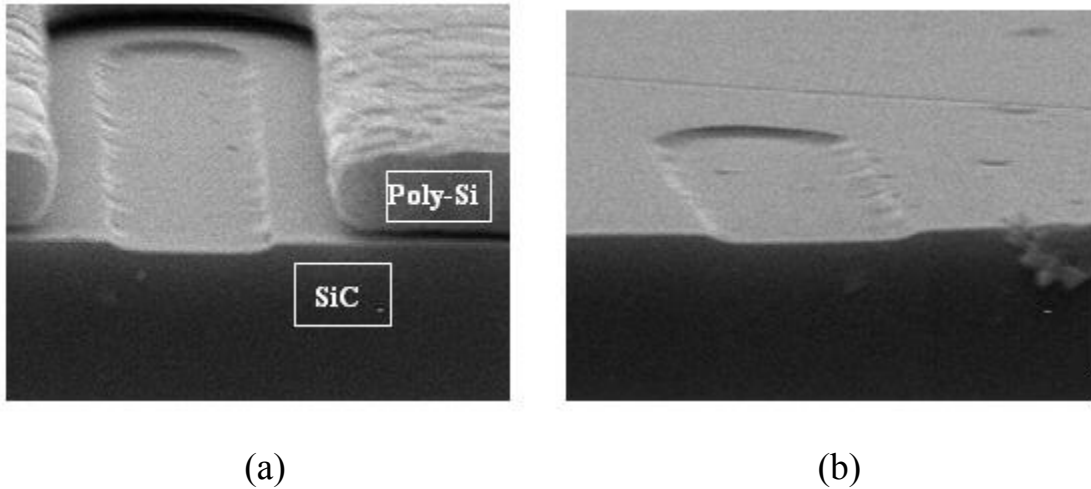(a)   (b)

Fig.6-8. SEM photos of gate trenches (a) with the oxide removed (b) with polysilicon layer removed, showing a tapering shallow sidewall.

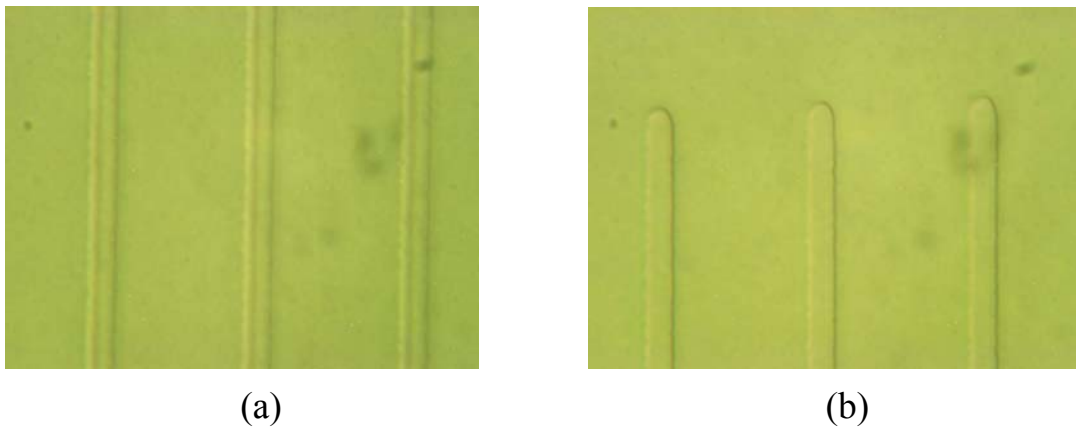(a)   (b)

Fig.6-9. Gate trenches viewed in back-illumination of microscope (a) before and (b) after the post-implantation annealing.

6.9 Conductivity Testing of Implanted Vertical Channels

This step is intended to use the test structures to verify the conductivity of implanted vertical channels after the activation of implanted nitrogen ions.

The temporary contact metals of AlTi (20 nm)/Ni (300 nm) were deposited on the front surface of the wafer and patterned by photolithography and lift-off. Then the wafer was placed upside down for the deposition of full-area back contact of AlTi (20nm)/Ni (300nm). No ohmic contact annealing was conducted at this stage.

The test structure (Fig.6-10) for conductivity verification was characterized using HP4145B semiconductor parameter analyzer, with the front contact as the anode and the back contact as the cathode. In addition to the test structure with implanted N channels, another test structure without implanted channels (essentially back-to-back PN diodes) was also tested for comparison. Fig.6-11a shows that the test structure without implanted channel only conducts ~10 pA current at a 20 V bias, indicating of the reverse leakage. The device with implanted channel conducts a much higher current of 2.6 mA at 3 V bias (Fig.6-11b). Since the front and back contacts were not annealed for ohmic contacts, the devices could not conduct as much the current as the devices with ohmic contacts. However, by comparing the current levels between the devices with and without implanted channels, it can be safely

concluded that the implanted vertical N channels were conductive after activation annealing process.
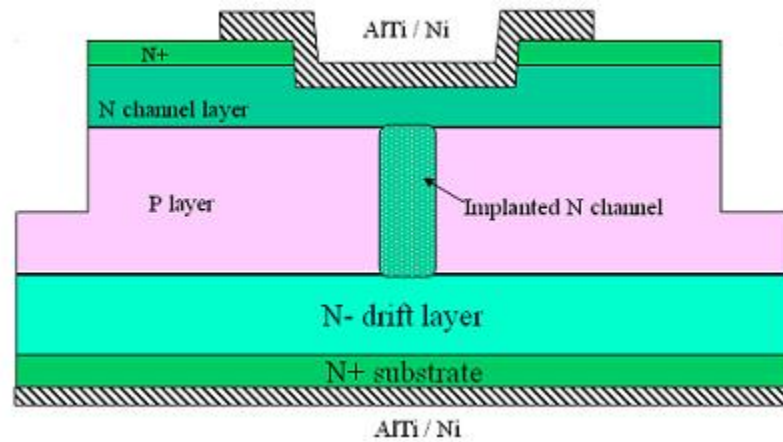

Fig.6-10. Cross-sectional view of the test structure with implanted vertical channel.
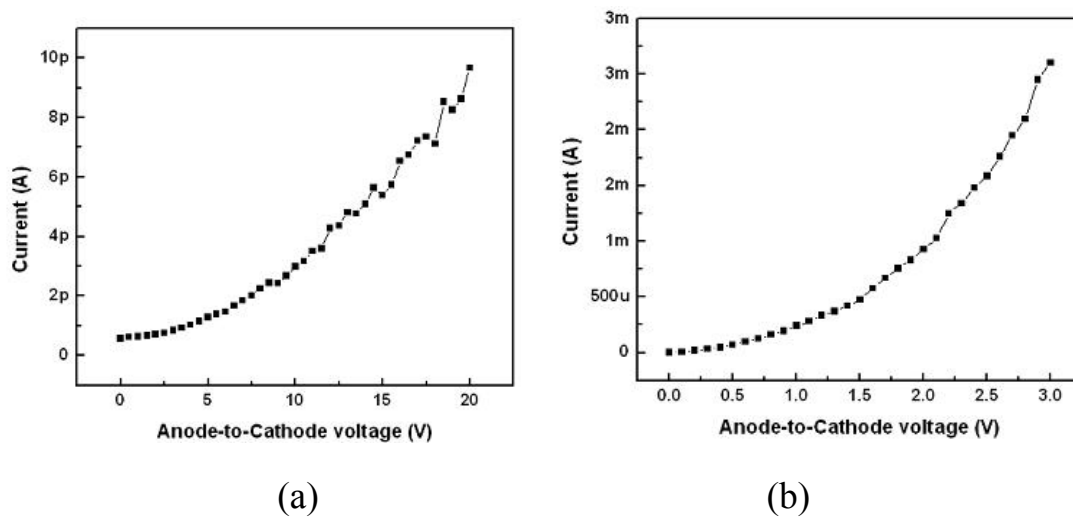

(a)   (b)

Fig.6-11. I-V characteristics of test structures (a) without implanted channel (b) with implanted channel.

6.10 Source Trench Formation

Unlike in the traditional DMOSFETs, the P-type epilayer in the vertical trench-gate MOSFET is buried underneath the N^+ cap layer and the N channel layer. Hence dry etching is needed to etch through the top N^+ and N channel layers and stop at the P-type epilayer to form a trench structure. P body contacts can be then deposited into the source trenches and capped by source contacts. In this way, the P body layer is grounded along with the source contact, eliminating the possible problem of floating potential.

Due to the difficulty in forming the dry-etching mask with a small linewidth of 2.5 μm, a double-layer metal mask was formed by a dual wet etching process for ICP etching. The double-layer metal (250 nm thick AlTi with 300 nm thick Ni on top) was deposited on the wafer, followed by two photolithography processes. The first photolithography process defined the patterns in the hardbaked photoresist for the wet etching of the Ni layer. Using standard nickel etchant (Type-TFB), the Ni layer was over-etched intentionally in case any possible Ni residuals exist in the trench regions. Subsequently the second photolithography process was performed with the same mask to define the exact dimensions of source trenches with a strictly controlled exposure time. With the hardbaked photoresist as the wet etching mask, the AlTi layer was patterned using standard aluminum etchant Al etch

II (with surfactant), followed by diluted hydrofluoric acid to clean any possible AlTi residuals. This double-layer etching mask can accurately define the small source trench dimensions as well as effectively prevent the pinholes on the dry etching mask. The double-layer etching mask formed on the wafer is shown in Fig.6-12. The target etching depth of source trenches was determined to be 450 nm by SIMS data, making source trench slightly etched into the P layer.
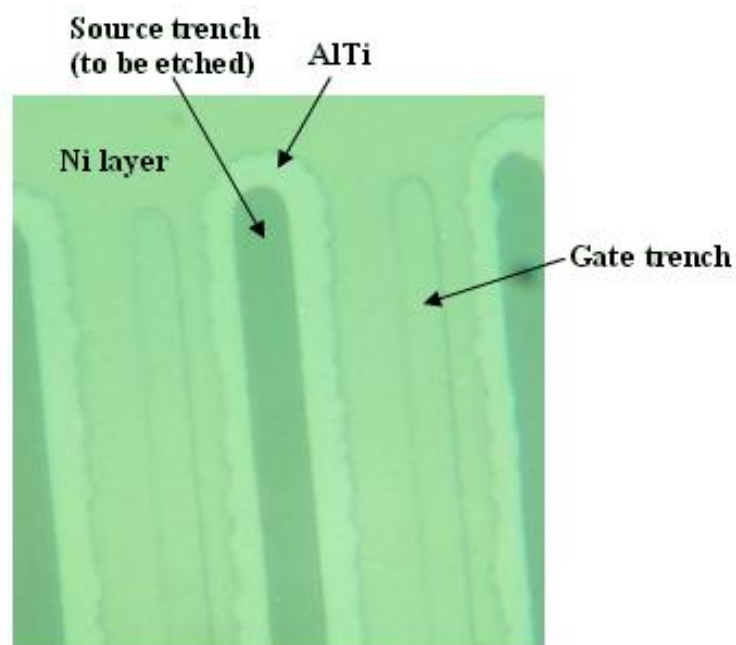

Fig.6-12. Microphotography of double-layer Ni/AlTi as dry etching mask for source trench formation.

6.11 MJTE Edge Termination

This step is intended to form the three-step junction termination extension on device periphery to reduce electric field crowding and improve the device breakdown voltage.

The parameters of MJTE structure were optimized on small-area test diodes on the same wafer and were later reproduced on the real devices. The schematic cross-sectional view of a test diode with no implanted vertical channels shown in Fig.6-13.

A full cleaning process was first conducted on the wafers to remove any possible contamination or residuals. The MJTE processing stared from the formation of JTE3. Since the JTE3 is a shallow step, ICP etching was conducted using the photoresist AZ5214E as dry etching mask patterned by standard photolithography. The etched depth was about 30 nm. Afterwards the photoresist etching mask was removed by photoresist stripper. JTE2 was formed by the same process for the similar etching depth.

The JTE1 formation involves a series of repeated "etching and testing" cycles to identify the optimum JTE1 depth such that the JTE test diodes could achieve the highest breakdown voltage and lowest reverse leakage. The JTE fabrication started from the patterning of the photoresist AZ5214E by an image reversal photolithography process. Subsequently the double-layer

metal AlTi (20 nm)/Ni (300 nm) was deposited on the wafer by sputtering, followed by a lift-off process using the photoresist stripper AZ400T to form dry etching mask. Following each run of a small etching step done by ICP, the test diodes were measured under reverse bias to determine the breakdown voltage and the reverse leakage. The JTE1 etching mask was directly used as the front contact. The wafer was immersed in Fluorinert oil for testing in case of any air sparking under high electric field. All the measure results were plotted and compared in Fig.6-14. The optimum JTE1 depth was about 410 nm, at which the test diodes could block up to 1530 V. It is seen that the highest blocking voltage achieved by JTE diodes is close to the theoretical breakdown value based on the actual wafer structure from SIMS data.
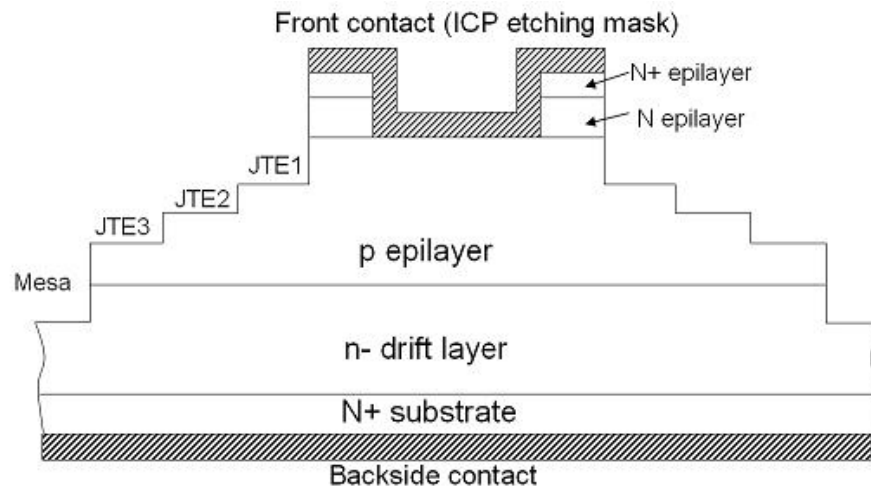
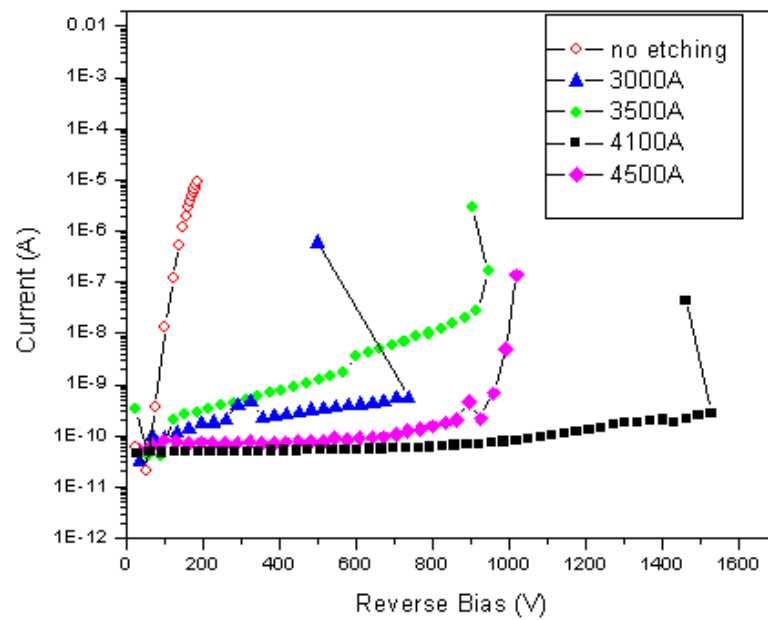Fig.6-13. Cross-sectional view of test diode with MJTE structure.

Fig.6-14. Blocking results of JTE test diode.

6.12 Gate Oxidation

High density of interface states in 4H-SiC MOSFETs may result in the low MOS channel mobilities. A promising "sandwich" oxidation process (nitric oxide growth, dry O_2 growth, and nitric oxide annealing) has been found to be able to grow high quality gate oxide and reduce the density of interface states.

Prior to the gate oxidation, the quartz tube of the oxidation system was cleaned using TransLC at 1100^oC for 6 hrs. The gate oxidation procedure started with a thorough cleaning of the samples. After the JTE metal etching mask was removed from the wafer by RCA acid, the following successive chemical process was conducted for a full cleaning:

(a) H_2SO_4 (100%) at 80 °C for 20 min;

(b) Diluted HF (15%) with ultrasonic agitation for 10 min;

(c) RCA basic ($NH_4OH:H_2O_2:H_2O$=1:1:5) at 80 °C for 20min;

(d) RCA acid ($HCl:H_2O_2:H_2O$=1:1:6) at 80°C for 20min;

(e) Diluted HF (5%) with ultrasonic agitation for 5 min.

Subsequently the cleaned wafers were thermally oxidized at 1100°C for 30 minutes in wet oxygen ambient to form a sacrificial oxide with a thickness of about 10 nm. The sacrificial oxidation may reduce defects density on the

SiC surface introduced by previous fabrication steps. After the wafers were taken out of the furnace, the sacrificial oxide layer was removed by diluted HF (15%) with ultrasonic agitation for 20 minutes.

With the fresh SiC surface exposed, the wafer was placed back to the oxidation tube for a long-time gate oxidation, i.e., a series of growth/annealing processes described in Table 6-4. The microphotographs of the devices after the gate oxidation are shown in Fig.6-15. The gate oxide thickness was measured to be 105 nm by wet etching the test structures on the wafer, part of which were protected by the hardbaked photoresist.

Table 6-4. Gate oxidation process.

Operation	Gas ambient	Temperature (^{o}C)	Duration (hours)
Ramp up	nitrogen	–	1.5
NO oxidation	Nitric oxide	1175	4
NO annealing	Nitric oxide	950	3
Ar purge	argon	1175	0.5
Dry O2 oxidation	oxygen	1175	7
Ar purge	argon	1175	0.5
NO annealing	Nitric oxide	1175	4
NO annealing	Nitric oxide	1050	4
NO annealing	Nitric oxide	900	4
Ramp down	nitrogen	–	1
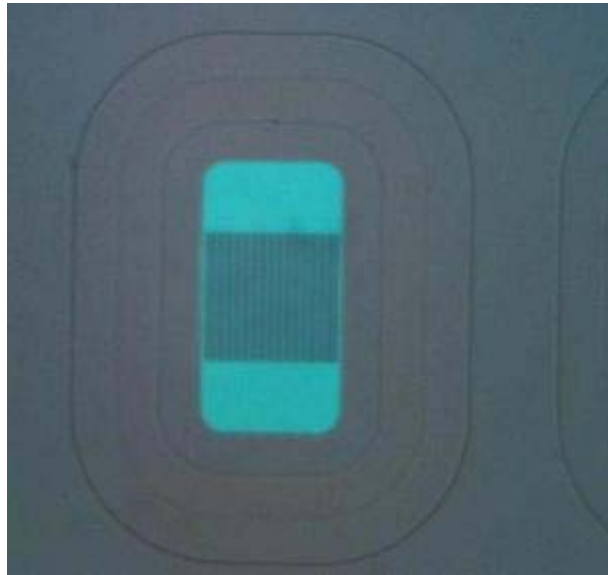
(a)
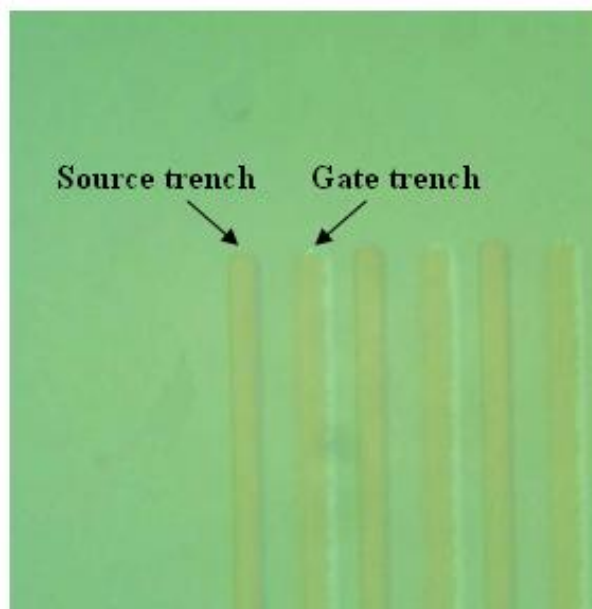
(b)

Fig.6-15. Micrographs of the devices after gate oxidation (a) small MOSFET

(b) gate trenches and source trenches.

6.13 Open Oxide Window for Source and Body Contact

This step is intended to open the windows in the oxide for the formation of the P body contact, the source N contact and the drain contact.

The oxide grown on the backside of the wafers, where the drain contact would be deposited, was first removed using diluted hydrofluoric acid with the front surface protected by the hardbaked photoresist. Subsequently the photoresist on the wafer frontside was removed by photoresist stripper.

After etching away the oxide on the wafer backside, the windows were opened in the oxide on the wafer frontside by wet etching for the body contact and the source contact. The wet etching mask was formed by hardbaked photoresist using standard photolithography. Subsequently the exposed oxide was cleaned by a series of short-time wet-etching steps using BOE (7:1) to avoid the undercut in the oxide window. The micrograph of the windows opened in the oxide is shown in Fig. 6-16a.

6.14 Body Contact Formation

In the MOSFET structure, the P-base region needs to be short-circuited to the N^+ source region to eliminate a floating potential. Although in silicon MOSFETs such short-circuiting can be readily done by depositing the same

contact metal for both the source and body regions, different contact metals for source N-type regions and body P-type regions are required in SiC MOSFETs to achieve the low contact resistance individually.

The P body contact formation started from the photolithography to define the locations of P body contacts. In order to ease the subsequent lift-off process, no photoresist hardbaking was performed. A double-layer metal of AlTi(20nm)/Ni(100nm) was deposited by sputtering into the middle region of the exposed source trench. Prior to the sample being loaded into the sputtering chamber, it was dipped into dilute hydrofluoric acid to remove any possible thin oxide layer in the exposed source trench. The lift-off process was carried out by photoresist stripper. The micrograph of the P body contacts is shown in Fig. 6-16b.

6.15 Source Contact Formation

The source N contact completely covers the source trench as well as the P body contact on the bottom of the source trench. A different metal scheme of Ni (30 nm)/TiW(100 nm) was deposited as the source contact. Similar to P body contacts, source N contacts were formed by lift-off process. The micrograph of the source contacts is shown in Fig. 6-16c.

6.16 Drain Contact Formation and RTA

The drain contact was a full-area metal layer formed on the wafer backside. A photoresist layer was spun on the wafer and softbaked to protect the front. Following a dip in diluted hydrofluoric acid, the wafer was placed upside down in the sputtering chamber for the deposition of AlTi (20 nm)/Ni (300 nm). The photoresist on the wafer frontside was removed using the photoresist stripper after the metal deposition.

Rapid thermal anneal (RTA) was performed by a high intensity lamp to heat a single wafer in nitrogen form gas ambient (5% H_2 in 95% N_2) to form the source and drain ohmic contacts simultaneously. The anneal temperature was chosen to be relatively low temperature ($\sim950^oC$), in order to prevent the SiO_2/SiC interface from damage that occurs at a high RTA annealing temperature ($>1000^oC$). The detailed RTA process is shown in Table 6-5.

Table 6-5. Rapid thermal anneal process.

Operation	Time (s)	Temperature (^oC)
Purging chamber	1200	25
1st Ramp	5	600
2nd Ramp	125	950
Anneal	300	950
Cooling down	600	-

6.17 Gate Contact Formation

Gate contacts were formed by wet etch process in case that rough metal strip edges by lift-off might cause shorting between the source and drain contacts.

Following a general cleaning on the wafer frontside, a 150 nm thick molybdenum layer was first deposited on the wafer by blanket sputtering. Subsequently a photolithography was carried out to pattern photoresist as wet etching mask, followed by photoresist hardbaking to improve the adhesion of the photoresist to the metal. Subsequently the Mo layer was wet etched using Al etch II solution to form the gate contact. The photoresist was then removed by photoresist stripper. The micrograph of the gate contacts is shown in Fig. 6-16d.
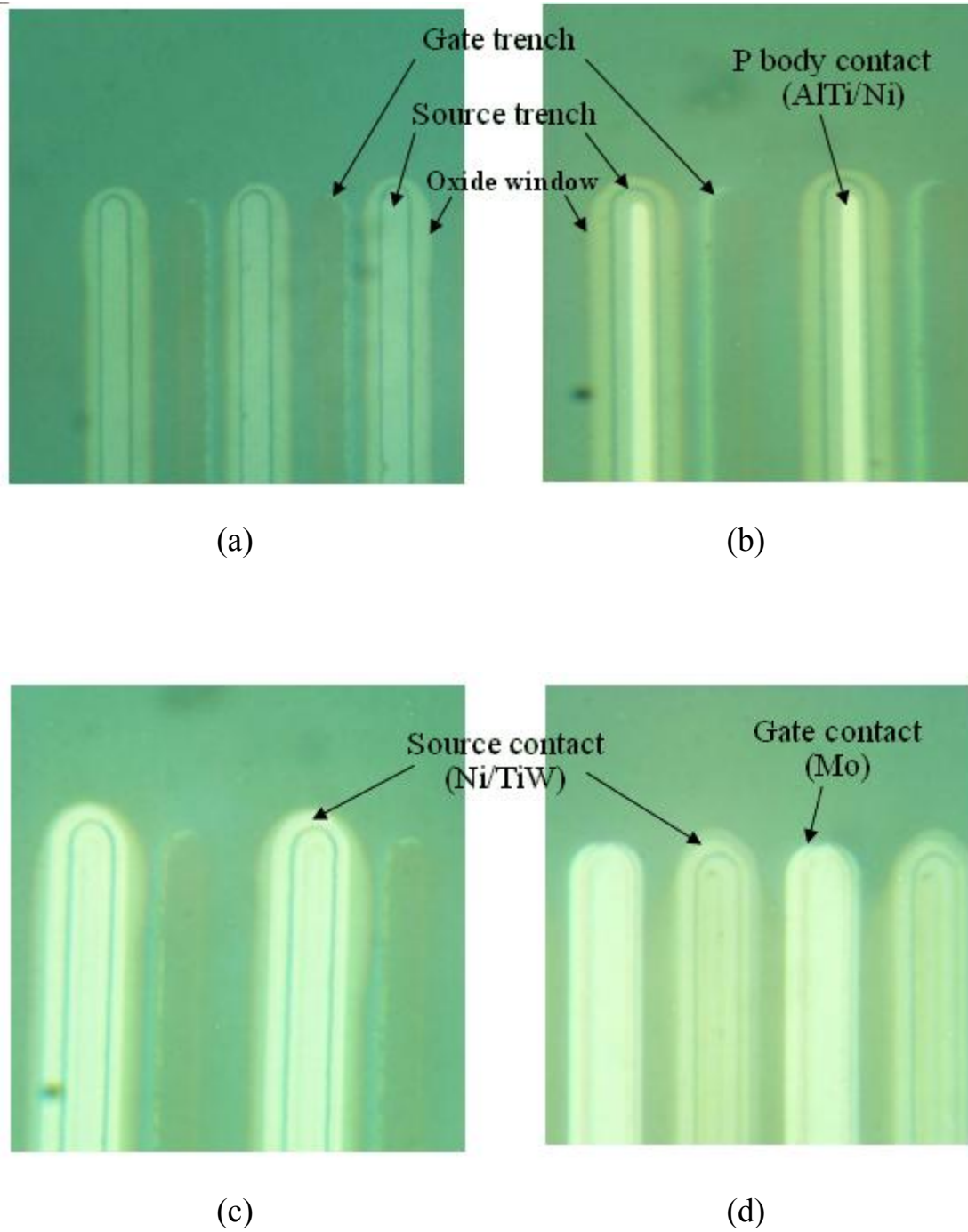
Fig.6-16. Micrographs of contact formation process (a) Open oxide windows (b) P body contact formation (c) Source contact formation (d) Gate contact formation.

6.18 Metal Overlay

This step is intended to electrically connect the gate or source fingers in the same device, as well as to form bonding pads on device periphery for the gate and source respectively.

A thick Al (500 nm)/AlTi (100 nm) layer was first deposited by sputtering and then patterned by photolithography and wet-etching with phosphoric acid. This metal layer was used to connect all of the gate fingers and source fingers in the same device. The thin AlTi layer was used as an etch stop in the later dry etching process of etching through thick SiO_2/Si_3N_4 isolation layer.

Subsequently a thick dielectric layer of 700 nm thick SiO_2 and 300 nm thick Si_3N_4 was deposited by PECVD on the wafer surface for reliable surface isolation. The thick photoresist AZ4400 was patterned by photolithography as dry etching mask. By a series of "etching-measure" cycles, the SiO_2/Si_3N_4 dielectric layer was etched through to expose the source and gate contacts. Following each etching run, the wafer was tested with HP4145B by probing the metal pad areas of the first overlay. Detection of a high conduction current indicates the oxide is etched through. Since the photoresist AZ4400 was only around 3 μm thick and could be consumed during the dry etching, one more photolithography process had to be performed to re-define the dry etching

mask. When the electrical measurement confirmed the SiO_2/Si_3N_4 dielectric layer was etched through, a thick metal layer of 1.5 μm was deposited by sputtering and was patterned by photolithography and wet etching.
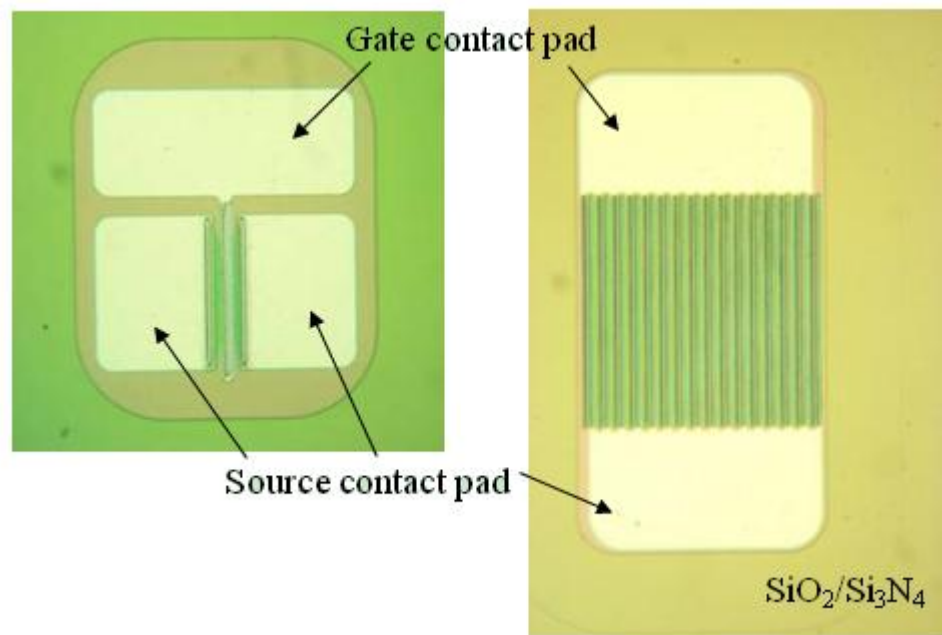

Fig.6-17. Micrographs of metal overlay formation on the single-gate MOSFET and the small-area MOSFET.

# Chapter 7   Characterizaton of Vertical Trench-Gate Power MOSFET

The tested structures and vertical trench-gate power MOSFETs of different sizes were tested at chip level using a standard probe station. The appropriate instruments were utilized for the different characterizations.

## 7.1 Experimental Results of Test Structures

7.1.1   Gate leakage current

The gate-source leakage was first measured on a single-gate MOSFET by HP 4145B semiconductor parameter analyzer to evaluate the quality of the oxide. With the source contact grounded, the gate contact is applied with positive voltages. Experimental results of a single-gate MOSFET on the wafer MV1 is shown in Fig. 7-1a. The maximum voltage applied on the gate is 40 V, which limits the maximum oxide field to be around 4 MV/cm. It is seen that the gate leakage current is only around 1 nA at the oxide field of 4 MV/cm. In Fig. 7-1b, the gate bias on a single-gate MOSFET was applied up to 100 V, corresponding to an oxide field of 10 MV/cm. It is seen that the gate leakage current remains at around 4 nA until the gate bias reaches 90 V, when

a signal of oxide breakdown is observed. It can be concluded that the gate

oxide is of good quality and is able to sustain a high oxide field up to 9

MV/cm.
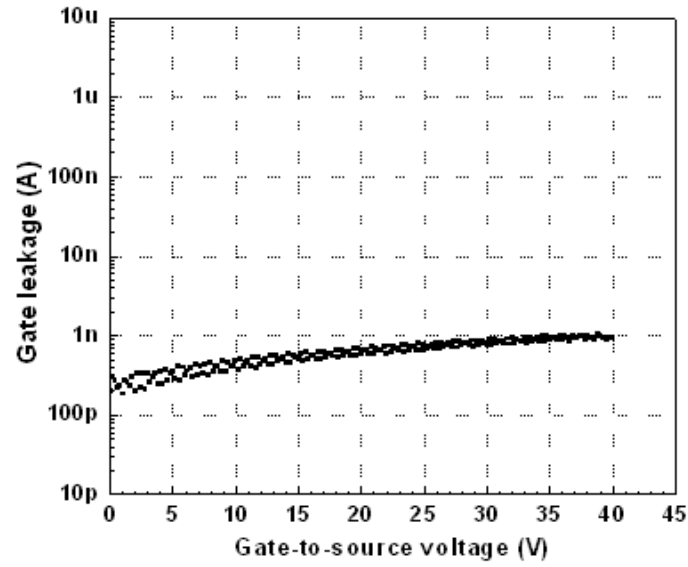
(a)
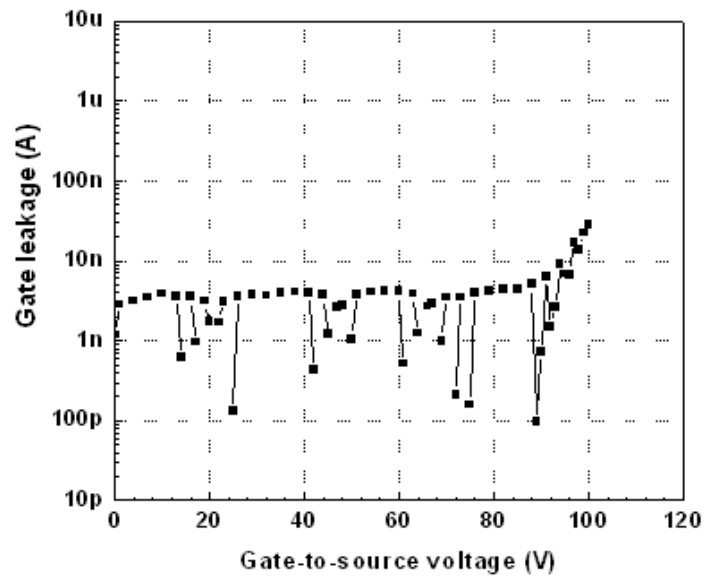
(b)

Fig.7-1. Experimental gate leakage of a single-gate MOSFET on (a) wafer MV1 and (b) wafer MV2.

7.1.2   TLM structure

The specific contact resistances of source ohmic contacts were measured by the Transfer Length Method (TLM). The TLM structure consists of seven TLM contacts (150 x 50 μm^2) in a row with different spacings of 4, 6, 8, 10, 15, 20 and 25 μm. Measurements were conducted using an HP 4145B semiconductor parameter analyzer by probing two adjacent TLM contacts. The I-V characteristics of TLM structures on two wafers are shown in Fig. 7-2a and Fig. 7-3a. The voltage bias was swept from -5 V to +5 V. The slope of each curve was calculated at the voltage drop of 2 V and plotted in Fig. 7-2b and Fig. 7-3b with respect to the spacing between TLM contacts. The specific contact resistance of source ohmic contact region was evaluated based on the theoretical analysis in [56]. In Fig. 7-2b, the slope found by linear fitting is 4.2 $\Omega/\mu m$ and the intercept (R_0) is 26.47 Ω. Using the TLM contact width (W) of 150 μm, the specific contact resistance is evaluated as $\rho_c = (\text{Slope x W})^{-1}(R_0 \text{ x } W/2)^2 = 6.26 \times 10^{-5} \Omega cm^2$. Similarly, the specific contact resistance is evaluated to be $8.5 \times 10^{-5} \Omega cm^2$ from Fig. 7-3b.
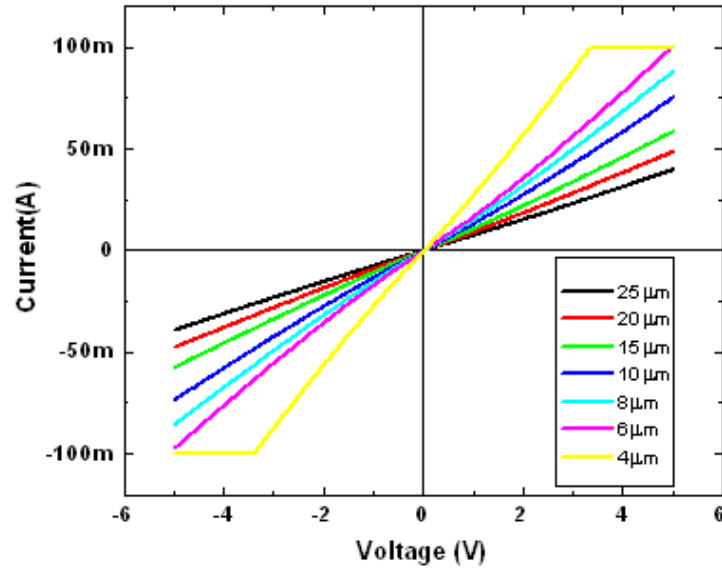
(a) I-V characteristics of the measured TLM structure.
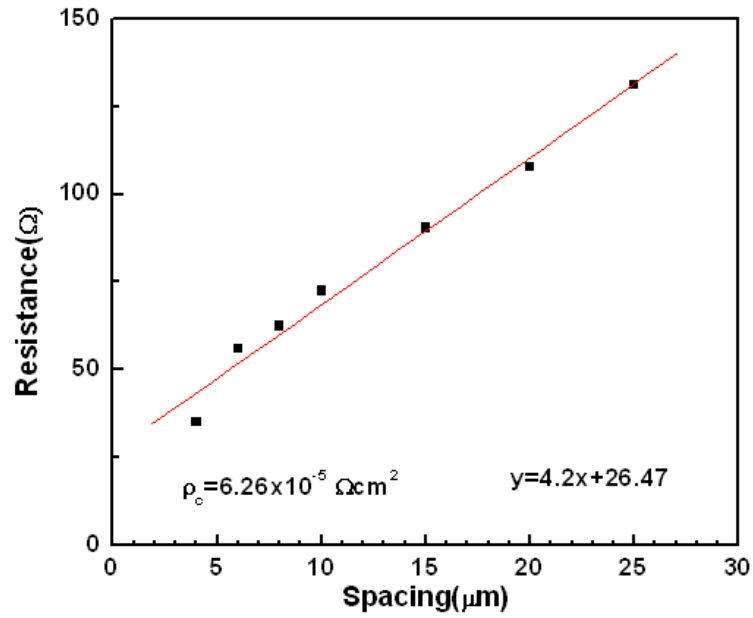
(b) TLM data for the N+ source region.

Fig.7-2. TLM characteristics of the contact resistivity for the N^+ source region on wafer MV1.
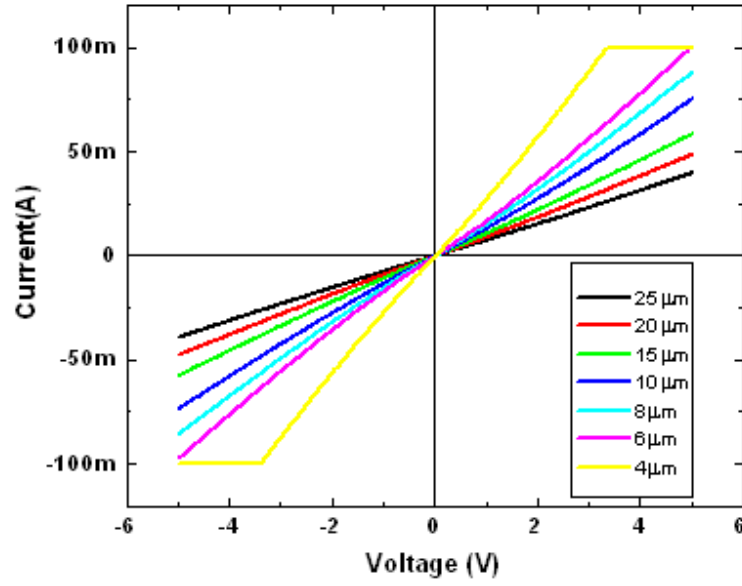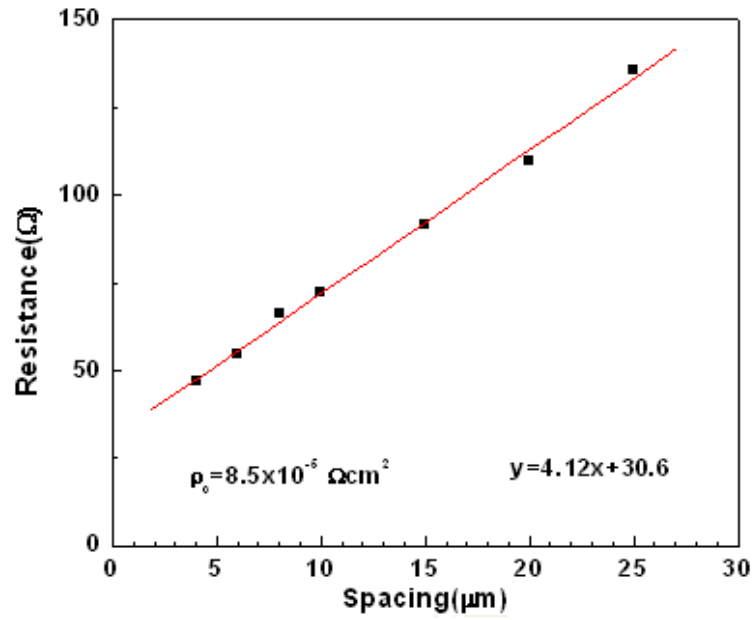
(a) I-V characteristics of the measured TLM structure.

(b) TLM data for the N+ source region.

Fig.7-3. TLM characteristics of the contact resistivity for the N$^+$ source region

on wafer MV2.

7.2 Characteristics of Vertical Trench-Gate Power MOSFETs

7.2.1   Single-gate MOSFET

The single-gate MOSFETs are the devices with the smallest active area of 1.679×10^{-5} cm^2 on the wafers. The forward I-V measurements of single-gate MOSFETs were performed using an HP 4145B semiconductor parameter analyzer. With the source grounded, the drain characteristics were obtained by applying positive voltages to the drain and gate. Fig. 7-4a shows the forward characteristics of a single-gate MOSFET on the wafer MV1. The maximum voltage applied on the gate is 40 V, which limits the maximum oxide field to be around 4 MV/cm. The specific on-resistance is then calculated from the linear portion of the I-V plot. A low specific on-resistance of 9.96 mΩcm^2 was obtained at the gate bias of 40 V and drain current density of 100.4 A/cm^2, which is close to the theoretical value of 8.91 mΩcm^2 extracted from the simulation.

In order to measure the devices under high voltage conditions, the wafer was immersed into Fluorinert^{TM} oil. Forward blocking of the devices on the wafer MV1 was characterized in quasi-DC mode using a 20 kV Glassman high voltage supply and a Keithley 6517A electrometer. Fig. 7-4b shows the blocking characteristics of the single-gate MOSFET measured with both the

source and the gate grounded, i.e., at zero gate-source voltage. It is seen that the device can block the drain-source voltage of 375 V. The FOM (V_B^2 / R_{sp}) of the devices is calculated to be 14 MW/cm^2. For comparison, the theoretical maximum FOM for silicon power MOSFETs is only about 4 MW/cm^2.

The blocking voltage of 375 V is lower than the theoretical value of 1900 V for the drift region doping and thickness utilized, whereas the JTE testing diodes after fabrication could still block up to 1200 V. Two possible reasons could contribute to this low blocking voltage. First, the width of a vertical implanted N channel might not be sufficiently small to provide an effective pinch-off during the reverse bias. Second, the tapering width of vertical implanted channels, resulting from the rounded profile of the polysilicon implantation mask after long-time thermal oxidation, significantly affects the pinch-off at the upper part of vertical implanted channels. The reduced pinch-off of the vertical channels in the blocking mode agrees with the quickly increased leakage current with drain voltage in Fig. 7-4b.

The transfer characteristics of the single-gate MOSFET was measured using the HP 4145B with a constant bias of 50 mV applied across the drain and source. The threshold voltage, V_{th}, extracted from the I_{DS}-V_{GS} transfer characteristics shown in Fig. 7-4c by the linear extrapolation method, is found to be 4.6 V, showing a stable normally-off operation. The drain current in the

transfer characteristics at V_{DS}=50 mV is also plotted in log scale in Fig. 7-4d to illustrate its subthreshold characteristics. The on/off ratio, defined by $\log(I_{DS,ON}/I_{DS}(V_{GS}=0))$, is over three. This indicates that this single-gate MOSFET can operate stably as switching device.

The single-gate MOSFETs on the wafer MV2 were also characterized. The forward I-V characteristics of a single-gate MOSFET were measured using an HP 4145B semiconductor parameter analyzer and are shown in Fig. 7-5a. At the gate bias of 40 V, the specific on-resistance was calculated to be 14.7 mΩcm^2 at the drain current density of 477.2 A/cm^2. This R_{on} is slightly higher compared to that of the single-gate MOSFET on the wafer MV1 (9.96 mΩcm^2). In order to further explore the forward capability of this device, the bias of up to 70 V was applied to the gate, as the gate leakage measurement in Fig. 7-1b has shown that the oxide may sustain a gate bias of up to 80~90 V with no signal of oxide breakdown. At the gate bias of 70 V, the specific on-resistance was calculated to be 9.3 mΩcm^2 at the drain current density of 756 A/cm^2.
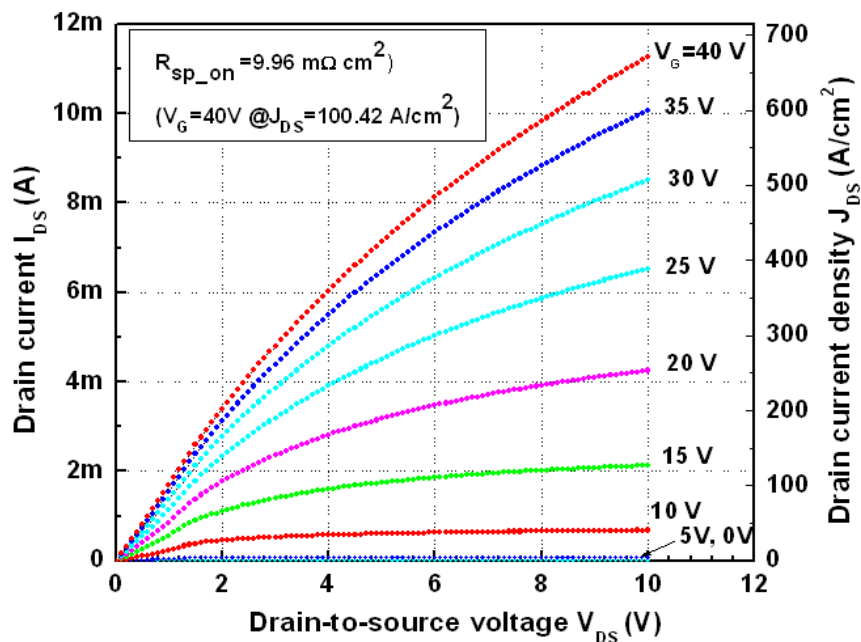
The blocking characteristics were measured using a Tektronix 371A curve tracer with the source and gate grounded (V_{GS}=0 V). Fig. 7-5b shows the device can block a high drain source voltage of 890 V, resulting in an improved FOM (V_B^2/R_{ON}) of 85 MW/cm^2. In addition to the much higher

blocking voltage than that of the device on wafer MV1, this device shows different characteristics of reverse leakage currents. At the breakdown voltage of 890 V, the leakage current is as low as 20 μA. The leakage currents increase slowly with drain voltage. The device was swept into sharp breakdown several times without permanent damage, indicating the gate oxide was effectively protected by pinched-off vertical implanted channels. The measured blocking voltage is about 54% of the theoretical value of 1650 V for the drift region doping and thickness of wafer MV2 from SIMS data.

Compared to the forward and blocking characteristics of the single-gate MOSFET on wafer MV1, the device on wafer MV2 has much improved blocking voltage with a low leakage current but has relatively higher specific on-resistance. Revisiting the fabrication process of these two wafers, we might attribute the discrepancies in the characteristics to the different openings of the vertical implanted channel. After the oxidation of polysilicon trenches, the trench openings on wafer MV2 range from 0.2 μm to 0.6 μm, smaller than those on wafer MV1 (0.6~0.85 μm). The vertical channels with smaller width may increase the specific on-resistance. However they favor the blocking performance by allowing more effective pinch-off in the channels.

The I_{DS}-V_{GS} transfer characteristics of the single-gate MOSFET on wafer MV2 were also measured with a constant drain voltage of 50 mV using an HP

4145B. Using the linear extrapolation method, the threshold voltage, V_{th}, is extracted from the transfer characteristics and found to be 5.1V, demonstrating stable normally-off operation. The subthreshold characteristics of the device are shown in Fig. 7-5d. The on/off ratio, defined by $\log(I_{DS,ON}/I_{DS}(V_{GS}=0))$, is also found to be over three, indicating this single-gate MOSFET can operate stably as switching device.

(a) Forward characteristics.
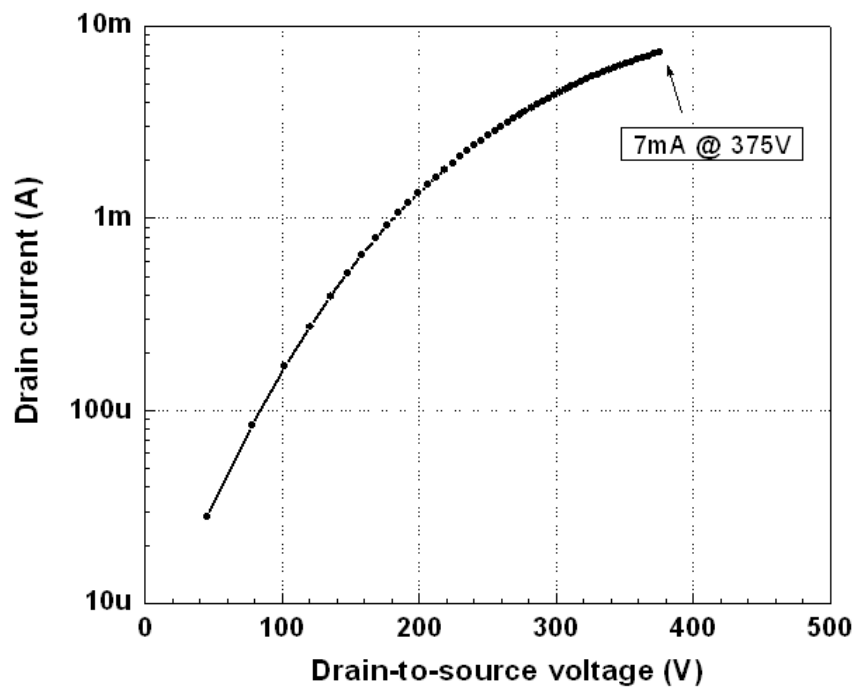
(b) Blocking characteristics.

Fig.7-4. Characterization of a single-gate MOSFET with active area of 1.679×10^{-5} cm^2 on the wafer MV1.

(c) Transfer characteristics measured at V_{DS}=50 mV.

(d) Subthreshold characteristics measured at V_{DS}=50 mV.

Fig.7-4. Characterization of a single-gate MOSFET with active area of 1.679×10^{-5} cm^2 on the wafer MV1 (continued).
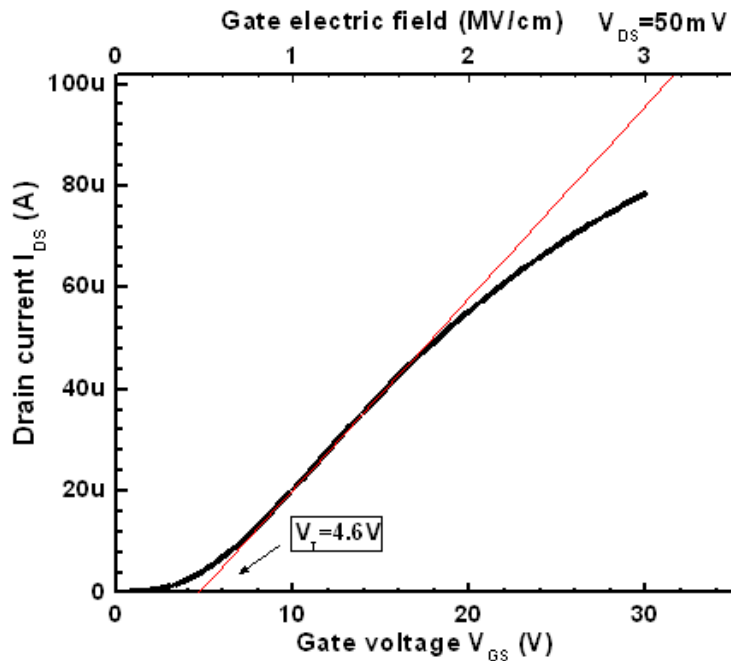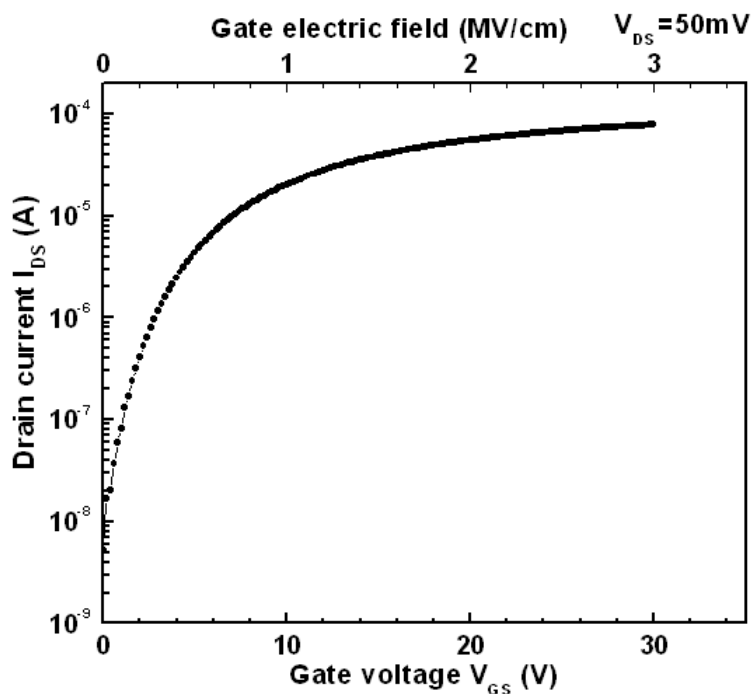
(a) Forward characteristics.

(b) Blocking characteristics.

Fig. 7-5. Characterization of a single-gate MOSFET with active area of 1.679×10^{-5} cm^2 on the wafer MV2.
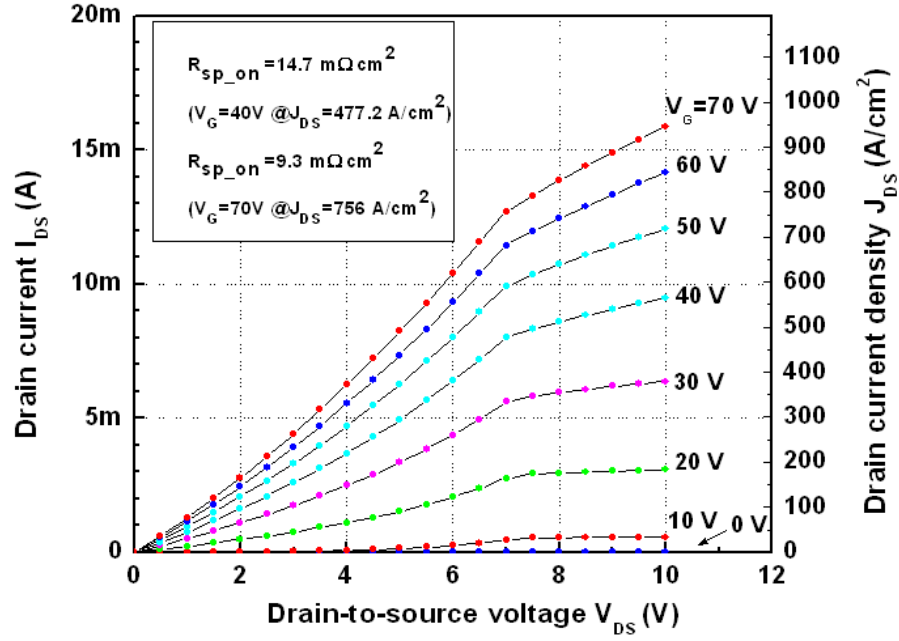
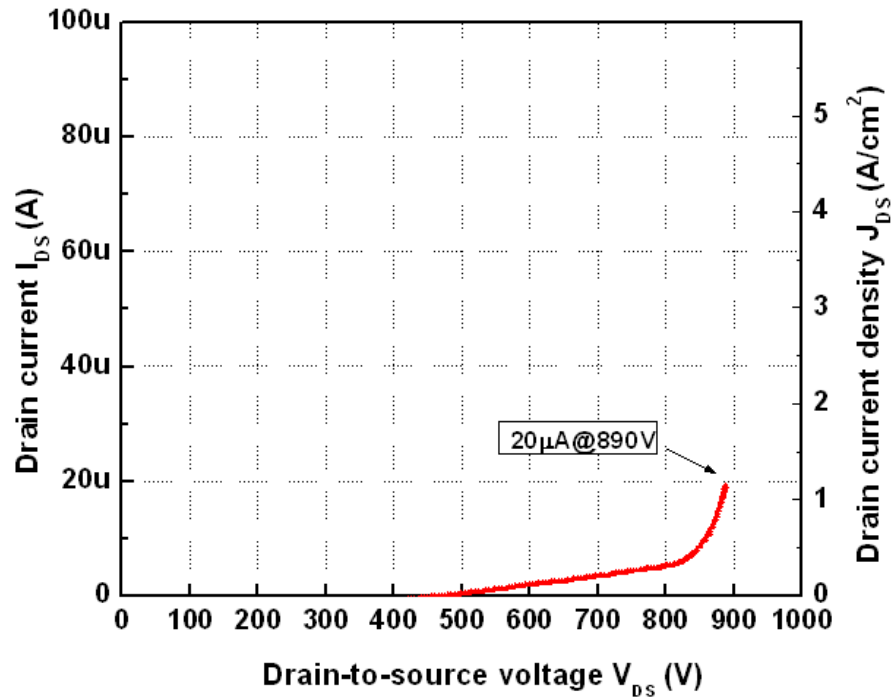(c) Transfer characteristics measured at V_{DS}=50 mV.

(d) Subthreshold characteristics measured at V_{DS}=50 mV.

Fig.7-5. Characterization of a single-gate MOSFET with active area of 1.679×10^{-5} cm^2 on the wafer MV2 (continued).
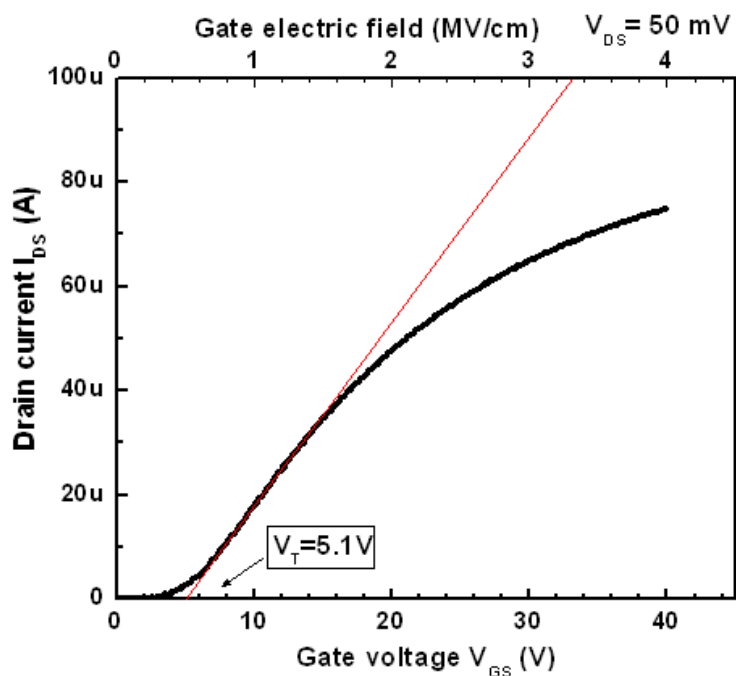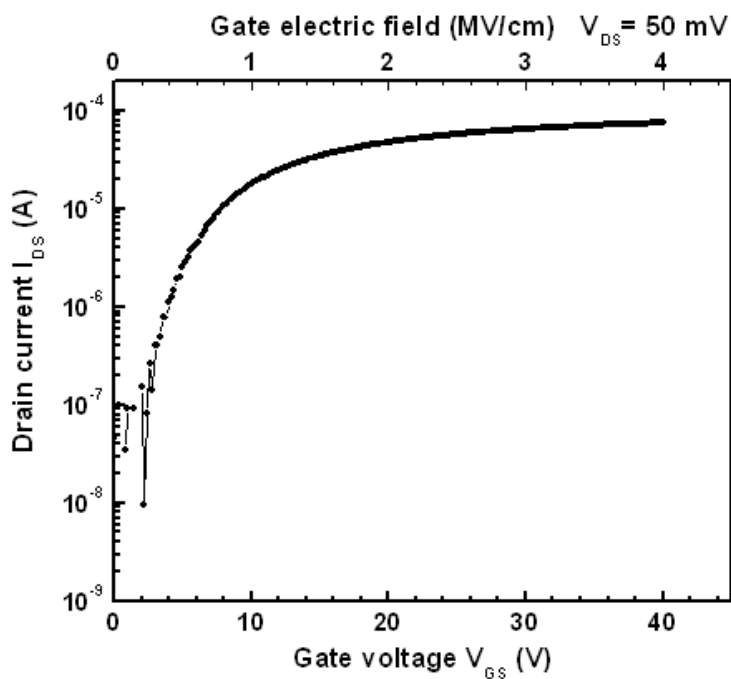
7.2.2 Large-area MOSFETs

Although the total yield of having good large devices was quite low due to the defects introduced during the fabrication process, a number of good large devices have been found in the fabricated wafer MV2. The characteristics of large-area MOSFETs with active areas of 1.03×10^{-2} cm^2 and 4.26×10^{-2} cm^2 are shown in Fig. 7-6 and Fig. 7-7 respectively.

The forward I-V characteristics of these large-area MOSFETs shown in Fig. 7-6a and Fig. 7-7a were measured using a Tektronix 371A curve tracer with the source grounded. The maximum voltage applied on the gate is 50 V, which limits the maximum oxide field to be around 5 MV/cm. At the drain voltage of 3 V with V_{GS}=50 V, the device with active area of 1.03×10^{-2} cm^2 can conduct a high current of 0.45 A, and the device with active area of 4.26×10^{-2} cm^2 can conduct a high current of 1 A. At V_{GS}=50 V, the specific on-resistance was calculated to be 66.2 mΩcm^2 and 113 mΩcm^2 respectively.

The blocking characteristics of these devices shown in Fig. 7-6b and Fig. 7-7b were measured using the Tektronix 371A curve tracer with the source and gate grounded (V_{GS}=0 V). In spite of large-area devices, both devices show good blocking capability with a drain voltage up to 818 V and 810 V respectively. These devices also exhibit very low leakages of 14 μA and 21μA, respectively, at the breakdown voltages.

The I_{DS}-V_{GS} transfer characteristics of the large-area MOSFETs were measured using the HP 4145B with a constant V_{DS}=50 mV. Using the linear extrapolation method, the threshold voltage, V_{th}, are extracted from the transfer characteristics and found to be 6.4 V and 6.5 V respectively (Fig. 7-6c and Fig. 7-7c), indicating stable normally-off operations for these large-area MOSFETs. Fig. 7-6d and 7-7d demonstrate the excellent subthreshold characteristics of the devices and their capability of operating stably as switching devices, as the on/off ratios, defined by the logarithm drain currents, are found to be over 5.

Compared to the single-gate MOSFET on the same wafer MV2 in Fig. 7-5, the large-area MOSFETs in Fig. 7-6 and Fig. 7-7 exhibit higher specific on-resistances with the increased active area. The discrepancies of the specific on-resistances might be linked to the large deviation of the polysilicon trench openings shown in Fig. 6-6. The trench openings on wafer MV2 range from 0.2 μm to 0.6 μm. The polysilicon trenches with smaller openings at some locations resulted in narrower implanted vertical channels or even pitched-off channels, and consequently higher specific on-resistance. Since large-area devices are liable to contain more portions of narrower vertical channels compared to small-area devices, they could exhibit higher specific on-resistance.
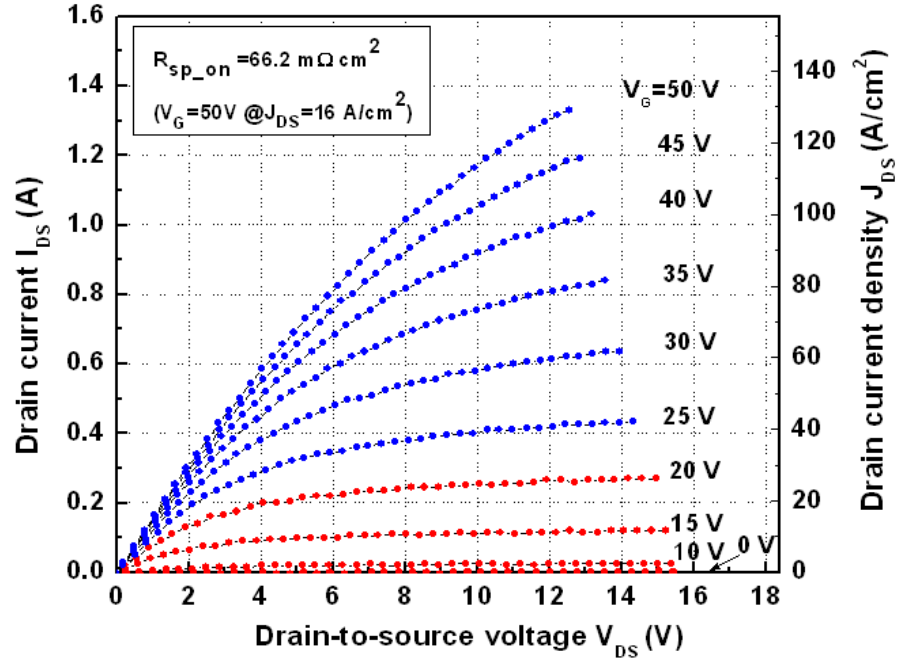
(a) Forward characteristics.

(b) Blocking characteristics.

Fig. 7-6. Characterization of a large-area MOSFET with active area of 1.03×10^{-2} cm^2 on the wafer MV2.
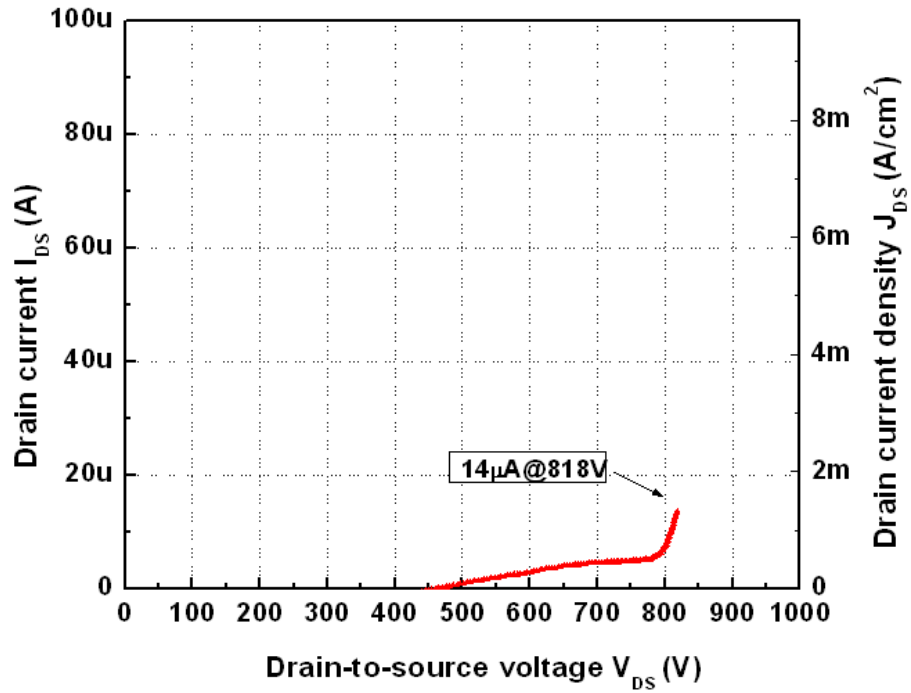
(c) Transfer characteristics measured at V_{DS}=50 mV.

(d) Subthreshold characteristics measured at V_{DS}=50 mV.

Fig. 7-6. Characterization of a large-area MOSFET with active area of 1.03×10^{-2} cm^2 on the wafer MV2 (continued).

(a) Forward characteristics.
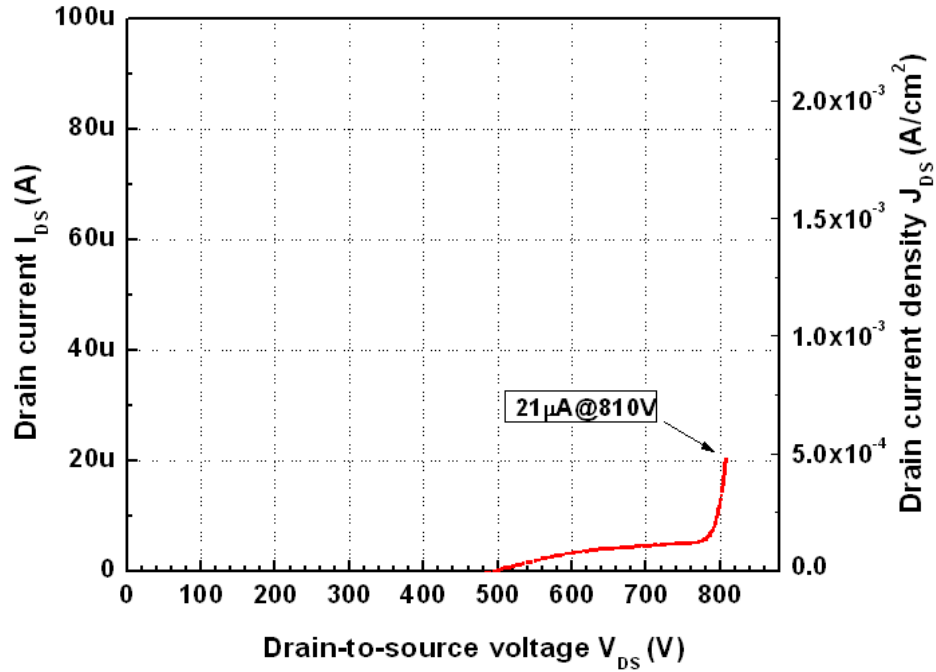
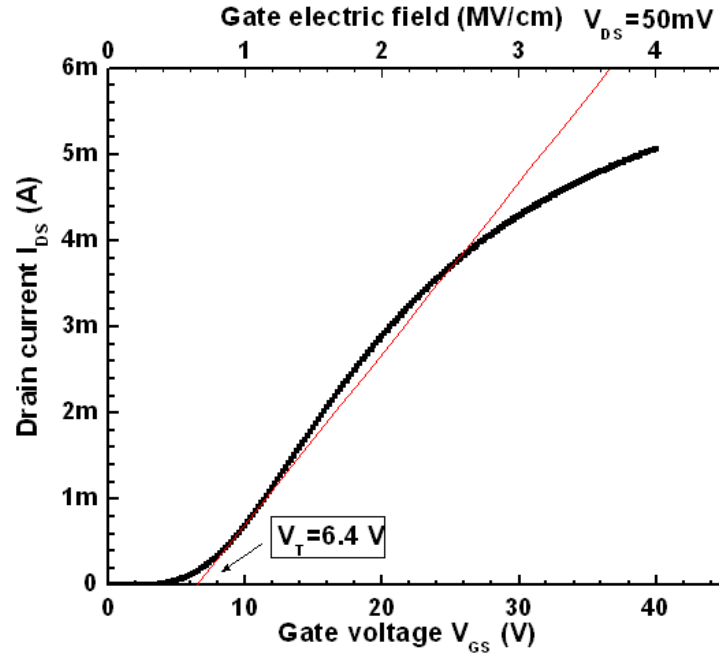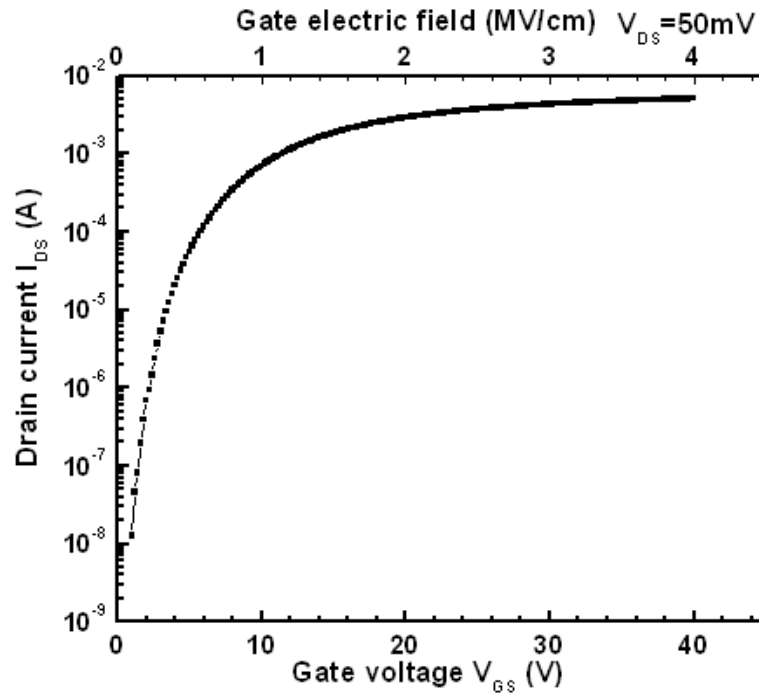(b) Blocking characteristics.

Fig. 7-7. Characterization of a large-area MOSFET with active area of 4.26×10^{-2} cm^2 on the wafer MV2.
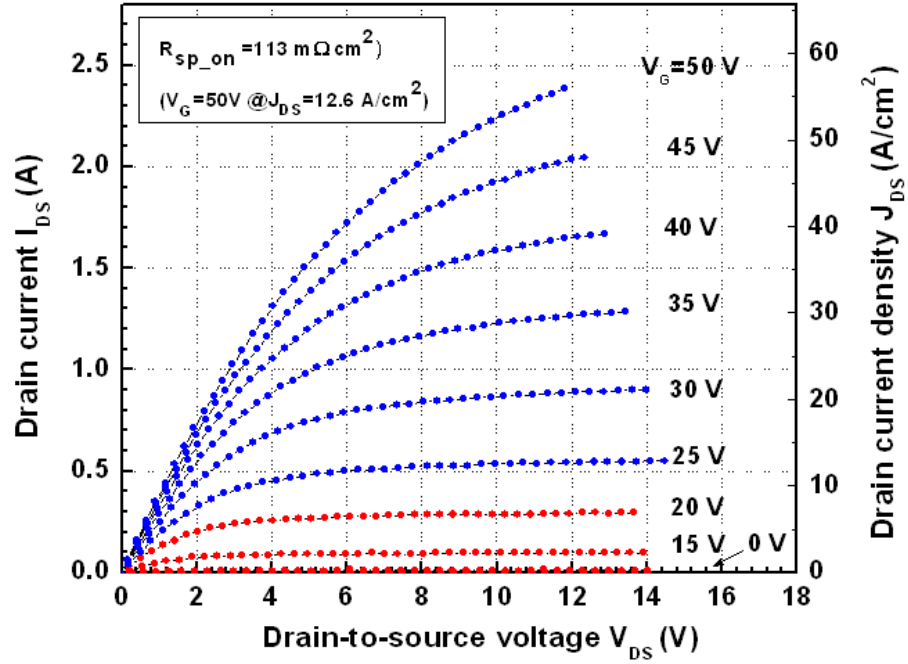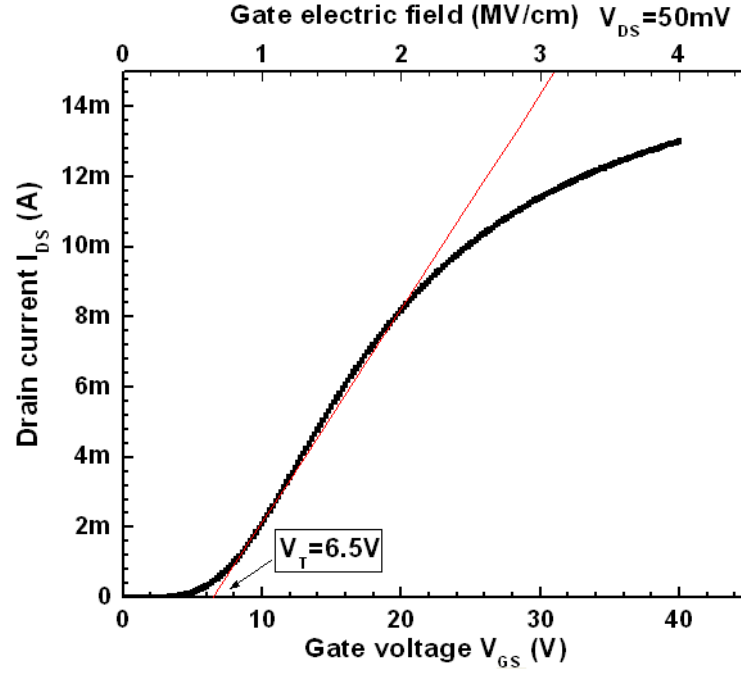
(c) Transfer characteristics measured at V_{DS}=50 mV.
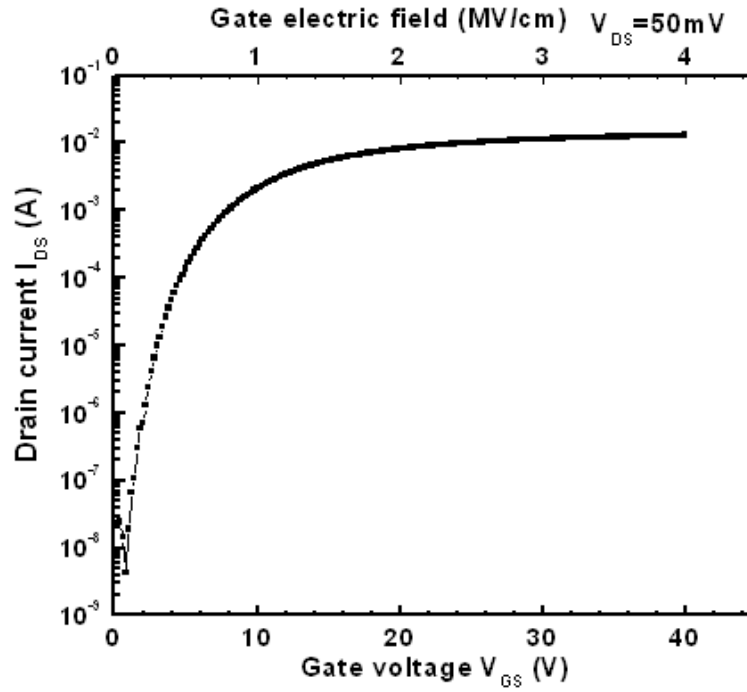
(d) Subthreshold characteristics measured at V_{DS}=50 mV.

Fig. 7-7. Characterization of a single-gate MOSFET with active area of 4.26×10^{-2} cm^2 on the wafer MV2 (continued).

Chapter 8   Conclusions and Future Work
Suggestions

4H Silicon Carbide (4H-SiC) is a very promising semiconductor for high power and high temperature applications, due to its wide bandgap, high breakdown field, high electron saturation velocity, and high thermal conductivity. The 4H-SiC power MOSFET is an excellent candidate for high-power and high temperature applications. High density of SiO_2/SiC interface states and interface surface roughness from high-temperature activation annealing, however, can cause low MOS channel mobility and gate oxide reliability in the development of 4H-SiC power MOSFETs.

The goals of this dissertation are to design a novel MOSFET structure and process to improve MOS channel mobility, to develop new processing technology for 4H-SiC power MOSFET with submicron implanted vertical channels, and to demonstrate the normally-off 4H-SiC power MOSFETs based on this structure.

In this research, a lateral trench-gate MOSFET structure was first designed to investigate the feasibility of channel mobility improvement. This structure features an epitaxial layer as accumulation channel, which keeps the conduction channel of electrons away from the inferior SiO_2/SiC surface.

Hence the interfacial trap effect on carrier mobility and the electron scattering by surface roughness is significantly reduced. The lateral trench-gate MOSFETs have been fabricated. The output and transfer characteristics were measured at room temperature (25^oC) and 200^oC, demonstrating the normally-off operation with very high peak field-effect mobility. The channel thickness dependence of channel mobility and threshold voltage were also studied to find the optimum range of channel thickness.

Based on the successful demonstration of high mobility in the lateral trench-gate structure, a vertical trench-gate power MOSFET structure was designed and fabricated. This structure introduces an epitaxial N-type accumulation channel to take advantage of the higher channel mobility, and eliminates the high-dose N^+ source implantation and P-base implantation in the process to avoid the surface degradation resulting from high-temperature ($\geq 1550\ ^0C$) activation annealing. This structure also features a submicron vertical N-type channel by counter-doping P base region via a low dose nitrogen ion implantation. The implanted vertical channel provides effective shielding to prevent high electric field in the gate oxide and electrical field crowding at the trench corners.

The design optimization of the vertical trench-gate power MOSFET strucutre was conducted to identify the optimum opening and doping of the

vertical channels. A self-alignment process using the oxidation of polysilicon was developed to obtain the submicron vertical N-type implanted channel and align it to the gate trench. A series of experiments were conducted to improve the uniformity of the width and etching depth of polysilicon trenches. The whole fabrication process of vertical trench-gate power MOSFET was developed. A new "sandwich" process including nitric oxide growth, dry O_2 growth and nitric oxide annealing was incorporated for gate oxidation. Deep nitrogen implantation and subsequent activation annealing at a lower temperature of 1450^oC was used to form N-type vertical channels. MJTE technology was implemented to improve the blocking voltage capability.

In this work, both lateral trench-gate MOSFETs and vertical trench-gate power MOSFETs have been successfully demonstrated. The fabricated lateral trench-gate MOSFET with an accumulation channel of 0.15μm in width exhibited a high peak channel mobility of 95 cm^2/Vs at room temperature (25^oC) and 255 cm^2/Vs at 200^oC with stable normally-off operation from 25^oC to 200^oC. The fabricated single-gate vertical MOSFET can block a drain voltage of 890 V at zero gate bias with a low leakage current of 20 μA. The device exhibited a low specific on-resistance of 9.3 mΩcm^2 at a gate bias of 70 V, resulting an improved FOM (V_B^2/R_{ON}) of 85 MW/cm^2. In addition, a large-area MOSFET with active area of 4.26x10^{-2} cm^2 exhibited a blocking

voltage of 810 V with a low leakage current of 21μA, and could conduct a high current of 1 A at a drain voltage drop of 3 V and a gate bias of 50 V. All of the fabricated devices exhibited the stable normally-off operation with threshold voltages between 5 and 6 V. Their subthreshold characteristics also show a large on/off ratio in the range between 3 and 5, suggesting that they may be capable of operating as normally-off devices over a wide temperature range.

Nevertheless, the following improvements would be beneficial for vertical trench-gate power MOSFETs.

(1) The oxidation process of polysilicon needs to be further optimized. Currently the oxidized polysilicon trenches face two problems. The first is that the oxidized poly-Si trenches had a rounded profile (Fig.5-5) instead of a vertical profile. Consequently the vertical channels formed by nitrogen ion implantation could have a tapering width with respect to the channel depth, which might affect the blocking performance of the devices. The second is that the widths of polysilicon trenches tend to be non-uniform after thermal oxidation. The vertical channels with smaller width may favor the blocking performance by more effective pinch-off of the channels, but at the cost of increased specific on-resistance. Further experiments need to be conducted to explore a more optimized

oxidation process to form the oxidized polysilicon trenches with vertical profile and uniform opening.

(2) The current cell pitch of 19.3 μm may be further reduced to increase the density of the unit cell so that the forward characteristics of the devices can be improved for lower specific on-resistance. Since the reduced cell pitch may tighten the misalignment margin resulting in more fabrication complexity, higher alignment accuracy is required. Alternatively the fabrication process needs to be optimized to alleviate reduced misalignment margins.

(3) The source ohmic contact resistance of 8.5×10^{-5} Ωcm^2 should be further reduced by using different metallization scheme and annealing conditions. Meanwhile, experiments of new annealing processes have to take into account the potential degradation of SiO_2/SiC interface under high annealing temperatures.

(4) Better control over MJTE is needed to achieve breakdown voltage closer to the theoretical value. Different MJFET geometries or hybrid edge-termination techniques might be explored to achieve high breakdown voltage.

With these improvements the vertical trench-gate power MOSFETs are expected to exhibit better performance.

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Curriculum Vita

Jian Wu

09/2002-01/2009   Ph.D. in Electrical and Computer Engineering
Rutgers, The State University of New Jersey
New Brunswick, New Jersey, USA

09/1998-03/2001   M.S. in Optical Engineering
Zhejiang University
Hangzhou, China

09/1994-06/1998   B.S. in Optical Engineering
Zhejiang University
Hangzhou, China

Publications

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