DEVELOPMENT OF 4H-SIC HIGH VOLTAGE UNIPOLAR POWER SWITCHING DEVICES

by

PETRE ALEXANDROV

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ABSTRACT OF THE DISSERTATION

Development of 4H-SiC High Voltage Unipolar Power Switching Devices

By PETRE ALEXANDROV

Dissertation Director:
Professor Jian H. Zhao

4H-SiC is a promising material for switching high power and high temperature device applications. The superior properties of SiC, such as wider band-gap and higher value of critical electric field allow significant reduction in device on-resistance compared to Si power devices of similar voltage ratings. In addition the excellent thermal conductivity of SiC alleviates the device cooling requirements and allows design of smaller and more efficient systems. Several advantages of the unipolar power switches over the bipolar switches make them desirable for fast switching applications. Voltage-controlled normally-off devices are particularly attractive for practical applications because of simpler gate-drive circuitry. The advantages of the vertical JFET device being free of the problems related to oxide reliability, as compared to the MOSFET, recognize it as an excellent candidate for high power, high temperature switching applications.

Device designs for normally-off and normally-on unipolar switches with blocking voltages from 400V to 11kV are proposed, based on a pure vertical trenched and implanted structure. Two different junction termination structures (junction termination

extension and guard rings) are designed and successfully implemented. A fabrication process is designed to achieve a simple and reliable self-aligned fabrication process. The fabrication challenges are discussed and ways to improve the process are identified. Three different devices were designed and fabricated.

The world's first normally-off 4H-SiC TIVJFET with a blocking voltage of 11kV was demonstrated, showing low specific on-resistance of 124mΩ.cm^2.

Normally-off and normally-on 4H-SiC High Frequency TIVJFETs with blocking voltages up to 400V were demonstrated. 3.3A-397V normally-off capability was achieved for a single die, corresponding to a high power of 1310 W/die. This corresponds to a class B operation RF power of 164W for a single die. Cut-off frequency f_T= 0.9 to 1.5 GHz was reached.

In the 1200V class devices a normally-on 4H-SiC TIVJFET with guard ring termination and substantially simplified processing was also demonstrated. The highest blocking voltage achieved was 1562V with a specific on-resistance of 2.8mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V and a current gain of 1495. The lowest specific on resistance achieved was 2.2mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V with a current gain of 1454 and a blocking voltage of 1232V.

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CHAPTER 1. INTRODUCTION

1.1. Silicon Carbide Material Overview for Power Electronics

Silicon is the main material used in semiconductor industry. It is readily available, well studied and its processing technology is mature. However, devices based on Si are not able to operate at temperatures above 200^{o}C because of excessive junction leakage currents. This limitation becomes even more severe when high operating temperatures are combined with high-power, high-frequency and high-radiation environment. High-temperature circuit operation is desired for use in various applications, such as aerospace applications, nuclear power instrumentation, space exploration, and automotive electronics. Wide band-gap materials have to be used in order to build devices, capable of operation at higher temperatures. Some of the main materials of interest for such applications are silicon carbide (SiC), gallium nitride (GaN), aluminum nitride (AlN) and diamond.

SiC has several advantages over other wide-bandgap semiconductors at the present time. Properties such as large breakdown electric field strength (10 times that of Si), large saturated electron drift velocity, small dielectric constant, reasonably high electron mobility and high thermal conductivity (about 3.3 times that of Si and better than copper) make SiC an attractive candidate for fabricating power devices with reduced power losses and die size. Table 1.1 shows the key physical properties of some important semiconductors.

Table 1.1. Physical properties for selected semiconductor materials [1, 2, 3].

Material	**E_G (eV)**	**n_i (cm^{-3})**	**ε_r**	**μ_n ($cm^2/V\cdot s$)**	**μ_p ($cm^2/V\cdot s$)**	**E_C (MV/cm)**	**v_{sat} (10^7cm/s)**	**λ (W/cm·K)**
Ge	0.66	2.4×10^{13}	16.0	3900	1900	0.1	0.5	0.6
Si	1.12	1.5×10^{10}	11.8	1350	450	0.3	1.0	1.5
GaAs	1.42	1.8×10^{6}	12.8	8500	400	0.4	2.0	0.5
3C-SiC	2.36	6.9	9.6	800	320	2.0	2.0	4.9
6H-SiC	3.0	2.3×10^{-6}	9.7	400(‖c) 85(⊥c)	90	3.0	2.0	4.9
4H-SiC	3.23	8.2×10^{-9}	9.7	960(‖c) 800(⊥c)	120	3.0	2.0	4.9
GaN	3.39	1.9×10^{-10}	9.0	900	200	3.3	2.5	1.3
AlN	6.1	$\sim10^{-31}$	8.7	300	14	1.3-1.8	1.8	2.5
Diamond	5.5	1.6×10^{-27}	5.5	2200	1800	5.6	2.7	20.0

From a technological point of view there is an advantage for SiC having a similar chemistry to that of the silicon, which gives immediate access to well-known device processing techniques. Perhaps the most important technological advantage of SiC is the ability to grow thermal oxide for use as device passivation layers, gate dielectrics, and as mask in processing. Another very important advantage is the commercial availability of SiC substrates (currently 4-inch wafers are available).

Various Figure-of-Merit (FOM) coefficients based on material parameters have been introduced to compare different semiconductor materials for high voltage, high frequency applications (Table 1.2. [3, 4]). Johnson FOM can be used to compare devices for high frequency signal amplifiers; Keyes FOM is suitable for high-speed switches comparison; Baliga FOM is for unipolar low frequency power devices; and Baliga high frequency FOM is for unipolar high frequency power switches. An important power device FOM is V_{BR}^2/R_{ON_SP}, which is related with BFOM by $\varepsilon_r\mu_n E_C^3 = \frac{1}{\varepsilon_0}\frac{V_{BR}^2}{R_{ON\_SP}}$, and is commonly used to compare the DC performance of power transistors. Huang FOMs are more useful from

an application point of view. HFOMs include Huang Material FOM (HMFOM) for evaluation of both conduction and switching losses, Huang Chip Area FOM (HCAFOM) for comparison of chip areas, and Huang Thermal FOM (HTFOM) for the junction temperature variation.

Based on FOMs comparison, 4H-SiC is the best material among the SiC polytypes and is expected to outperform silicon substantially for high voltage switching applications. GaN shows comparable mobility, breakdown field, and saturation velocity as SiC but lower by more than a factor of 3 thermal conductivity than SiC, which corresponds to worse FOMs related with thermal conductivity. In addition, GaN has a direct bandgap, resulting in a short minority carrier life time, which is undesirable for bipolar device operation. Another disadvantage for GaN compared to SiC at present time is several orders of magnitude higher defect density in GaN materials. AlN has one of the largest bandgaps, however the growth of defect free AlN crystals is seriously problematic. Diamond has superior physical, chemical and electrical properties, compared to any other material. However, taking advantage of diamond's excellent properties is limited by the unavailability of large area high quality diamond substrates and the fact that only p-type diamond is available at present. Based on all of the above considerations 4H-SiC is currently the best choice for power switching applications.

Table 1.2. Figures-of-Merit (FOM) normalized to Si [2, 4]

Material	**Johnson JFOM** $(E_C v_{sat} / 2\pi)^2$	**Keyes KFOM** $\lambda\sqrt{v_{sat} / \varepsilon_r}$	**Baliga BFOM** $\varepsilon_r \mu E_C^3$	**Baliga high frequency BHFFOM** μE_C^2	**Huang Material HMFOM** $E_C\sqrt{\mu}$	**Huang Chip Area HCAFOM** $\varepsilon_r E_C^2\sqrt{\mu}$	**Huang Tempera-ture HTFOM** $\lambda/(\varepsilon_r E_C)$
Si	1	1	1	1	1	1	1
Ge	0.028	0.24	0.15	0.32	0.57	0.26	0.9
GaAs	7	0.45	16	11	3.3	4.8	0.2
3C-SiC	178	5.1	143	26	5.1	28	0.6
6H-SiC	400	5.1	244	30	5.4	45	0.4
4H-SiC	400	5.1	585	71	8.4	69	0.4
GaN	756	1.6	677	81	9.0	75	0.1
Diamond	2540	32	4940	568	23.8	207	1.5

1.2. Power Switching Devices – Alternatives and Current Status

1.2.1. Unipolar vs. Bipolar Power Devices

The main types of power switching devices include Bipolar Junction Transistor (BJT), Thyristor, Insulated Gate Bipolar Transistor (IGBT), Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), and Junction Field Effect Transistor (JFET). Based on the type of current carriers utilized they can be divided into two types – bipolar and unipolar. Bipolar devices such as BJT and IGBT employ majority and minority carriers. They have the advantage that due to minority carrier injection during operation, conductivity modulation could be realized to reduce the device on-resistance and forward voltage drop. However, the minority carrier charge stored during the device on-state has to be removed by recombination during switching to off-state, which leads to increased switching times and switching losses. Furthermore bipolar devices in SiC currently have the problem of forward voltage shift caused by the stacking faults migration in SiC under high current density operation [14].

Unipolar devices use only majority carriers, so they do not suffer from the problems related to minority carrier storage and hence offer faster switching speeds and reduced switching losses. Therefore a unipolar switch would be the device of choice for fast switching applications. According to a recent detailed modeling study SiC unipolar power switches have an advantage in comparison to bipolar power switches at voltages up to 20kV when switching frequency is above 800Hz for a device junction temperature of 175^{o}C [5]. In silicon over a certain voltage range the IGBT is the preferred type of switching device. If silicon IGBTs can be replaced by unipolar SiC switches, the switching losses could be radically reduced [6]. Due to SiC higher critical electric field unipolar devices in SiC have ten times lower resistivity compared to unipolar silicon devices. For a given on-resistance SiC switching devices are much smaller and offer very low input and output capacitances. Therefore for application where Si MOSFETs are used, benefits are possible from using SiC unipolar switches by reduction of parasitic capacitances.

1.2.2. Unipolar Power Devices – MOSFET vs. JFET

Among the unipolar devices there are two types of power devices - MOSFET and JFET. MOSFET is the most popular unipolar power switching device. Power MOSFETs are designed to be in normally off, i.e. in the off state with no bias applied to the gate. In a MOSFET the current flows through a thin surface channel formed by applying an appropriate bias at the gate, which is insulated from the semiconductor. A critical characteristic of the device is the quality of the semiconductor-oxide interface. In silicon carbide this interface contains high density of carbon related surface states, which results in low electron mobility at the channel surface. Substantial progress has been made in the

development of SiC MOSFET. 4H-SiC MOSFET with low on-resistance of 1.8 $m\Omega cm^2$ and a blocking voltage of 660 V has been reported with very fast switching speed (rise time of 19 ns and a fall time of 39 ns) [7]. However, the reliability of SiC MOSFETs at high temperatures and high electric field is a key concern [11,12]. An intrinsic disadvantage of SiC is the smaller conduction band discontinuity for the SiC-oxide interface compared to Si-oxide [10]. Moreover if the higher breakdown filed of SiC is to be utilized, the oxide would be subjected to an even larger stress. This would lead to threshold voltage instability, due to carrier trapping in the gate oxide, and premature oxide breakdown, especially at high temperatures. The use of a MOSFET at higher temperature is limited due to the exponential influence of the temperature on the device life time [8]. A recent work [11] suggest that 4H-SiC double implanted MOSFETs (DIMOSFETs) have at least more than two orders of magnitude less Mean Time To Failure (MTTF) than MOS capacitors on n-type 4H-SiC, which indicates that reliability for operation up to 300^oC will be nearly impossible.

JFETs on the other hand are free of gate oxide and use only p-n junctions in the active device area where high electric field stress occurs and so are not subject to oxide related reliability issues. Therefore JFETs can fully exploit the high temperature capability of SiC in a voltage controlled switching device. Another benefit of the JFET is that the threshold voltage is practically independent of temperature, (the pinch-off voltage V_p is determined by the channel doping and its geometry $V_p = \frac{q.N_D.a^2}{2.\varepsilon_s} - V_{bi}$, where N_D is the channel doping, q is the electron charge, a is the half of the channel height and ε_s is the SiC permittivity). The change in the built in-voltage V_{bi} with temperature can be

neglected for $V_p >> V_{bi}$. In MOSFETs several temperature dependent factors result in a decrease of the threshold voltage with temperature

$V_T = \sqrt{\frac{4.\varepsilon_s.k.T.N_A.\ln(N_A/n_i)}{\varepsilon_{ox}/t_{ox}}} + \frac{2.k.T}{q}\ln\frac{N_A}{n_i} - \frac{Q_{ss}(T)}{C_{ox}}$, where k is the Boltzmann constant, N_A is the acceptor concentration in the channel region, n_i is the intrinsic concentration, ε_{ox} the permittivity of the oxide, t_{ox} is the oxide thickness, Q_{ss} is the interface charge and C_{ox} the oxide capacitance.

1.2.3. JFET – A Better Choice for High Temperature Power Device

Based on the above comparison at this point the JFET has a clear advantage over the MOSFET. As serious work is being done to solve different problems in the MOSFET, it might be improved in the future, however the JFET will still remain the device of choice for high temperature and harsh environment applications [8]. Experimental results show that 4H-SiC JFETs have a very wide temperature range of operation. 4H-SiC JFETs have been characterized at high temperatures up to 450°C [15] and down to cryogenic temperatures of 30K [16]. 4H-SiC JFETs have also demonstrated feasibility of at least 500h life at 500°C [17]. A DC-DC converter using 4H-SiC JFETs and 4H-SiC Schottky diodes was tested at ambient temperature up to 400°C [18]

Regarding the device structure, there are two main types of JFET – Lateral (LJFET), where the source, gate and drain terminals are all one side of the wafer and Vertical (VJFET), where the source and gate terminals are on the front side of the wafer and the drain terminal is placed on wafer backside. The VJFET structure allows higher cell packing density, and hence can achieve lower on-resistance. The LJFET structure, even

though offering lower packing density, has a clear advantage for realizing power integrated circuits.

Based on operation JFETs could be classified as normally-on (conducts high drain current at zero gate bias) or normally-off (blocks high drain-to-source voltage at zero gate bias). Normally-off structure is preferred from application point of view, as it ensures safe system operation. In a normally-off structure the channel has to be designed narrow enough to be pinched off at zero gate bias and at the same time to have e reasonable on-resistance, which requires a precise control of the channel width. This leads to relatively smaller technology process windows and makes the process more challenging.

On the other hand normally-on JFETs can deliver lower on-resistance and are even desirable in certain applications. The disadvantage of the normally-on device can be overcome in applications by using a cascode configuration composed of a low voltage Si MOSFET and the high voltage SiC JFET [8, 12], however for this configuration the high temperature performance of the composed device will be limited by the Si MOSFET. A more attractive solution is a JFET cascode switch, based on SiC only. Such a switch has been demonstrated by combining a low-voltage normally-off SiC JFET, used as the controlling device, in series with a high-voltage normally-on SiC JFET, capable of blocking over 1000V with a specific on-resistance of 3.6 $m\Omega cm^2$, which could be operated at temperatures over 150°C [17]. Unfortunately for this solution the process challenges related to realizing high current normally-off SiC JFET will still be in effect.

High voltage normally-off SiC JFET can be more easily realized by combining a lateral, low voltage, normally-off JFET structure with a vertical normally-on, high-voltage structure [19-22]. However, the fabrication of this type of JFET is more

complicated and a low specific on-resistance is more difficult to achieve, compared to a pure lateral or vertical structure. The best results achieved with this kind of structure are 5.3kV 4H-SiC SEJFET with specific on-resistance (R_{SP_ON}) of 69mΩcm^2 [21] and a 4,340V, 40mΩcm^2 normally-off 4H-SiC VJFET [22].

Based on the above considerations a vertical JFET type is the most interesting for power device application, as it offers higher packing density than the lateral type, has a potential to achieve very low on-resistance and is simpler to realize than a combined lateral plus vertical structure.

Different approaches have been used to realize a vertical JFET structure. A SiC static induction transistors (SITs) was fabricated using e-beam lithography and vertical implantation [23, 24]. One disadvantage of this SIT structure is that because of the implantation scattering effect, the vertical channel does not have a uniform channel width. Another disadvantage is that longer channel length is difficult to achieve because it is determined by the implantation depth, which is limited by the ion implanter energy capability. Typical commercial implanters provide several hundred kiloelectron-volt ion implantations, and megaelectron-volt ion implantations, required to form a reasonably long vertical channel, have a very limited availability.

Another way to realize a vertical JFET structure uses the epitaxial regrowth approach [25, 26]. A very low on-resistance of 1.0mΩ.cm^2 with a blocking voltage of 700V was achieved using a buried gate structure [25]. Another device achieved and 1270V, and 1.21mΩ.cm^2. However, the buried-gate SIT is likely to have issues during switching operation because the relatively long p-type buried gate without metal has a much larger resistance and, hence, a much larger gate RC time, compared to a vertical structure with

ohmic contact metal close to the p-gate region surrounding the channel. Also the fabrication process for this type of JFET is more complicated as it requires epitaxial regrowth in the middle of the processing.

The third type of a VJVET structure is the Trenched and Implanted VJFET (TIVJFET). It is simple to fabricate, as no epitaxial re-growth is needed, and it can achieve low specific on-resistance [27]. Normally-off performance can be achieved with a scalable design from 1.7kV to 14kV [28]. Normally-off 4H-SiC TIVJFET was reported, with R_{SP_ON} of 3.6mΩ.cm^2 and blocking voltage of 1726V, corresponding to a figure of-merit (FOM) (V_B^2/R_{SP_ON}) of 830 MW/cm^2, which is 28 times better than the state-of-the-art silicon Cool-MOS power devices [29]. The first reported VJFET in the 10kV class is a TIVJFET and the highest blocking voltage reported for a TIVJFET is 11.1 kV with R_{SP_ON} of 124 mΩcm^2 [30, 31]. Therefore the Trenched and Implanted VJFET structure is a very attractive approach to realize low on-resistance and high voltage power switching devices using a relatively simple fabrication process.

1.3. Objectives of the Proposed Ph.D Thesis Research

The objective of the proposed research is to develop unipolar power switches with blocking voltages from 300V to >10kV and low on-resistance. Normally-off and normally-on structures will be designed based on the TIVJFET concept. An 11kV normally-off TIVJFET will be designed and fabricated. A normally-off and normally-on 400V High Frequency TIVJFET (HF-TIVJFET) will be designed and fabricated. A normally-on 1.2kV TIVJFET will be designed and fabricated. Two different junction termination approaches (Junction Termination Extension and Guard Rings) will be investigated. Completely self-aligned method for defining source and gate contacts will

be pursued. Critical processing issues will be investigated in details and improved. A main goal of this work is to develop a simple and robust process to fully exploit the advantages of the TIVJFET structure.

CHAPTER 2. BASIC TIVJFET STRUCTURE AND PROCESS DESIGN

2.1. Basic TIVJFET Structure Design

2.1.1. Unit Cell Design

A cross sectional view of a unit cell TIVJFET structure is shown on Figure 2.1.

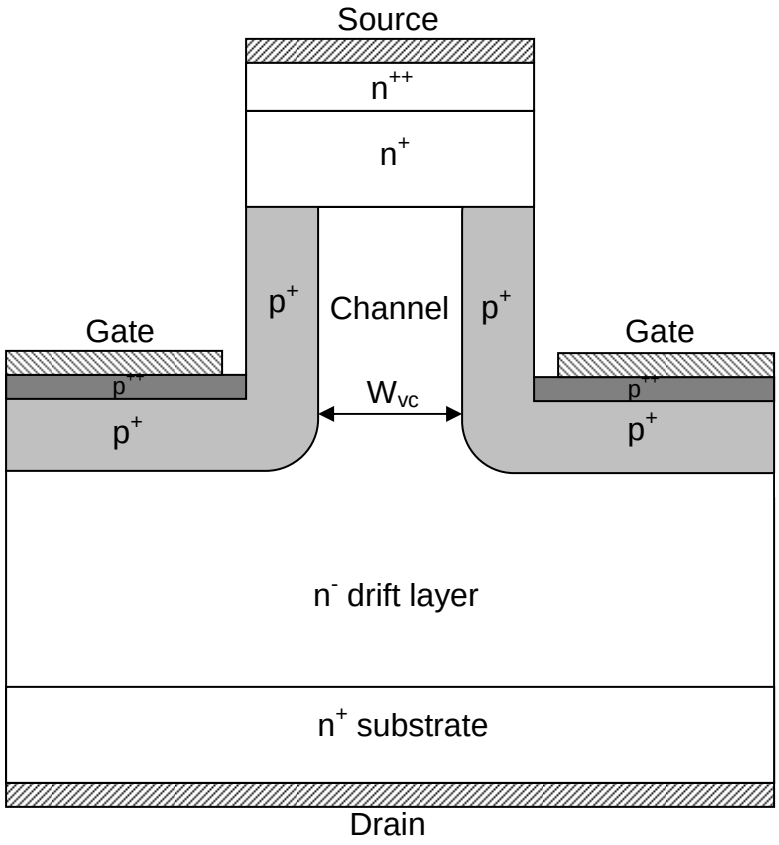


Figure 2.1. Unit Cell Structure of TIVJFET structure.

The wafer structure consists of three n-doped epitaxial layers. The upper heavily doped ($>1\times10^{19}cm^{-3}$) n++ epilayer is used to create the source ohmic-contact. The next n+ epilayer is slightly more lightly doped to $2\text{-}8\times10^{18}cm^{-3}$. It serves to define the vertical boundary of the gate-source p-n junction and provides a process margin for the planarization process used to fabricate the device. The third epilayer is used to form the

vertical channel and to support the voltage. Its thickness and doping are designed so that the device can support the required voltage. A vertical channel is formed by etching source mesas and implanting the gate. Normally-off or normally-on structures can be formed by choosing a vertical channel width. For a normally-off device the width of the channel is designed to be completely depleted at zero gate bias to ensure normally-off behavior. For a normally-on device channel is designed to be open at zero gate-to-source bias and its width is chosen so that it can be closed by applying a reasonable negative voltage to the gate with respect to the source. The width of the gate trench is chosen to be the minimum allowed by the fabrication process in order to maximize source-to-gate area ratio and device current density. The device is designed to be able to operate in a large temperature range from 70K to 600K. Since the vertical channel will become more "open" at higher temperature than at lower temperature due to the decrease of the p-n junction built-in voltage with temperature, the design should be performed at the highest temperature.

2.1.2. Drift Layer Design

The breakdown voltage of the TIVJFET structure depends on the semiconductor critical field (electric field at which avalanche multiplication of current carriers by impact ionization will occur), epilayer doping, epilayer thickness, and device edge termination. Therefore epilayer doping and thickness can be determined from the desired breakdown voltage under parallel plane avalanche breakdown conditions. The desired epilayer doping is the maximum doping that will sustain the specified breakdown voltage. The relationship for the epilayer doping is [34]:

$$N_D = \frac{\varepsilon_s E_C^2}{2qV_B} \tag{2.1}$$

where E_C is the semiconductor critical field and V_B is the breakdown voltage.

The epilayer thickness is the reverse bias depletion region width at the breakdown voltage. The relationship for the epilayer thickness is [34]:

$$t_{epi} = \frac{2V_B}{E_C} \tag{2.2}$$

For 4H-SiC the critical field dependence on the doping concentration is described by [35]:

$$E_C = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log_{10}\left(\frac{N_D}{10^{16}}\right)} \tag{2.3}$$

According to other authors [36] the critical field dependence on the doping concentration for 4H-SiC is:

$$E_C = 1.64 \times 10^4 N_D^{1/7} \tag{2.4}$$

Alternative epilayer doping and thickness can be used, based on the punch-through concept. The punch-through structure has a smaller thickness to support the same voltage as a non-punch-through structure and thus can provide a lower on-resistance and a reduced wafer cost. The breakdown voltage of a punch-through diode can be calculated using the expression:

$$V_{PT} = E_C t_{PT} - \frac{1}{2}\frac{qN_{Dpt} t^2_{PT}}{\varepsilon_s} \tag{2.5}$$

where V_{PT} is the punch-through voltage, t_{PT} is the punch-through layer thickness.

The drift layer doping and thickness to support a desired voltage are calculated using equations (2.1-2.5). Results are shown on Figure 2.2-2.3 and can be used for choosing the right epilayer thickness and doping concentration. The values of the parameters will depend on the critical electric field chosen for the calculations. The two different models shown above give different numbers for the breakdown voltage and epilayer thickness.

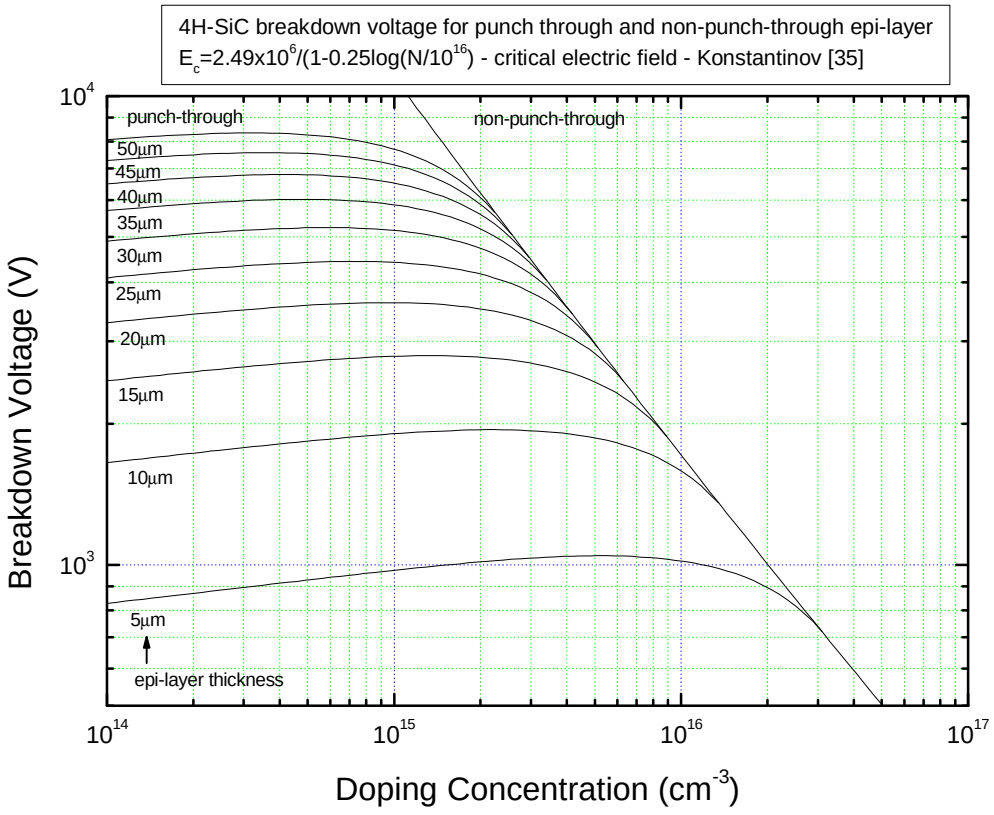


Figure 2.2. Breakdown voltage vs. doping concentration for non-punch-through and punch-through 4H-SiC epilayers, based on Konstantinov's critical electric field [35].

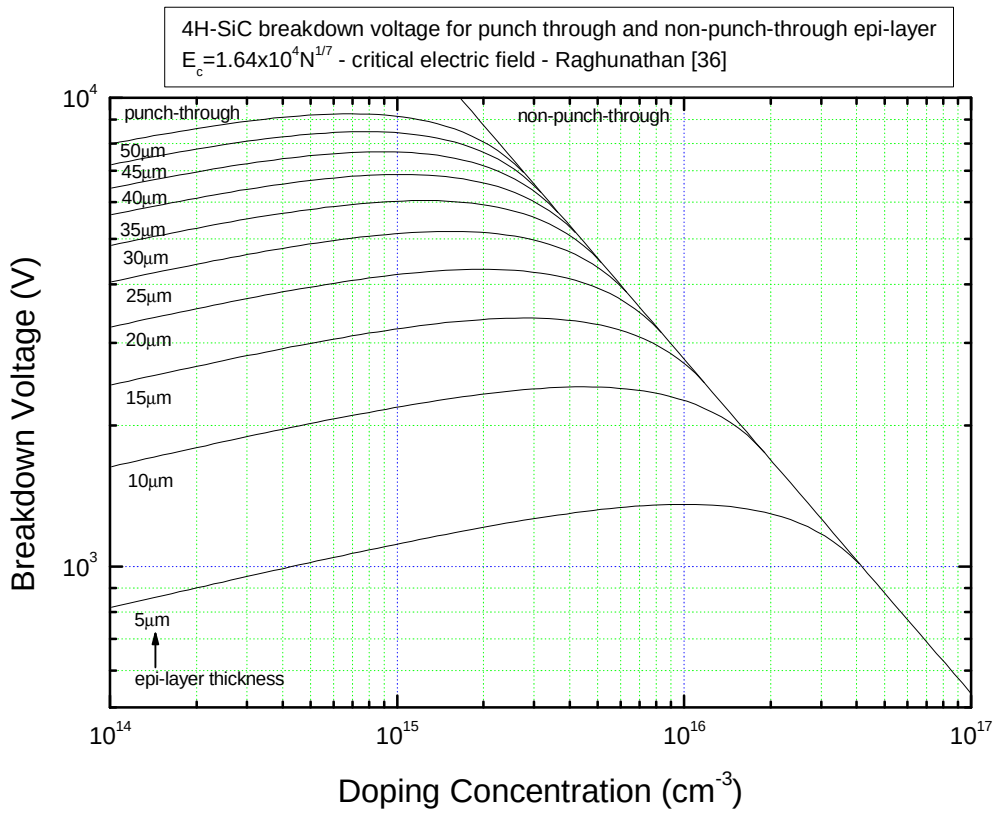


Figure 2.3. Breakdown voltage vs. doping concentration for non-punch-through and punch-through 4H-SiC epilayers, based on Raghunathan's critical electric field [36].

2.1.3. Junction Termination Design

In practice it is not possible to achieve the theoretically predicted avalanche breakdown voltage, because of two-dimensional and three-dimensional field crowding at contact and junction edges. Edge termination is necessary to reach the parallel plane breakdown voltage. Many different types of edge terminations have been used for power devices [33] including beveled edges, field plates, floating metal rings, p-type floating filed rings, junction termination extension. The most commonly used termination methods are these that use planar junctions, because they are compatible with the planar fabrication technology. Up to 80% of the ideal breakdown voltage could be achieved using floating field rings, and up to 95% using junction termination extension. For SiC, with its high

critical field, the last two techniques, which do not rely on dielectrics, should be the best choice.

2.1.3.1. Junction Termination Extension (JTE)

Junction termination extension (JTE) technique [33] can give almost parallel plane breakdown voltage (up to 95%). It is convenient, because no complicated photolithography steps are needed and the amount of introduced charge can be precisely controlled by ion implantation. JTE region should be totally depleted at the required blocking voltage applied. Key parameters of JTE are the length L_{JTE}, the depth d_{JTE} and the doping concentration N_{JTE}. A schematic view of a p-n junction with JTE region is shown on Figure 2.4.

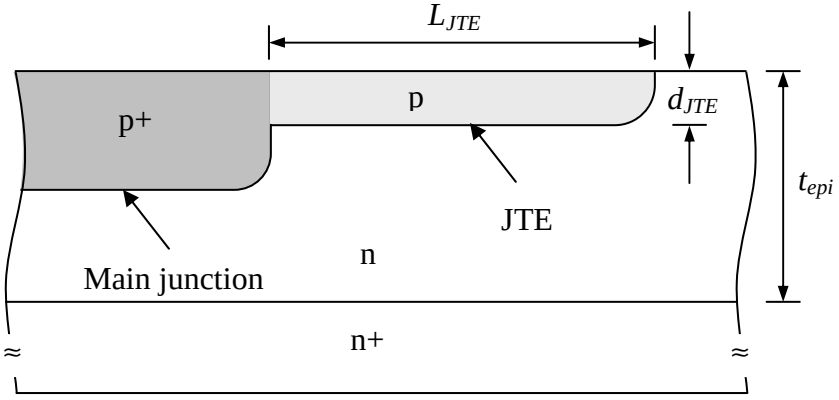


Figure 2.4. Schematic cross section of a p-n junction with junction termination extension.

The length should be chosen to be larger than the epilayer thickness in order to reduce the field at the surface by supporting the same voltage with larger depletion width. However it should not be much larger than the epilayer thickness in order to save valuable wafer space. The implanted dose $D = N_{JTE}d_{JTE}$ is determined by the maximum electric filed and is equal to $\frac{\varepsilon_s E_C}{q}$. If we express it in terms of the epilayer parameters it

is: $D = N_D t_{epi}$, where N_D and t_{epi} are the epilayer doping and thickness respectively. Once we choose the dose, we can decide about d_{JTE} and N_{JTE}. Numerical analysis shows that for a given doping level of the junction extension, the breakdown voltage increases and then decreases, going through a maximum when the depth of the junction extension increases [37, 38].

One problem with the JTE structure in SiC is the uncertainty in p-dopants activation, which can lead to ineffectiveness of the termination. A practical approach to realize a JTE structure is to implant it together with the gate and then remove as much of the implanted thickness as needed to achieve the right charge balance. This reduces the number of photomasks needed, saves one implantation step and eliminates the uncertainty in the p-dopant activation efficiency, as the actual JTE charge can be adjusted by etching after implantation and dopant activation. A multiple-zone JTE structure is more effective than a single-zone JTE. A three-zone JTE structure was chosen to be implemented. Figure 2.5 shows a schematic view of the JTE structure. The different zones are formed by additional etching steps.

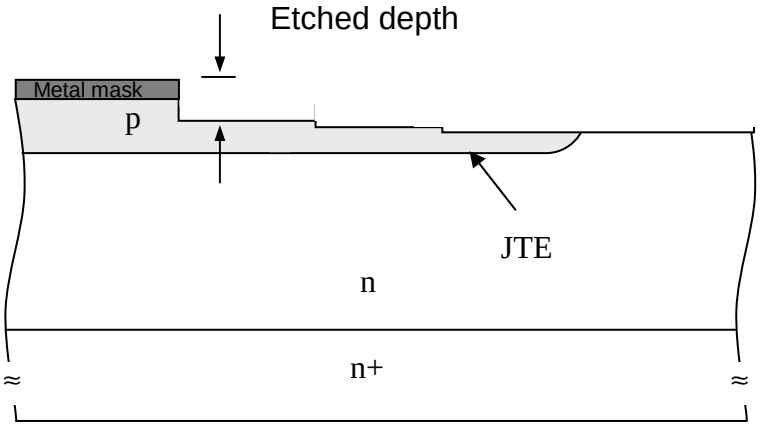


Figure 2.5. Three-zone JTE structure, realized by implantation and subsequent surface etching.

There are two additional issues with JTE. First, the presence of surface charge over the implanted region can strongly affect the electric field distribution. This can cause high electric field to arise at the surface and wide variation of breakdown voltage from device to device. Second, the high electric field near the surface can cause excessive leakage current flow. In order to reduce the surface charge the semiconductor surface needs to be properly passivated.

2.1.3.2. Floating Guard Rings

JTE is a very good termination technique as it can achieve breakdown voltage that is as close as possible to the theoretical limit. It, however, has the disadvantages of more complicated practical realization and sensitivity to surface charge. In order to simplify the fabrication process guard ring termination was also designed. The guard rings can be implanted together with the gate and no additional processing is required. The guard ring structure is shown schematically on Figure 2.6 and Figure 2.8. The design uses 28 rings with non-uniform spacing. The spacing increases from the main junction toward the device periphery. Numerical modeling shows that this termination structure can achieve more than 90% of the parallel plane breakdown voltage. By shifting the guard ring spacing proportionally (same amount for all spacings) the structure can serve for a range of drift epilayer doping. Figures 2.7 and Figure 2.9 show the maximum electric field at breakdown for two different epilayer doping levels.

The actual structure to be fabricated is shown on Figure 2.10. The guard rings are formed in the same manner and at the same time as the JFET gate. The spacing between the individual guard rings are defined with mesas etched together with the source mesas.

The whole guard ring structure is self aligned and requires no additional processing step, as it is formed together with the source and gate formation.

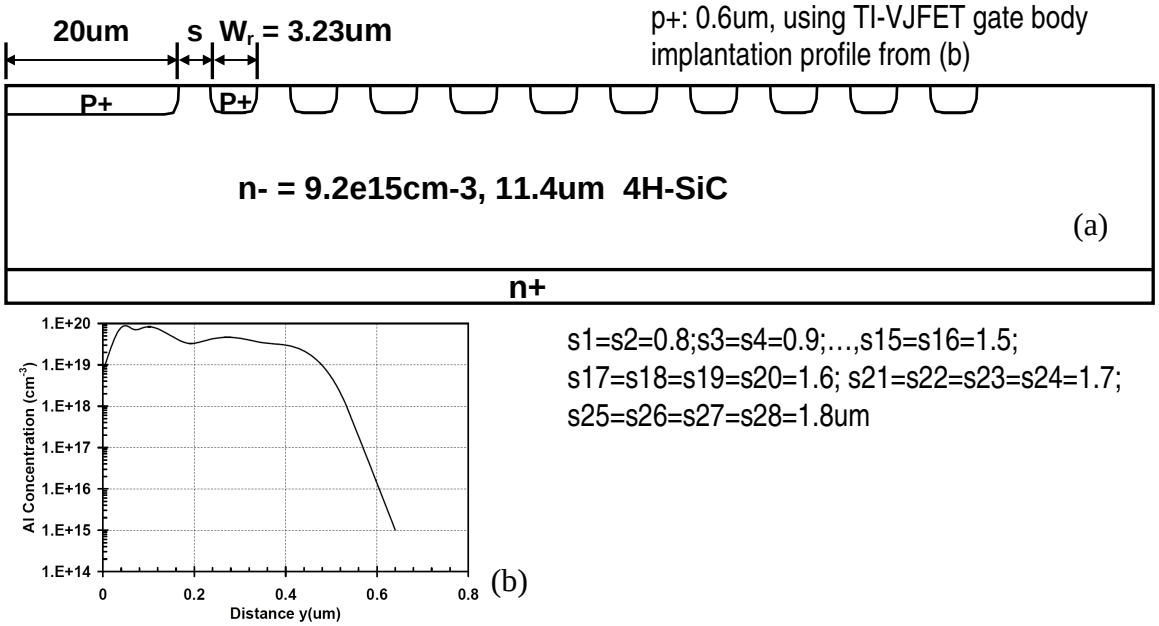


Figure 2.6. Guard ring structure (a) and Al implantation profile (b).

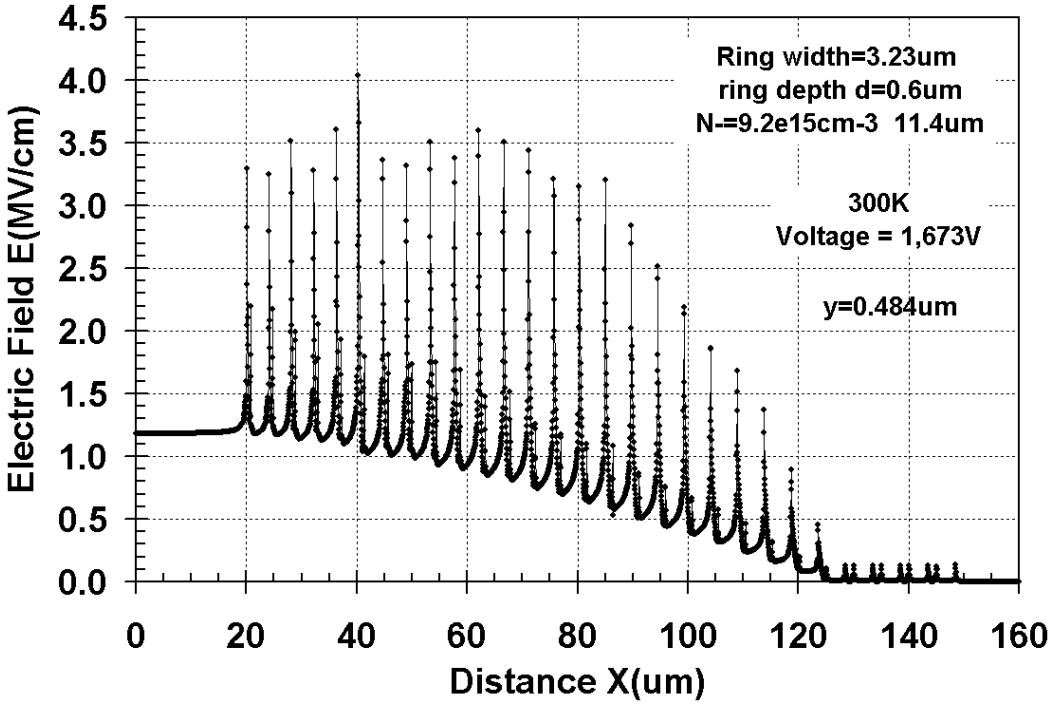


Figure 2.7. Maximum field in the device at 1673V.

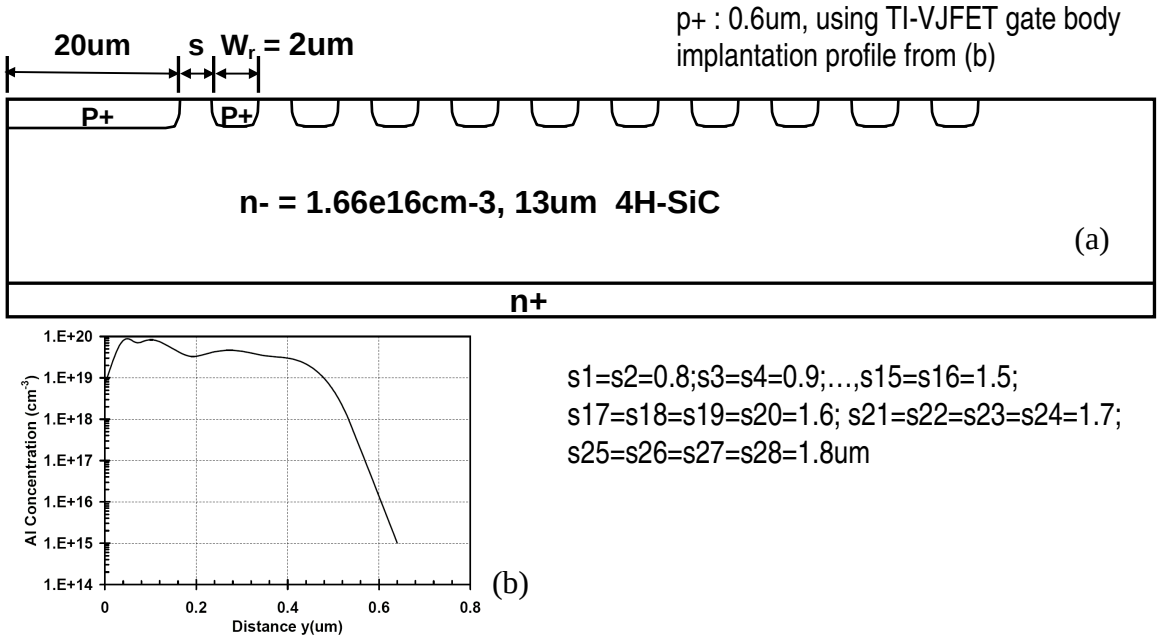


Figure 2.8. Guard ring structure (a) and Al implantation profile (b).

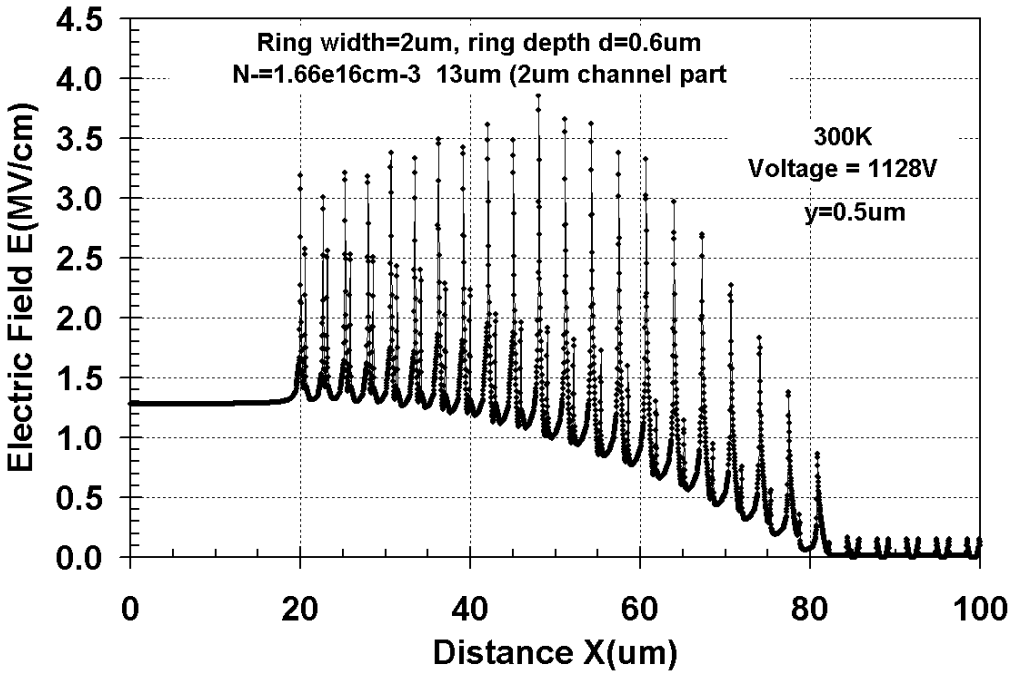


Figure 2.9. Maximum field in the device at 1128V.

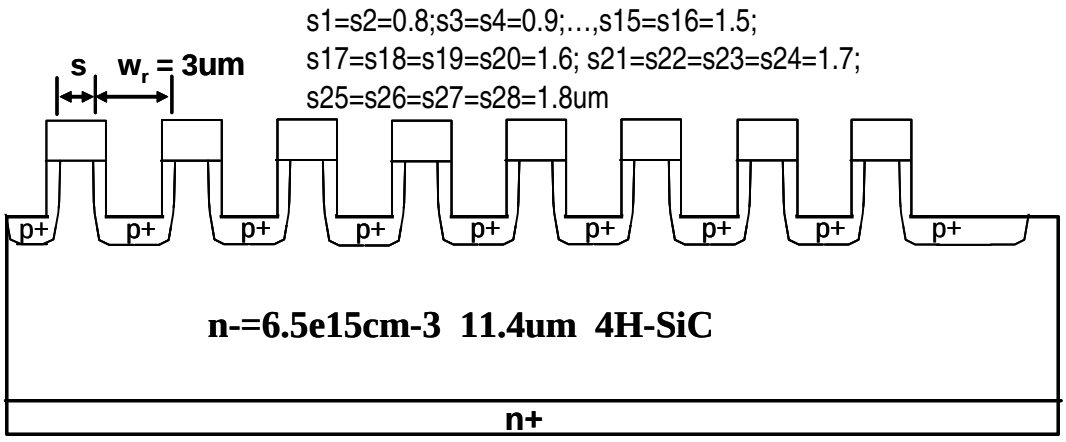


Figure 2.10. Floating guard ring structure, using etched mesas similar to the source mesas.

2.1.4. Vertical Channel Design

The design of the vertical channel is the most critical part of the unit cell design. The gate is formed by ion implantation. The channel width is defined by the width of the etched source mesa and the gate ion implantation depth. Three sets of Al implantation are applied on the lower half part of the gate trench to form the vertical channel and to create gate ohmic contact. The first Al implantation (p+) is applied mainly on the sidewall of the gate trench with a tilted angle so that a vertical channel with a certain height and opening can be established. The second Al implantation (p+ body) is applied on the bottom of the gate trench to form the high-voltage blocking junction and the last shallow Al implantation (p++) on the bottom of the gate trench to form the gate ohmic contact. The designed profiles of p+ implantation along a horizontal line across the channel is shown in Figure 2.11.

The implantation profile is simulated by ProfileCode™ with Person IV distribution assumption [39]. It was previously found that the simulation software does not accurately predict the implantation tail [40] and the tail of aluminum is approximately modeled by a

linear slope of 0.1µm per decade. The implantation depth is defined by the intersection of the modeled implantation profile, including the approximated tail, and the channel doping concentration.

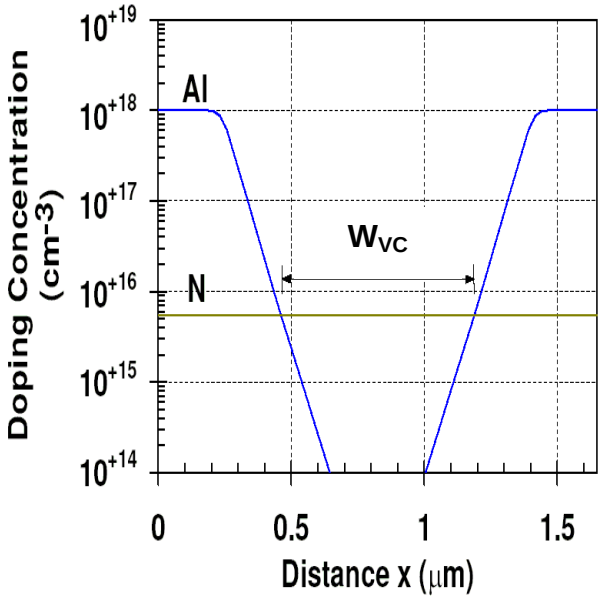


Figure 2.11. Gate implantation profile defining the vertical channel width.

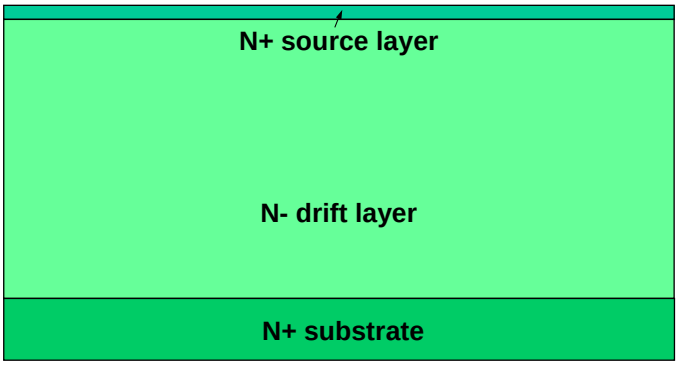
2.2. Process Design

2.2.1. Major Fabrication Steps

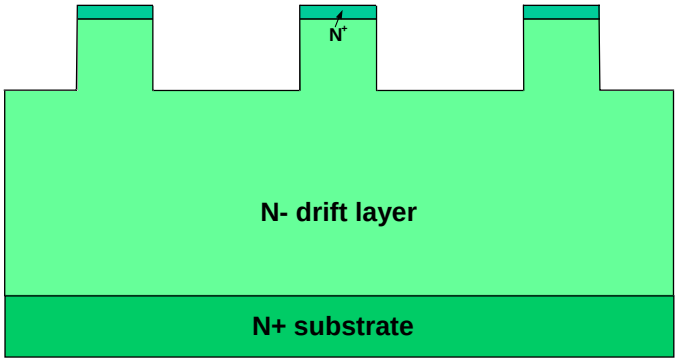
The major fabrication steps are as follows (Figure 2.12):

- Source mesa formation (Figure 2.12(b)).
- Gate and termination formation by p^+ implantation and dopant activation annealing (Figure 2.12(c)).
- Surface passivation by SiO_2 and Si_3N_4 (Figure 2.12(d)).
- Gate contact formation (Figure 2.12(e)).
- Source contact formation (Figure 2.12(e)).
- Drain contact formation (Figure 2.12(e)).

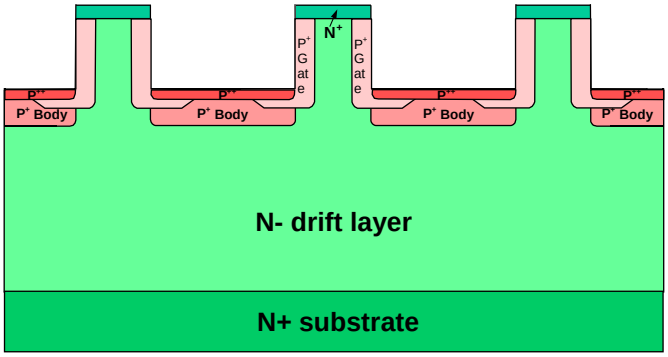
- Trench filling planarization (Figure 2.12(f).
- Source metal overlay formation (Figure 2.12(f)).



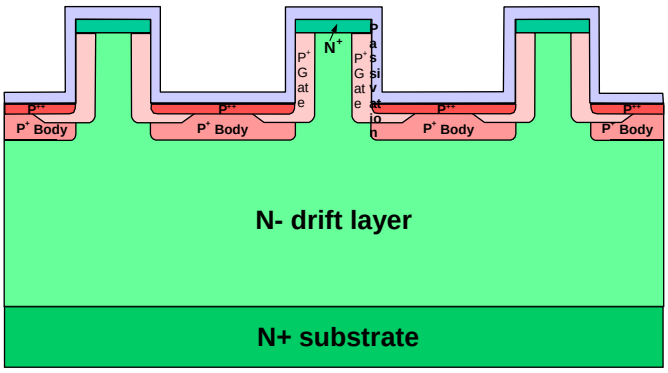
(a) Starting wafer;



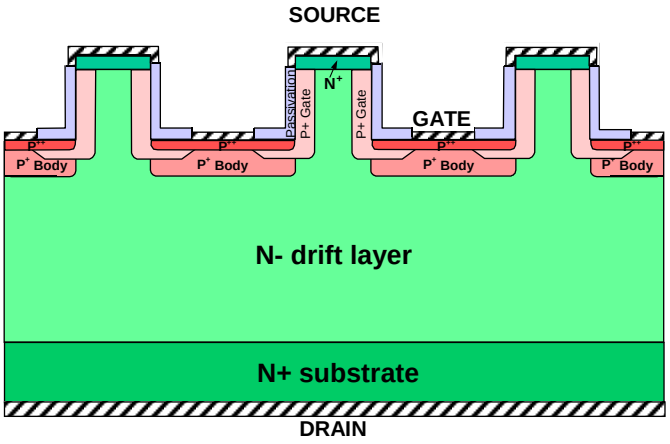
(b) Source mesa formation;



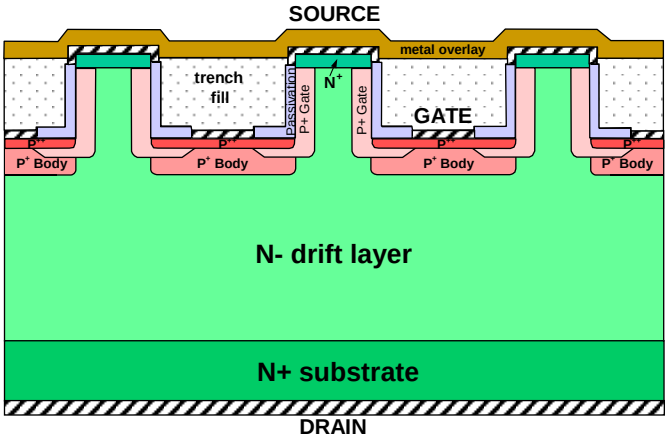
(c) Gate and junction termination formation by p^+ implantation and dopant activation annealing;



(d) Surface passivation by SiO_2 and Si_3N_4;



(e) Gate, source and drain contact formation



(f) Trench filling planarization and source metal overlay formation

Figure 2.12. (a)-(f): Fabrication steps of TIVJFET structure.

Source mesa formation: The first part of the fabrication is the mesa-etching process to create the mesas in the 4H-SiC epitaxial wafer pieces. The etching is done with an ICP

etching system; the etching masks are made of AlTi film, which is patterned by standard photolithography with wet chemical etching.

Gate and junction termination formation: Implantation for gate and junction termination includes three parts: body vertical implantation by high-energy implanter, sidewall skew implantation for gate p-type region and vertical implantation for p-type ohmic contact. Since n-type doping is done during epitaxial growth all implantations required for the device are Aluminum ion implantations. Post implantation annealing at 1550^{o}C for 30 min in Argon is done to activate the implanted Al impurities and recover the damaged crystal structure. Two different approaches are considered for the junction termination – Junction Termination Extension (JTE) and Guard Rings (GR). The JTE is created by the Aluminum implantation done to form the vertical gate. The JTE region needs to be thinned down by dry etching in order to achieve the charge balance that will give the desired field suppression at the device periphery. The optimum etching depths of the JTE steps need to be determined experimentally on a test sample. After the optimal etch depth is found the etching of the main sample is done. Guard ring termination is created by etching ring mesas at the same time with the source mesas and later implanting the guard rings together with the gate implantation.

Surface passivation: After thorough cleaning samples are thermally oxidized at 1100^{o}C for 30 min in wet O_2 ambient to form a sacrificial oxide. The sacrificial oxide is then removed and another thermal oxidation is done at 1100^{o}C for 3 hours in wet oxygen ambient to passivate the surface. The oxide is then annealed at 1100^{o}C for 1 hour in Ar. The thermal oxide is then covered with a PECVD Si_3N_4 layer with thickness of 0.2μm.

Gate, source and drain contact formation: For the gate contact two options are possible – with alignment and with a self-aligned process. By the alignment method windows are opened in the passivation by photolithography and dry etching. Gate contact metal of Ti/TiN with a total thickness of 3000Å is deposited by sputtering on the sample surface. The metal is patterned by a lift-off process. The metal is finally annealed to get ohmic contact. Self-aligned process uses photoresist planarization. Metal layer of Ti/TiW with a total thickness of 3000Å is sputtered over the device active area. Photoresist planarization is then performed and the metal is etched from the source region surface by a wet etching process. The metal is annealed together with the source and drain metals. For the source ohmic contact a self-aligned lift-off process is utilized. First, the passivated surface is planarized by photoresist deposition. Second, the planarized surface is etched back until all the mesa tops are exposed. Then, Ni/TiW contacts are deposited by sputtering and lift-off. A contact to the drain is formed by sputtering AlTi/Ni (200/3000Å) on the wafer back side. High temperature annealing is done at a temperature $\geq 950^{o}C$ to form both source and drain ohmic contacts. Alternative method for self aligned method for source and gate metal definition is possible, based on nickel silicides. After the ohmic contacts are formed the additional gate metal can be deposited to reduce the gate resistance. This is done by photoresist planarization and metal wet etching.

Trench filling planarization and source metal overlay: This fabrication step consists of two phases. First, thick dielectric material is deposited and then etched back to expose the source contacts. Second, thick metal overlay consisting of Al/Ti/Au is deposited and patterned. There are two choices for the planarizing dielectric. Polyimide is relatively easier to planarize, but its high temperature capabilities are limited. SiO_2 is

more difficult to planarize, but it ensures device performance capabilities at higher temperatures.

2.2.2. Critical Fabrication Steps – Challenges and Improvements

Gate trench etching: Channel width, especially for normally-off devices, is very sensitive to process non-uniformity. To establish a god control of the vertical channel width the fabrication process has to ensure line-width uniformity, good vertical mesa profile and smooth mesa sidewall. Photoresist spinning conditions should be adjusted to give maximum thickness uniformity. The metal mask wet etching conditions should be optimized to get uniform etching along the sample. Plasma-etching conditions should be refined to provide a vertical mesa sidewall as much as possible.

Gate implantation: Implantation for vertical gate is a critical step in the fabrication, as it defines the vertical channel width, which determines the device normally-off behavior. Aluminum is used to create the p-type regions. The gate implantation consists of three parts. First, an Aluminum vertical implantation is done to form the blocking junction. Second, the vertical gate is formed by Al implantation on the sidewalls. The third part of the implantation is shallow implantation with high concentration for the gate contacts. The most critical part of the design is the vertical sidewall implantation. This Al implantation needs to be done at a tilted angle so that the p+ regions are established with a certain thickness at the sidewalls. The tilt angle is chosen based on the consideration that shadowing from neighboring mesas should not occur. Another concern with the gate implantation is the masking. The source should be covered with a mask during the implantation. The mask should be patterned by photoresist planarization, metal deposition and lift-off. This method, however, is more time consuming and can achieve a

limited mask thickness. Another more practical approach is to do the implantation for gate without covering the source mesa tops with a mask. After the gate implantation the top of the source mesas is removed by planarization and dry etching process.

Self-aligned Gate and Source Contacts: One of the most challenging steps in the fabrication is to define gate contacts in the gate trenches. The gate trench is only about 2μm-wide and it needs to be covered with metal, while keeping this metal safely away from the source contact that is on the top of the source mesa. The initial self-aligned process uses the following procedure for metal formation. The gate metal is defined by metal sputtering, photoresist planarization and metal wet etching. The source metal is defined by photoresist planarization, metal sputtering and metal lift-off process. For increased area devices the planarization nonuniformity becomes more significant and metal lift-off process becomes less reliable, which may lead to partial gate and source metal contact shorting.

A second method for source contact metal definition, based on a new self-aligned approach is possible without using a lift-off step. First, the gate is filled with silicon dioxide deposited by PECVD, prior to source metal deposition. Second, a photoresist planarization is performed. Third, a new self aligned method for source metal definition is applied, based on nickel silicides. The idea utilizes the fact that metals, such as nickel (Ni), react with SiC when heated to form silicides, but will not react with SiO2. Metal is deposited above the source (free of oxide) and the gate trench (covered with oxide). If the contact metal (Ni) is annealed at a high enough temperature it will react with SiC and form silicide on the source, but will not react with the oxide in the gate trench. Then the

un-reacted nickel can be removed by wet etching, so only the silicide that is sitting on the source will remain.

Finally a third method is possible that uses self-aligned nickel silicide contacts for both the gate and the source.

Gate Overlay metal: The device layout is such that the gate is probed at a gate probing pad, which is located on one side of the device. Gate current flowing through the gate metal results in voltage drop along the gate, due to the gate metal resistance. Because the channel opening is controlled through a change in the depletion region width of the gate-to-source p-n junction by applying forward voltage to the gate (in forward conduction mode), it is sensitive to the applied voltage. The resistance of the gate metal, even if not very large, may cause a voltage drop enough to create different opening conditions for the channel in different regions of the device. A device consists of multiple channels connected in parallel. When the channels that are close to the gate probing pad are open and start conducting high current, other remote channels are not yet open enough. If the gate voltage is increased further more channels become fully open, but the control gate-to-source p-n junctions of the channels closer to the gate contact pad start injecting too much gate current. A p-n junction current increases exponentially with the applied voltage, so before all the channels get a chance to open completely some part of the gate starts conducting too much current and contributes most of the allowed gate current. In order to increase device current density and utilize fully the total device active area the gate metal resistance needs to be decreased. This can be done by increasing the gate metal thickness and using metals with lower resistivity.

CHAPTER 3. NORMALLY-OFF HIGH VOLTAGE (11KV) TIVJFET

3.1. Device and Process Design

3.1.1. Unit Cell Design

A cross sectional view of a unit cell TIVJFET structure is shown on Figure 3.1 The wafer structure consists of three n-doped epitaxial layers. The upper heavily doped ($>1\times10^{19}cm^{-3}$) n+ epilayer is used to create the source ohmic-contact. It also serves to define the vertical boundary of the gate-source p-n junction and provides a process margin for the planarization process used to fabricate the device. The second epilayer with a doping of $4.3\times10^{15}cm^{-3}$ and thickness of 3.5μm is used to form the vertical channel. The third epilayer is the drift layer that supports the voltage. The thickness of 120μm and doping of $4.9\times10^{14}cm^{-3}$ were designed so that the device can support a voltage of more than 10kV. A vertical channel is formed by etching source mesas and implanting the gate. The width of the channel is designed to be completely depleted at zero gate bias to ensure normally-off behavior. The width of the gate trench is chosen to be minimum allowed by the fabrication process in order to maximize source-to-gate area ratio and device current density. The device is designed to be able to operate in a large temperature range from 70K to 600K. Since the vertical channel will become more “open” at higher temperature than at lower temperature due to the decrease of the p-n junction built-in voltage with temperature, the design should be performed at the highest temperature.

The gate is formed by ion implantation. The channel width is defined by the width of the etched source mesa and the gate ion implantation depth. Three sets of Al implantation are applied on the lower half part of the gate trench to form the vertical channel and to create gate ohmic contact. The first Al implantation (p+) is applied mainly on the

sidewall of the gate trench with a tilted angle so that a vertical channel with a certain height and opening can be established. The second Al implantation (p+ body) is applied on the bottom of the gate trench to form the high-voltage blocking junction and the last shallow Al implantation (p++) on the bottom of the gate trench to form the gate ohmic contact. The designed profiles of p+ implantation along a horizontal line across the channel is shown in Figure 3.1(b).

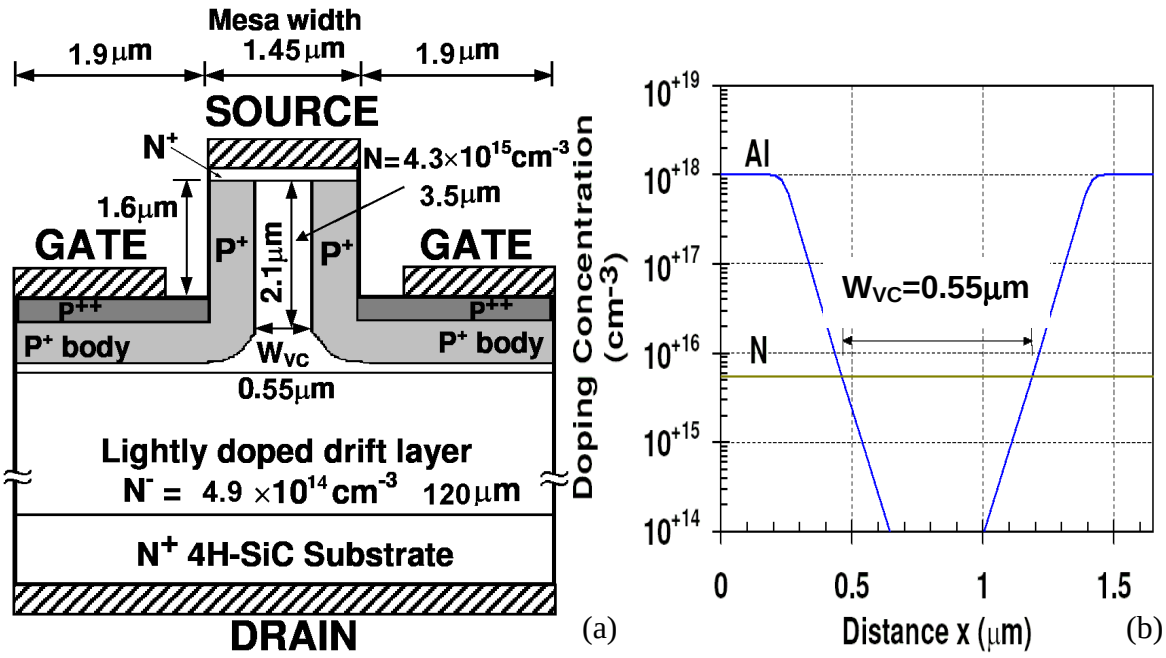


Figure 3.1. (a) Unit Cell Structure of 10kV 4H-SiC TIVJFET; (b) Gate implantation profile.

3.1.2. Device Layout and Photomask Design

The complete device layout design is shown on Figure 3.2. The active area contains a number of source lines (“fingers”) surrounded by a gate region. A gate contact pad was designed with dimensions large enough to ensure probing and wire bonding capability. The device active area is surrounded by a three-step Junction Termination Extension (JTE) area that is used to suppress the high electric filed at device periphery. The width

of each step is 100mm, forming a total width of 300mm, enough to ensure that the electric filed in the JTE region will be lower than the vertical filed in the bulk of the blocking epilayer. Test p-n diodes and TLM structures were also included in the design to evaluate the effectiveness of the termination and the quality of the ohmic contacts.

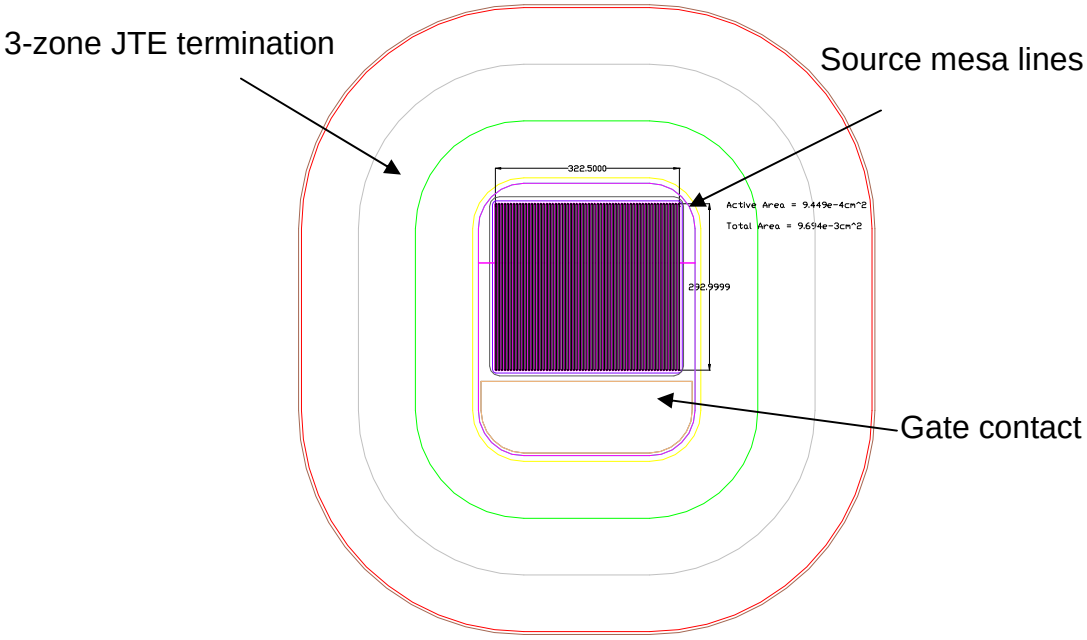


Figure 3.2. 10kV TIVJFET layout design.

A set of masks suitable for self-aligned processing of SiC HF-TIVJFETs has been designed. This set of masks has been manufactured and used for the fabrication of the device. The mask set includes the following masks:

(1) Source Mesas;

(2) JTE-1;

(3) JTE-2;

(4) JTE-3;

(5) JTE-Implant;

(6) JTE-Mesa;

(7) Gate Contact;

(8) Gate Pad Window;

(9) Metal Overlayer;

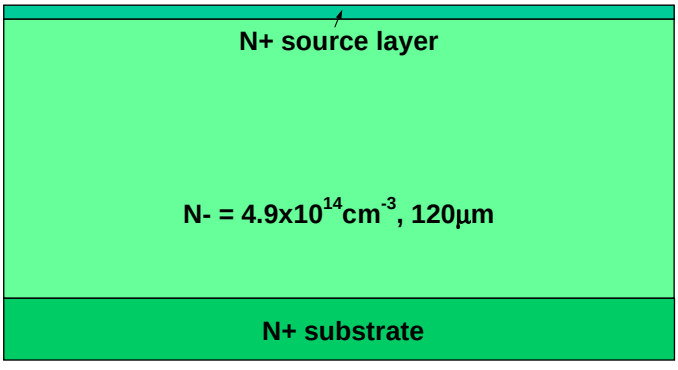
(10) Planarization Help;

(11) Oxide Etching Active Area.

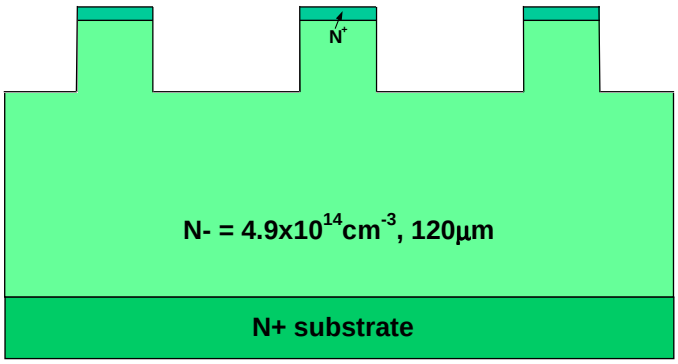
3.1.3. Process Design

The major fabrication steps are as follows (Figure 3.3):

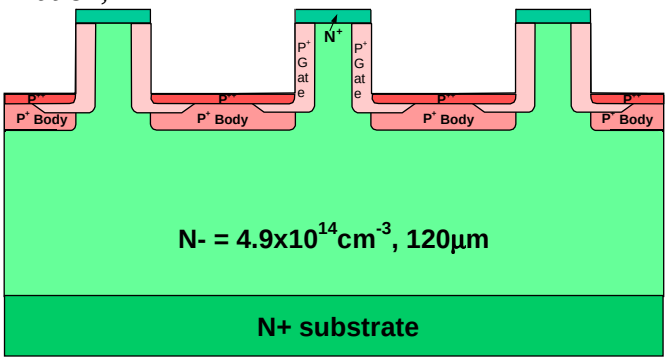
- Source mesa formation (Figure 3.3(b)).
- Gate and termination formation by p^+ implantation and dopant activation annealing (Figure 3.3(c)).
- Junction Termination Extension (JTE) formation by ICP etching (Figure 3.3(d)).
- Surface passivation by SiO_2 and Si_3N_4 (Figure 3.3(e)).
- Source contact formation (Figure 3.3(f)).
- Drain contact formation (Figure 3.3(f)).
- Gate contact formation (Figure 3.3(f)).
- Trench filling planarization and source metal overlay formation (Figure 3.3(g)).



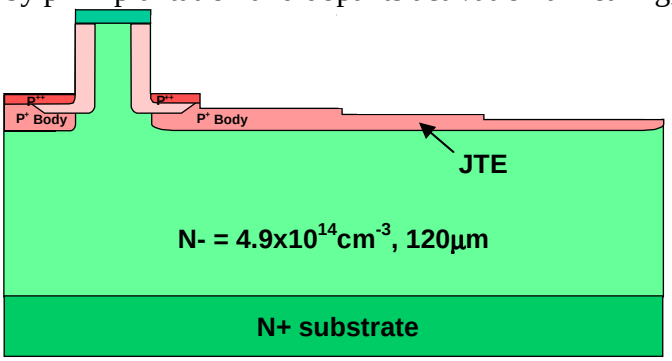
(a) Starting wafer;



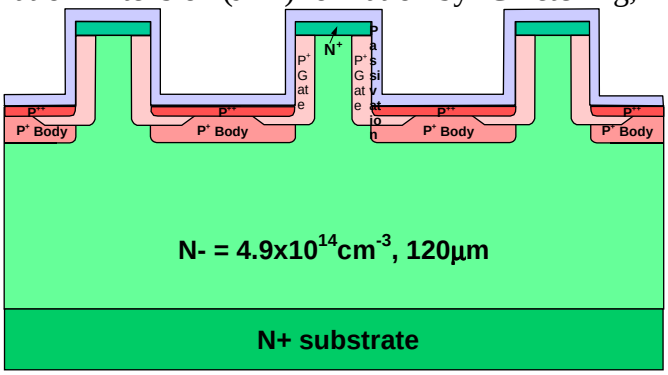
(b) Source mesa formation;



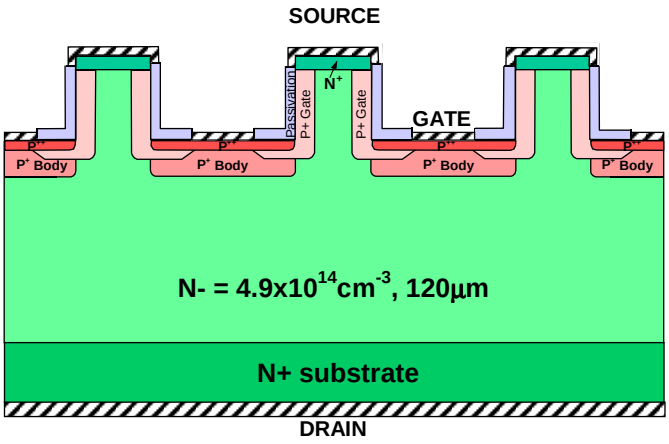
(c) Gate formation by p^+ implantation and dopants activation annealing;



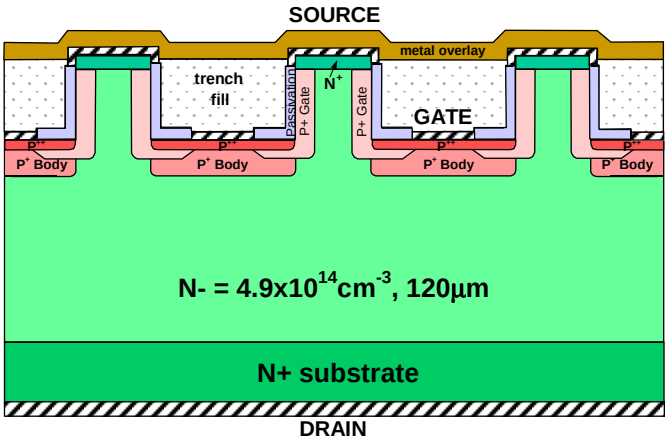
(d) Junction Termination Extension (JTE) formation by ICP etching;



(e) Surface passivation by SiO_2 and Si_3N_4;



(f) Source, drain and gate contact formation



(g) Trench filling planarization and source metal overlay formation

Figure 3.3. (a)-(g): Fabrication steps of normally-off TIVJFET structure.

3.2. Fabrication

3.2.1. Source Mesa Formation

The device fabrication starts with etching of the deep trenches by inductively-coupled plasma (ICP) using CF_4 and O_2 gas mixture, forming a source mesa array. The etching masks are made of AlTi (Ti: 3.5% by weight) film, which is patterned by standard photolithography with wet chemical etching. A 2000-Å thick layer of AlTi was deposited by sputtering on the 4H-SiC wafer pieces. The deposited metal film was then patterned by the photomask “(1) Source mesa” for mesa definition with mesa width of 2.25µm.

After that the gate trenches were etched in an ICP etcher in CF_4+O_2 plasma. The etching was done in several runs and the final etched depth was 3.2μm.

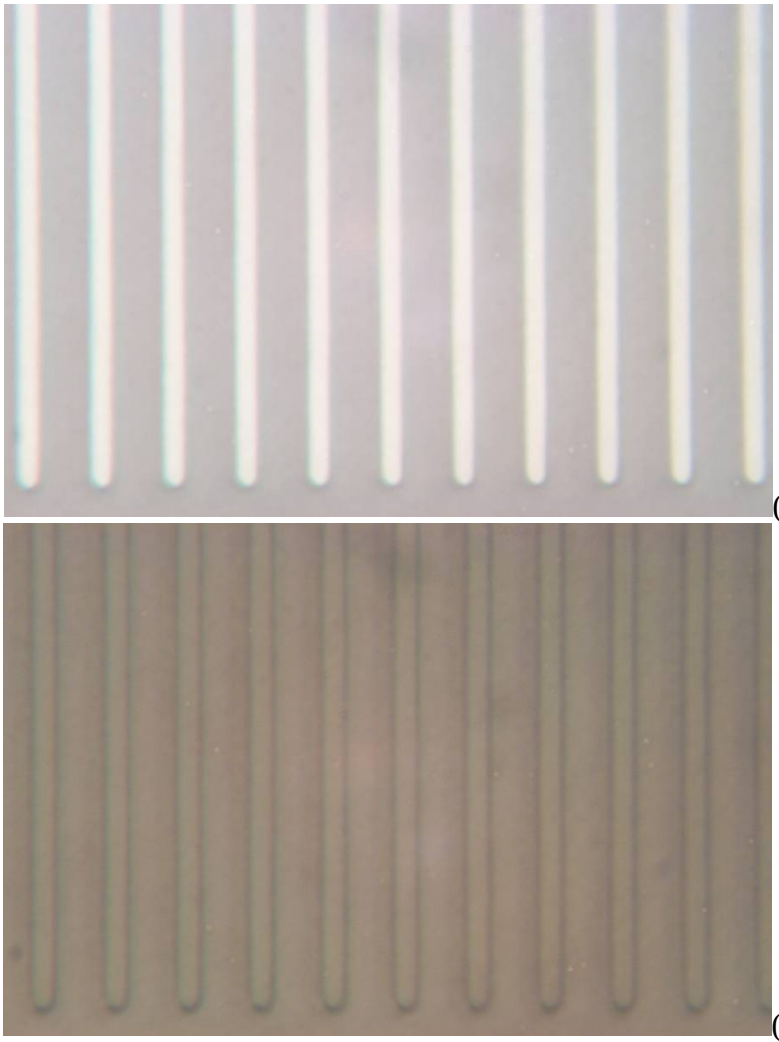


Figure 3.4. Optical microphotograph of source mesas: (a) AlTi pattern for ICP etching of source mesas; (b) etched source mesas. Structure period is 5.5μm.

3.2.2. Gate and Termination Formation by P+ Implantation and Dopant Activation Annealing

Implantation for Gate and JTE include three parts: JTE vertical implantation by high-energy implanter, sidewall tilted implantation for gate p-type region and vertical implantation for p-type ohmic contact. Owing to the presence of the deep-trenched

structures, self-alignment processes become possible based on planarizing the coating of photoresist and etching-back by oxygen plasma to expose the mesa tops for a blank metal sputtering and the subsequent self-aligned metal mask formation by lift-off. The implementation of the multi-step implantation structure of the gate becomes greatly simplified by the use of self-aligned implantation masks placed on the mesa top (Figure 3.5).

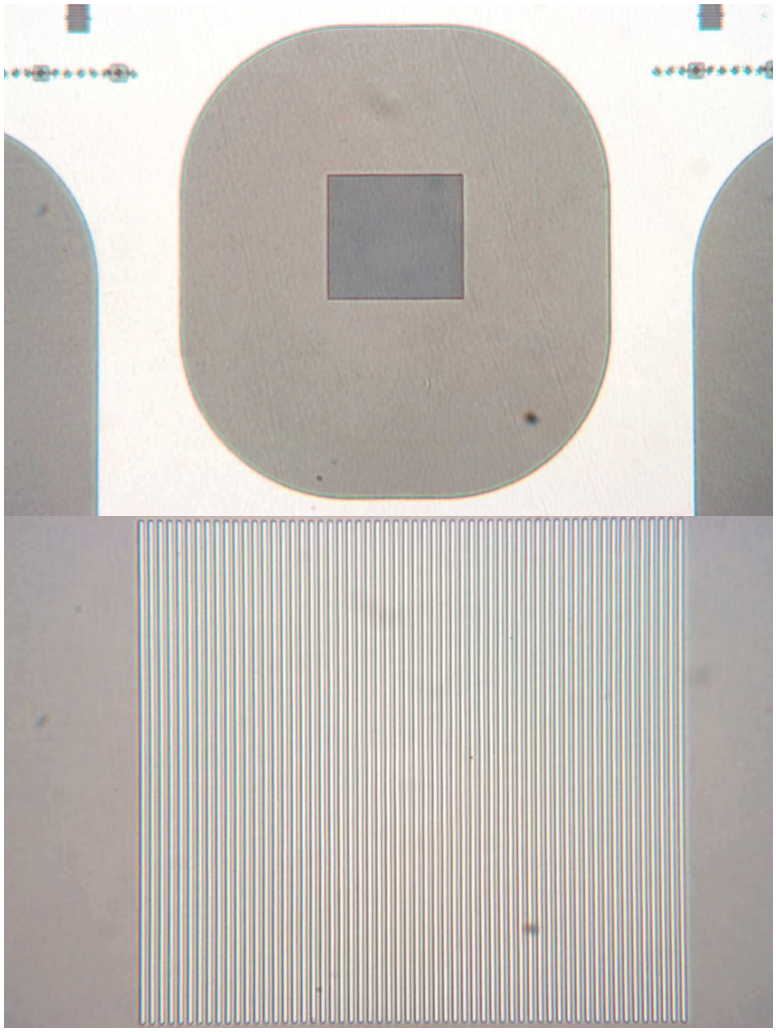


Figure 3.5. Optical microphotograph of Mo implantation mask for gate and JTE implantation (a) complete device view; (b) source mesa only view.

Once the implantation metal mask is formed on the mesa top, the sample is subjected to a three-step Al implantation, followed by removing the implantation mask

and post-implantation annealing at 1550^{o}C for 30 min. In the first set of implantation, the p^{+} trench bottom regions are created by normal incidence Al implantation while the mesa top is protected by an implantation metal mask. The implantation energies and doses are 570KeV $3\times10^{13}cm^{-2}$, 345KeV $1.8\times10^{13}cm^{-2}$, 200KeV $1.3\times10^{13}cm^{-2}$, and 105KeV $8\times10^{12}cm^{-2}$. The second set of Al implantation is applied mainly on the sidewall of the deep trench with a tilted angle so that a vertical channel with a length of 2.1μm and an opening of 0.55μm can be formed. For this set of Al implantation, the implantation energies and doses are 240KeV $3.1\times10^{13}cm^{-2}$, 100KeV $1.2\times10^{13}cm^{-2}$, and 25KeV $3\times10^{12}cm^{-2}$, and the implantation angle was 35^{o} with respect to the sample normal. The third set of Al implantation is applied on the bottom of the deep trench to create shallow p^{++} regions with a peak concentration of $9\times10^{19}cm^{-3}$ for gate ohmic contact. After gate implantation, the sample is annealed at 1550^{o}C for 30 min in Ar ambient to activate the implanted Al.

3.2.3. Junction Termination Formation

Three-step junction termination extension (JTE) was employed to reduce the electric field at the device periphery. This JTE is created by the Aluminum implantation done to form the vertical gate. The JTE region needs to be thinned down by dry etching in order to achieve the charge balance that will give the desired field suppression at the device periphery. The optimum etching depths of the JTE steps need to be determined experimentally. For this purpose, a 4H-SiC dummy piece cut from the same wafer, in which all the implantations and the post-implantation annealing have been performed together with the device samples, was prepared. The dummy piece was then processed to have simple p^{+}-n^{-} diodes with three-step JTE with the step width of 100μm. The outer

steps were etched to 300Å. The inner step depth was gradually increased by repeated ICP etching while the reverse I-V characteristics were monitored at every etching run. The results are shown in Figure 3.1.5

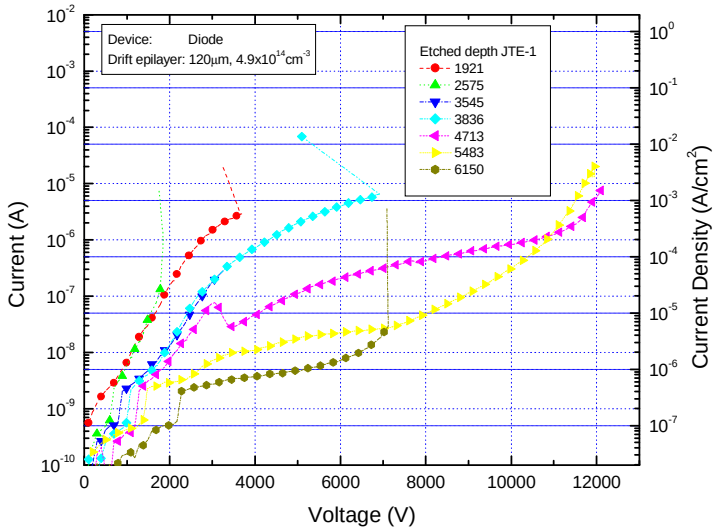


Figure 3.6. 12kV MJTE optimization.

3.2.4. Surface Passivation

After thorough cleaning the samples were then thermally oxidized at 1100^{o}C for 30 min in wet oxygen ambient to form a sacrificial oxide with a thickness of approximately 150Å. The sacrificial oxide was then removed by HF and another thermal oxidation was done at 1100^{o}C for 3 hours in wet oxygen ambient. The oxide was then annealed at 1100^{o}C for 1 hour in Ar. The oxide thickness is estimated to be about 600Å. After that a 2000A-thick layer of silicon nitride was deposited by PECVD.

3.2.5. Source and Drain Contact Formation

For source contact formation the passivation dielectric is removed from only the mesa tops and the source Ni/TiW contacts are defined by using a self-aligned process. The self-aligned process consists of photoresist planarization, metal deposition by sputtering and

subsequent lift-off. Next, the drain contact was formed on the samples back side by removing the passivation oxide by etching in buffered HF and depositing Al/Ni (200/3000Å) by sputtering. Annealing of source metal is performed at 1050^{o}C for 10min together with the drain metal to form ohmic contacts. Figure 3.7 shows the device after the source contact was formed.

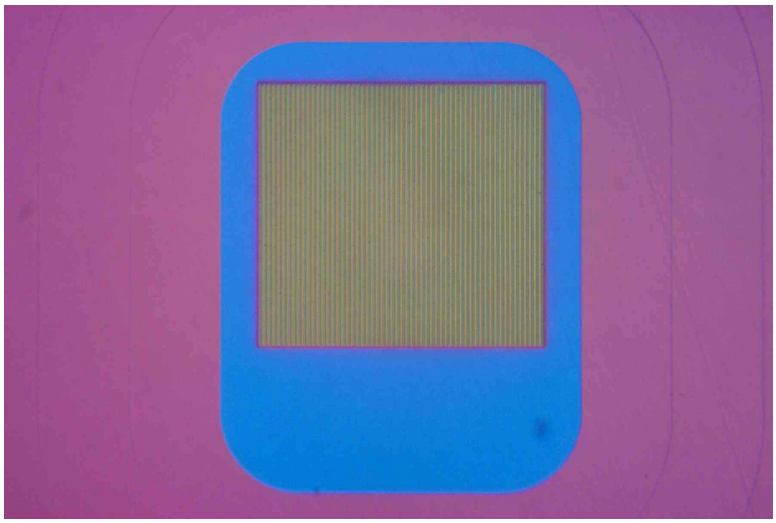


Figure 3.7. Optical microphotograph of 11kV TIVJFET after source contact formation.

3.2.6. Gate Contact Formation

Next, the first and only photolithographic critical alignment is made to open windows in the passivation for gate contacts. Windows in oxide/nitride were etched in ICP using Freon and oxygen mixture plasma. Gate contact metal of Ti/TiN (1500Å/1500Å) was deposited by sputtering on the sample surface. The metal was patterned by a lift-off process. The metal was finally annealed at 700^{o}C for 10min to get an ohmic contact. Figure 3.8 shows the device after the gate contact was formed.

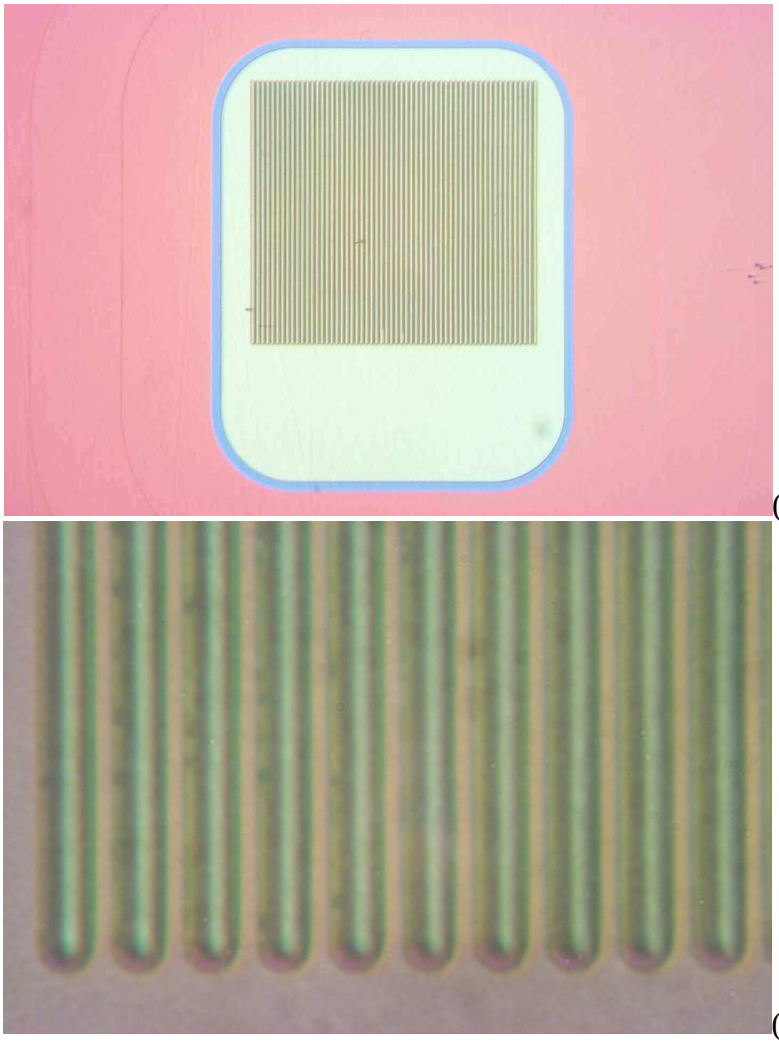


Figure 3.8. Optical microphotograph of 11kV TIVJFET after gate contact formation: (a) complete view; (b) source and gate close-up.

3.2.7. Trench Filling Planarization and Source Metal Overlay

This fabrication step consists of two phases. First, thick polyimide coating was deposited, cured at temperature > 350^{o}C and then etched back in oxygen plasma to expose the source contacts. Second, thick metal overlay consisting of Al/Ti/Au with a total thickness of 2µm was deposited and patterned by lift off. The fabricated device is shown on Figure 3.9. Finally the device was packaged in a high-voltage-operation capable package (Figure 3.10).

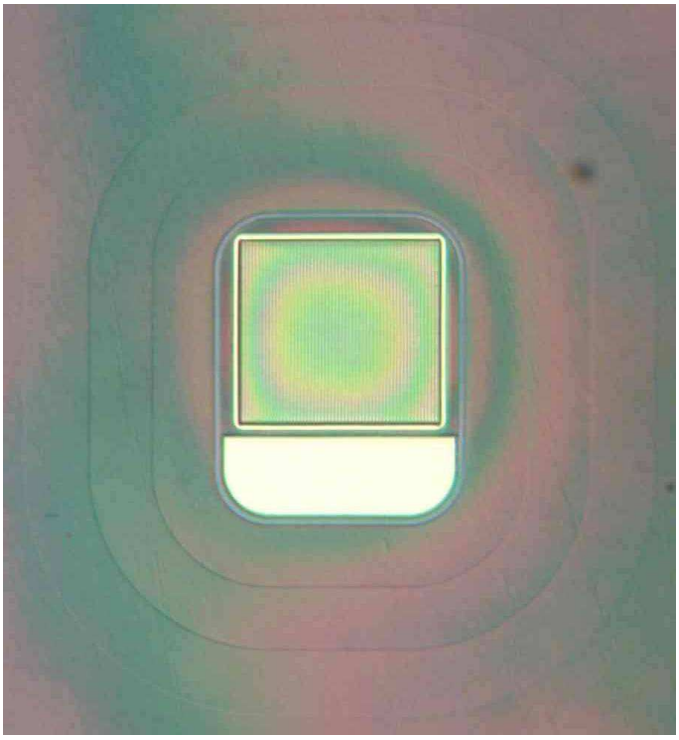


Figure 3.9. Fabricated 11kV normally–off TIVJFET.

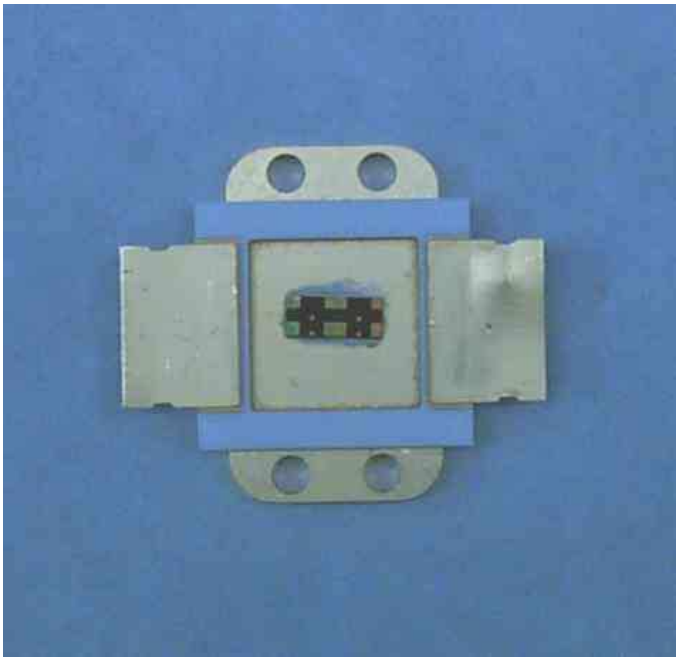


Figure 3.10. Packaged 11kV normally–off TIVJFET.

3.3. Characterization

Figure 3.11(a) shows the dependence of the drain current I_D (current density J_D) on the drain voltage V_D of a fabricated TIVJFET. The current density in Figure 3.11 is for the on-state forward current density normalized to the source area. The leakage current in the blocking mode is amplified by 1000× in order to show the detail. The blocking voltage is measured up to 10,400 V with a leakage current I_D=1.6mA/cm^2 at V_G=0, which is 67.7% of the theoretical breakdown voltage of 15,364V for this structure obtained from computer simulation. The leakage current of 1.6μA at 10.4kV represents a leakage current density of 0.5mA/cm^2 when normalized to the device blocking junction area which is responsible for the generation of the leakage current in blocking mode. As can be seen, the leakage current slightly decreases as the blocking voltage is increased beyond about 7000V. The reason for this anomaly is not clear but could be due to trapping effects. Figure 3.11(b) shows another TI-VJFET tested up to 11,000V without the anomaly. The higher gate voltage needed for this device is most likely due to the narrower channel opening, revealing the need to improve process uniformity. As can be seen in Figure 3.11, which shows a high forward current density of 50A/cm at V_D=7.2V and V_G=4V and 22.2A/cm at V_D=3V and V_G=3.5V, respectively, the specific on-resistance R_{SP-ON}, normalized to the source active area of 320.25×293μm is 130mΩ.cm^2 at V_D=3V and V_G=3.5V, which is lower than the theoretical R_{SP-ON} of 166mΩ.cm^2 of the 120μm drift layer, assuming an ideal electron mobility for 4H-SiC of 947cm^2/Vs. The observed lower is due to current spreading effect. Testing of packaged TIVJFETs (Figure 3.12) has reconfirmed the blocking voltage up to 11kV and shown a lower R_{SP-ON} of 124mΩ.cm^2.

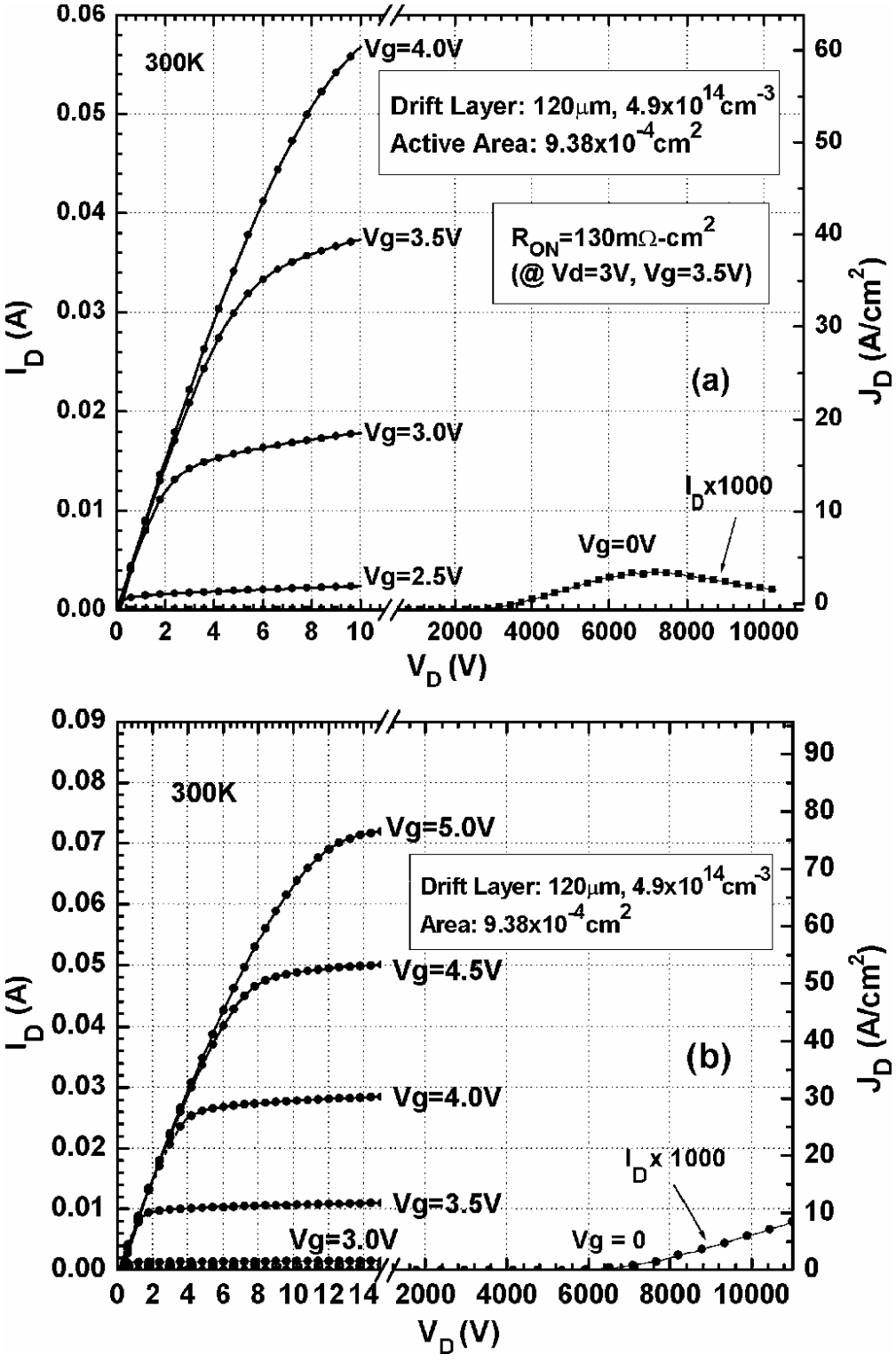


Figure 3.11. Measured dependence of drain current (current density) versus drain to source voltage of (a) a 10.4 kV and (b) an 11 kV 4H-SiC TI-VJFET.

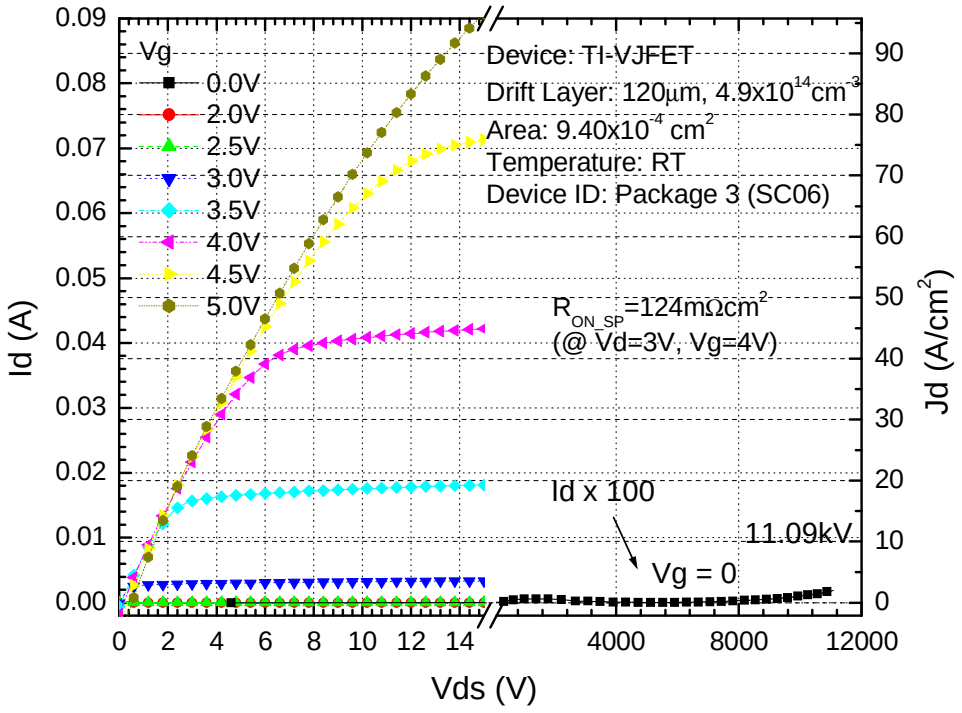


Figure 3.12. I-V curves of a packaged 11kV TIVJFET.

In the actual device, the active region is rectangular with a dimension of 320.25×293μm. The active region is surrounded by a three-step JTE region, which has a width more than 300μm. Thus, the electron collecting area at the drain side is substantially larger than the active area. Three-dimensional device simulation has been performed to investigate the current spreading effect and evaluate the theoretical $R_{SP\text{-}ON}$ of the drift layer of the TI-VJFET when the current spreading effect is taken into account. Figure 3.13 presents the simulated electron current density near the drain contact along a straight line parallel to the longer side of the active region. It is seen from Figure 3.13 that there is indeed a large mount of current in the region under JTE although the current density decreases rapidly away from the active region. Because of the very nonuniform and rapidly decreasing current density outside the active region, a unique device $R_{SP\text{-}ON}$ can not be defined. A useful characterization of the device $R_{SP\text{-}ON}$ can be defined as the

ratio of forward voltage drop V_D over the current density J_D at drain side. Obviously, this is position dependent because current density varies with position. The R_{SP-ON} with such a definition is also presented in Figure 3.13. It is seen that is approximately 170mΩ.cm^2 near the center of the active region and increases rapidly away from the active region. If the TIVJFET were substantially larger in size where current spreading at device edge can be neglected, the TIVJFET would have a specific on-resistance of 168mΩ.cm^2, which is the sum of the drift layer specific resistance of 170mΩ.cm^2 and the vertical channel specific resistance of 2mΩ.cm^2.

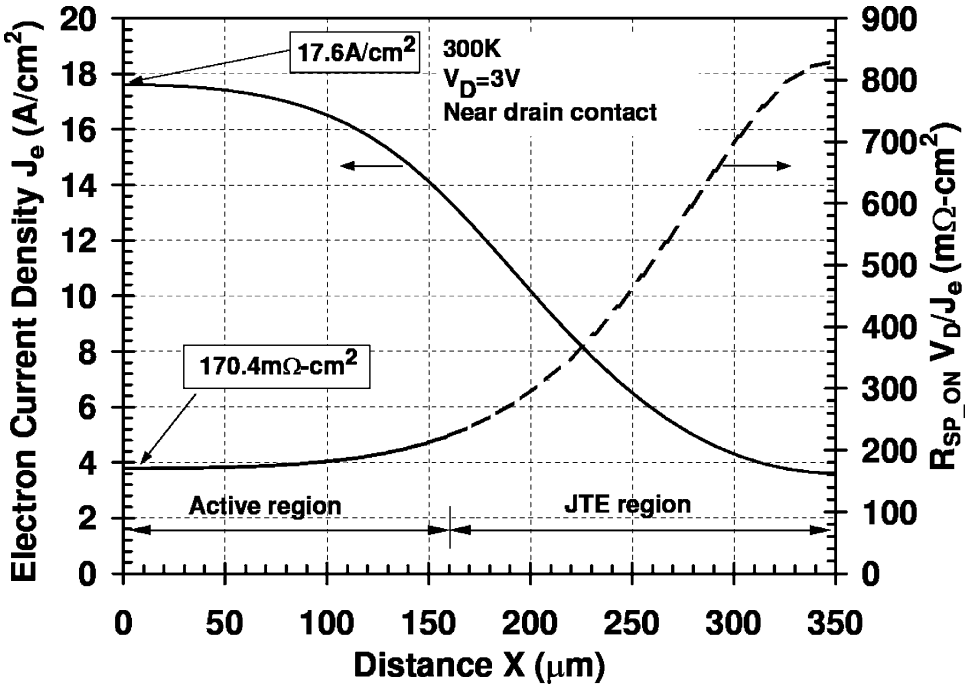


Figure 3.13. Simulated electron current density and R_{SP-ON} near the drain contact at a drain voltage of 3 V. The center of the active region is at X = 0.

CHAPTER 4. NORMALLY-OFF AND NORMALLY-ON HIGH FREQUENCY TIVJFETS WITH A BLOCKING VOLTAGE OF 400V

4.1. Device and Process design

4.1.1. Unit Cell Design

The cross sectional view of the normally-off unit cell of the HF-TIVJFET device is shown in Figure 4.1(a). This structure is designed to be able to block over 400V at a temperature range from RT to 300°C when the gate voltage is zero. Normally-on structures were also designed, using the same gate width and a wider channel. The device pitch size was aggressively minimized to get the maximum current density. The design was made possible based on the use of a self-aligned process to form gate and source contacts.

The wafer structure uses three epilayers. The top layer serves as the source contact layer and has a high doping concentration of $n \sim 1x10^{19} cm^{-3}$ and thickness of 1.6µm, which allows a good control over various planarization steps used throughout the fabrication. The drift layer has a thickness of 3.5µm and a doping concentration of $n=2x10^{16}\ cm^{-3}$.

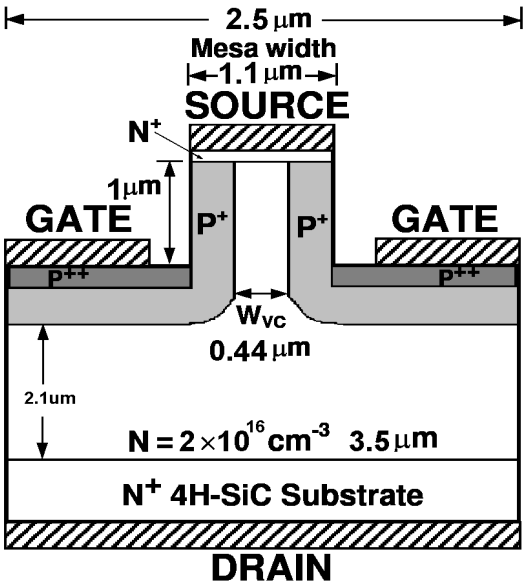


Figure 4.1. (a) Unit Cell Structure of 4H-SiC HF-TIVJFET.

4.1.2. Device Layout and Photomask Design

The complete device layout design includes an active area containing a number of source lines fingers surrounded by a gate region, three-step JTE region, probing pads for the source, gate and drain, and finally wire-bond pads. The smallest dimensions designed were the gate width: 0.5um and 0.75um. Figures 3.2 to 3.4 show design of different cells realized in the design. The probing pads were designed to be used with standard commercially available RF probes. The width of each JTE step is 3μm, with a total width of 9μm. The dimensions of the probing and wire-bonding pad were minimized to reduce parasitic capacitance. Test p-n diodes, TLM structures and some additional test structures were also included in the design to evaluate the effectiveness of the termination and the quality of the ohmic contacts.

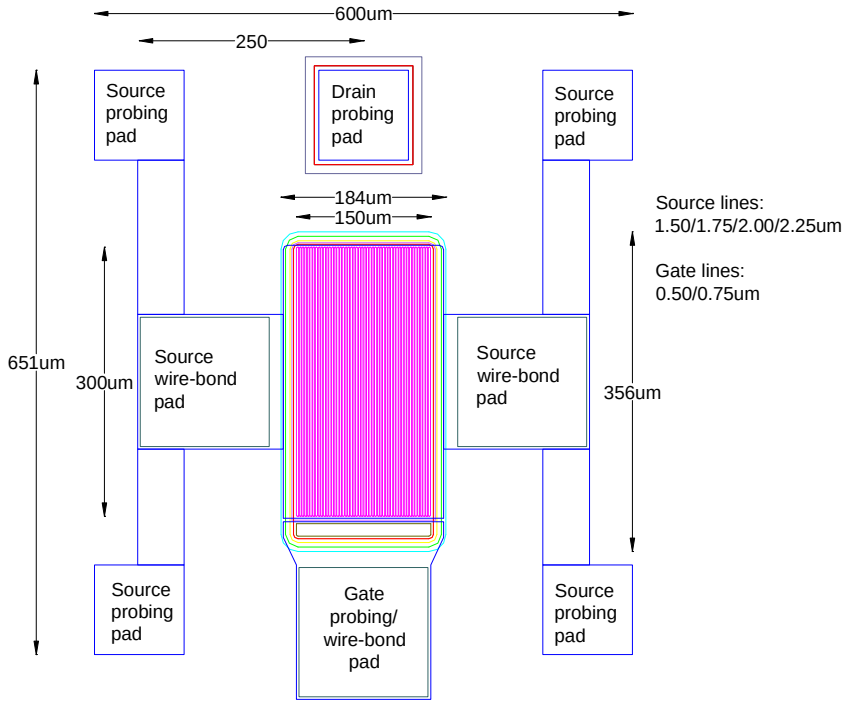


Figure 4.2: Top view of HF-TIVJFET design showing wafer level probing pads and bonding pads – small device type.

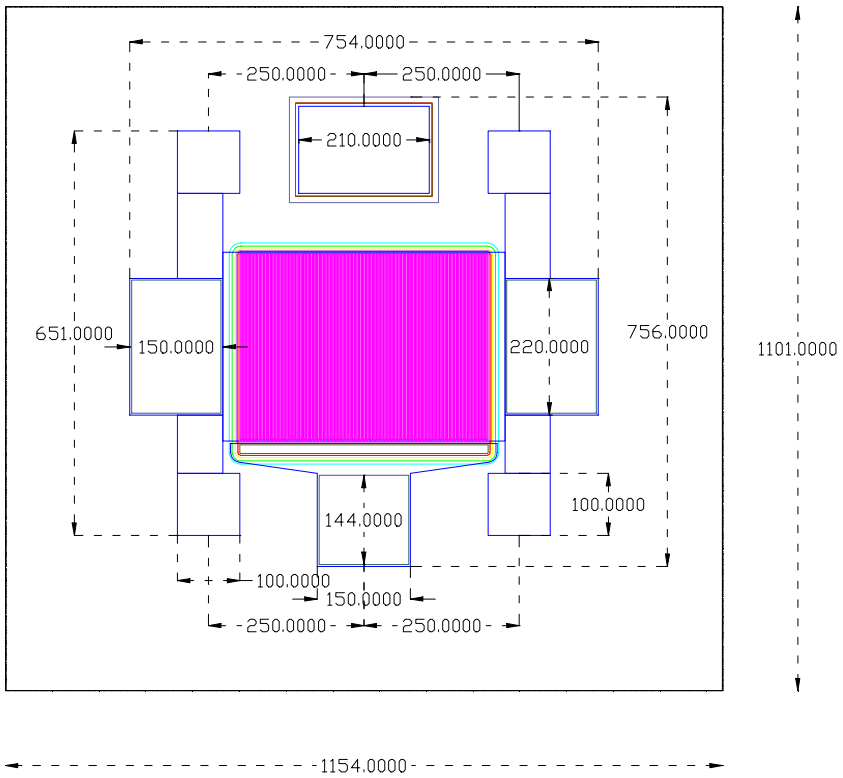


Figure 4.3: Top view of HF-TIVJFET design showing wafer level probing pads and bonding pads – medium device type.

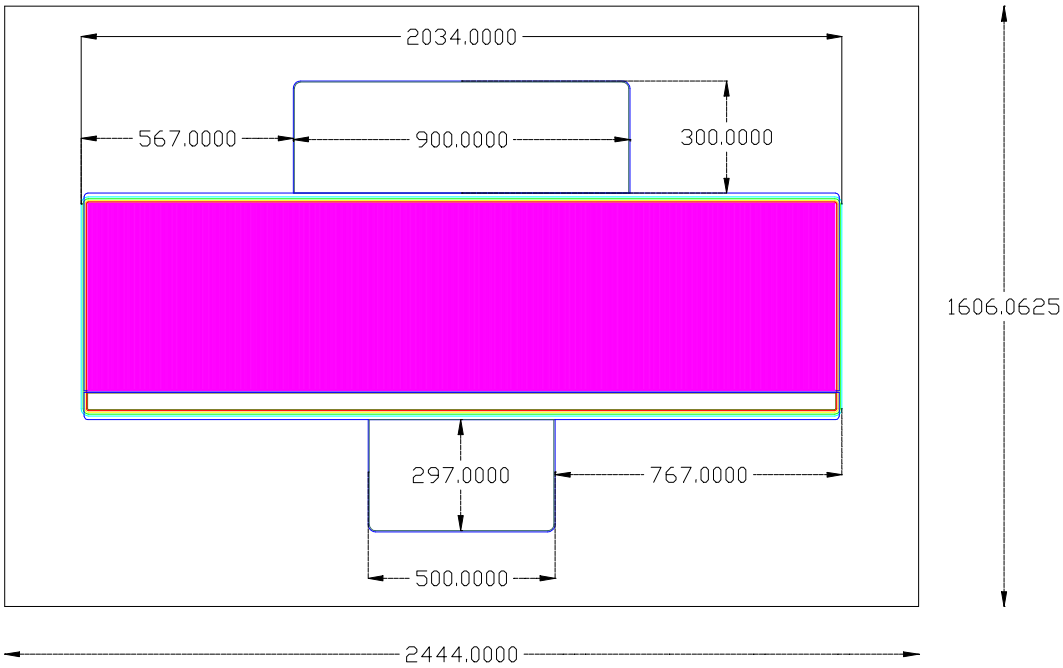


Figure 4.4: Top view of HF-TIVJFET design showing wire bonding pads – large device type.

A major effort was put into the design of a set of HF-TIVJFET masks suitable for normally–off and normally-on switches. The set of masks include:

(1) Alignment marks

(2) Drain Trench

(3) Source Mesa

(4) JTE-1

(5) JTE-2

(6) JTE-3 (Implantation)

(7-1) G-S-D Contact

(7-2) G Contact

(7-3) D Contact

(8) G-D Window Overlay

(9) G-S-D Metal Overlay

(10) G-S Wire-bond Windows

4.1.3. Process Design

4.1.3.1. Process Improvement

For increased power handling capabilities a new device design and improved processing technology were implemented. The design uses reduced source and gate line dimensions that allow achieving higher power density. A new set of mask was used with gate line width of 0.50 and 0.75μm. A number of improvements to the processing technology were introduced to improve device performance and increase processing reliability.

The processing technology was substantially improved to use self-aligned gate contact formation, which reduced the number of critical mask alignment steps to zero.

Gate implantation without source mesa top mask: As the device design uses increased source line density, it becomes very challenging to define an implantation mask covering the thin and dense source mesas. A much more simplified approach is used, in which during the implantation for gate the source mesas are not covered with a mask. After the implantation the top of the source mesas will be inverted into p-type and has to be removed by planarization and dry etching process.

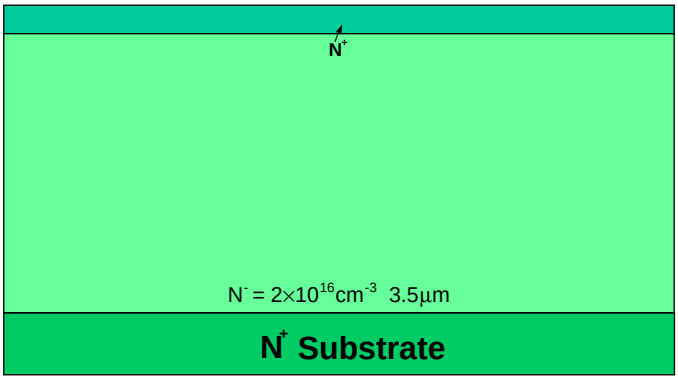
Self-aligned gate contacts: This approach allows the increased source line density design used. A self-aligned process was used to form the gate contact. The approach of photoresist planarization and metal wet etching was used.

4.1.3.2. Fabrication Sequence

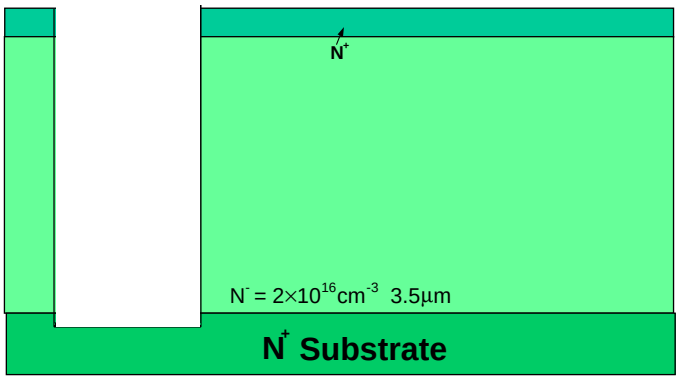
The major fabrication steps are as follows (Figure 4.5):

- Wafer cutting, cleaning, and alignment marks formation.
- Top-side drain trench formation (Figure 4.5(b)).

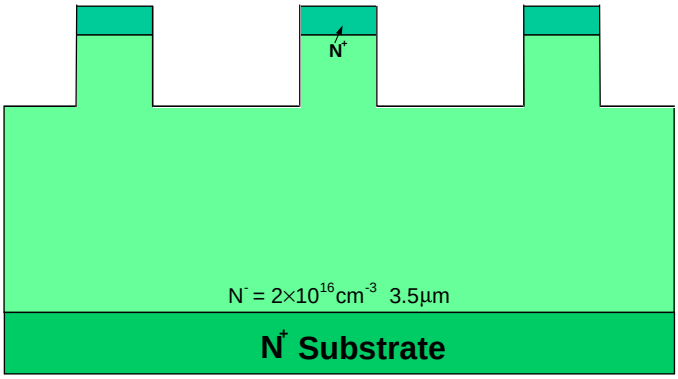
- Source mesa formation (Figure 4.5(c)).
- Gate formation by p^+ implantation and dopant activation annealing (Figure 4.5(d)).
- Removing of Al-implanted source mesa top (Figure 4.5(e)).
- Junction Termination Extension (JTE) formation by ICP etching (Figure 4.5(f)).
- Surface passivation by SiO_2 and Si_3N_4 (Figure 4.5(g).
- Gate contact formation (Figure 4.5(h)).
- Top-side drain contact formation (Figure 4.5(h)).
- Source contact formation (Figure 4.5(h)).
- Ohmic contact metal annealing (Figure 4.5(h)).
- Trench filling planarization (Figure 4.5(i)).
- Metal overlay formation (Figure 4.5(i)).



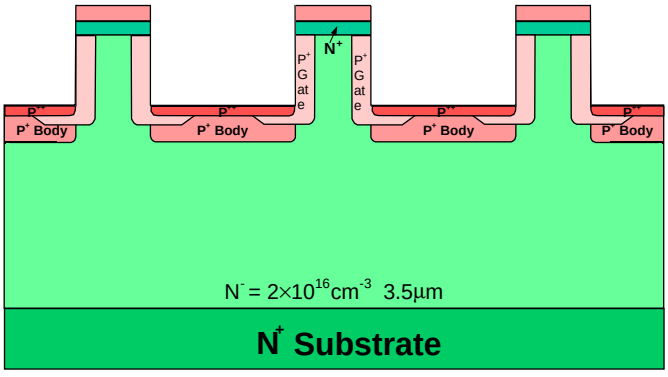
(a) Starting wafer;



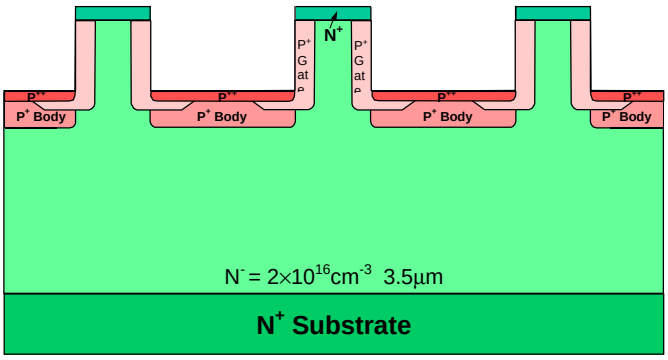
(b) Top-side drain trench formation;



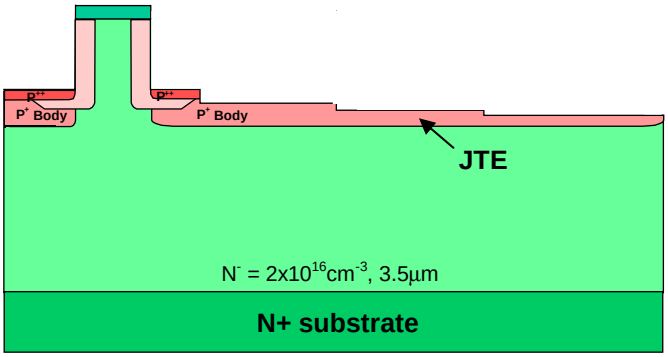
(c) Source mesa formation;



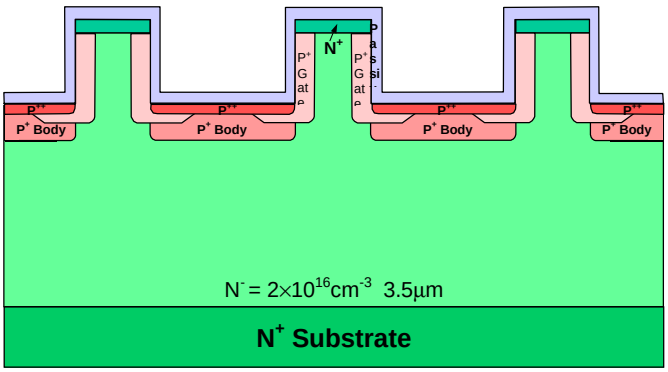
(d) Gate formation by p^+ implantation and dopants activation annealing;



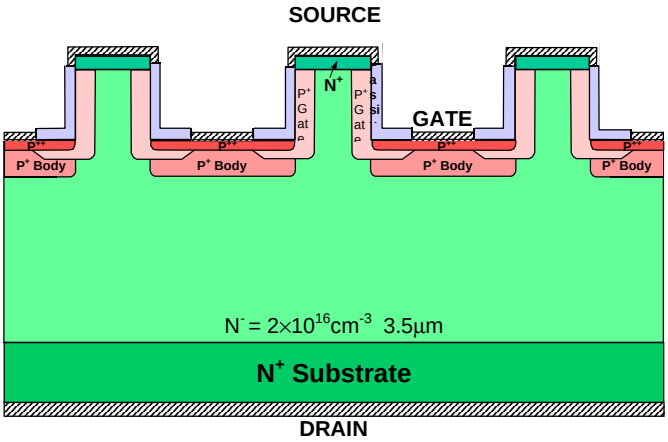
(e) Removing of Al-implanted source mesa top;



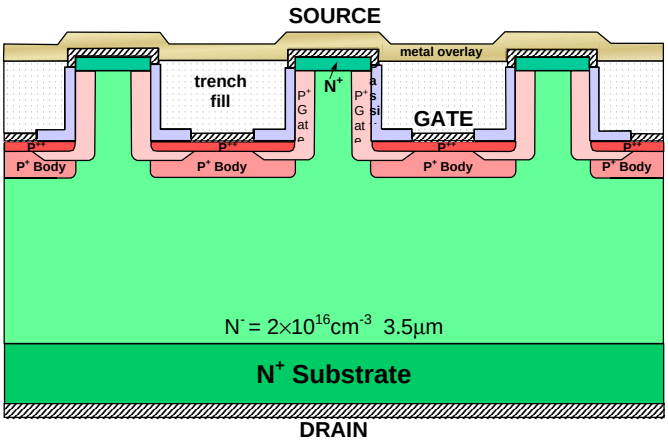
(f) Junction Termination Extension (JTE) formation by ICP etching;



(g) Surface passivation by SiO_2 and Si_3N_4;



(h) Gate, source and drain contact formation;



(i) Trench filling planarization and metal overlay formation.

Figure 4.5. (a)-(i): Fabrication steps of HF-TIVJFET device

4.2. Fabrication

4.2.1. Alignment Marks Formation

Alignment marks, used only for the purpose of alignment of subsequent photo masks, were created by dry etching with inductively coupled plasma (ICP), using an AlTi (Ti: 3.5% by weight) etching mask. First, a 2000Å thick AlTi layer was deposited on the samples surface by sputtering. To pattern the metal lithography was done using the photo mask “(1) Alignment marks”. Then the metal layer was patterned by wet etching in standard Al etching solution. The photoresist was then removed then and the alignment

marks were etched by ICP, which used Freon (CF_4) and oxygen (O_2) gases as etchants. The etching depth was 0.8μm. After the etching, the mask was removed by using diluted HF. The alignment marks could be seen on Figure 4.6 together with a drain trench, which was formed at the next processing step.

4.2.2. Drain Trench Formation

Drain trenches, used for a front-side contact to the drain, were created by dry etching with ICP, using an AlTi etching mask. First, a 5000Å thick AlTi layer was deposited on the samples surface by sputtering. To pattern the metal lithography was done using the photo mask "(2) Drain trenches". Then, the metal layer was patterned by wet etching in aluminum etchant. After that the photoresist was removed by O_2 plasma. Finally, the drain trenches were etched by ICP in CF_4+O_2 gas mixture. The etching depth was 5.7μm. After the etching, the mask was removed by using diluted HF. A drain trench is shown on Figure 4.6.

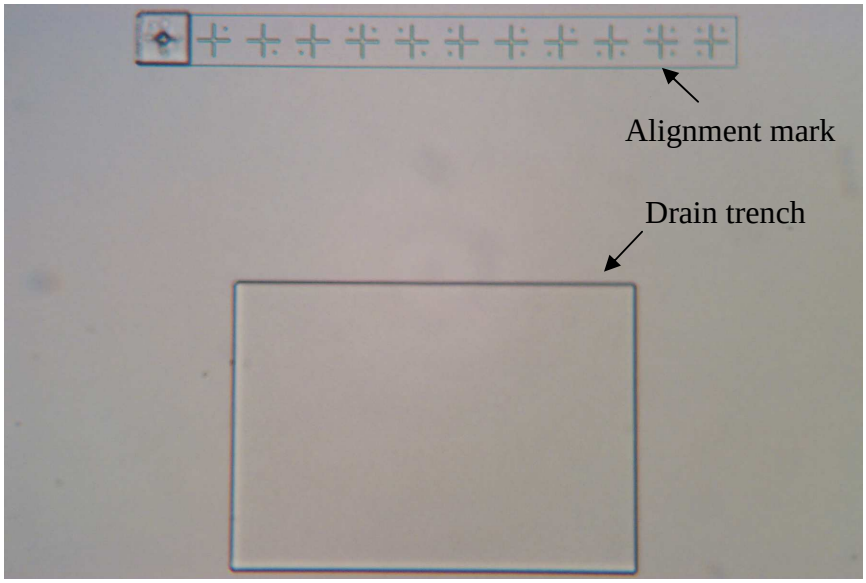


Figure 4.6. Optical microphotograph of a drain trench and alignment mark after AlTi etching mask has been removed.

4.2.3. Source Mesa Formation

The next part of the HF-TIVJFET fabrication is the mesa-etching process to create the mesas in the 4H-SiC epitaxial wafer pieces. The etching is done with an ICP etching system. The etching masks are made of AlTi film, which is patterned by standard photolithography with wet chemical etching. The 4H-SiC wafer pieces were first deposited with 2000-Å thick AlTi by sputtering. The deposited AlTi films were second patterned by the photomask "(3) Source mesa" for mesa definition with four different dimensions – 1.50µm, 1.75µm, 2.00µm, and 2.50µm wide mesas. Third, the AlTi films were etched by a standard Al etching solution. Fourth, the photoresist was removed by oxygen plasma, and the line widths of the AlTi patterns were confirmed under an optical microscope. Figure 4.7 shows an optical microscope photo of the AlTi pattern created by the photomask pattern of 1.75-µm wide mesa stripes; the periodicity of the structure is 2.50µm. In the photo, the width of the AlTi pattern is measured to be 1.4µm, which is about 0.35µm narrower than the corresponding photomask pattern width. Fifth, the SiC pieces with the AlTi etching masks were etched by ICP in CF_4+O_2 plasma to a depth of 2.6µm. Finally, after the ICP etching, the AlTi etching mask was removed by diluted HF. Figure 4.8 shows an optical microphotograph of the SiC mesa pattern created by the ICP etching. The mesa width measured in Figure 4.8 is 0.85µm.

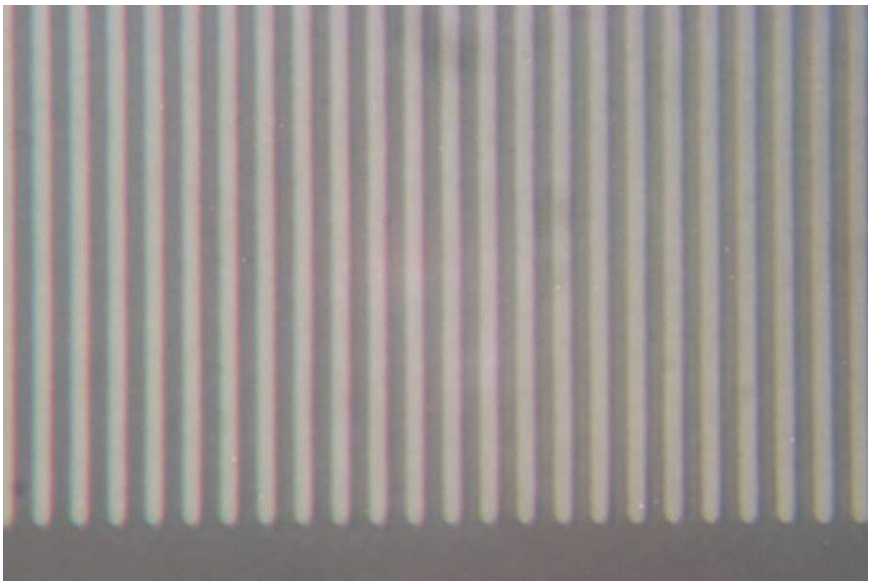


Figure 4.7. Optical microphotograph of AlTi pattern for ICP etching of mesas. The periodicity of the structure is 2.5µm.

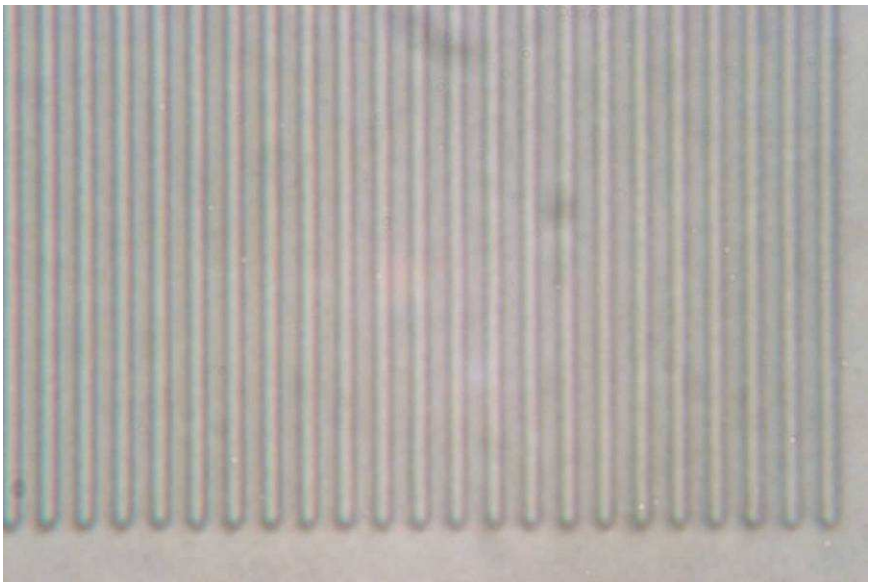


Figure 4.8. Optical microphotograph of SiC mesas. The pattern width is 0.85µm when measured under this microscope. The periodicity of the structure is 2.5µm.

4.2.4. Gate Implantation

Gate formation requires aluminum ion implantation into both the source mesa sidewall and the gate trench. Metal mask protects the regions that are not implanted. The samples were implanted with tilt angle of 23^{o} from the direction normal to the sample surface. The

implantation conditions are shown in Table 4.1. The implantation was done at four directions perpendicular to the sides of the samples. Each implantation at the specified conditions in Table 4.1 was repeated 4 times on each sample at the four different rotation angles and the same tilt angle.

Table 4.1. Energies and doses for HF-TIVJFET vertical sidewall implantation.

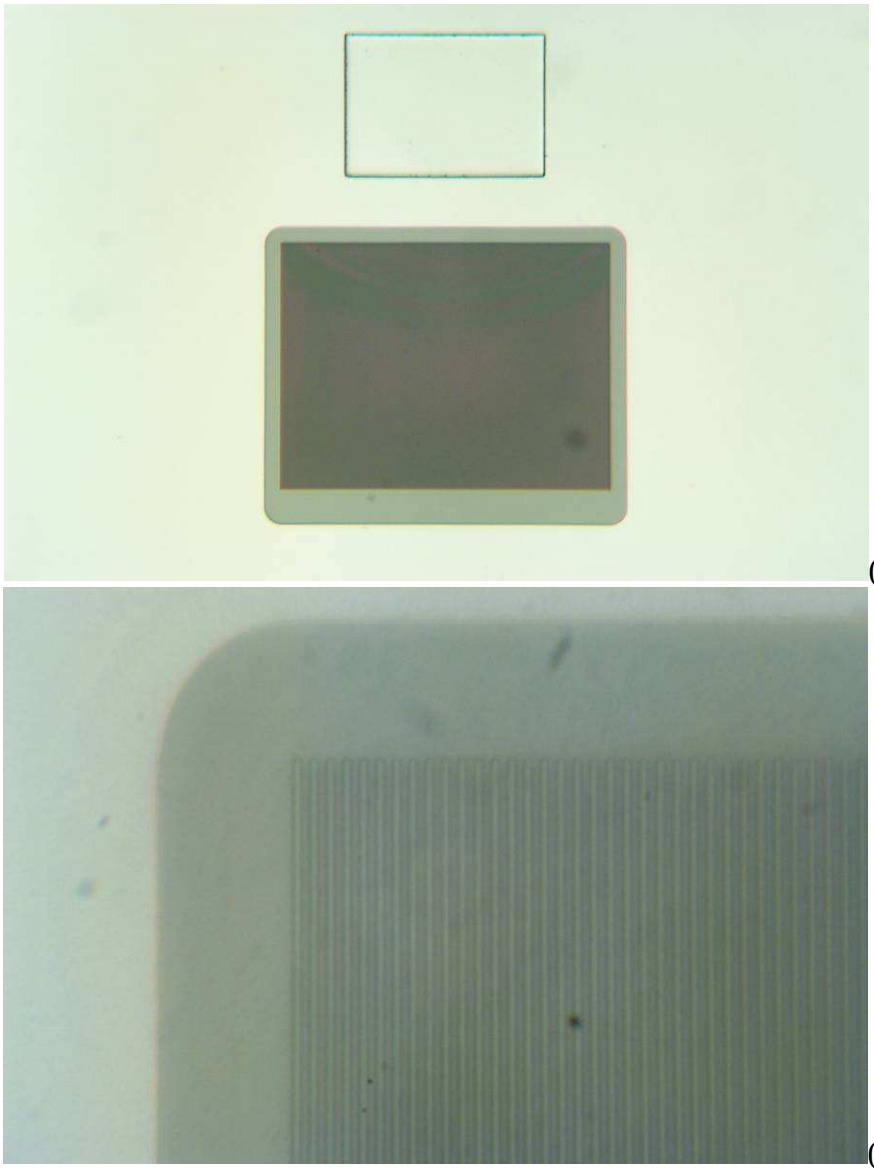
	Ion	**Energy (KeV)**	**Dose (cm^{-2})**
1	Al	225	1.84×10^{14}
2	Al	55	3.60×10^{13}

In addition to the vertical sidewall gate implantation, the design uses one more set of Al implantation at the bottom of the trenches: the p+ body implantation with very high concentration for the gate contacts (Table 4.2).

Table 4.2. Energies and doses for HF-TIVJFET gate ohmic contact implantation.

	Ion	**Energy (KeV)**	**Dose (cm^{-2})**
1	Al	90	6.20×10^{14}
2	Al	40	3.00×10^{14}

To avoid the process complications related to forming an implantation mask on top of the thin source mesas an improved technique was used. During the implantation for gate the source mesas were not covered with a mask. After the implantation the top of the source mesas will be inverted into p-type and has to be removed by planarization and dry etching process. Molybdenum implantation mask was patterned to define the gate outside boundary. Figure 4.9 shows the top view of a “medium” device type after the formation of Mo implant mask.



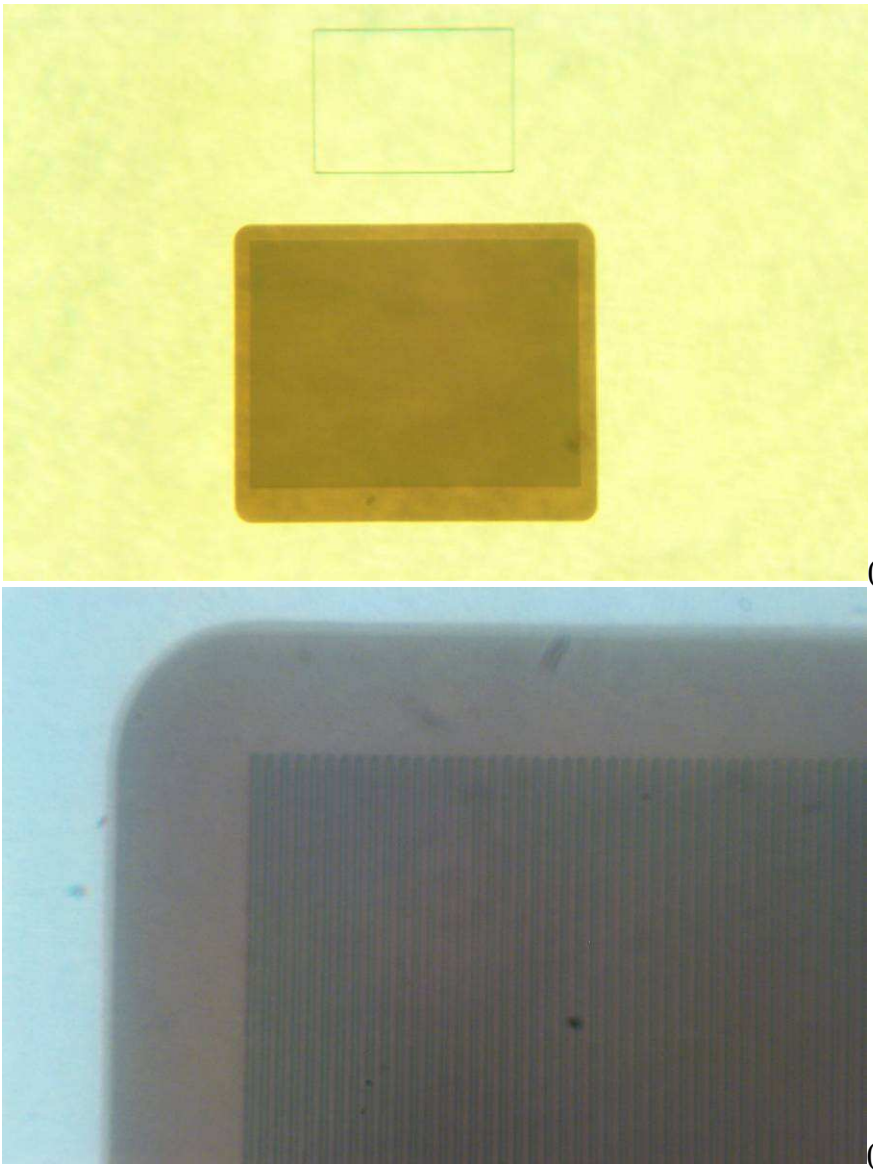
(a)

(b)

Figure 4.9. Optical microphotograph of Mo implantation mask for gate implantation: (a) complete device view, (b) one corner of a device, showing part of the source mesas and the JTE region.

Figure 4.10 shows an optical microphotograph (using back-side illumination) taken after gate implantation is completed. The implantation mask is removed. The implanted region structure has become amorphous, so it looks darker on the photos. After the implantation was done the samples were subjected to high-temperature annealing at 1550^{o}C for 30 minutes in argon to activate the implanted p-type dopants. Figure 4.11

shows an optical microphotograph (using front-side illumination) taken after post-implantation annealing at 1550^{o}C for 30 min in Argon. After annealing the implanted region has recovered original structure and looks identically to the non-implanted parts.



(a)

(b)

Figure 4.10. Optical microphotograph (using back-side illumination) taken after gate implantation was completed: (a) complete device view, (b) one corner of a device, showing part of the source mesas and the JTE region. The implantation mask was removed. The darker region is implanted.

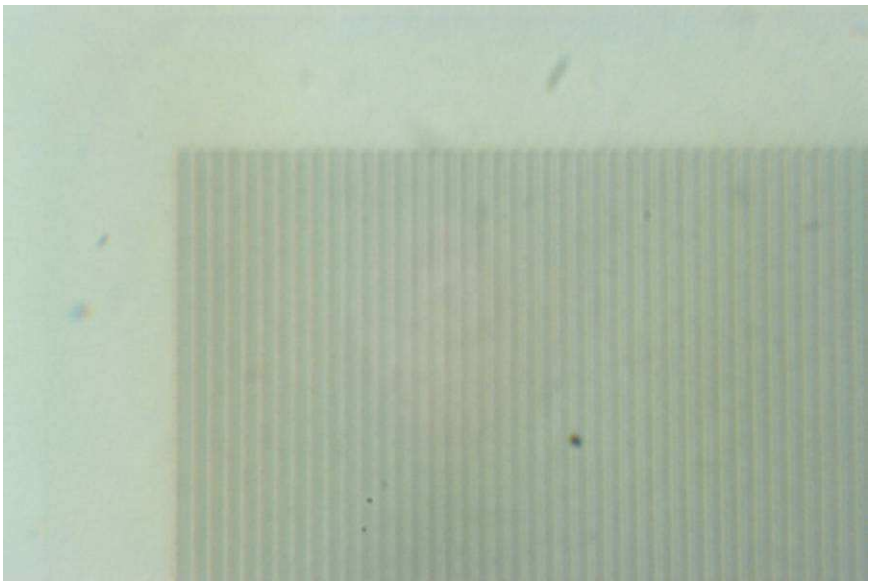


Figure 4.11. Optical microphotograph (using front-side illumination) taken after post-implantation annealing.

4.2.5. Removing of Al-implanted Source Mesa Top

During the aluminum implantation for gate the device source mesa tops were not covered with mask. Instead, another approach was chosen that makes the fabrication process relatively simpler. After the gate implantation the top of the source mesas had to be removed by dry etching.

First, a dry etching mask consisting of 6000Å AlTi metal alloy was deposited by sputtering. Then, a planarization procedure was performed, so that only the top of the source mesa lines would be exposed to the dry etching. This was done by deposition of photoresist (PR) and a following etch back by oxygen plasma. The photoresist was etched back in a barrel type etcher with O_2 plasma. After etch back only the source mesa tops were exposed from the photoresist. The metal covering the top of the source lines was then removed by wet etching in standard aluminum etchant. After that the remaining PR was removed by O_2 plasma. Finally, ICP etching was done to remove only the aluminum-implanted top of the mesa source lines, thus restoring the n+ type of the source mesa very

tops. The etched depth was 0.3μm. After the ICP etching was finished, the AlTi etching mask was removed by diluted HF. Figure 4.12 shows a HF-TIVJFET device source mesa lines, ready for the step of removing the implanted source mesa top. The AlTi layer over the source mesas is etched. The source lines look brighter on the photo with back-side illumination.

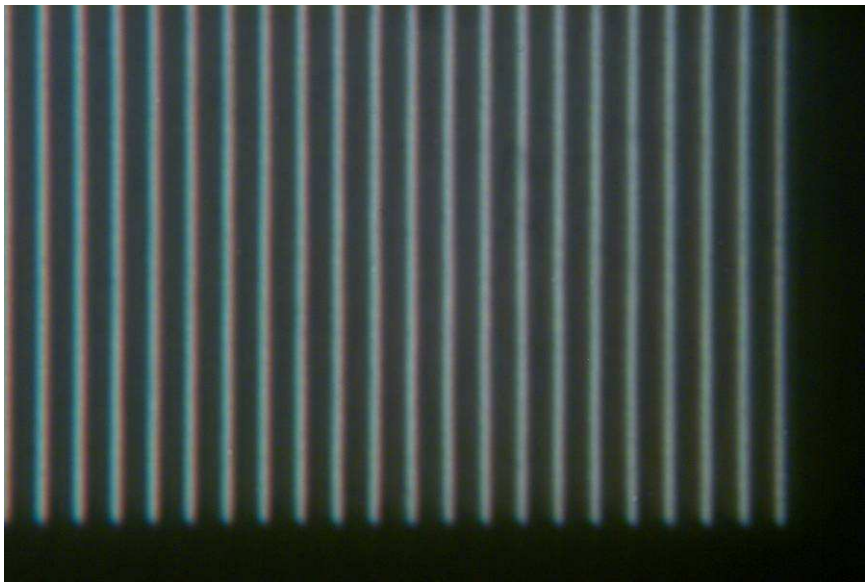


Figure 4.12. Optical microphotograph (using back-side illumination) showing HF-TIVJFET device source mesa lines, ready for the step of removing the implanted source mesa top. The AlTi layer over the source mesas is etched. The source lines look brighter on the photo.

4.2.6. Junction Termination Extension (JTE)

Two-step junction termination extension (JTE) was employed to reduce the electric field at the device periphery. This JTE is created by the aluminum implantation done to form the vertical gate. The JTE region needs to be thinned down by dry etching in order to achieve the charge balance that will give the desired field suppression at the device periphery. The optimum etching depths of the JTE steps need to be determined experimentally. For this purpose, a 4H-SiC dummy piece, in which all the implantations

and the post-implantation annealing have been performed together with the device samples, was prepared. The dummy piece was then processed to have simple p+n– diodes with two-step JTE with the step width of 5 µm. The outer step was etched to 400Å. The inner step depth was gradually increased by repeated ICP etching while the reverse I-V characteristics were monitored at every etching run. The results are shown in Figure 4.13.

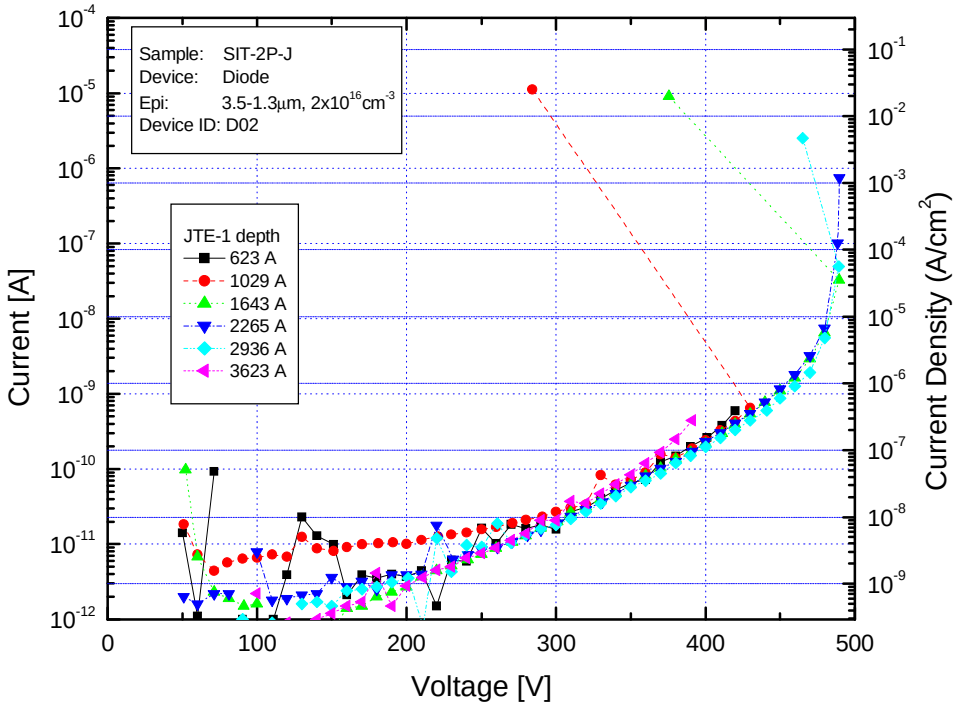


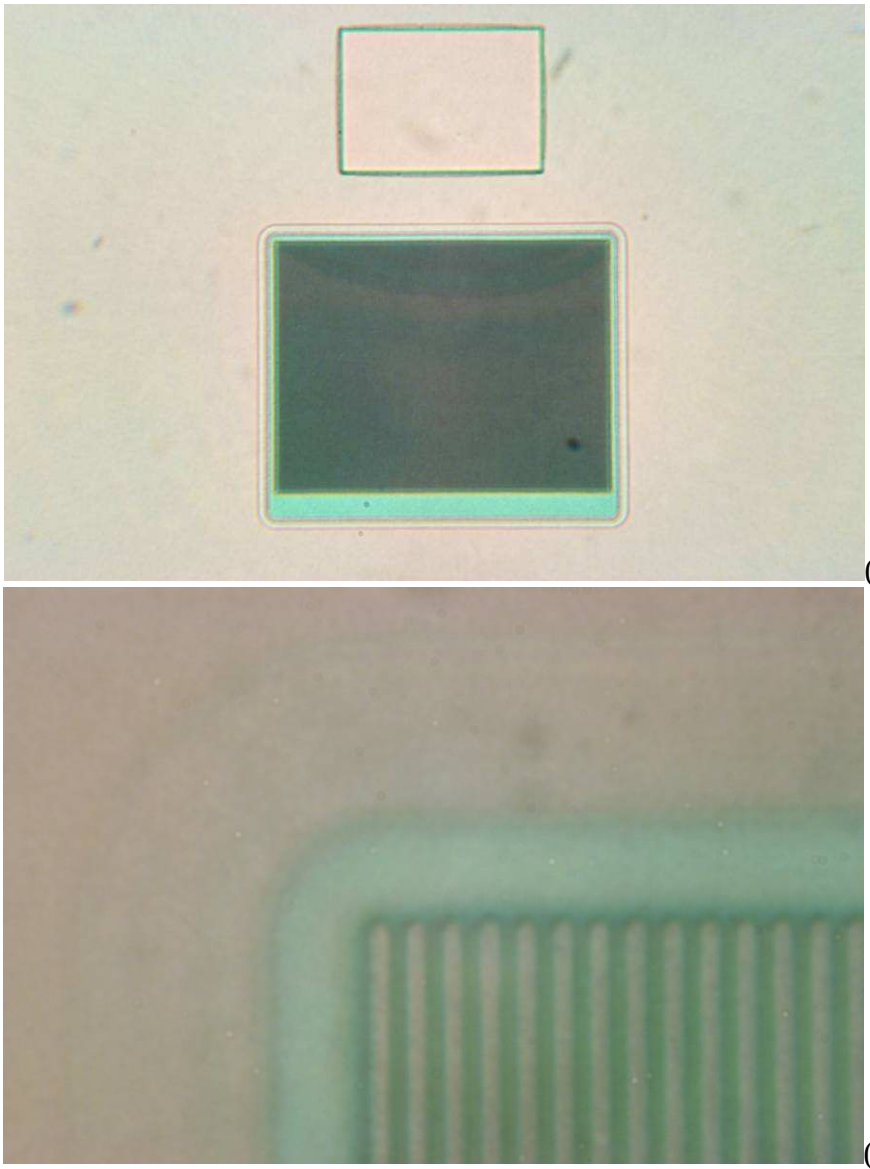
Figure 4.13. Reverse I-V characteristics of p+n– diode with two-step JTE measured at different stages of the JTE determination process.

It is clearly seen in the Figure 4.13 that show the breakdown voltage increases, reaches a maximum, and then decreases as the etching depth is increased. The maximum breakdown voltage corresponds to the optimum etching depth, which in this case is around 2200Å. For both of the JTE steps etchings were done with AlTi etching masks of 6000Å in thickness patterned by photolithography and standard Al etchant.

After the optimal etch depth was found the etching of the main samples was done using CF_4+O_2 plasma. The etched depth was 1900Å, which is slightly smaller than the optimum depth, due to correction for the SiC consumption during the following oxidation. After the etching the AlTi mask was removed by diluted hyrdofluoric acid.

4.2.7. Surface Passivation

Before oxidizing the samples to form the passivation needed, the wafers were cleaned using a thorough cleaning procedure. The cleaned samples were then thermally oxidized at 1100^{o}C for 30 min in wet oxygen ambient to form a sacrificial oxide. The sacrificial oxide was then removed by HF and another thermal oxidation was done at 1100^{o}C for 3 hours in wet oxygen ambient. The oxide was then annealed at 1100^{o}C for 1 hour in Ar. The oxide thickness is estimated to be about 600Å. The thermal oxide was then covered with a PECVD Si_3N_4 layer with thickness of 0.2μm. After that a layer of SiO_2 with thickness of 0.9um was deposited, covered by another Si_3N_4 layer with thickness of 0.25μm. Figure 4.14 shows the devices after the final stage of passivation.



(a)

(b)

Figure 4.14. Optical microphotograph of one HF-TIVJFET device after thermal SiO_2 and PECVD $Si_3N_4/SiO_2/Si_3N_4$ deposition (a) complete device view, (b) one corner of a device, showing part of the source mesas and the JTE region.

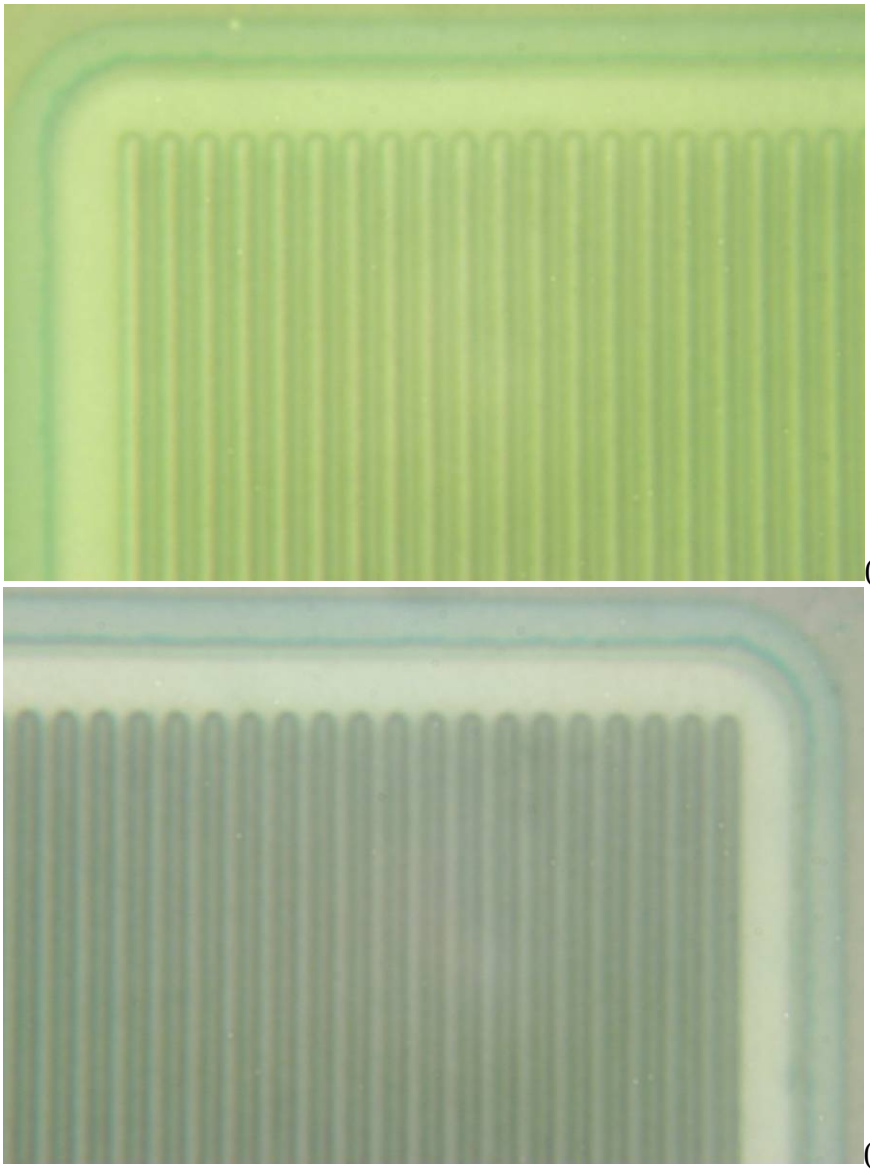
4.2.8. Gate Contact Formation

The fist step in the gate contact formation was to open windows in the passivation. Photolithography was done with mask "(7-2) G Contact", using thick-film photoresist. The passivation was etched by a combination of dry and wet etching steps. First, the top silicon nitride layer was removed by ICP etching, using CF_4 plasma. Second, the silicon

dioxide layer was etched by Buffered Oxide Etch (BHF). Third, the lower Si_3N_4 layer and the thermal SiO_2 were etched by ICP etching with using CF_4 plasma. And finally, the remaining thermal SiO_2 on the SiC surface was cleaned with buffered HF.

The gate contact metal, consisting of a Ti layer followed by a TiW layer with a total thickness of 2300Å was deposited by sputtering on the sample surface. The metal was patterned by a lift-off process in photoresist stripper. After the lift-off the remaining metal covered not only the gate region, but also the source mesas. To remove the metal from the source, wet etching process was used.

Self-aligned process was used to form the gate contact. The approach of photoresist planarization was used again. Photoresist was deposited on the sample surface in such a manner that would maximize the surface flatness. To do that, two photolithography steps were performed using a designated mask “Planarization Help” that made the surface level as flat as possible before the final PR coating. The photoresist was etched in a barrel type etcher with O_2 plasma. The source mesa lines were exposed to a depth, which is below the level of the gate-to-source p-n junction. After that the metal was etched from the source region surface by a wet etching process. Figure 4.15 illustrate the process of gate contact formation.



(a)

(b)

Figure 4.15. Optical microphotograph (using front-side illumination) of one corner of a HF-TIVJFET device after gate contact metal (Ti/TiW) deposition (a) before the metal over the source mesas was etched, (b) after the metal over the source mesas was etched.

4.2.9. Top-side and Bottom-side Drain Contact Formation

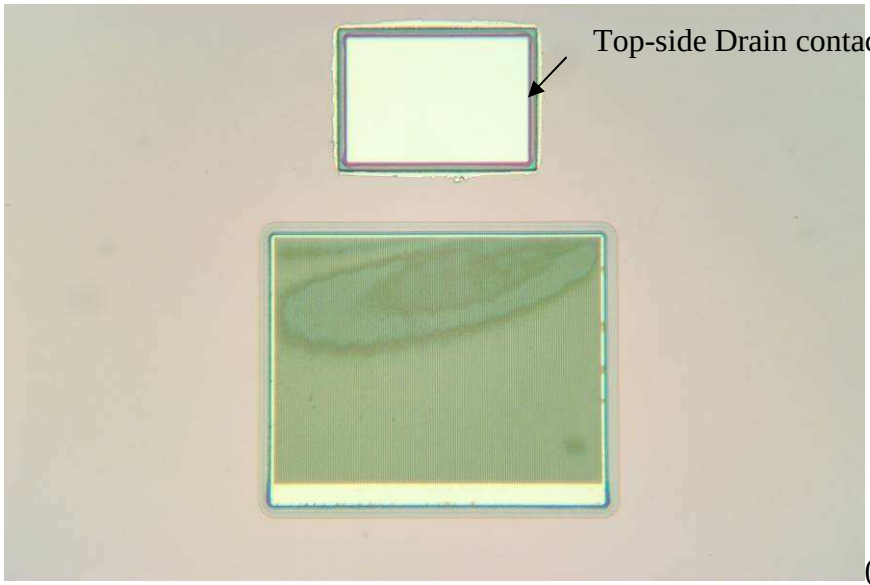
For the purpose of convenient on-chip testing a drain contact on the sample top surface was created in the device design. The contact to the top-side drain was created by a layer of Ni and another layer of TiW.

To pattern the top-side drain contact photolithography was done with mask “D Contact”, using thick-film photoresist. Windows in the passivation were opened by the same process as for the gate contact. The passivation was etched by a combination of dry and wet etching steps. The contact metal (Ni/TiW) was deposited by sputtering and patterned by lift off in photoresist stripper. The drain contact can be seen on Figure 4.16.

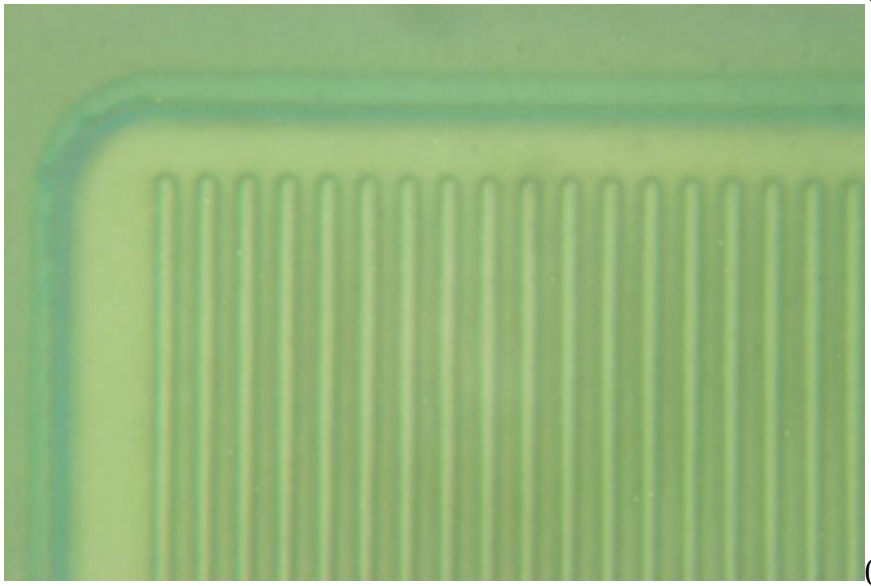
After that the passivation from the sample back side was removed by etching in buffered HF and AlTi/Ni with a total thickness of 3000Å was deposited by sputtering for a bottom-side drain contact.

4.2.10. Source Contact Formation

This step utilized the self-aligned lift-off process. First, the passivated surface was planarized by photoresist using the same conditions as in the previous planarization steps. Second, the planarized surface was etched back by a barrel type etcher with O_2 plasma. The etch-back was continued until all the mesa tops were confirmed to be exposed under an optical microscope. After the PR etch back the samples were briefly soaked in BHF to ensure the surface is clean of any oxide. Fourth, a Ni layer followed by a TiW were deposited by sputtering. During the sputtering deposition, the samples were placed so that the deposition occurred at the normal incidence in order to help ease the following lift-off. Sixth, the deposited Ni/TiW film lying in the gate trench was lifted off by dissolving the photoresist in the trenches in the photoresist stripper. Figure 4.16 show the device after source contact formation was completed.



(a)



(b)

Figure 4.16. Optical microphotograph of one HF-TIVJFET device after gate, top-side drain and source contacts have been deposited (a) complete device view, (b) one corner of a device, showing part of the source mesas and the JTE region. The top-side drain contact can also be seen on the figure.

4.2.11. Ohmic Contacts Annealing

After all the contact metal layers were deposited and patterned the samples were loaded in a high temperature furnace to anneal the metals in order to form ohmic contacts to the device drain, source and gate at the same time. The samples were annealed at 1050°C in an Ar-H_2 (5%) ambient to form the ohmic contacts.

4.2.12. Trench Filling Planarization and Metal Overlay Formation

This fabrication step consists of two phases – (a) deposition and planarization etch-back of trench-filling material and (b) deposition and patterning of metal overlay. For the trench-filling material, a planarizing polyimide (PI) was selected, because of its excellent ability to fill deep trenches without cracking, and because of the relative simplicity of the planarization etch-back process it uses. The planarizing polyimide was deposited in a regular photoresist spinner. The deposition was done in two identical steps and then a curing was performed at temperature > 350^{o}C.

Next, the gate-pad and drain-pad contact windows were defined in the polyimide coating. This was done by ICP etching with AlTi masks. AlTi (4000Å) mask layer was deposited by sputtering. The mask was then patterned with the photomask "(8) G-D Window Overlay" and wet chemical etching using aluminum etchant. The polyimide etching was not completed at this step and a certain thickness remained on the gate contact surface that is enough to be completely removed by the following etch-back process of the polyimide. Figure 4.17 shows a gate contact pad window opened in the PI.

After that, the polyimide planarizing etch-back step was done. AlTi mask was used to cover the regions around device active area, in order to keep the original polyimide thickness. AlTi mask layer was deposited by sputtering and then patterned by photolithography with photomask "(7-2) G Contact" and wet chemical etching. The oxygen plasma etch back was performed in a barrel-type plasma etcher. Several etch-back runs were repeated until all mesa tops were confirmed to be exposed.

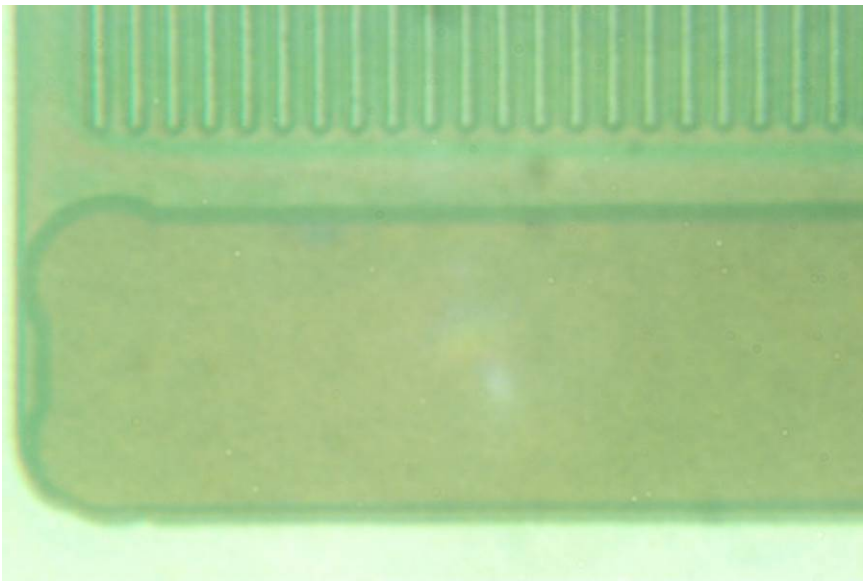


Figure 4.17. Optical microphotograph of a “Medium” type HF-TIVJFET device after gate/drain pad windows were opened in the polyimide layer and the planarizing polyimide etch-back was finished. The gate pad is shown together with a part of the source mesas.

Finally, the metal overlays for the source and gate pads were deposited on the etched-back surfaces and patterned by photomask “(9) G-S-D Metal Overlay”. The source pad is directly placed on the active area of each device to connect the source contacts exposed by the preceding etch-back process. The PI remaining in the gate trenches serves as an insulating layer between the gate and source contact layers. The overlay metal consists of three layers – Al/Ti/Au with a total thickness of 1.5μm. First, the aluminum layer was deposited by sputtering. Photolithography with mask “(9) G-S-D Metal Overlay” was done and the Al mask was wet etched with aluminum etchant. Next, Ti/Au metals were deposited by sputtering and patterned by photolithography with the same mask and a subsequent lift-off process in photoresist stripper. In addition, a layer of Ni/Au was deposited on the substrate side. Figures 4.18-4.19 show the optical microscope photographs of the fabricated devices.

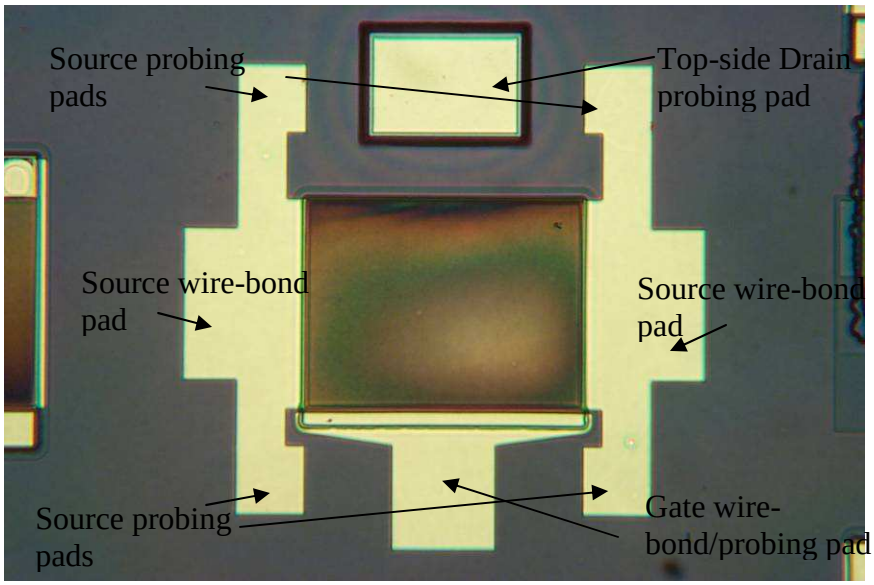


Figure 4.18. Optical microphotograph of a “Medium” type HF-TIVJFET device after the final metal overlay was done.

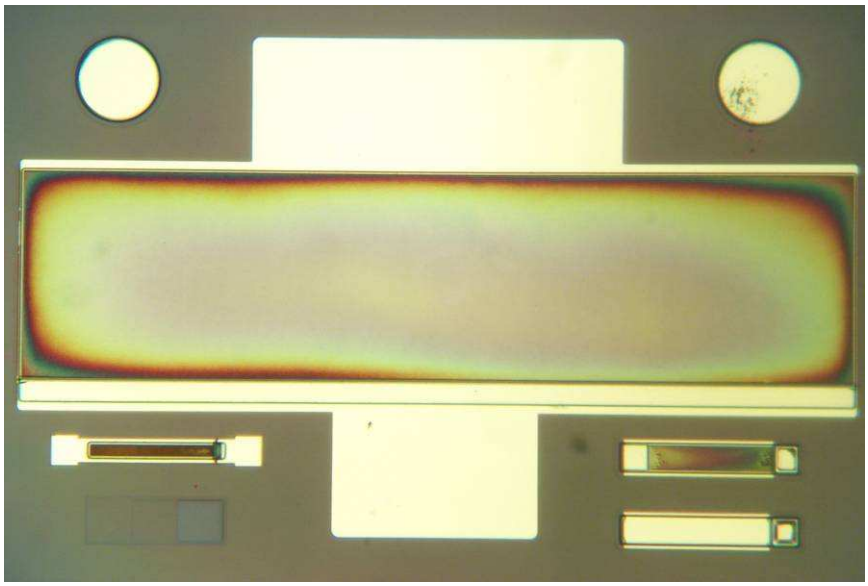


Figure 4.19. Optical microphotograph of a “Large” type HF-TIVJFET device together with test structures after the final metal overlay was done.

4.3. Characterization

4.3.1. Characterization under DC Conditions

4.3.1.1. Medium Type Devices

The on-state and off-state characteristics of fabricated HF-TIVJFET devices of type "Medium" were tested at room temperature under quasi-DC conditions with Tektronix 371A High Power Curve Tracer. For the 1.50μm source mesa design a very high current density of 479A/cm^2 is achieved for normally-off blocking voltage of 434V (I-V shown on Figure 4.20). This corresponds to a power density of 208kW/cm^2 in normally-off mode. The specific on-resistance at V_{DS}=0.5V and V_{GS}=5V is R_{SPON}=1.84mΩ.cm^2.

For the 1.75μm design with wider vertical conducting channel, even higher current density of 717A/cm^2 is achieved for normally-off blocking voltage of 329V (I-V shown on Figure 4.21). If a small negative voltage is applied to the gate the device can block 458V. This corresponds to a power density of 236kW/cm^2 in normally-off mode and 328kW/cm^2 in normally-on mode. The specific on-resistance at V_{DS}=0.5V and V_{GS}=5V is R_{SPON}=1.84mΩ.cm^2.

For the 2.00μm design the devices show lower blocking voltages at zero gate bias with higher current density, since the vertical channel width is further increased. For this design the highest current density achieved is 1370A/cm^2 (I-V shown on Figure 4.22). The specific on-resistance at V_{DS}=0.5V and V_{GS}=5V is R_{SPON}=1.42mΩ.cm^2. The blocking voltage at zero gate bias for this particular device is 65V, however it can support 420V with negative gate bias of 10V. This corresponds to a power density of 575kW/cm^2 in normally-on mode.

For the 2.25μm design the vertical channel width is further increased and the devices are clearly normally-on. For this design the highest current density of 2075A/cm^2 was achieved (I-V shown on Figure 4.23). The lowest specific on-resistance of R_{SPON}=1.24mΩ.cm^2 (at V_{DS}=0.5V and V_{GS}=5V) was achieved for this design. The blocking voltage with a gate bias of –25V is 262V, which is lower than the structure ultimate blocking capability. Apparently the channel is too wide in this case, so a reasonable reverse gate bias is not enough to fully close the vertical channel. The power density obtained for this structure is 544kW/cm^2 in normally-on mode.

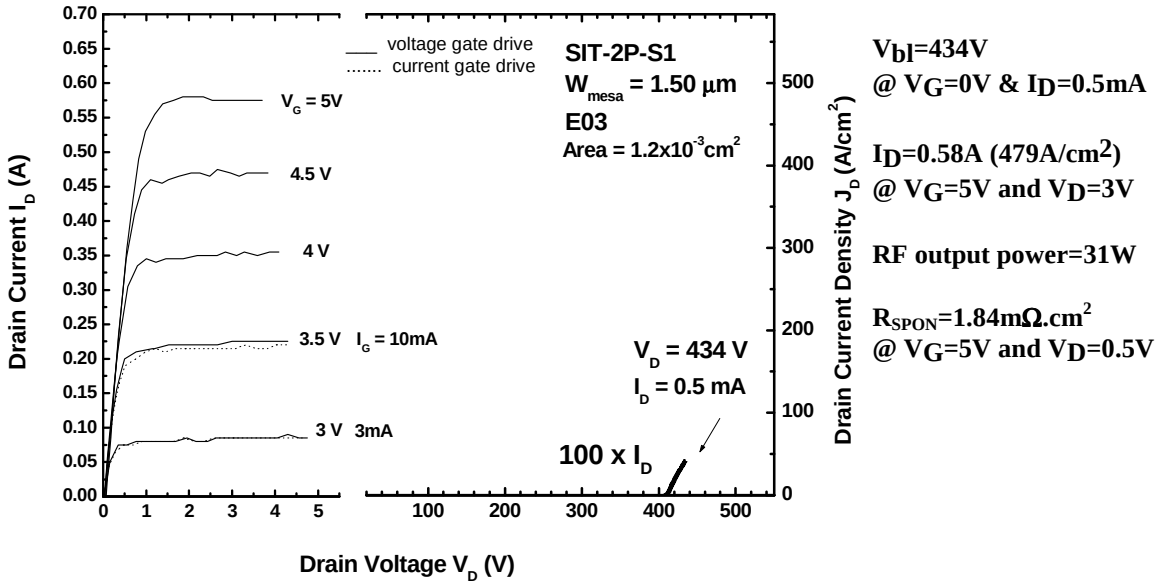


Figure 4.20. I-V curves of HF-TIVJFET with source mesa width of 1.50μm by mask design, showing 479A/cm2 current density and a blocking voltage (normally-off) of 434V.

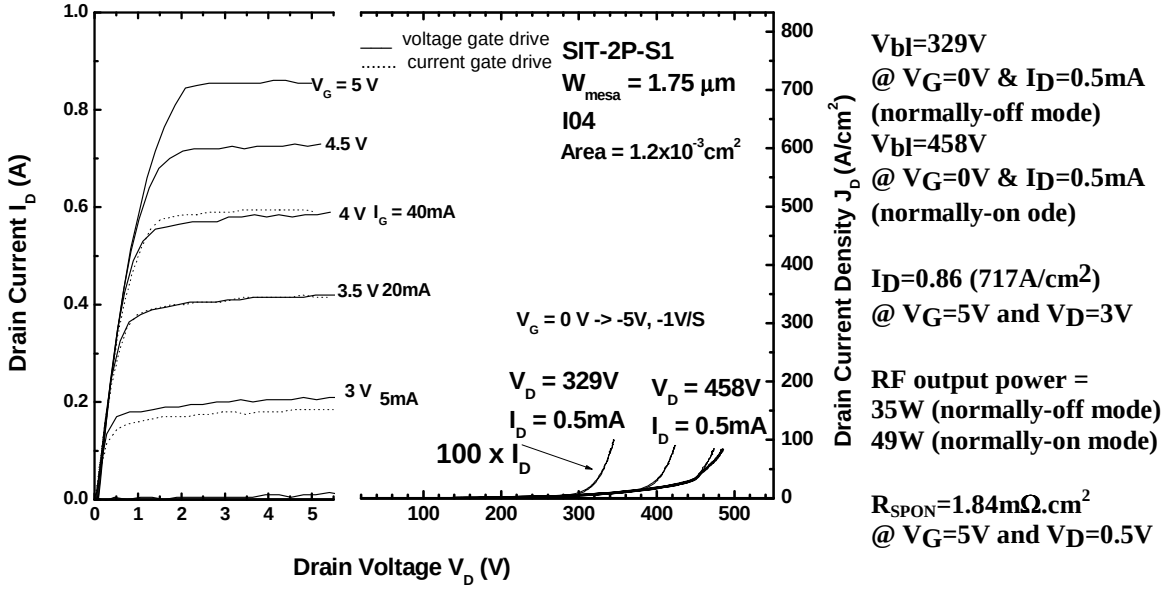


Figure 4.21. I-V curves of HF-TIVJFET with source mesa width of 1.75µm by mask design, showing 717A/cm2 current density and a blocking voltage (normally-off) of 329V and 458V in normally-on mode.

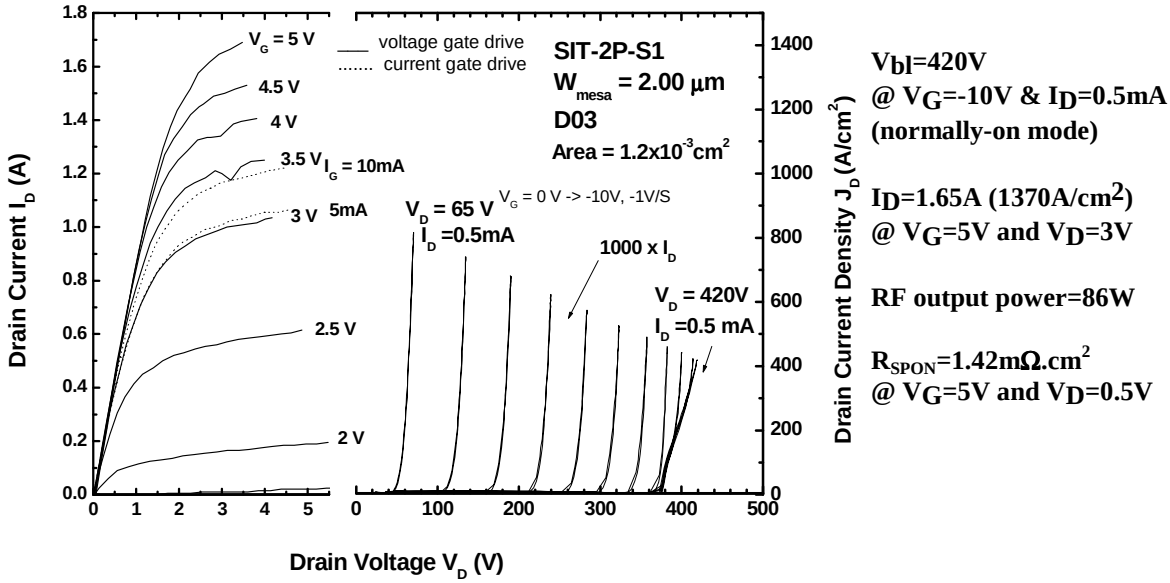


Figure 4.22. I-V curves of HF-TIVJFET with source mesa width of 2.00µm by mask design, showing 1370A/cm2 current density and a blocking voltage (normally-on) of 420V.

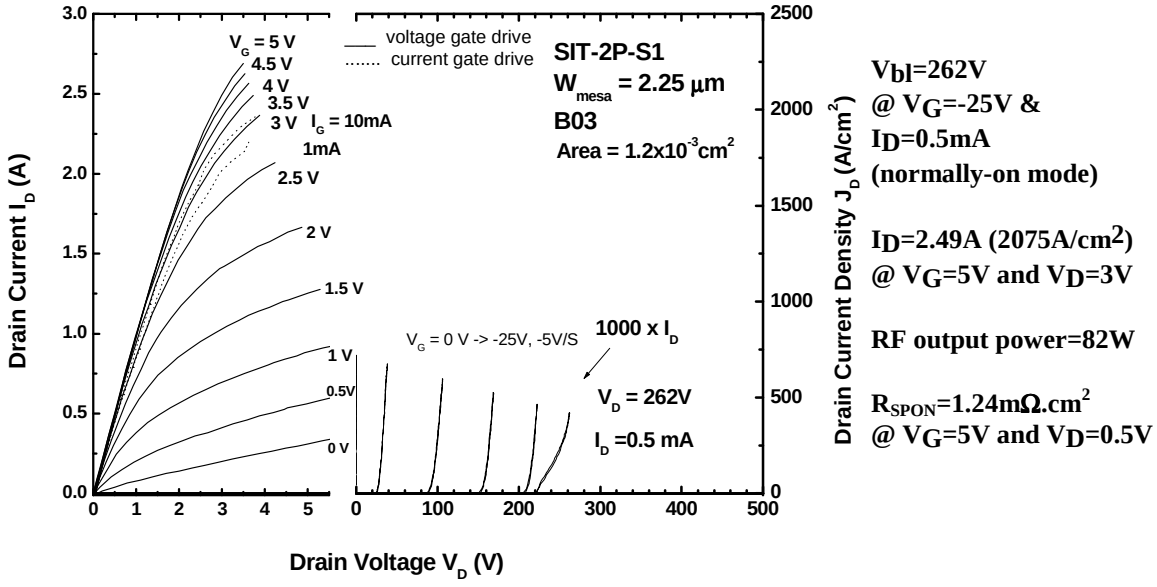


Figure 4.23. I-V curves of HF-TIVJFET with source mesa width of 2.25μm by mask design, showing 2075A/cm^2 current density and a blocking voltage (normally-on) of 262V.

4.3.1.2. Large Type Devices

Large size HF-TIVJFET with 1.50μm mesa design was tested. Figure 4.24 shows I-V curves for a large size HF-TIVJFET. It is seen that 3.3A-397V normally-off capability was achieved for a single die, corresponding to a high power of 1310 W/die. This corresponds to a class B operation RF power of 164W for a single die. The specific on-resistance at V_{DS}=0.5V and V_{GS}=5V is R_{SPON}=2.44mΩ.cm^2.

Devices with large size and wider vertical channel width were also tested. Figure 4.25 shows the I-V curves for a large HF-TIVJFET with 1.75μm mesa design. The device conducts a current of 6A at V_F=2V and blocks a voltage in normally-off mode of 176V. If tested in normally-on mode it can block a voltage of 346V (negative voltage at the gate). The maximum RF power achieved was 155W in normally-off mode and 305W in normally-on mode. The specific on-resistance at V_{DS}=0.5V and V_{GS}=5V is R_{SPON}=2.07mΩ.cm^2.

Figure 4.26 shows the I-V curves for a large HF-TIVJFET with 2.00μm mesa design. The device should conduct a current much larger than 6A at V_F=1V and blocks a voltage (normally-on) of 145V. Current is not tested above 6A to prevent burning of the device during testing without proper packaging (probes testing). The estimated forward current capability at 2V is 10A. The specific on-resistance at V_{DS}=0.5V and V_{GS}=5V is R_{SPON}=1.48mΩ.cm^2.

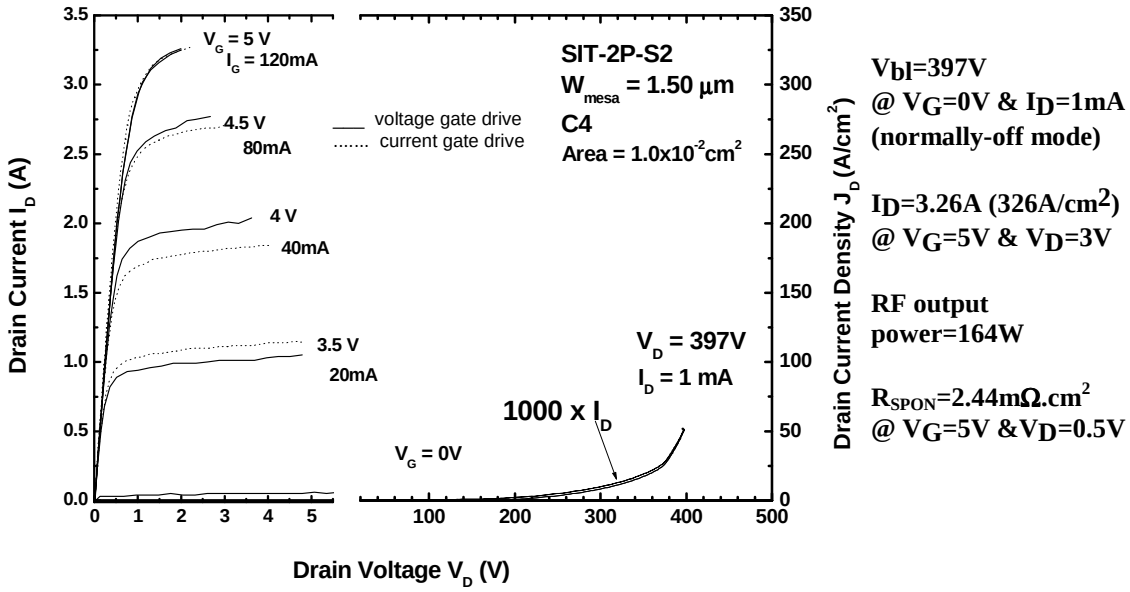


Figure 4.24. I-V curves for a large size HF-TIVJFET with 1.50μm source mesa width. It is seen that 3.3A-397V normally-off capability has been achieved for a single die, corresponding to a high power of 1310W/die.

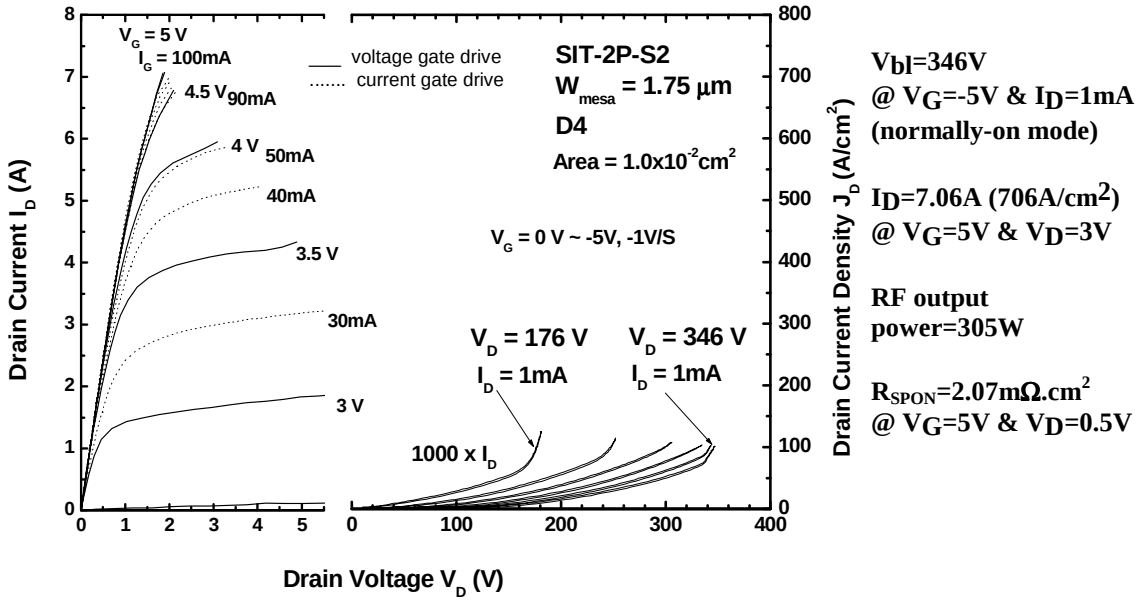


Figure 4.25. I-V curves for a large size HF-TIVJFET with 1.75µm source mesa width. The device conducts a current of 7A at forward voltage V_F=2V and blocks a voltage (normally-off) of 176V. If a negative voltage is applied to the gate (as for a device in normally-on mode) the blocking is 346V.

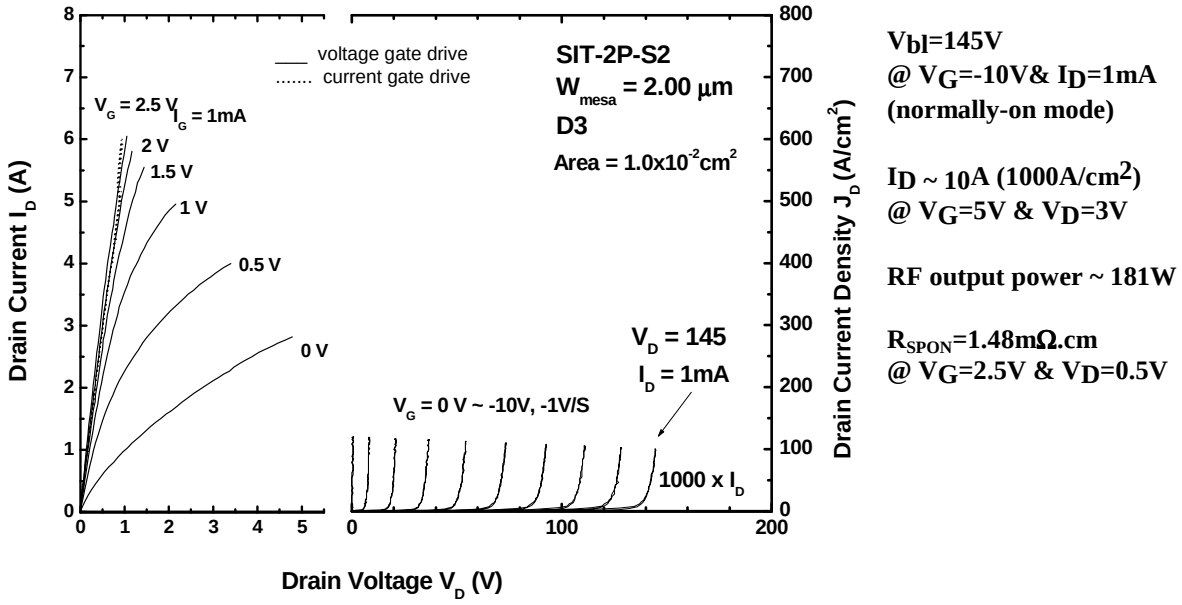


Figure 4.26. I-V curves for a large size HF-TIVJFET with 2.00µm source mesa width. The device should conduct a current much larger than 6A at V_F=1V with proper packaging and blocks a voltage (normally-on) of 145V. (Current is not tested above 6A to prevent burning of the device during testing without proper packaging.)

4.3.2. RF Small Signal Characterization of Fabricated HF-TIVJFETs

The microwave characteristics of fabricated VJFET devices of type “Medium” were tested at room temperature with HP 8722ES Network Analyzer. Small signal RF measurements were done on wafer level using microwave probes. The S-parameters were tested and converted to H-parameters and the cut-off frequency was extracted. The results are shown on Figure 4.27-4.29.

Figure 4.27 shows the S-parameters magnitude vs. frequency for a medium size HF-TIVJFET mesa design of 1.75um. Figure 4.28 shows the S-parameters phase vs. frequency for a medium size HF-TIVJFET mesa design of 1.75μm. Figure 4.29 shows short circuit current gain vs. frequency for a medium size HF-TIVJFET with source mesa design of 1.75μm. The device was tested with drain voltages up to 100V, which is limited by the testing setup. Linear extrapolation shows a cut-off frequency of approximately f_T=800MHz. Figure 4.30 shows RF test results of short circuit current gain vs. frequency for another medium size HF-TIVJFET with source mesa design of 1.75μm. Linear extrapolation shows a cut-off frequency f_T=900MHz, which is near the theoretically predicted maximum frequency of ~1-2GHz for the normally-off design.

Figure 4.31 shows the S-parameters magnitude vs. frequency for a medium size HF-TIVJFET mesa design of 2.00um. Figure 4.32 shows the S-parameters phase vs. frequency for a medium size HF-TIVJFET mesa design of 2.00μm. Figure 4.33 shows short circuit current gain vs. frequency for a medium size HF-TIVJFET with source mesa design of 2.00μm. Linear extrapolation shows a cut-off frequency f_T=1.5GHz.

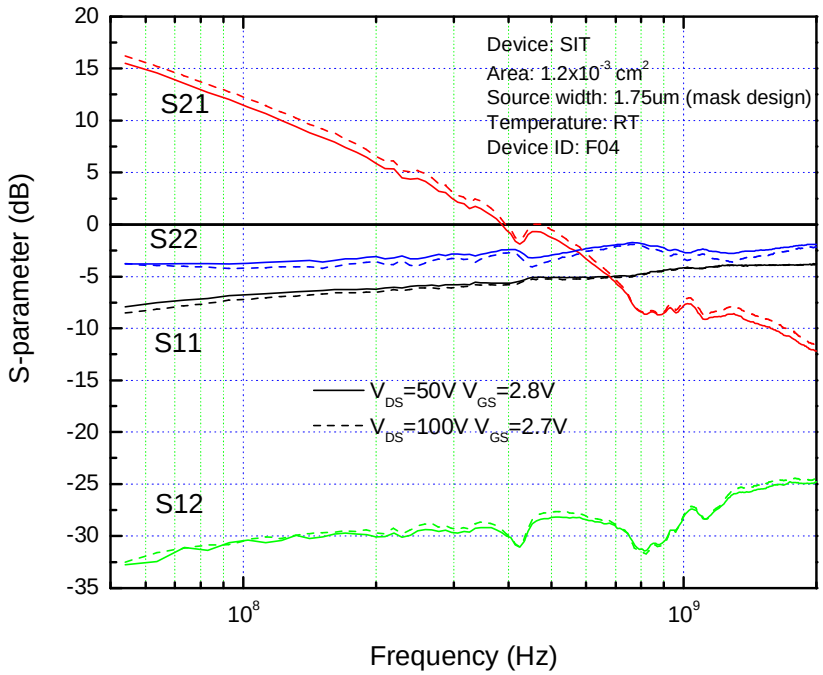


Figure 4.27 RF test results: S-parameters magnitude vs. frequency for a medium size HF-TIVJFET mesa design of 1.75µm.

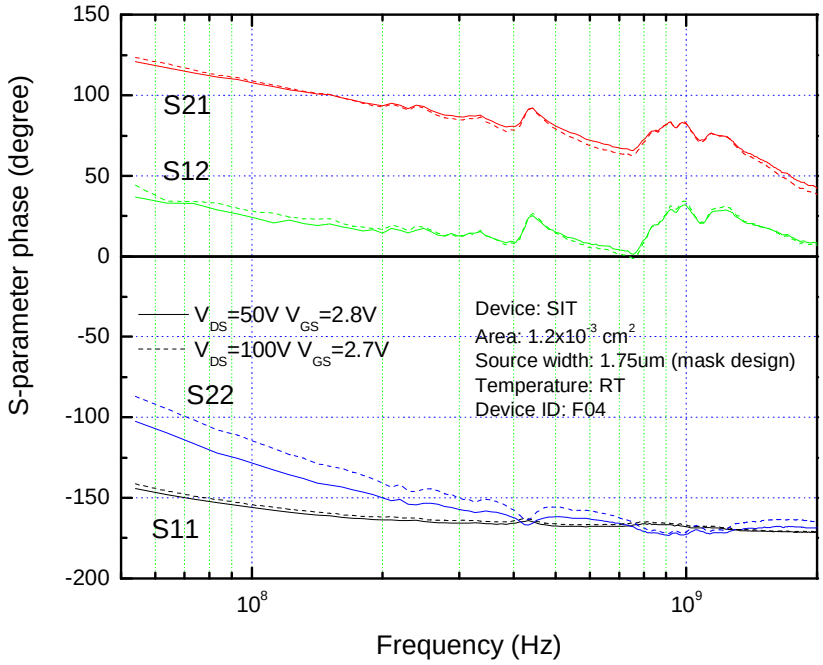


Figure 4.28. RF test results: S-parameters phase vs. frequency for a medium size HF-TIVJFET mesa design of 1.75µm.

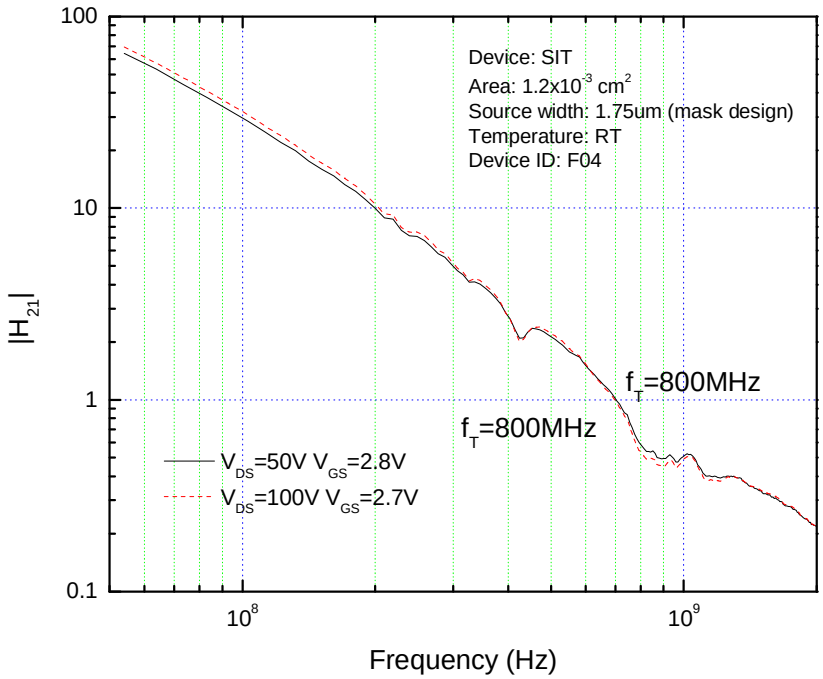


Figure 4.29. RF test results of short circuit current gain vs. frequency for a medium size HF-TIVJFET with source mesa design of 1.75µm. Linear extrapolation shows a cut-off frequency f_T=800MHz.

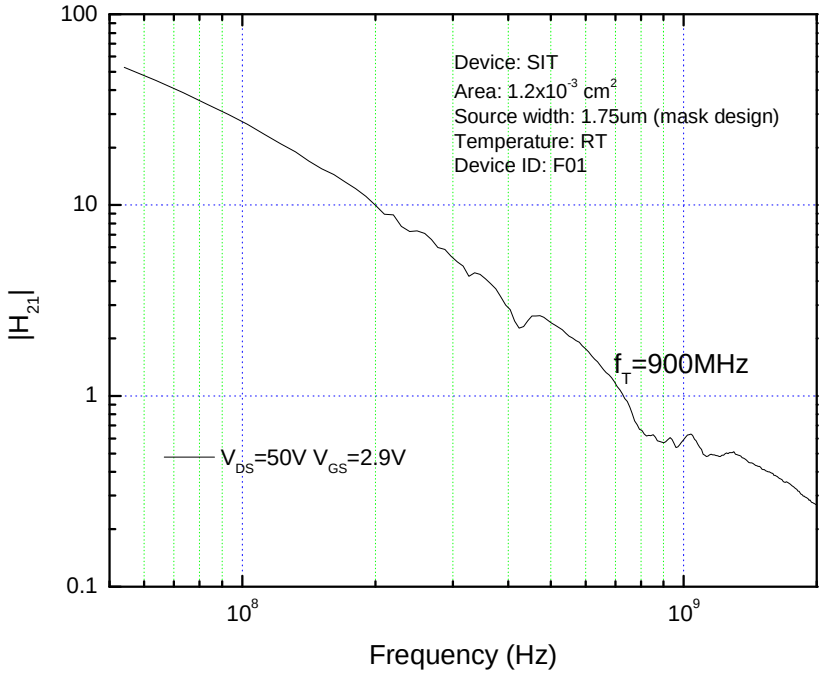


Figure 4.30. RF test results of short circuit current gain vs. frequency for another medium size HF-TIVJFET with source mesa design of 1.75µm. Linear extrapolation shows a cut-off frequency f_T=900MHz.

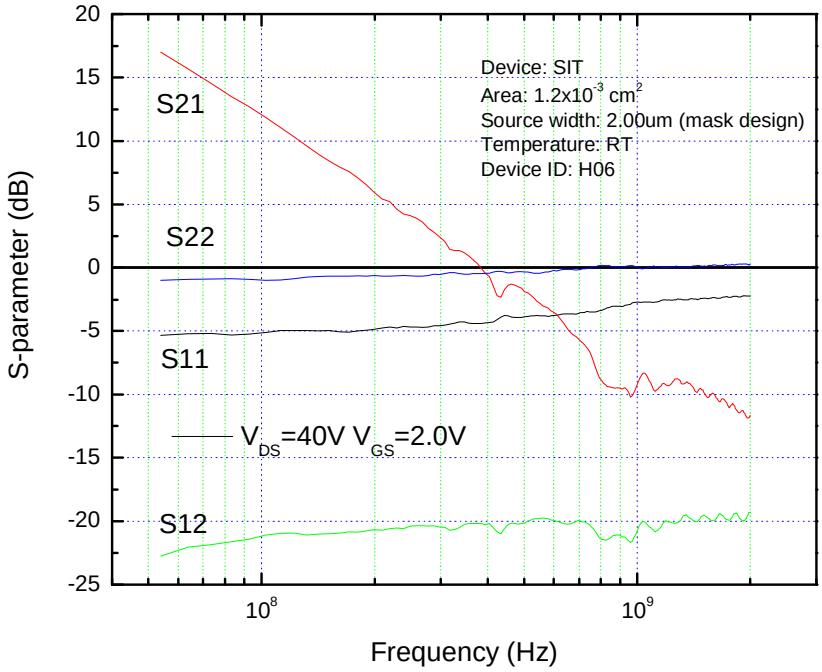


Figure 4.31. RF test results: S-parameters magnitude vs. frequency for a medium size HF-TIVJFET mesa design of 2.00µm (normally-on).

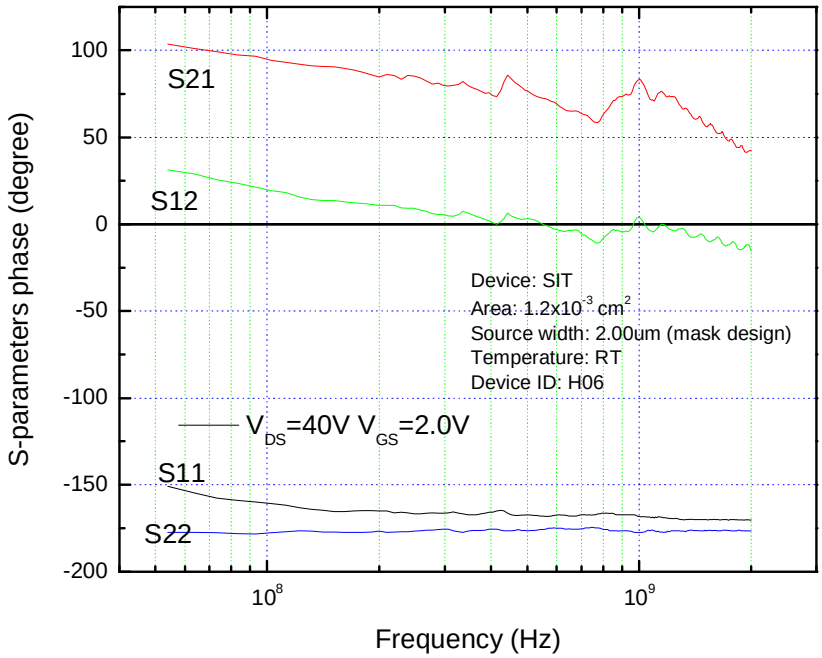


Figure 4.32. RF test results: S-parameters phase vs. frequency for a medium size HF-TIVJFET mesa design of 2.00µm (normally-on).

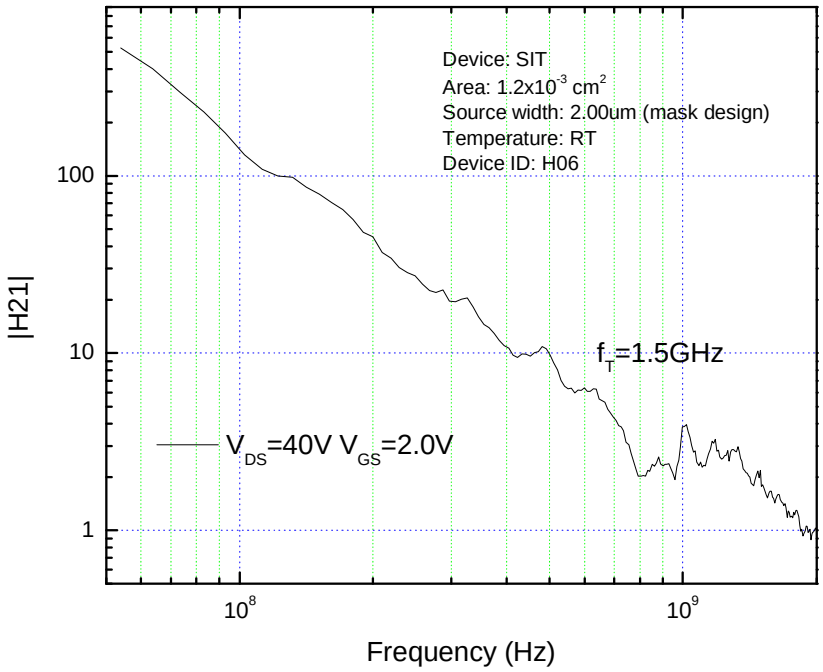


Figure 4.33. RF test results of short circuit current gain vs. frequency for a medium size HF-TIVJFET with source mesa design of 2.00μm. Linear extrapolation shows a cut-off frequency f_T=1.5GHz.

CHAPTER 5. NORMALLY-ON TIVJFET WITH A BLOCKING VOLTAGE OF 1200V

5.1. Device and Process design

5.1.1. Unit Cell Design

The cross sectional view of the normally-on unit cell of the TIVJFET device is shown in Figure. 5.1. This structure is designed to be able to block over 1200V at a temperature range from RT to 300°C when the gate voltage is -30V. The device pitch size was minimized to get the maximum current density. The design is based on the use of a self-aligned process to form gate and source contacts. The vertical channel opening was designed to be W_{VC}=2.1μm.

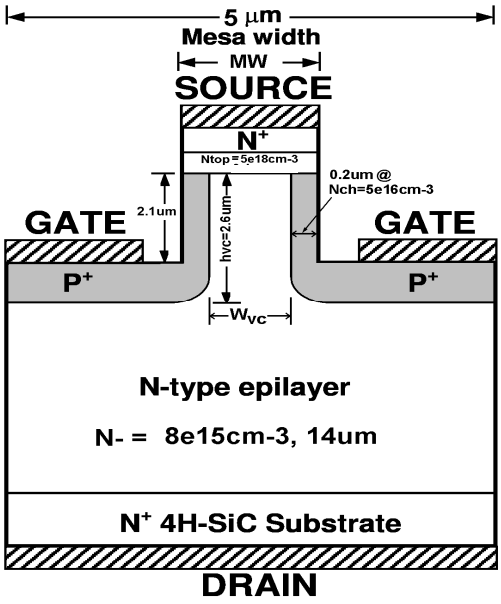


Figure 5.1. Unit Cell Structure of normally-on 4H-SiC TIVJFET.

A single n- epilayer with a thickness of 14μm and doping concentration of $8\times10^{15}cm^{-3}$ was used to form the vertical channel and to support the voltage. The n+ source layer at the top of the structure has two parts – an upper highly doped ($>1\times10^{19}cm^{-3}$) epilayer and a lower more moderately doped n+ epilayer.

5.1.2. Floating Guard Ring Termination Design

The three-zone JTE structure proved to be very successful in the fabrication of both the high-voltage normally-on TIVJFET and the low-voltage HF-TIVJFET. The main disadvantage of the JTE technique was its more complicated practical realization, as it requires three additional photolithography and etching steps. In order to substantially simplify the fabrication process guard ring termination was designed for the normally-on TIVJFET structure. The guard rings are implanted together with the gate and no additional processing is required. The guard ring structure is shown on Figure 5.2. The guard rings are formed in the same manner and at the same time with the device JFET gate. The design uses 28 rings with non-uniform spacing. The spacing between the individual guard rings is defined by the etched mesa width and the implanted sidewall depth, exactly like the device vertical channel. The spacing increases from the main junction toward the device periphery. Numerical modeling shows that this termination structure can achieve more than 90% of the parallel plane breakdown voltage. By shifting the guard ring spacing proportionally (same amount for all spacings) the structure can serve for a range of drift epilayer doping. The whole guard ring structure is self aligned and requires no additional processing step, as it is formed together with the source and gate formation. The guard ring spacing is the critical parameter. It can be controlled very well by adjusting the implanted sidewall depth and can be made very small. No mask is used during the implantation, thus avoiding any concerns related to difficulties defining narrow and tall implantation mask lines.

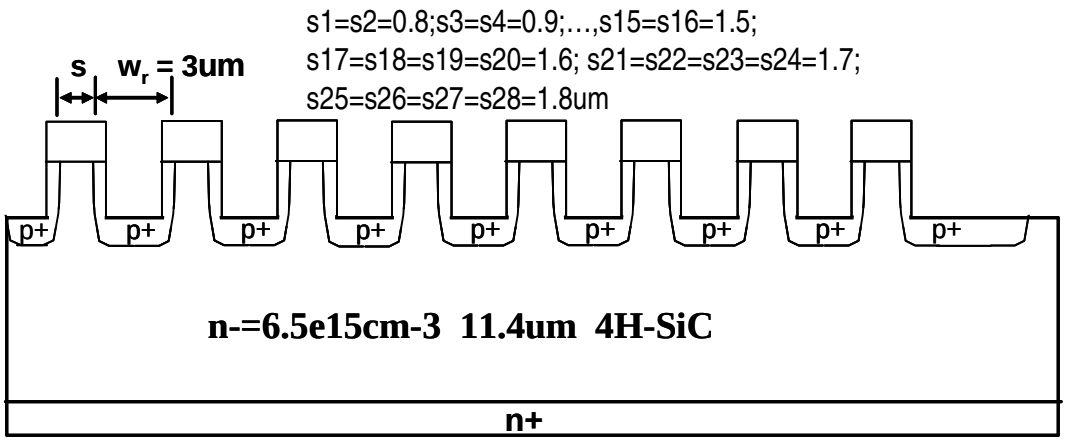


Figure 5.2. Floating guard ring structure, using etched mesas similar to the source mesas

5.1.3. Device Layout and Photomask Design

The complete device layout design is shown on Figure 5.3. The active area contains a number of source lines surrounded by a gate region. A gate contact pad was designed with dimensions large enough to ensure probing and wire bonding capability. The device active area is surrounded by a guard ring termination area that is used to suppress the high electric filed at device periphery. Devices with two different sizes were designed. Test p-n diodes and TLM structures were also included in the design to evaluate the effectiveness of the termination and the quality of the ohmic contacts. A set of photomasks was designed and fabricated. Only six masks are used throughout the fabrication. The set contains the following maks.

(1) Source Mesa;

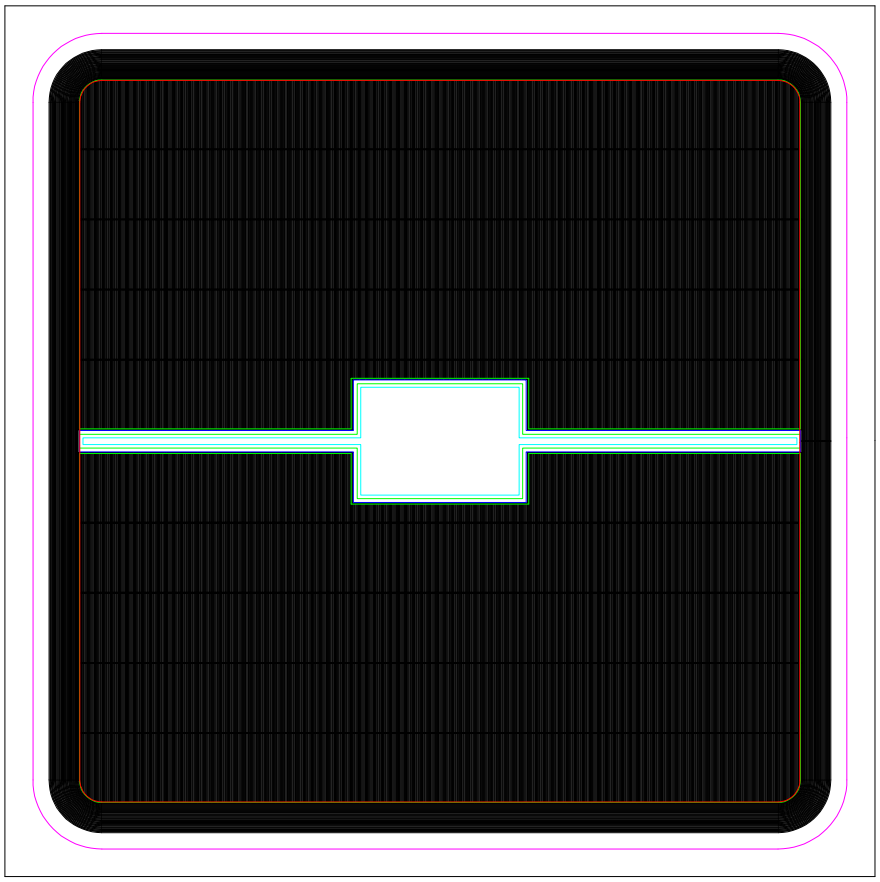
(2) Implantation;

(3) Gate Contact;

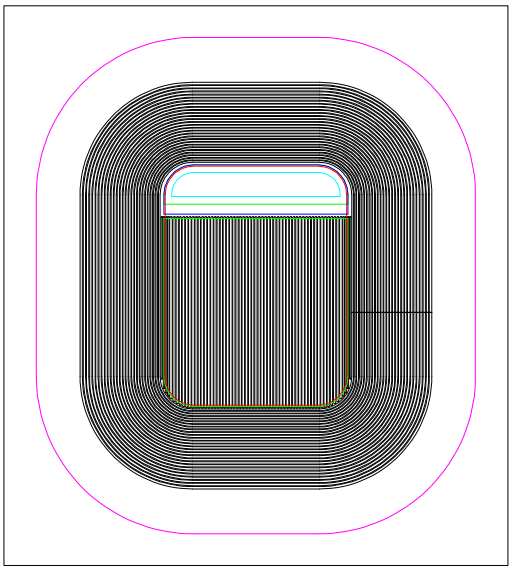
(4) Windows;

(5) Metal Overlay;

(6) Planarization Help.



(a)



(b)

Figure 5.3. A 1200V normally-on TIVJFET device layout: (a) Large type (active area 3x3mm); (b) Small type (active area 300x300μm).

5.1.4. Process Design

5.1.4.1. Process Improvement

For increased device performance and decreased processing complexity and a new device design and improved processing technology were implemented. The design uses a floating guard rings termination to simplify the fabrication. The number of photomasks used throughout the fabrication was reduced to six. A number of improvements to the processing technology were introduced to improve device performance and increase processing reliability.

Source mesa etching: First, the source mesa etching conditions were improved to achieve a highly vertical sidewall profile. To establish a god control of the vertical channel width the fabrication process has to ensure line-width uniformity, good vertical mesa profile and smooth mesa sidewall. To achieve a highly vertical source mesa profile an ICP etching conditions based on Bosch process (with alternative polymer deposition by C_4F_8 and dry etching by CF_4+O_2) were used.

Elimination of a separate junction termination formation step: The previously used junction termination extension design required an additional fabrication step to adjust the JTE layer thickness. With this design this step was completely eliminates, as the guard ring termination is completely defined during the source mesa formation and gate implantation.

Self-aligned nickel silicide gate and source contacts: Second, a new contact formation approach was implemented that allows self-aligned source metal definition without using a lift-off step. The idea utilizes the fact that metals, such as nickel (Ni), react with SiC when heated to form silicides, but will not react with SiO_2. Metal is

deposited above the source (free of oxide) and the gate trench (covered with oxide). The contact metal (Ni) is annealed at relatively low temperature to form nickel silicide on the source and the gate. After that annealed metal is wet etched to remove the unreacted metal, so only the top of the source mesas and the gate trenches are covered with silicide. Finally, a high temperature annealing is done to create ohmic contacts by further reaction of the remaining silicide with the SiC surface.

Thick gate metal overlay formation: In order to increase device current density and switching performance, and utilize fully the total device active area the gate metal resistance needs to be decreased. This can be done by increasing the gate metal thickness and using metals with lower resistivity. In this batch in addition to the metal used to form the ohmic contact to the gate, a gate metal overlay is used that increased the total metal thickness.

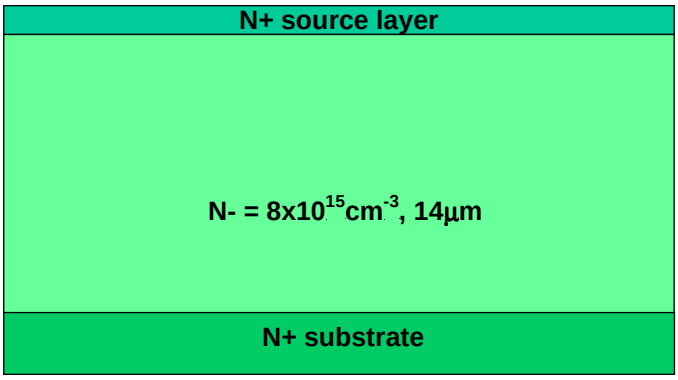
Silicon dioxide trench fill: In order to improve the device high-temperature capabilities, a trench-fill material based on silicon dioxide was chosen. The dielectric is deposited by PECVD and then etched back using CF_4 plasma to expose the source contact.

5.1.4.2. Fabrication Sequence

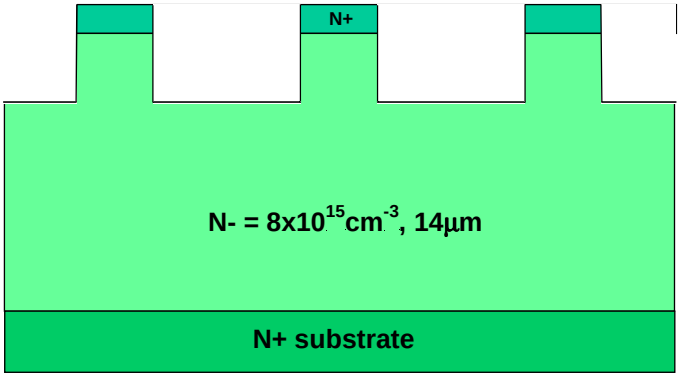
The major fabrication steps are as follows (Figure 5.4):

- Source mesa formation (Figure 5.4(b)).
- Gate formation by p^+ implantation and dopant activation annealing (Figure 5.4(c)).
- Removing of Al-implanted source mesa top (Figure 5.4(d)).
- Surface passivation by SiO_2 and Si_3N_4 (Figure 5.4(e)).

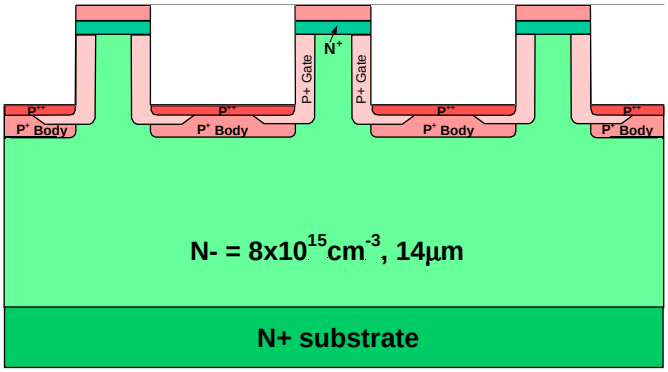
- Gate, source and drain contact formation (Figure 5.4(f)).
- Gate metal overlay formation (Figure 5.4(g)).
- Trench filling planarization and source metal overlay formation (Figure 5.4(h)).



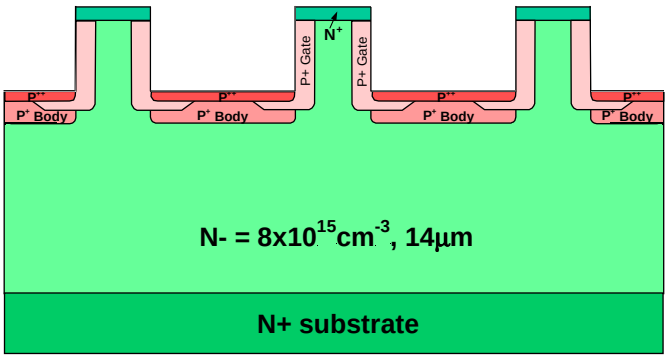
(a) Starting wafer;



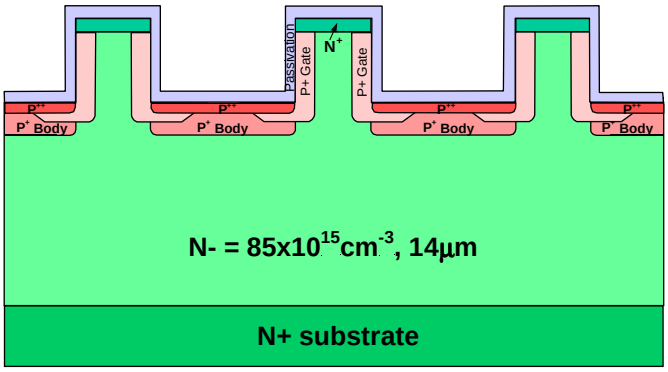
(b) Source mesa formation;



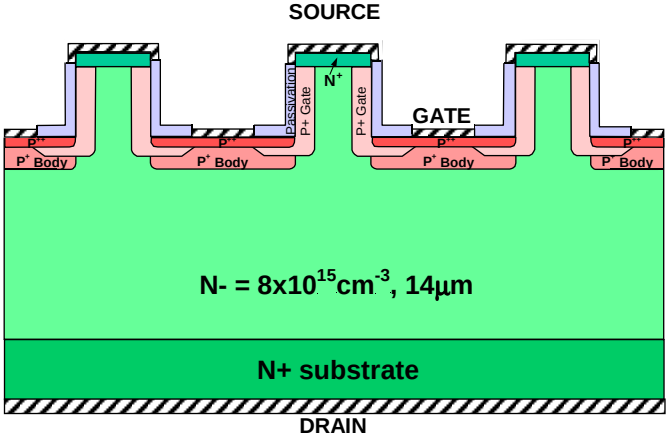
(c) Gate formation by p^+ implantation and dopants activation annealing;



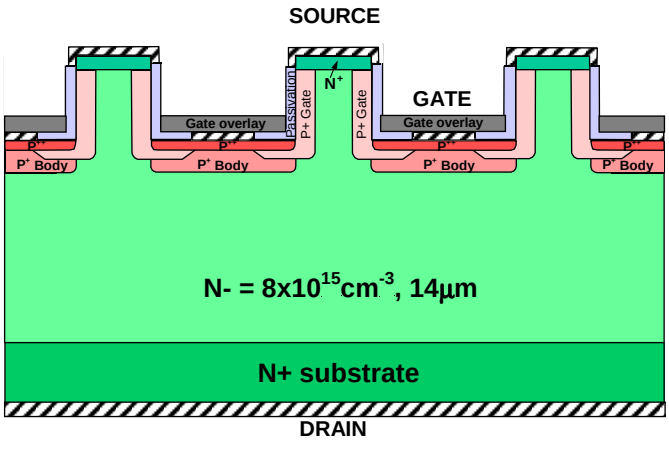
(d) Removing of Al-implanted source mesa top;



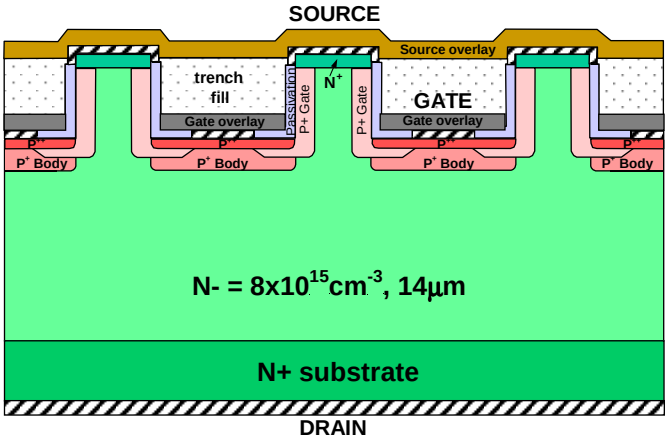
(e) Surface passivation by SiO_2 and Si_3N_4;



(f) Gate, source and drain contact formation



(g) Gate metal overlay formation



(h) Trench filling planarization and source metal overlay formation

Figure 5.4. Fabrication steps of normally-on TIVJFET structure.

5.2. Fabrication

5.2.1. Source Mesa Formation

The first step of the fabrication is the mesa-etching process to create mesas in the 4H-SiC epitaxial wafer pieces. The etching is done with an ICP etching system. The etching masks are made of AlTi film, which is patterned by standard photolithography with wet chemical etching. The 4H-SiC wafer pieces were first deposited with 3000-Å thick AlTi by sputtering. Second, the deposited AlTi films were patterned by the photomask “(1)

Source mesa" to form an etching mask. Third, the AlTi films were etched at room temperature by a standard Al etching solution. Fourth, the photoresist was removed and the line widths of the AlTi patterns were measured using optical microscope. Figure 5.5 shows an optical microphotophotograph of the AlTi pattern created by the photomask.

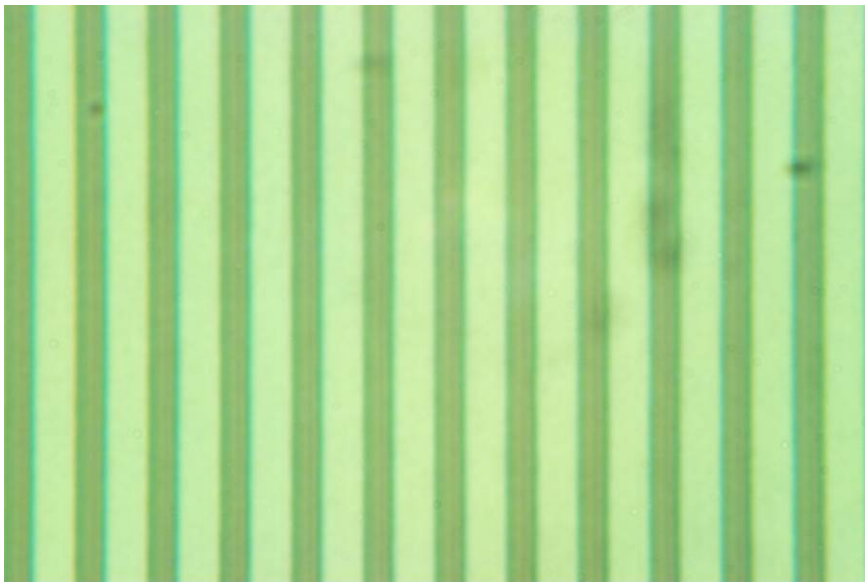
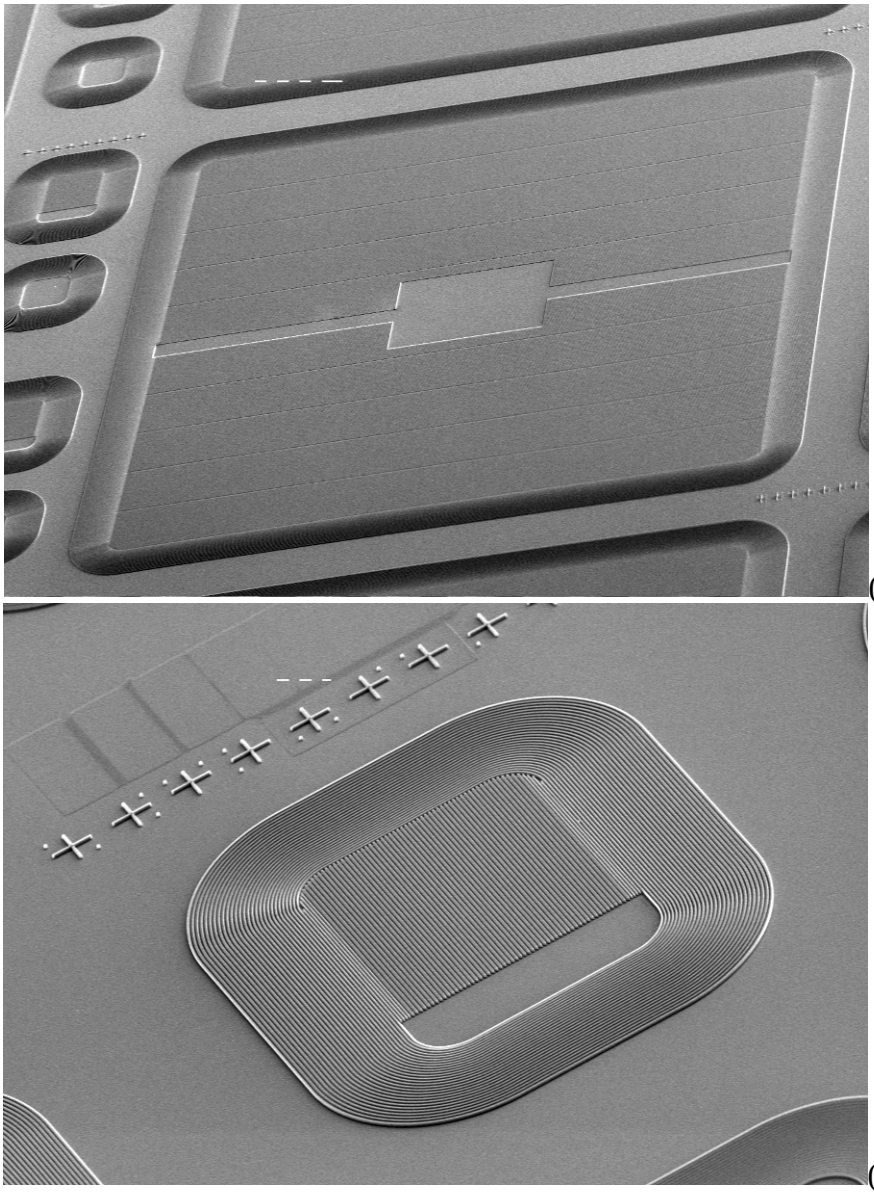


Figure 5.5. Optical microphotograph of AlTi pattern for ICP etching of mesas. The periodicity of the structure is 5.2μm.

To establish a god control of the vertical channel width the fabrication process has to ensure line-width uniformity, good vertical mesa profile and smooth mesa sidewall. To achieve a highly vertical source mesa profile an ICP etching conditions based on Bosch process (with alternative polymer deposition by C_4F_8 and dry etching by CF_4+O_2) were used. Figure 5.6 shows SEM microphotographs of etched source mesas and guard ring spacing mesas. A SEM photograph of source mesas showing a good vertical profile and smooth sidewalls is shown on Figure 5.7.



(a)

(b)

Figure 5.6. SEM microphotograph of etched source mesas and ring spacing mesas – complete device view: (a) large type device, (b) small type device.

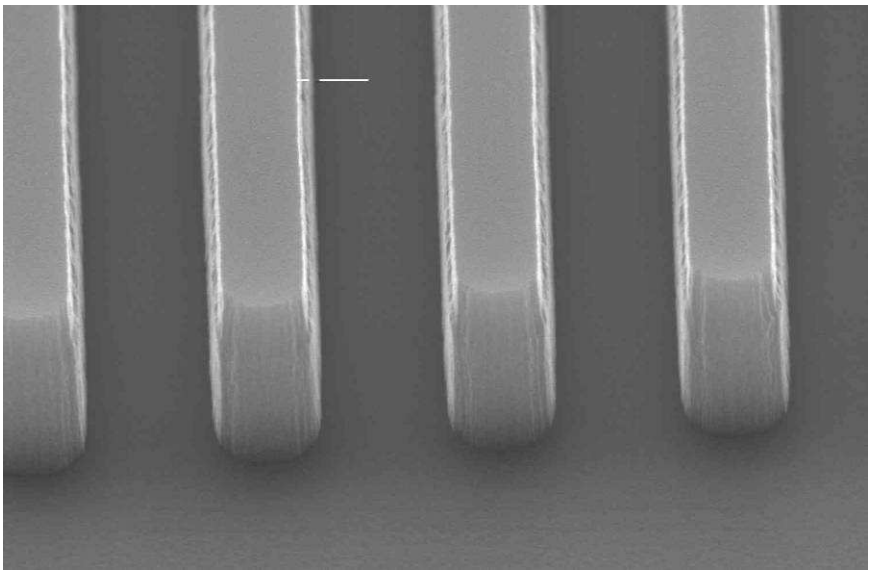


Figure 5.7. SEM microphotograph of etched source mesas. The periodicity of the structure is 5.2µm.

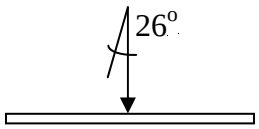
5.2.2. Gate Implantation

Gate formation is done by Aluminum ion implantation into both the source mesa sidewall and the gate trench. Photoresist mask protects the regions between devices that are not implanted. The first part of the implantation is done with tilt angle of 26^{o} from the direction normal to the sample surface. Each implantation at the specified conditions at a tilt angle of 26^{o} was repeated 4 times at the four different rotation angles and the same tilt angle. The second part of the implantation is done at a zero tilt angle to the bottom of the trenches to form a p+ body and a highly doped surface layer to form a gate ohmic contact. The implantation conditions are shown in Table 5.1 and the implantation profiles are shown on Figure 5.8. The implantation was done at four directions perpendicular to the sides of the samples. During the implantation for gate the source mesas were not covered with a mask. After the implantation the top of the source mesas will be inverted into p-type and has to be removed by planarization and dry etching process. To further

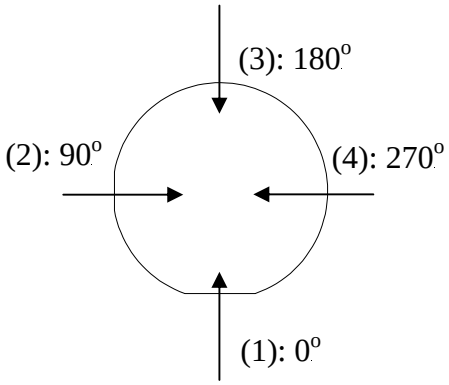
simplify the fabrication a thick-film photoresist implantation mask, instead of a metal one, was patterned to define the gate outside boundary (Figure 5.9).

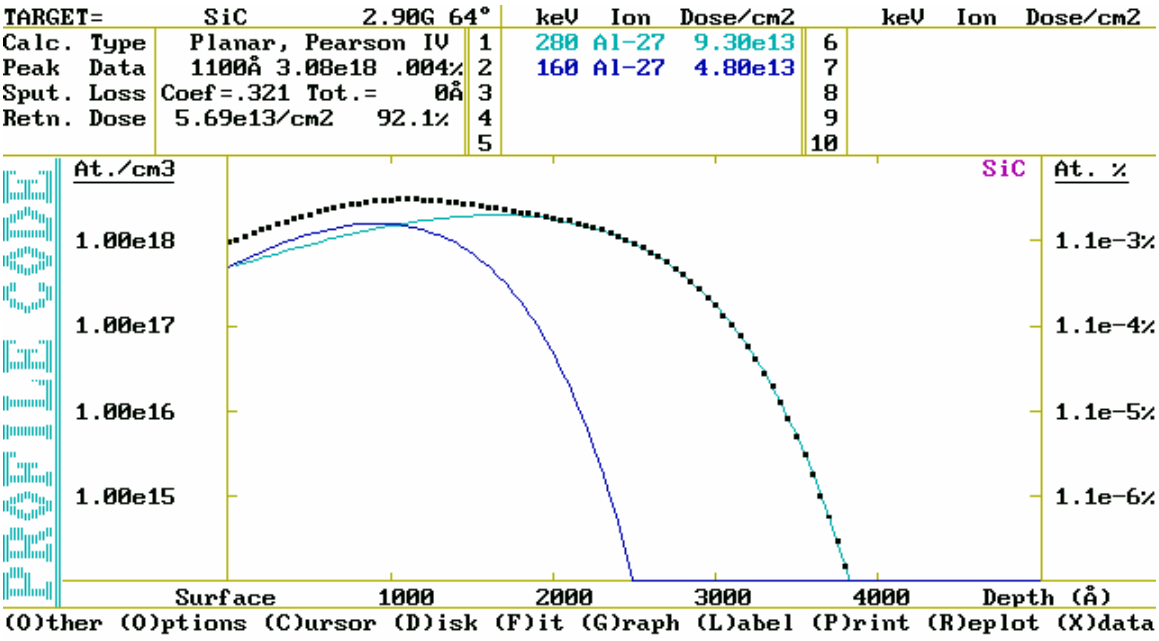
Table 5.1. Energies and doses for normally-on TIVJFET implantation.

	Ion	**Energy (KeV)**	**Dose (cm^{-2})**	**Beam angle**
1	Al	280	9.3×10^{13}	**Tilt angle** = 26^o from the direction normal to the sample surface **Rotation angle** = Four (4) directions: 0^o, 90^o, 180^o, 270^o with respect to the wafer major flat. Each implantation needs to be repeated at the four directions
2	Al	160	4.8×10^{13}	
3	Al	360	$2.7\text{x}10^{13}$	**Tilt angle** = 0^o (normal to the sample surface)
4	Al	180	9.3×10^{14}	
5	Al	110	4.1×10^{14}	

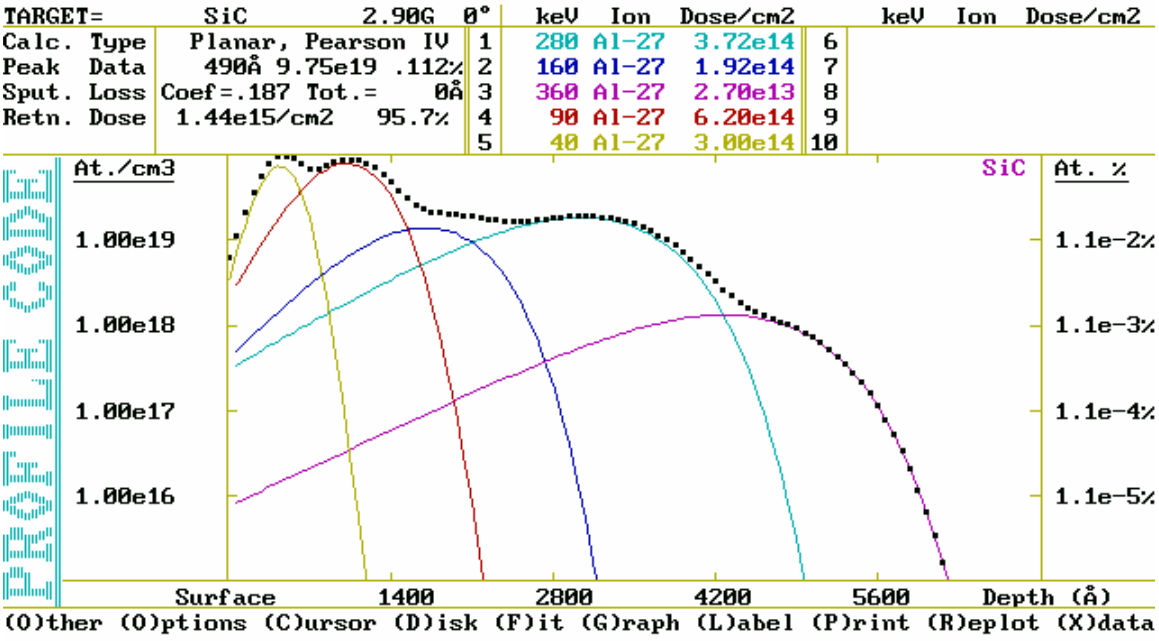


Tilt angle



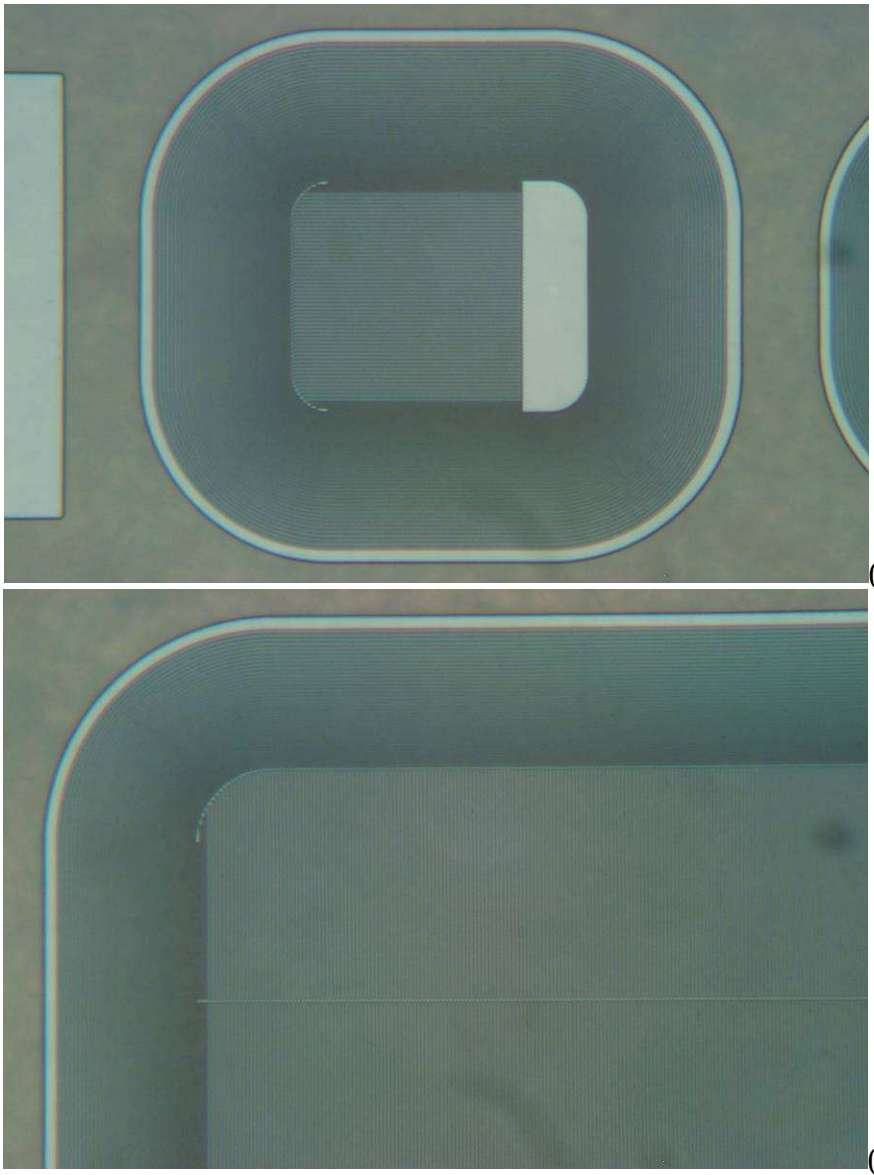


(a)



(b)

Figure 5.8. Gate implantation profile: (a) into mesa side wall, (b) into gate trench.



(a)

(b)

Figure 5.9. Optical microphotograph of photoresist implantation mask for gate implantation: (a) complete device view, (b) one corner of a device, showing part of the source mesas and the guard ring region.

5.2.3. Removing of Al-implanted Source Mesa Top

During the Aluminum implantation for gate the device source mesa tops were not covered with mask. After the gate implantation the top of the source mesas had to be removed by dry etching. A 6000Å-thick AlTi dry etching mask was deposited by sputtering. Then, a planarization step was performed to expose only the top of the source

mesa lines. Photoresist (PR) was deposited and then etched back by oxygen plasma. After etch back only the source mesa tops were not covered with photoresist. The metal covering the top of the source lines was then removed by wet etching in aluminum etchant. After that the remaining PR was removed by photoresist stripper. Figure 5.10 shows a SEM photograph of source mesas with metal removed from the top. Finally, ICP etching in CF_4+O_2 plasma was done to remove only the Aluminum-implanted top of the mesa source lines, thus restoring the n+ type of the source mesa very tops. The etched depth was 0.4μm. After the ICP etching was finished, the AlTi etching mask was removed by diluted HF.

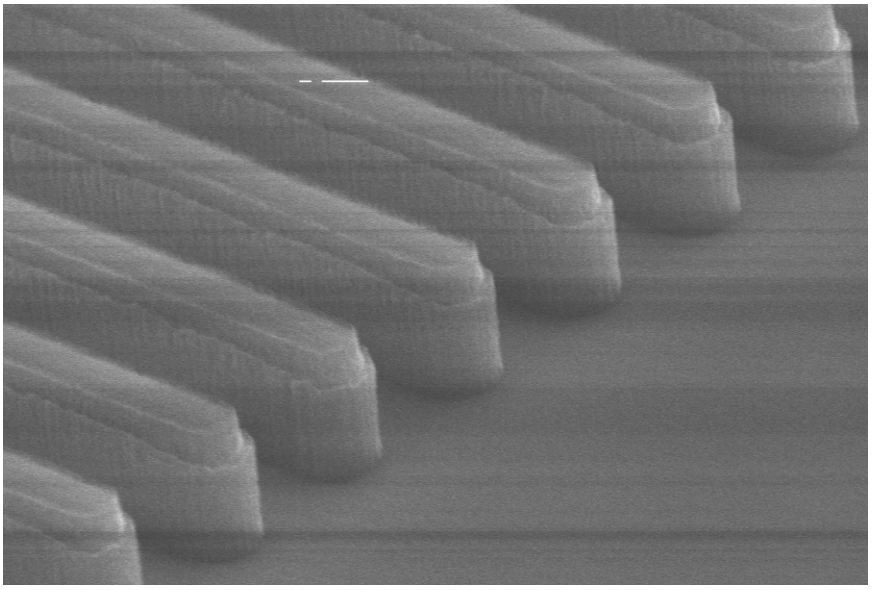


Figure 5.10. SEM microphotograph source mesas with metal removed from the top, before the source mesa top was removed by ICP etching.

5.2.4. Surface Passivation

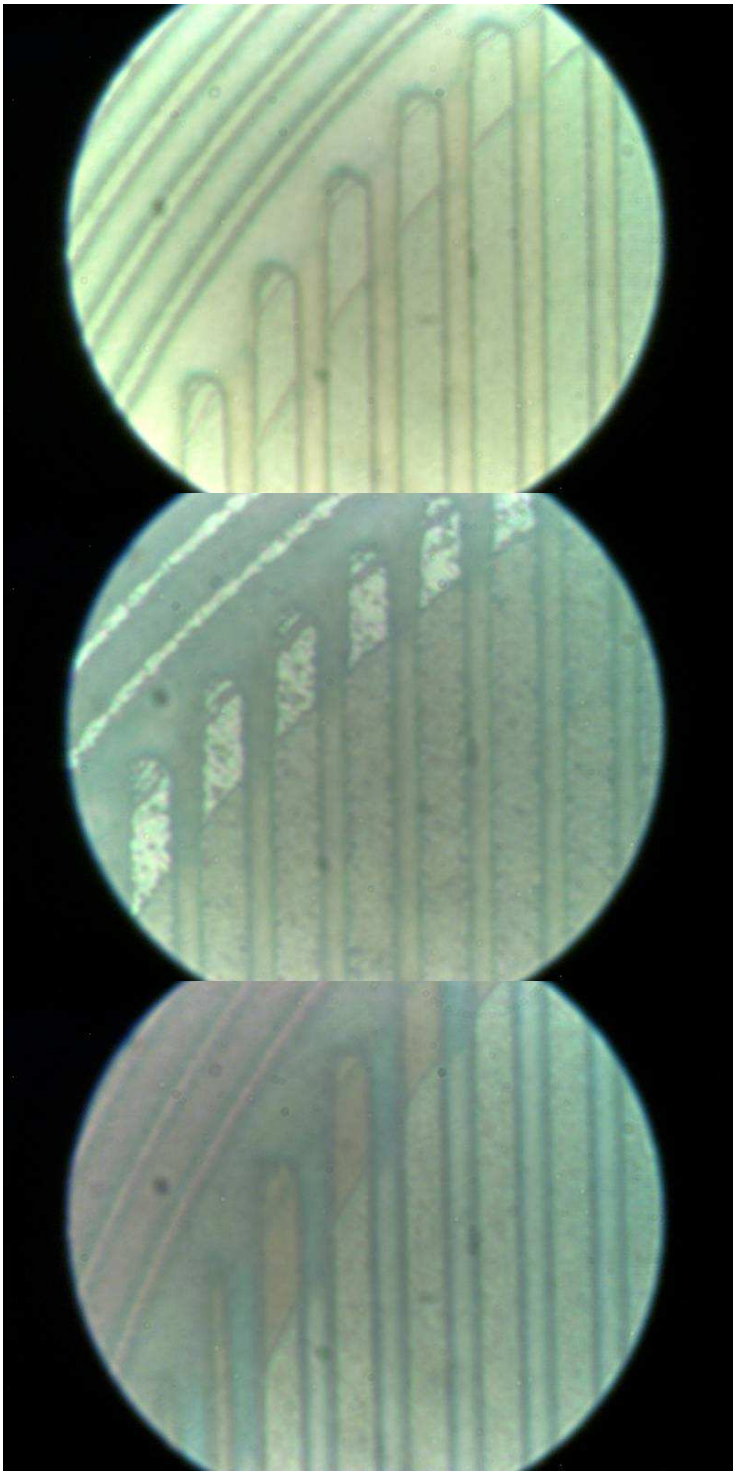
Before oxidizing the samples to form the passivation needed, the wafers were cleaned using a thorough cleaning procedure. The cleaned samples were then thermally oxidized at 1100^{o}C for 30 min in wet oxygen ambient to form a sacrificial oxide with a thickness

of approximately 150 Å. The sacrificial oxide was then removed by HF and another thermal oxidation was done at 1100^{o}C for 2 hours in wet oxygen ambient. The oxide was then annealed at 1100^{o}C for 1 hour in Ar. The thermal oxide was then covered with a PECVD 1000Å-thick SiO_2 layer, followed by a 2000Å-thick Si_3N_4.

5.2.5. Gate, Source and Drain Contact Formation

A new approach was implemented that allows self-aligned source metal definition without using a lift-off step. The idea utilizes the fact that metals, such as nickel (Ni), react with SiC when heated to form silicides, but will not react with SiO_2. This process is commonly used in Si technology and can provide important benefit if implemented for SiC devices. The process was developed with the joint efforts from the people in SiCLAB. Later it was found that a similar process is patented by Denso Corporation [32].

Fist windows were opened in the passivation. Photolithography was done with mask "(3) Gate Contact", using thick-film photoresist. The passivation on top of the gate and the source was etched by ICP etching with CF_4 plasma, using a high substrate bias. Due to the anisotropic nature of this etching only the horizontal surface of the gate and the source were etched and the mesa sidewall was not affected. Nickel with thickness of 1500Å was blanket deposited by sputtering on the sample surface.



(a)

(b)

(c)

Figure 5.11. Optical microphotograph source and gate nickel silicide contact formation: (a) sputtered metal before annealing, (b) metal after annealing; (c) contacts after non-reacted metal removed.

The contact metal was then annealed at relatively low temperature around 700^{o}C to form nickel silicide on the source and the gate, but not on the oxide covered mesa sidewall. This relatively low-temperature annealing is not enough to form ohmic contact, but is sufficient to ensure that Ni will react with SiC and form nickel silicide. The annealed metal was then wet etched until the unreacted metal was removed. The result was that only the top of the source mesas and the gate trenches were covered with silicide. Figure 5.11 illustrates the nickel silicide contact formation process.

After that the passivation from the sample back side was removed by etching in buffered HF and AlTi/Ni was deposited by sputtering for a drain contact. Next, a high temperature annealing was done RTA system at temperatures above 900^{o}C in H_2/Ar (5%/95%) gas mixture that would create ohmic contacts on the gate, source and drain at the same time.

5.2.6. Gate Metal Overlay Formation

In order to increase device current density and switching performance, and utilize fully the total device active area the gate metal resistance needs to be decreased. This can be done by increasing the gate metal thickness and using metals with lower resistivity. In this batch in addition to the metal used to form the ohmic contact to the gate, we used gate metal overlay that increased the total metal thickness. Systematic experiments were done to find a process to define copper gate overlay, as Cu has second lowest resistivity after silver. To improve adhesion and avoid Cu oxidation gate overlay should consist of thee layers – AlTi/Cu/TiW with total thickness of about 1μm. Wet etching, which is the process used to define the overlay, is a challenging task for such a multiplayer structure. Multiple etching experiments were done with the above multiplayer structure.

AlTi/Cu/TiW layer was sputtered on the sample surface. Then a PR planarization step was done to expose the source mesa top. The top TiW layer was etched by hydrogen peroxide, the Cu layer was etched by ammonium persulfate and the bottom AlTi was etched by phosphoric acid. The control of this wet etching process was found to be extremely difficult. Due to planarization uniformity limitations, Cu was over-etched in one part of the device while still remaining on another. It was concluded that this process is not suitable for a reliable fabrication due to the small error margin. Figure 5.12 illustrates the Cu process.

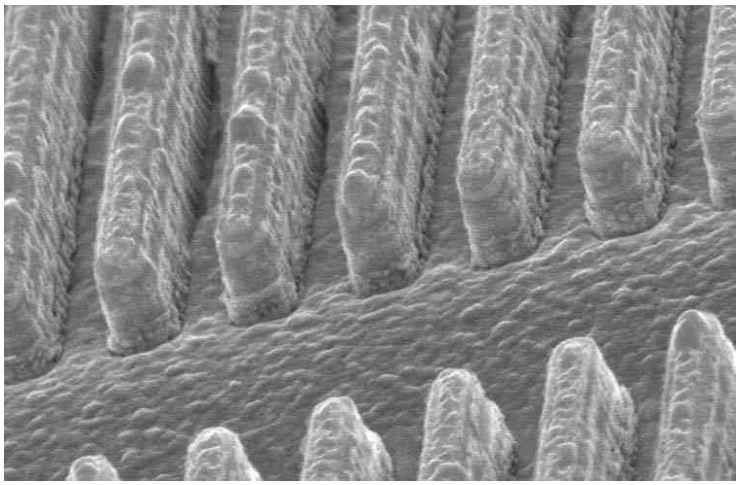


Figure 5.12. SEM photograph of source mesas and gate trenches after AlTi/Cu/TiW gate metal overlay was etched from the source mesa top and sidewalls. The mesa sidewall is not completely cleaned and the trench is already severely attacked by the etchant.

Eventually a layer of AlTi/No/AlTi was used to form the gate overlay, as that process is much more reliable. A thick layer of AlTi/Mo/AlTi with a thickness of 1μm was deposited on the sample surface to serve as an additional gate metal overlay. To remove the metal from the source and leave it only in the gate region a photoresist planarization process was used. Photoresist was deposited on the surface and then etched back by O_2 plasma to expose the source mesas. After that the metal was etched by aluminum etchant until it was removed from the source mesa top and sidewall. Figure 5.13 shows the gate

metal overlay layer before (a), after it was partially (b) and completely (c) removed from the source mesa top and sidewall.

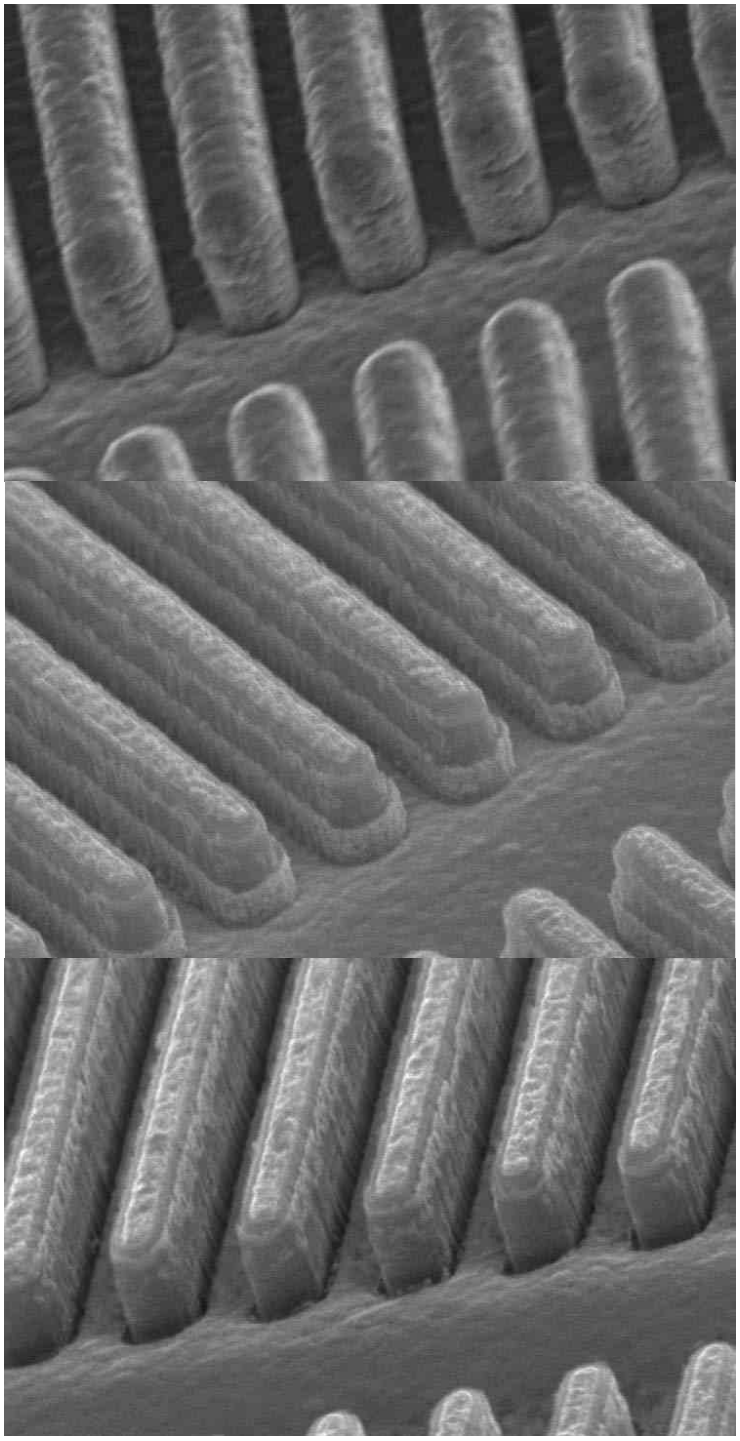


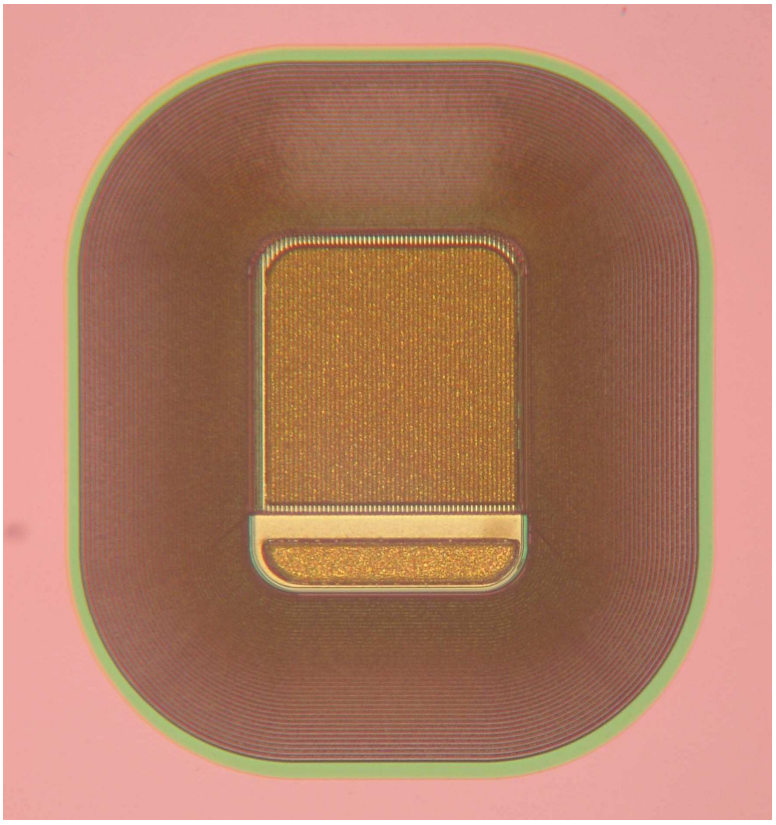
Figure 5.13. SEM photograph of source mesas and gate trenches before (a), after gate metal overlay was partially (b) and completely (c) etched from the source mesa top and sidewall.

5.2.7. Trench Filling Planarization and Source Metal Overlay Formation

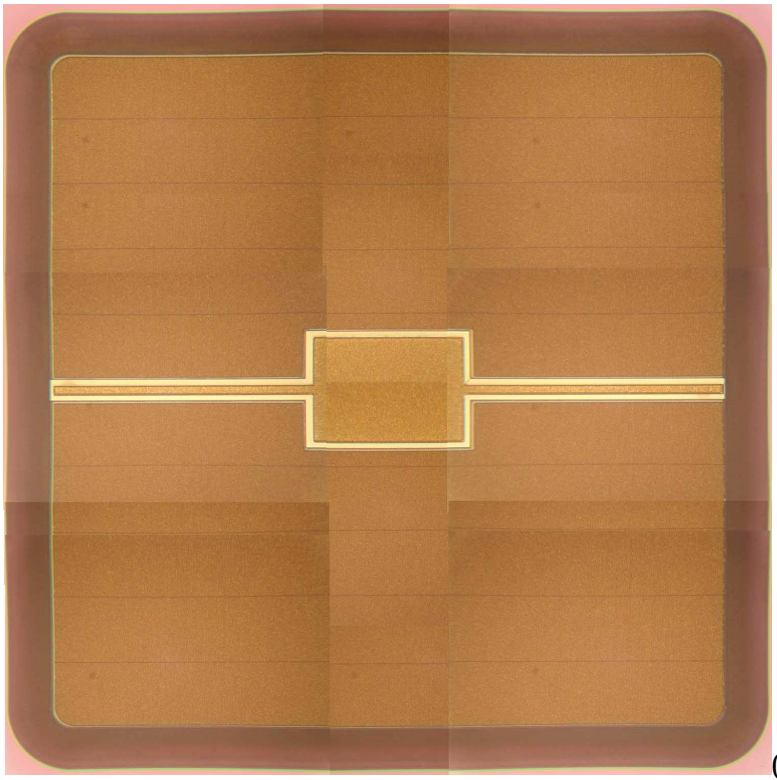
This fabrication step consists of two phases – (a) deposition and planarization etch-back of trench-filling material and (b) deposition and patterning of source metal overlay.

Trench filling was done using a thick layer of silicon dioxide. First the gate trench was filled with silicon dioxide deposited by PECVD. The deposition was done in four steps to get a total thickness of 1.2µm. Second, an oxide planarization etch back was done in ICP Freon plasma to expose the source contacts. A metal AlTi mask was used to protect the gate trenches. The mask was deposited by sputtering and patterned by planarization etch back with photoresist in O_2 plasma and metal wet etching with aluminum etchant. Third, the gate-pad contact windows were defined in the oxide film. This was done by ICP etching with thick-film photoresist as a mask.

Metal overlays for the source and gate contact pads were deposited on the etched-back surfaces and patterned by photomask "(5) Metal Overlay". The source pad is directly placed on the active area of each device to connect the source contacts exposed by the preceding etch-back process. The overlay metal consists of three layers – Al/Ti/Au with a total thickness of 2.5µm, patterned by photolithography and lift-off. Figure 5.14 shows the optical microscope photographs of the fabricated device and Figure 5.15 shows a view of a complete 2-inch wafer.



(a)



(b)

Figure 5.14. Optical microscope photo of a normally-on TIVJFET device after the final metal overlay was done (a) “small” device, (b) “large” device.

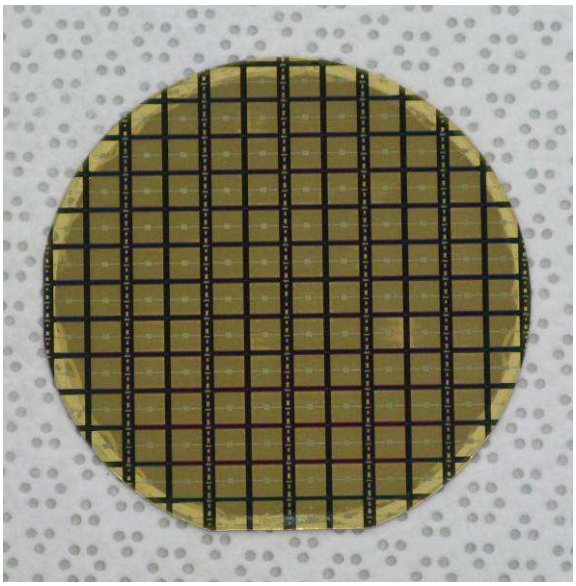


Figure 5.15. Optical microscope photo of a complete 2-inch wafer with normally-on TIVJFET devices after the final metal overlay was done.

5.3. Characterization

5.3.1. TLM Test Pattern Characterization

The quality of the gate ohmic contact reflects on the operation of a HF-TIVJFET switching device. Although the gate of a TIVJFET is not conducting high current, lowering the gate contact resistance is important for reducing the device switching speed. The higher the resistance, the slower the device switching will be. A transmission line model (TLM) structures were used to evaluate the gate ohmic contact. The results are show on Figure 5.16. The contact resistance extracted from the data was found to be in the range $1.8\times10^{-3}\Omega.cm^2$ – $2.2\times10^{-3}\Omega.cm^2$, which although not record low is very reasonable and completely adequate.

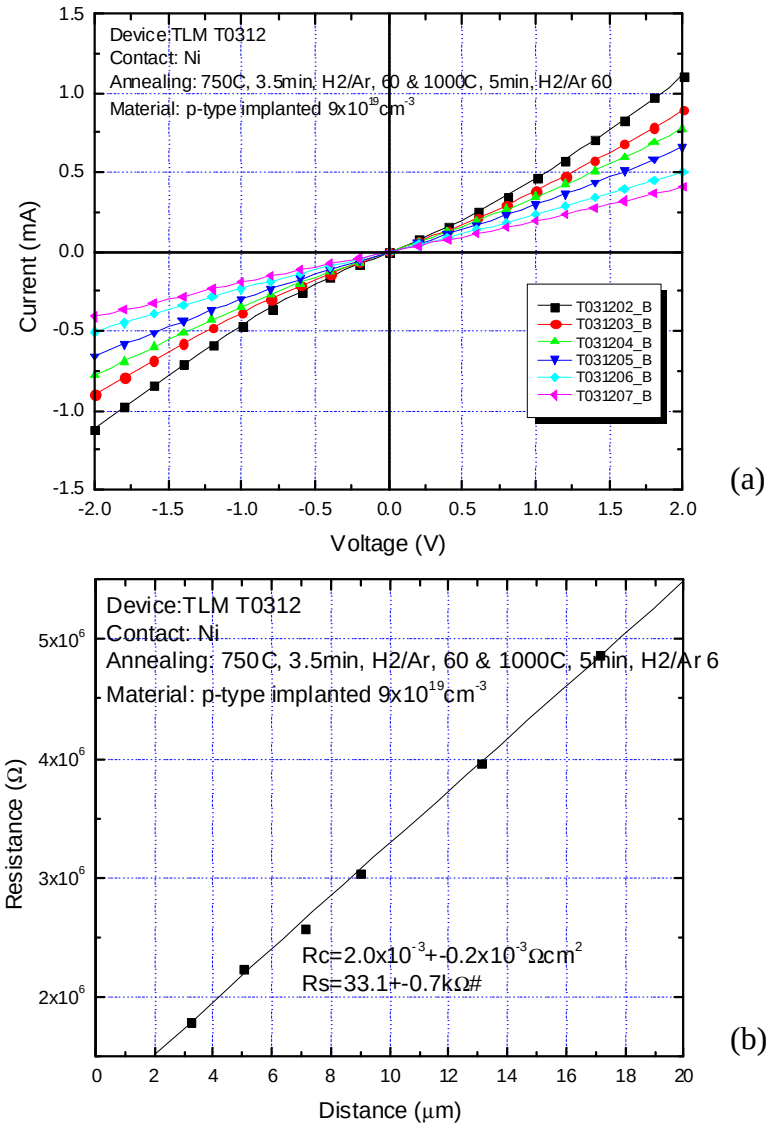
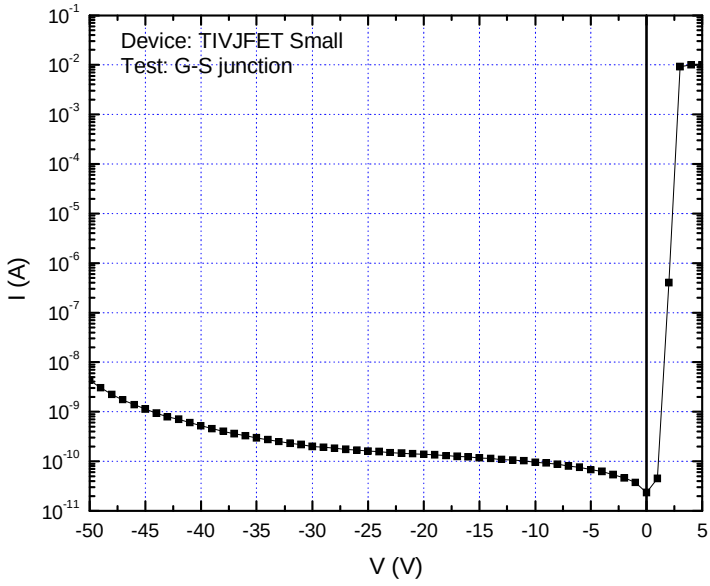


Figure 5.16. TLM characterization of p-type contacts: (a) TLM contacts I-V curves, (b) TLM resistance vs. contact spacing.

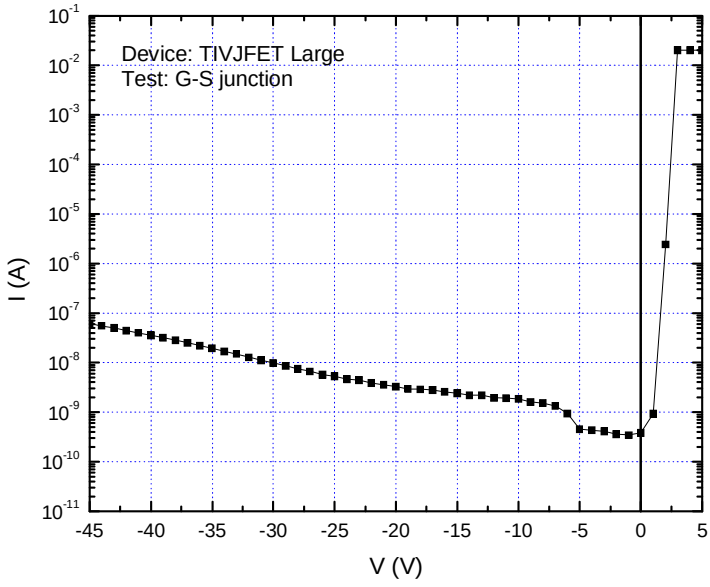
5.3.2. Gate-Source Junction Characterization

The quality of the gate-source p-n junction is important for the proper JFET operation. This junction should be able to block high enough voltage and ensure low leakage currents in the gate voltage operating range. A typical gate-source junction I-V curve is shown on Figure 5.17. The gate-source junction breakdown voltage is more than 50V

(Figure 5.18). The leakage currents observed are low and the device can be safely operated with a gate voltage of up to -40V.



(a)



(b)

Figure 5.17. Typical gate-source junction I-V characteristics: (a) “small” type device, (b) “large” type device.

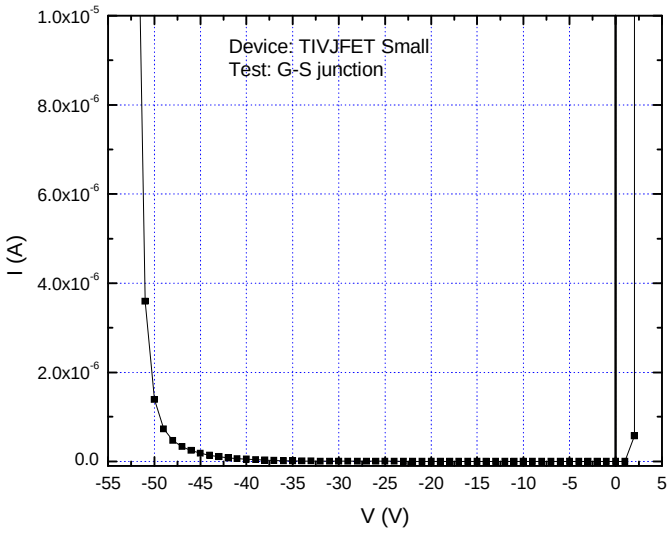


Figure 5.18. A gate-source junction I-V characteristics, showing a breakdown voltage of about 50V.

5.3.3. JFET Blocking and Forward Conduction Characterization

The reverse blocking characteristics and the forward conduction characteristics were tested with a Tektronix 371A curve tracer. The high voltage measurements were done with the samples immersed in Fluorinert™ electronic liquid.

The I-V characteristics for "small" type devices are shown on Figure 5.19. In all of the figures the leakage currents are multiplied by factor of 1000 to show more details. The gate-source p-n junction currents for the same three devices are shown on Figure 5.20. The device on Figure 5.19(a) can block 1562V with gate voltage of -45V and has a forward current of I_{DS}=0.16A and a specific on resistance R_{SPON}=2.8mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V and, I_{DS}=0.103A and R_{SPON}= 4.4mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=0V. The gate current at V_{GS}=2.5V is 107μA, which corresponds to a current gain of 1495 at V_{DS}=0.5V, and 3178 at V_{DS}=1V. The device on Figure 5.19(b) can block 1492V with gate voltage of -40V and has a forward current of I_{DS}=0.175A and a specific on

resistance R_{SPON}=2.4mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V and, I_{DS}=0.125A and R_{SPON}=3.7mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=0V. The gate current at V_{GS}=2.5V is 114μA, which corresponds to a current gain of 1543 at V_{DS}=0.5V, and 3026 at V_{DS}=1V. The device on Figure 5.19(c) can block 1232V with gate voltage of -30V and has a forward current of I_{DS}=0.208A and a specific on resistance R_{SPON}=2.2mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V and, I_{DS}=0.138A and R_{SPON}=3.3mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=0V. The gate current at V_{GS}=2.5V is 143μA, which corresponds to a current gain of 1454 at V_{DS}=0.5V, and 2762 at V_{DS}=1V.

The I-V characteristics for “large” type devices are shown on Figure 5.20. In all of the figures the leakage currents are multiplied by factor of 1000 to show more details. The forward current was measured only on one half of the cell due to probing limitations. The blocking voltage of the large devices is not as high as that of the small devices. Both small and large devices have identical vertical channel width and termination, so ideally they should have the same performance. The reason for the discrepancy is that large device performance is limited by both wafer defects and process-introduced localized defects. Channel width and guard ring spacing nonuniformity could limit blocking capabilities. Localized wide channel or wide guard ring spacing spots can severely limit a large device performance. For example such defects may be introduced by dust during photolithography of implantation.

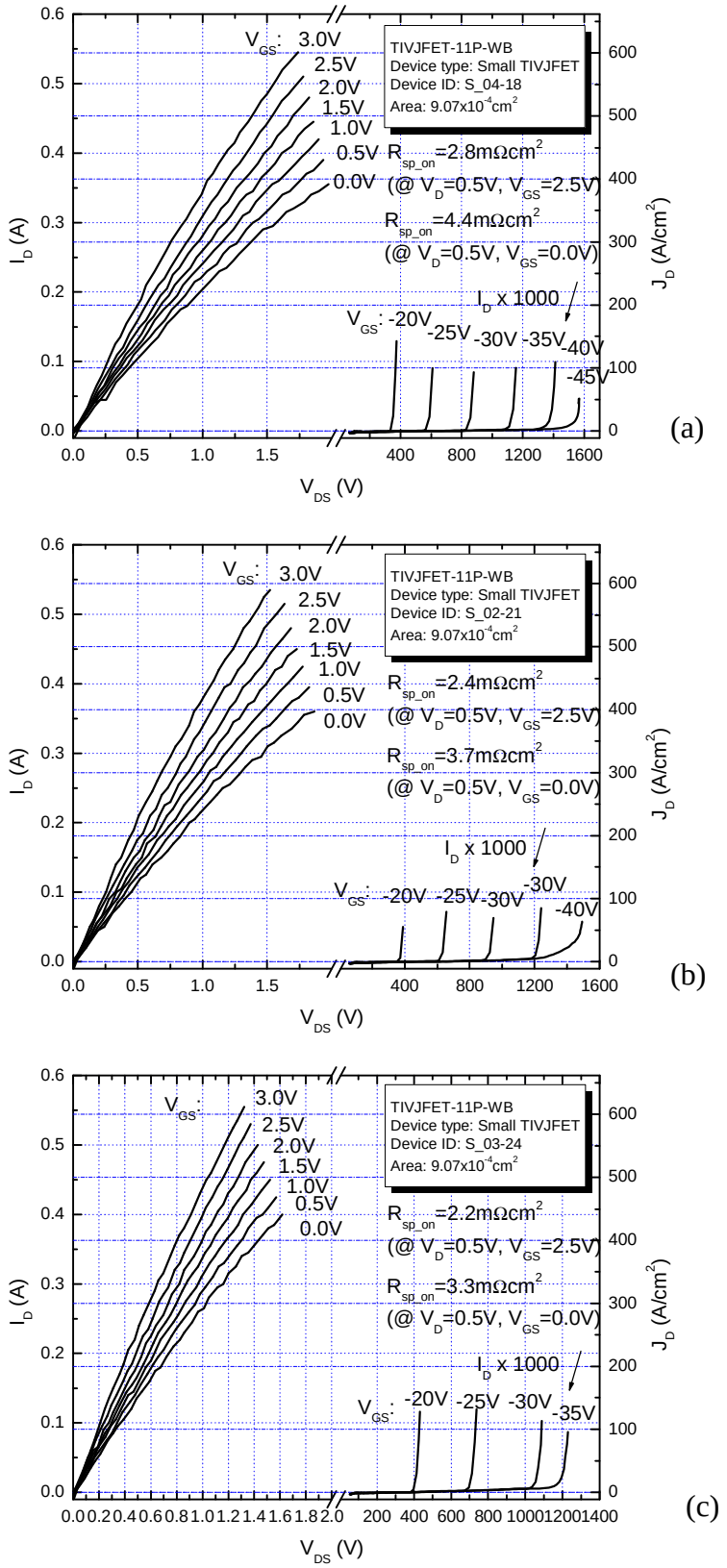


Figure 5.19. I-V characteristics of “small” type normally-on TIVJFETs

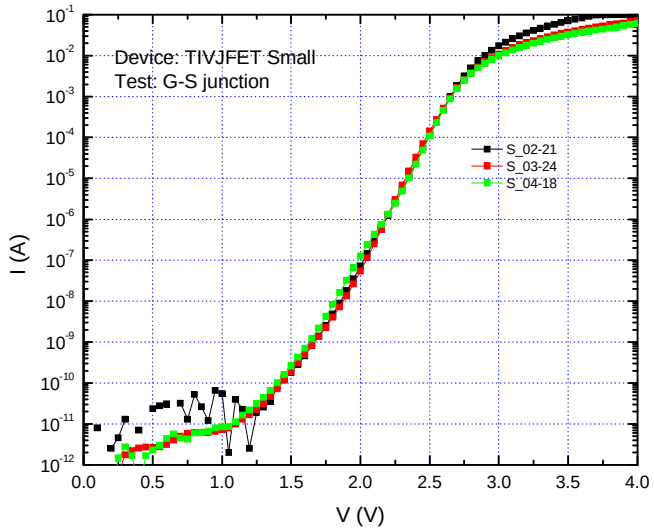
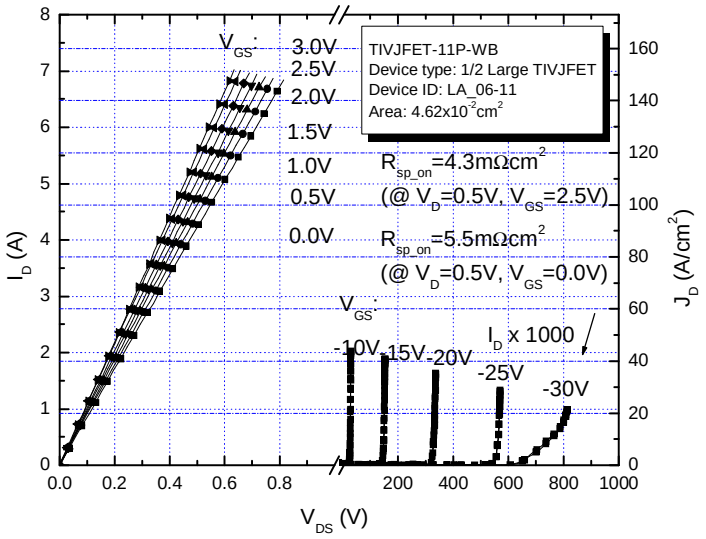
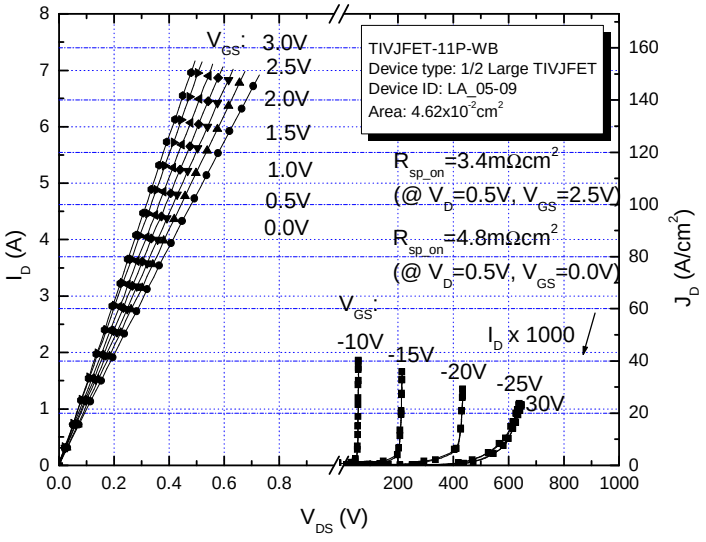


Figure 5.20. Forward I-V characteristics of a gate-source p-n junction of the TIVJFETs from Figure 5.19.

The device on Figure 5.21(a) can block 816V with gate voltage of -30V and has a specific on resistance R_{SPON}=4.3mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V and, R_{SPON}= 5.5mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=0V. The device on Figure 5.21(b) can block 604V with gate voltage of -30V and has a specific on resistance R_{SPON}=3.4mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V and, R_{SPON}= 4.8mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=0V.



(a)



(b)

Figure 5.21. I-V characteristics of "large" type normally-on TIVJFETs. The forward current was measured only for ½ of the area and limited to below 8A due to probing limitations.

5.3.4. Blocking Voltage Mapping

Mapping of device blocking voltage is shown on Figure 5.22-5.24. A guard ring structure was used in the design and fabrication of the normally-on TIVJFET. Test p-n diodes with identical guard ring termination were included in the design of the photomask to evaluate the efficiency of the approach. The test diodes were distributed across the sample to

check the effect of process nonuniformity on the blocking capabilities of the structure. The experimental results for the blocking voltage of p-n diodes with nonuniform spacing guard ring termination are shown on Figure 5.22. The wafer structure was designed to ensure at least 1200V blocking capability. It can be seen that the approach provides a good blocking capability and uniformity with the majority of diodes exceeding the design blocking voltage of 1200V. At the same time the fabrication process becomes substantially simpler because guard ring formation does not require a separate processing step as they are formed together with the JFET vertical channels. A maximum blocking voltage of 1900V was reached, which is close to the theoretical limit. There is some variation of the blocking voltages across the wafer that is probably due to local variation in guard ring spacing and a few wafer defects.

The blocking voltage mapping of small type TIVJFETs is shown on Figure 5.23-5.23. It can be seen that many of the devices have reached the designed blocking voltage value. Generally, the blocking capabilities of the JFETs haven’t reached the values of that for the p-n diodes and there is a larger variation across the wafer. The JFET blocking is limited by the vertical channel opening, since the termination is identical to that of the p-n diodes. The larger variation in values is probably also contributed by the quality of the gate-source p-n junction.

The blocking voltage mapping of large type TIVJFETs is shown on Figure 5.25. The blocking voltages reached are substantially smaller than that for the small type devices. The reason for this is that large device performance is limited by both wafer defects and process-introduced localized defects.

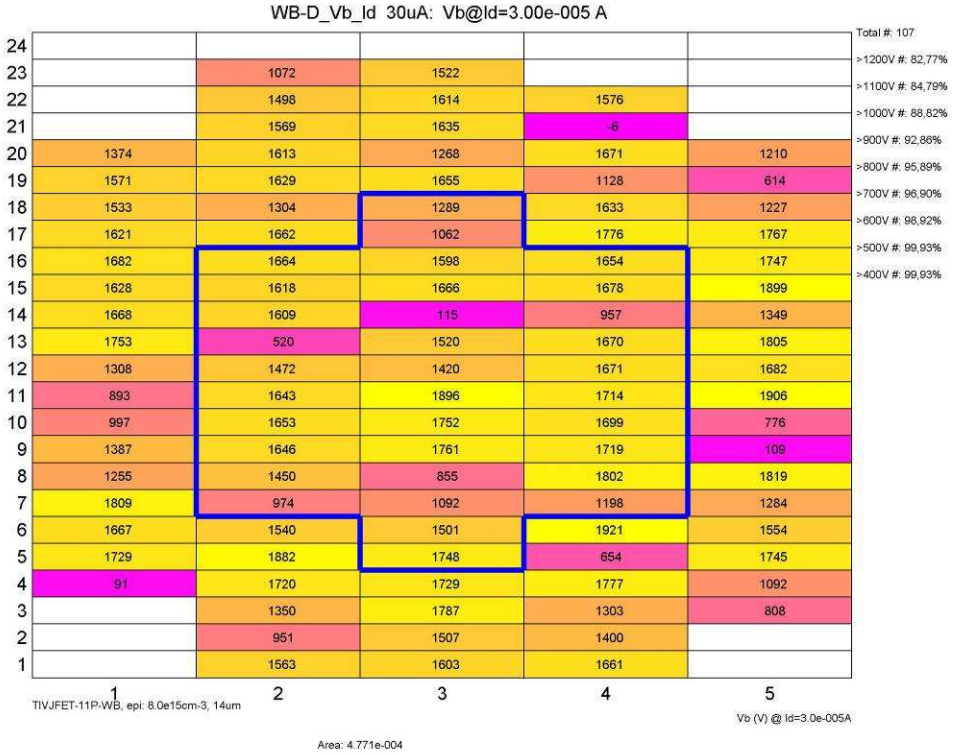


Figure 5.22. Test p-n diodes reverse blocking voltage.

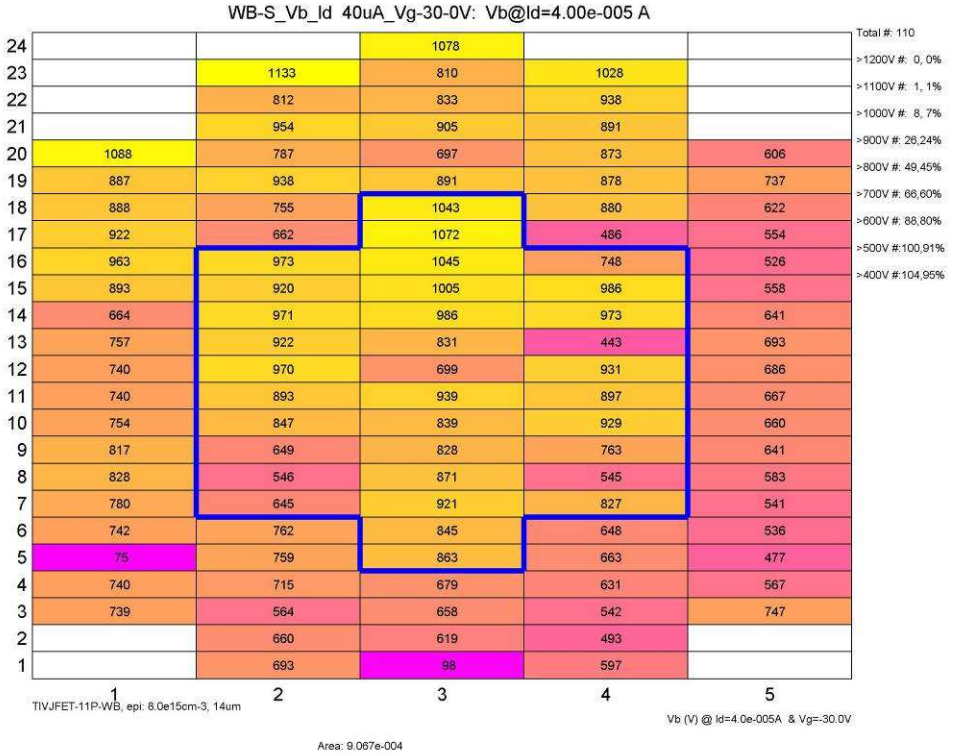


Figure 5.23. Small TIVJFET reverse blocking voltage @ V_{GS}=-30V.

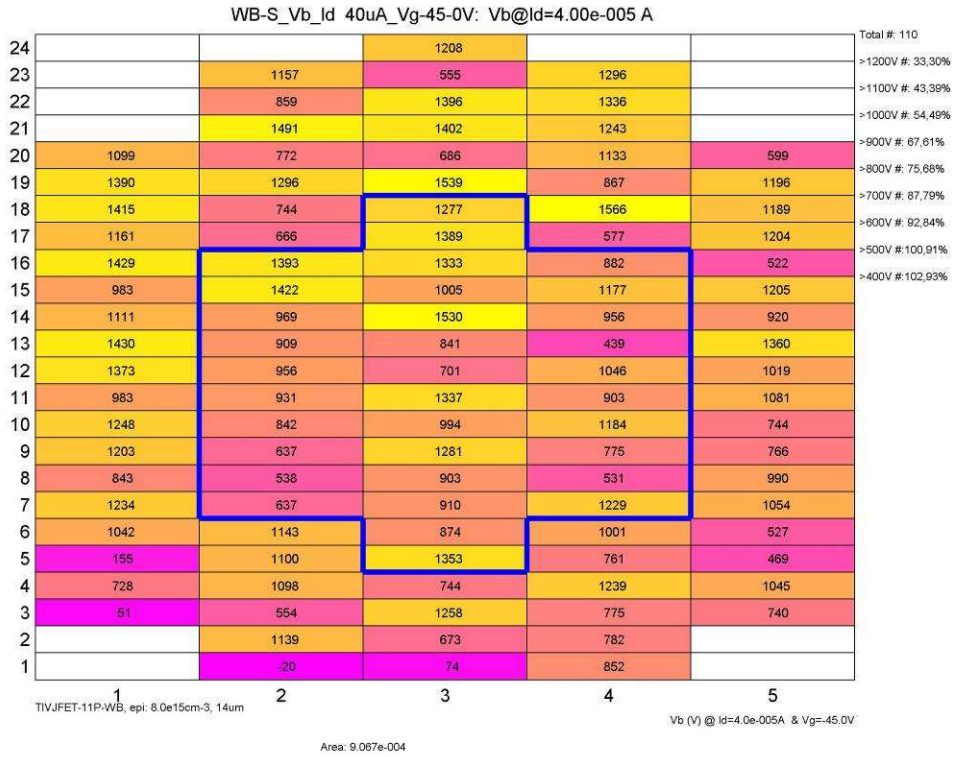


Figure 5.24. Small TIVJFET reverse blocking voltage @ V_{GS}=-45V.

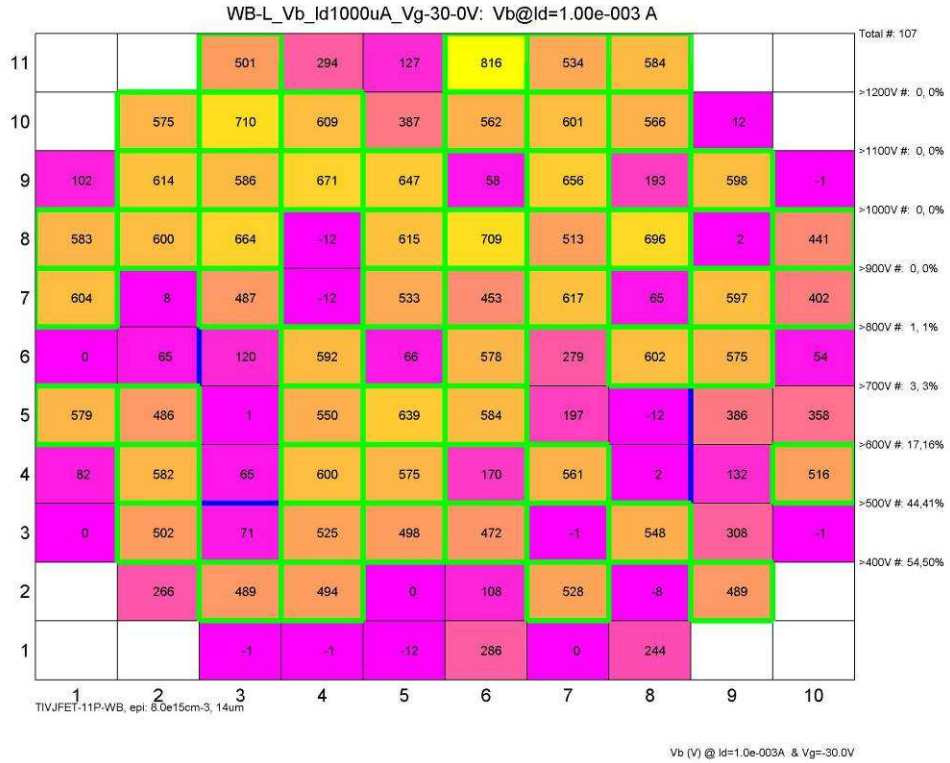


Figure 5.25. Large TIVJFET reverse blocking voltage @ V_{GS}=-30V.

5.3.5. Specific On-resistance

The TIVJFET specific on-resistance $R_{SP\text{-}ON}$ was extracted from the I-V data for all measured devices at a drain voltage of 0.5V and a gate voltage of 0V and 2.5V. The results for small devices are shown on Figure 5.26 and Figure 5.27. The smallest $R_{SP\text{-}ON}$ at V_{DS}=0.5V & V_{GS}=0V is 3.0mΩ.cm^2, and the smallest $R_{SP\text{-}ON}$ at V_{DS}=0.5V & V_{GS}=2.5V is 2.1mΩ.cm^2. The observed variation in $R_{SP\text{-}ON}$ is due to vertical channel width and channel doping variation. The specific on-resistance is very uniform in the wafer center where the channel width is uniform and is noticeably lower for devices located very close to the wafer edge. The source mesa, and hence the vertical channel, for those edge devices is slightly narrower, so the reason for smaller $R_{SP\text{-}ON}$ has to be a higher channel/drift epilayer doping concentration close to the wafer edge.

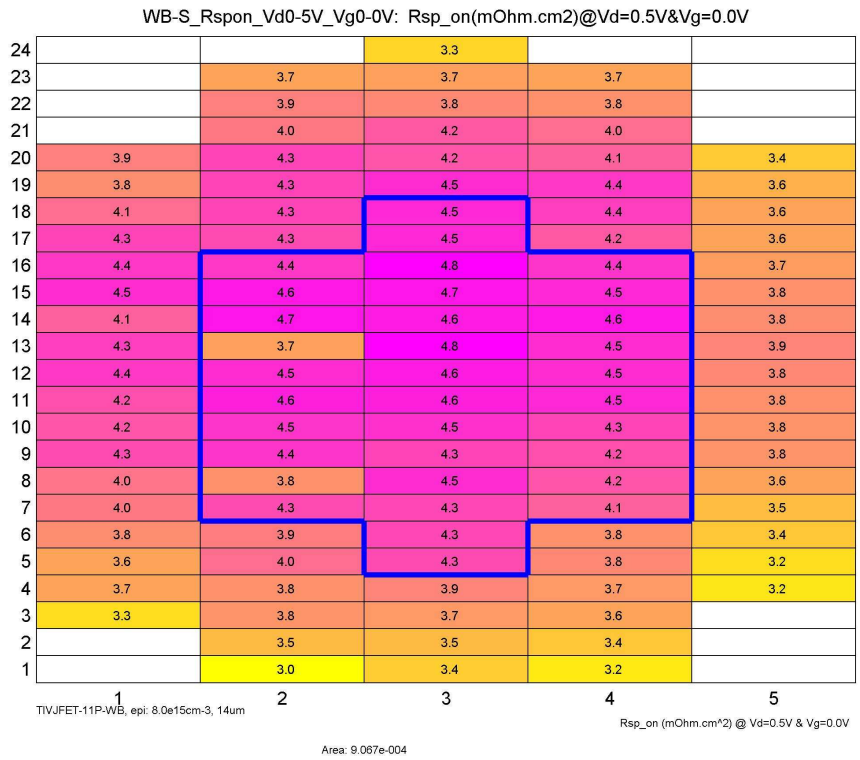


Figure 5.26. Small TIVJFET reverse blocking voltage @ V_{DS}=0.5V & V_{GS}=0V.

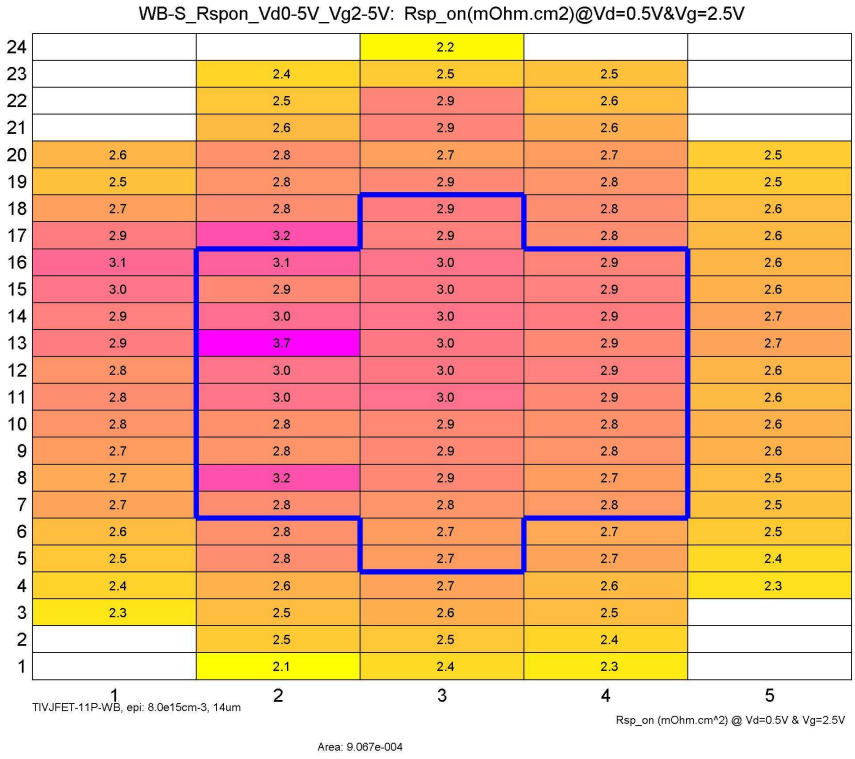


Figure 5.27. Small TIVJFET reverse blocking voltage @ V_{DS}=0.5V & V_{GS}=2.5V.

Let us consider the values for the specific on-resistance in more detail and compare them to the theoretical expectations. There are several factors contributing to $R_{SP\text{-}ON}$ – drift layer resistance, channel resistance, substrate resistance, source contact resistance and drain contact resistance.

(i) Drift layer resistance:

$$R_{D-SP} = \rho d = \frac{d}{q\mu N_D} = 1.08\Omega.cm^2$$

For the drift layer of d=11.5μm with doping of $N_D=8\times10^{15}cm^{-3}$ a mobility of $\mu=829cm^2/Vs$ is assumed for the calculations.

(ii) Channel resistance:

$$R_{CH-SP} = \rho L_{CH} \frac{W_{CH} - 2W_D}{W_P} = \frac{L_{CH}}{q\mu N_D} \frac{W_{CH} - 2W_D}{W_P} =$$

$$= 1.63\Omega.cm^2 (V_{GS} = 0V) / 0.78\Omega.cm^2 (V_{GS} = 2.5V),$$

where L_{CH}=2.5μm is the channel length, W_{CH}=2.0μm is the channel width, $W_D = \sqrt{\frac{2\varepsilon_s (V_{bi} - V_{GS})}{qN_D}}$ is the depletion region width, and W_P=5μm is the unit cell width.

(iii) Substrate resistance:

$$R_{Sub-SP} = \rho_{Sub} d_{Sub} = 0.66\Omega.cm^2,$$

where ρ_{Sub}=0.018Ω.cm is the substrate resistivity, and d_{Sub}=366μm is the substrate thickness.

(iv) Drain and Source ohmic contact resistance:

$$R_{DS-SP} = R_{C-SP} + R_{C-SP} \frac{W_P}{W_S} = 0.02 + 0.04 = 0.06m\Omega \cdot cm^2,$$

where a contact specific on resistance $R_{C\text{-}SP} = 2 \times 10^{-5} \Omega \cdot cm^2$ is assumed for the nickel silicide contact, W_S=2.53μm is the source mesa top width, and W_P=5μm is the unit cell period.

(v) Total specific on resistance is:

$$R_{SPON} = R_{D-SP} + R_{CH-SP} + R_{Sub-sSP} + R_{DS-SP}.$$

The total R_{SPON} is thus 2.58Ω.cm^2 for V_{GS}=2.5V, which is in a reasonable agreement with the experimental data of 2.1-3.1Ω.cm^2, considering the variation in channel width and epilayer doping. Table 5.2 shows the expected variation of R_{SPON} and its components

with a variation of drift/channel doping concentration and channel width. A deviation of the epilayer doping of 20% from the specification values could be expected.

Table 5.2 Specific on resistance variation with epilayer doping and channel width variation.

N_D (cm^{-3})	W_{CH} (μm)	$R_{D\text{-}SP}$ ($\Omega.cm^2$)	$R_{CH\text{-}SP}$ ($\Omega.cm^2$)	$R_{Sub\text{-}SP}$ ($\Omega.cm^2$)	$R_{DS\text{-}SP}$ ($\Omega.cm^2$)	R_{SPON} ($\Omega.cm^2$)
6.4×10^{15}	1.9	1.06	1.33	0.66	0.06	3.12
	2.0	0.99	1.33	0.66	0.06	3.04
	2.1	0.93	1.33	0.66	0.06	2.98
8.0×10^{15}	1.9	0.83	1.08	0.66	0.06	2.64
	2.0	0.78	1.08	0.66	0.06	2.58
	2.1	0.73	1.08	0.66	0.06	2.53
9.6×10^{15}	1.9	0.69	0.92	0.66	0.06	2.32
	2.0	0.64	0.92	0.66	0.06	2.28
	2.1	0.60	0.92	0.66	0.06	2.24

5.3.6. JFET Threshold Voltage and Vertical Channel Width Uniformity

The threshold voltage of a JFET can be extracted from the transfer (I_D-V_{GS}) characteristics. The drain current of a JFET with a uniformly doped channel can be written as [41]:

$$I_D = G_i\left\{V_{DS} - \frac{2}{3\sqrt{V_P}}\left[\left(V_{bi}+V_{DS}-V_{GS}\right)^{3/2} - \left(V_{bi}-V_{GS}\right)^{3/2}\right]\right\}, \qquad (5.1)$$

where $G_i = \frac{Zq\mu_n N_D a}{L_{CH}}$ (5.2) is the full channel conductance, and $V_P = \frac{qN_D a^2}{2\varepsilon_S}$ (5.3) is the pinch-off voltage, n is the channel doping, a is the half channel width, Z is the device unit cell width, and L_{CH} is the channel length.

In the linear region, where $V_D << V_G$ and $V_D << V_P$ Eq. 5.1 is reduced to

$$I_D = G_i\left(1-\sqrt{\frac{V_{bi}-V_{GS}}{V_P}}\right)V_{DS}\,. \tag{5.4}$$

The threshold voltage of a JFET is defined by

$$V_T = V_{bi} - V_P\,. \tag{5.5}$$

Equation 5.4 can be simplified using Taylor's expansion around $V_{GS} = V_T$ to be

$$I_D = \frac{G_i}{2V_P}(V_{GS}-V_T)V_{DS}\,,\ \text{for}\ V_{GS}\approx V_T \tag{5.6}$$

The threshold voltage can be found by applying a very small V_{DS} and measuring the drain current versus the gate voltage. The drain current depends linearly on V_{GS} when V_{GS} is around V_T.

The transfer chracteristics of small TIVJFETs were measured with V_{DS} = 0.05V and the threshold voltage was extracted from the linear portion of the curve around V_T. A typical I-V curve is shown on Figure 5.28

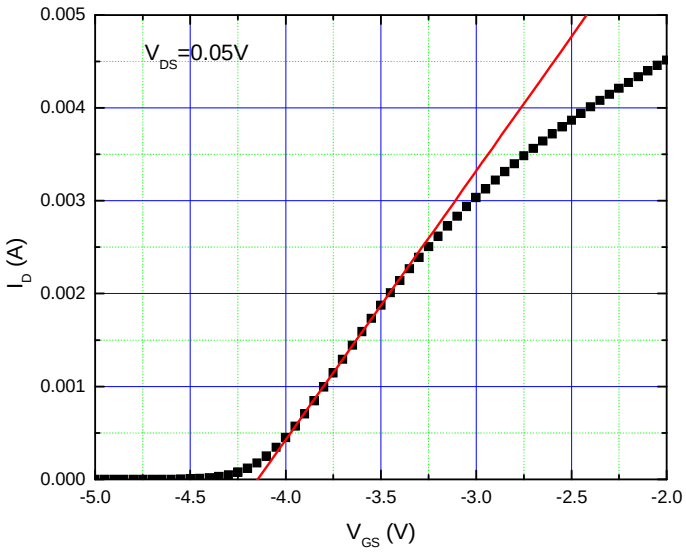


Figure 5.28. Transfer characteristics of a small type TIVJFET with V_{DS} = 0.05V. The threshold voltage V_T was extracetd from the linear part of the curve.

The JFET threshold voltage depends on the vertical channel doping and channel width (Eq. 5.3 and Eq. 5.5). If the channel doping concentration is assumed to be reasonably uniform across the wafer, the threshold voltage variation can be a good measure of the vertical channel width uniformity. Figure 5.29 shows a mapping of the threshold voltage of small TIVJFETs. The vertical channel width W_{CH} derived from the source mesa width measured at a few spots, is shown in the white boxes on Figure 5.29. The vertical channel width variation is in a good agreement with the measured threshold voltage variation. From the values of the threshold voltage it can be concluded that W_{CH} is reasonably uniform in most of the wafer area. The reasons for the variations in W_{CH}, is wafer thickness and photoresist thickness noniniformity, which create line size nonuniformity during photolithography.

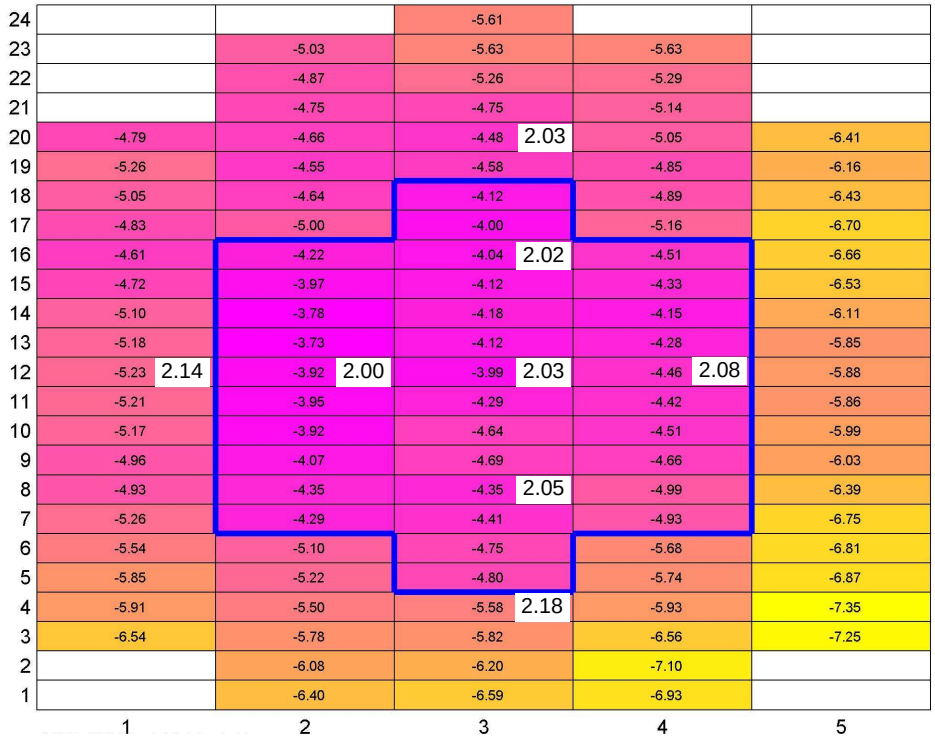


Figure 5.29 Small TIVJFET threshold voltage extracted from the linear parts of the I_D-V_{GS} curve, measured with V_{DS}=0.05V. The vertical channel width, derived from the source mesa width measured at a few spots, is shown in the white boxes.

The values of V_T for devices located very close to the wafer edge are noticably higher than V_T for the rest of the devices. This cannot be explained by a wider vertical channel for devices close to the wafer edge. The source line width, and hence W_{CH}, for devices very close to the edge of the wafer is in fact smaller, so V_T should also be smaller. The reason for this higher V_T for devices close to the wafer edge has to be a higher channel doping concentration at the wafer edge, compared to the rest of the wafer.

The variation of V_T is a measure of variation of the TIVJFET vertical channel width and also of the variation of termination guard ring spacing across the wafer. If we consider the distribution of the threshold voltage values across the wafer on Figure 5.29 and the distribution of the p-n diode blocking voltage V_B from Figure 5.22, we can see no correlation between them. This shows that the blocking voltage is not sensitive to the guard ring spacing nonuniformity across the wafer, which we will call a global nonuniformity. This proves the robustness of the termination design. The variation of the V_B observed for some devices on Figure 5.22 can be explained by the effect of wafer defects and by the existence of process related defects in the guard ring area that would create a local guard ring spacing dsitributuoin disruption.

CHAPTER 6. SUMMARY AND FUTURE WORK SUGGESTIONS

6.1. Summary

The advantages of 4H-SiC for switching power device applications are discussed. The advantages of unipolar power switches are discussed over the bipolar switches. The vertical JFET device was identified as an excellent candidate for high power, high temperature switching applications. Device designs for normally-off and normally-on unipolar switches with blocking voltages from 400V to 11kV are proposed, based on a pure vertical trenched and implanted structure. Different junction termination structures are designed and successfully implemented. A fabrication process is designed to achieve a simple and reliable self-aligned fabrication process. The fabrication challenges are discussed and ways to improve the process are identified. Three different devices were designed and fabricated.

The world's first normally-off high voltage 4H-SiC TIVJFET with a blocking voltage of 11kV was demonstrated, showing low specific on-resistance of 124mΩ.cm^2.

Normally-off and normally-on 4H-SiC HF-TIVJFET with blocking voltages up to 400V were demonstrated. 3.3A-397V normally-off capability was achieved for a single die, corresponding to a high power of 1310 W/die. This corresponds to a class B operation RF power of 164W for a single die. Cut-off frequency f_T= 0.9 to 1.5 GHz was reached.

In the 1200V class devices a normally-on 4H-SiC TIVJFET with guard ring termination and substantially simplified processing was also demonstrated. The highest blocking voltage achieved was 1562V with a specific on-resistance of 2.8mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V and a current gain of 1495. The lowest specific on resistance

achieved was 2.2mΩ.cm^2 at V_{DS}=0.5V and V_{GS}=2.5V with a current gain of 1454 and a blocking voltage of 1232V.

6.2. Future Work Suggestions

In order to improve performance of unipolar switching devices based on the TIVJFET structure a number of design and process improvements and refinements are possible.

6.2.1. Design Improvement

To improve device performance the device specific on-resistance and gate resistance need to be decreased.

6.2.1.1. Specific On-resistance Decrease

There are two factors that determine the on-resistance – the drift layer resistivity and the channel resistivity. The drift layer parameters are determined by the blocking voltage requirement and its resistivity will be decided by that. In order to decrease the channel resistivity the channel doping concentration needs to be increased and source line density needs to be increased at the expense of reduced gate trench width.

Channel doping concentration increase: Channel resistivity can be decreased by using an additional more highly doped epilayer for the device vertical channel. This will lead to some increase of wafer price but is justifiable in terms of gained performance. With increasing channel doping concentration the channel width will be decreasing, which will require a better process control to avoid channel width nonuniformity.

Source line density increase: Source line density can be increased by decreasing the gate trench width. In the current design the gate trench width is limited by the use of wet etching process to define the source mesa etching metal mask. If a dry etching process is used for the mask definition the source line density can be increased. A well-controlled

dry etching process for AlTi etching mask needs to be established, e.g. a chlorine based plasma etching.

6.2.1.1. Gate Resistance Decrease

Using a gate metal overlay is a good way to achieve lower gate resistance. The process used to define the gate overlay has a narrow process margin. To avoid potential problems with this processing step the device layout may be optimized. Another way to decrease the gate resistance is to decrease the gate ohmic contact resistance by improving the process.

Device layout improvement: To avoid potential problems with gate metal overlay definition the device layout may be optimized to include additional gate buses with thick metal to interconnect gate regions further away from the gate probing/wire-bonding pads. The length of the gate trench with relatively thin ohmic contact metal needs to be limited to a certain distance to ensure low total resistance.

6.2.2. Process Improvement

A number of process improvements and refinements can be done to improve device performance.

6.2.2.1. Source Mesa Definition

To establish a god control of the vertical channel width the fabrication process has to ensure source line-width uniformity, good vertical mesa profile and smooth mesa sidewall. The best way to achieve this would be to use dry etching method to define the source mesa etching mask. AlTi could still be used as an etching mask. The metal can be patterned by etching in chlorine plasma with a photo resist mask. This way the source line density can be increased by reducing the gate trench width and also a smooth mesa

sidewall can be achieved by having smoother etching mask edge. Plasma-etching conditions could be further refined to provide a virtually vertical mesa sidewall.

6.2.2.2. Gate Ohmic Contact

To reduce the gate ohmic contact resistance nickel silicide annealing conditions may be optimized. It is expected that lower annealing temperature to give a lower contact resistance to p-type. Hence the annealing of the gate and source ohmic contact can be divided into to separate steps using different temperatures.

6.2.2.2. Gate Trench Dielectric Fill

Gate trench oxide filling process by PECDV SiO_2 deposition and planarization ecth-back is a time consuming step that requires a tight control. One possible improvement is to use a chemical mechanical polishing to planarize the oxide in the trench. Another way to improve the process is to use spin-on glass to simplify the deposition process and improve planarization.

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CURRICULUM VITA

Petre Alexandrov

09/2001 – 10/2009	Ph.D. in Electrical and Computer Engineering Rutgers, The State University of New Jersey New Brunswick, New Jersey, USA
09/2000 – 10/2009	Senior Research Engineer United Silicon Carbide, Inc. New Brunswick, New Jersey, USA
09/1998 – 05/2001	M.S. in Electrical and Computer Engineering Rutgers, The State University of New Jersey New Brunswick, New Jersey, USA
05/1993 – 09/1998	Research Associate Institute of Solid State Physics, Bulgarian Academy of Sciences Sofia, Bulgaria
01/1989 – 05/1993	Semiconductor Test and Characterization Engineer Institute of Microelectronics Sofia, Bulgaria
09/1981 – 07/1986	M.S. in Engineering Physics, Sofia University, Sofia, Bulgaria

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