POWER DEVICES AND INTEGRATED CIRCUITS BASED ON 4H-SIC LATERAL JFETS

by

MING SU

A dissertation submitted to the Graduate School-New Brunswick

Rutgers, The State University of New Jersey

In partial fulfillment of the requirements for the degree of

Doctor of Philosophy

Graduate Program in

Electrical and Computer Engineering

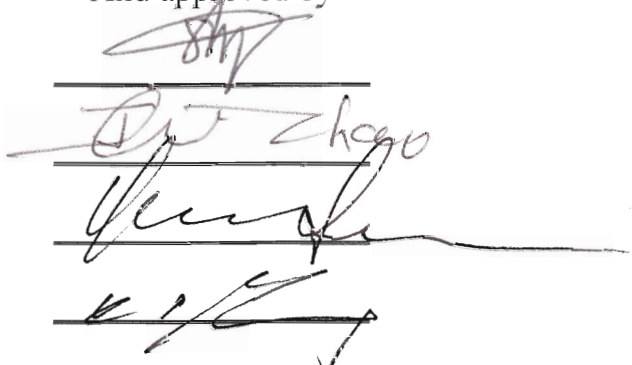
Written under the direction of

Professor Kuang Sheng

And the co-direction of

Professor Jian H. Zhao

And approved by



New Brunswick, New Jersey

May, 2010

ABSTRACT OF THE DISSERTATION

Power Devices and Integrated Circuits Based on 4H-SiC Lateral JFETs

By MING SU

Dissertation Director

Professor Kuang Sheng

Dissertation Co-director

Professor Jian H. Zhao

Silicon carbide (SiC) is a wide-bandgap semiconductor that has drawn significant research interest for the next-generation power electronics due to its superior electrical properties. Excellent device performance has been repeatedly demonstrated by SiC vertical power devices. However, for lateral power devices that offer the unique advantage of possible monolithic integration of a power electronics system-on-chip, the progress has been limited. This dissertation describes the 4H-SiC vertical-channel lateral JFET (VC-LJFET) technology that provides a suitable solution for power integration applications. Power devices based on this structure have a trenched-and-implanted vertical channel and a carefully designed lateral drift region, enabling normally-off operation with a high-voltage blocking capability. Low-voltage (LV) versions of VC-LJFET feature

nearly identical device structures with a reduced drift length, and can be readily fabricated on the same wafer with the power devices. Essential components for a power integrated circuit, such as gate drive buffers, can be thus implemented monolithically on the VC-LJFET technology platform.

This dissertation research starts with the process improvement investigation for the TI-JFET structure. Particularly, a novel ohmic contact scheme is developed using Ni to replace the troubling process in TI-VJFETs. The entire process flow of VC-LJFET is then designed and demonstrated in experiments, leading to the world's first demonstration of a normally-off lateral power JFET in SiC. As of today, power JFETs fabricated in this technology are still representing the best-performing lateral power transistors in SiC and silicon.

Based on the VC-LJFET structure, low-voltage circuits critical to the power integration applications are investigated. Gate drive buffer provides the interface between low-voltage control circuits and the power device, and is recognized as a key component for an integrated power electronics system. A thorough design, modeling and optimization work on the LJFET-based gate drive circuits is described. These buffer drivers using resistor or transistor loads will enable high-frequency switching of the power LJFETs at megahertz levels.

The results achieved in this research strongly suggest the feasibility of SiC power integration technologies in general, as well as the suitability of the SiC VC-LJFET platform for such applications in particular.

DEDICATION

To my parents and my fiancée

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my dissertation advisor, Prof. Kuang Sheng, and my co-advisor, Prof. Jian H. Zhao, for their excellent technical guidance, continuous support and encouragement throughout this dissertation research. I would also like to thank my dissertation committee members, Prof. Yicheng Lu of the Department of Electrical and Computer Engineering and Dr. Kin P. Cheung of National Institute of Standards and Technology (NIST), for their critical reading of this dissertation and valuable suggestions.

During the power IC technology development, my team partner, Dr. Yongxi Zhang and I worked closely with excellent discussion and collaboration efforts. His critical contribution on the RESURF enhancement of power VC-LJFET and the demonstration of the first power IC greatly enhanced the success of our project. I would also like to acknowledge Dr. Xueqing Li, Dr. Petre Alexandrov, Dr. Leonid Fursin of United Silicon Carbide, Inc for their help on TCAD simulation and assistance in clean-room fabrication processes. Additionally, the valuable discussion and cooperation from all fellow students in SiCLAB and Power Lab are in many ways indispensible for my research accomplishments. I wish to extend my gratitude to all my current and past colleagues. Finally, I would like to acknowledge the financial support provided by DARPA/Air Force under the Robust Integrated Power Electronics initiative, and Army TARDEC under the Reliable 4H-SiC MOSFET project.

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CHAPTER 1 INTRODUCTION

1.1 Power Semiconductor Devices and Their Applications

The modern industry and life is increasingly dependent upon the use of energy in the electrical form. After the replacement of vacuum tubes by solid-state devices in the last century, the regulation of electrical power generation, distribution and conversion is now dominated by the applications of power electronics systems based on semiconductor switches. [1] In these systems, power semiconductor devices play a fundamental and critical role. An example called full H-bridge inverter circuit shown in Fig. 1-1 shows how power devices are usually applied in power electronics systems. [2] Power diodes D1~D4 and power transistors S1~S4 are the key components of the circuit. By alternative turn-on of S1/S3 and S2/S4, the DC voltage supply V_d is converted to an AC power source in respect to the Load.

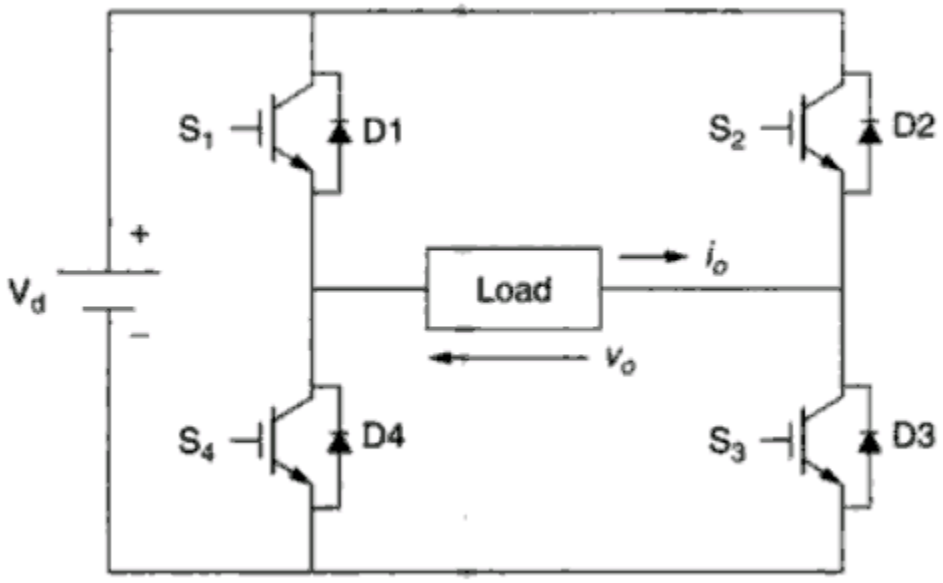


Fig. 1-1 Schematic of a single-phase DC-to-AC power converter

Power electronics circuits are not only capable of power conversion between AC and DC forms; they are also used to modify other properties of the electrical power like voltages and frequencies. Detailed discussion on this topic is beyond this dissertation and may be found in textbooks such as [3].

Depending the specific applications, power devices can be classified in terms of their current and voltage handling requirements as in Fig. 1-2. [1] Typically, a specific power device structure is only suitable for a certain voltage or power range of application. The high-power end of this chart is dominated by power thyristors. In the medium voltage range of 300 to 3kV, insulated gate bipolar gate bipolar transistors (IGBT) are usually an optimal choice with significant current handling capability. Power MOSFETs are normally used at lower voltage ratings for higher frequency applications. [1]

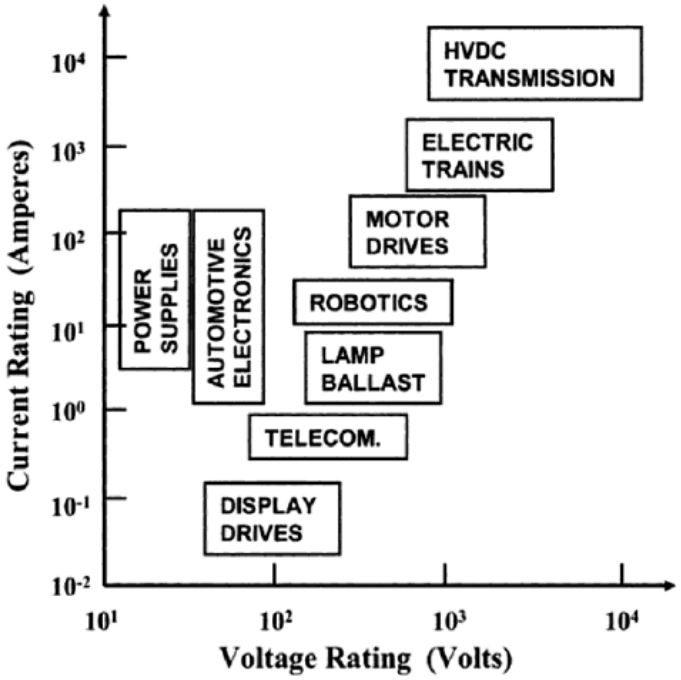
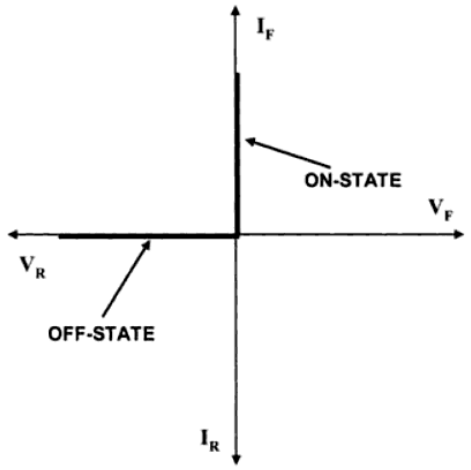
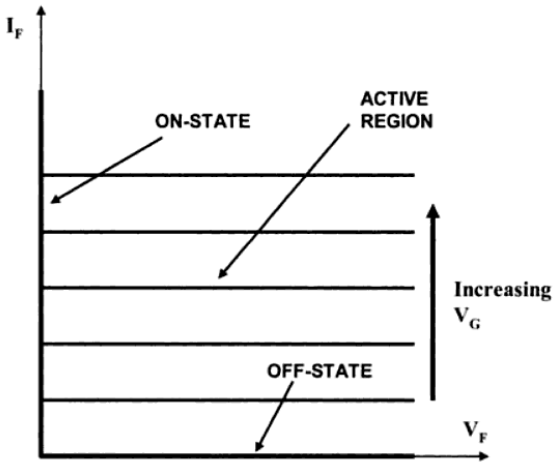


Fig. 1-2 System ratings for power devices

In general, power electronics circuits require both rectifiers to control the direction of current flow and power switches to regulate the duration of current flow. [1] Apparently, an ideal device for power switching applications should be able to stand high voltage while in the off-state, and conduct high current with minimal power loss at on-state, as in Fig. 1-3. The ideal power devices never carry current and voltage at the same time, and therefore will not consume power themselves.



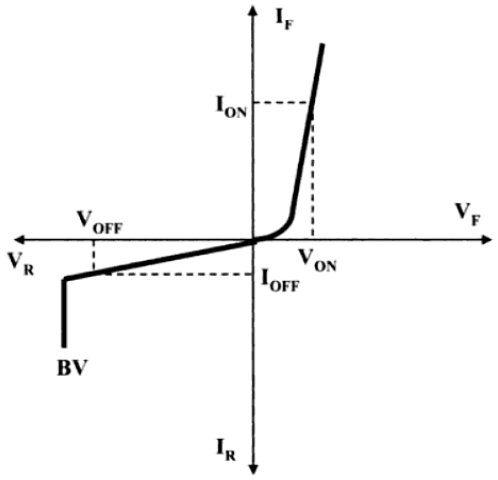
(a) Ideal power rectifier



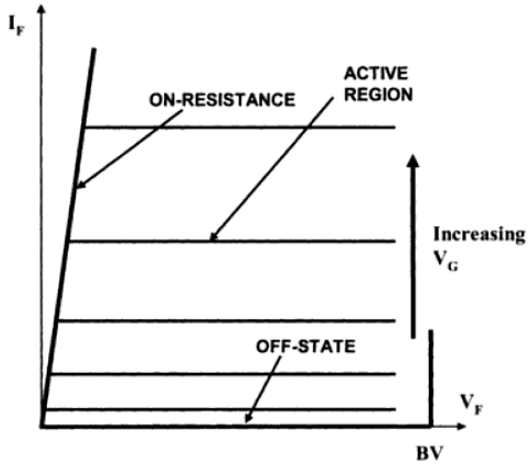
(b) Ideal power switching transistor

Fig. 1-3 Characteristics of ideal power devices

In reality, all devices have non-zero on-state resistances and non-zero off-state leakage current. And when the voltage applied reaches a maximum allowable value, the device will undergo avalanche breakdown, as in Fig. 1-4.



(a) Power rectifier



(b) Power switching transistor

Fig. 1-4 Characteristics of typical power devices

Power semiconductor devices can be constructed in bipolar or unipolar modes depending on whether minority charge carriers are involved in the on-state current

conduction. They are both designed to include a drift region in order to support electrical field and hence the blocking voltage in the off-state. For conventional unipolar devices made from a certain semiconductor material, the more voltage the drift region can support through doping and thickness adjustments, the more resistance per unit area it will contribute in the on-state current conduction. The analytical equation describing this tradeoff is shown as (1.1). [1, 4]

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^{\ 3}} \tag{1.1}$$

where $R_{on\text{-}ideal}$ is the specific on-resistance of the drift layer, BV is the breakdown voltage of the power device, ε_s is the dielectric constant of the semiconductor, μ_n is the electron mobility and E_c is the semiconductor's critical electric field at the onset of breakdown.

1.2 Material Properties and Advantages of 4H-SiC

In Equation (1.1), although the BV^2/R ratio stays as constant for a given semiconductor, we can however drastically increase its value by selecting different semiconductors, i.e. different values for $\varepsilon_s \mu_n E_c^3$. Today's power device market is still dominated by silicon components, which is certainly the most mature and commercially successful semiconductor to date. However, silicon's material properties are inferior to many other semiconductors in terms of $\varepsilon_s \mu_n E_c^3$, or *Baliga's figure-of-merit (BFOM) for power devices*. Thanks to the third power of critical electric field in the BFOM expression, high values of this merit are typically found in wide bandgap semiconductors,

including SiC, GaN and diamond. Table 1-1 compares the material properties of these semiconductors against silicon. The BFOM values for all materials in this table have been standardized to that of silicon.

Table 1-1 Properties of silicon and wide bandgap semiconductors [5~6]

Material	E_g (eV)	ε_r	μ_n ($cm^2/V{\cdot}s$)	E_c (MV/cm)	V_{sat} (10^7 cm/s)	λ (W/cm·K)	*BFOM*
Si	1.1	11.8	1350	0.3	1.0	1.5	1
4H-SiC	3.26	10	720	3.0	2.0	4.9	450
GaN	3.39	9.0	900	3.3	2.5	1.3	676
Diamond	5.45	5.5	1900	5.6	2.7	20	4260

Notes: E_g – bandgap,ε_r – relative dielectric constant, μ_n- electron mobility, E_c – critical electric field, V_{sat} – electron saturation velocity, λ – thermal conductivity

From this comparison, we can see that popular wide bandgap semiconductors are at least hundreds of times better than silicon for power device purposes. As silicon devices are approaching its theoretical limits, wide bandgap semiconductors are naturally suitable for the next generation power electronics applications. Even though they are not yet challenging silicon's existing dominance in this market, their increasingly maturing technology is expected to lead to great commercialization success in the years to come.

Among these wide bandgap semiconductors, diamond is often cited as the ultimate semiconductor [7], which is readily explainable by the BFOM criteria. However, the extreme difficulties in single crystal growth and shallow doping have kept diamond from

successful electronics development for many years. GaN, on the other hand, has been a notable alternative to SiC and is under active research by many teams worldwide. However, the difficulty in GaN native substrate technology and the high defect density in GaN epilayers still invite serious concerns and questioning, making it less successful than SiC for power device applications. In short, although SiC does not possess the highest BFOM in the group, it is by far the most mature and commercially available wide bandgap material compared to its alternatives. In addition, 4H-SiC, the most commercially available polytype of SiC, offers the more favorable properties compared to others, such as 3C-SiC and 6H-SiC. Today's SiC material suppliers like Cree are already offering zero-micropipe density 4H-SiC wafers up to 100mm in diameter. Given the vastly improved material technology as of today and the superior properties of SiC over silicon, we strongly believe that this is the right time to engage in the development of novel power device and integrated circuit technologies on 4H-SiC.

1.3 Process Technologies for SiC

While SiC has been identified as a very promising material for power electronics applications, the high-performance devices based on SiC cannot become true unless a broad range of device fabrication technology has been developed for this material. During the last twenty years, a substantial amount of efforts have been spent on the research and experimental development of SiC processing technologies. Fortunately, most of the general microelectronic techniques developed by the silicon industry can be

directly applied to SiC device fabrication with little or minor modification. These procedures include lithography, metal and dielectric deposition and patterning, thermal oxidation, device packaging and etc. However, processing of SiC does have some important differences from Si technology that need to be addressed specifically. This section briefly reviews and compares the key procedures and techniques used in Si and SiC device fabrication.

Thermal Oxidation

Thermal oxidation procedure is required for the fabrication of MOSFETs and other MOS-controlled devices. The technology and procedure used for silicon and SiC oxidation are not significantly different. However, SiC has a much slower rate of oxide growth compared to Si at the same temperature and conditions, as shown in Fig. 1-5. In addition, 4H-SiC MOSFETs fabricated using simple oxidation procedures suffer from poor oxide quality and low inversion channel mobility. [8]

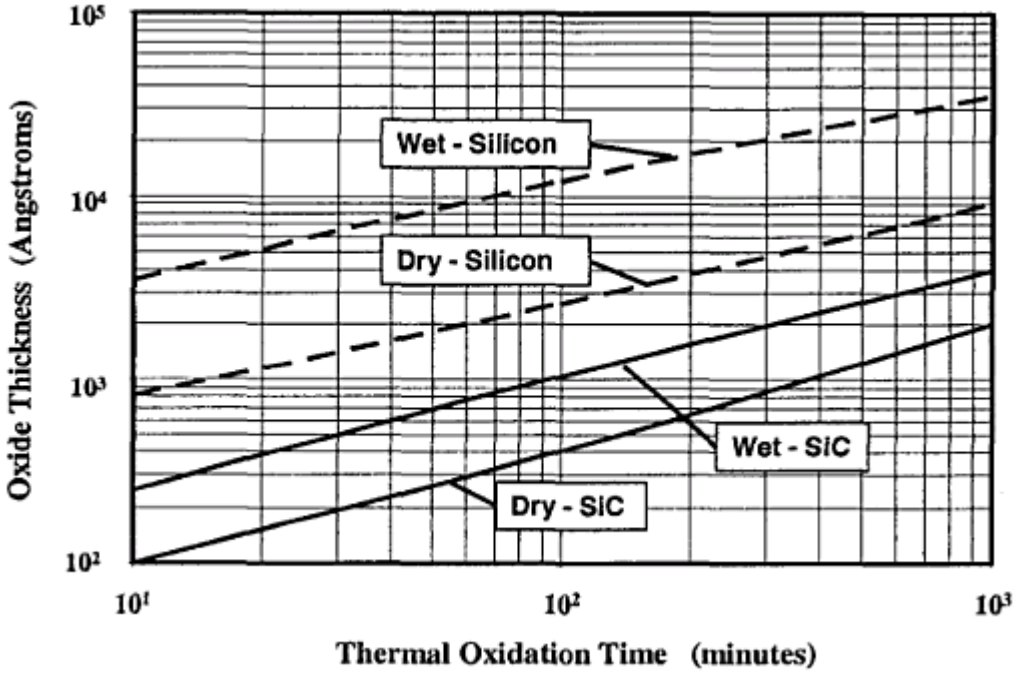


Fig. 1-5 Comparison of thermal oxidation of SiC with silicon at 1200^{o}C

SiC power MOSFETs have been a major research interest for years. Many teams have developed specialized oxidation and annealing techniques that may result in improved channel mobility, such as annealing in nitric oxide ambient. [9] However, unlike the mature Si oxidation technology, in the meantime, growing high-quality oxide on 4H-SiC is still a major challenge and an active area of scientific research.

Diffusion

One of the major differences in Si and SiC technology lies in the applicability of impurity atoms diffusion. In Si VLSI processing, diffusion can be used to form bases, emitters and resistors in bipolar devices. It can also form source and drain regions, and

dope polysilicon in MOS devices. [10] In addition, diffusion occurs when high-temperature annealing is used to activate dopants from ion implantation, which can drive in the impurities and result in dopant redistribution. Without high-resolution lithography, submicron DMOSFET channels can be fabricated by diffusing dopants from the same window to form p-base and n+ source regions based on their different junction depths. [8]

In SiC, however, the diffusion coefficients of dopants are very small even at relatively high temperatures, making it impractical to utilize the traditional process of diffusion in silicon VLSI technology. [11] In general, doping of SiC can either be accomplished *in situ* during the epitaxial layer growth, or through ion implantation.

Ion Implantation and Activation

Ion implantation technology is widely used in silicon device fabrication as it allows precise control of the number of implanted dopant atoms. Upon annealing, precise dopant concentrations between 10^{14} to 10^{21} atoms/cm^3 in silicon can be obtained. [10] As a Group IV semiconductor, n-type doping of silicon can be accomplished by introducing Group V elements such as phosphorus and arsenic. P-type doping for silicon can be done with boron, a Group III element. The electrical activation of these dopants is usually achieved by a 600^{o}C ~1000^{o}C thermal annealing.

Compared to silicon, ion implantation technique for the selective doping in SiC devices is even more indispensable, because of the low diffusion coefficient limitation for

SiC discussed above. In doping SiC, either Si or C atoms in the crystal structure has to be replaced by the impurity atoms. Because Si and C are both Group IV elements, just like silicon itself, the principles of using Group V donors and Group III acceptors for Si and SiC is the same. The electrical activation of these dopants, however, will require substantially higher annealing temperature for SiC than for silicon, typically at least 1500^{o}C~1600^{o}C. The high temperature needed for dopant activation and lattice damage removal is yet limited by the onset of SiC surface damage by Si sublimation or evaporation at above 1600^{o}C. [8, 12]

Another difference for silicon and SiC ion implantation is the higher ion energies required for implanting into SiC due to the higher density of SiC than Si. [12] While 3 to 500keV energy can implant boron, phosphorus or arsenic dopants into silicon by 100A to 1μm below the surface [10], creating μm-range implant depth in SiC often require energies in the MeV range. The masking layer for SiC implantation is therefore considerably thicker or denser than needed for an equivalent depth profile in silicon. [12]

The exact implant species commonly used for doping SiC are also not necessarily the same as for silicon. For n-type doping, the most popular elements are nitrogen and phosphorus. The nitrogen ions predominantly occupy C sublattice sites, and the phosphorus replaces Si atoms in SiC. [12] The low atomic mass of nitrogen results in a versatile ion range and low lattice damage, while phosphorus has the advantage of high solubility in SiC leading to lower sheet resistance. [12, 13] As for acceptor doping, the most popular implant species are boron and aluminum. Boron has low atomic mass

compared to aluminum, but aluminum possesses more significant advantages, such as lower carrier ionization energy (190meV for Al vs 285meV for B in 4H-SiC [14, 15]), higher solubility in SiC [16] and easier implant activation (~1600^{o}C annealing for Al vs ~1700^{o}C for B [17]).

In summary, while a significant amount of research has been published on the ion implantation and activation annealing topics for SiC, the commonly accepted procedures for selectively doping SiC are implanting nitrogen ions as n-type donors, and aluminum ions as p-type acceptors, followed by an activation annealing of these dopants under 1600^{o}C. This routine has been adopted for the device fabrication efforts in this dissertation research.

Dry Etching

Plasma-assisted etching or dry etching is commonly used in silicon VLSI processing because of its very-high-fidelity transfer of patterns of the masking layer. [10] These techniques are required for Si and SiC device fabrication to create vertical mesas and trenches, make trench isolation, and form other shapes or structures.

The earliest application of plasma etching in silicon ICs is the stripping of photoresists by oxygen plasma. [18] Afterwards, plasma etching of silicon and silicon nitride was developed, using gas mixtures of CF_4 and O_2. [10] These efforts marked the beginning of large-scale research and development activities on plasma etching techniques in the silicon IC industry.

Similarly for SiC, dry etching techniques have been intensively investigated since the 1990s. It has been established that reactive ion etching (RIE) or inductively coupled plasma (ICP) etching can be used to transfer mask patterns to SiC, in CF_4 [19], SF_6 [20] or chlorine-based [21] gas chemistries. In our device fabrication practice, CF_4/O_2-based etching of 4H-SiC is used due to its easier handling and reliability. The etching conditions for different shaped profiles, as well as for SiO_2 and silicon nitride layers are all individually optimized to obtain the best etching results.

Ohmic Contacts

Ohmic contacts are non-rectifying metal-to-semiconductor connections that allow current transport in both directions with minimal voltage drop. They are necessary in the fabrication of semiconductor devices to form good electrode access. Aluminum has traditionally served as the metal of choice for both n-type and p-type ohmic contacts to silicon devices and ICs. [10]

When metal and semiconductor make intimate contact, a Schottky barrier is formed, the height of which is given by:

$$\text{n-type:}\quad \phi_B = \phi_M - \chi_S \tag{1.2}$$

$$\text{p-type:}\quad \phi_B = E_G - (\phi_M - \chi_S) \tag{1.3}$$

where ϕ_M is the work function of the metal, χ_S is the electron affinity of the semiconductor, and E_G is the semiconductor band gap. The current-conducting

quality of the metal-semiconductor contact is described by the specific contact resistance R_c:

$$R_c = \left(\frac{\partial J}{\partial V} \right)^{-1} \text{ at } V=0 \tag{1.4}$$

For low doping semiconductors, the charge transport between metal and semiconductor is dominated by thermionic emissions over the potential barrier, which results in a specific contact resistance given by [22]:

$$R_c = \frac{k}{qA^* T} \exp\left(\frac{q\phi_B}{kT} \right) \tag{1.5}$$

where A* is the Richardson constant, k is the Boltzmann constant, q is the electric charge of carrier, T is the absolute temperature, and ϕ_B is the barrier height.

At higher doping levels, carrier tunneling through the potential barrier becomes important. And the specific contact resistance is mainly determined by thermionic field emission (TFE), and is given by [22]:

$$R_c \propto \exp\left[\frac{4\pi\sqrt{m^* \varepsilon_s}}{h} \frac{\phi_B}{\sqrt{N_D}} \right] \tag{1.6}$$

where ε_s is the dielectric permittivity of the semiconductor, m* is the effective mass of the charge carrier, h is Planck's constant, ϕ_B is the barrier height, and N_D is the doping concentration.

Equation (1.5) and (1.6) indicate that a low Schottky barrier height is desirable for ohmic contact formation. However, in the search for good ohmic contact metal for SiC, the classic theory based on Schottky barrier height has not been successful

in predicting the best material of choice. [23] In fact, the most widely accepted metal for n-type SiC ohmic contact, Ni, and the metal for p-type ohmic contact, Al, are both non-ideal choices in terms of their work functions. Hence the development of SiC ohmic contact technology is largely based on experimental trial and error. Explanations for experimentally discovered ohmic contact behaviors are given in literature by many research teams, but a decisive consensus is usually yet to be reached.

In the first part of this Dissertation research, a novel ohmic contact scheme for SiC JFETs is developed, which is presented in Chapter 2. Further discussion on the physics mechanism of forming SiC ohmic contacts using Ni will be given based on our observations during the technology development.

1.4 SiC JFETs and Alternatives

Today, the major types of power transistors under research and improvement include bipolor junction transistors (BJTs), metal-oxide-semiconductor field effect transistors (MOSFETs) and junction field effect transistors (JFETs). [24]

SiC bipolar devices, such as BJTs, have the advantage of conductivity modulation as the minority carriers inject into the collector in on-state condition. [24] In many ways, BJTs are easier to fabricate than FETs, and are free from certain challenging issues, particularly with the gate oxides of MOSFETs. Many teams have been able to report low specific on-resistance, high-voltage BJTs. However, BJTs are current-controlled devices,

and have their limitations. High base drive current is required compared to voltage-controlled FETs. This can account for substantial power dissipation in the device, and require complex and expensive input drive circuitry. Teams working on SiC BJTs are typically making concentrated efforts to maximize the current gain (β) of these devices. [25, 26]

JFETs and MOSFETs, on the other hand, are voltage-controlled, unipolar transistors that are low in gate drive current, and more advantageous for fast switching applications. The attractiveness of SiC MOSFETs is obvious, considering the success of silicon MOS technologies and the fact that SiC is the only known wide bandgap semiconductor that can be thermally oxidized to form native SiO_2. However, with many teams making efforts in this area, several major problems still remain and limit its near-term applications, including low inversion layer electron mobility and poor gate oxide reliability. [24, 27] SiC power JFETs, on the other hand, offer a very promising alternative to SiC power MOSFETs by avoiding the trouble-making SiC-SiO_2 material interfaces. The first normally-on high-performance SiC power JFETs were reported in 1999 [28]. Afterwards, significant progress has been achieved in this area. Normally-off power JFETs with V_B^2/R_{ON} FOMs up to 830MW/cm^2 were reported [29, 30]. While the theoretical V_B^2/R_{ON}-FOM limit for 4H-SiC power devices at about 4000 MW/cm^2 still leaves room for further improvements, one should note that the performance demonstrated by SiC power JFETs already far exceeds their silicon counterparts. [24]

1.5 Lateral Power Devices towards SiC Power IC

In silicon power electronics, the ability to integrate high voltage power device structures with low voltage CMOS and bipolar devices has enabled the smart power technology. [31] Power semiconductor technology on discrete devices was explored before the success of integrated circuits. Over the years before the invention of power MOSFETs, process technology for discrete power devices was significantly different from that used for silicon integrated circuits. This situation changed after the introduction of power MOSFETs and MOS/bipolar devices in the 1970s and 1980s, resulting in a desirable process compatibility of silicon power devices with the VLSI technology. The advantages of power integration are reflected in lower cost, improved reliability, compactness in weight and space, as well as reduced electromagnetic interferences. [32, 33] The reduction of parasitic circuit components in monolithically integrated power electronics systems is especially attractive for high-frequency switching operations.

In a monolithic power integration technology, isolation between different devices is a key issue that needs to be addressed. For this reason, lateral power devices are significantly more suitable for power IC applications. As the example in Fig. 1-6, electrical isolation of lateral devices through reverse-biased p-n junctions can be readily accomplished. [34]

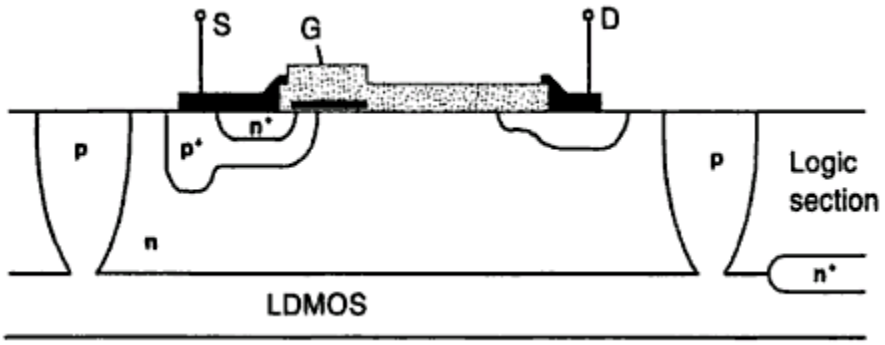


Fig. 1-6 LDMOS-based power IC with junction isolation

In comparison, vertical power devices do not offer the convenience of monolithic integration. Traditional vertical power transistors use the semiconductor substrate as the drain or collector electrode, which is shared by all such structures on the same chip. Isolating multiple vertical power devices on the same chip is not impossible, but requires much more complicated process and costs than the lateral devices scenario. An example of using multiple vertical power devices on a power IC is illustrated in Fig. 1-7, where all electrodes are on the top surface, and isolation is accomplished by a dielectric layer. [34]

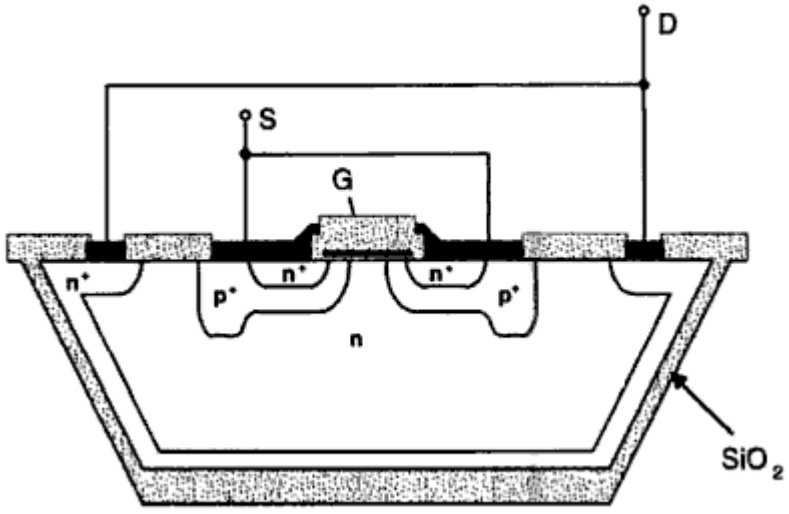


Fig. 1-7 A structure for monolithic integration of multiple VDMOS devices

It is worthwhile to note that, while lateral power devices offer the unique advantages for power integration and hence high-frequency switching applications, they do have limitations. Because of the need of a lateral drift region for voltage blocking purpose, the current packing density of these devices is smaller than the similar vertical structures. Therefore they are practical only for handling the switching of low to medium levels of power. When high power switching is needed, vertical power devices become necessary or preferred.

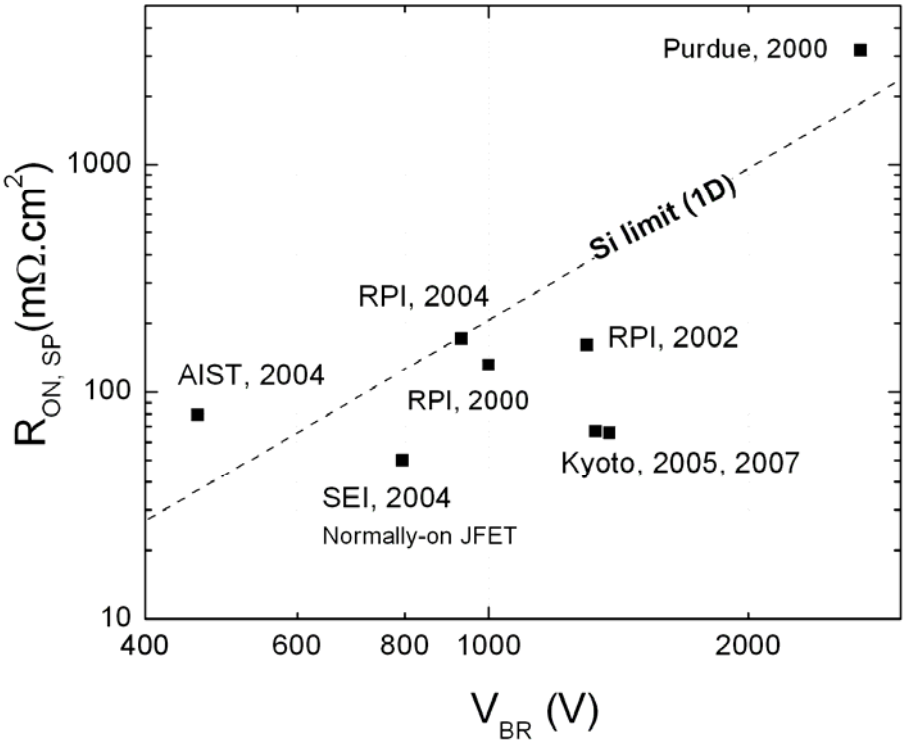


Fig. 1-8 Specific on-resistances versus breakdown voltages of state-of-the-art SiC lateral power devices, excluding recent results from Rutgers SiCLAB

In SiC, vertical power JFETs, MOSFETs and BJTs have been well investigated by many teams worldwide. However, lateral versions of these power transistors for power IC applications are not as frequently reported. A performance summary of SiC lateral power JFETs (SEI, 2004) and MOSFETs (all others) published to date is shown in Fig. 1-8, excluding results from this dissertation research and related work at Rutgers SiCLAB.

SiC power integration based on a lateral device platform is promising and is believed to be able to challenge silicon's smart power technology in the future thanks to the material property advantage of SiC over silicon discussed earlier. The smart power technology consists of three different modules and each of them needs to be addressed before a practical integrated power electronics system can be realized. Fig. 1-9 [31] gives an overview of the functional elements and their implementation.

The key component of the smart power technology is the power control module, which handles high voltage and/or high current and carries the uniqueness of a power electronics system in comparison to conventional VLSI circuits. In the research efforts towards SiC power IC, lateral power devices and their drive circuits made by a fully compatible fabrication technology are indispensible. This dissertation research is hence originated upon the excellent opportunity in SiC power integration technology, and will address the issues on the development of SiC power control components using the 4H-SiC lateral JFET platform.

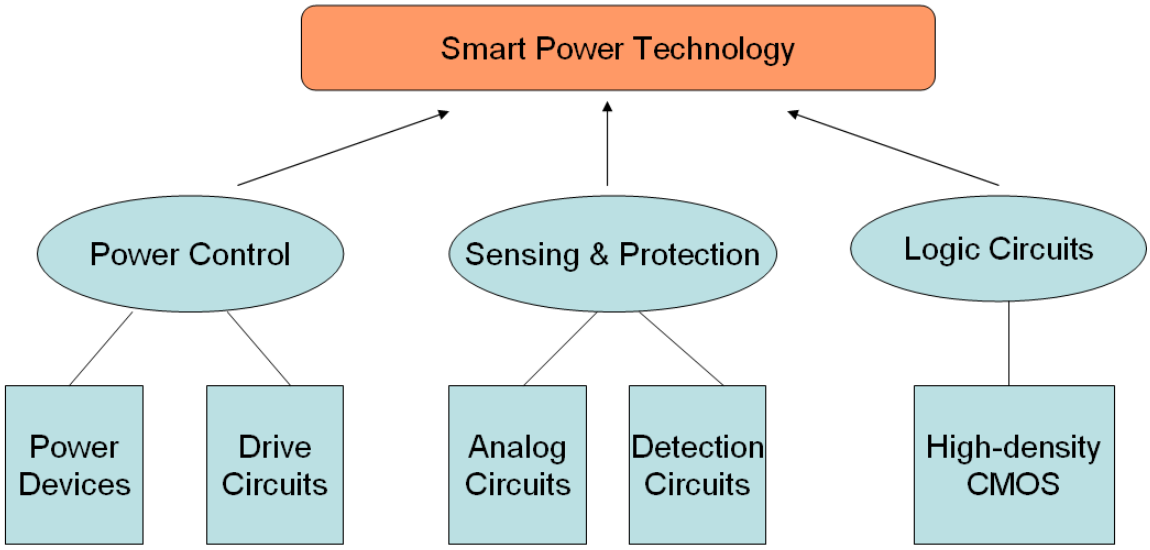


Fig. 1-9 Overview of the smart power technology of silicon

1.6 Outline of This Dissertation Research

The trenched-and-implanted vertical JFET (TI-VJFET) technology in 4H-SiC has been developed in Rutgers University and reported by Kiyoshi Tone and co-workers since 2002. [35] In this dissertation research on 4H-SiC lateral power JFETs and ICs, many device process procedures have been adapted from the accumulated fabrication knowledge and experience on TI-VJFETs. In spite of the TI-VJFET tradition available to our advantage, a number of challenges and original research work have to be addressed in this dissertation, including:

(1) Review the established process flow of TI-VJFETs and identify procedures that are not optimized, efficient or robust. Explore new ideas and develop novel process steps to facilitate the fabrication of lateral or vertical JFETs.

(2) Design and optimize the SiC lateral power JFET structure based on consideration of the practical facility capability at Rutgers MERL laboratory.

(3) Design the process flow of SiC lateral JFETs, confirm the process and device design experimentally by a demonstration of high-voltage, low specific-on-resistance lateral power JFETs.

(4) Investigate and design low-voltage gate drive circuits for the power JFETs based on a monolithically compatible technology. Perform modeling work and computer simulation on the high-frequency switching of the power JFET driven by the integrated gate buffer circuits. Explore and compare different options and circuit configurations for the buffer driver. Analyze the functionality of the power IC against process and wafer variations, as well as temperature conditions.

(5) Implement simulated gate buffer drivers on photomask level for the experimental confirmation of the design concepts.

In the following chapters, the above issues and challenges will be further discussed. And the results and knowledge gained through this research work will be presented.

Specifically, Chapter 2 addresses the ohmic contact formation challenge in the TI-VJFET process. A novel procedure featuring self-aligned Ni contact for the source and gate electrodes will be developed for TI-VJFETs and lateral JFETs.

Chapter 3 presents the detailed device design and process flow for lateral power JFETs in 4H-SiC. This chapter reports the first successful experimental demonstration of a normally-off power lateral JFETs in SiC.

Chapter 4 focuses on the low-voltage driver part of the SiC power IC technology. Modeling and simulation of the super buffer drivers for power LJFETs are presented, along with discussions on design windows, different circuit topologies, possible experimental uncertainties, and operation at elevated temperature. The photomask design and wafer fabrication consideration are also reviewed.

Chapter 5 summarizes the achievements in this research and the knowledge gained through the technology development. A discussion on the remaining challenges and suggestion for future work are given for the reader's reference.

CHAPTER 2 INVESTIGATION OF OHMIC CONTACT FORMATION SCHEME TO 4H-SiC VERTICAL-CHANNEL JFETS

2.1 Challenges and Issues in Existing Process Technology of TI-VJFETs

The proposed 4H-SiC VC-LJFET concept originated from the fabrication experiences of trenched-and-implanted vertical JFETs (TI-VJFETs) at SiCLAB, Rutgers University. The TI-VJFET itself has several key structural advantages. Particularly, the structure requires no epitaxial regrowth, features a simple unit-cell design and is proven to provide normally-off operation with a high on-state current density. [30, 35]

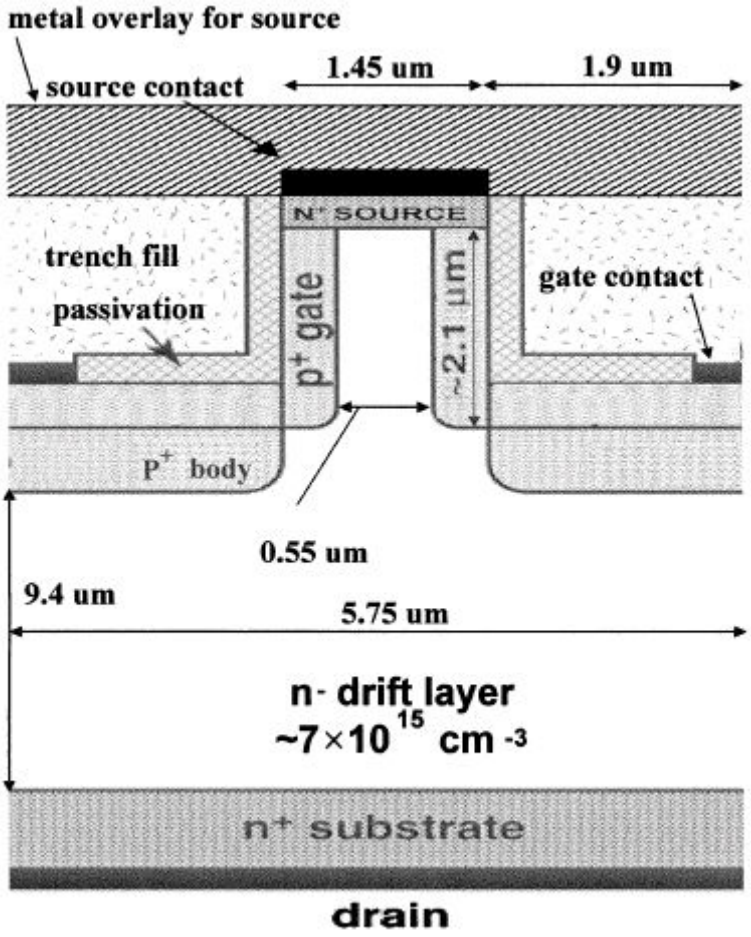


Fig. 2-1 Cross-sectional view of the 4H-SiC normally-off TI-VJFET [30]

Fig. 2-1 shows the cross-sectional view of a normally-off TI-VJFET unit cell. The source mesas feature double-sided (gate) aluminum implantation, leaving a narrow vertical channel with opening Wvc=0.55μm in Fig. 2-1. This vertical channel is depleted by the sidewall implants under zero-gate-bias condition, making the transistor normally off. By converting this structure into a lateral JFET device, the bottom drain contact is placed on the top surface, as in Fig. 2-2.

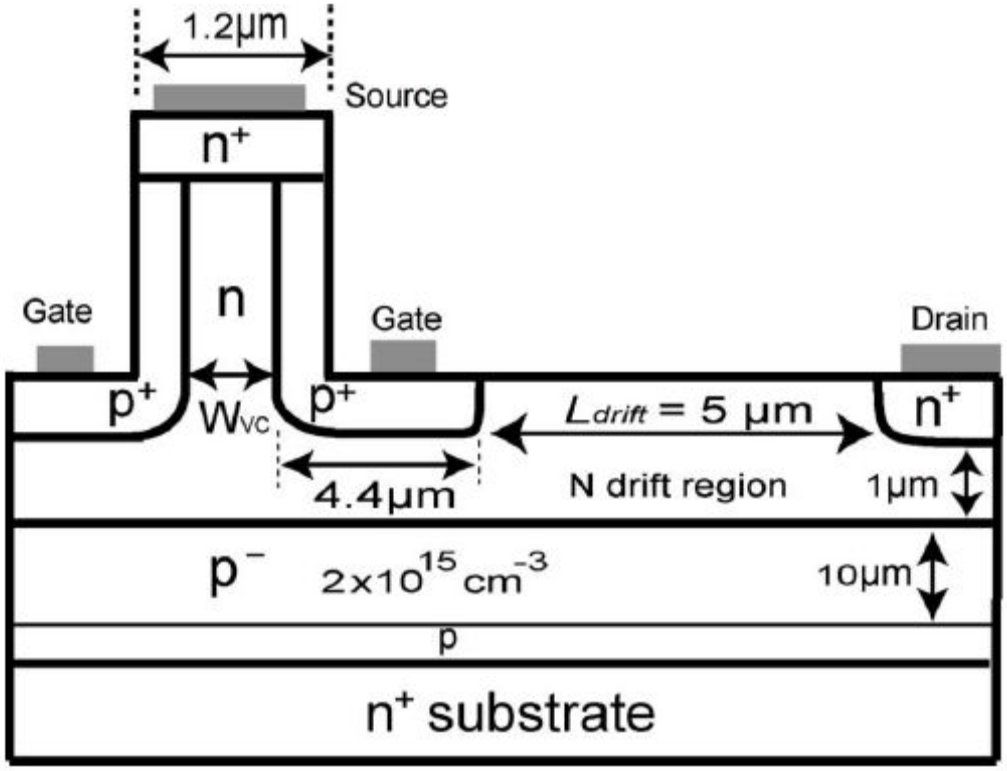


Fig. 2-2 Cross-sectional view of a 4H-SiC normally-off VC-LJFET [36]

Thanks to the structural similarity between the VC-LJFET and TI-VJFET, many of the established TI-VJFET fabrication process and techniques may be applied to the VC-LJFET. However, the original process flow created by Dr. Kiyoshi Tone [35] includes some

complicated and unreliable techniques, making the devices prone to low processing yield and other problems. An especially troubling procedure was the ohmic contact formation. From the mesa geometry shown in Fig. 2-1, it is easy to see that the key challenge in forming source and gate ohmic contacts lies in how to avoid shorting between them through sidewall metallic residues. This will be increasingly difficult if the width of the gate trenches between two source mesas is further shrunk to enhance the device's current packing density. In Kiyoshi's established process, a photoresist layer is first coated on the wafer, which undergoes ICP etch-back to expose source mesa tops. A Ni metal layer is then sputtered for source contacts, patterned by the lift-off procedure from the planarized photoresist. Then an additional critical lithography for gate metal patterning is needed, followed by gate metal Ti/TiN deposition and lift-off. This complicated procedure not only takes substantial time and efforts, but also significantly affects device yield. Defining the gate contact by lithography at the μm-scale is also inviting problems. This exact issue has been recognized by Dr. Yuzhu Li in his Ph. D. dissertation on his continued work in SiC TI-VJFETs. A slightly revised approach was proposed by Dr. Li, which defines the gate contacts by wet etching the sputtered metal layer after a photoresist planarization and etch-back trick. [37] This approach does not require fine lithography, but it remains questionable in that the sidewall metal residue removal is really dependent on the photoresist profile and the tiny air gap between the processed photoresist and the mesa sidewalls, which varies across the wafer and is very difficult to control by the process person. In short, although different ohmic contact schemes for the TI-VJFET structure

have been tried before, a robust approach for simple and reliable application is still to be found. To overcome this problem in our development of vertical-channel lateral JFET (VC-LJFET), a substantial change in the ohmic contact formation technique needs to be investigated. The new process to be developed should be simple, reliable, self-aligned and practical for the fabrication of vertical and lateral TI-JFETs.

2.2 Experimental Development of a Self-aligned Ni Contact Process

After extensive experimental trial and error, we developed a novel process using Ni as the contact metal for both n-type source and p-type gate ohmic contacts in the TI-JFET structures. The use of Ni for n-type ohmic contact to SiC is widely recognized and used. For p-type SiC, Ni ohmic contact was first reported by Leonid Fursin *et al.* in 2001. By eliminating the need for separate metal materials for the source and gate contacts, the metal deposition is consolidated into one single step. The key issue to be solved now is how to isolate the two contacts in a self-aligned manner.

We first tried to separate the as-deposited the source and gate metal by targeted wet etching techniques on the sidewall, which failed to produce any meaningful and usable recipe due to metal peeling-off or persistent shorting problems. After these failures, we decided to try an alternative method by performing the ohmic contact annealing prior to the removal of gate-source shorting path. This idea is feasible as long as we can define a layer of thermally stable thin film on the mesa sidewalls that blocks the reaction between Ni and SiC at the annealing temperature. In this scheme, Ni reaction with SiC forms

silicide in the source and gate contact regions. After annealing, the selective removal of sidewall Ni in the presence of Ni silicide is not difficult because commonly used Ni etchants do not appear to substantially attack Ni silicide. The material choices for the sidewall blocking layer that we considered include PECVD silicon dioxide and silicon nitride. However, we quickly found that PECVD silicon nitride cannot serve the purpose because it reacts with Ni and form irremovable residues after annealing at high temperatures. SiO_2, on the other hand, does prevent Ni from chemical reactions at the annealing temperatures. A usable recipe is soon developed based on this idea, and is illustrated in Fig. 2-3.

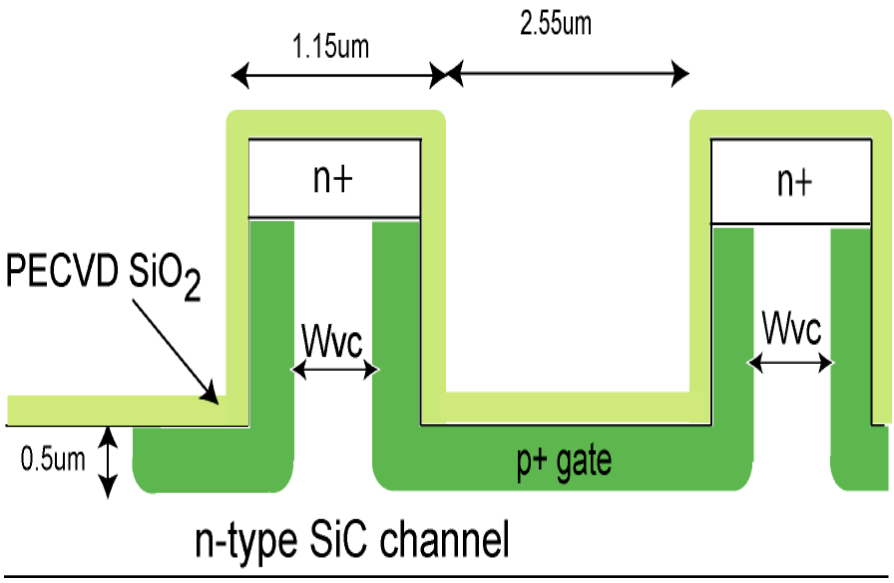


Fig. 2-3 (a) PECVD oxide deposition

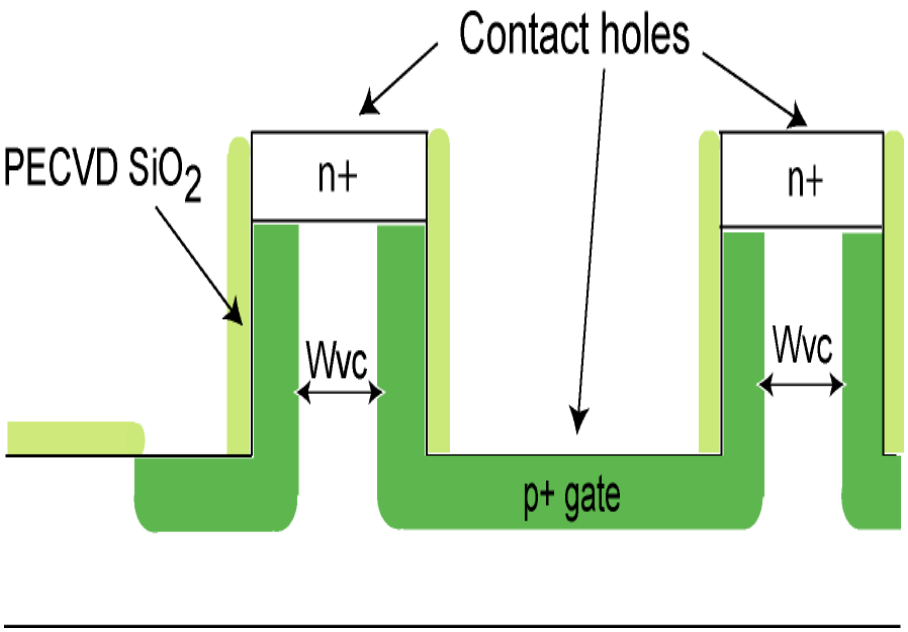


Fig. 2-3 (b) Contact hole opening by ICP etching

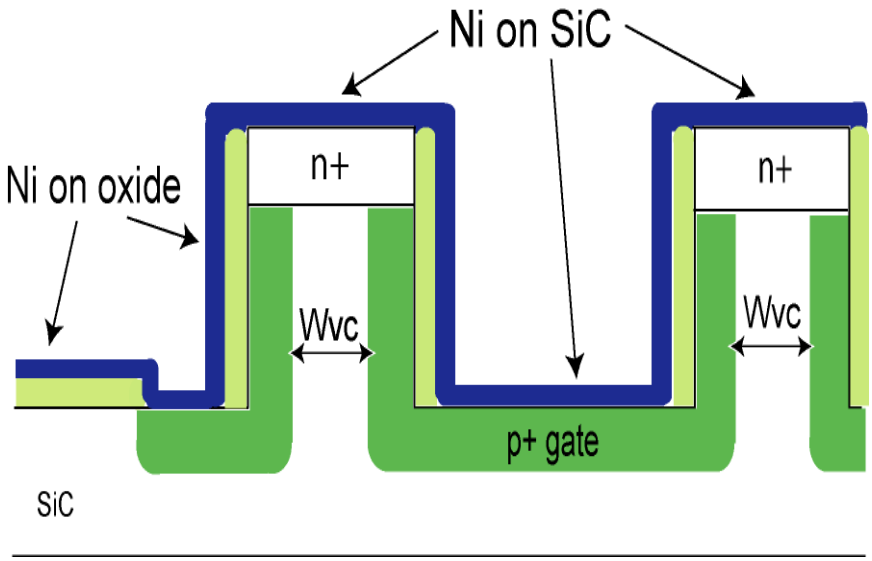


Fig. 2-3 (c) Ni deposition

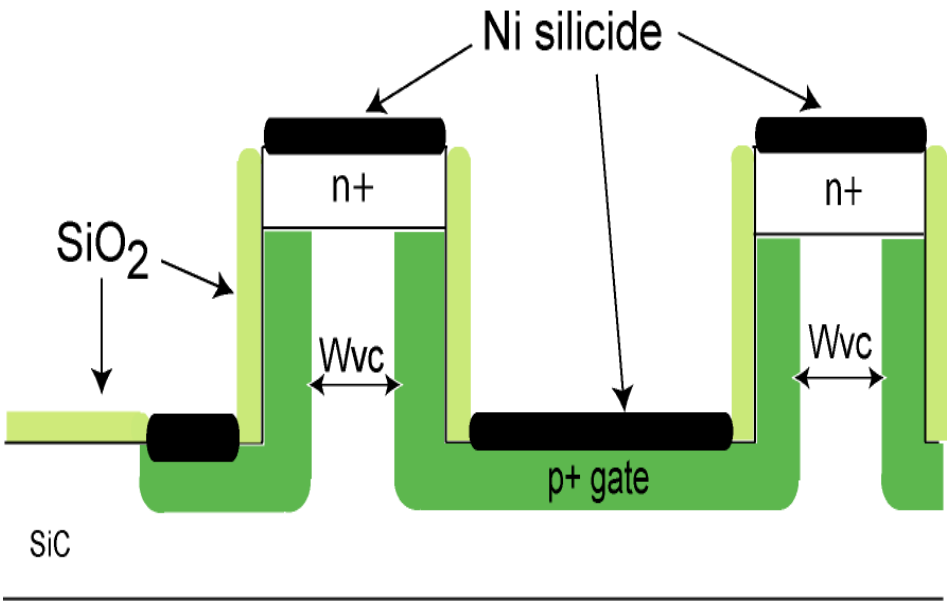


Fig. 2-3 (d) Ni silicide formed after two-step annealing

Prior to ohmic contact formation, both vertical and lateral versions of the TI-VCJFETs undergo the source mesa creation and tilted sidewall implantation procedures that forms the vertical JFET channel structure. The self-aligned Ni contact process starts after all implantations are complete, with the deposition of a 200nm SiO_2 layer across the wafer by PECVD. (Fig.2-3a) Patterning the oxide layer is a key step for the subsequent selective removal of Ni after annealing. AZ4400 photoresist is applied to the SiC sample, and photoresist windows in the mesa and trench region are opened by UV exposure and developing in an AZ 1:1 developer solution. The removal of the PECVD oxide on top of the mesas and at the bottom gate contacts is accomplished with the AZ4400 masking layer by vertical ICP etching in CF_4, which does not attack the oxide layer on the mesa sidewalls. (Fig. 2-3b) Ni metal layer of 100~200nm is then deposited by sputtering, covering the

entire wafer including the contact holes, the top of the remaining oxide layer, as well as the mesa sidewalls. (Fig. 2-3c) Subsequently a low-temperature annealing in argon forming gas at 700^{o}C to 800^{o}C for 3 to 5 minutes forms nickel silicides in the contact holes, while leaving Ni in its original state where oxide layer still exists to block the reaction between Ni and SiC. A mixture of sulfuric acid and hydrogen peroxide is used to selectively remove the unreacted Ni. The nickel silicide at the source and gate contact regions is not affected by the exposure to sulfuric acid in this step. These silicide contacts are further annealed at 950^{o}C~1050^{o}C to form ideal ohmic contacts to the n-type source. (Fig. 2-3d) It is noted that two annealing steps are necessary because the high-temperature annealing needed for the source contacts, if performed without the prior low-temperature annealing and wet etching steps, would cause excessive Ni-SiC reaction and form irremovable silicide residues even on top of the oxide layer, making the self-aligned Ni removal impossible. An example showing the excessive Ni reaction after a single 1050^{o}C annealing is shown in Fig. 2-4, where TLM-patterned oxide windows were opened for the trial experiment of selective Ni removal.

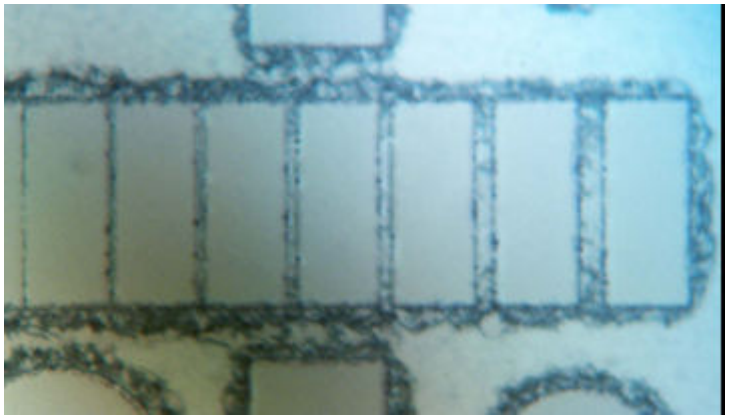


Fig. 2-4 (a) Optical microscope image after 1050^{o}C Ni annealing

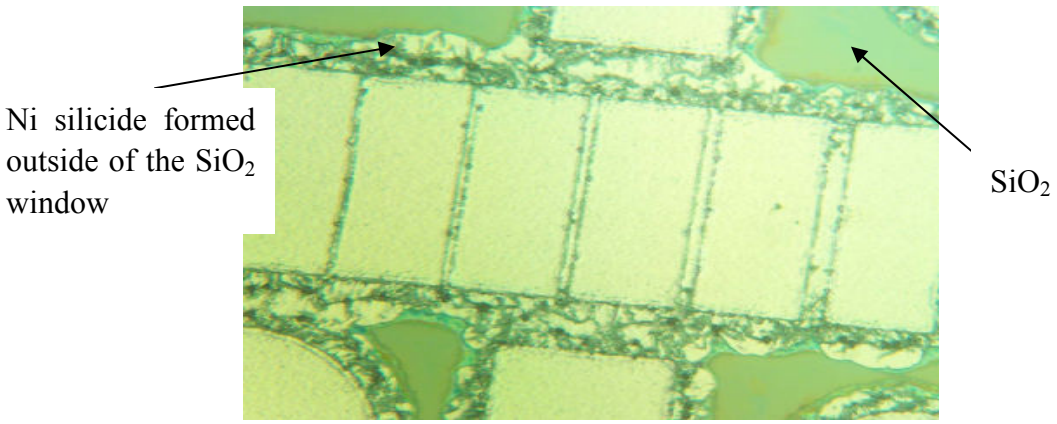


Fig. 2-4 (b) Optical microscope image after selective wet etching of Ni

After the development of the two-step annealing, self-aligned Ni ohmic contact scheme, it has been successfully applied to the fabrication of vertical and lateral TI-JFET structures by myself and co-workers at SiCLAB.

2.3 Physics Aspects of Forming Ohmic Contacts to SiC

While the above experimental procedure has been established and confirmed in our device fabrication, the mechanism of one metal forming both n- and p-type ohmic contact to a wide bandgap material like SiC calls for an analysis.

The work function of Ni is 5.15eV [23], and the electron affinity of 4H-SiC commonly used in literature is between 3.3eV [39] and 4.05eV [40]. According the the Schottky Barrier Height estimation, the contact between Ni and n-type and p-type 4H-SiC should be rectifying, not ohmic. In fact, as-deposited Ni contact to 4H-SiC does show a rectifying behavior. The Ni ohmic contact behavior, typically reported for n-type contacts, can only be achieved after a high temperature annealing over 950^{o}C. Because

Ni reacts with SiC to form nickel silicide at the high temperatures required for ohmic contact annealing, it was assumed that the formation of silicide is responsible for the ohmic contact behavior. [41] The reaction between Ni and SiC at temperature above 700^{o}C is dominated by the formation of the Ni_2Si phase: [23]

$$2Ni + SiC \rightarrow Ni_2Si + C \quad (2.1)$$

However, more recent research suggests that the true mechanism of Ni to n-type SiC ohmic contact may be less relevant to Ni_2Si. A particular interesting paper by Nikitina *et al.* [42] revealed that the ohmic contact behavior after the Ni-SiC reaction is preserved even if the Ni_2Si and graphite films formed during the high-temperature annealing is removed by etching and replaced by new metal without any annealing. Along with reports from other teams [43], there is increasing evidence that carbon vacancies created in SiC after the Ni-SiC reaction may act as donors for electrons, and effectively reduce the Schottky barrier width and height in the Ni-SiC contact interface, resulting in the Schottky-to-ohmic contact conversion.

During my experimental development of the Ni contact process for TI-JFETs, a temperature dependency of the Ni to n-SiC and p-SiC specific contact resistance is observed. This interesting phenomenon may support the above-mentioned view on the physics mechanism of Ni-to-SiC ohmic contacts, and will be described in this section.

In our experiments for specific contact resistance measurement, an n-type 4H-SiC sample with a top epilayer doped to $2x10^{19}cm^{-3}$ is used. The p-type sample has a top epilayer with an aluminum doping level at $8x10^{19}cm^{-3}$. The Ni-to-SiC specific contact

resistances are estimated by using the Linear Transfer Length Method (L-TLM) explained below.

In the L-TLM method, two masks are usually needed. One will define TLM patterns like in Fig. 2-5, and the other will constrict the current in one dimension either by mesa etching or junction isolation.

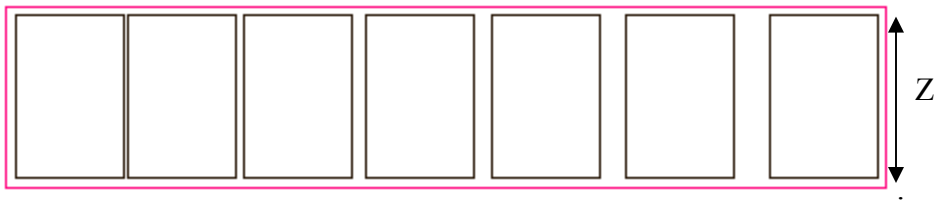


Fig. 2-5 TLM pattern

Each of the rectangular shaped pads is intended to for a metal contact. The width of the mesa is Z, and the distance between two adjacent pads is d, a variable parameter from the narrowest at the left side to the widest on the right. When performing a TLM test, each pair of the adjacent pads are probed to find the total resistance between them, resulting in a group of resistance points as a function of the distance of the spacing d. The total resistance of any two adjacent TLM pads is given by [44]

$$R_T = \frac{\rho_s d}{Z} + 2R_C \tag{2.2}$$

where ρ_s is the sheet resistance of the epilayer, and R_c is the contact resistance for one metal-semiconductor contact pad.

The total resistance (R_T) measurement results can be plotted as a function of the spacing distance as in Fig. 2-6. [44] R_c contact resistance can then be determined from

the y-axis intercept of the linear fit line based on the R_T data points. The x-axis intercept of the line gives L_T, the linear transfer length.

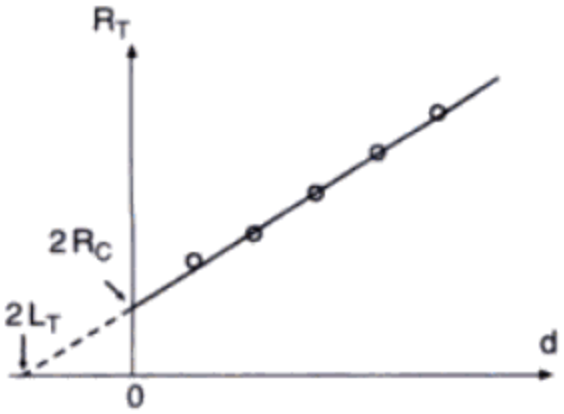


Fig. 2-6 Plot of total resistance versus spacing

If the length of each contact pad L is shorter than half of L_T, then the effective contact area for the pad is the actual area ZxL. However, in most cases the effective contact area is not the pad's size because of current crowding effect. In practice, as long as the length of the pad is greater than $1.5L_T$, the effective area ZxL_T is used for the metal-semiconductor contacts. The specific contact resistance can therefore calculated by:

$$\rho_c = R_c L_T Z \tag{2.3}$$

In our exploration of various annealing conditions for Ni ohmic contacts to n-SiC and p-SiC, we first observed that as-deposited Ni shows no ohmic contact behavior to either n- or p-type SiC. After the low-temperature annealing, nickel silicide is formed. The

p-type specific contact resistance is measured in the $10^{-4}\,\Omega\cdot cm^2$ range. A typical p-type TLM measurement example is shown in Fig. 2-7.

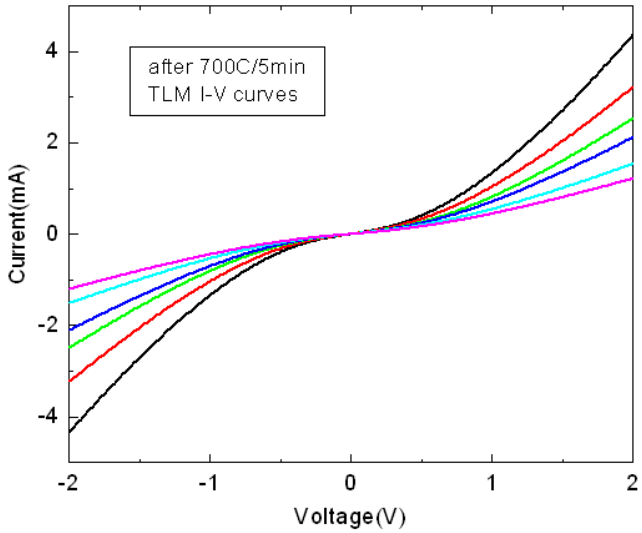


Fig. 2-7 (a) TLM I-V testing results for p-type contacts after 700°C annealing

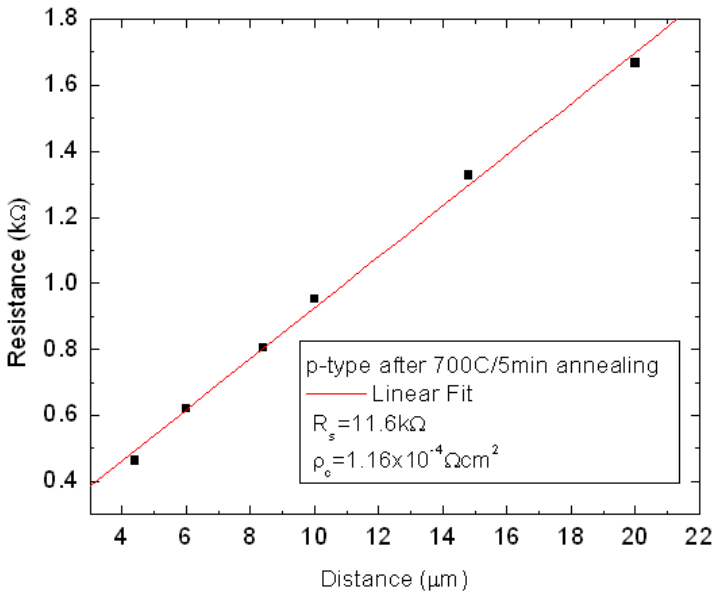


Fig. 2-7 (b) TLM plot of p-type contacts after 700°C annealing

When the annealing temperature is elevated to over 950°C, excellent n-type ohmic contacts are formed. The I-V curves measured from n-type TLM patterns are perfectly

linear. A plot example for calculating the n-type specific contact resistance is shown in Fig. 2-8.

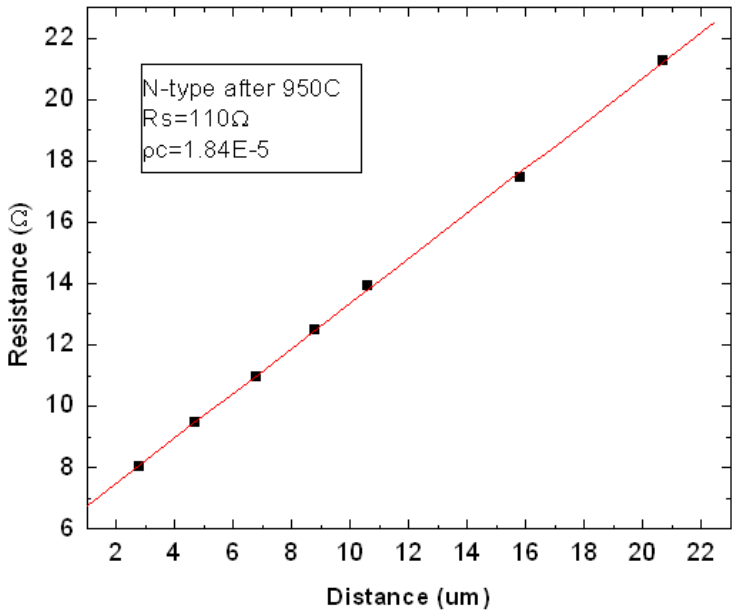


Fig. 2-8 n-type TLM test plot after 950°C annealing

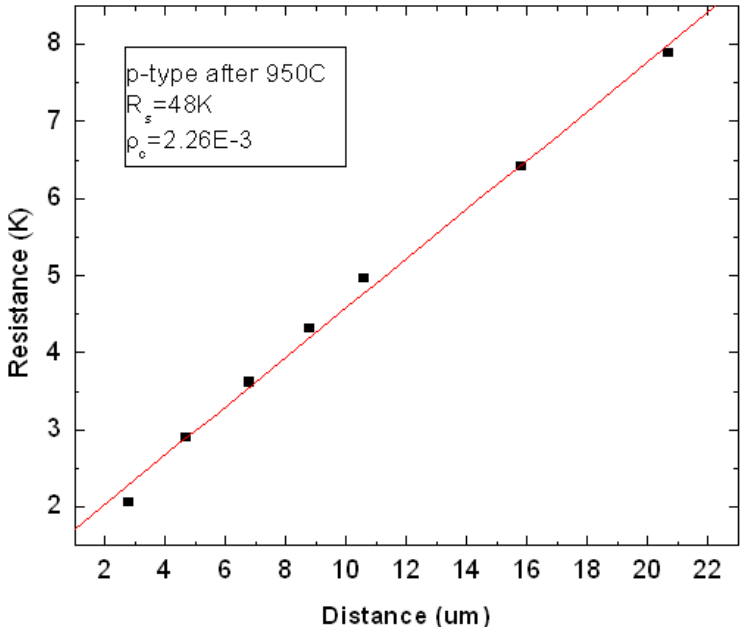


Fig. 2-9 p-type TLM test plot after 950°C annealing

While this annealing temperature is necessary to create n-type Ni ohmic contacts, it is seen that the p-type ohmic contacts are degraded in comparison to the lower-temperature annealed ones. A typical p-type TLM measurement result after 950°C annealing is shown in Fig. 2-9, giving a specific contact resistance in the 10^{-3} $\Omega \cdot cm^2$ range. After a group of experiments at different annealing temperatures, the average specific contact resistances measured for n-type and p-type SiC are summarized in Fig. 2-10.

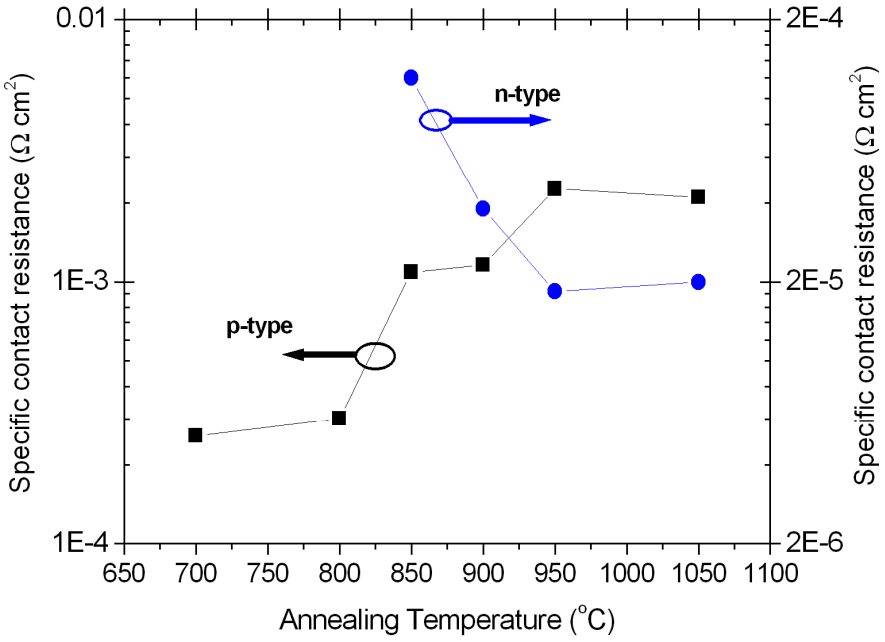


Fig. 2-10 Annealing temperature dependence of Ni specific contact resistances

This interesting balance between n-type and p-type ohmic contact resistances can be explained by the recently suggested carbon-vacancy mechanism for Ni-SiC contacts. [45] Specifically, the low-temperature annealing at 700~800°C forms nickel silicide in a variety

of phases including Ni_2Si, which has a higher work function than Ni [43]. According to the classic Schottky Barrier Height (SBH) theory, this will lower the barrier at the Ni to p-type SiC interface, and hence facilitate the formation of ohmic contacts in the presence of a highly doped p-type SiC epilayer. However, the formation of Ni_2Si itself does not make the n-type contacts ohmic because carbon outdiffusion does not happen at these temperatures. A higher temperature annealing above 950^{o}C is needed for the carbon atoms to outdiffuse and accumulate at the contact surface. Hence a so-called "catalytic graphitization" effect by Ni creates abundant donor-like carbon vacancies in the near-interface region of SiC. [42] As a result, the effective doping level at the n-type SiC surface is greatly enhanced, leading to a reduction of the Schottky barrier width. Ohmic contacts are therefore obtained in the n-type samples. For the p-type contacts, on the contrary, the acceptor doping level in the near-interface region of SiC is effectively reduced due to charge compensation. The Schottky barrier width for the p-type contacts is hence increased, degrading the ohmic contact resistances after the high-temperature annealing.

In our application of the Ni contact scheme to SiC JFETs, the higher temperature annealing is required to ensure optimal ohmic contacts for the n-type source and drain, even though this comes at a modest cost to the gate contact. The n-type contact resistance carries much more attention since the current level at the source and drain contacts will be orders of magnitude larger than at the gate.

CHAPTER 3 DEVELOPMENT OF 4H-SiC POWER LJFETS

3.1 Device Structure and Simulation Results

In 2005, a theoretical study of normally-off VC-LJFET structure was first reported. [46] The designed normally-off VC-LJFET has an optimized double RESURF termination, capable of up to 1535V blocking with a specific on-resistance of only 3.24 mΩ·cm^2. These simulation results demonstrate the VC-LJFET structure's potential of very high figure-of-merit (FOM) performances comparable to state-of-the-art vertical power JFETs.

In this dissertation research, the proposed power VC-LJFET device structure is shown in Fig. 3-1. Similar to TI-VJFETs, the VC-LJFET does not require epitaxial regrowth.

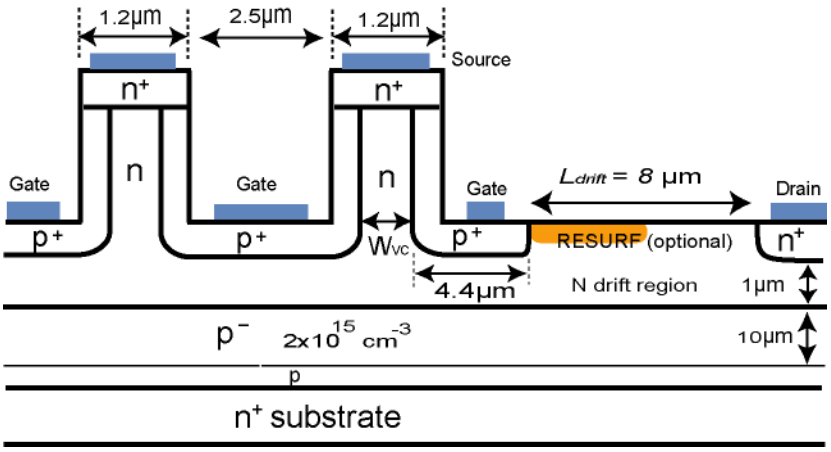


Fig. 3-1 Power VC-LJFET Unit Cell Structure

The structure starts from a 4H-SiC N+ substrate for best available wafer quality. On top of it, two p-type layers are designed to support the voltage drop between the high-voltage drain and grounded substrate, and avoid vertical punch-through. The lateral n-type drift layer is doped to 7.5x10^{16} cm^{-3}. An 8μm drift length is used to laterally support

the high drain voltage. A separate area in the lateral drift region may be converted to p-type and serve as an additional Reduced Surface Electric Field (RESURF) termination. The RESURF design principle is widely used in silicon lateral power devices. [47] With this approach, two-dimensional charge-coupling between the N-drift layer and the p-type adjacent regions is utilized to modify the lateral electric field so that the breakdown voltage is enhanced. In the VC-LJFET design, the 10μm p- layer below the lateral channel serves as the bottom RESURF, while the optional p-type region at the top of the lateral channel is created by ion implantation and provides a double RESURF effect.

Further up from the lateral drift layer, the vertical JFET channel is 1.8μm long, and has a nitrogen doping concentration of $3x10^{16}$ cm^{-3}. The double sidewall p implantation leaves a vertical submicron channel width Wvc that is self-depleted by the built-in p-n junction potential at zero gate bias; making the power LJFET normally off. A heavily doped n++ layer caps the vertical channel for source ohmic-contact formation.

The proposed power VC-LJFET device was simulated in a TCAD package, courtesy of Dr. Xueqing Li of United Silicon Carbide, Inc. The theoretical blocking voltage was found to be 1.1kV to 1.3kV depending on field crowding considerations, illustrated in Fig. 3-2 (a). And the forward characteristics of the VC-LJFET are shown in Fig. 3-2 (b), with a vertical channel opening Wvc of 0.43μm. It can be seen that under 2.75V gate bias, the LJFET offers a low specific on-resistance of 9.5 $m\Omega \cdot cm^2$, giving it a potential V_{br}^2/R_{sp} FOM up to an impressive value of 177 MW/cm^2. It should be noted that the vertical channel opening (Wvc) of this device is a critical parameter. A channel too wide will make

the device normally on, making it undesirable based on the fail-safe considerations for power electronic circuits. On the other hand, a channel too narrow will compromise the device's current conduction capability and its specific on-resistance at on-state. Based on fine-tune optimization on the TCAD simulator, the submicron channel opening (Wvc) is determined in the range of 0.35–0.55 μm for an optimal balance between forward current conduction and gate threshold voltages.

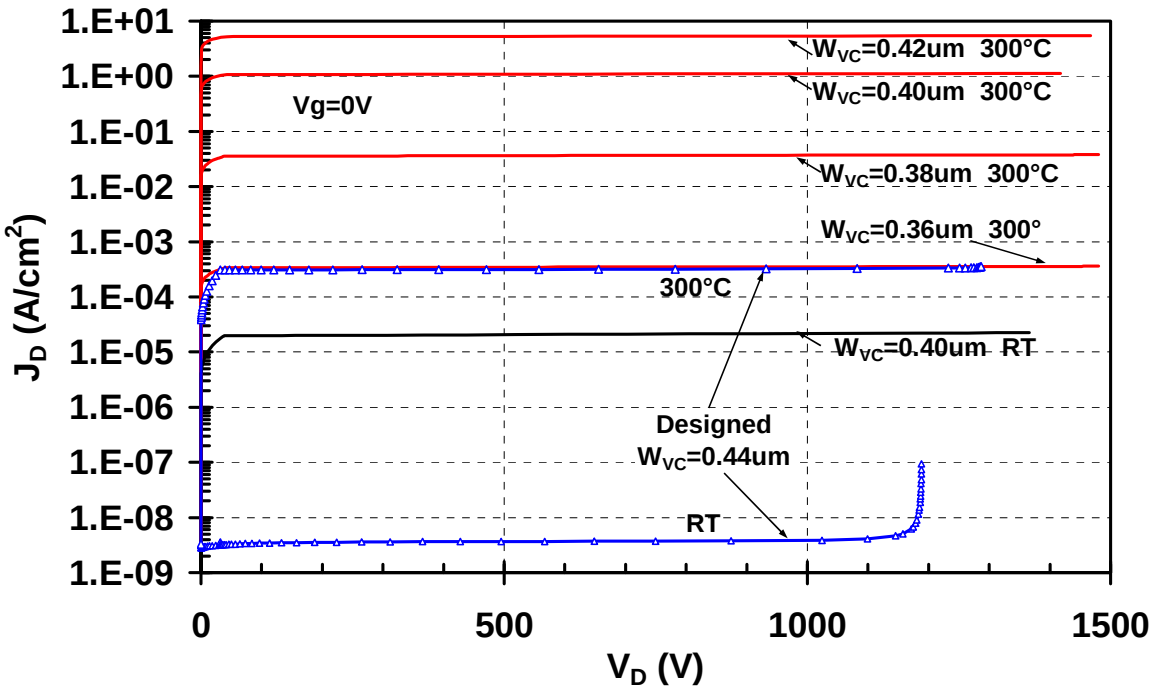


Fig. 3-2 (a) Simulated blocking characteristics of the VC-LJFET

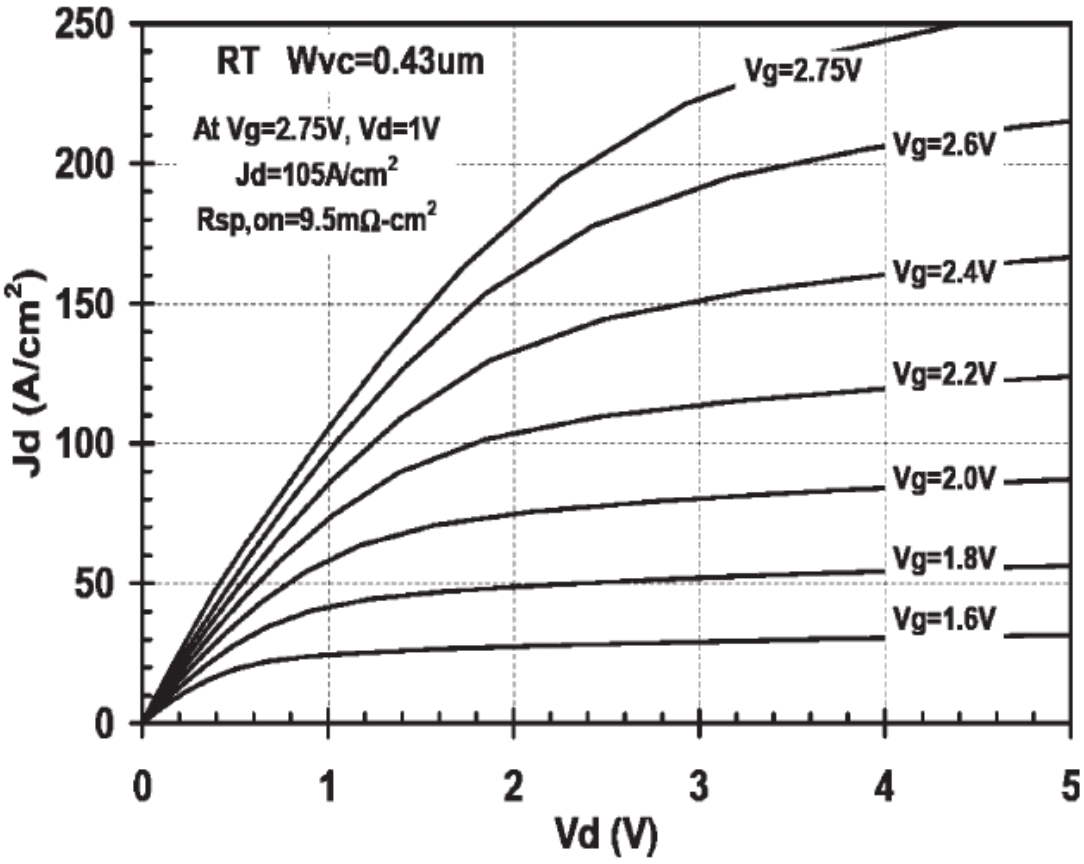


Fig. 3-2 (b) Output characteristics of a normally off lateral JFET

at room-temperature simulated by ISE TCAD

The intended fabrication procedure for this power VC-LJFET is in many ways similar to a TI-VJFET process, with an improved ohmic contact scheme discussed in the earlier chapter. More critical alignment steps are needed for the VC-LJFETs due to the top-surface placing of all the electrodes. The key fabrication procedures will include mesa etching, implantation for gate and device isolation, implantation for drain contacts, post-implantation activation annealing, surface oxidation and passivation, forming ohmic contacts and adding metal overlayers. Based on the device unit cell design, process flow

planning, and linewidth control data from our fabrication experiences, the mask layout for power LJFET is designed. Power JFETs of various sizes and geometry are included in the mask, two of which are shown in Fig. 3-3 (a) and (b). Fig. 3-3 gives the reader a close-up view of a JFET unit cell, including mesa structures and each implantation boundaries. Along with these power JFETs, test patterns such as TLM, diodes, gate-source shorting tests, isolation tests are also designed and implemented on the mask.

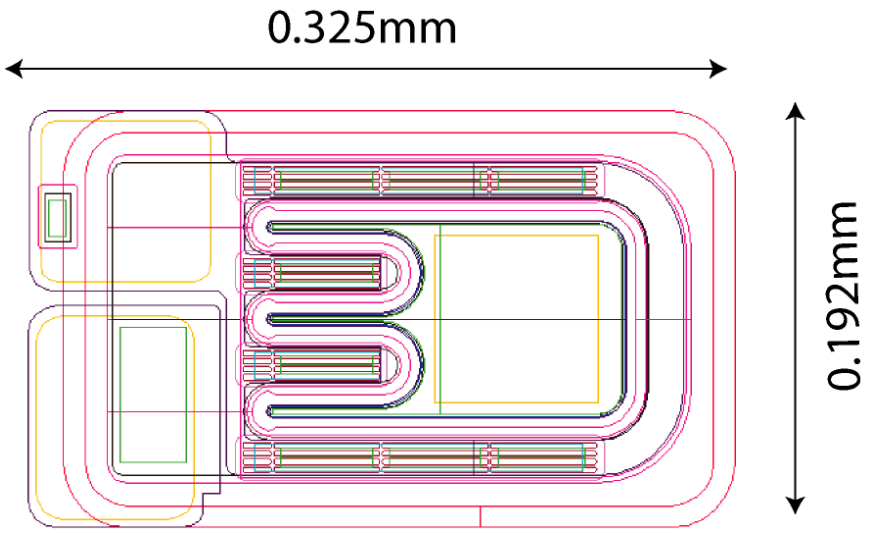


Fig. 3-3 (a) A small power VC-LJFET on the mask

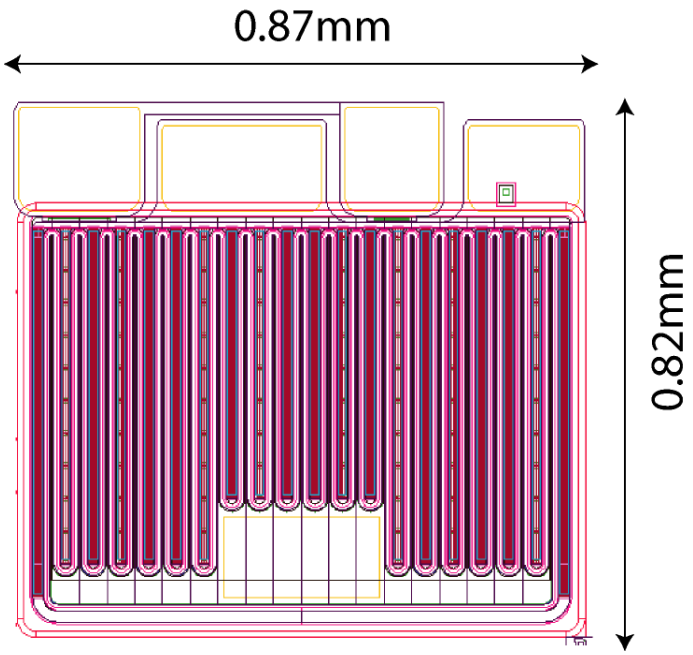


Fig. 3-3 (b) A larger VC-LJFET on the mask

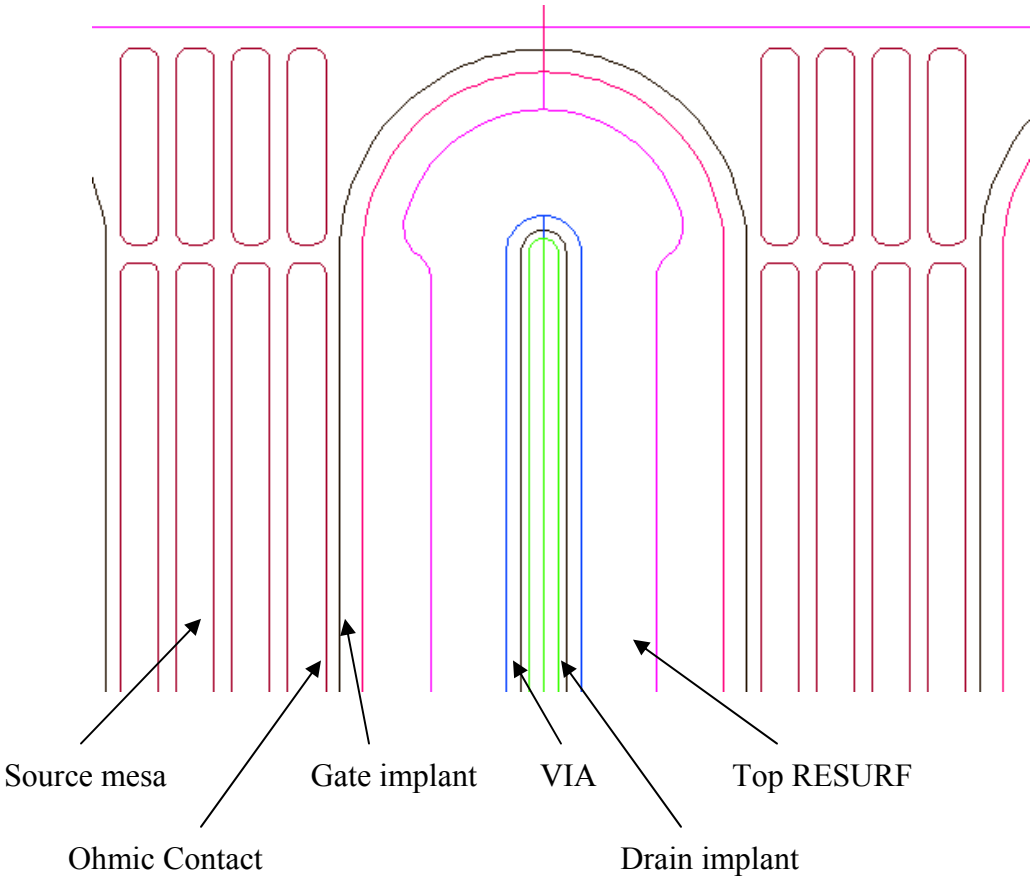


Fig. 3-3 (c) Close-up view of a device unit cell on mask

3.2 Fabrication of the World's First 4H-SiC Normally-off Power Lateral JFET

3.2.1 Wafer Specification and Cleaning

The starting 4H-SiC wafer was ordered from Cree, Inc. with requested layer doping specification as in Fig. 3-3 (a). Fig. 3-3 (b) is a SIMS depth profile for the dopants measured from the actual wafer.

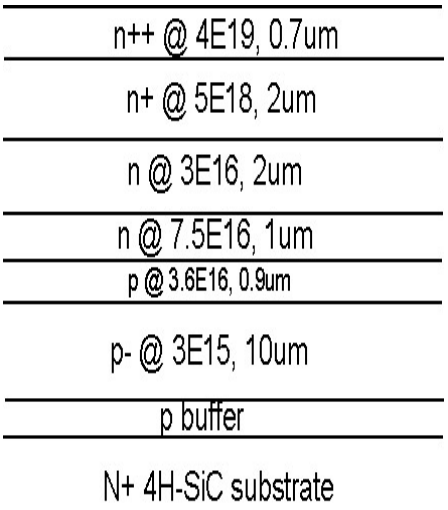


Fig. 3-3 (a) Wafer layer structure

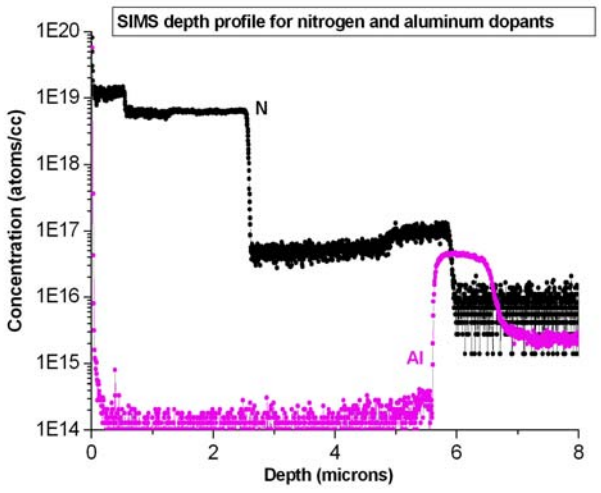


Fig. 3-3 (b) SIMS analysis for dopants

From bottom up, the wafer has an n+ substrate and a 10μm p- layer for vertical voltage support. A thin p layer follows for bottom RESURF effect in blocking mode. The lateral and vertical n-type channels are grown on the RESURF layer with doping concentration of $7.5x10^{16}$ cm^{-3} and $3x10^{16}$ cm^{-3}, respectively. 2μm n+ region is used primarily to allow a larger mesa height thus gate and source terminals are easier to separate. The wafer is finally capped with a 0.7μm n++ layer for source ohmic contacts.

Wafer fabrication starts with a full cleaning of the ordered wafer, including the following steps: [48]

(1) Acetone ultrasonic: This is a general cleaning that removes dust and some contaminations on the wafer.

(2) Mixture of sulfuric acid and hydrogen peroxide: 98% H_2SO_4 (sulfuric acid) is mixed with 30% H_2O_2 (hydrogen peroxide) at the volume ratio of 4:1 and heated to 85^oC. The SiC wafer is then immersed in this solution for 30 minutes for the removal of possible gross organic materials, such as photoresist, polymer or other contaminants. These contaminants are destroyed by the wet-chemical oxidation effect of the mixed solution.

(3) RCA cleaning: This procedure was developed at RCA forty years ago, and has been widely used for silicon wafer cleaning. [48] First, a mixture of deionized (DI) water (H_2O), hydrogen peroxide (H_2O_2) and ammonium hydroxide (NH_4OH) is prepared at the volume ratio of 5:1:1 and heated up to 80^oC. This solution is commonly called SC-1. The SiC wafer is placed in the SC-1 solution for up to 30 minutes. SC-1 is

intended to remove organic contaminants that are attacked by both the solvating action of NH_4OH and the powerful oxidizing action of the alkaline H_2O_2. NH_4OH also removes certain metals such as Cu, Au, Ag, Zn, Cd, Ni, Co and Cr by complexing them. After this, an acidic solution commonly called SC-2 is prepared by mixing DI H_2O, H_2O_2 and hydrochloric acid (HCl) at the volume ratio 5:1:1. This solution is also heated to 80^oC for a 30-minute cleaning of the SiC wafer. The SC-2 is designed to dissolve and remove alkali residues and any trace metals, such as Au and Ag, as well as metal hydroxides, including $Al(OH)_3$, $Fe(OH)_3$, $Mg(OH)_2$ and $Zn(OH)_2$.

(4) 10% hydrofluoric (HF) acid: The full cleaning procedure is completed with an ultrasonic cleaning in diluted hydrofluoric acid, refreshing the SiC surface by removing the top oxide layer.

3.2.2 Mesa etching and trimming

After wafer cleaning, source mesas are etched in an inductively-coupled plasma (ICP) chamber by a Bosch process based on CF_4 and O_2 gas chemistry. As discussed earlier, dry etching methods for SiC materials have been examined in many reports and the most effective gases are usually based on fluorine chemistry. In CF_4+O_2 gas mixture for SiC etching, the following reactions are proposed to take place:[44, 49]

$$CF_4+O_2 \rightarrow CF_x + F + O + (CO, CO_2) \quad (3.1)$$

$$Si + xF \rightarrow SiF_x \quad (3.2)$$

$$C + xF \rightarrow CF_x \quad (3.3)$$

$$C + xO \rightarrow (CO,\ CO_2) \tag{3.4}$$

A 300nm AlTi layer is deposited on the wafer by sputtering to serve as the etching mask layer. Photolithography using AZ5214 resist followed by wet etching in a commercial Al Etch II solution creates the mesa etching mask patterns. The lithography recipe is listed in Table 3-1. AlTi mask etching is finalized by a Al residue cleaning procedure in highly diluted hydrofluoric acid (3%x3%x3%) for one minute. After this, photoresist is removed in heated AZ400T stripper at 80^{o}C for 20 minutes.

Dry bake	130^{o}C, 30 minutes
Photoresist Spin-coat	AZ5214 photoresist with 1μm syringe filter Spin at 4000 RPM for 40 seconds
Soft Bake	90^{o}C 20 minutes
Exposure	UV exposure, 5 seconds
Develop	AZ 1:1 developer, 90 seconds
Hard bake	130^{o}C, 30 minutes

Table 3-1 Photolithography recipe for mesa etching mask using AZ5214

The Bosch etching process used here for etching SiC was initially developed by Dr. Y. Li using CF_4, O_2 and C_4F_8 source gases. [37] This process utilizes alternating steps of polymer deposition from the C_4F_8 source gas, and anisotropic ICP etching by CF_4 and O_2. The polymer deposited on the mesa sidewalls provides protection against side etching

and therefore makes the Bosch process suitable for deep trench applications. A comparative study of 4μm trench etching using various Bosch and regular ICP recipes was performed in this dissertation research, based on which the optimized etching conditions for the VC-LJFET mesas are determined. Fig 3-4 presents the etching profiles by different recipes.

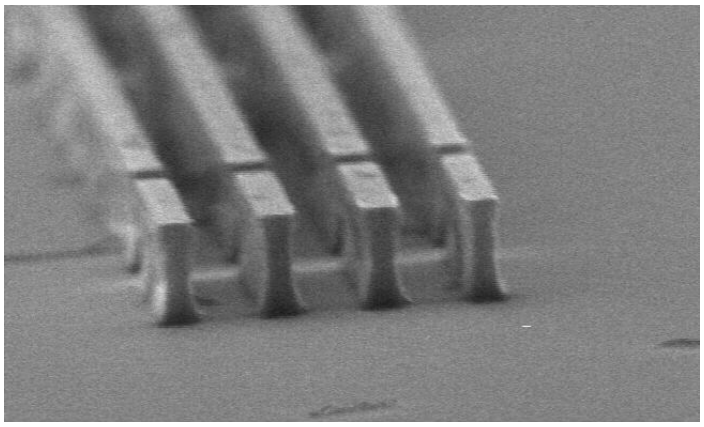


Fig. 3-4 (a) Regular CF_4/O_2 ICP process 50V 700W

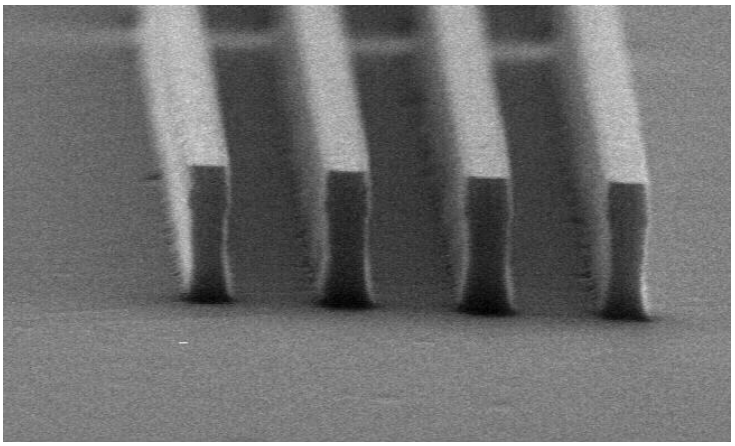


Fig. 3-4 (b) CF_4/O_2 ICP etching with 100V DC bias

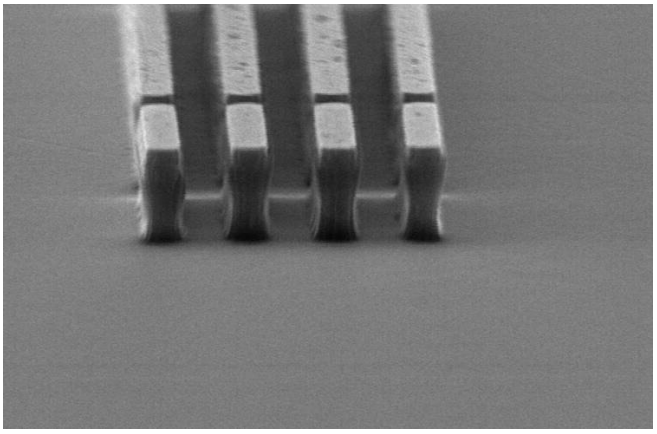


Fig. 3-4 (c) Bosch recipe originally developed by Dr. Li [37]

(etching 9 cycles with 100V DC bias, followed by 50V DC bias)

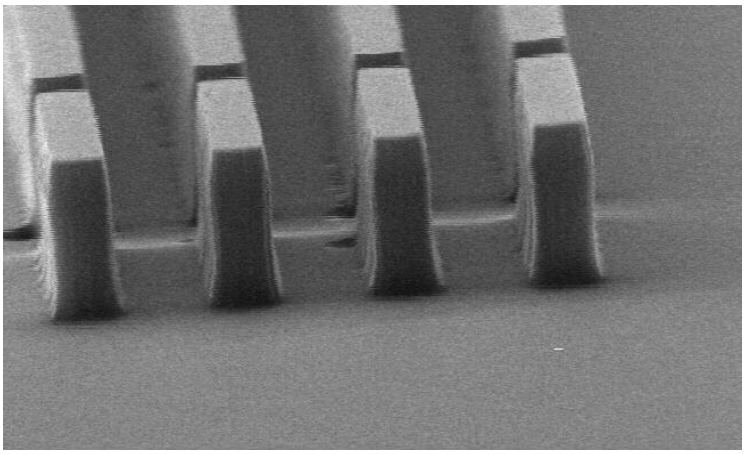


Fig. 3-4 (d) Bosch recipe using 100V DC bias only

Fig. 3-4 (a) ~ (d) 4μm deep trench etching in SiC:

SEM pictures of mesas etched by Bosch and regular CF_4/O_2 recipes

The results from the deep trench etching study strongly favor the 100V-only Bosch process for vertical sidewall profile, which is applied to the VC-LJFET fabrication. The resulting cross-sectional structure after mesa etching is illustrated in Fig. 3-5.

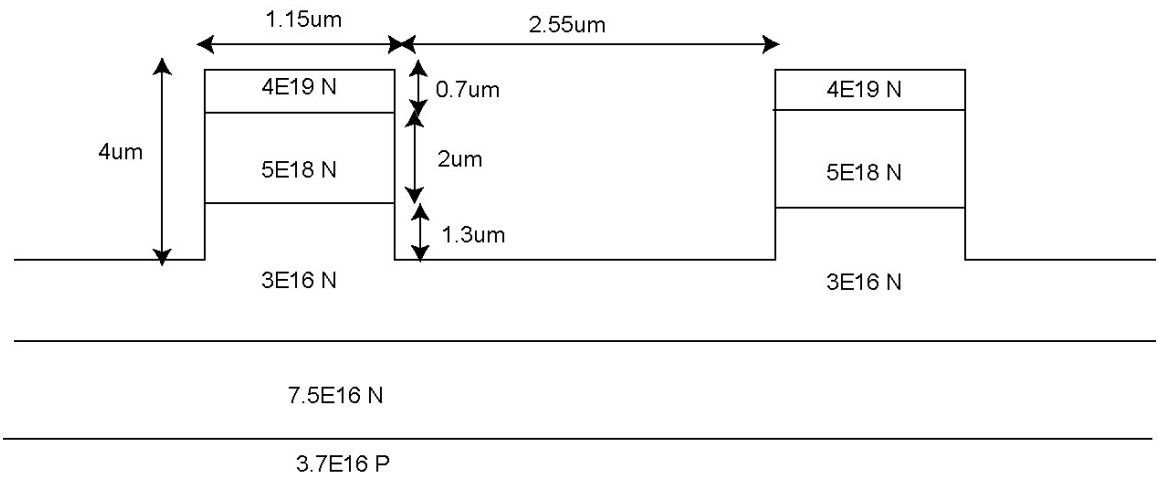


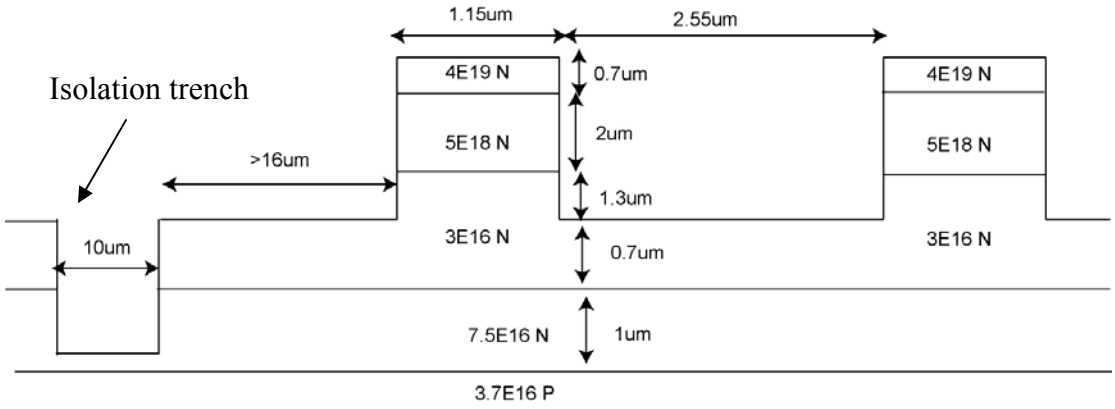
Fig. 3-5 Schematic illustration of VC-LJFET mesa etching

In order to prevent vertical channel choke-off due to insufficient Wvc, the mesa widths after the Bosch process are intentionally planned to be slightly wider than the design target. We then performed 0V-bias CF_4/O_2–based ICP trimming on the wafer in small intervals until the mesa widths across the wafer matches the designed target range.

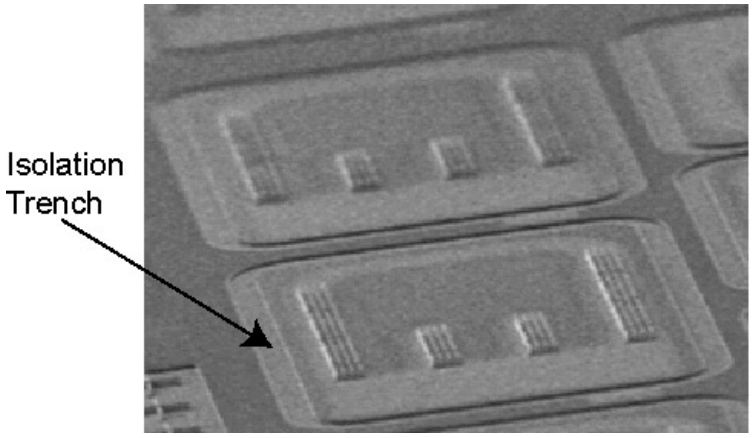
3.2.3 Isolation trench etching

Device isolation for the VC-LJFETs is accomplished by etching 1.7μm-deep peripheral trenches around the active devices, and then adding junction isolation by implanting the etched trenches together with the gate regions. Trench etching allows the relatively shallow gate implantation to reach the buried p layer, thus eliminating the need of a separate implantation solely for the device isolation purpose. This process uses a 600nm-thick AlTi mask, patterned by wet etching in Al Etch II solution. AZ4400 thick photoresist is defined on the wafer prior to the wet etching to transfer the photomask

patterns to AlTi. The lithography condition for AZ4400 is listed in Table 3-2. Following the photoresist removal in AZ400T, a regular 50V ICP etching recipe is used to create the trenches in SiC. A schematic cross-sectional view and an SEM photo showing the etched isolation trenches are included in Fig. 3-6 (a) and (b). This process step is completed with a hydrofluoric acid cleaning of the AlTi etching mask.



(a) Schematic illustration of the isolation trench



(b) SEM picture of VC-LJFET devices after isolation trench etching

Fig. 3-6 Isolation trenches

Dry bake	130^{o}C, 30 minutes
Photoresist Spin-coat	AZ4400 photoresist with 1μm syringe filter Spin at 3500 RPM for 40 seconds
Soft Bake	100^{o}C 20 minutes
Exposure	UV exposure, 30 seconds
Develop	AZ 1:1 developer, 4 minutes
Hard bake	130^{o}C, 30 minutes

Table 3-2 Photolithography recipe using AZ4400

3.2.4 Gate and Isolation Implantation

The mesa sidewalls and trench bottom regions are required to be converted to p-type gate for proper JFET function. This is accomplished by a masked implantation procedure using aluminum ions. This implantation also adds junction isolation to the VC-LJFETs as mentioned earlier. Fig. 3-7 illustrates the device regions converted by the gate implantation. To create the implantation mask, a 1μm-thick molybdenum (Mo) film is deposited onto the wafer and patterned by photolithography (AZ4400) and wet etching (Al Etch II). The wafer with Mo mask was sent to Leonard J. Kroko, Inc. for the aluminum ion implant service.

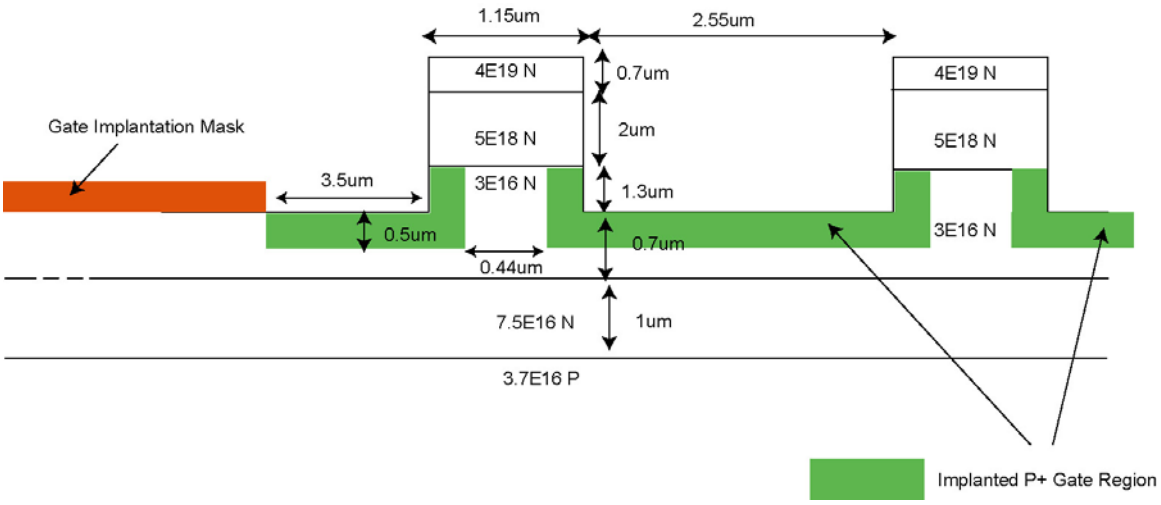


Fig. 3-7 Illustration of Gate implantation process

In order to create the p+ regions in the mesa sidewalls, we requested four groups of tilted Al doses with a 28^{o} incidence angle. The four groups of implants, each including a 350keV dose and a 100keV dose, are in orthogonal directions as in Fig. 3-8, converting all sides of the mesa into gate regions. The tilted implantation process was originally created for normally-off TI-VJFETs [35], and we used the same procedure here to define normally-off VC-LJFETs.

Besides the tilted Al doses, two low-energy doses strictly perpendicular to the wafer surface are used to create a heavily doped p++ regions for ohmic contacts. Fig. 3-9 (a) and (b) give the simulated implantation depth profiles for the sidewall and gate body regions. The simulation software used is Profile Code, with the assumption of Pearson IV distribution. It should be emphasized that the sidewall implantation depth control is extremely critical for normally-off device operation since the Wvc channel opening parameter is determined by the mesa widths minus double of that depth.

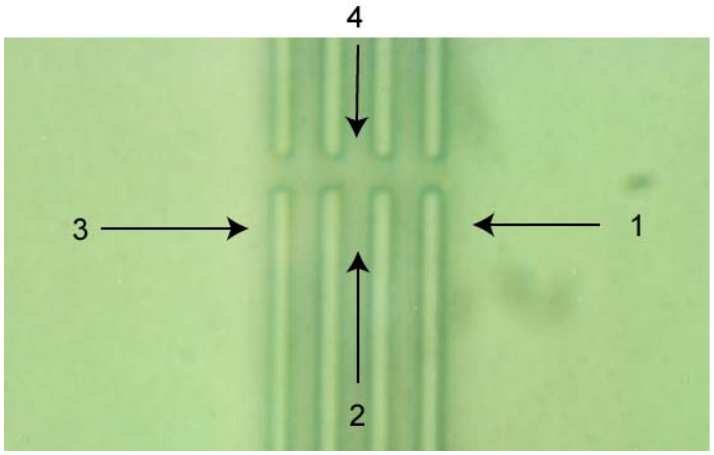


Fig. 3-8 Al implant doses in four directions

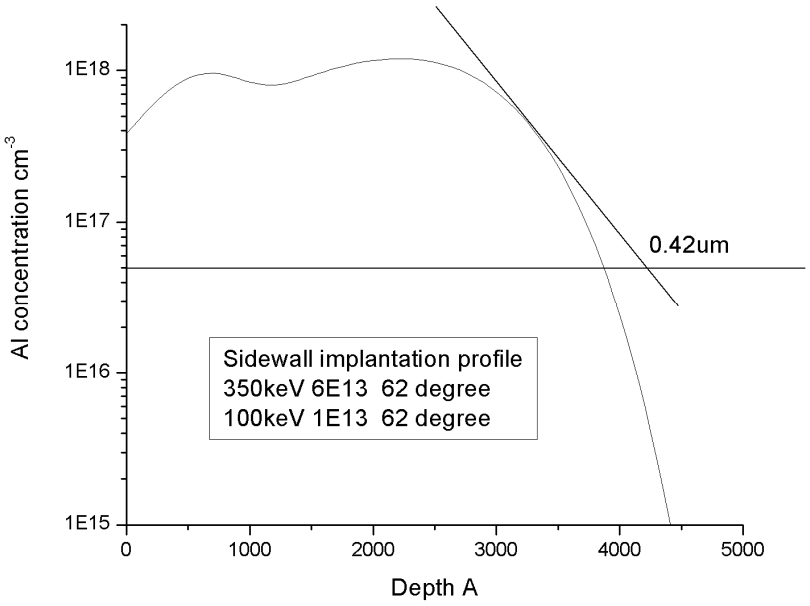


Fig. 3-9 (a) Mesa sidewall Al depth profile

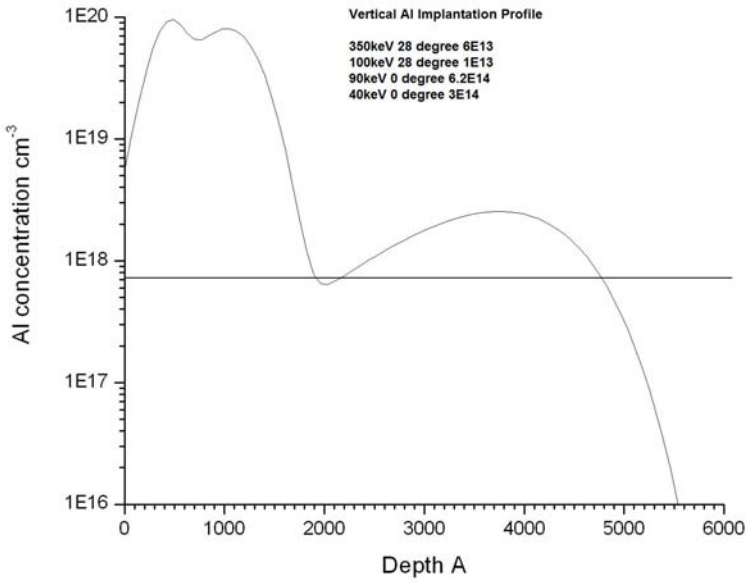


Fig. 3-9 (b) vertical Al depth profile in gate region

Fig. 3-9 Gate implantation simulations by Profile Code

3.2.5 Drain Implantation and activation annealing

Following the gate implantation and wafer cleaning, the sample is patterned with molybdenum mask and sent out again for nitrogen ion implantation. This implantation creates n+ regions for the device drain contacts. A cross-sectional schematic of the VC-LJFET after drain implantation is shown in Fig. 3-10. The simulated nitrogen ion depth profile from this implantation has a 200nm box figure at the concentration of $1x10^{19}$ cm^{-3}, as shown in Fig. 3-11.

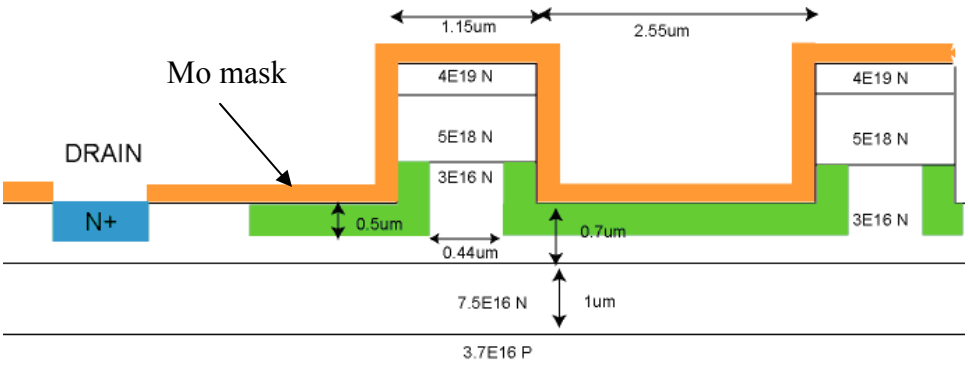


Fig. 3-10 Cross-sectional view after drain implantation

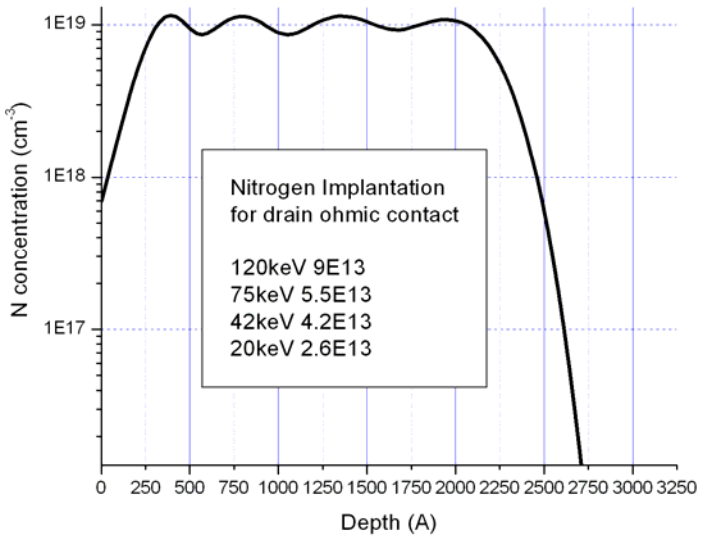


Fig. 3-11 Drain implantation (nitrogen ion) depth profile

3.2.6 Activation of Implanted Dopants

In the first batch of power VC-LJFET fabrication, we decided to skip the optional top RESURF implantation as a measure to simplify the process steps. Without the top RESURF, the device is expected to block less voltage than the optimized design predicts.

This leaves room for further performance improvement while allowing us to demonstrate the first functional normally-off power LJFET as early as possible.

The sample returned from drain implantation has completed gate and drain regions and is ready for implant activation. We performed full cleaning of the wafer in sulfuric acid, RCA SC-1, RCA SC-2 and hydrofluoric acid. Then it is annealed in argon ambient at 1550^{o}C for 30min to electrically activate the implanted nitrogen and aluminum dopants.

The entire implantation and post-implantation annealing process was established in SiCLAB with practical considerations of the equipment and safety margin. However, we are aware that better conditions in terms of surface morphology, dopant activation and damage reduction exist. When feasible, these process improvements will be explored. Currently, there is a consensus in the SiC community that implantation done at a temperature above 500^{o}C together with a post-implantation annealing at around 1600~1700^{o}C may yield the best results. [8, 44]

3.2.7 Mesa top removal

Based on the gate implantation process described earlier, the topmost n++ layer in the source mesas has been exposed to high-dose aluminum implantations. This was not the case when Dr. Kiyoshi Tone developed his TI-VJFETs because he placed a thick metal masking layer on the mesa tops by lift-off before the gate implantation. [30] The current process eliminates this procedure and simplifies the gate implantation mask formation. In this scheme, the very top portion of the mesas is severely affected by aluminum ions and

therefore converted to p-type, making it unsuitable for source contacts. The mesa top removal procedure etches away the affected top SiC, and once again turns the mesa tops into ohmic-contact-ready regions. Fig. 3-12 illustrates this step, which involves a 500nm AlTi mask, patterned by a sequence of AZ4400 photoresist planarization, etchback in O_2 plasma, and wet etching in Al Etch II to expose the mesa tops. CF_4-O_2 plasma ICP then removes 0.2~0.3μm of SiC at the top of source mesas.

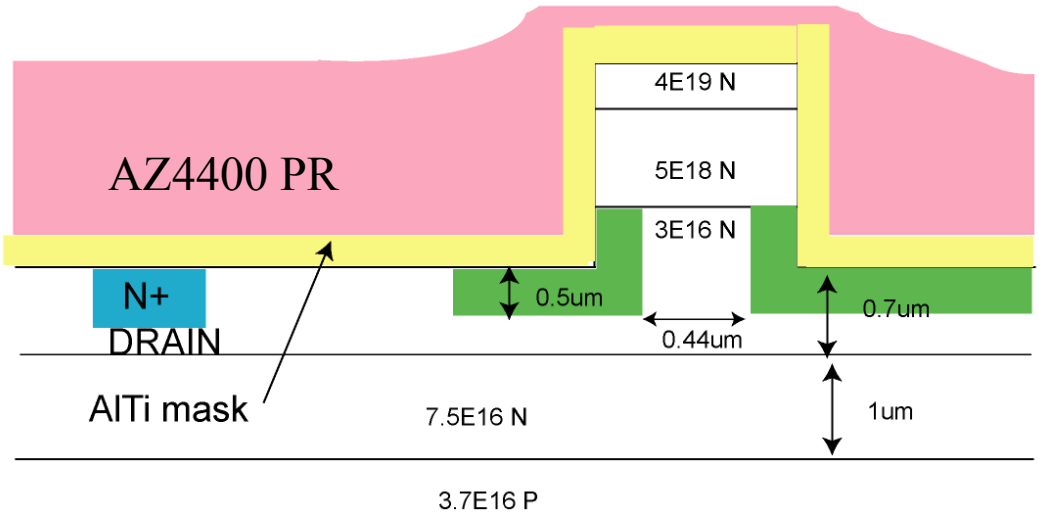


Fig. 3-12 (a) AZ4400 photoresist coated on the wafer

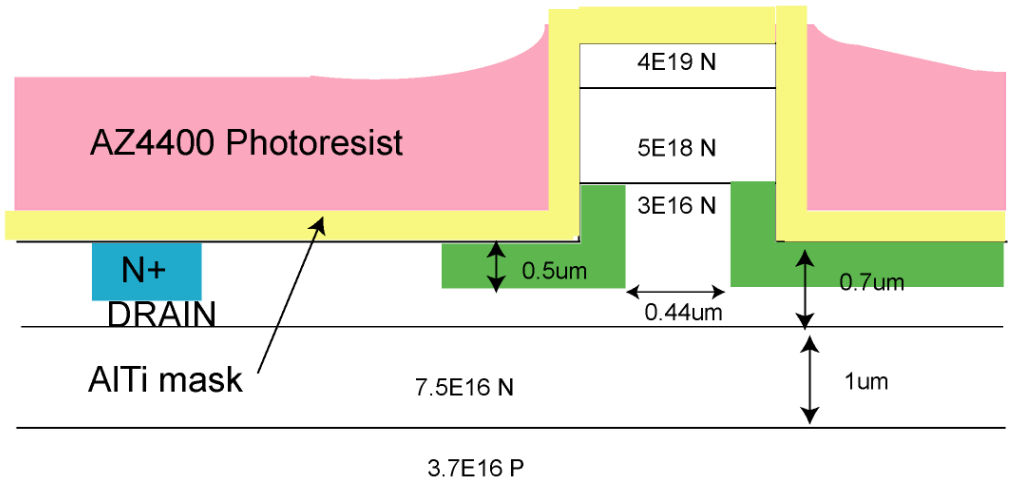


Fig. 3-12 (b) Photoresist etch back by O_2 ICP plasma to expose mesa tops

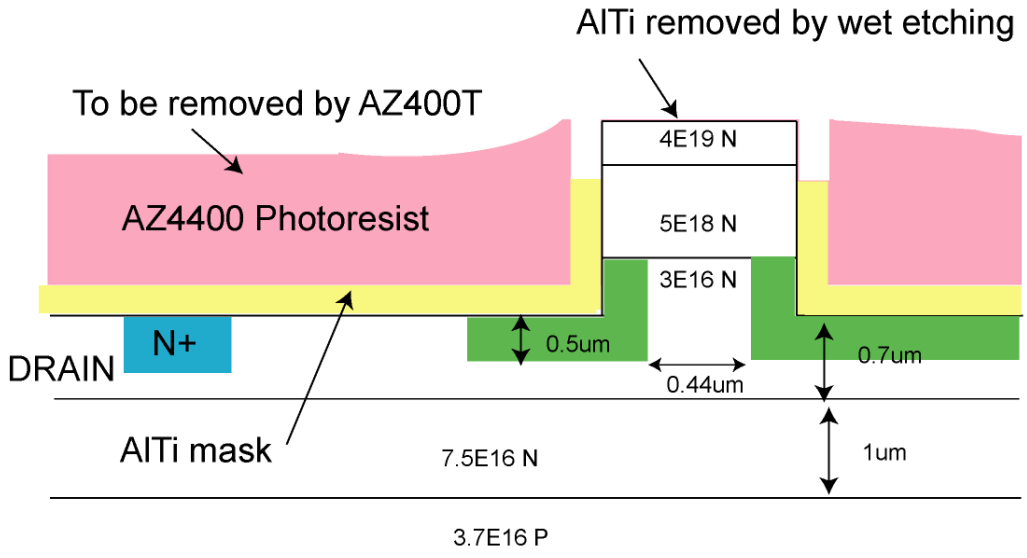


Fig. 3-12 (c) Wet etching of AlTi masking layer on mesa top

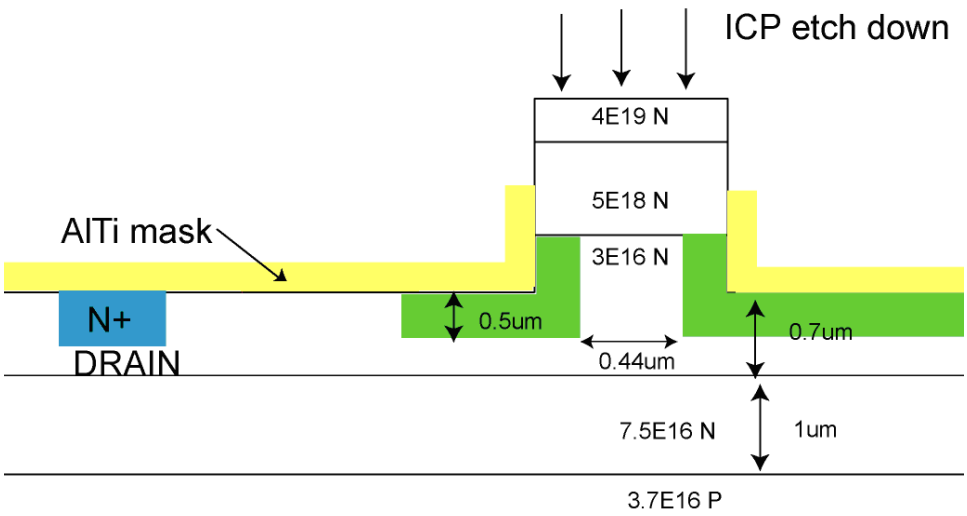


Fig. 3-12 (d) SiC mesa top etching in CF_4/O_2 plasma

Fig. 3-12 Mesa top removal procedure

As explained above, the new process eliminates a photoresist planarization and lift-off compared to the original TI-VJFET's, but needs an additional planarization and wet etching here for mesa top removal. So what makes the new process advantageous? The primary reason lies in the process difficulty. To lift off a thick layer of metal on small-dimensioned features like the JFET mesas is very challenging. In comparison, the wet etching removal of AlTi after photoresist planarization is easier and less likely to cause problems.

3.2.8 Oxidation and Passivation

After a complete sequence of wafer cleaning by sulfuric acid, RCA and hydrofluoric acid, sacrificial oxidation is performed for 0.5 hour at 1100^{o}C in wet oxygen. The thin

oxide is then removed by diluted hydrofluoric acid, together with certain surface defects and damages caused by ion implantation and plasma etching processes. Immediately after that, the wafer is reloaded to the oxidation chamber for surface passivation, a 2-hour procedure at 1100^{o}C to form a permanent layer of thermal SiO_2. The chemical reactions responsible for SiC oxidation include: [44]

$$SiC + 3/2\ O_2 \rightarrow SiO_2 + CO \tag{3.5}$$

$$SiC + O_2 \rightarrow SiO_2 + C \tag{3.6}$$

The SiC-SiO_2 interface in SiC JFETs is not critical as compared to SiC MOSFETs. While carbon clusters and other defects formed during the oxidation process may be a serious concern for SiC MOSFETs [44, 50], it does not pose a problem for the VC-LJFETs.

Following the oxide passivation, a 200nm layer of PECVD silicon nitride is additionally deposited. Silicon nitride is commonly used to passivate silicon devices because it provides an extremely good barrier to the diffusion of water and sodium. [10] These impurities cause devices to corrode or become unstable. For the SiC VC-LJFETs, we employ the nitride layer as a protection for the lateral drift region.

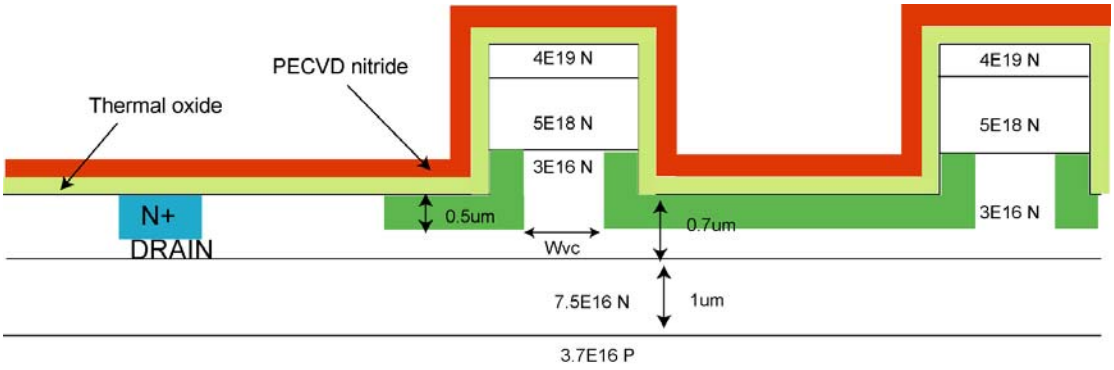


Fig. 3-13 Passivation by thermal oxide and PECVD nitride

It is interesting to note that the PECVD method provides an excellent platform for low-temperature deposition of the dielectrics, compared to LPCVD. [10] However, the silicon nitride layer deposited by PECVD usually contains a significant amount of hydrogen. These thin films typically have less tensile stress but also dielectric strength. The overall reaction of this PECVD process can be expressed by the following equation: [51]

$$SiH_4 + NH_3 \text{ or } N_2 \rightarrow Si_xN_yH_z + H_2 \quad (3.7)$$

3.2.9 Ohmic Contacts

Ohmic contacts to the VC-LJFET source, gate and drain electrodes are formed by the self-aligned Ni process after opening windows in the passivation layers. The complete procedure is described as the followings.

First, the PECVD nitride layer is thoroughly cleaned from the mesa/trench region to avoid its reaction with Ni during the ohmic contact annealing. This is accomplished by a

10mtorr 0V CF_4 plasma etching with thick photoresist (AZ4400) mask. The self-aligned Ni contact process then starts with the deposition of 200nm PECVD SiO_2 in a gas mixture of silane (SiH_4) and nitrous oxide (N_2O). The oxide layer is then patterned by ICP etching to expose the mesa tops and gate contact windows. 100nm Ni is sputtered on the wafer, and annealed at 750°C to form silicide in the contact holes. Sulfuric acid with hydrogen peroxide then removes unreacted Ni, followed by high-temperature annealing at 1000°C in argon forming gas to complete the ohmic contact formation. At this point, the VC-LJFETs have a cross-sectional structure as in Fig. 3-14. For more details on the self-aligned Ni contact process, please refer to Chapter 2 of this dissertation.

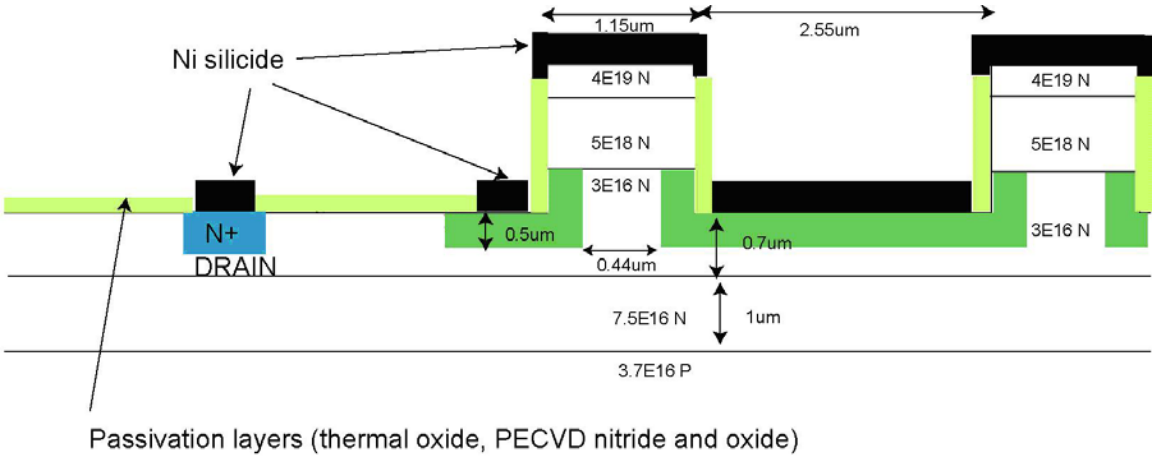


Fig. 3-14 Cross-sectional view after ohmic contact formation

3.2.10 Gate and Drain Metal Thickness Enhancement

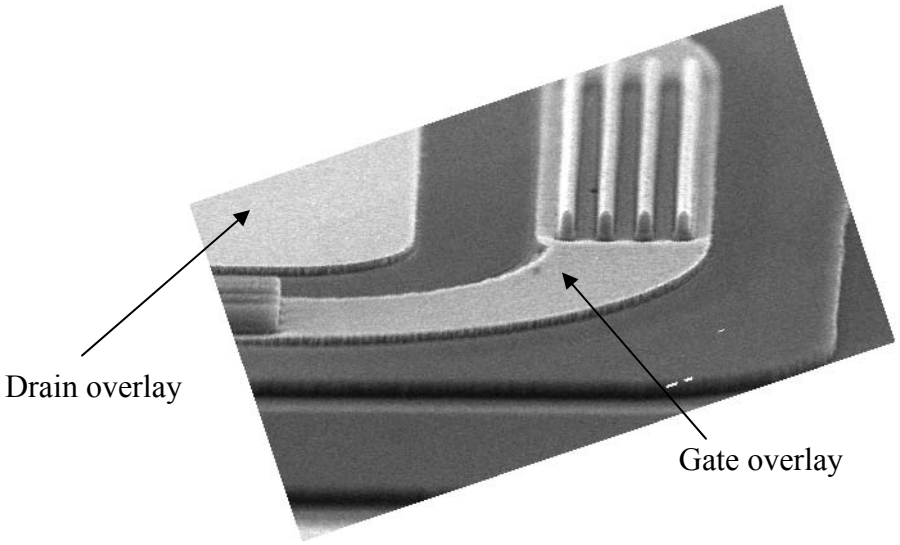


Fig. 3-15 Gate and Drain contact overlay (SEM picture)

To reduce gate and drain contact resistances, 1μm molybdenum (Mo) overlay is added onto the gate and drain contact silicide by sputtering, lift-off and wet etching. In particular, the removal of Mo on mesa tops and sidewalls is accomplished after a photoresist planarization and etchback procedure. Fig. 3-15 shows the SEM image of a VC-LJFET device with overlay added to gate and drain contacts. The sequence of process is illustrated in Fig. 3-16.

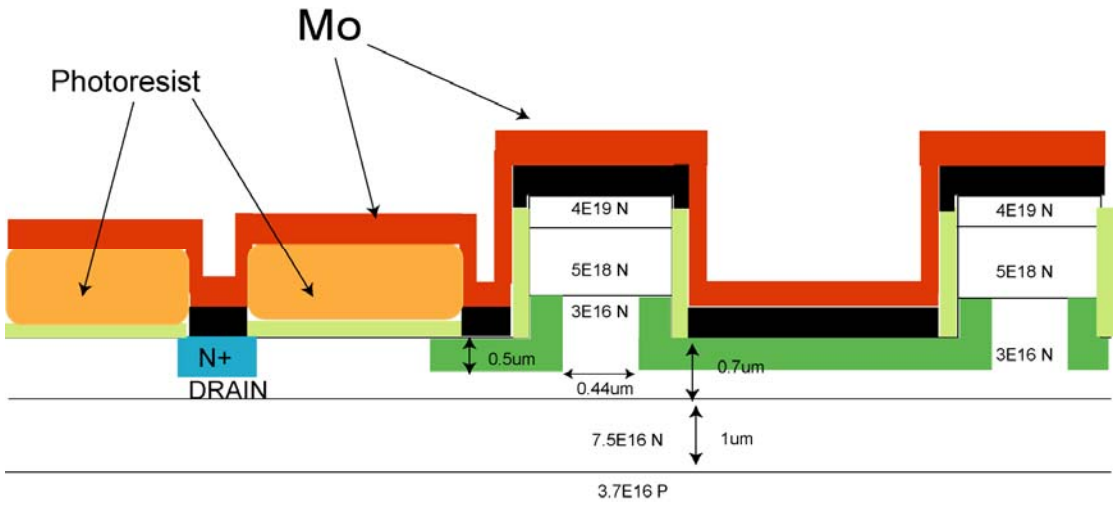


Fig. 3-16 (a) Photoresist patterns defined for Mo liftoff,

and then Mo sputtered on the wafer

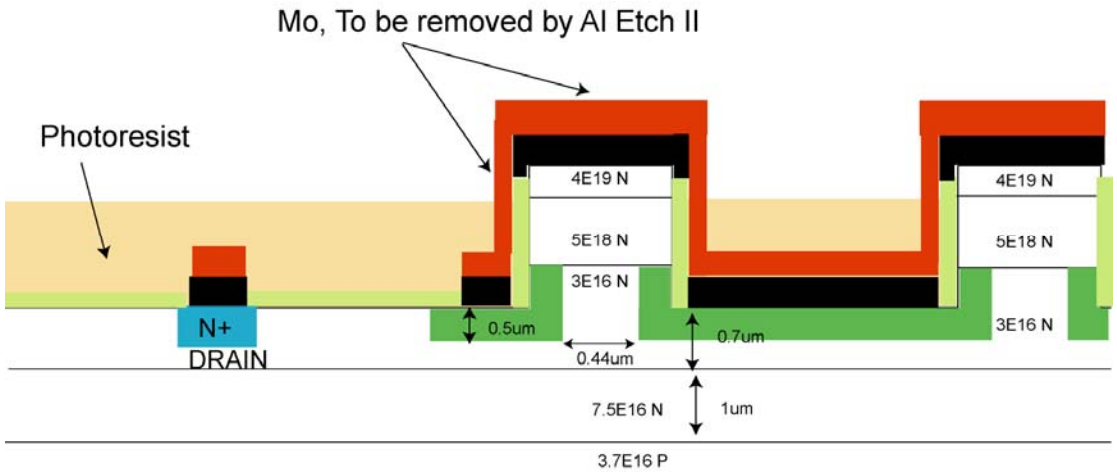


Fig. 3-16 (b) After Mo lift-off, a photoresist planarization and etchback

is performed until the mesa tops are exposed

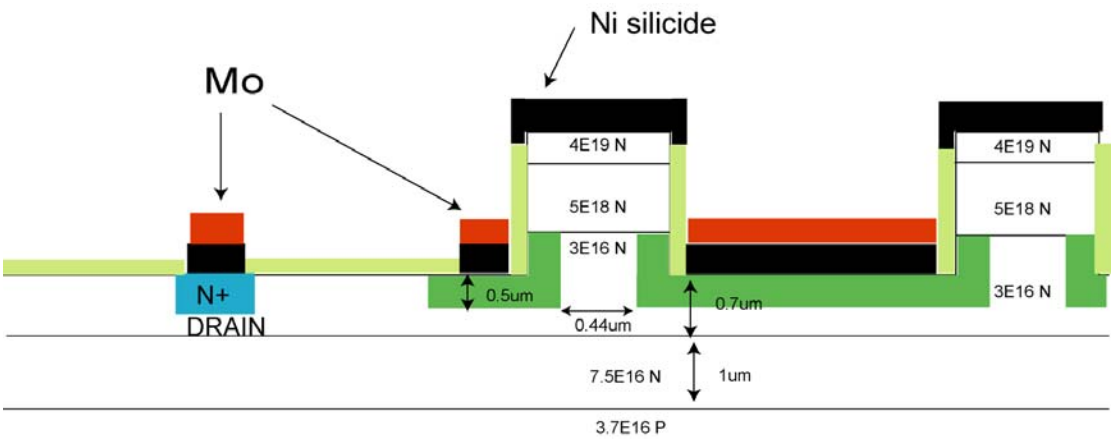


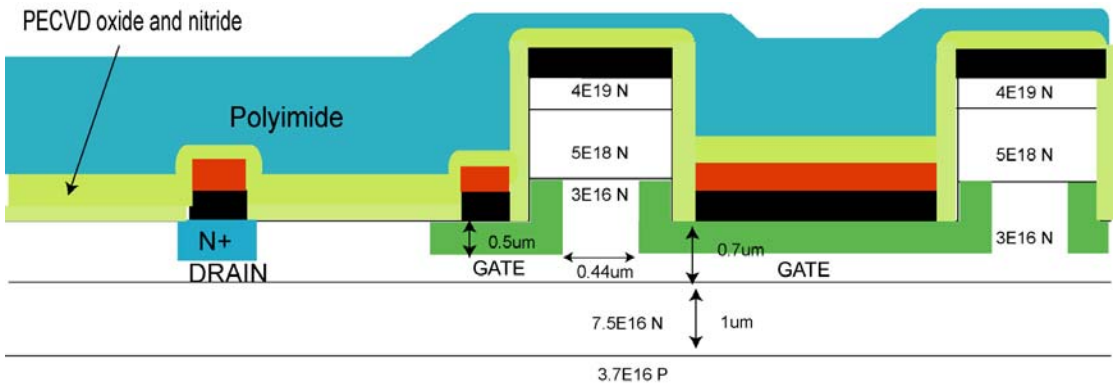
Fig. 3-16 (c) Mesa top and sidewall Mo removed by wet etching, photoresist stripped

Fig. 3-16 Gate/drain metal thickening process

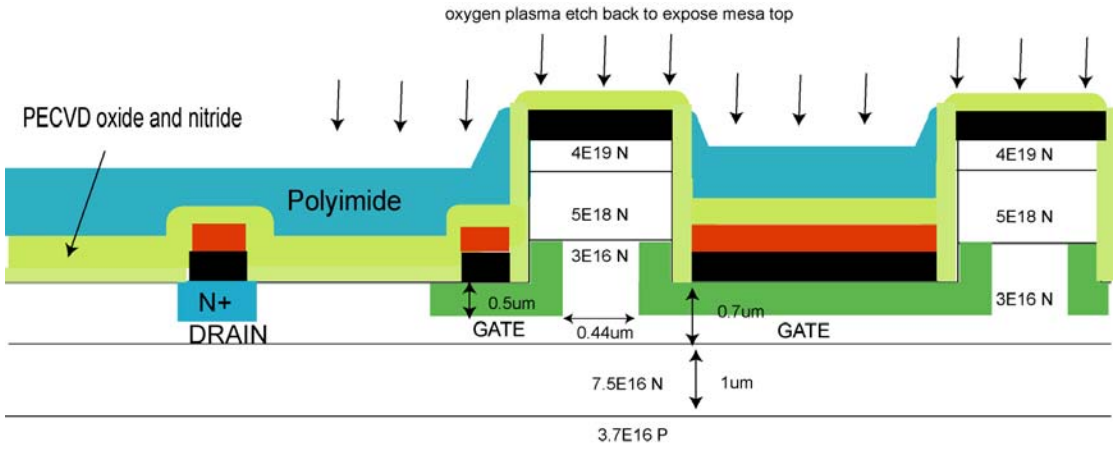
The metal thickening step is sometimes a troubling procedure, making the gate and source electrodes prone to shorting. Therefore this step is sometimes skipped in order to improve the process reliability.

3.2.11 Interlayer Dielectrics (ILD) and Trench Fill

PECVD dielectric layers consisting 200nm SiO_2 and 200nm silicon nitride are deposited to provide insulation for the metal overlayers. Then a polyimide layer film is coated onto the wafer to fill up the trenches. To allow overlay access to the mesa tops, the polyimide film is etched back in oxygen plasma until the source contacts are exposed. Fig. 3-17 visualizes the above process.



(a) Cross-sectional view after polyimide coating



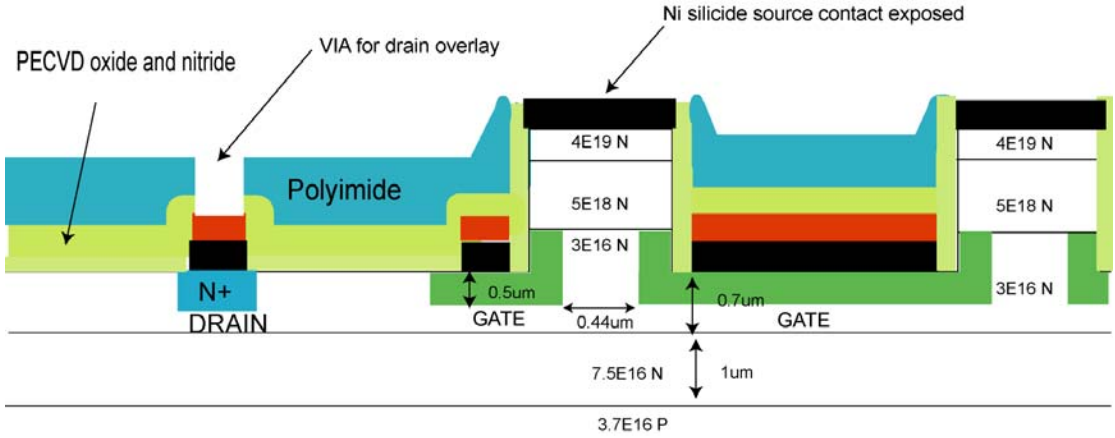
(b) Cross-sectional view after polyimide etchback

Fig. 3-17 PECVD dielectrics and polyimide trench-fill

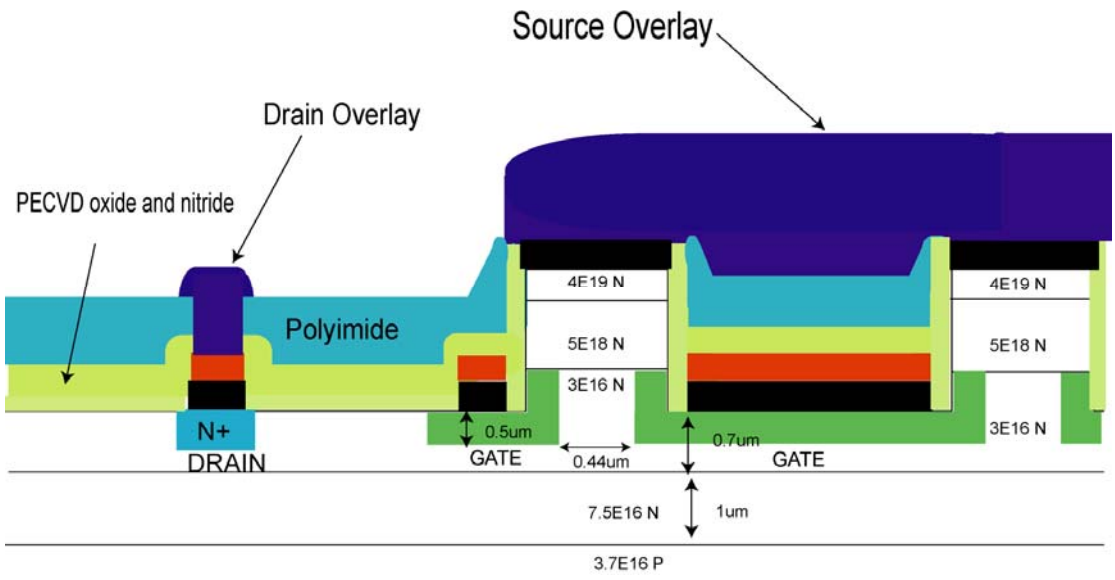
3.2.12 VIA Opening and Metal Overlay

Before the final overlay, the remaining insulating layers (PECVD oxide, nitride and polyimide) are removed from the mesa tops, and the designated gate, drain and isolation VIA windows by ICP etching. A final overlay of thick aluminum is then deposited and patterned by wet etching to provide all the electrical connections, including joining all the mesa tops to a common source probing pad. Fig. 3-18 is a cross-sectional view of the

device after final overlay. Fig. 3-19 shows a finished power VC-LJFET device in SEM, with gate, source and drain pads labeled.



(a) VIA opening before overlay



(b) Deposition and patterning of final overlay

Fig. 3-18 Schematic of VC-LJFET overlay process

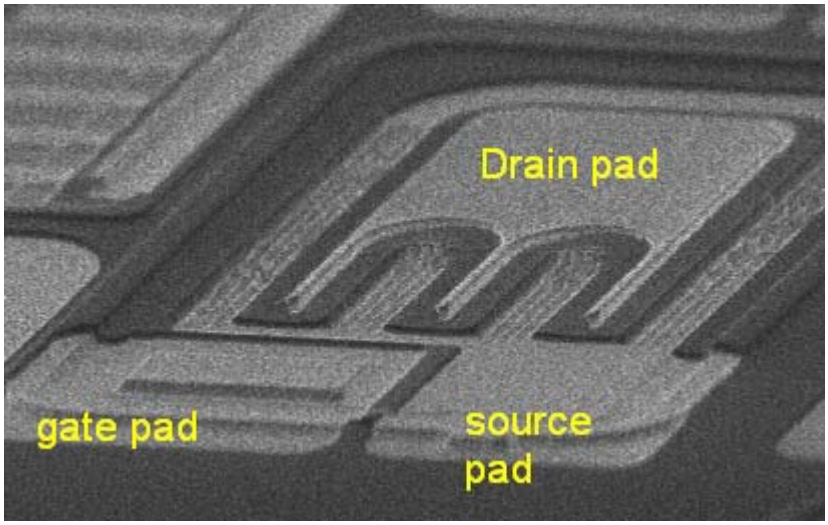
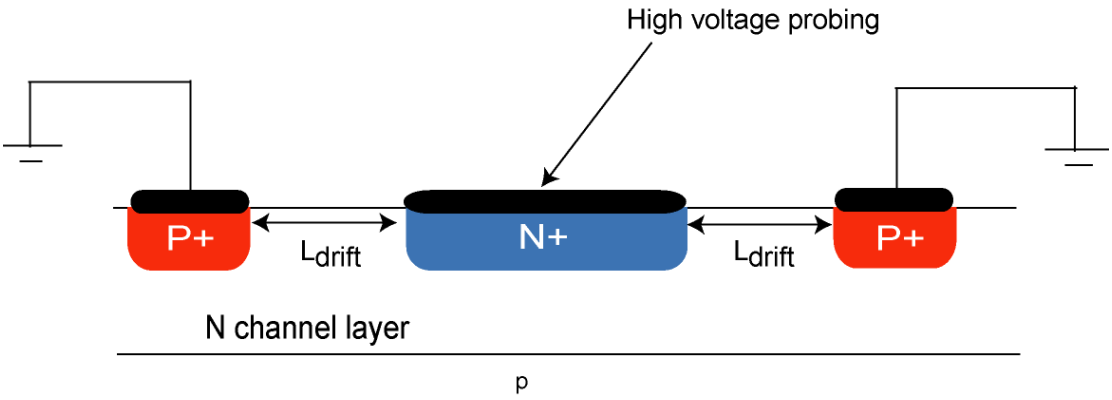


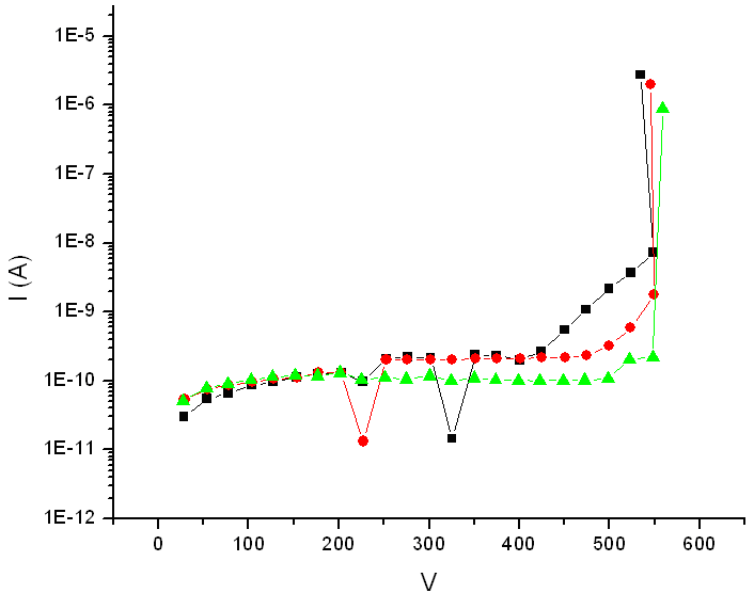
Fig. 3-19 SEM image of a VC-LJFET after overlay

3.2.13 Device Testing Results

The devices are immersed in Fluorinert to prevent air breakdown during the blocking tests, and characterized on a either a Glassman high-voltage test system or a Tektronix 370 curve tracer. The blocking voltage test is first performed on lateral diode patterns, which is free from the source mesa and JFET channel complications. These diodes have the same lateral drift length as the VC-LJFETs, and are found to block 400V~600V with low leakage current. Fig. 3-20 shows the test setup and a few blocking test data.



(a) Diode blocking test setup



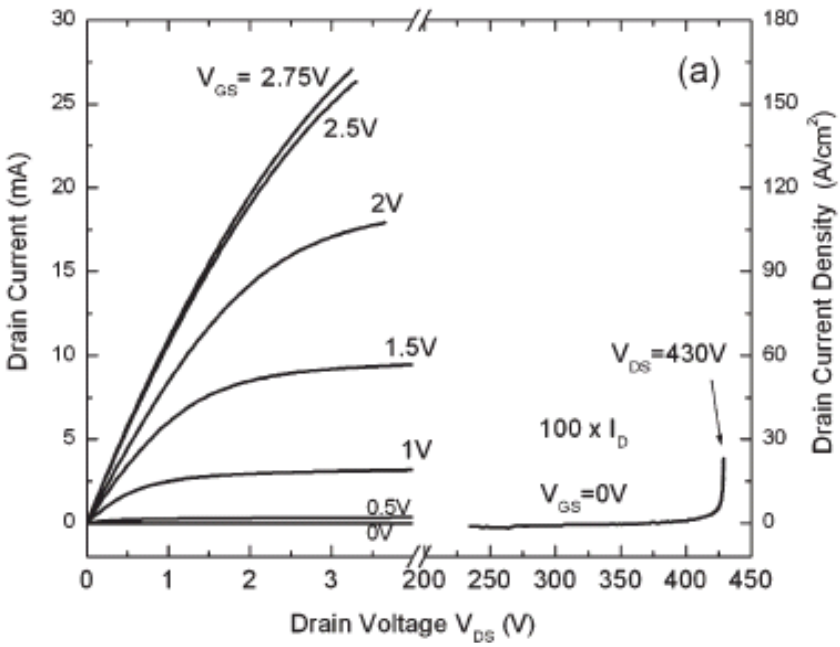
(b) Blocking voltage tests on three diode patterns

Fig. 3-20 Diode blocking test

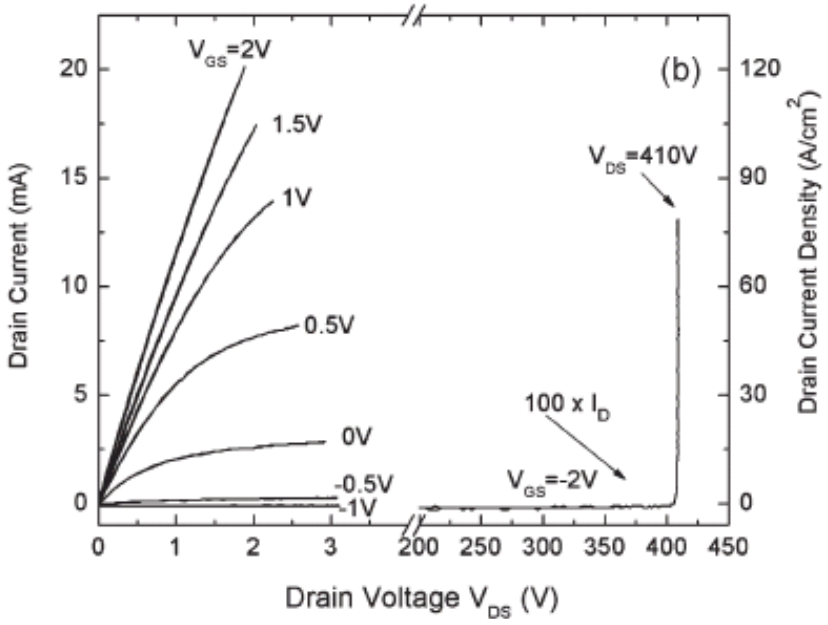
After confirmation of the voltage blocking capability from test diodes, the power VC-LJFETs are characterized for both forward conduction and blocking voltages. Forward characterization is performed on an HP 4145B semiconductor analyzer (small devices) or a Tektronix curve tracer.

Fig. 3-21 (a) shows the characteristics of drain current I_{DS} versus drain voltage V_{DS} of a normally-off VC-LJFET. [36] This device is able to block 430V with a V_{GS} of 0V. The on-resistance measured at V_{GS}=2.75V and V_{DS}=1V is 74.8Ω after deduction of a 9 Ω parasitic resistance from the test setup. Gate current is found to be only 60μA. The n+ substrate and the p-region beneath the drift layer are grounded during these measurements. Taking the device active area into consideration, the specific on-resistance is 12.4mΩ·cm^2, giving a FOM of 15MW/cm^2. In calculating the active device area, drain N+, gate P+ and source N+ regions are all included except the bonding pads. The threshold voltage is found to be around 0.4V. Fig. 3-21 (b) shows a nearly identical device to the normally-off one but with 0.15μm wider vertical channel opening (W_{VC}). This JFET is normally on with a threshold voltage of –0.6V and blocks 410V with a negative gate bias. As predicted by computer simulation, it is also experimentally verified for this device structure that the gate threshold voltage is sensitive to the W_{VC} parameter, but the blocking voltage is not significantly affected by the vertical channel as long as a sufficient gate bias is applied to keep it off.

Besides the small-sized JFET described in Fig. 3-21, some medium-sized power devices are also found functional in the first batch fabrication of power VC-LJFET. These larger devices have nearly the same blocking voltage but higher specific resistance. Fig. 3-22 shows the characteristics of a medium-sized JFET of 4x10^{-3} cm^2.



(a) 430V Normally-off power VC-LJFET



(b) Normally-on device with channel width 0.15μm wider.

Fig. 3-21 measured dependence of drain current vs. drain to source voltage

(Devices have an active area of 1.66×10^{-4} cm^{-2}.)

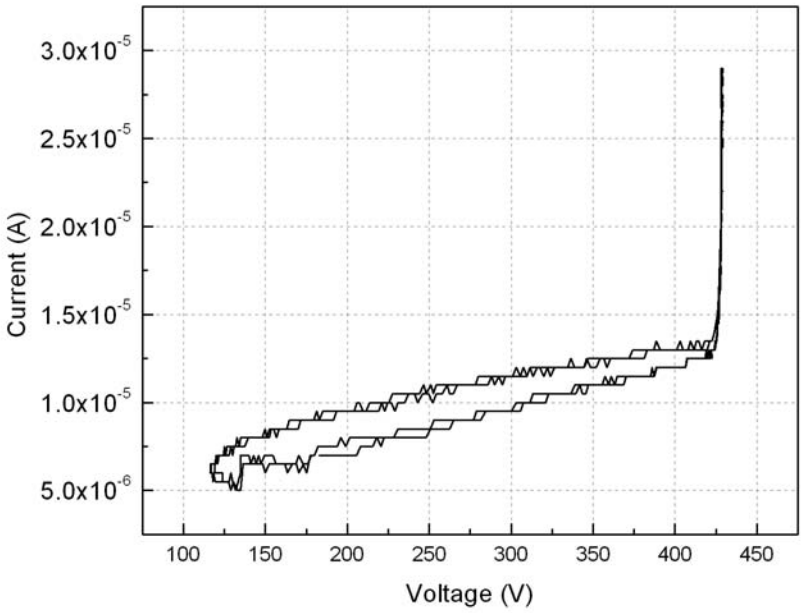


Fig. 3-22 (a) Blocking voltage test (medium-sized power VC-LJFET)

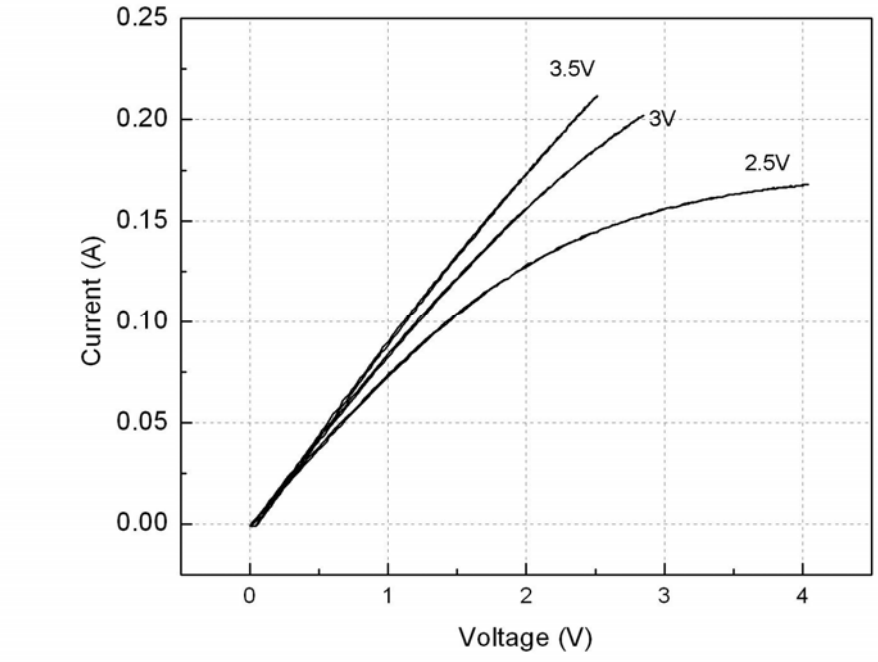


Fig. 3-22 (b) Device on-current tested to 0.2A

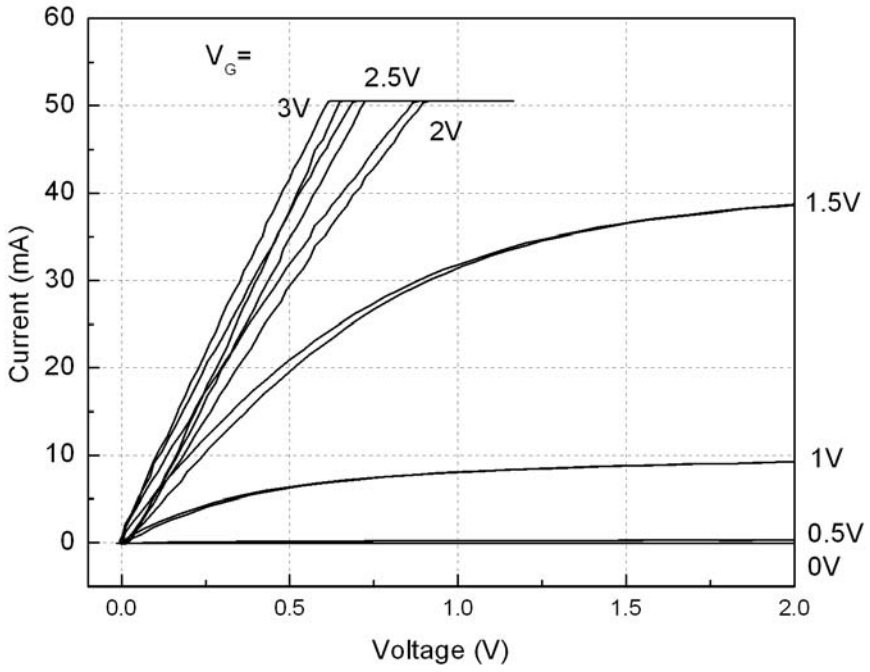


Fig. 3-22 (c) Forward characteristics (current limit set at 50mA)

Fig. 3-22 Characterization of a medium-sized power VC-LJFET

3.3 Summary and Discussion

In the first batch fabrication of power VC-LJFETs, the entire process is explored and the device design is experimentally demonstrated. Novel procedures including the Ni self-aligned ohmic contact scheme are confirmed. The reported 12.4mΩ·cm^2 normally-off power VC-LJFET nearly achieved the theoretical specific on-resistance but the breakdown voltage is yet to be optimized. It is worth noting that only 5μm drift-region distance was used effectively in voltage blocking, due to misalignment of multiple mask layers. The functional medium-sized device indicates the feasibility of pushing the VC-LJFETs to

larger area and power handling capacities. This first fabrication also verified that the device's gate threshold voltage is sensitive to the source mesa width. Mesa width control in experiment, as well as line width variation designed on mask is critical to achieve normally-off device operation. The 430V normally-off power VC-LJFET has a figure of merit of 15 MW/cm^2, making it one of the best-performing SiC lateral power devices as of the reported date. [36]

After the first VC-LJFET batch, continued efforts have been spent on the improvement of the power device's blocking capabilities. By introducing the top implanted P RESURF region, the electric field crowding at the surface region can be substantially reduced. A subsequent batch of power VC-LJFET devices fabricated by a team partner Dr. Y. Zhang with my close collaboration confirmed that the higher breakdown voltages can be achieved by the RESURF optimization. [52] The full RESURF version of the power VC-LJFETs boosts the device figure-of-merit over 7 times to 116 MW/cm^2.

In summary, the combined efforts of the first-batch power VC-LJFET fabrication and the subsequent RESURF optimization done by the Rutgers SiCLAB team demonstrated the theoretical potential of the VC-LJFET device structure. While the first power VC-LJFET was found to have one of the best performances among SiC lateral power transistors, the enhanced results achieved with double RESURF termination place the power VC-LJFET structure in a leading position among these devices by a wide margin, as shown in Fig. 3-23. With the successful demonstration of 4H-SiC high-voltage

power VC-LJFETs, low-voltage driver and control circuits based on devices of the same JFET structure targeting monolithic power integration become increasingly attractive to investigate.

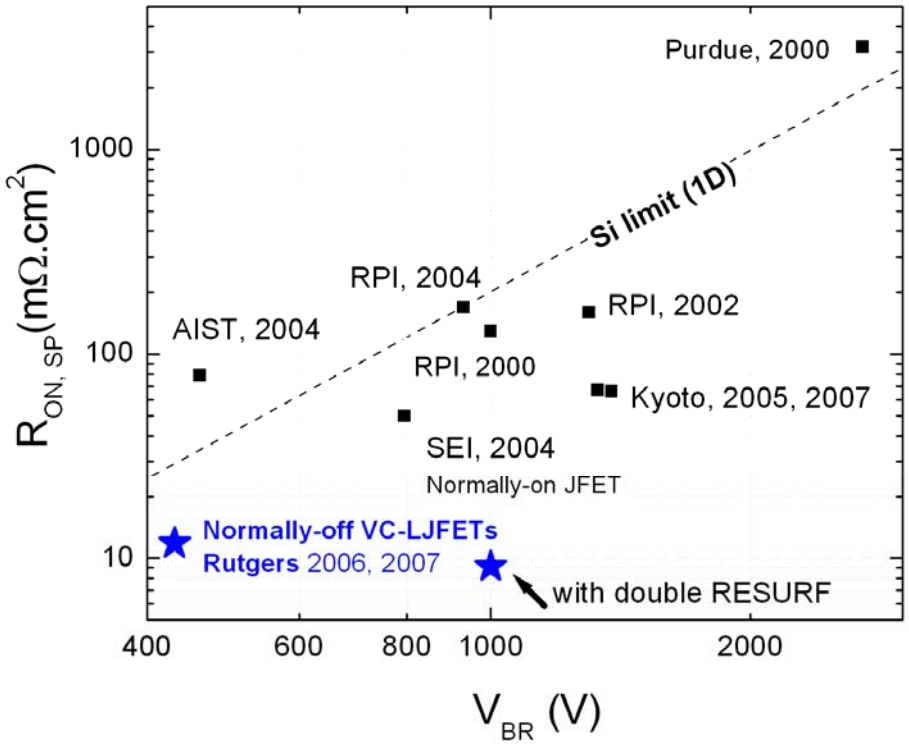


Fig. 3-23 Performance of power VC-LJFETs vs. other SiC lateral devices

CHAPTER 4 DEVELOPMENT OF LOW-VOLTAGE INTEGRATED DRIVERS

4.1 Principles of Super Buffer Drivers

The ultimate goal of the VC-LJFET technology development is the realization of a power electronics systems-on-chip (SoC). Among many components required for a power IC system, the power transistor and its on-chip gate drive/control unit are considered most valuable. Due to the relatively large size of the power switching transistor, it presents itself as a significant capacitance. On the other hand, the on-chip input signal used to control the power switch usually comes from a low-power logic circuit of very limited current-driving capability. In order to interface the logic control components and the power devices, a gate drive buffer needs to be developed to allow fast switching of the power JFET.

The simplest gate buffer can be made by using a single logic inverter between the input signal and the power device. Assuming the control circuit, the buffer and the power device are all based on the same device technology, if the area ratio between the power device and the logic circuit's output stage is *x*, then the optimal area ratio between the buffer inverter and the power device for minimized propagation delay is given by $\sqrt{x}$. [53] When the ratio *x* is very large, a single inverter stage becomes insufficient. A more powerful approach is to use a chain of multiple-stages logic inverters. The first inverter stage of the buffer has to be reasonably small to avoid excessive delay caused by the capacitive loading effect to the preceding signal generation unit. On the other end, the

output of the last inverter stage is connected to the power device and is used to supply a strong charging/discharging current to the gate terminal. Therefore the last stage needs to be of significant size to fulfill the current drive requirements. A multiple-stage buffer is hence designed to include inverter stages of increasing size and current drive capabilities. Fig. 4-1 illustrates the buffer circuit logics. If the area scaling factor between two neighboring inverter stages is u, and the number of buffer stages is N, then

$$N = \frac{\ln(x)}{\ln(u)} \tag{4.1}$$

and the minimal total propagation delay is achieved when [53]

$$u_{optimal} = e = 2.718 \tag{4.2}$$

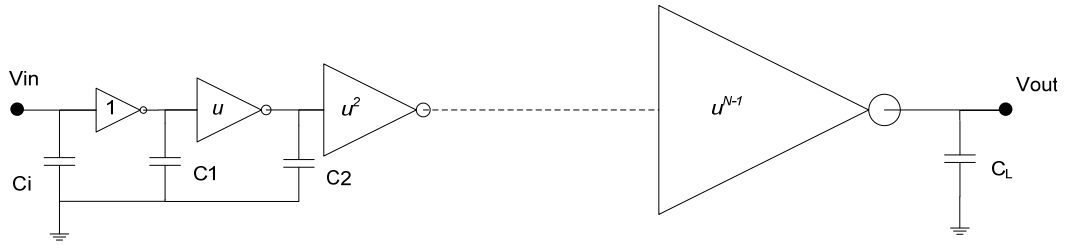


Fig. 4-1 N-stage buffer

In practice, a scaling ratio of 3 to 5 is almost equally efficient and also helps reduce the required number of stages and the chip area. Another important requirement for the stable buffer functioning is that the logic inverters used in the circuit must be able to cascade indefinitely.

4.2 Review of the First Demonstration of LJFET-based Buffer Driver and Power IC

The first VC-LJFET based power integrated circuit was experimentally demonstrated by the Rutgers SiCLAB team including myself in 2008. [54] The gate drive buffer has four stages of logic inverters with a scaling ratio of 5. As shown in Fig. 4-2, each of the inverter stages consists of a low-voltage normally-off VC-LJFET and a matching resistor.

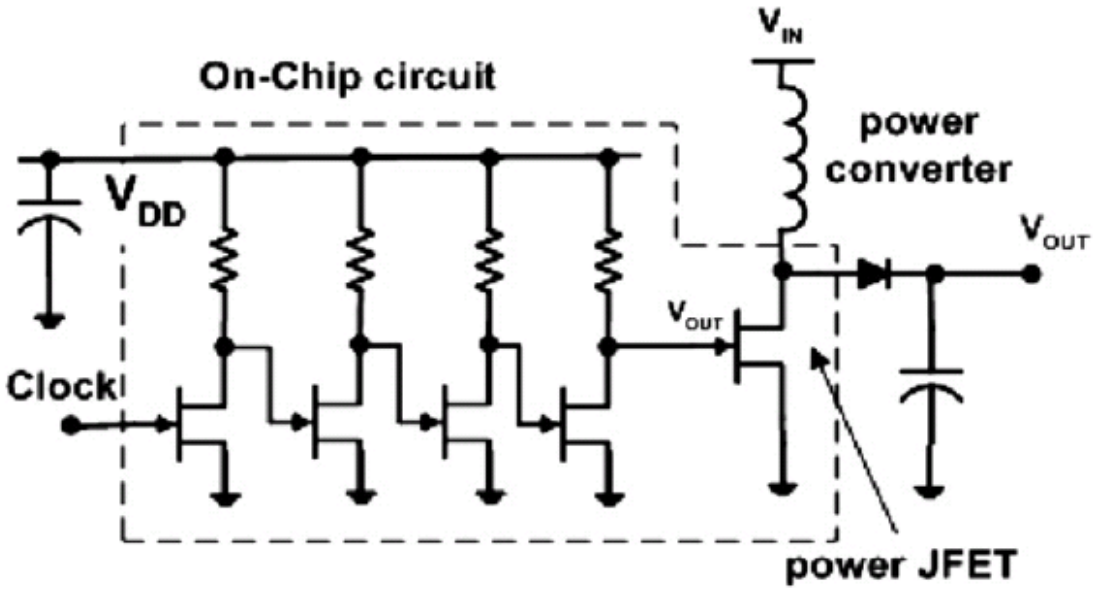


Fig. 4-2 The first SiC Power IC based on a power VC-LJFET

and integrated resistor-load inverter buffer driver

The resistor-load inverter based buffer driver is monolithically integrated with a power VC-LJFET. After on-chip probe testing, a functional integrated circuit is diced from the SiC wafer and mounted on a hermetic package by silver nano paste. The electrical access to the SiC circuits is accomplished by gold wire bonding. A photo of the packaged SiC IC is shown in Fig. 4-3. The SiC chip is then connected to an external

inductor, a SiC diode, and a capacitor in a DC-DC boost converter configuration, as in Fig. 4-2. Dynamic test on the SiC power IC confirmed its capability of operating at 1MHz, 200V and 2A. [54]

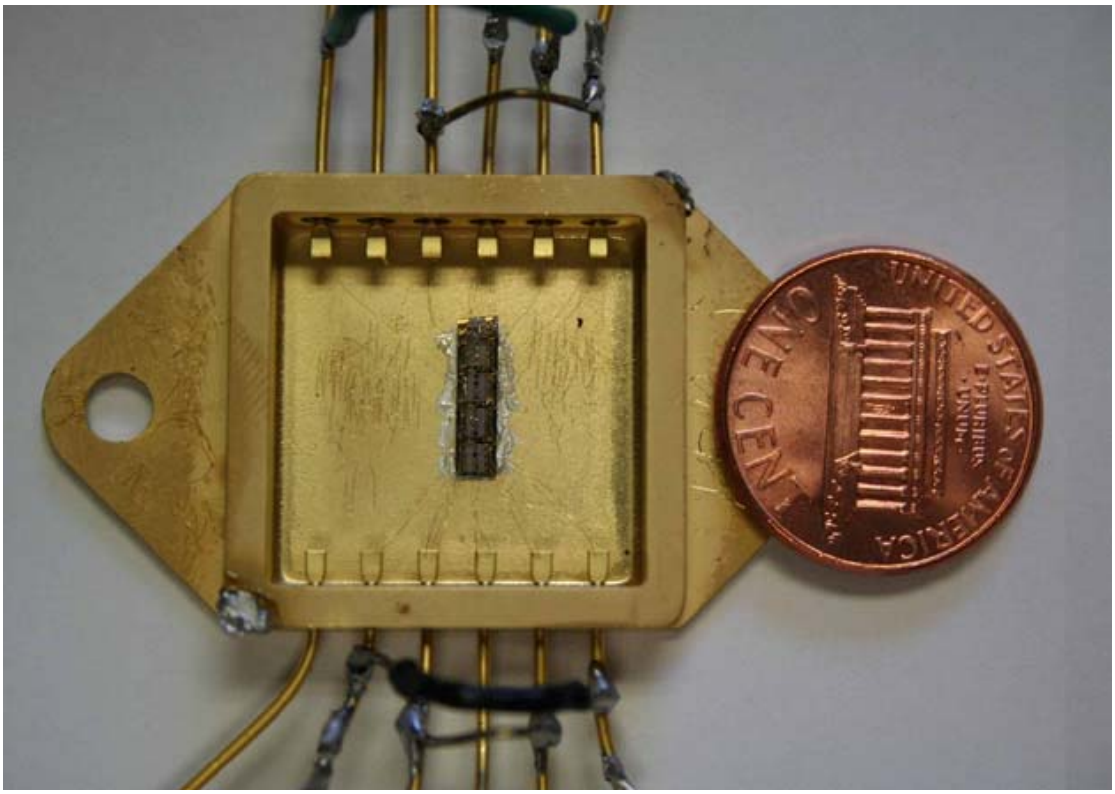


Fig. 4-3 An optical photo of the SiC power integrated circuit

4.3 Motivation for the Improved Driver Design and Configuration

While high frequency switching of the first VC-LJFET based power IC has already been demonstrated, the buffer driver design and optimization is yet to be fully explored. Besides the need to model and thoroughly investigate the circuit's functionality and toleration of variations, this is an opportunity to bring the circuit performance to another level by revisiting the design of the logic inverters. After all, it is no secret that inverters

based on the resistor-transistor logic are obsolete in silicon industry and have been superseded by more advanced logic configurations as far as 30 years ago.

Similar to silicon technology, the most preferred choice for SiC inverters is to employ complementary pairs of transistors in a CMOS logic configuration. In such scenarios, zero static power loss can be achieved thanks to the alternating on and off states of the pairing transistors. In reality, the state-of-the-art silicon CMOS technology is by no means easy in SiC. While a SiC CMOS approach has been reported in [55], the very low hole mobility in the PMOS makes it unsuitable for practical design requirements.

Historically, silicon-based logic inverter circuits evolved from resistive-load NMOS logic, to a "high-performance" or depletion-load NMOS logic before the CMOS technology matured. In the latter circuit, normally-on transistors with shorted gate and source electrodes are fabricated to replace the load resistors, like in Fig. 4-4. This advance was originated from the attention on the high resistance required for the load resistor in an inverter and the slow low-to-high transition it causes. The high resistance is necessary because when the transistor is turned on, most of the V_{DD} voltage drop has to be on the resistor in order for the inverter to output a proper V_{OL} level. This in turn limits the current through the resistor when the transistor is switched off, making the available current for charging the next-stage gate capacitance low.

When a depletion-mode transistor is used as the load in an inverter, the transition speed problem can be significantly improved by the load transistor's non-linear current characteristics. As an inverter's output terminal charges up, the current through a resistor

load steadily decreases as the output voltage increases. In contrast, the current through an ideal depletion-mode transistor remains constant, thanks to its current saturation characteristics. An ideal current source in place of the load resistor could reduce the required charging time by more than half. In a properly designed depletion-load inverter, a significant portion of this speed benefit can be realized.

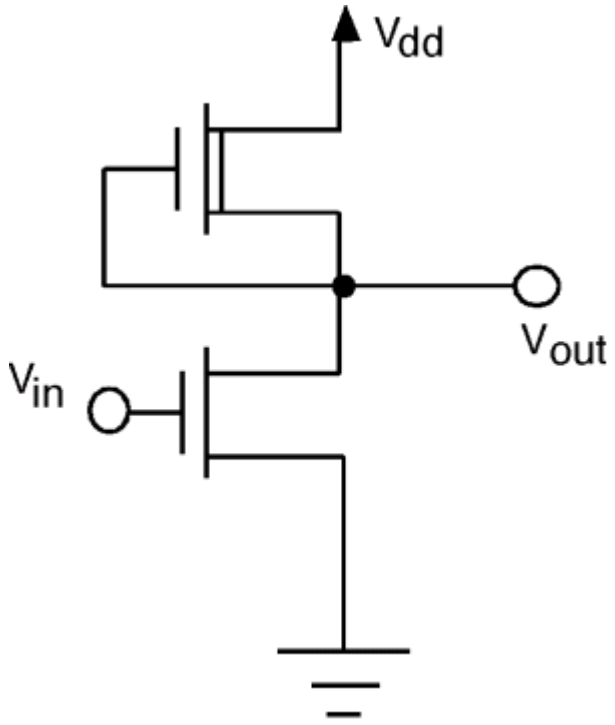


Fig. 4-4 Logic inverter based on a depletion-mode transistor load

In addition, a depletion-mode VC-LJFET is essentially the same structure as the enhancement-mode VC-JFET already fabricated in the driver except for a slightly varied vertical channel width (Wvc). Inclusion of such devices into the buffer circuit does not require additional process development. By eliminating the need for on-chip resistors, we

also avoid the processing uncertainties and variations that are specific to them. This provides an additional bonus from a design and manufacture perspective.

In the following section, modeling and optimization work on the SiC VC-LJFET based buffer driver circuits will be presented. Both resistor-load and JFET-load cases are simulated in a DC-equivalent fashion. A dynamic performance comparison is then summarized and discussed.

4.4 Design and Comparison of Depletion-load and Resistor-load Buffer Drivers

4.4.1 Numerical Device Modeling and Circuit Parameter Extraction

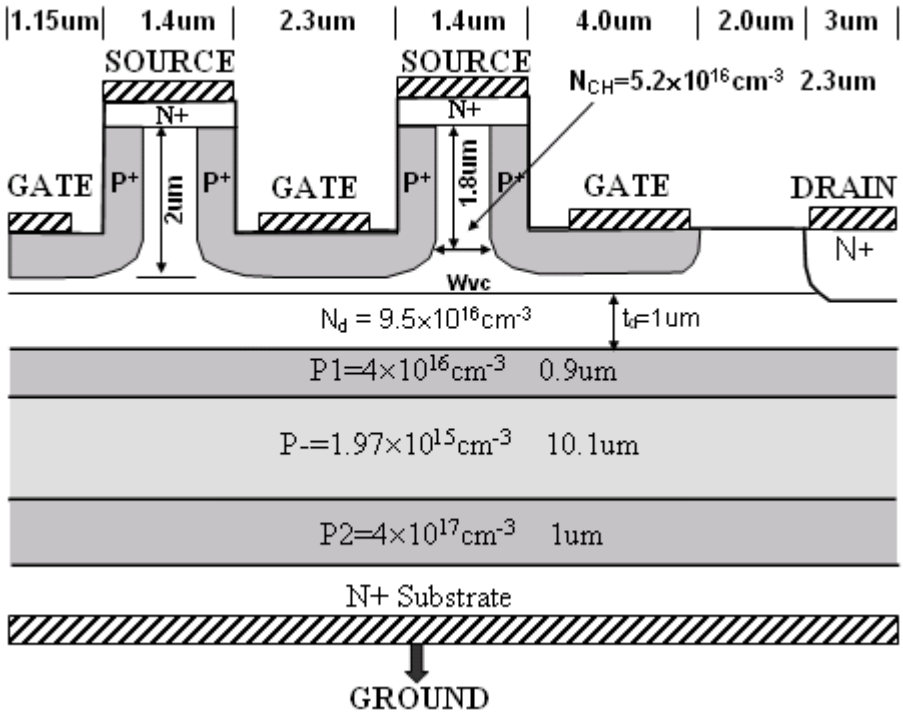


Fig.4-5. Cross sectional view of LV VC-LJFET

The low-voltage (LV) VC-LJFET structures are evaluated with a numerical simulator, courtesy of Dr. Xueqing Li at United Silicon Carbide, Inc. Fig.4-5 shows the LV LJFET device cell structure.

In the numerical analysis, electron mobility in vertical channel is assumed as 500 cm^2/Vs. Threshold voltages are measured at drain current density of $1x10^{-3}$ A/cm^2 when V_d=0.5V. For the enhancement-mode LJFET, the vertical channel opening (Wvc) is set at 0.36 μm, which corresponds to a threshold voltage of 0.54V. A series of 10 Wvc values are considered for the depletion-load LJFETs, covering the threshold voltage range -1V to -10V. For the depletion-mode VC-LJFETs, the dependence of the threshold voltages (Vth) on Wvc at room-temperature and 200°C is shown in Fig.4-6.

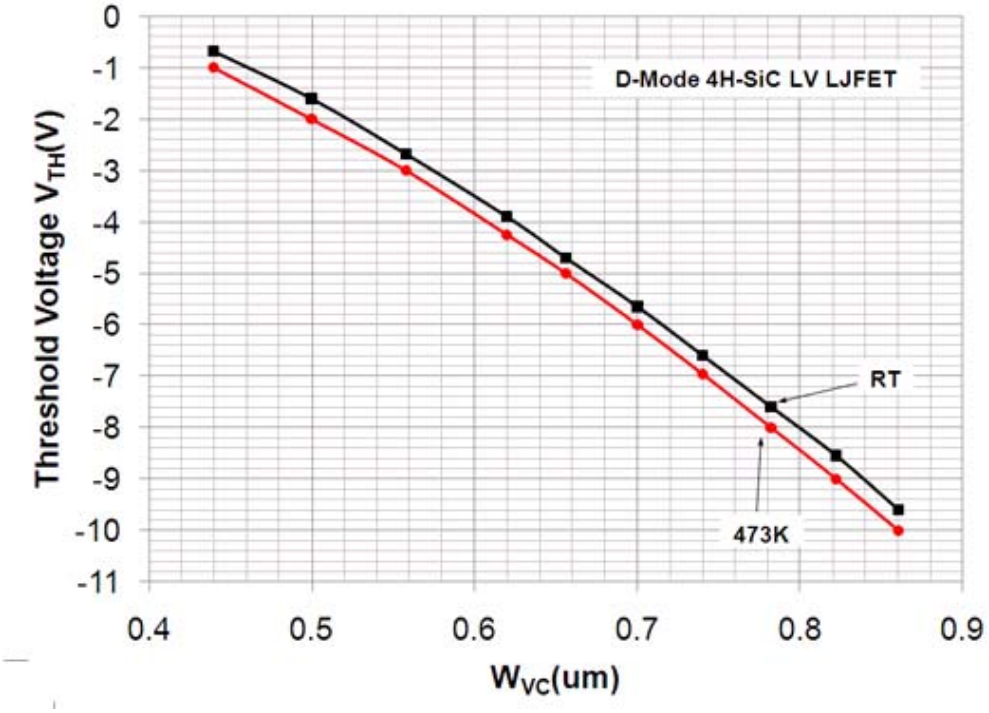


Fig. 4-6. Vth dependence on. Wvc for depletion-mode LV VC-LJFET

For each of the simulated LV-LJFETs, the I_{ds} *vs* V_{gs} and I_{ds} *vs* V_{ds} characteristics are extracted, along with the parasitic capacitances (Cgs, Cgd and Cds) as functions of the bias voltages. These numerical simulation data provide the foundation for modeling these LV-LJFETs in circuit-level simulators (PSPICE). After proper parameter fittings, compact models for the JFET devices can be developed, facilitating the buffer circuit simulation on PSPICE.

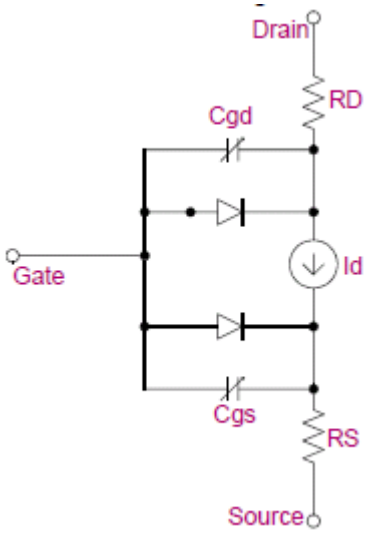


Fig. 4-7 JFET model in PSPICE

In PSPICE, a JFET device is considered as an equivalent of the circuit shown in Fig. 4-7. To reproduce the JFET's numerically simulated current and capacitive characteristics on PSPICE, several parameters can be customized. The equations governing JFET's *I-V* operation in PSPICE include:

Gate-to-source current:

$$\text{Igs (normal current)} = \text{IS}\cdot(e^{\text{Vgs}/(\text{N}\cdot\text{Vt})}-1) \qquad (4.3)$$

Drain currents:

for cutoff region: Vgs-**VTO** < 0,

$$\text{Idrain} = 0 \tag{4.4}$$

for linear region: Vds < Vgs-**VTO,**

$$\text{Idrain} = \mathbf{BETA}\cdot(1+\mathbf{LAMBDA}\cdot\text{Vds})\cdot\text{Vds}\cdot(2\cdot(\text{Vgs}-\mathbf{VTO})-\text{Vds}) \tag{4.5}$$

for saturation region: 0 < Vgs-**VTO** < Vds,

$$\text{Idrain} = \mathbf{BETA}\cdot(1+\mathbf{LAMBDA}\cdot\text{Vds})\cdot(\text{Vgs}-\text{VTO})^2 \tag{4.6}$$

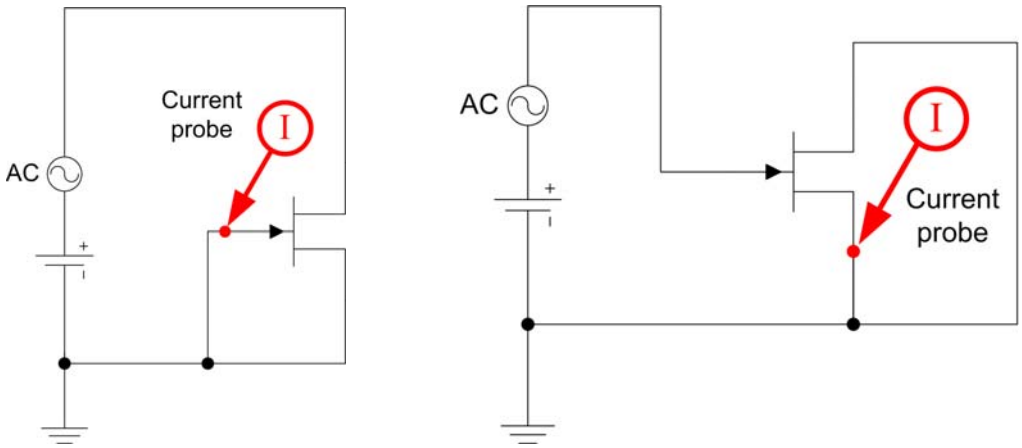
Based on these equations, the IS parameter is determined from the turn-on voltage of the G-S diode. BETA, VTO, LAMBDA and rd are obtained by fitting the Jds vs Vds and Jds vs Vgs curves of the numerical simulation results. For parasitic capacitances, the equations used by PSPICE are:

$$\text{When Vgs} < \mathbf{FC}\cdot\mathbf{PB}, \qquad \text{Cgs} = \textit{area}\cdot\mathbf{CGS}\cdot(1-\text{Vgs}/\mathbf{PB})^{-M} \tag{4.7}$$

$$\text{When Vgd} < \mathbf{FC}\cdot\mathbf{PB}, \qquad \text{Cgd} = \textit{area}\cdot\mathbf{CGD}\cdot(1-\text{Vgd}/\mathbf{PB})^{-M} \tag{4.8}$$

where CGS, CGD, PB and M parameters can be obtained by fitting the capacitance's dependence on Vgs or Vgd.

Since PSPICE does not directly give capacitances as an output, like voltage or current, the parasitic capacitances are evaluated by AC current amplitudes and performing appropriate conversions. Fig. 4-8 (a) and (b) show the PSPICE circuit configurations when evaluating Cgd and Cgs values.



(a) (b)

Fig. 4-8 PSPICE circuit configurations for evaluating (a) Cgd, and (b) Cgs

Since the depletion-mode load JFETs are always used with shorted the gate and source terminals, in the modeling of these devices, only the V_{gs}=0V curves for the I_{ds} vs V_{ds} characteristics are evaluated. Cgs in these JFET models is also set to zero for the same reason. The compact model parameter extraction results are summarized in Table 4.1, including the enhancement-mode and depletion-mode LV VC-LJFETs at room-temperature and 200^{o}C. All devices are assumed to have 1 cm^{2} in active area. The characteristics fitting details are shown in Fig. 4-9 (a)~(z).

Device	VTO	IS	BETA	Rd	LAMBDA	CGD	PB	M	CGS
0.36R	0.55	1E-45	101.5	1.8E-3	2.1E-2	24n	3	0.45	20n
0.36H	0.3	1E-45	40	6E-3	2.9E-2	24n	3	0.45	20n
0.44R	-0.58	1E-45	95	8E-3	2.8E-2	38n	3	0.25	0
0.44H	-0.89	1E-45	30	1.1E-2	4E-2	44n	3	0.2	0
0.50R	-1.45	1E-45	95	4.7E-3	2.3E-2	50n	3	0.15	0
0.50H	-1.75	1E-45	34	9E-3	3E-2	58n	3	0.15	0
0.56R	-2.5	1E-45	74	2.5E-3	2.3E-2	57n	3	0.15	0
0.56H	-2.8	1E-45	27	6E-3	3.8E-2	61n	3	0.05	0
0.62R	-3.8	1E-45	56	1.7E-3	2.4E-2	54n	3	0.05	0
0.62H	-4.1	1E-45	22	4.7E-3	4E-2	57n	3	-0.05	0
0.66R	-4.65	1E-45	46	1.5E-3	2.9E-2	52n	3	0.01	0
0.66H	-4.95	1E-45	17	3.9E-3	6E-2	47n	3	-0.25	0
0.70R	-5.55	1E-45	33	0.6E-3	6E-2	30n	3	-0.45	0
0.70H	-5.85	1E-45	13	2.7E-3	9E-2	35n	3	-0.4	0
0.74R	-6.5	1E-45	28	0.5E-3	6.1E-2	28n	3	-0.4	0
0.74H	-6.8	1E-45	14	3E-3	4.5E-2	40n	3	-0.2	0
0.78R	-7.5	1E-45	22	0	7E-2	21n	3	-0.5	0
0.78H	-7.8	1E-45	7.8	5E-4	1.1E-1	25n	3	-0.32	0
0.82R	-8.5	1E-45	20	0	6E-2	3	20n	-0.5	0
0.82H	-8.8	1E-45	8	1E-3	8E-2	3	27n	-0.25	0
0.86R	-9.5	1E-45	19.5	0	4.2E-2	3	18n	-0.5	0
0.86H	-9.8	1E-45	7	0	6E-2	3	23n	-0.2	0

Table 4.1 PSPICE parameter extraction results for LV VC-LJFETs

(Device ID: 0.36R – JFET with Wvc of 0.36μm, data at room-temperature;

0.36H – JFET with Wvc of 0.36μm, data at 200^{o}C)

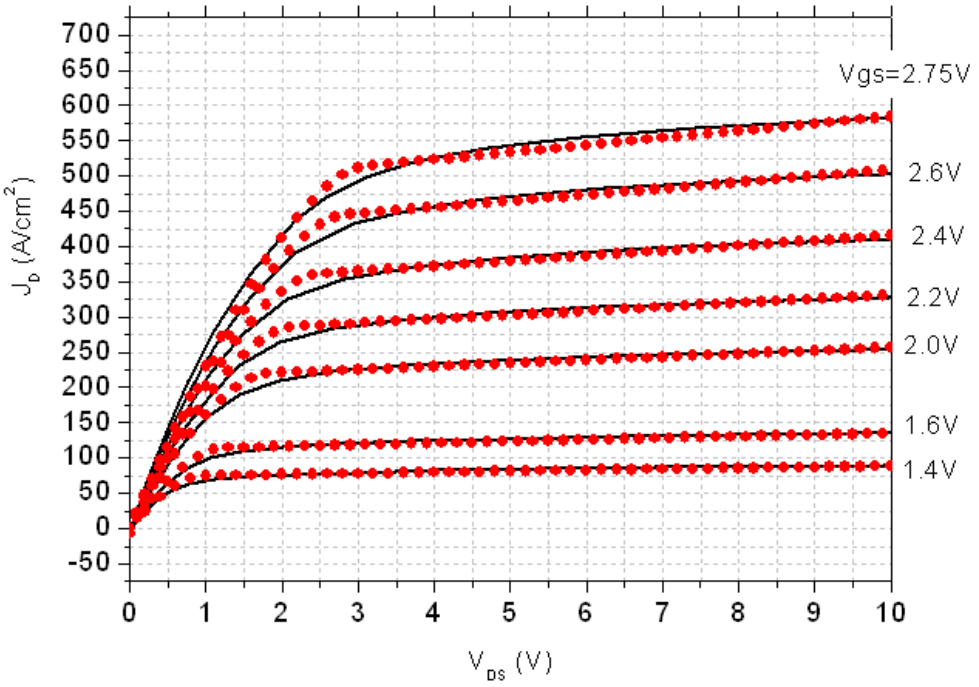


Fig. 4-9 (a) Jds vs Vds fitting for enhancement-mode LV-LJFET (RT)

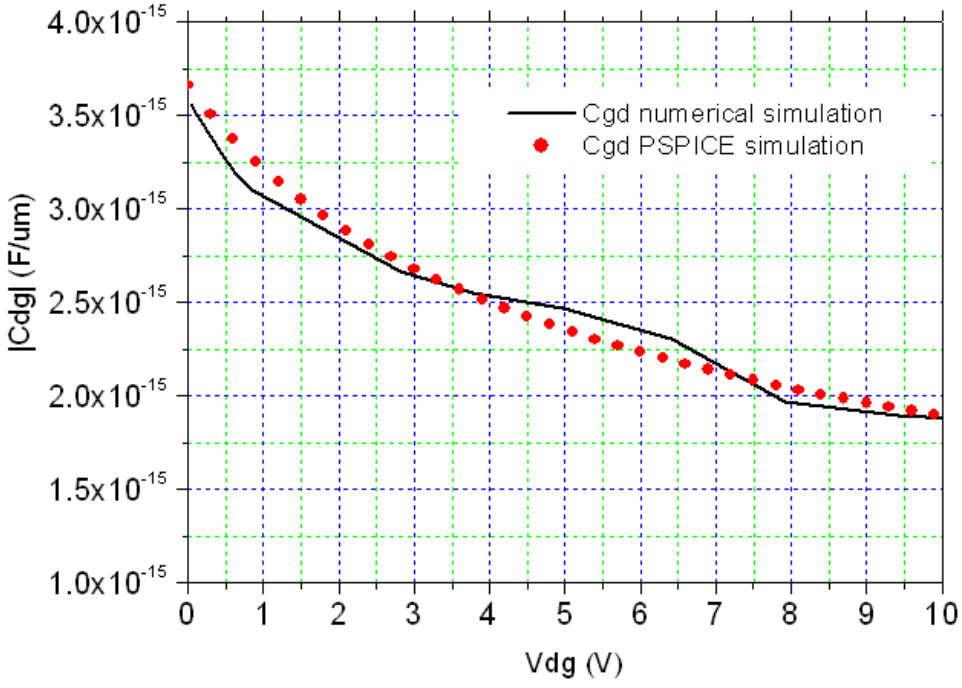


Fig. 4-9 (b) Cdg vs Vdg fitting for enhancement-mode LV-LJFET (RT)

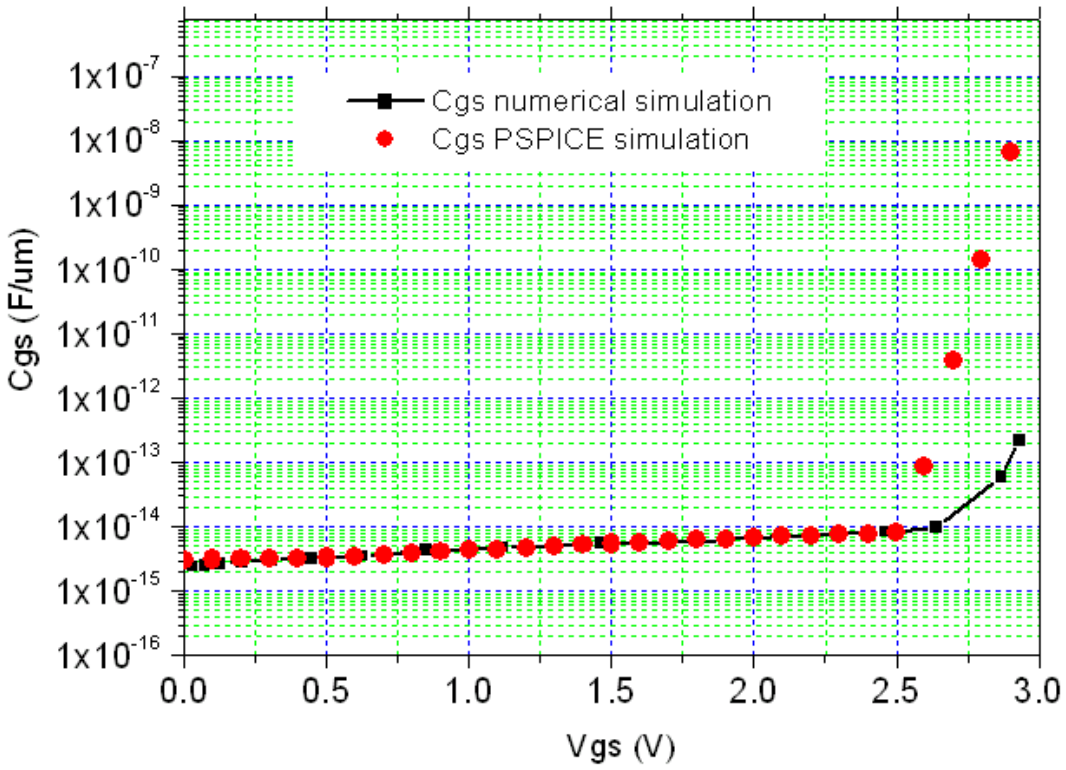


Fig. 4-9 (c) Cgs vs Vgs fitting for enhancement-mode LV-LJFET (RT)

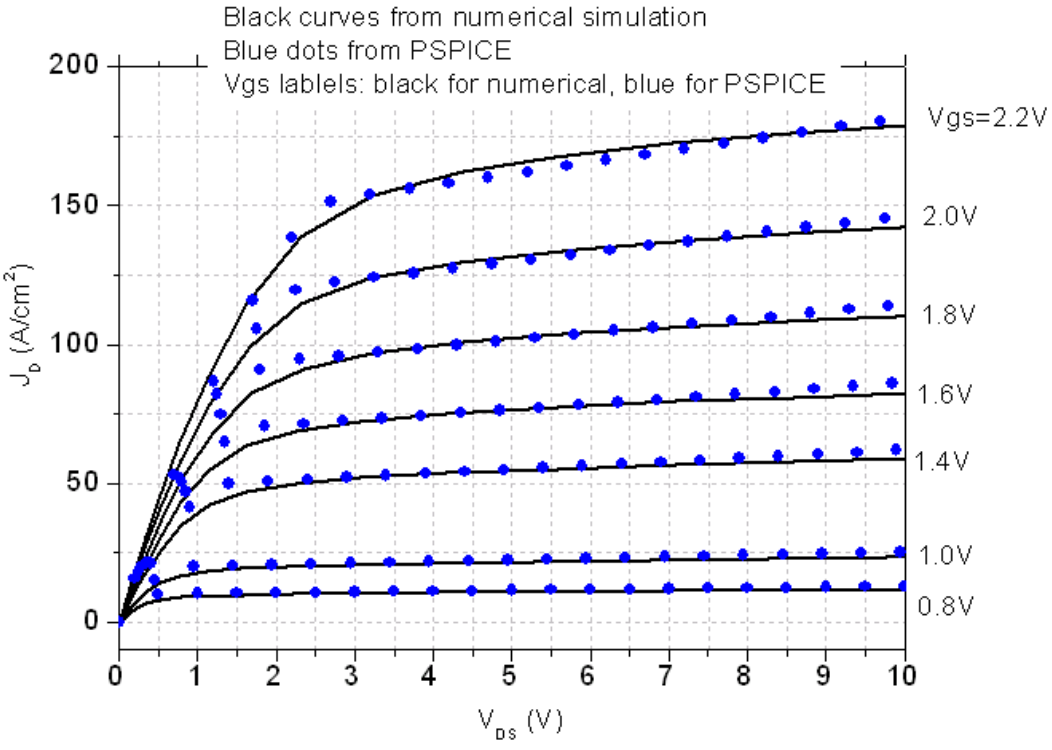


Fig. 4-9 (d) Jds vs Vds fitting for enhancement-mode LV-LJFET (473K)

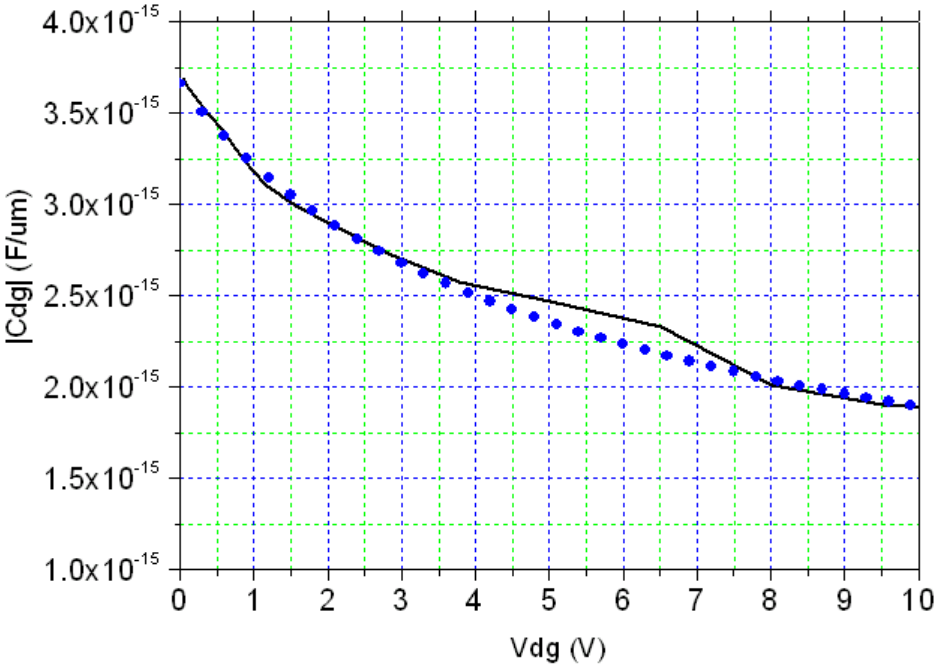


Fig. 4-9 (e) Cdg vs Vdg fitting for enhancement-mode LV-LJFET (473K)

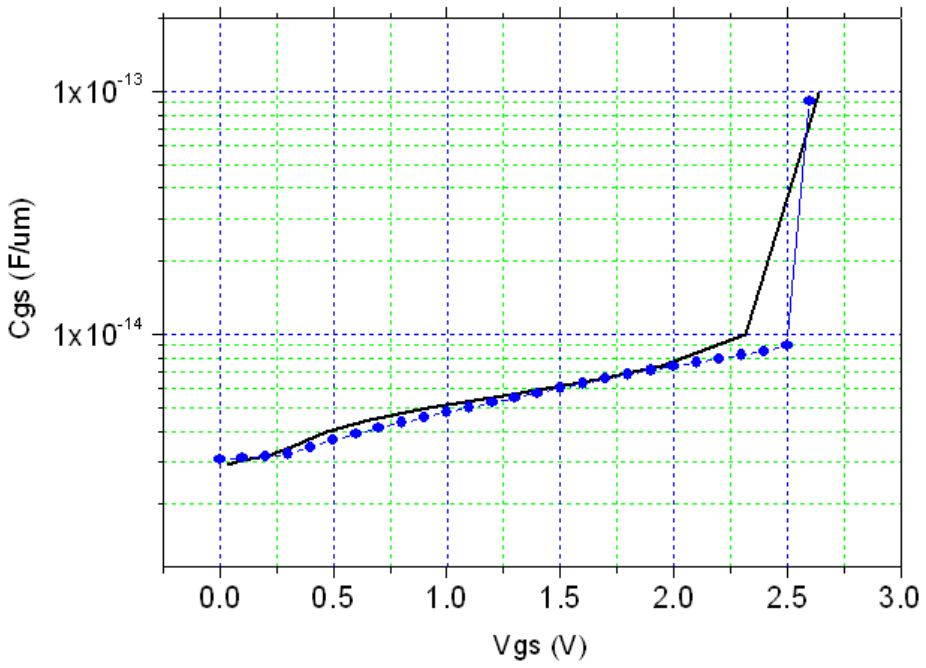


Fig. 4-9 (f) Cgs vs Vgs fitting for enhancement-mode LV-LJFET (473K)

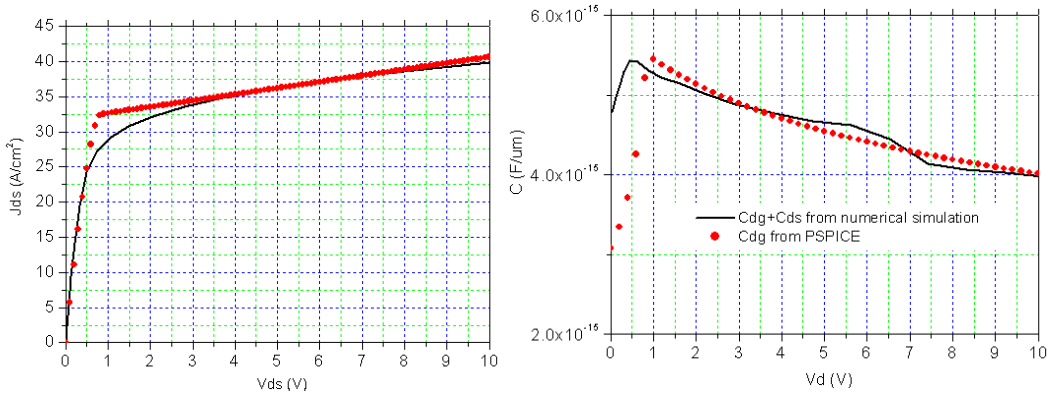


Fig. 4-9 (g) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.44um-Wvc JFET (RT)

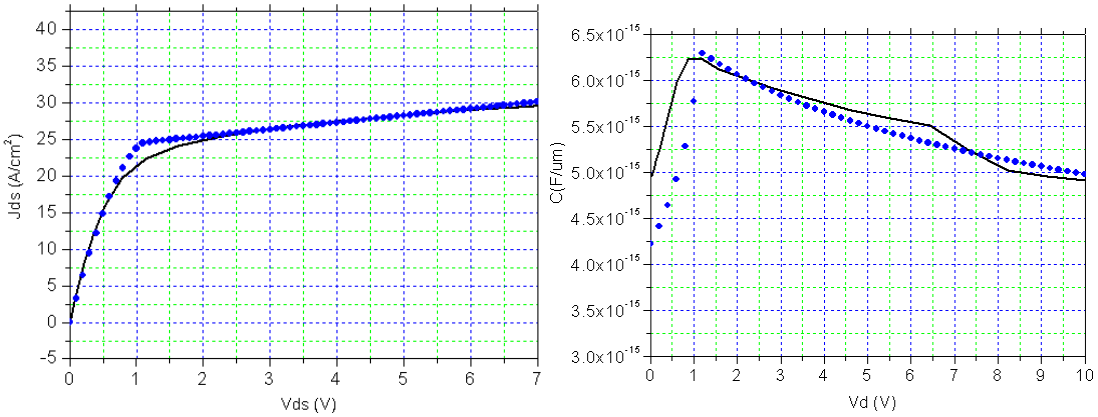


Fig. 4-9 (h) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.44um-Wvc JFET (473K)

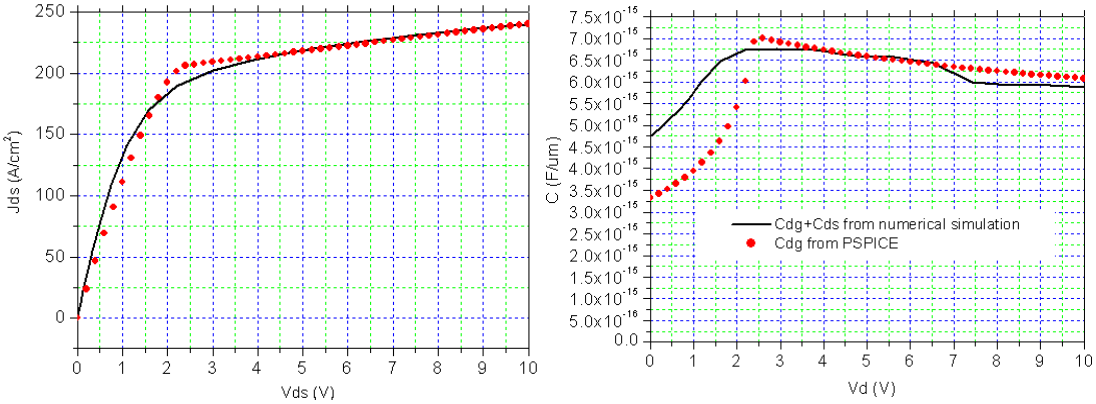


Fig. 4-9 (i) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.50um-Wvc JFET (RT)

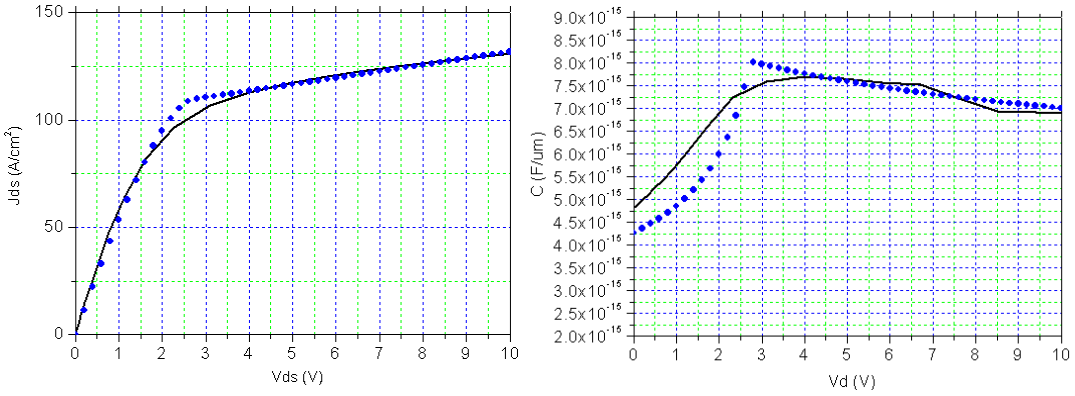


Fig. 4-9 (j) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.50um-Wvc JFET (473K)

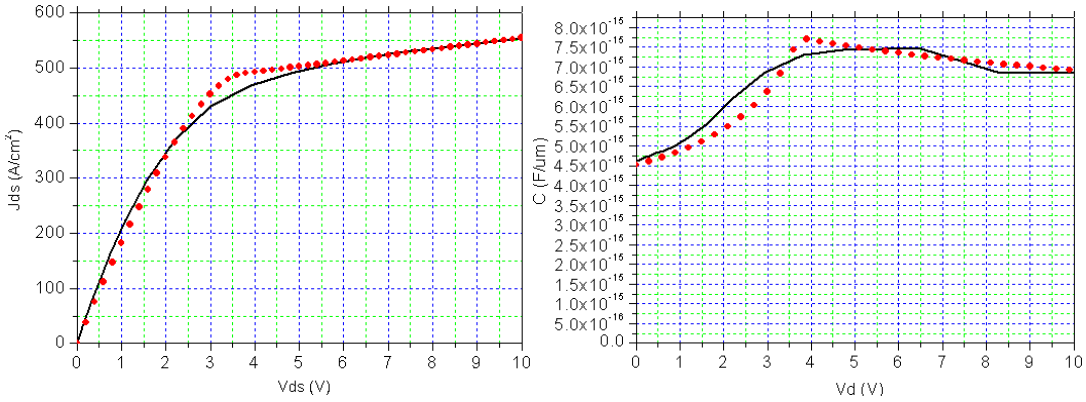


Fig. 4-9 (k) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.56um-Wvc JFET (RT)

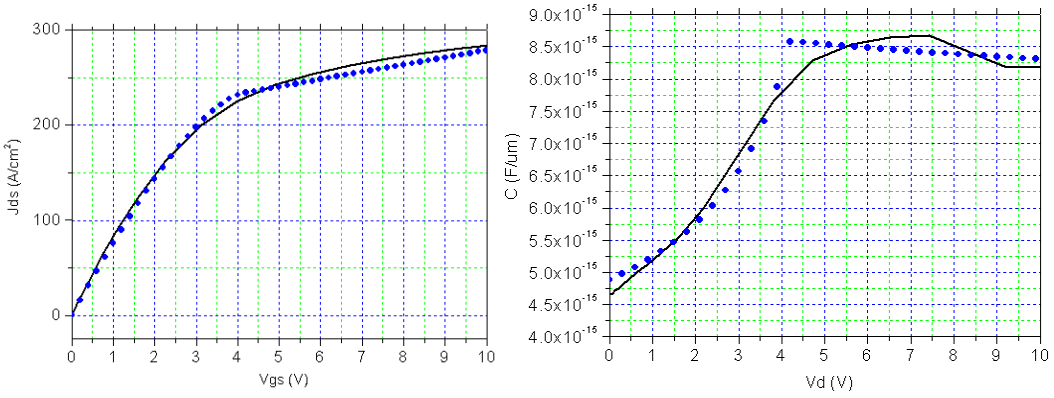


Fig. 4-9 (l) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.56um-Wvc JFET (473K)

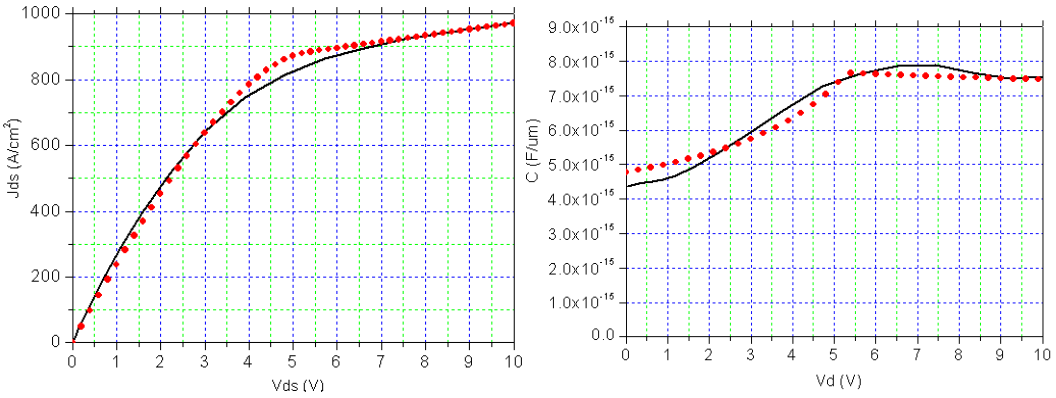


Fig. 4-9 (m) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.62um-Wvc JFET (RT)

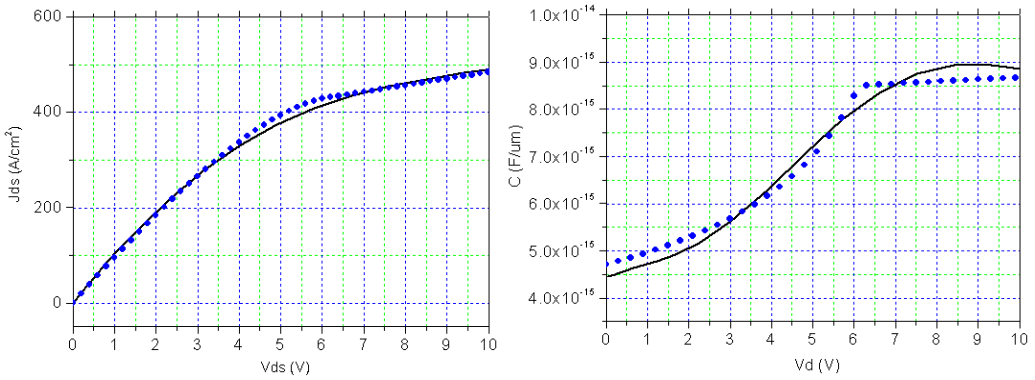


Fig.4-9 (n) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.62um-Wvc JFET (473K)

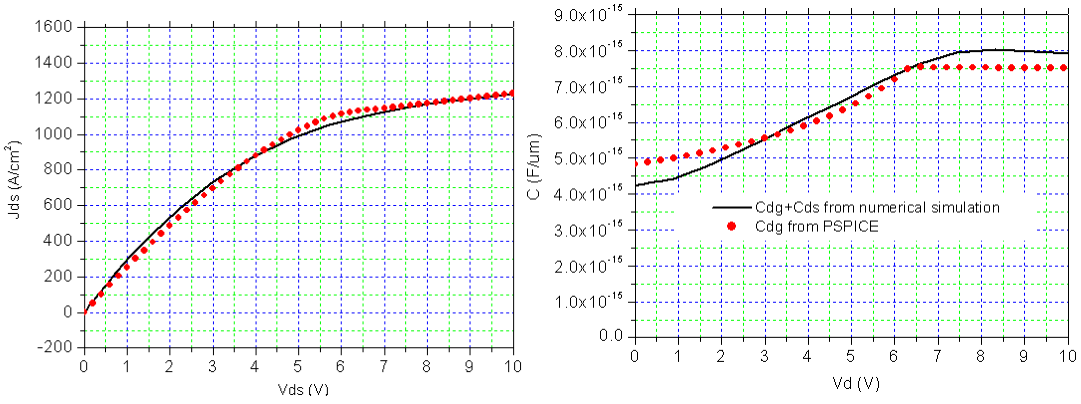


Fig. 4-9 (o) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.66um-Wvc JFET (RT)

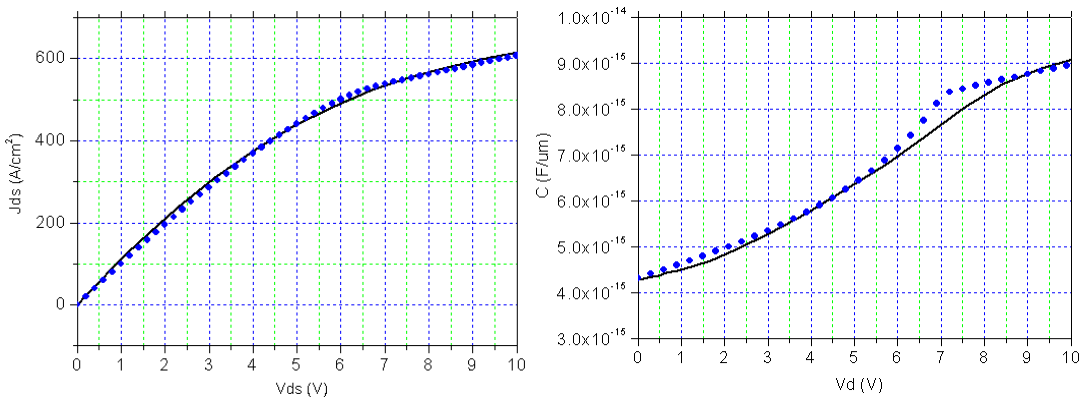


Fig.4-9 (p) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.66um-Wvc JFET (473K)

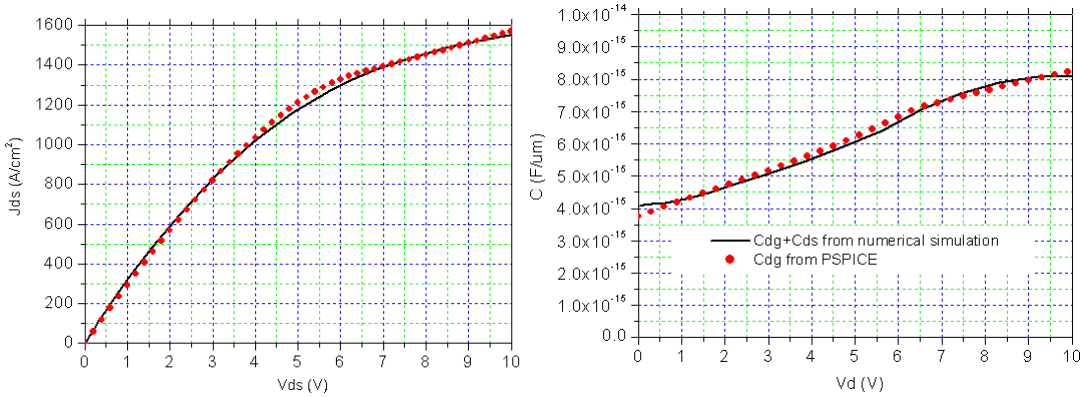


Fig. 4-9 (q) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.70um-Wvc JFET (RT)

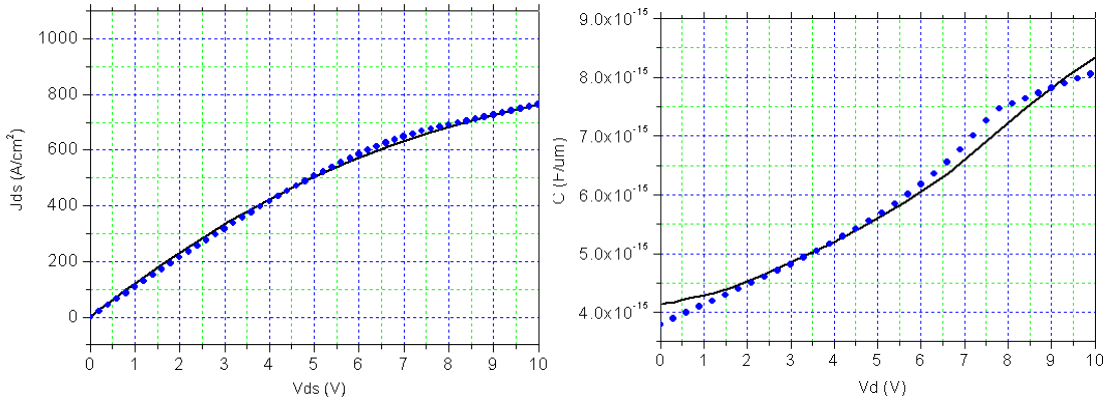


Fig.4-9 (r) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.70um-Wvc JFET (473K)

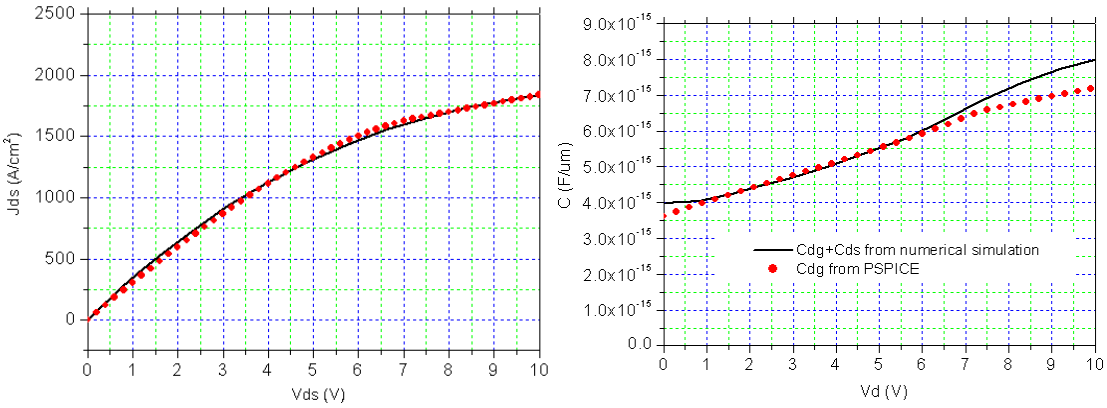


Fig. 4-9 (s) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.74um-Wvc JFET (RT)

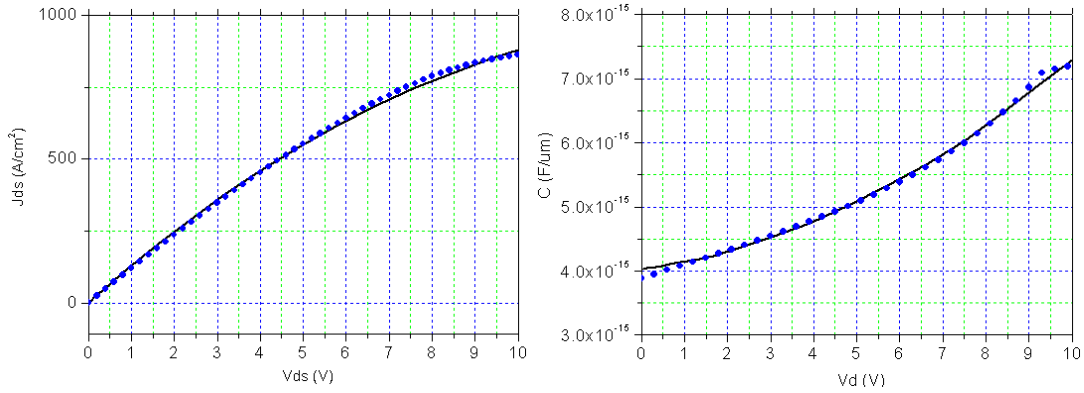


Fig. 4-9 (t) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.74um-Wvc JFET (473K)

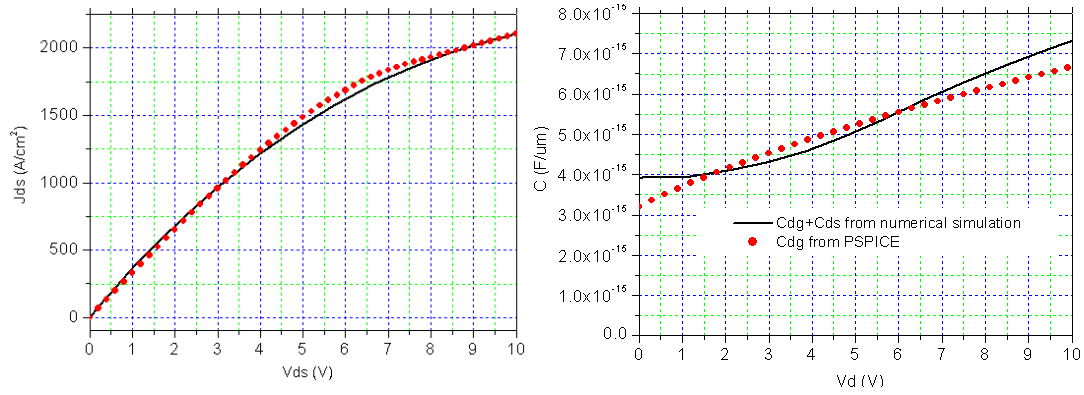


Fig. 4-9 (u) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.78um-Wvc JFET (RT)

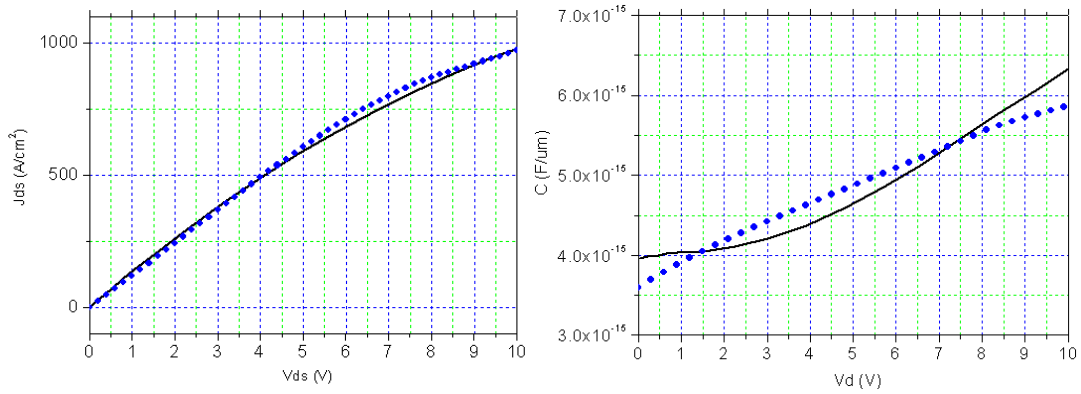


Fig. 4-9 (v) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.78um-Wvc JFET (473K)

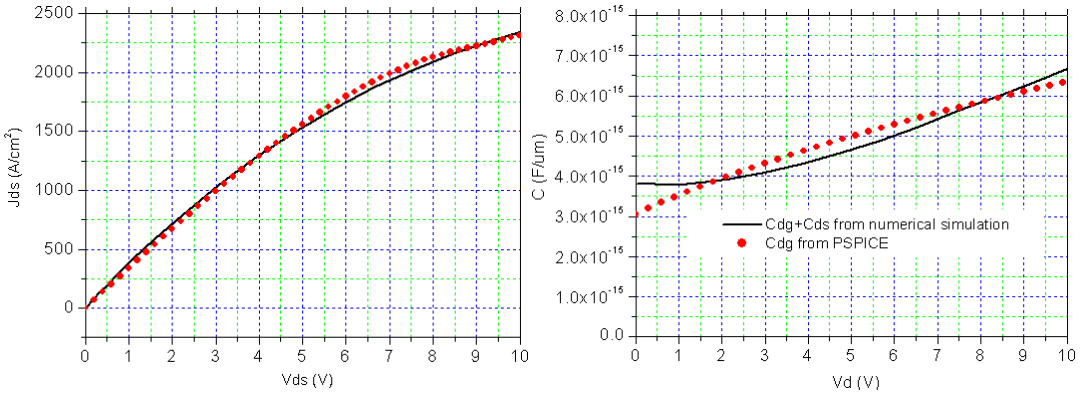


Fig. 4-9 (w) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.82um-Wvc JFET (RT)

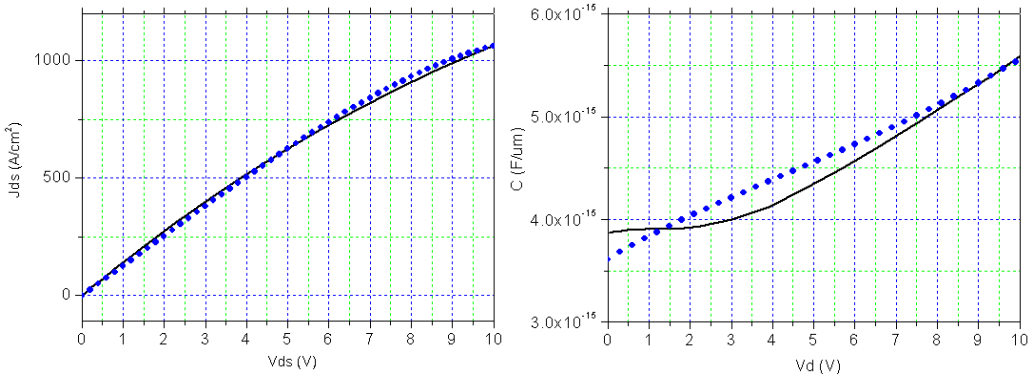


Fig. 4-9 (x) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.82um-Wvc JFET (473K)

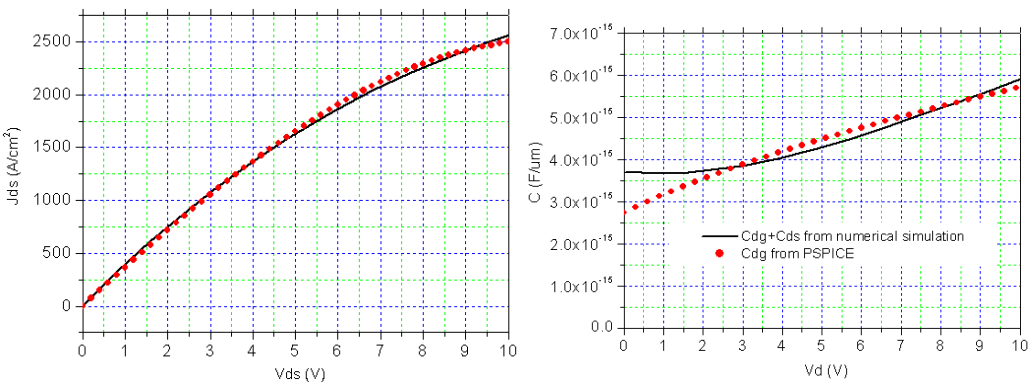


Fig. 4-9 (y) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.86um-Wvc JFET (RT)

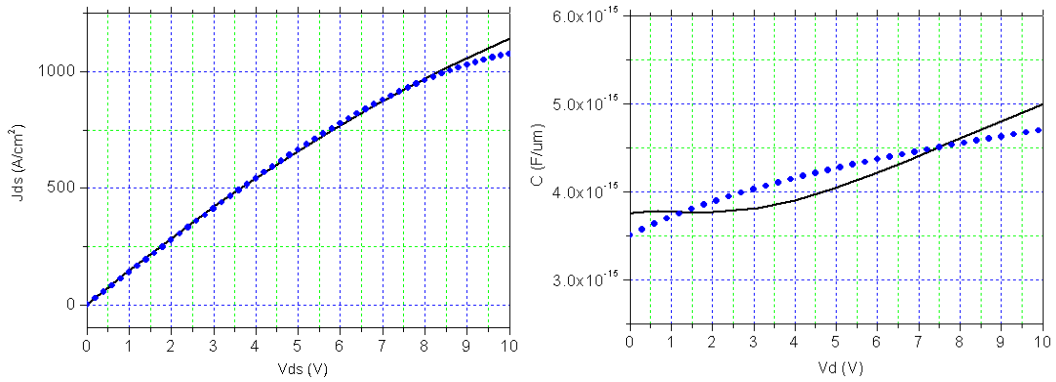


Fig. 4-9 (z) *Jds vs Vds* and *capacitance vs Vd* fittings for 0.86um-Wvc JFET (473K)

In addition to the low-voltage VC-LJFETs, a power LJFET model is determined from the experimental characterization data of a previously fabricated device as the following:

Room-temperature model:

.model J_HV_ljfet NJF Beta=0.6 Vto=0.7 N=3.7 Pb=2.85 FC=0.5 Lambda=0.049

+ Rd=0.225 Cgs=0.2n Is=1e-15 Cgd=43p M=0.5 Betatce=-0.553

.model D_HV_ljfet D Is=1e-15 Cjo=0.165nF bv=1500V VJ=75 M=5 N=4

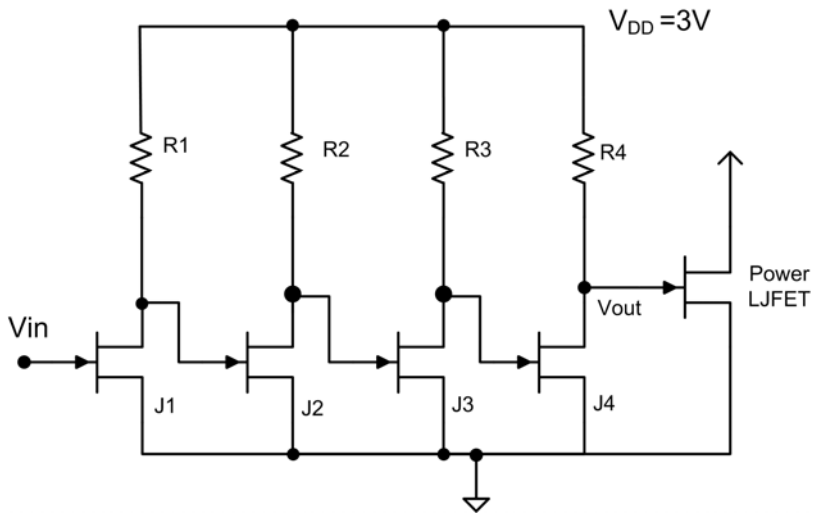
473K model:

.model J_HV_ljfet_200c NJF Beta=0.23 Vto=0.3 N=3.7 Pb=2.85 FC=0.5 Lambda=0.049
+ Rd=0.55 Cgs=0.2n Is=1e-15 Cgd=43p M=0.5 Betatce=-0.553

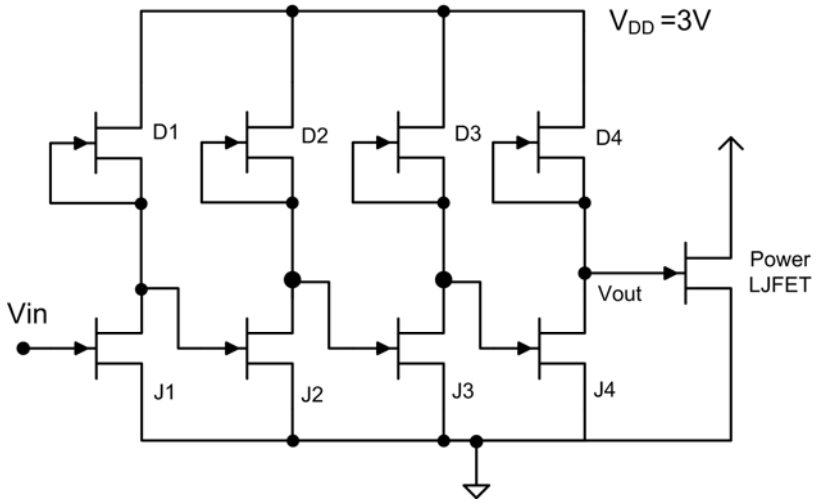
.model D_HV_ljfet_200c D Is=1e-15 Cjo=0.165nF bv=1500V VJ=75 M=5 N=4

4.4.2 Buffer Driver Circuit Setup in PSPICE

The target of our buffer circuit design is to minimize the delay times of the buffer circuit and the switching times of the larger power device being driven, while at the same time, ensure proper logic switching functionality (on/off) by a reasonable safety margin against processing uncertainties. The resistor-load and depletion-load versions of the gate buffer circuits are set up in PSPICE as illustrated in Fig. 4-10. The drain terminals of the power LJFET is connected to a 2A current source in parallel with a freewheeling diode. A high-voltage power supply then pulls up the current source and diode to 200V. The scaling factor between two neighboring stages is 5.



(a) Resistor-load buffer drive circuit diagram



(b) Depletion-load buffer drive circuit diagram

Fig. 4-10 Circuit setup for simulation in PSPICE

4.4.3 The Depletion-load Advantage Visualized

In this example, we performed circuit switching simulation for the buffer drivers loading a 1.6mm^2 power VC-LJFET. The 0.44μm-Wvc LJFET is selected as the depletion load, and the device areas for the load and switching transistors in each inverter

stage are equal. A 3V DC source supplies power to the driver circuit. For comparison to the resistor-load buffer, resistors equivalent to the JFET loads are determined by the DC operating points when the enhancement-mode JFETs are turned on. In other words, the resistor-load and depletion-load versions of the buffer driver have the same DC output voltage levels, and are being compared against each other for their dynamic performance. Fig. 4-11 compares the high-voltage switching performance of the power device driven by the two buffer circuits. Calculated from these waveforms, using the LJFET loads in place of resistors cuts the switching fall time and hence the switching loss by nearly 50% from 123ns to 67ns. [56]

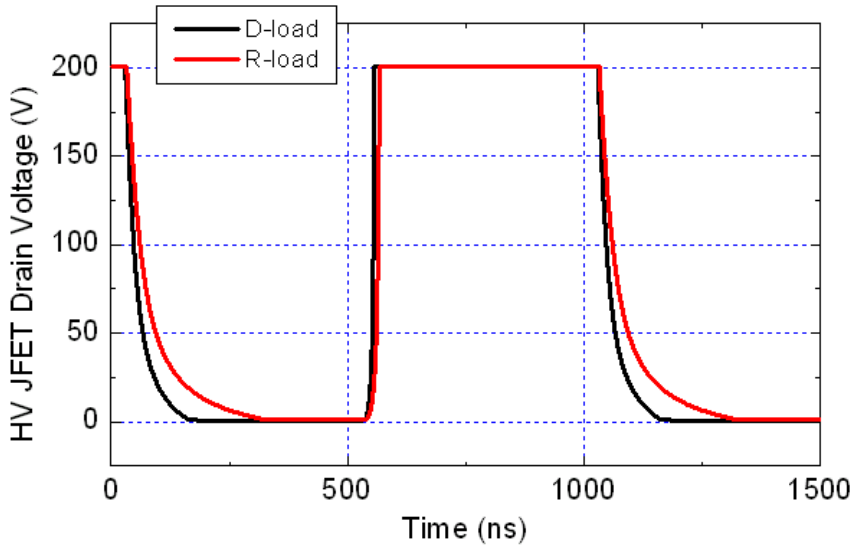


Fig. 4-10 Simulated 1MHz switching waveforms

of SiC power ICs with JFET and resistor loads

We shall note that load LJFETs of wider Wvc may be used, which would reduce the chip area needed for the same load resistance. However, the trade-off here is a slower

switching time, since the I-V characteristics of wider-channel VC-LJFETs become more linearly shaped like that of a resistor. Table 4.2 compares the dynamic performance of drivers using LJFET loads in three vertical channel openings, where they all have equivalent DC voltage transfer characteristics (VTC). The depletion- load advantage in switching time gradually diminishes as the Wvc of the load LJFETs gets wider.

Wvc of load (μm)	Chip area for driver (mm^2)	Fall time (ns)
0.44	0.5	67
0.50	0.29	85
0.56	0.27	108
Resistor	0.25 + resistor area	123

Table 4.2 Comparison of chip area usage and power device switching fall times by using LJFET loads of different Wvc in the driver

4.4.4 Design for Practical Buffer Fabrication

While the above example shows the speed benefit of using narrow channel JFETs, in practice designing the buffer with 0.44μm-Wvc JFET loads is very risky. Due the extreme sensitivity on the mesa width, the narrow-channel load JFET could be normally off easily if the mesa is etched 0.1μm narrower. On the other hand, a wider mesa will significantly enhance the current conduction and result in a much lower load resistance. This will in turn elevates the V_{OL} level of the logic inverters, and easily lead to

insufficient off-biasing of the next-stage switching JFET and hence the malfunction in the logic inverter cascading.

A practical design for the load JFET channel should allow slight variation in the mesa width control; while still achieve a reasonable speed benefit over the resistor-load equivalent. In this design work, the 0.56μm vertical channel is selected on this ground. The following simulations based on a 5V buffer circuit power supply and a 1:5 area ratio of the load and switching JFETs will predict roughly 25% fall-time reduction for the depletion-load buffer as compared to its resistor-load DC equivalent.

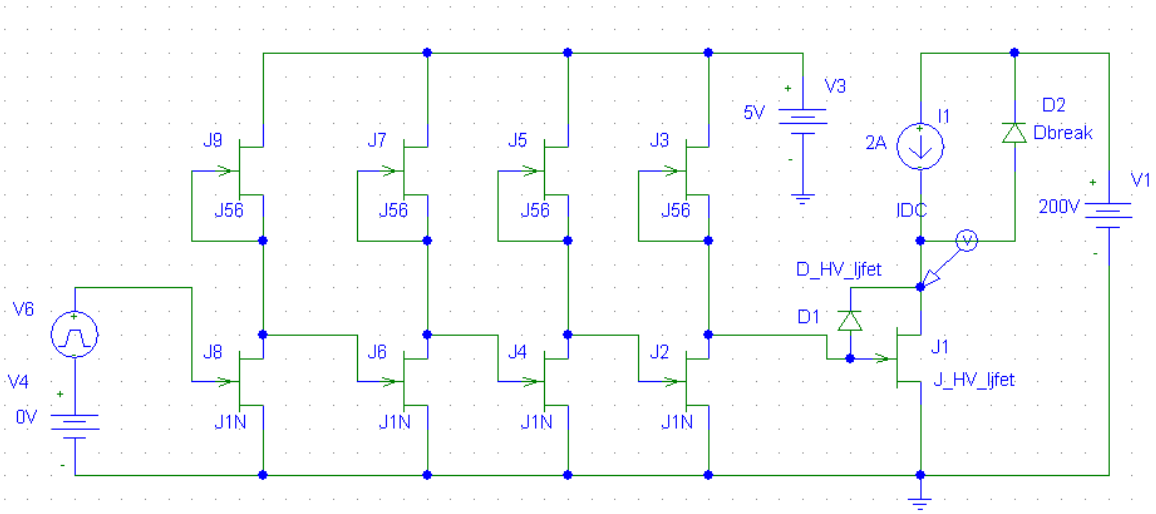


Fig. 4-11 PSPICE Circuit setup of a four-stage buffer driving a power LJFET

Fig. 4-11 shows a screenshot of PSPICE circuit setup of the designed four-stage buffer circuit driving the power LJFET of 1.6mm^2. A 5V voltage source is used to power the buffer circuits for charging speed enhancement over the 3V supply. The scaling factor of 5 is used, and the total area of the buffer driver is controlled within 20% (18.72%) of the

size of the power JFET. Depletion-load transistors are designed to be 5 times smaller than the enhancement-mode JFET of the same stage considering the trade-off between switching speed and output voltage levels. The load transistors with Wvc between 0.44μm and 0.66μm is paired to the enhancement-mode JFET and simulated in this circuit. Load transistors of Wvc larger than 0.66μm are not considered because their I-V characteristics are already very similar to a resistor load and hence are not able to deliver the performance benefits of a depletion-mode transistor load.

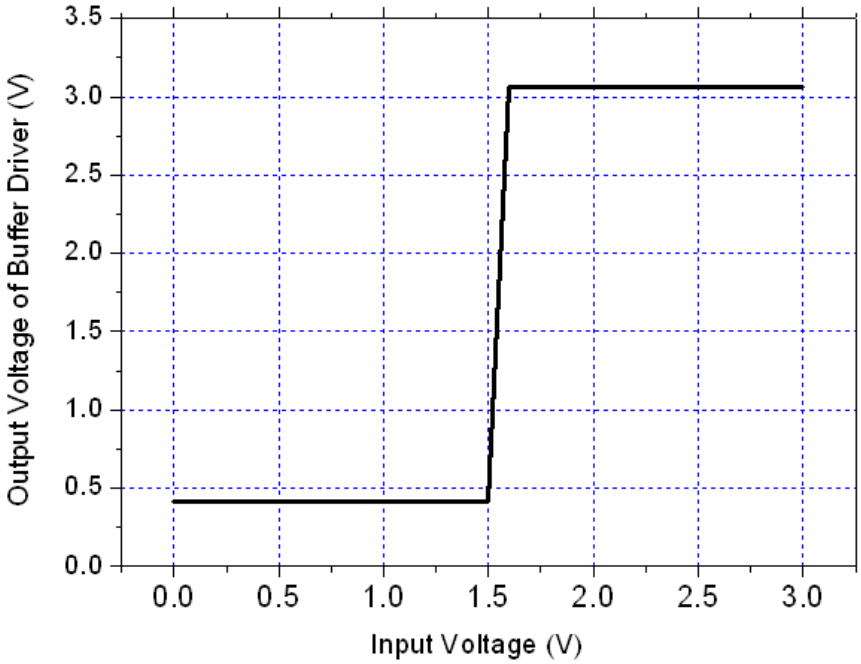


Fig. 4-12 (a) DC voltage transfer curve (VTC) of four-stage driver using Wvc=0.56μm depletion load (VOL=0.414V, VOH=3.06V)

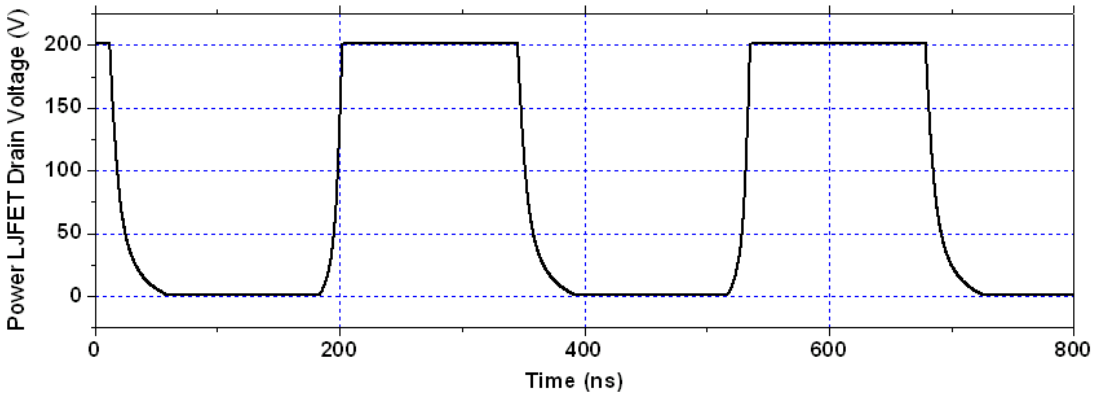


Fig. 4-12 (b) High voltage switching waveform at 3MHz (Wvc_load=0.56μm)
T_rise=11ns, T_fall=23ns, T_rise+T_fall=34ns

Fig. 4-12 (a) and (b) show the PSPICE simulation results using the depletion-load model J56. The V_{OL} and V_{OH} levels can be determined from the voltage transfer curve in Fig. 4-12(a), and the switching waveform in Fig. 4-12 (b) illustrates the rise and fall times in the power JFET's output terminal. The total of rise and fall time is an important measure of how fast the circuit is capable of switching. For the five depletion-load JFETs we simulated, their rise and fall time values, together with DC V_{OH}/V_{OL} levels are shown in Table 4.3.

Wvc=	0.44μm	0.50μm	0.56μm	0.62μm	0.66μm
T_rise (ns)	24	12.5	11	16.6	18
T_fall (ns)	323	52.9	23	16.7	15
T_total (ns)	347	65.4	34	33.3	33
V_{OH} (V)	2.85	3.01	3.06	3.09	3.1
V_{OL} (V)	0.03	0.18	0.414	0.69	0.78

Table 4.3 High-voltage switching rise and fall times
and DC V_{OH}/V_{OL} levels on different Wvc load transistors

From Table 4.3, we determined that the center design 0.56μm is an optimal load because of its fast switching speed and relatively low V_{OL} level. A wider channel opening would offer similarly fast switching but result in a higher V_{OL} at the same time. We require the V_{OL} level to be lower than the threshold voltage of the enhancement-mode JFET to ensure proper on and off switching. And a room-temperature V_{OL} level above 0.5V would pose a risk of malfunction, especially when temperature is elevated.

To compare with a resistive load driver, we replaced the depletion-load JFETs with resistors. The resistance values are determined to maintain the same V_{OL} level (0.414V) as the depletion-mode load case. Specifically, this gives a 23.1Ω resistance for the 4^{th} stage, and 5 times larger for each preceding stage. The rise time, fall time and total of the two are calculated from the switching waveforms, and found to be 11ns, 31ns and 42ns respectively. In such a circuit configuration, it is seen that the 0.56μm depletion-load JFETs realize a 25% reduction in the power device's switching fall time as compared to the resistor-load counterpart. In our design for the buffer driver fabrication, the enhancement/depletion-mode (E/D mode) circuit simulated in this configuration provides the foundation for the mask layout strategy. The 0.36μm-0.56μm VC-LJFET pairs are therefore targeted for vertical channel width control purposes.

4.4.5 Circuit Functionality at High Temperature

4H-SiC is a wide bandgap semiconductor with demonstrated potential of high-temperature electronics applications. In this work, we are therefore naturally

interested in analyzing the device and IC functioning under elevated temperatures. By replacing the room-temperature models of the transistors with their respective 200°C models, the high-temperature functionality of the buffer driver and power IC can be predicted.

Using the same enhancement-mode (Wvc=0.36μm) and depletion-mode (Wvc=0.56μm) JFETs, the DC voltage transfer curve at 200°C is shown in Fig. 4-13 (a). A slight increase in the V_{OL} level is expected compared to the room-temperature results.

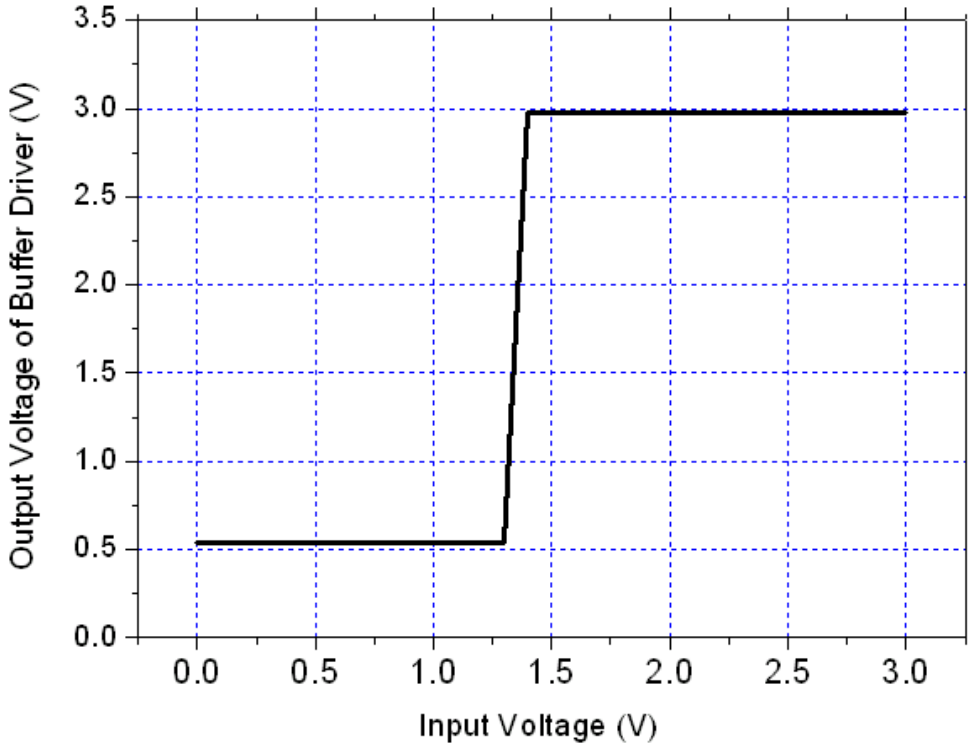


Fig. 4-13 (a) 200°C DC voltage transfer curve (VTC) of four-stage driver using Wvc=0.56μm depletion load (V_{OL}=0.54V, V_{OH}=2.98V)

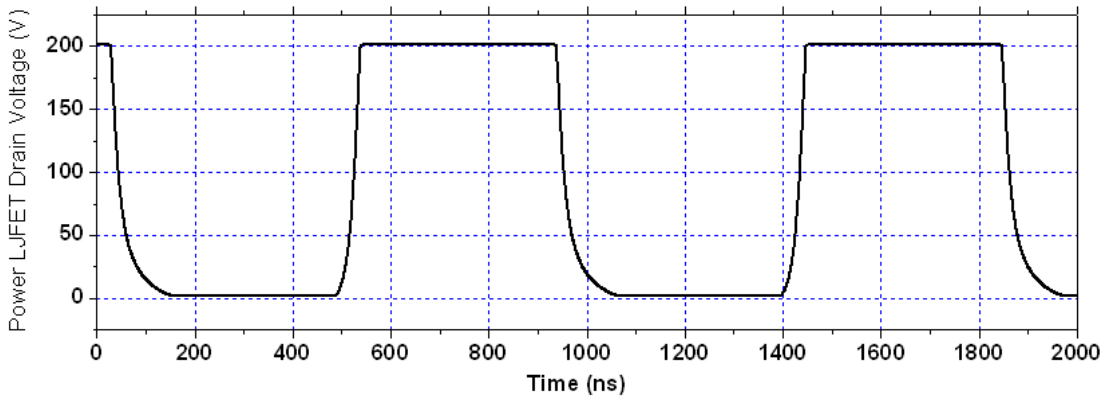


Fig. 4-13 (b) High voltage switching waveform at 1.1MHz

T_rise=31ns, T_fall=58ns, T_rise+T_fall=89ns

The buffer driver still functions well at 200^{o}C but the switching speed is slower due to lower current driving capabilities of the transistors, which can be seen from Fig. 4-13 (b). In short, the designed four-stage E-D mode buffer and power IC are simulated to operate at up to 200^{o}C with megahertz switching capability, making it an attractive technology for high-frequency medium-power switching applications.

4.4.6 Circuit Functionality with Wafer and Process Variations

In the actual wafer fabrication, the Wvc parameter of VC-LJFETs is determined by the source mesa widths and the depth of sidewall gate implants. This parameter is critical but difficult to precisely control. To experimentally hit the design target, multiple mesa widths are usually included on the photomasks. To determine the optimal arrangement of mesa widths on the mask, a thorough understanding on the Wvc variation tolerance is needed. In Section 4.3.4, we used five different depletion-load transistors to simulate the power

switching functionality. From Table 4.3, the effect of load transistor Wvc variation can be seen. The buffer driver is found to be functional in all the five cases, only at different speed ratings.

In addition to the load variation, the enhancement-mode LJFET's channel opening can be off the target width as well. Analysis of this effect can be accomplished by modifying the threshold voltage parameter (VTO) of the enhancement-mode LJFET model according to its V_{th} dependence on Wvc, and then performing the transient simulation with the new parameters. By setting the enhancement-mode LJFET's Wvc values from 0.24μm to 0.46μm in these simulations, we see a more critical channel control demand for the switching devices than the load. Specifically, the enhancement-mode JFET's Wvc window for room-temperature operation is found to be around 0.15μm, whereas the load varying from 0.44μm to 0.66μm was found allowable for proper switching. A summary of buffer functionality with varied Wvc of the load and switching JFETs is shown in Fig. 4-14, including room-temperature and 200^{o}C results.

Based on these results, the channel width step designed on the mask has to be no more than 0.1μm to ensure that one of the variants will hit the Wvc window for the enhancement-mode JFET.

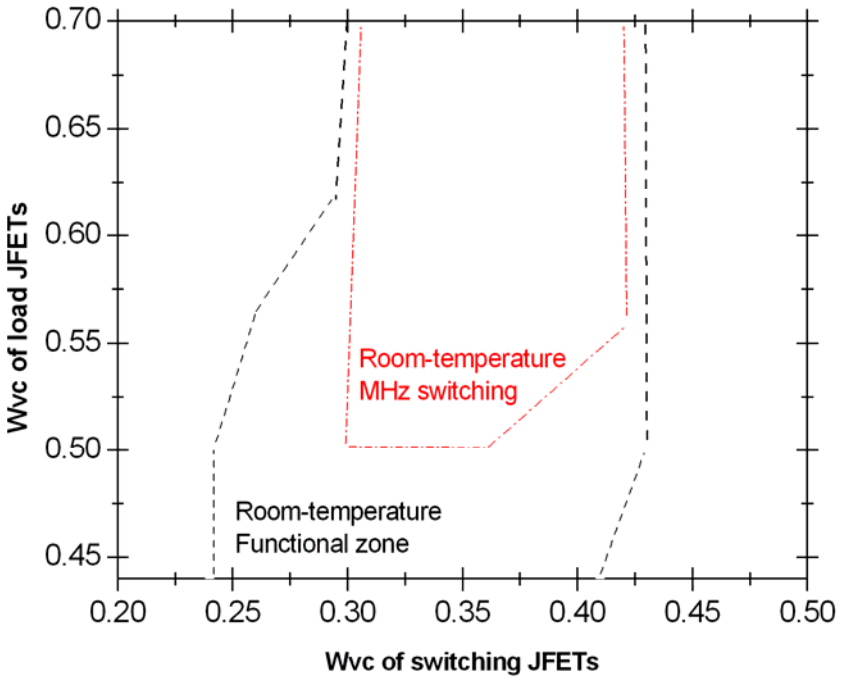


Fig. 4-14 (a) Power switching functionality at RT with varied Wvc values

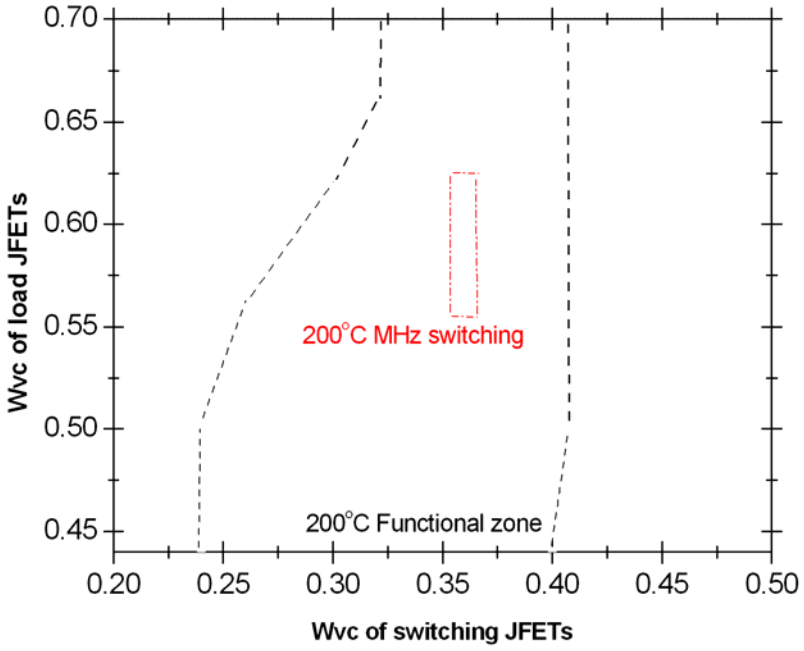


Fig. 4-14 (b) Power switching functionality at 200°C with varied Wvc values

In addition to possible channel width variations, the doping concentration of the epitaxial channel layer is also a parameter that may be significantly out of specification. The designed doping is $5.2x10^{16}cm^{-3}$, but a realistic expectation of epi-layer's actual doping concentration would be somewhere between 3 and 8 $x10^{16}cm^{-3}$. The effect of a doping concentration change to an LJFET can be roughly considered equivalent to a change in Wvc, at the condition that these two changes result in the same variation of the gate threshold voltage.

On theoretical calculation, when the doping concentration is at 3 $x10^{16}cm^{-3}$, the enhancement-mode LJFET (Wvc=0.36μm) will have a threshold voltage of 1.59V. This is equivalent to an LJFET of Wvc=0.277μm with the target doping 5.2 $x10^{16}cm^{-3}$. At the same time, the load transistor (Wvc=0.56μm) will have a threshold voltage of -0.27V, equivalent to Wvc=0.416μm at doping level of 5.2 $x10^{16}cm^{-3}$. In order to restore the original threshold voltages (Vth_e= 0.54V, Vth_d=2.68V), the channel opening for the enhancement-mode JFET has to be increased to 0.48μm, and for the depletion-mode JFET, 0.748μm. The analysis for doping at 8 $x10^{16}cm^{-3}$ is similar but with opposite directions of change.

A summary of the calculations is shown in Table 4-4. From this result, we conclude that to compensate the possible epilayer doping inaccuracies, channel width variations of +/- 0.1~0.2μm from the targeted value need to be included in the photomask design.

Actual Doping Level (cm^{-3})	E-mode JFET equivalent Wvc at target doping level	E-mode JFET Wvc needed to offset doping change	D-mode JFET equivalent Wvc at target doping level	D-mode JFET Wvc needed to offset doping change
N=3E16	0.277μm	0.48μm	0.416μm	0.748μm
N=5.2E16	0.36μm	0.36μm	0.56μm	0.56μm
N=8E16	0.448μm	0.28μm	0.703μm	0.445μm

Table 4-4 Calculation for doping variation effects

4.4.7 Circuit Performance with Fewer Stages

In super buffer circuit theory, the optimal scaling factor for minimal propagation delay is the Euler's number, e (~2.718). In practice, a larger scaling factor is usually used to reduce the number of inverter stages and the circuit complexity. The four-stage driver designed above uses a scaling factor of 5 for good performance without excessive number of stages.

However, if worse propagation delay is tolerable and a better chance of driver functionality is desired, alternative buffer designs using fewer stages can be implemented. In this section, we compare the performance of the four-stage driver to optimized 3, 2 and 1 stage alternatives of equal chip area.

To compare the performance of the buffer drivers, a realistic on-chip source of weak input signal is needed. In the circuit, we included a final stage of a ring oscillator to present

the output impedance effect of the signal source. Such a stage is assumed to consist of an enhancement-mode LJFET of 20μm channel width and a resistor load paired to it.

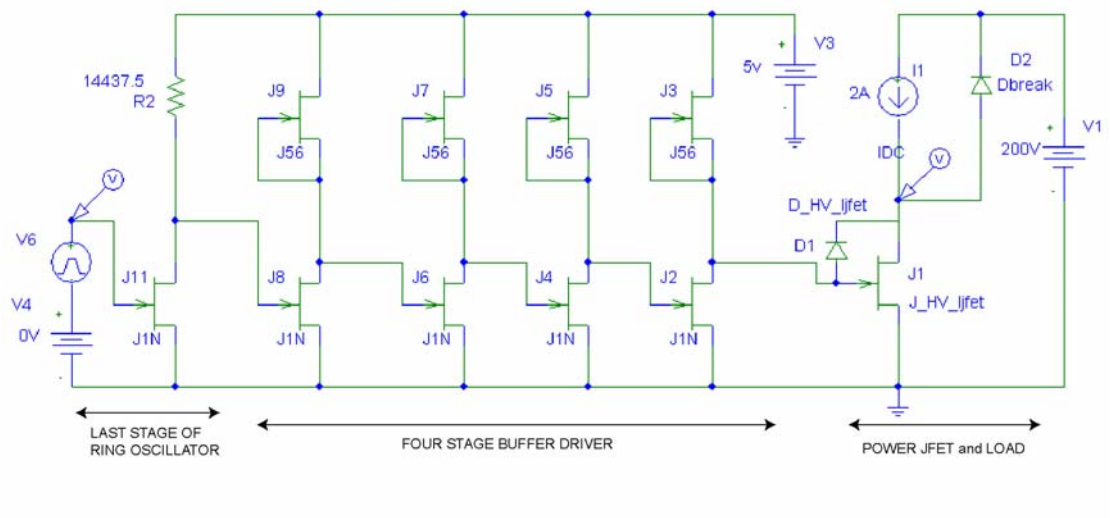


Fig. 4-15 Configuration of the LJFET-based power IC with input-side interface

The four-stage buffer driver in Fig. 4-15 is the same one designed in the previous sections. The first-stage enhancement-mode LJFET is 5 times the size of the transistor in the oscillator. Each of the following stage is 5 times larger than the previous one. The buffer drives a power LJFET of 1.6mm^2. The total area used for the buffer is 18.72% of that for the power JFET.

Fig. 4-16 shows 5MHz high-voltage switching of the four-stage buffer-driven circuit. We define four figures-of-merit from the waveform to evaluate the switching delay and speed, as in Table 4-5. The four-stage driver simulation results are included in Table 4-5, row 3.

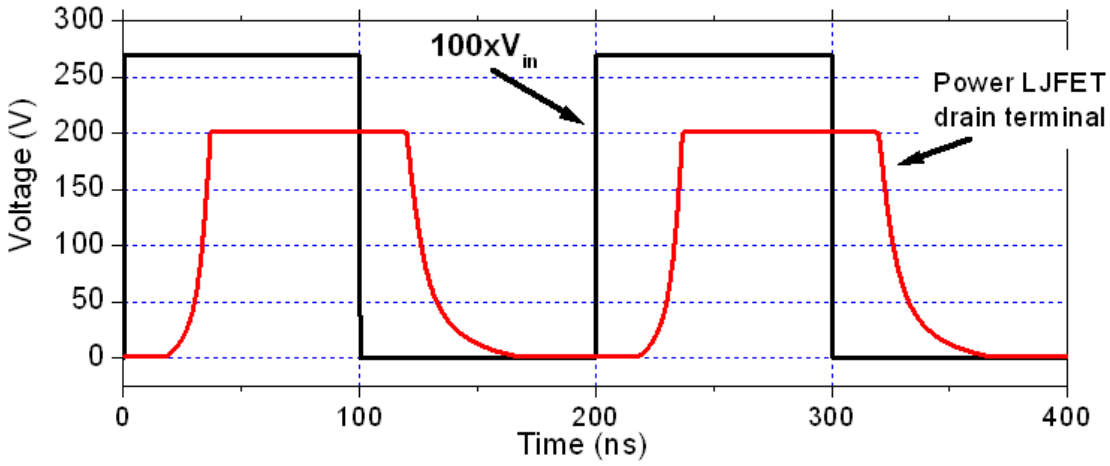


Fig. 4-16 Transient switching waveforms of the power IC with four-stage buffer driver

(The 3V input square wave is magnified by 100 for visual comparison purpose)

Td_on	Td_off	T_f	T_r
Delay time from input change to 10% of output voltage drop	Delay time from input change to 10% of output voltage rise	Time needed for output voltage falling from 90% to 10%	Time needed for output voltage rising from 10% to 90%
21ns (four-stage)	25ns (four-stage)	23ns (four-stage)	10ns (four-stage)

Table 4-5 Definition of delay and switching times

To simulate the performance of an alternative buffer design with fewer stages, we make modifications to the circuit according to the following rules. The alternative designs determined this way are optimized for their respective number of stages and suitable for comparison to the four-stage driver of the same chip area.

1. Keep the last stage of the ring oscillator and power device loads intact.
2. Remove 1, 2 or 3 stages

3. Define a to-be-determined scaling parameter α, so that the first-stage enhancement-mode LJFET in the driver is α times the size of the transistor in the ring oscillator. The depletion-load is still 5 times smaller than the enhancement-mode LJFET of the same stage to maintain the same DC voltage transfer characteristics. Each of the stage towards the power device is α times larger than the previous stage.
4. Add up the total size of the driver, which is dependent on the parameter α, and make it equal to the total size of the four-stage driver.
5. Find the value for α based on the above equation. Implement the sizes of the transistors in the circuit according to step 3.

The scaling parameters such determined for 3-, 2-, and 1-stage buffer drivers are 8.85, 27.5 and 780. These circuits are simulated for high-voltage switching, and the delay times are found from the waveforms. They are summarized in Fig. 4-17. For reference purpose, a circuit without any buffer stages is also simulated with delay results included.

It is seen from Fig. 4-17 that when the number of stages is reduced to 3 and 2, the delay times have moderate degradation in the Td_off and/or Td_on values. Nevertheless, 5MHz switching in these circuits can still function down to this point. Fig. 4-18 shows the switching waveforms of 4-, 3- and 2-stage buffer driver circuits with the same 5MHz signal source (High-low polarity is inverted for the 3-stage for visual comparison purpose). With such an input source, a perfectly fast switching circuit would yield a square-shaped waveform that toggles between 0V and 200V sharply at the 100, 200 and 300ns points. In

this figure, the three plotted waveforms all have visible delays at the tens-of-nanosecond level. Depending on specific application requirements, however, these driver circuits may be sufficiently competent for fast power switching purposes up to megahertz frequencies.

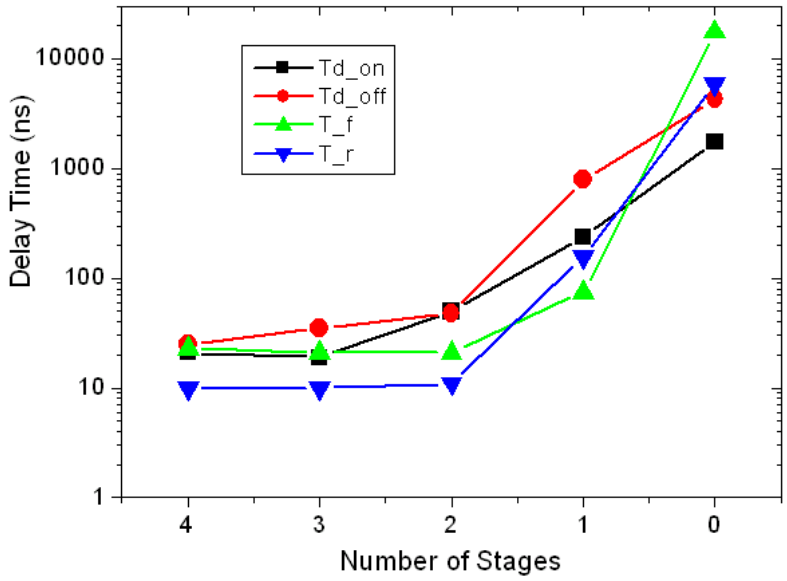


Fig. 4-17 Simulated delay times of buffer drivers with varied number of stages

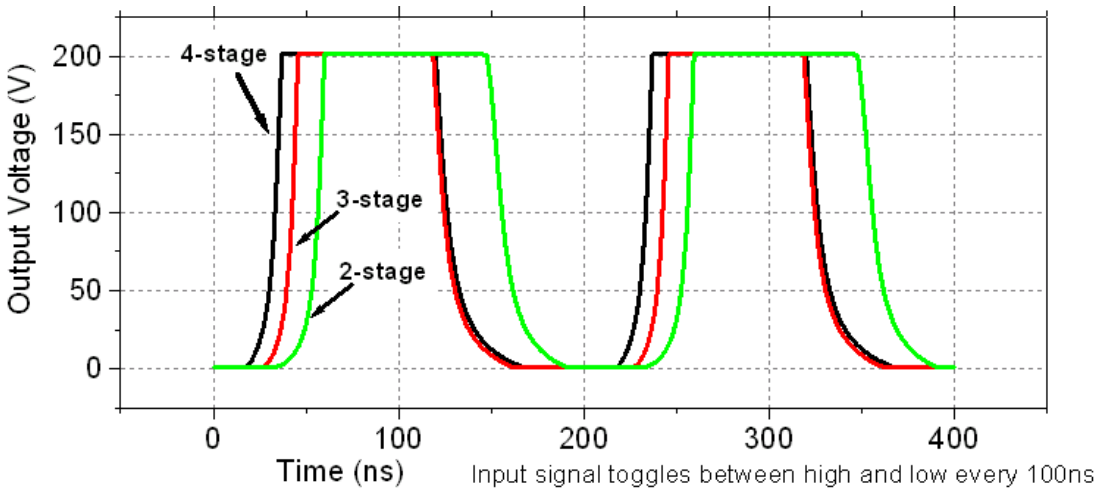


Fig. 4-18 Switching waveforms of 4-, 3- and 2-stage buffer driver circuits at 5MHz

When the number of stages is further reduced to 1, MHz switching is no longer possible due to a sharp increase in delay times. However, a single-stage logic inverter serving as a driver offers the simplest form of super buffer without the multi-stage voltage matching requirements. It is therefore an indispensible test structure and prototype cell for the development of the LJFET-based power integrated circuits.

4.5 Fabrication Process Consideration and Simplification

Since the complete process flow of VC-LJFET has been demonstrated during the development of lateral power devices, the fabrication procedure for the experimental demonstration of the integrated depletion-load gate buffer driver only requires minor process revision and simplification. Because of the low current and voltage requirements for the driver devices, top RESURF implantation, as well as the gate/drain metal thickening procedure is not required. VIA and overlay process can be simplified by using only one layer of metal. Other steps remain essentially the same.

A brief overview of necessary process steps for the integrated E-D mode buffer demonstration is listed below.

1. Clean wafer prior to fabrication
2. Gate trench etching by ICP Bosch process, followed by trimming in CF_4/O_2 plasma until desired mesa width is reached
3. Isolation trench etching by ICP with thick AlTi mask cover
4. Gate and isolation implantation by tilted and vertical aluminum ion doses

5. Drain contact region implantation

6. Post implantation annealing

7. Mesa top removal by ICP etching for source contact preparation

8. Oxidation and passivation

9. Ohmic contact formation by self-aligned Ni silicide process

10. Insulating layers deposition (polyimide and PECVD oxide/nitride) and VIA window opening for final overlay access

11. Deposit final overlay (Al-based) and pattern by wet etching

12. On-chip driver testing

4.6 Mask Design and Layout

The buffer driver modeling and optimization work has concluded with the following design parameters to be implemented in the photomask design:

1. For enhancement-mode LJFET with 0.36μm Wvc, a 0.56μm Wvc depletion-load LJFET of 1/5 size is an optimal match considering switching speed and DC voltage transfer characteristics. This configuration offers a switching fall time benefit of about 25% compared to a DC-equivalent resistor-load buffer.
2. Considering the imprecise control of channel openings in actual device fabrication, different widths have to be designed on the mask level. Wvc variation in depletion-load LJFET affects the speed capacity of the buffer driver but is not very critical for low-frequency functionality. The Wvc tolerance for enhancement-mode

JFET is however quite stringent. A window of only 0.1μm ~0.15μm in the enhancement-mode JFET channel opening is available for the buffer driver functionality.

3. At elevated temperature, power switching speed is significantly lower, and the tolerance room for Wvc variation is also slightly narrower than the room-temperature case.
4. The channel doping inaccuracy affects the buffer driver's effective Wvc. For doping variation range down to $3x10^{16}cm^{-3}$, the Wvc value needs to be made larger than the standard design by 0.1~0.2μm to offset the doping effect. For doping up of $8\ x10^{16}cm^{-3}$, the Wvc value needs to be made smaller than the standard design by 0.1~0.2μm.
5. The four-stage buffer driver design offers better speed than alternative buffers using fewer stages on the same chip area. However, the three and two-stage driver counterparts are not substantially poorer in switching performance, and can be implemented as good buffer circuits too. Fewer stages reduce the circuit's complexity and usually lead to better chance of functionality. The power IC with single-stage buffer or no buffer at all will perform switching at very low frequencies. They are apparently not optimal designs of the circuit, but single-stage logic inverters should be included on the mask as important test patterns and the simplest prototype of the depletion-load buffer driver.

Considering the above simulation conclusions, the mask Wvc parameters are designed with 5 variations. The center target is Wvc=0.36μm/0.56μm. Two wider designs (+0.1μm, +0.2μm) and two narrower designs (-0.1μm, -0.2μm) will largely compensate possible channel doping inaccuracies and process uncertainties affecting the channel width. In addition to four-stage buffer drivers, two-stage drivers as good alternatives are included on the mask drawing. Logic inverters are also designed for testing and trouble shooting

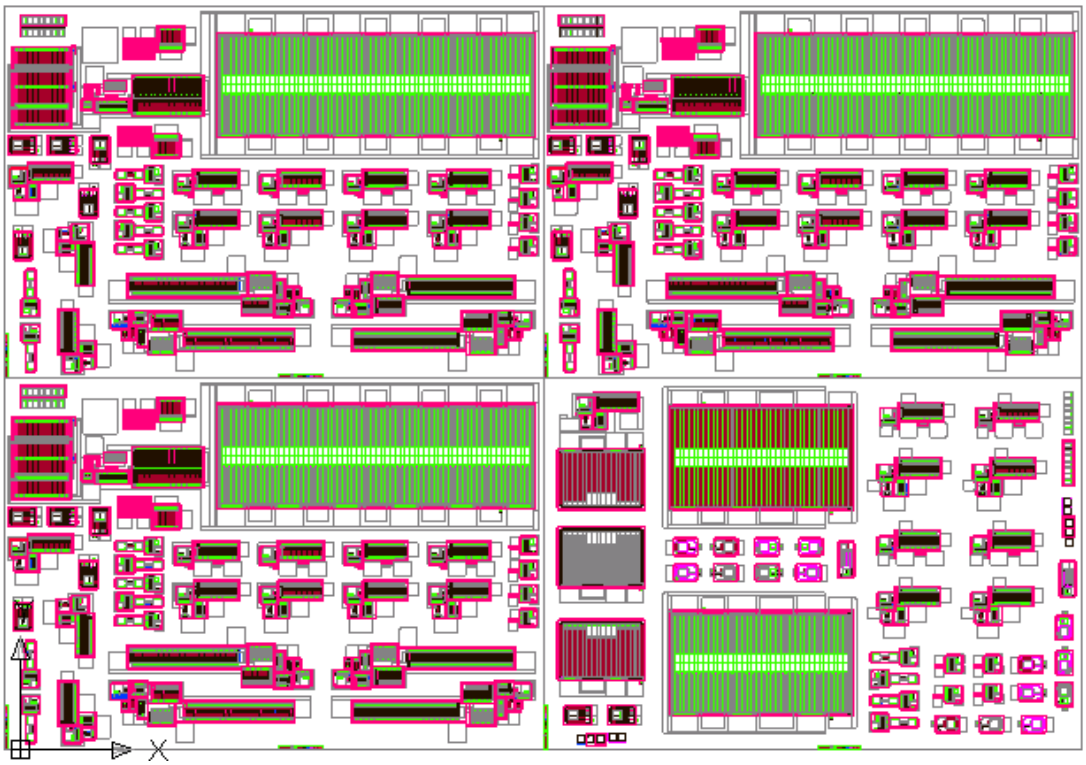


Fig. 4-19 Full block view of mask drawing (12.2mm x 8.4mm)

The mask drawing of a full block is shown in Fig. 4-19. The size of a full block is 12.2mm x 8.4mm, repeated on a 4-inch mask set. Roughly 30 full blocks can be fit into a 3-inch SiC wafer, giving an estimated device count as in Table 4-6.

Cell Name	Sub-block	#	Comments/Variations
TEST PATTERNS			
Alignment marks	A & B	240	
TLM (n and p)	A & B	120	
Isolation test pattern	B	60	
Gate-source shorting test	B	60	
Test diode for Vbr	B	180	Includes RESURF variation
FUNCTIONAL DEVICES			
Small UV	A	180	Small UV JFET integrated with a matching resistor
Integrated UV	A	90	UV JFET integrated with driver and power JFET
Small Power JFET	A & B	500	Includes Wvc variation and RESURF variation
Small 4D-mesa power JFET	B	300	Incl. Wvc variation and RESURF variation
Medium power JFET	B	60	Includes Wvc variation
Large power JFET	B	60	Includes Wvc variation
R-load inverter	A & B	480	Includes Wvc variation
D-load inverter	A & B	750	Includes Wvc variation
R-load 2-stage	A	360	Includes Wvc variation
R-load 2-stage diagnostic	B	120	Includes Wvc variation
D-load 2-stage	A	630	Includes Wvc variation
D-load 2-stage diagnostic	B	120	Includes Wvc variation
D-load 4-stage	A	360	Includes Wvc variation
Integrated medium IC	B	30	Integrated 2-stage buffer to medium power JFET

Table 4-6 Designed structure types and their number counts on 3-inch SiC wafer

Test structures designed on the photomask include alignment marks, TLM and other patterns. Functional devices include drift-length-revised power VC-LJFETs, resistor-load

and depletion-load inverters, two-stage buffers and four-stage buffers, an integrated version of the depletion-load power IC, as well as a UV-triggered power IC for a different project thrust.

The photomask set includes 8 layers, as in Table 4-7, and is manufactured by Photo Sciences, Inc. The drawing images for typical inverters and buffer drivers are shown in Fig. 4-20.

Layer name	Critical dimension
Finger mesa for gate trench etching	1.2μm
Isolation trench	3.0μm
P gate implant	5.0μm
P RESURF implant (optional)	5.0μm
N+ implant for drain	5.0μm
Metal for ohmic contacts	2.5μm
VIA for windows in insulating layers	2.0μm
Overlay	5.0μm

Table 4-7 Photomask layer details

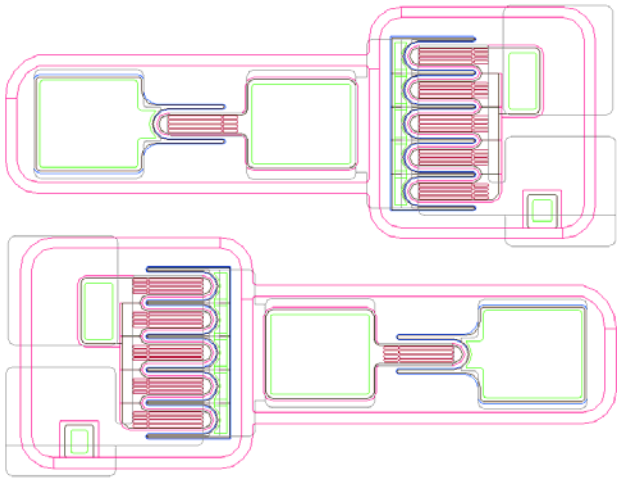


Fig. 4-20 (a) Two depletion-load logic inverters of varied Wvc designs

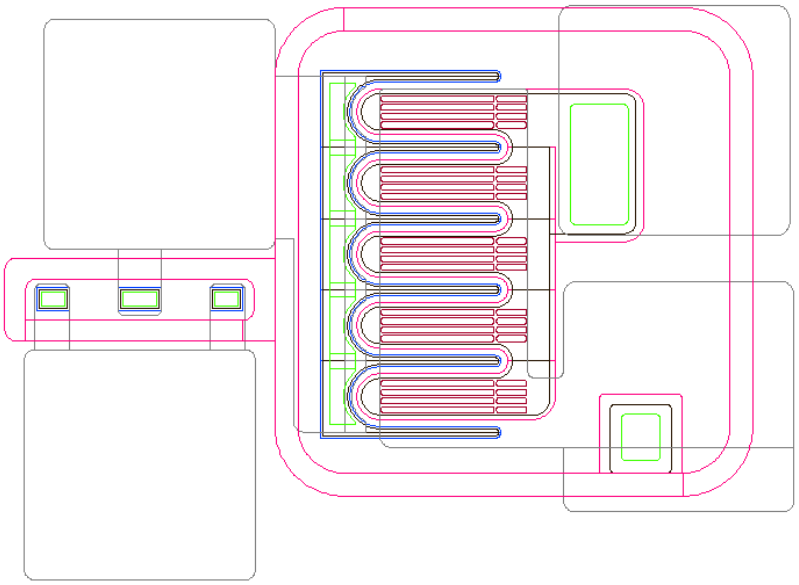


Fig. 4-20 (b) A resistor-load logic inverter

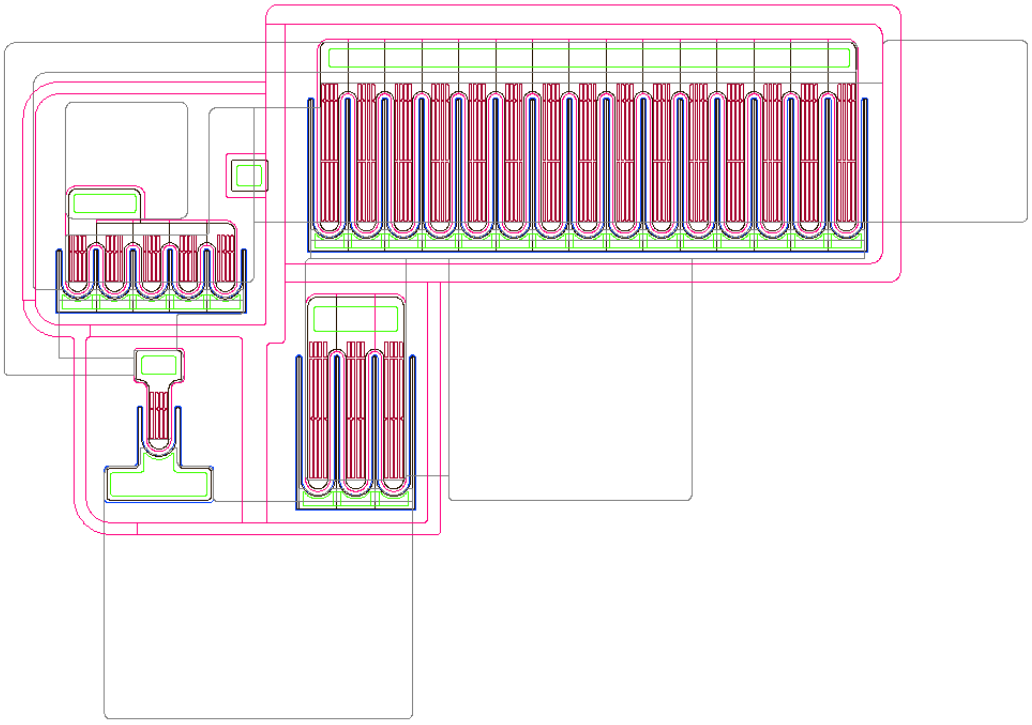


Fig. 4-20 (c) A depletion-load two-stage buffer driver

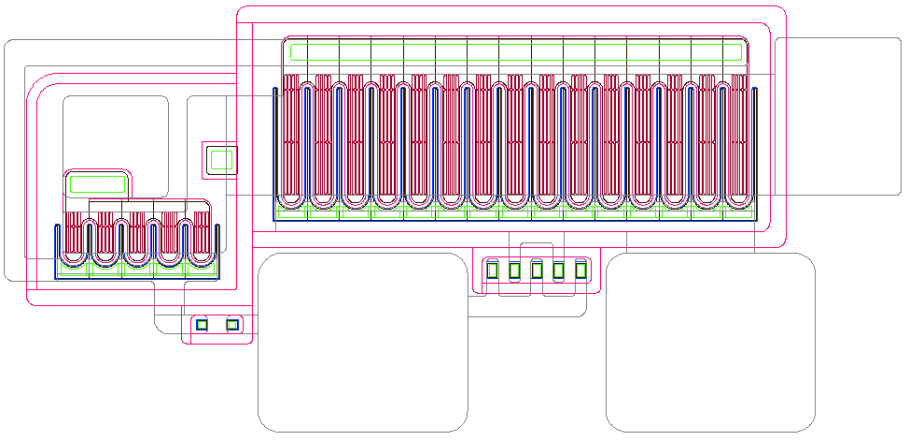


Fig. 4-20 (d) A resistor-load two-stage buffer driver

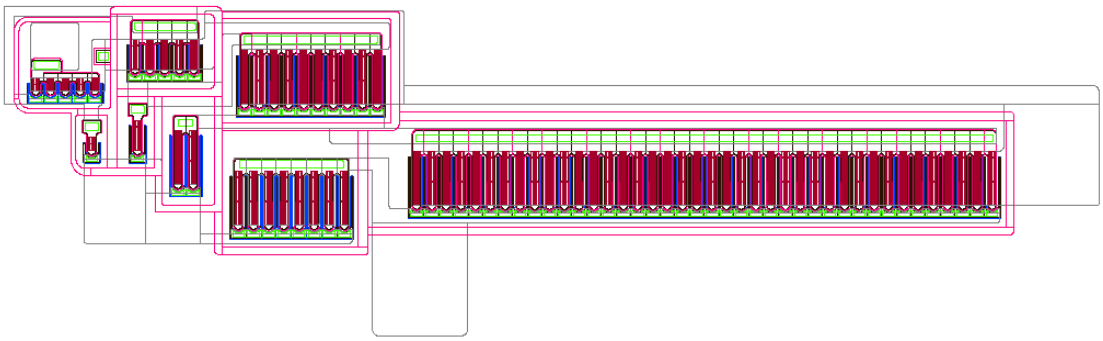


Fig. 4-20 (e) A depletion-load four-stage buffer driver

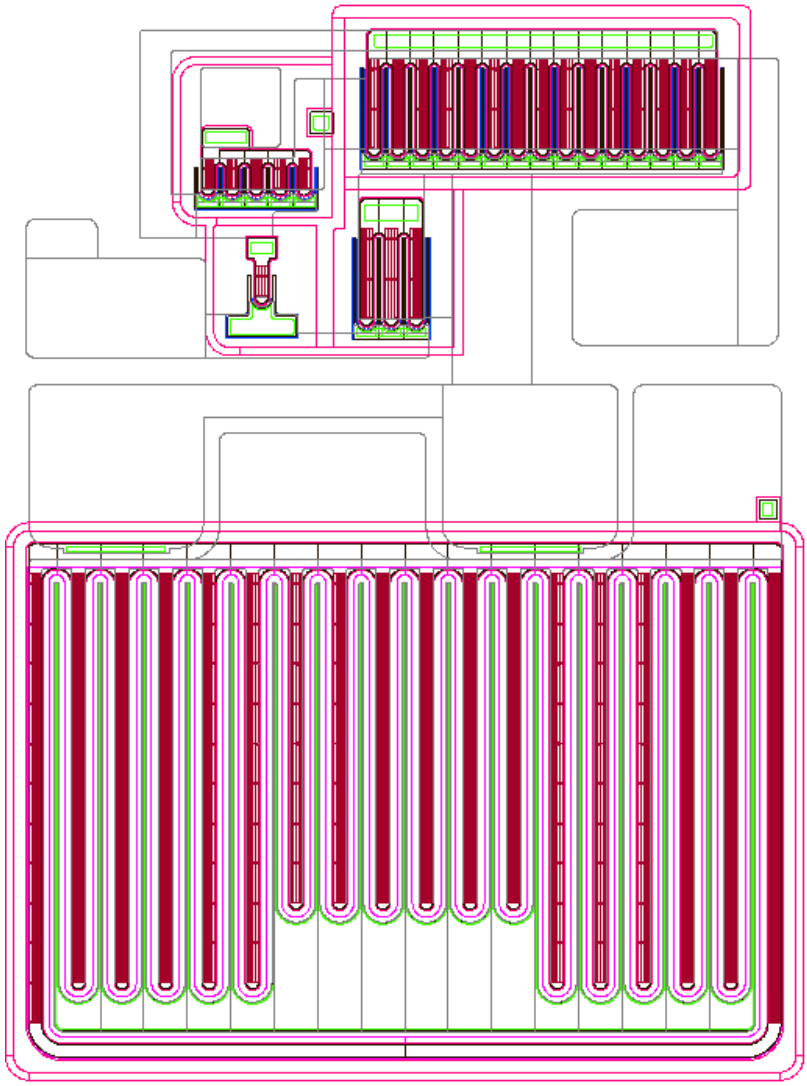


Fig. 4-20 (f) An integrated power IC (medium-size power device and two-stage buffer)

Fig. 4-20 Mask drawing for some device patterns

4.7 Wafer Fabrication for Second-generation Buffer Drivers

Upon the delivery of our photomask order, we started experimental fabrication of the designed buffer drivers. Major process steps are depicted in Section 4.4.

The 3-inch 4H-SiC wafer used for buffer fabrication is provided by Dow Corning Corporation, with an epilayer structure of Fig. 4-21. A photo of the wafer prior to any metal contact process is shown in Fig. 4-22.

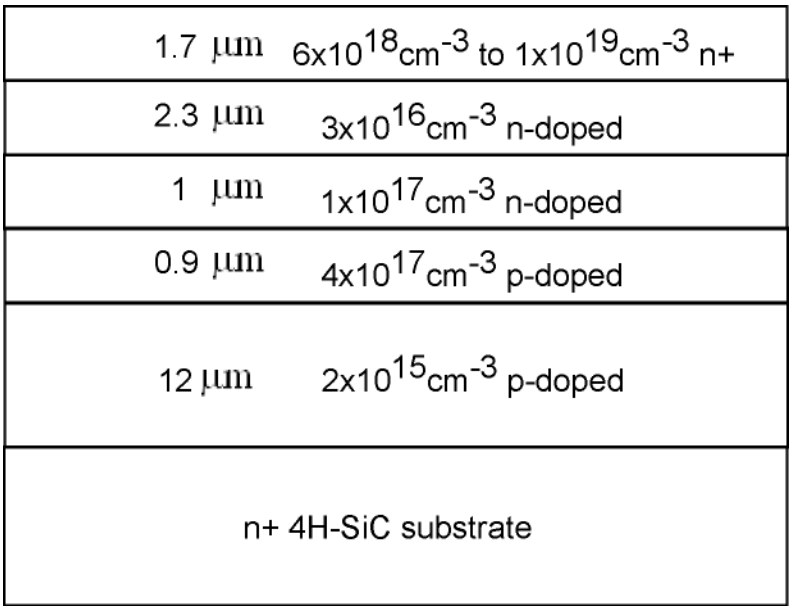


Fig. 4-21 Wafer structure for buffer fabrication

It is noted that an epilayer structural modification is made for this batch of JFET. Specifically, the top n+ layer thickness is reduced, which allows shallower gate trench etching than previously practiced and may afford better control of the vertical channel openings.

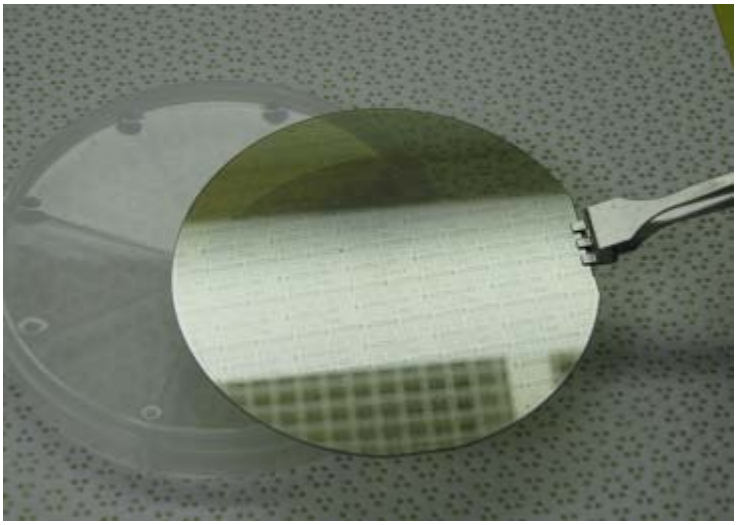


Fig. 4-22 Wafer photo before any metallization process

The buffer drivers designed in this dissertation are currently under wafer fabrication by anther graduate student of SiCLAB. Further experimental results on this effort will be reported separately when they become available.

CHAPTER 5 CONCLUSIONS AND SUGGESTIONS

5.1 Conclusions

In the efforts to develop a feasible technology on SiC for the realization of a robust power electronics system-on-chip, a fully integrated 4H-SiC power device and IC technology has been proposed based on lateral JFET structures. The extent of this work starts from the very initial process development for a reliable fabrication procedure of the VC-LJFET devices, including a thorough investigation and improvement of the TI-VJFET technology. These efforts have enabled the successful implementation of a novel metal contact formation scheme in SiC vertical-channel JFETs, and the experimental demonstration of the world's first normally-off lateral power JFET device on this material. The high-voltage JFETs fabricated on this device platform are among the best lateral power devices in the $BV^2/R_{ON,SP}$ figure of merit. Upon the experimental confirmation of the power LJFET concept, a monolithically integrated gate drive buffer circuit on the same lateral device technology platform is investigated. Modeling and optimization work for the power ICs using various circuit topologies is accomplished. The integrated power device and buffer driver are found capable of high-voltage power switching at frequencies up to a few megahertz. Photomask and process design for the experimental demonstration of these buffer drivers has also been completed.

The research results accomplished in this dissertation in many ways contribute to the continued efforts in the development of SiC power electronics technologies. From the process technology of SiC ohmic contacts to the design considerations of an integrated

SiC power switch system, scientists in this technical community may find useful information from more than one aspects of this work. With the superior material advantage of SiC over silicon, power device and circuit technologies based on this semiconductor could seriously challenge the Si dominance in power electronics market in the near future. Among various choices of device structures, the SiC VC-LJFET platform described in this dissertation is believed to offer a competitive and attractive solution for the power integration applications in SiC.

The accomplishments of this dissertation research can be summarized as the followings:

1. The original TI-VJFET process is reviewed. Troubling procedures are identified for improvements. The VC-LJFET process is then designed based on the improved JFET fabrication technology and certain unique considerations for lateral devices.

2. A novel self-aligned Ni ohmic contact process is developed for SiC TI-JFET structures. In this procedure, simultaneous formation of source, gate and drain ohmic contacts can be made without the need for critical lithography.

3. An interesting dependence of Ni to SiC ohmic contact resistances on the annealing temperature is observed and analyzed. The findings are supportive to a recent carbon-vacancy explanation of the Ni-SiC ohmic contact formation mechanism.

4. The full process flow of the power VC-LJFET is explored, leading to the demonstration of the first normally-off power lateral JFET on 4H-SiC.

5. Numerical modeling and compact parameter extraction of high-voltage and low-voltage VC-LJFET devices is performed for the circuit-level simulation of gate buffer drivers and power ICs.

6. Resistor-load and depletion-load versions of gate buffer drivers are studied in PSPICE for performance comparison and design window investigations. It is found that using depletion-load buffers could reduce the high-voltage switching fall time of the driven power LJFET by 25~50% compared to the DC-equivalent resistor-load buffer drivers.

7. The second-generation SiC LJFET-based power ICs are designed and implemented on the mask level.

5.2 Future Work Suggestions

To further improve the power LJFET devices for integrated power electronics, the following challenges remain to be addressed. [57]

Firstly, critical device dimensions can be further shrunk. An inspection of the fabricated device cross-sectional structure reveals that it has a unit cell width of over 20 μm with 5~8 μm responsible for blocking voltage. The other portions include a P+ gate ohmic contact region, as well as an N+ drain region. Shrinking of these dimensions can help reducing the LJFET specific on-resistance by both increasing the cell density and reducing unit-cell device resistance. In addition, the trench width and channel length can also be reduced to further lower the device resistance. Improved photolithographic resolution as well as refined process control can lead to such improvements. It is

predicted that a specific on-resistance as low as 3 to 4mΩ·cm^2 is possible for a 1.2 kV device, challenging even the best performance figures obtainable from vertical SiC devices. Secondly, parasitic capacitances of the LJFET should be minimized to further reduce the device switching losses in power switching circuits as well as to increase the switching frequency of these circuits. Capacitances between gate and source (Cgs) and gate and drain (Cgd) play a dominant role in determining the switching frequency of these devices and their efficiency in a high frequency circuit. Cgs can be reduced by minimizing or avoiding the contact between the gate P+ region and the source N+ region. Cgd can be reduced by narrowing the gate P+ regions and/or by shielding the gate region from the drain by ground plane field-plating. It is expected that the device switching losses in a hard-switching circuit can be substantially reduced if these two capacitances are minimized. Thirdly, the device structure and process can be further optimized for high power and high temperature applications. Designing a normally-off JFET becomes increasingly challenging as the targeted operation temperature increases. A more robust device and process design, plus the state-of-the-art facilities will be required to overcome these challenges. Lastly, the very high temperature potential (> 600°C) of SiC JFET devices calls for substantial advances in high temperature packaging technologies. Promising as they are, the unique capabilities of SiC JFETs can make a practical impact only after robust high-temperature packaging solutions become available.

In addition, the low-voltage portion of SiC LJFET-based power integrated circuit is still in its very primitive stage. A fully integrated smart power technology requires not

only the gate driving buffers, but also signal generation, processing and control modules as well as various analog and digital functional blocks and protection circuits. [58] The theoretical study and experimental demonstration of these circuits are highly attractive, and will pave the way for the VC-LJFETs towards the ultimate goal of a power electronics system-on-chip technology in SiC.

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CURRICULUM VITA

Ming Su

09/2004 – 05/2010	Ph.D. in Electrical and Computer Engineering Rutgers, The State University of New Jersey New Brunswick, New Jersey, USA
09/2004 – 05/2006	M. S. in Electrical and Computer Engineering Rutgers, The State University of New Jersey New Brunswick, New Jersey, USA
09/2002 - 05/2004	Graduate studies in Electrical Engineering University of South Carolina Columbia, South Carolina, USA
09/1998 – 07/2002	B. Eng. in Electronic Engineering Tsinghua University Beijing, China

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