SIMULATION, MODELING AND CHARACTERIZATION OF SIC DEVICES

By

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ABSTRACT OF THE DISSERTATION

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With superior material properties, Silicon carbide (SiC) power devices show great potential for high-power density, high temperature switching applications. Among all the power device structures, SiC MOSFET attracts the most attention because of its high gate input impedance, simple gate control and fast switching speed. However, low inversion channel mobility, high near-interface state density close to the conduction band edge, questionable oxide reliability as well as theoretical limit on the device figure-of-merit still remain to be significant challenges to the development of SiC power MOSFETs.

In this dissertation, all of the above challenges are addressed from various approaches. First, simulations on the super-junction structure show that the unipolar theoretical limit of SiC can be broken even with the state-of-the-art processing technologies. An easy-to-implement analytical model is developed for calculations of the blocking voltage, specific on-resistance and charge imbalance effects of 4H-SiC super-junction devices. This model

is validated by extensive numerical simulations with a large variety of device parameters. Device design and optimization using this model are also presented.

Second, a wafer-level Hall mobility measurement technique is developed to measure channel mobility more accurately, more efficiently and more cost-effectively. Device characterization and development are much more convenient by using this technique. With this method, further explorations of interactions between interface traps and channel carriers as well as device degradation mechanisms become possible.

Third, reliability of SiO_2 on 4H-SiC is characterized with time dependent dielectric breakdown (TDDB) measurements at various temperatures and electric fields. Lifetime prediction to normal operation conditions suggests that the oxide on SiC has a characteristic lifetime of 10 years at 375 °C if the oxide electric field is kept below 4.6 MV/cm. The observed excellent reliability data contradict the widespread belief that the oxide on SiC is intrinsically limited by its physical properties. Detailed discussions are provided to re-examine the arguments leading to the misconception.

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1 INTRODUCTION

1.1 Material properties of Silicon Carbide

In recent years, silicon carbide (SiC) has attracted extensive attention for power semiconductor applications because of its superior material properties that show great promise for high power density switching applications. A comparison of some material properties of several important semiconductors is listed in Table 1.1 [1]. When compared to silicon, SiC has three times wider bandgap (E_g), ten times higher critical electric field (E_c), nineteen orders of magnitude lower intrinsic carrier concentration (n_i), three times larger thermal conductivity (λ) and two times higher saturation velocity (v_{sat}). These characteristics show great potential to make power devices that can operate at higher power, higher temperature and higher frequency with lower leakage current, smaller conduction and switching losses, less stringent requirements in heat removal etc. With these high-performance power devices, more efficient and compact power systems become possible. Among the three SiC polytypes, 4H-SiC is more favorable due to its wider bandgap, higher carrier mobility with more isotropic nature compared to 6H-SiC.

Table 1.1 Material properties of important semiconductors [1]

Material	E_g [eV]	n_i [cm^{-3}]	ε_r	μ_n [$cmV^{-1}s^{-1}$]	E_c [MV/cm]	v_{sat} [10^7 cm/s]	λ [$Wcm^{-1}K^{-1}$]
Si	1.12	1.5×10^{10}	11.8	1350	0.3	1.0	1.5
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	2.0	0.5
GaN	3.39	1.9×10^{-10}	9.0	900	3.3	2.5	1.3
3C-SiC	2.2	6.9	9.6	900	1.2	2.0	4.5
6H-SiC	3.0	2.3×10^{-6}	10	370[a] 50[c]	2.4	2.0	4.5
4H-SiC	3.26	8.2×10^{-9}	9.7	720[a] 650[c]	3.0	2.0	4.5
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20

Wide bandgap material technology is far less mature than silicon-based technology. Does it really worth the effort to push the development of wide bandgap power devices? In some applications that require the electronics to work with high temperature, high voltage or high efficiency, Si power devices are physically limited by its material properties.

a) High temperature: The intrinsic carrier density is a very sensitive function to temperature. In Si devices, there can be more intrinsic carriers than dopant carriers at temperatures beyond 300 °C. The desired operation of semiconductor devices relies on the local concentration of carriers. As temperature increases, the circuit functions can be seriously degraded or fail. In some high temperature electronics applications where the environment temperatures are higher than 600 °C, for example space exploration, deep-well drilling or automobile exhaust sensing and control, it is impossible to design a functional system using silicon power devices [2]. Furthermore, when the ambient temperature is high, the control circuit has to either reside in a cooler remote area, which requires extra wiring and connectors, or demand active cooling with air or liquid, which adds extra weight to the system. In some applications such as aircraft systems, these overheads may reduce the efficiency as well as raise serious reliability issues that can cause fatalities of passengers. On the other hand, even if the environment temperature is not that extreme, for example < 100 °C, the junction temperature inside power devices can still be high because they have to handle high power density and the power losses in the devices translate to heat dissipation and hence high junction temperature. In this case, heat removal is essential to the system, which may add extra complexity and cost.

b) High voltage: In the design of power semiconductor devices, lightly-doped long drift region is necessary in achieving high blocking voltage. In the high voltage power transmission applications, blocking voltage of tens of thousands volts is often required. In order to meet the targeted blocking voltage, a drift region thicker than 1000 μm is required for Si-based devices, which is not practical in fabrication. The much higher breakdown electric field of SiC compared to Si enables reduction of drift region thickness by nearly 10 times, which combined with 10 times higher doping concentration permit a roughly 100 times decrease in the drift region resistance that dominates the total on-state resistance.

c) High efficiency: Significant energy losses in many Si high-power circuits arise from semiconductor switching energy loss. High switching frequency in power circuits is highly desirable because it enables use of smaller capacitors, inductors and transformers, which greatly reduces the size and weight of the system. The wide bandgap as well as the high breakdown electric field of SiC permit faster switching that increases switching frequency at certain energy budget or improves system efficiency with a fixed switching frequency. Furthermore, the energy losses when the device is conducting current or blocking voltage are much smaller as well due to 100 times lower on-resistance and much lower leakage current than Si devices, which further improves the circuit efficiency by reducing energy losses when the device stays on and off. Minimizing energy loss is essential in the power systems of hybrid electric vehicles, where heavy heat sinks and/or complex active cooling system are highly undesirable. With SiC devices, the power system can operate at higher temperature, generate less heat and require much simpler cooling.

Among the wide bandgap materials, SiC and GaN are the most developed [3, 4]. In addition to the comparable material properties to SiC, such as bandgap, electron mobility, saturation velocity etc, GaN become more competitive to SiC mainly because it can be grown on cheap substrates like Si and sapphire, as well as High Electron Mobility Transistor (HEMT) can be realized by forming two dimensional electron gas (2DEG) at the interface of AlGaN/GaN. However, the fact that SiC bulk crystals had orders of magnitude fewer dislocation defects than GaN made it a more preferable candidate for wide bandgap research. As a result, SiC is more advanced in some important fabrication technology areas such as control of impurity doping, fabrication of reliable Ohmic contacts etc. Moreover, vertical power devices cannot be implemented on GaN film grown on Si substrate, therefore device with high power density is hard to achieve. Furthermore, native oxide can be grown on SiC, which offers the potential of making more reliable MOS-based devices, such as MOSFET and IGBT.

1.2 Overview of SiC power devices

Power switch is an essential component in any power electronics system, which determines the functionality, controllability and efficiency of the system. An ideal power device works like a switch, conducting current with no voltage drop at on-state and blocking high voltage with no leakage current at off-state.

Bipolar Junction Transistor (BJT), Junction Field Effect Transistor (JFET), Insulated Gate Bipolar Transistor (IGBT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are the major types of structure that are usually employed in power circuits.

BJT is a bipolar device, in which the conductivity of (part of) the collector region is modulated by the minority carrier injection at on-state, which can lead to reduced on-resistance. However, in SiC BJT, the forward voltage drop increases significantly after high current stress due to recombination-induced stacking faults migration in the drift layer [5]. Therefore minority carrier injection should be avoided in SiC-based power devices unless material quality has been greatly improved. The bipolar nature of BJT also limits the switching frequency because of charge storage in the device. Furthermore, as a current-driven transistor with a relatively low current gain, complicated gate drive circuit is required to control the device.

JFET is a voltage-controlled unipolar device, which can be controlled by simpler gate drive and does not have the stacking faults migration problem compared to BJT. However, it is difficult to design normally-off JFET without significantly sacrificing the device performance (on-resistance or blocking voltage). Although normally-on device is able to handle more current density, it conducts current even when the gate bias is not applied. Therefore more complex gate drive and protection circuits are required in case of accidental failures of the gate control signal.

IGBT is basically a bipolar transistor driven by a power MOSFET. It has the advantages of being a bipolar device, as discussed with BJT, and low impedance of the insulated gate that require simple gate drive circuits. However, similar to BJT, the bipolar nature gives rise to the recombination-induced stacking faults migration, and the switching speed is limited as well. Moreover, the forward voltage drop is greater than 2.7 V due to the built-in voltage in the SiC p-n junction, which confines the practical use of SiC IGBT to applications where the blocking voltage is higher than ~5 kV.

MOSFET structure is advantageous over other devices. The gate input impedance is much smaller even compared to JFET, so that the gate drive circuit requires very little power to control. The uni-polar nature permits faster turn-on and turn-off speed compared to BJT and IGBT, and there is no stacking faults migration problem. In contrast to IGBT, there is no built-in forward voltage drop.

The two most favorable power MOSFET structures are DMOSFET and UMOSFET. Their structures are depicted in Fig.1.1 and Fig.1.2 respectively. The primary difference between them is the placement of channel region. In DMOSFETs, the inversion channel is located laterally on the surface of the implanted pwell region, whereas in UMOSFETs, the channel is in vertical direction on the surface of the trench in the epitaxial p layer. UMOSFETs has lower on-resistance compared to DMOSFETs due to the absence of the JFET region and higher channel mobility. However, the blocking voltage is limited by the oxide breakdown at the trench corners.

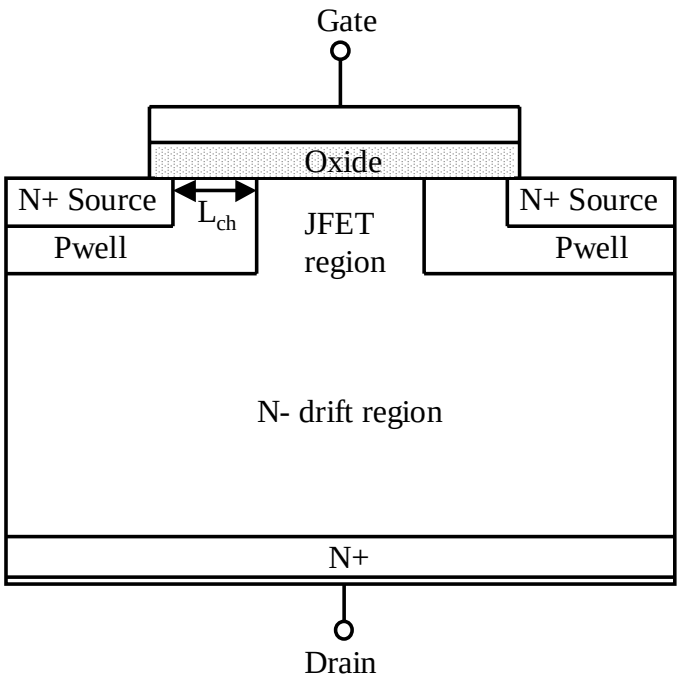


Fig.1.1 Cross-sectional view of n-channel DMOSFET

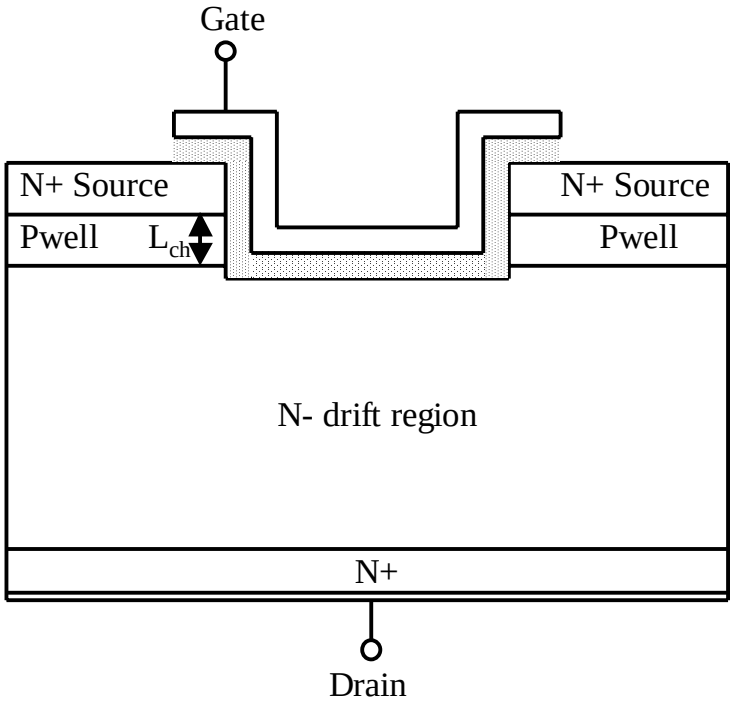


Fig.1.2 Cross-sectional view of n-channel UMOSFET

1.3 Challenges to the development of SiC power MOSFETs

Although SiC power MOSFET has many advantages compared to its silicon counterparts as well as other types of SiC switches, several technological challenges remain to be surmounted.

a) Theoretical limit on uni-polar device performance

Attentions were drawn to SiC power devices in late 1980s because the power switching devices based on Si were approaching to its theoretical limit [6],

$$R_{SP\_ON} = \frac{4V_B^2}{\mu_n \varepsilon_s E_C^3} \qquad \text{Eq.1.1}$$

where R_{SP_ON} is the specific on-resistance in Ωcm^2, V_B is the blocking voltage, μ_n is the electron mobility, ε_s is the permittivity of the semiconductor and E_C is the critical electric field. The ten times higher critical electric field of SiC compared to Si enable large improvements on the performance to break the theoretical limit of Si. After decades of extensive study, SiC power devices have achieved remarkable performances in recent years. The Figure-of-Merit (V_B^2/R_{SP_ON}) of SiC power MOSFETs is approaching its theoretical limit. Table 1.2 summarizes the breakdown voltage and specific on-resistance of some of the most representative MOSFETs fabricated in the past decade. The R_{SP_ON} versus V_{BR} of these devices are plotted in Fig.1.3 as well as the theoretical uni-polar limits of Si and 4H-SiC calculated based on Eq.1.1 and Table 1.1. This trend of improvement towards the uni-polar theoretical limit also holds for other types of uni-polar devices made of SiC. The Figure-of-Merit as high as 485 MW/cm^2 and 827 MW/cm^2 have been reported on 700 V 4H-SiC JFET [7] and 1.7 kV 4H-SiC JFET [8] respectively. These Figure-of-Merits are not far from the theoretical 4H-SiC unipolar limit. With the current trend of device performance improvement, it is expected that the Figure-of-Merit of 4H-SiC device will be limited by its own theoretical limit in the near future. Therefore, research on developing innovative device structures on SiC is necessary to improve the device performances.

Table 1.2 V_{BR} and R_{SP_ON} of representative MOSFETs

V_{BR} [V]	R_{SP_ON} [$m\Omega cm^2$]	Year	Affiliation	Ref.
790	1.7	2009	Rohm	[9]
900	2.9	2009	Rohm	[9]
1100	5.7	2009	Denso	[10]
660	1.8	2009	AIST	[11]
990	8.3	2008	GE	[12]
1000	6.95	2007	Purdue	[13]
1500	8	2007	GE	[14]
1300	7	2007	Mitsubishi	[15]

1200	5	2006	Mitsubishi	[16]
1100	4.3	2006	AIST	[17]
1800	8	2006	CREE	[18]
2000	10.3	2005	CREE	[19]
900	9.95	2004	Purdue	[20]
600	8.5	2004	AIST	[21]
10000	123	2004	CREE	[22]
2400	42	2002	CREE	[23]
1600	27	2002	CREE	[24]
5000	88	2002	Kansai, CREE	[25]
5050	105	2002	Purdue	[26]
4580	387	2000	Kansai, CREE	[27]
1800	82	1999	Siemens	[28]

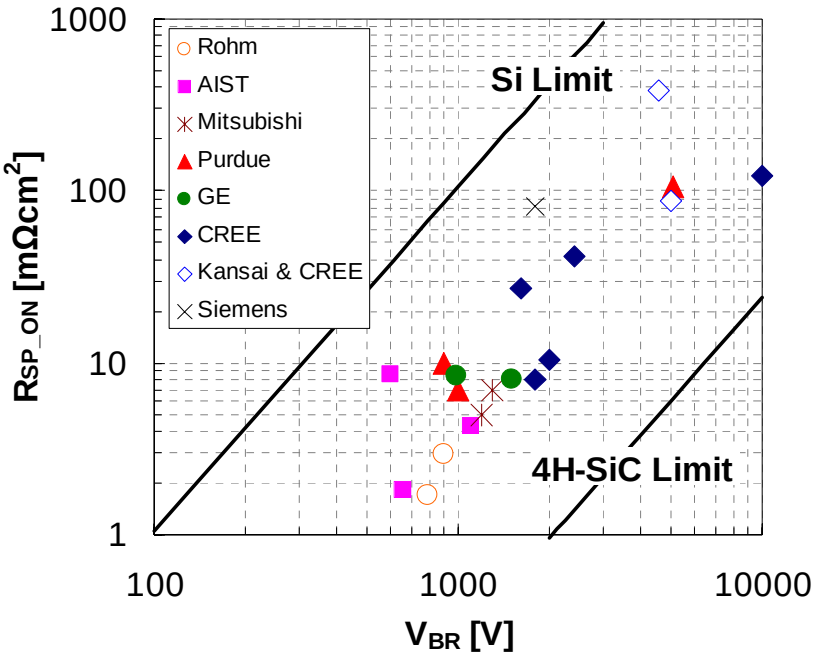


Fig.1.3 Specific on-resistance versus breakdown voltage for the representative MOSFETs fabricated in the past decade. The theoretical limits of 4H-SiC and Si are also shown.

b) Low channel mobility

The uni-polar theoretical limit mentioned above only considers the drift region resistance. However, for devices with blocking voltage of 1 kV or lower, the total on-resistance is dominated by the channel resistance [29]. The channel resistance could be

minimized by shorten the channel length and improve the channel electron mobility. Device optimizations with sub-micron gate length are under development [13, 29].

The channel mobility values measured in the state-of-the-art SiC MOSFETs are much lower than expected. It is believed that the poor inversion mobility is caused by the high interface state density (D_{IT}) near the conduction band edge with the following two effects. First, substantial fraction of channel electrons are trapped by the oxide defects so that they no longer contribute to the channel current. Second, those trapped electrons give rise to the Coulomb scattering of the free electrons remaining in the channel and further reduce the electron mobility [30]. Continuous improvements to the 4H-SiC/SiO_2 interface have resulted in further D_{IT} reduction near the conduction band edge and hence a higher channel electron mobility [31]. Several processing technologies have been developed to enhance the mobility, such as incorporation of a post-oxidation nitric oxide (NO) or nitrous oxide (N_2O) anneals [32, 33], nitrogen ion implantation [34], alternative crystal orientations of (11-20) [35] and (000-1) [36] and sodium enhanced oxidation [37]. However, the exact picture of the SiC/SiO_2 interface still remains unknown, and the channel mobility has to be further improved to make SiC power MOSFET more competitive with Si power devices.

c) Oxide reliability

In the realization of power MOSFETs that have practical use, the reliability of the gate oxide is extremely important. It is widely believed that the reliability of silicon dioxide grown on SiC is physically limited [38], especially at high temperatures [39, 40]. The concern is mainly because the conduction band offset between SiC and SiO_2 is lower than that between Si and SiO_2, and the Fowler-Nordheim tunneling current is

exponentially dependent on the conduction band offset. In the literature, only a limited amount of work has been performed on SiC oxide reliability. Some early research shows that the oxide is not reliable under high electric field (> 4 MV/cm) or high temperature (> 150 °C) [41, 42]. However, at the time of the above research, the oxide defect density was a few orders of magnitude higher than in the devices fabricated nowadays, therefore the conclusion was obscured by the extrinsic defects in the oxide.

Recently, with continuous improvements of processing technologies, more measurements of oxide reliability on SiC showed great promise that silicon dioxide on SiC is reliable. Matocha et al. [43] reported a mean-time-to-failure (MTTF) of 2300 hours at 6 MV/cm and 250 °C on MOS capacitors thermally grown with N_2O and NO annealing. Yu et al. [44] reported $t_{63\%}$ of 215 hours measured at 6.4 MV/cm and 375 °C. Using TDDB with constant current stress, Fujihira et al. [45] found that charge-to-breakdown (Q_{BD}) increased from 0.1 C/cm^2 to 10 C/cm^2 by employing N_2O annealing.

In the oxide lifetime projection, the field-acceleration model and the field-acceleration factor employed in the lifetime prediction are of crucial importance. The recently observed change of the field-acceleration factor raises concerns about change of breakdown mechanisms at lower electric fields and the validity of the lifetime projection [46]. Long-term reliability tests are necessary for further understanding of the intrinsic oxide reliability.

1.4 Thesis outline

The challenges for SiC power devices discussed above are mainly two fold, low on-resistance and good reliability. In this thesis work, all of these challenges are addressed from different aspects.

Depending on the application or blocking voltage required, the on-resistance can be dominated by drift region resistance for (V_{BR} > 3 kV) or dominated by the channel resistance (for V_{BR} <1 kV). In Chapter 2, the super-junction structure in 4H-SiC is studied through numeric simulations to find its capability for reducing drift region resistance and breaking the uni-polar theoretical limit. An easy-to-implement analytical model is developed for efficient device design and optimization. In Chapter 3, the focus is the channel resistance, which is limited by the low channel mobility. In order to understand the mobility degradation mechanisms, accurate measurement of the mobility is a prerequisite. Therefore, Hall mobility should be measured instead of the field effect mobility or effective mobility because of the high oxide trap density in SiC MOSFETs. However, regular Hall mobility measurement requires tedious sample preparation that is very time-consuming. In this work, a wafer-level Hall mobility measurement technique is developed to measure Hall mobility accurately with much less experimental efforts.

In Chapter 4, the long-term oxide reliability is studied systematically at various stress temperatures and electric fields. Lifetime projections are provided. Field acceleration factor and the breakdown mechanisms are discussed. A more accurate way of extracting Weibull slope β is presented by employing area scaling. Evidences are presented to answer the questions “Whether this good oxide reliability is intrinsic yet? Is there any room for further improvement?” Since the good oxide reliability data contracts the widely

accepted belief that the silicon dioxide on SiC can never be reliable, a detailed discussion is provided to re-examine the early arguments leading to the misconception.

2. SIMULATION AND MODELING OF SiC SUPER-JUNCTION STRUCTURES

2.1 Introduction

One of the main objectives in the design of power semiconductor devices is to obtain high breakdown voltage (V_{BR}) at off state while keeping the specific on-resistance (R_{SP_ON}) as low as possible. However, high V_{BR} and low R_{SP_ON} impose conflicting requirements on device structural parameters. There is a well-known trade-off, $R_{SP\_ON} \propto V_{BR}^{2.4\text{-}2.6}$ [47], between the two sought performances for a unipolar power semiconductor device. The Baliga's figure of merit (FOM), defined as V_{BR}^2 / R_{SP_ON}, is therefore used to evaluate quantitatively the superiority of a device. The FOM of unipolar devices made on 4H-SiC can theoretically be close to three orders of magnitude higher than their silicon counterparts. With a large amount of research efforts invested, SiC power devices have achieved remarkable performances in recent years [7, 8]. With the current trend of device performance improvements, it is expected that 4H-SiC device FOM will approach its own theoretical limit in the near future. New device structures and approaches are needed to maintain a continued reduction of device specific on-resistance.

Super-junction structures (also called CoolMOS, charge compensation [47, 48]) using 4H-SiC were proposed to break this limit and provide exciting prospects for much better device performances. Such structures involve the realization of long and narrow N and P stripes over a large device area and its fabrication process have been recognized as challenging. Nevertheless, SiC dry etching process to produce long and narrow N and P stripes have already been developed and mesas and trenches with relatively high aspect ratio (i.e., height to width ratio more than 4 to 1) are already practically feasible.

In this work, the structures and approaches that will be able to break the 4H-SiC theoretical unipolar limit will be analyzed quantitatively. While the idea of super-junction or buried floating region on SiC has been studied in the literature [49, 50], the focus has been on their comparison with super-junction on silicon. Its potential in breaking the SiC limit and effects of important structural parameters have not yet been fully revealed. In this work, the super-junction structure on 4H-SiC will be studied systematically over a wide range of possible design parameters by extensive 2D numerical simulations.

In the super-junction device design and optimization process, simulating a large number of structures with different combinations of parameters (for example device dimensions, doping, charge imbalances etc.) is very time-consuming. Therefore, a good and compact model for this 4H-SiC super-junction structure is desired to quickly and easily predict R_{SP_ON} and V_{BR} as well as to give the optimal device parameters according to certain design constraints. In the literature, several models for the super-junction structure based on Si were reported [51-53]. However, these models involve multiple complicated infinite series in their electric field equation. To implement these equations and to calculate a device breakdown voltage based on a given set of physical parameters will involve substantial amount of human and computational effort. Moreover, charge imbalance effect was not well modeled. In the current processing technology of SiC devices, the activation efficiency of p-type dopant cannot be controlled as precisely as in Si technology. This can lead to significant charge imbalance to the SiC super-junction devices (if doping is introduced through implantation) and degrade their breakdown voltage.

In this work, a simpler model is developed to predict R_{SP_ON} at on state and V_{BR} at off state accurately for 4H-SiC super-junction structures. The accuracy has been confirmed by numeric simulation results using Silvaco simulator with various structural and geometrical parameter combinations. The influence of charge imbalance is also incorporated into this model with very good accuracy. Using this model, the optimal design methods for 4H-SiC super-junction devices for a given set of constraints are also discussed. This is helpful for the design of such a structure for practical fabrication.

2.2 Simulation Results

The cross-sectional view of a 4H-SiC super-junction MOSFET is shown in Fig.2.1. The super-junction structure replaces the homogeneous drift region in conventional structure with a composition of N and P doped stripes. When the device is reverse biased, a lateral junction is formed across the NP stripes, and two abrupt junctions are formed at the two vertical ends of the drift region. With very narrow stripes, the drift region can be fully depleted easily by the lateral junction, while the depletion regions of the other two vertical abrupt junctions have not yet grown too far into the bulk of the drift region. After full depletion, as the reverse bias voltage further increases, the electric field grows almost uniformly across the drift region, because there is no further variation on the charge distribution in the drift layer. With a more uniform electric field distribution along the drift region, breakdown occurs at a much higher voltage compared with a conventional unipolar structure. In addition to the higher breakdown voltage for a given drift region length, this structure is also advantageous on device specific on-resistances because the doping of N and P stripes can be raised to a level much higher than possible in the

conventional structure. Devices with such a structure is therefore known to have the capability of achieving a specific on-resistance lower than the theoretical one-dimensional limit.

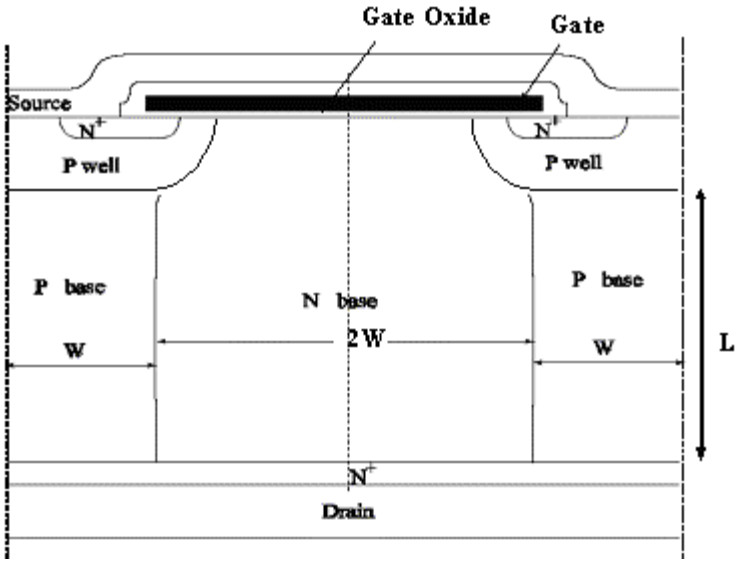


Fig.2.1 Cross-sectional view of the super-junction MOSFET

In this simulation work, Silvaco ATLAS is employed as the simulator. Impact ionization rates are crucial in the modeling of breakdown voltage. The following model is used [54]:

$$\alpha_n = a_n \exp[-\frac{b_n}{E}], \qquad \alpha_p = a_p \exp[-\frac{b_p}{E}] \qquad \text{Eq.2.1}$$

where α_n and α_p are ionization rates for electrons and holes in 4H-SiC respectively. The parameters $a_n = 1.14\times10^9$ cm^{-1}, $b_n = 3.8\times10^7$ cm^{-1}, $a_p = 6.85\times10^6$ cm^{-1}, $b_p = 1.41\times10^7$ cm^{-1} are selected by fitting experimental data presented by Konstantinov et al. [55] These parameters had been used in simulation and fitted well with experimental results of devices made by our group [56, 57]. Electron mobility model counting doping dependence is used [58]:

$$\mu_n(N) = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + (\frac{N}{N_{ref}})^{\alpha}} = 40 + \frac{950 - 40}{1 + (\frac{N}{2e17})^{0.76}} \qquad \text{Eq.2.2}$$

To evaluate the blocking and conduction performances of super-junction structure with different designs, structures with different N/P stripe widths (2W) and lengths (L) are simulated. Three values of W (0.5 μm, 1 μm and 2 μm) and four values of L (5 μm, 10 μm, 20 μm and 50 μm) are studied. In order to find out the full potential of this device, their MOS channel resistances have been minimized by using high gate bias and short channel lengths.

Device breakdown voltages and specific on-resistances with these different designs are plotted in Fig.2.2 and Fig.2.3. It can be seen that, for each L and W combination, device breakdown voltage remains virtually constant if N/P doping is low. This is because the electric field distribution along the drift region is close to uniform when the N/P doping is low. With a critical electric field of roughly 2.5 MV/cm or 250 V/μm, the device can hence block an average electric field of approximately 200 V/μm. Therefore, a 5 μm-thick drift region can give a blocking voltage of ~1100 V and a 20 μm-thick drift region results in a blocking voltage of ~3800V. On the other hand, with a conventional one-dimensional structure, the electric field has a triangular distribution along the drift region. The average electric field in the drift region is therefore limited to ~$E_C/2$ (or ~120 V/μm) before the device breaks down.

Fig.2.3 shows that, as expected, the device specific on-resistance decreases with increasing base doping. On the other hand, as the base doping increases above a certain level, device breakdown voltage drops quickly as the lateral electric field between the N/P stripes starts to contribute significantly to the total field in the drift region. Therefore,

for each set of L and W combinations, there exists a doping concentration, at which the FOM reaches maximum. Such a design is considered to be optimum for that specific L and W combination.

FOMs of the investigated devices are depicted in Fig.2.4 together with the theoretical limit of 4H-SiC conventional unipolar devices. Clearly, thicker super-junction drift region (L = 50 μm) and narrower column (W = 0.5 μm) result in a higher FOM. The optimum design for such a combination can give a FOM as high as 50 GW/cm^2, almost 10 times higher than the 4H-SiC theoretical limit. Similar observations can be made in Fig.2.5 where the specific on-resistances are plotted versus breakdown voltage. Performance exceeds the theoretical unipolar limit is clearly possible. It is worth mentioning that practical fabrication of such a 4H-SiC structure with N/P columns having aspect ratio of 20:1 is exceedingly challenging at the current stage. However, from Fig.2.5(a), a structure with L = 5 μm and 2W = 1 μm, which is capable of giving 4 times lower R_{SP_ON} than the theoretical limit at the same V_{BR}, is practical even with current technology.

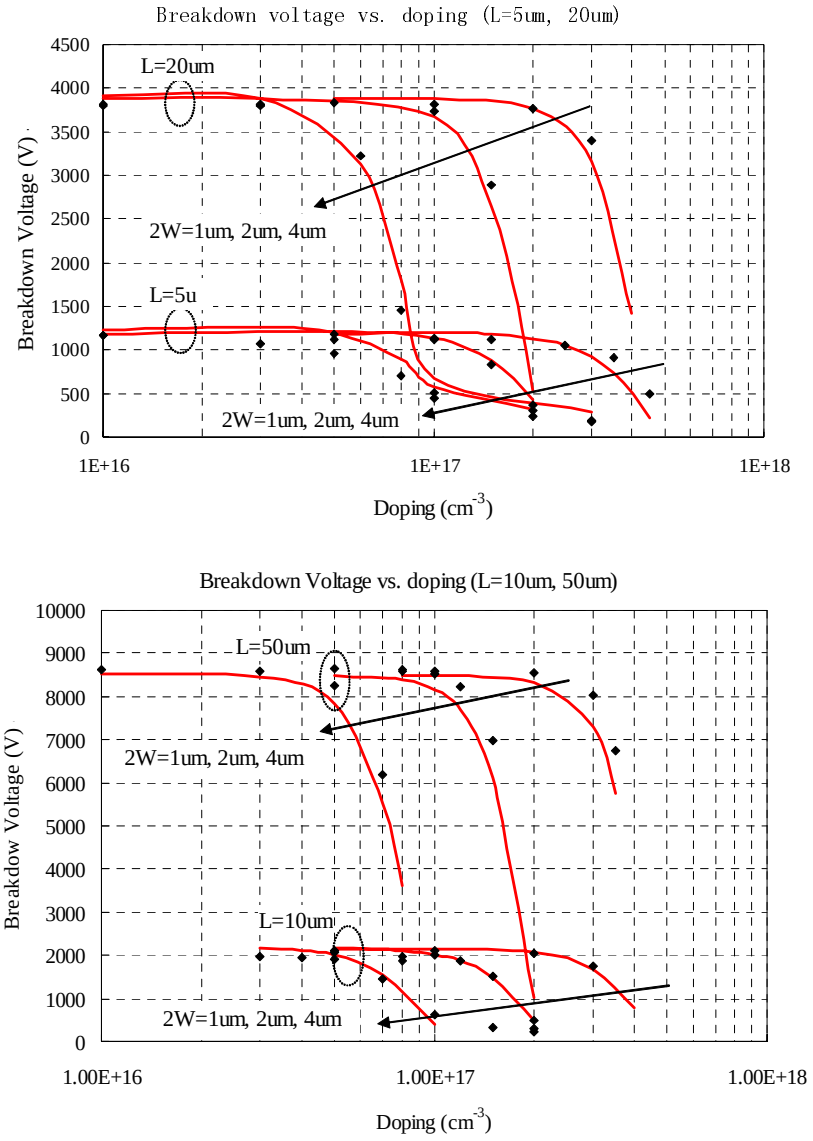
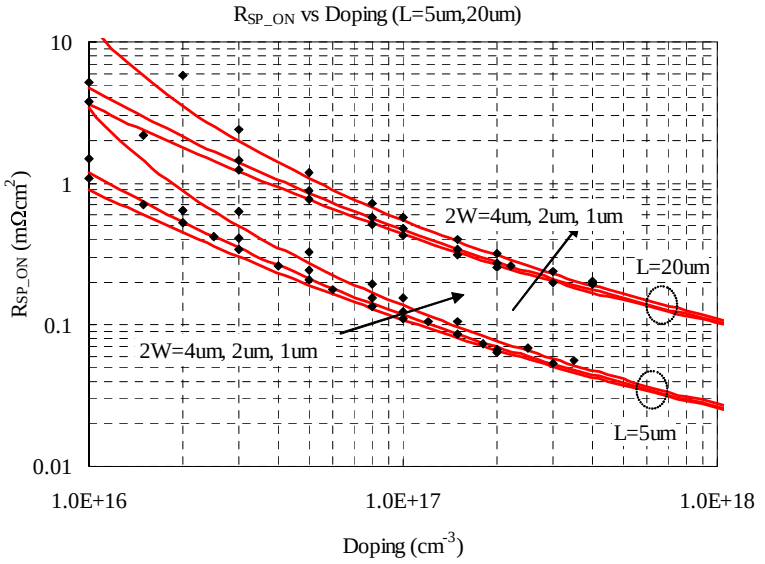
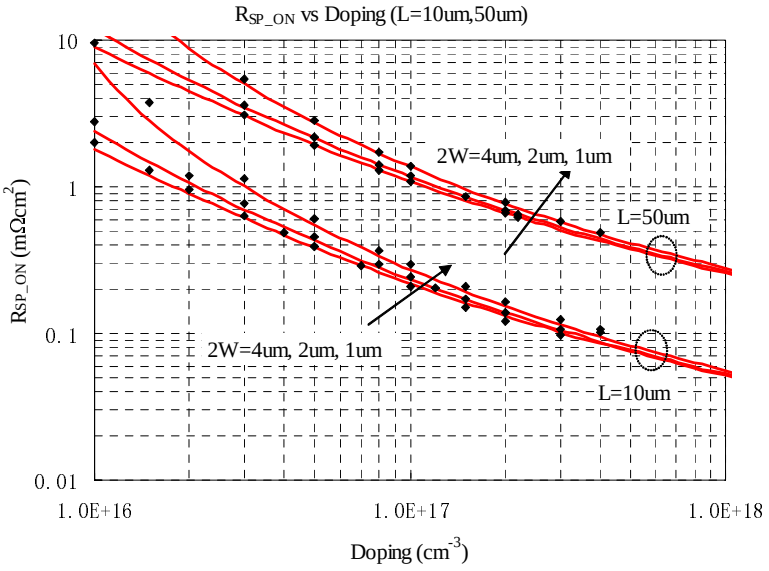


Fig.2.2 Breakdown voltage versus base doping for 4H-SiC super-junction devices with different L/W combinations. (a) L=5 μm, and L=20 μm (b) L=10 μm and L=50 μm. Line: analytical model, symbol: numerical simulation.

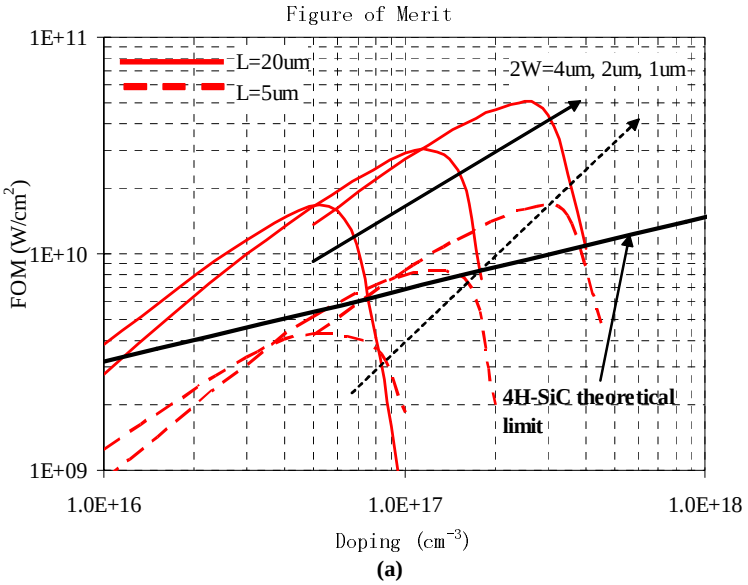


(a)

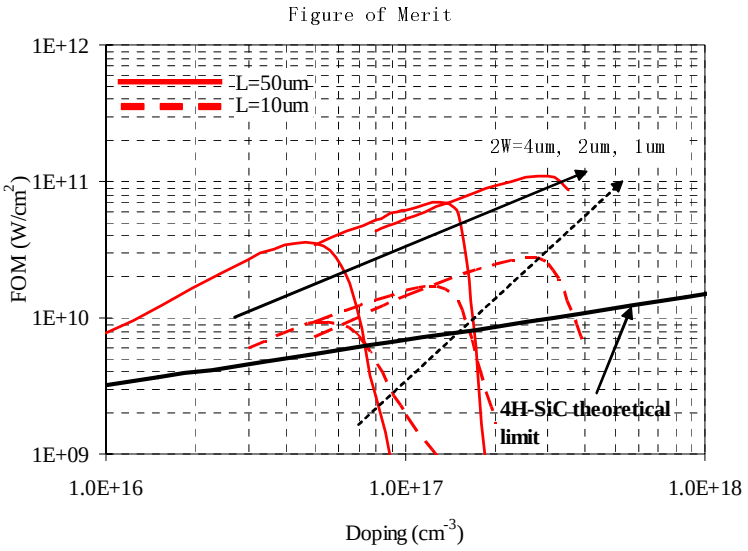


(b)

Fig.2.3 R_{SP_ON} versus base doping for 4H-SiC super-junction devices with different L/W combinations. (a) L=5 μm, and L=20 μm (b) L=10 μm and L=50 μm. Line: analytical model, symbol: numerical simulation.



(a)



(b)

Fig.2.4 Figure of Merit (FOM) of 4H-SiC super-junction structures with different L and W (0.5 μm, 1 μm and 2 μm) (a) L (solid lines: 20 μm, dashed lines: 5 μm) (b) L (solid lines: 50 μm, dashed lines: 10 μm).

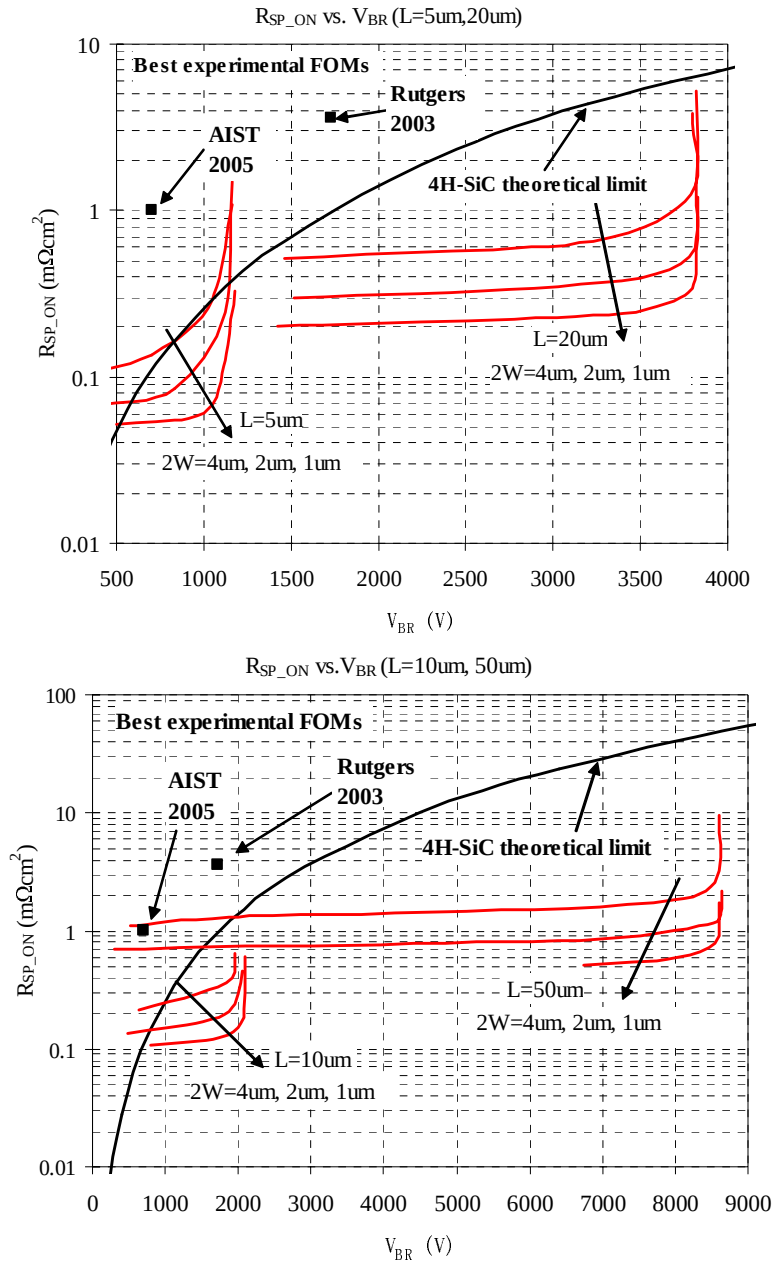


Fig.2.5 R_{SP_ON} versus breakdown voltage for 4H-SiC super-junction structures. Best experimental FOMs in the region are also shown. (a) L=5 μm, and L=20 μm (b) L=10 μm and L=50 μm

2.3 Modeling

With simulation results showing that the 4H-SiC theoretical limit can be broken by employing super-junction structure, device design and optimization become of interest. However, simulating a large number of structures with different combinations of parameters (for example device dimensions, doping, charge imbalances etc.) is very time-consuming. Therefore, a good and compact model for this 4H-SiC super-junction structure is desired to quickly and easily predict R_{SP_ON} and V_{BR} as well as to give the optimal device parameters according to certain design constraints.

2.3.1 Structure

In this work, the super-junction diode structure is the focus of analysis, because it is the most basic one among all the structures that use super-junction concept. With the understanding of the super-junction diode structure, other devices, e.g. MOSFET, JFET etc, could be easily analyzed by considering several secondary effects.

The cross-sectional view of a super-junction diode structure is shown in Fig.2.6(a). Compared with conventional structures, the homogeneous drift region is replaced by alternating N and P doped stripes. The unit cell of this structure is depicted in Fig.2.6(b). When the structure is in the reverse voltage-blocking mode, a lateral depletion region is formed across the N and P stripes, and two abrupt vertical junctions are formed across the P+/N and N+/P interfaces. As the reverse bias increases, the N and P stripes are further depleted by both the lateral and vertical junctions. For structures with narrow stripes, i.e. L>>W, the drift region can be fully depleted by the lateral junction at a relatively low

voltage bias, while the two vertical junctions have not yet grown too far into the bulk of the drift region. The two dimensional Poisson equation can be written as

$$\frac{\partial E_x(x,y)}{\partial x} + \frac{\partial E_y(x,y)}{\partial y} = \frac{\rho(x,y)}{\varepsilon} \qquad \text{Eq.2.3}$$

Where $\rho(x,y)$ is the charge density and $E_x(x,y)$ and $E_y(x,y)$ are the x and y components of the electric field, respectively. Once the P-N stripes are fully depleted by lateral junctions, further increase in the reverse bias will not change the charge distribution ($\rho(x,y)$ in Eq.2.3) within the super-junction stripes. As a result, $E_x(x,y)$ remains unchanged, and $E_y(x,y)$ grows almost uniformly across the drift region due to further depletion into the N+ and P+ regions at both ends of the super-junction region. The evolutions of E_x and E_y as reverse bias voltage increases are plotted in Fig.2.7 and Fig.2.8 respectively. Given that the charges are balanced, the electric field distribution in the N stripe is symmetric to that in the P stripe with respect to the center of the unit cell. Fig.2.9 shows the symmetry by plotting the 3-D electric field distribution of a super-junction diode structure at breakdown. With a more uniform electric field distribution than that in a conventional structure, this super-junction structure can sustain a significantly higher voltage. In addition to the higher breakdown voltage, this structure can also provide lower specific-on resistance as the doping of N and P stripes can be raised to a level orders-of-magnitude higher than possible in the conventional structure. In other words, the theoretical limit of unipolar devices, $R_{SP\_ON} \propto V_{BR}^{2.4\text{-}2.6}$, can be broken by using the charge-compensation principle.

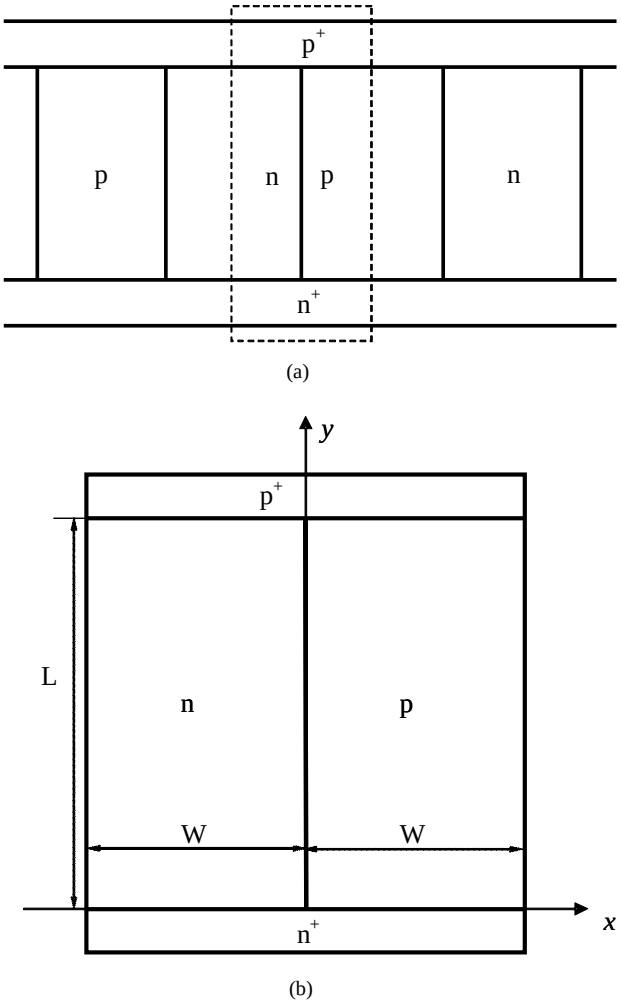


Fig.2.6 Cross-sectional view of (a) A super-junction diode with alternating P and N drift regions; (b) One unit cell of the super-junction structure (the part within the dashed box in (a))

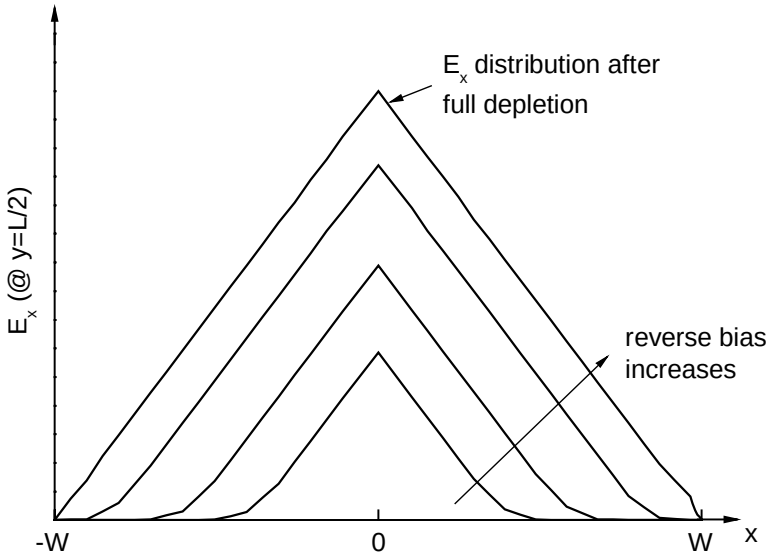


Fig.2.7 Evolution of the lateral electric field distribution (E_x) along the center of the drift region (y = L/2) as reverse bias increases.

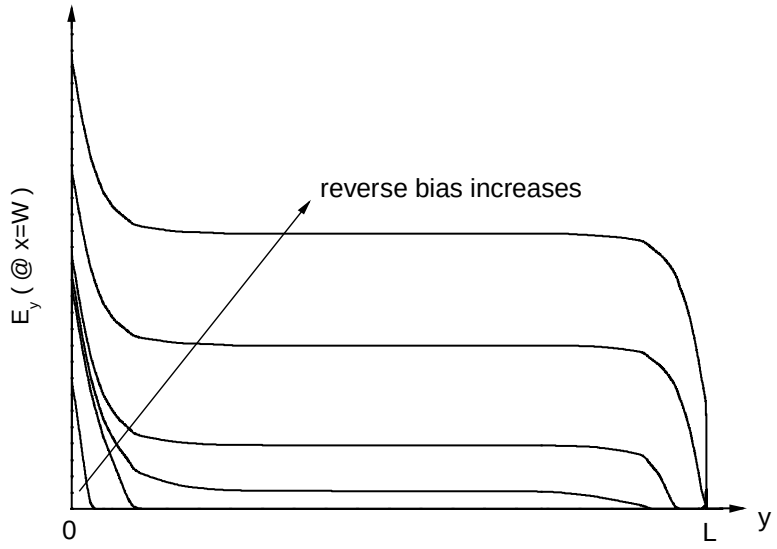


Fig.2.8 Evolution of the vertical electric field distribution (E_y) along the middle of the P stripe (x = W) as reverse bias increases.

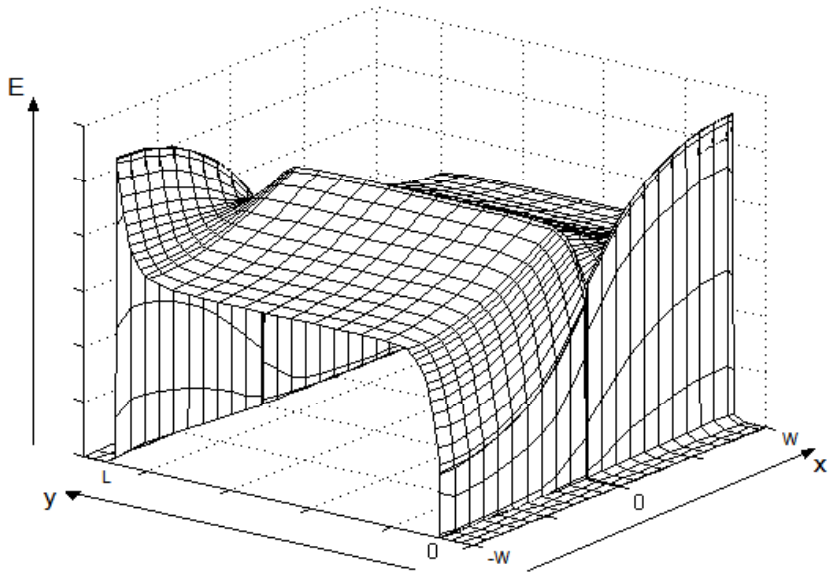


Fig.2.9 3-D electric field distribution for a super-junction diode structure at breakdown.

2.3.2 Model for Reverse Voltage Blocking

A. Impact Ionization Coefficients

In the voltage-blocking mode, the avalanche breakdown occurs when [59]

$$\int_0^w \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p) dx'\right] dx = 1 \qquad \text{Eq.2.4}$$

where w is the length of the breakdown path, α_n and α_p are the ionization coefficients of electrons and holes respectively. A common effective value for both electrons and holes is often used to simplify the avalanche breakdown condition. Substitution of $\alpha_n = \alpha_p = \alpha_{eff}$ into Eq.2.4 gives

$$\int_0^w \alpha_{eff}\, dx = 1 \qquad \text{Eq.2.5}$$

In this model, $\alpha_{eff} = CE^g$ in Fulop's form [60] is employed for its simplicity. In order to build a good model for the voltage blocking capability of the 4H-SiC super-junction devices, it is important that the impact ionization coefficients are modeled precisely. In the literature, two teams has systematically measured and reported the impact ionization coefficients for 4H-SiC [55, 61]. Significant differences exist between these two sets of data. The data and expressions given in [55] are found to provide more accurate predictions to experimental results [62]. The constants C and g in Fulop's form are determined by fitting α_{eff} into the impact ionization coefficient expressions provided in [55]. $C = 4 \times 10^{-48}$ cm^7V^{-8} and g = 8 are the values that are used in this work as they give the best results. Fig.2.10 shows α_n, α_p and the fitted α_{eff} versus the electric field ranging between 1.5×10^6 and 3.5×10^6 V/cm. The avalanche breakdown condition, i.e. Eq.2.5, for 4H-SiC devices becomes

$$\int_0^w 4\times10^{-48} \cdot E^8 dx = 1 \qquad \text{Eq.2.6}$$

where E is in the unit of V/cm, and w is the length of the critical path, along which avalanche breakdown takes place.

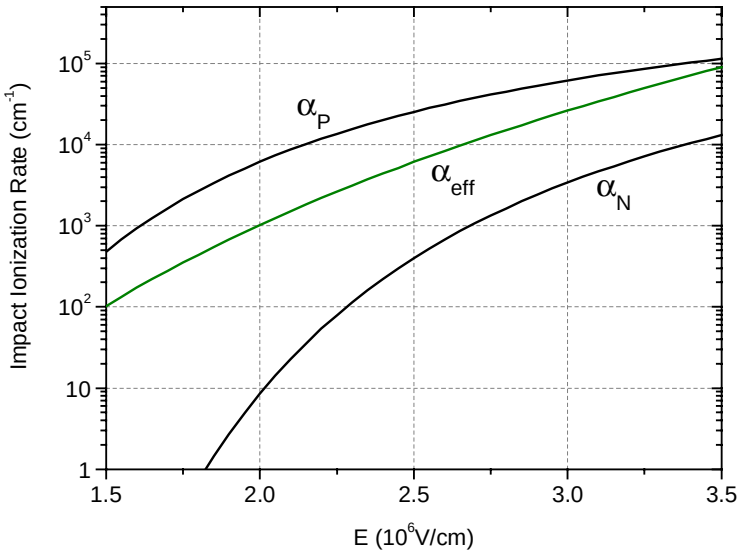


Fig.2.10 Impact ionization coefficients for holes and electrons [55] and the fitted effective impact ionization coefficient in the interested electric field range.

B. Electric Field Distribution modeling along the Critical Path

For the super-junction diode structure shown in Fig.2.6(b), due to the electric field peaks at corners (x = -W, y = L) and (x = W, y = 0), breakdown usually occurs along the middle of the N or P stripes (x = ±W). This has been confirmed in numerous numeric simulations. Therefore, x = ±W are the two critical paths, where the lateral component of electric field E_x is zero. At those locations, the total electric field equals to its vertical component, i.e. $E(\pm W,y) = E_y(\pm W,y)$, which further simplifies the calculation of breakdown voltage. For charge-balanced structures, since the electric field distributions along the two critical paths are symmetrical to each other with respect to the center of the unit cell (x = 0, y = L/2), the ionization integration in Eq.2.6 can be taken along either of these two critical paths. The length of the critical path is the same as the drift region length L.

Modeling of the electric field along the critical path is the most crucial part in the calculation of breakdown voltage. The electric field distribution is governed by the two-dimensional Poisson Equation (Eq.2.3).

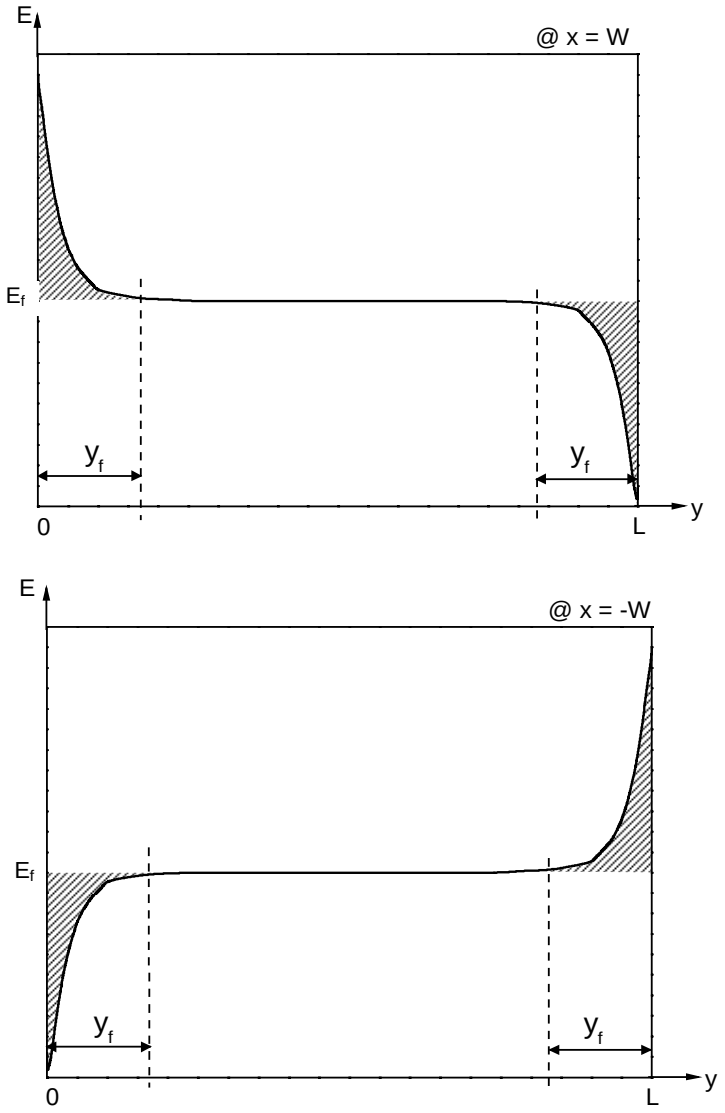


Fig.2.11 Electric field distributions along the critical paths (x = ±W) of a charge-balanced super-junction structure.

Plotted in Fig.2.11 are the electric field distributions along the critical paths (x = ±W) of a fully depleted charge-balanced super-junction structure, which are symmetrical to each other with respect to the center of the unit cell. After full depletion, due to charge

balance, the two distribution curves at x = W and x = -W have the same slope with opposite polarity at any y location. Therefore, the regions of peak and tail (shaded areas) are identical ("peak-and-tail symmetry"). The applied voltage at this moment is $E_f \times L$, where E_f is the electric field of the flat region. Along one critical path (say, x = W), as y increases from 0 to L, the slope of the electric field ($\partial E_y/\partial y$) decreases because of the increasing lateral depletion effect that gives rise to an increasing $\partial E_x/\partial x$ term in the Poisson Equation. In other words, the two-dimensional charge compensation effect helps decreasing the slope of E_y and makes it more uniform along the critical path. Beyond certain location, defined as $y \equiv y_f$, the E_y distribution becomes flat, i.e. $\partial E_y/\partial y = 0$. As y increases further to $y \geq L\text{-}y_f$, the slope of E_y increases because of the "peak-and-tail symmetry". Due to the nature of the lateral depletion effect on the electric field distribution along the critical path, the distance at which E_y becomes virtually flat (y_f) is mainly determined by the half-pillar width (W) for structures with reasonably long drift region (longer than $2y_f$). By observing numerous simulation results, the value of y_f can be well approximated by

$$y_f = 2.4W \qquad \text{Eq.2.7}$$

In this model, the electric field distribution in the region $[0, y_f]$ is modeled in the form of polynomial equation with the following boundary conditions.

$$E\big|_{y=y_f} = E_f \qquad \text{Eq.2.8}$$

$$\left.\frac{\partial E}{\partial y}\right|_{y=y_f} = 0 \qquad \text{Eq.2.9}$$

$$\left.\frac{\partial E}{\partial y}\right|_{y=0} = -\frac{qN}{\varepsilon} \qquad \text{Eq.2.10}$$

Eq.2.10 sets a constraint on the slope of E at y = 0 because right at the moment when depletion starts, $\left.\frac{\partial E}{\partial y}\right|_{y=0}$ is not influenced by the lateral depletion at all, and should be the same as that in a one-dimensional PN junction, i.e. $-\frac{qN}{\varepsilon}$.

Consider all the above, the electric field distribution can be derived as

$$E = E_f + \frac{qN}{\varepsilon} \cdot \frac{(y_f - y)^m}{m \cdot y_f^{m-1}}, \qquad y \in [0, y_f] \qquad \text{Eq.2.11}$$

where m is the order of the polynomial equation that will be fitted later.

Within the region $y \in [y_f, L-y_f]$, the E distribution is as simple as

$$E = E_f, \qquad y \in [y_f, L-y_f] \qquad \text{Eq.2.12}$$

Because of the “peak-and-tail symmetry”, derivation of the electric field distribution in the region $[L-y_f, L]$ is similar to those above. We can get

$$E = E_f - \frac{qN}{\varepsilon} \cdot \frac{[y - (L - y_f)]^m}{m \cdot y_f^{m-1}}, \qquad y \in [L-y_f, L] \qquad \text{Eq.2.13}$$

In the derivation of Eq.2.11 to Eq.2.13, it is assumed that the super-junction structure is fully depleted. When this assumption is not valid, for example the applied voltage is not high enough to deplete the N/P stripes, the electric field distributions would look like the lower four curves in Fig.2.8. Since the analyses of y_f and the “peak-and-tail symmetry” in the depleted region are still applicable, the E field distribution above could be modified by eliminating the negative portion. Therefore, the E field distribution can be rewritten as

$$E_1 = \begin{cases} E_f + \dfrac{qN}{\varepsilon} \cdot \dfrac{(y_f - y)^m}{m \cdot y_f^{m-1}}, & y \in [0, y_f] \\ E_f, & y \in (y_f, L - y_f) \\ E_f - \dfrac{qN}{\varepsilon} \cdot \dfrac{[y - (L - y_f)]^m}{m \cdot y_f^{m-1}}, & y \in [L - y_f, L] \end{cases} \qquad \text{Eq.2.14}$$

$$E = \frac{1}{2}[E_1 + ABS(E_1)]$$

This modification made the model capable of dealing with structures that break down before full depletion takes place.

Finally, for a given E_f, which is related to the applied voltage, the E distribution can be obtained by Eq.2.14.

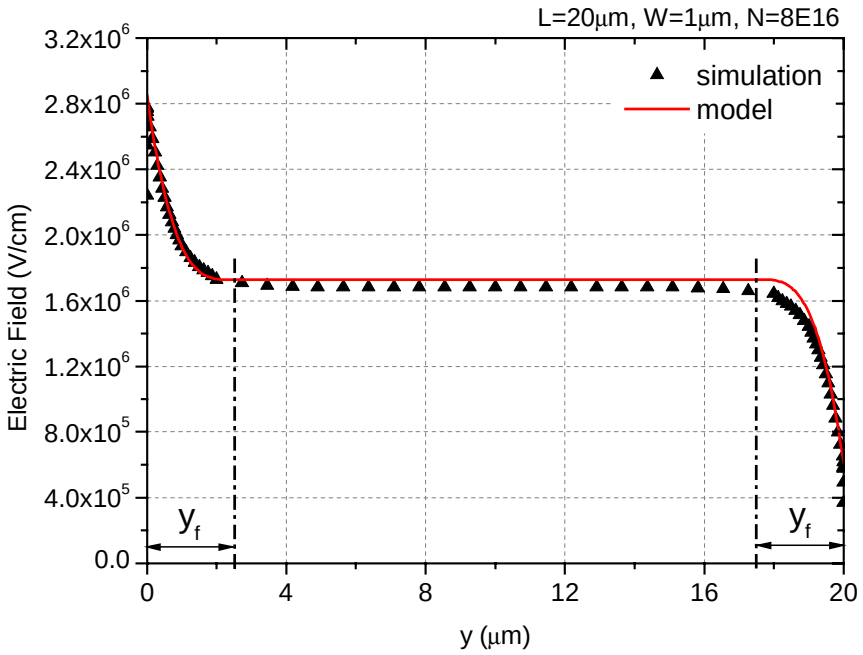


Fig.2.12 Electric field distribution model compared with simulation data: E field distribution along one critical path in a 4H-SiC super-junction diode with L=20 μm, W=1 μm and $N = 8 \times 10^{16}\ cm^{-3}$.

By fitting with numerous electric field distributions in various super-junction structures, m=3.2 is found to give the best approximation. Fig.2.12 shows the comparison between the modeled and simulated electric field distribution along the critical path (x =

W) at breakdown in the super-junction diode structure with L = 20 μm, W = 1 μm and doping $N_n = N_P = 8 \times 10^{16}\,cm^{-3}$. It can be seen that the model fits well with the simulation data, especially in the peak region which contributes the most to the avalanche breakdown process due to the high sensitivity of the impact generation rate to the electric field as evident from the "E^8" term in Eq.2.6.

C. Breakdown Voltage Calculation

Once the electric field distribution has been modeled, the breakdown voltage can be calculated by substituting the E distribution (Eq.2.14) into the avalanche breakdown condition (Eq.2.6). For a given E_f which is related to the applied voltage, there is one corresponding E distribution and hence a resulted value of the impact ionization integration. The breakdown voltage can be found when the ionization integral reaches unity.

Two-dimensional numerical simulations with Silvaco software have been carried out to verify the results obtained with this model. The physical parameters used in the simulation including impact ionization coefficients are based on experimental data. The following parameters are used for impact ionization coefficients.

$$\alpha_n = a_n \exp\left[-\frac{b_n}{E}\right], \qquad \alpha_p = a_p \exp\left[-\frac{b_p}{E}\right] \qquad \text{Eq.2.15}$$

where $a_n = 1.14 \times 10^9\,cm^{-1}$, $b_n = 3.8 \times 10^7 cm^{-1}$, $a_p = 6.85 \times 10^6\,cm^{-1}$ and $b_p = 1.41 \times 10^7$ cm^{-1} are selected by fitting experimental data presented by Konstantinov et al. [55]. It should also be noted that Schottky barrier diodes with the super-junction structure, instead of the P-N diode plotted in Fig.2.6, were simulated in the numerical simulation for their breakdown voltage and forward on-resistance. This is to avoid the effect of

conductivity modulation resulted from bipolar injection of a P-N structure. Device on-resistance reduction due to bipolar injection is extrinsic to a super-junction structure and is beyond the scope of this work.

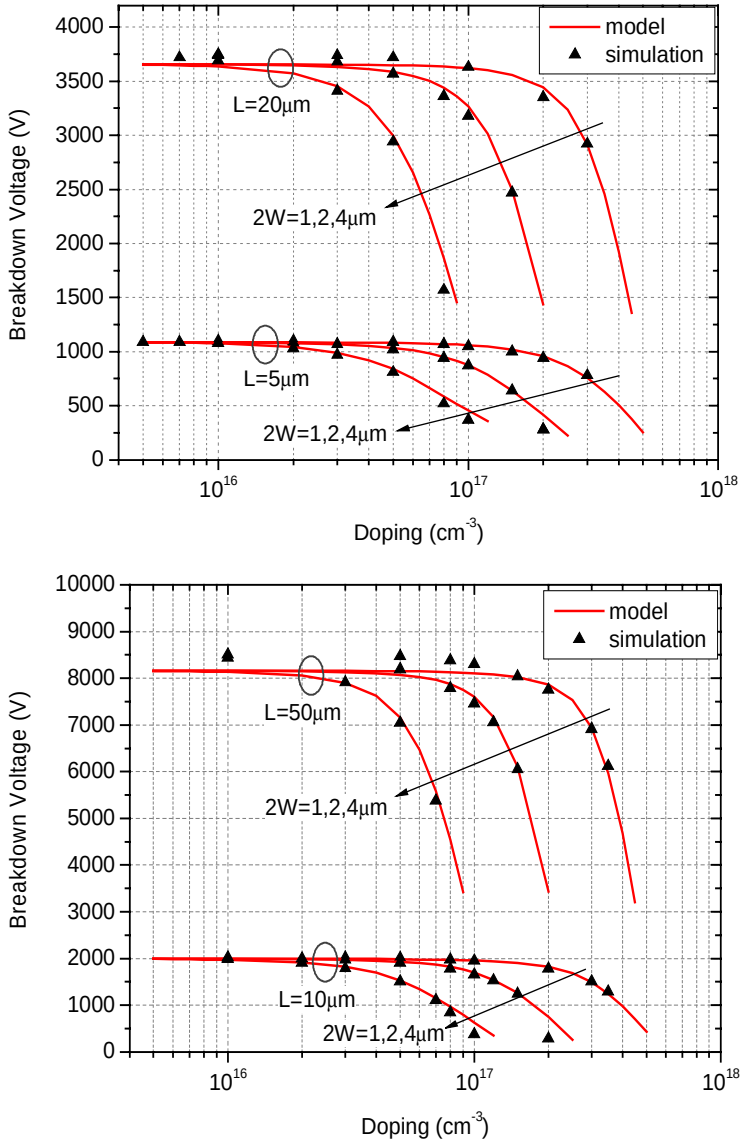


Fig.2.13 Reverse voltage blocking model compared with numerical simulation results: Breakdown voltage at various L, W and doping conditions for 4H-SiC super-junction devices.

A comparison of breakdown voltages obtained in numerical simulations and using the above model can be found in Fig.2.13. They agree very well through devices with

various structural parameters (L = 5 μm, 10 μm, 20 μm and 50 μm; W = 0.5 μm, 1 μm and 2 μm; N ranging from 5×10^{15} to 5×10^{17} cm^{-3}).

2.3.3 Model for Forward Current Conduction

As the super-junction structure is mostly used in unipolar devices, only the forward conduction in unipolar mode is modeled in this paper. The intrinsic specific resistances of the super-junction structures are obtained based on the unit-cell structure shown in Fig.2.6 with the p^+ region replaced by an Ohmic contact electrode, in order to avoid bipolar injection. In the unipolar mode, the current flows only in the un-depleted part of N stripe. The specific-on resistance can be calculated as following

$$R_{SP\_ON} = \frac{1}{q \cdot \mu_n(N) \cdot N} \cdot \frac{L}{W_{n\_undep} \cdot z} \cdot 2W \cdot z = \frac{2L}{q \cdot \mu_n(N) \cdot N} \cdot \frac{1}{1 - \frac{W_{n\_dep}}{W}} \qquad \text{Eq.2.16}$$

where q is the electron charge, N is the doping concentration of N stripe, W_{n_undep} is the undepleted N stripe width, z is depth of the device in the third dimension, and $\mu_n(N)$ is the electron mobility in 4H-SiC that can be modeled as [58]

$$\mu_n(N) = 40 + \frac{950 - 40}{1 + \left(\frac{N}{2e17}\right)^{0.76}} \qquad (cm^2V^{-1}s^{-1}) \qquad \text{Eq.2.17}$$

With perfectly matched N and P stripe doping concentrations, the depleted width of N stripe is

$$W_{n\_dep} = \frac{1}{2}\sqrt{\frac{2\varepsilon_r\varepsilon_0(V_{bi} + V_F)}{q \cdot \frac{N \cdot P}{N + P}}} \approx \sqrt{\frac{\varepsilon_r\varepsilon_0 V_{bi}}{q \cdot N}} \qquad \text{Eq.2.18}$$

where $\varepsilon_r\varepsilon_0$ is the permittivity of 4H-SiC, V_{bi} is the P/N junction built-in voltage, V_F is the forward biasing voltage. V_F is neglected in the equation above since $V_F << V_{bi}$ with reasonable forward current densities.

According to this model, R_{SP_ON} versus doping curves for different L/W combinations (L = 5 μm and 20 μm, 2W = 1 μm, 2 μm and 4 μm) are plotted in Fig.2.14, where they are compared with the 2-D numerical simulation results. A good agreement can be seen between the modeled curves and the simulation data points.

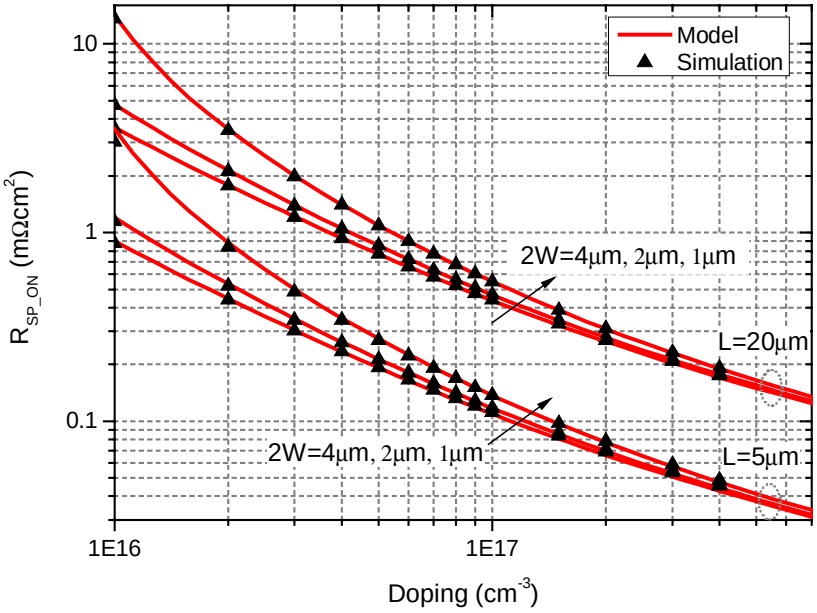


Fig.2.14 Forward conduction model compared with simulation results: R_{SP_ON} versus doping for 4H-SiC super-junction devices with different L/W combinations.

2.3.4 Modeling of Charge Imbalance Effects

As described previously, the super-junction concept relies on the charge-compensation principle. In order to completely utilize the benefits of this structure, the opposite charges in the N and P stripes should be balanced perfectly, which is very

difficult in reality. Charge imbalance would degrade the voltage blocking capability of super-junction devices. This issue is of particular importance for SiC super-junction devices as the doping techniques (implantation, epi grow and p dopant activation etc.) are not as well controllable as in Si devices. Therefore, a super-junction model is not complete without modeling the charge imbalance effects.

The method used to model the degradation of V_{BR} due to charge imbalance is similar to that in the voltage blocking model. The avalanche breakdown condition, i.e. Eq.2.6, is still valid. The only thing that needs remodeling is the electric field distribution along critical path. Fig.2.15 shows the E_y distribution in a charge imbalanced super-junction structure, which is similar to that in a charge-balanced structure except that the E_y distribution in the middle of the drift region has a significant slope. This slanting distribution is caused by the net charge in the drift region; hence the slope is given by $\frac{q|P-N|}{2\varepsilon}$. The E field distributions along x = ±W still have the peak and tail on top of the slanting line. It should be noted that the two distributions are not symmetrical any more in this case. The one in the higher doped side has a more non-uniform shape, as can be see in Fig.2.15, which results in an earlier breakdown. The E field distribution in a charge-imbalanced super-junction structure can be modeled as

$$\mathrm{E}_1 = \begin{cases} \mathrm{E}_{\mathrm{slope}} + \dfrac{q\cdot\max(P,N)}{\varepsilon}\cdot\dfrac{(y_f - y)^m}{m\cdot y_f^{m-1}}, & y\in[0,y_f] \\ \mathrm{E}_{\mathrm{slope}}, & y\in(y_f, L-y_f) \\ \mathrm{E}_{\mathrm{slope}} - \dfrac{q\cdot\max(P,N)}{\varepsilon}\cdot\dfrac{[y-(L-y_f)]^m}{m\cdot y_f^{m-1}}, & y\in[L-y_f, L] \end{cases} \qquad \text{Eq.2.19}$$

$$\mathrm{E} = \frac{1}{2}[\mathrm{E}_1 + ABS(\mathrm{E}_1)]$$

where

$$E_{slope} = \frac{V_a}{L} - \frac{q \cdot |P - N|}{2\varepsilon} \cdot \left(y - \frac{L}{2} \right) \qquad \text{Eq.2.20}$$

When the device is fully depleted, V_a is the applied voltage.

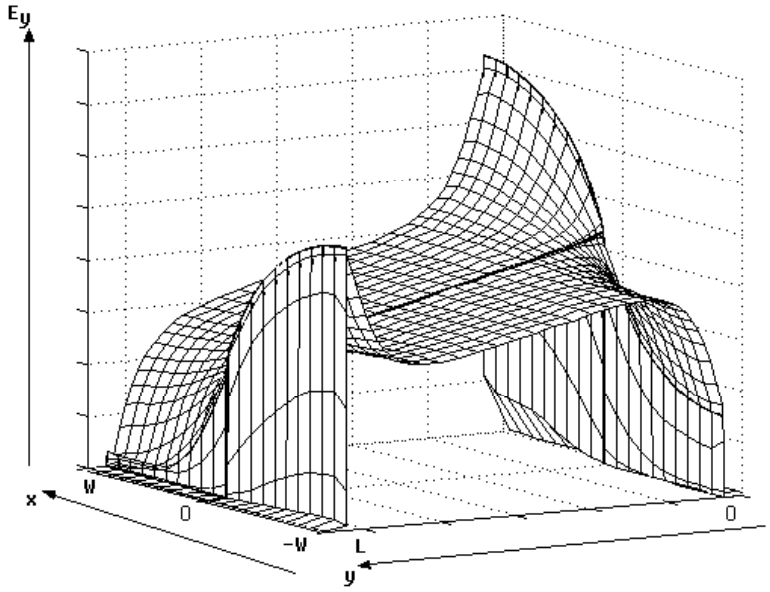


Fig.2.15 3D E_y distribution in a super-junction diode structure with charge imbalanced.

Fig.2.16 shows the comparison of the E field computed using the above model and from the numeric simulations. This model agrees well with the simulation data for various charge imbalance percentages (defined as $\frac{P-N}{N} \times 100\%$).

Once the E field model is ready, the breakdown voltage can be calculated using Eq.2.6. The breakdown voltages of such structures have been calculated and plotted against the charge imbalance percentage in Fig.2.17 for structures with L = 20 μm, W = 1 μm and a variety of N stripe doping concentrations. The results fit those obtained from numerical simulation very well. Evidently, the higher the N stripe doping, the more sensitive the breakdown voltage is to the charge imbalance percentage. To obtain a

breakdown voltage ≥ 80% of the ideal value (~ 3650 V), the allowable charge imbalance percentage are found to be 25%, 12% and 5% for N doping of 3×10^{16} cm^{-3}, 5×10^{16} cm^{-3}, and 8×10^{16} cm^{-3}, respectively. Similar results have been plotted in Fig.2.18 for L = 10 μm, W = 2 μm and in Fig.2.19 for L = 5 μm, W = 0.5 μm. The developed model is capable of predicting the breakdown voltage with good accuracy for almost all cases.

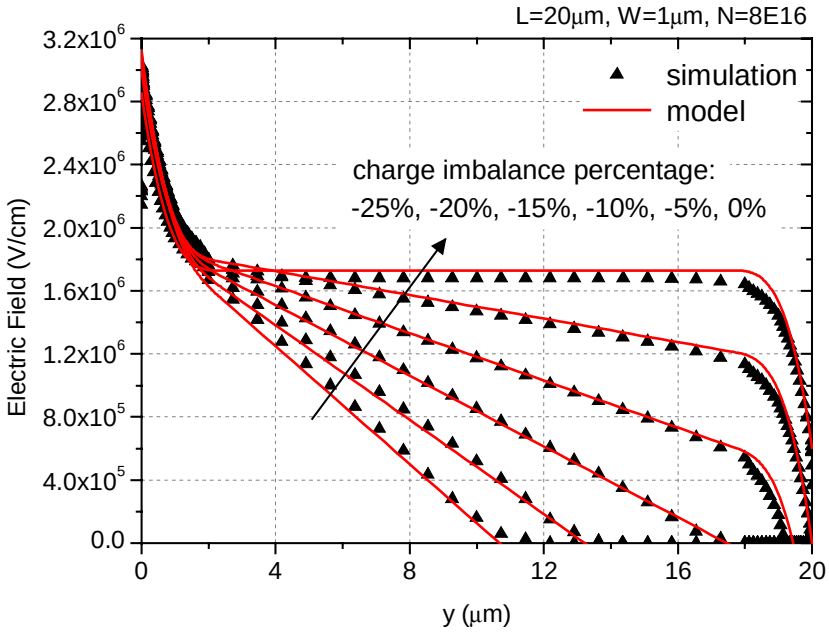


Fig.2.16 Charge imbalance model of E field distributions compared with simulations: The electric field distributions in charge imbalanced super-junction diode structures with various charge imbalance percentages.

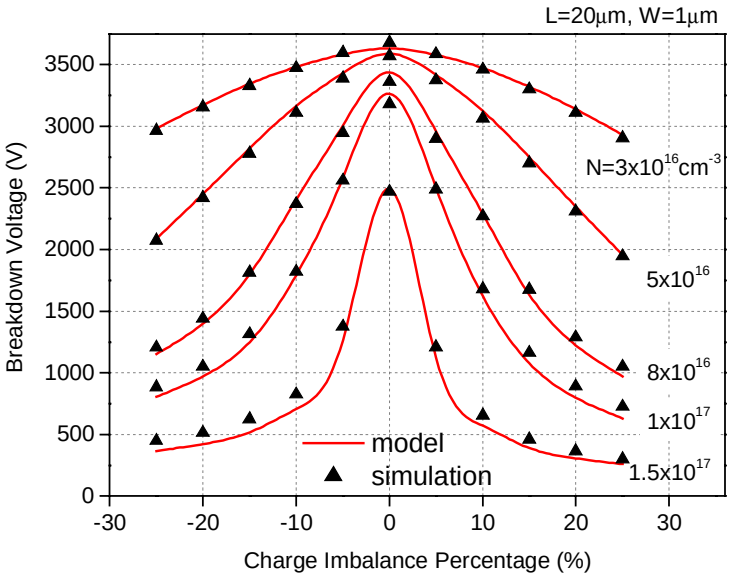


Fig.2.17 Charge imbalance model compared with simulations: The breakdown voltage versus charge imbalance percentage at various doping concentrations for a 4H-SiC super-junction structure with L = 20 μm and W = 1 μm.

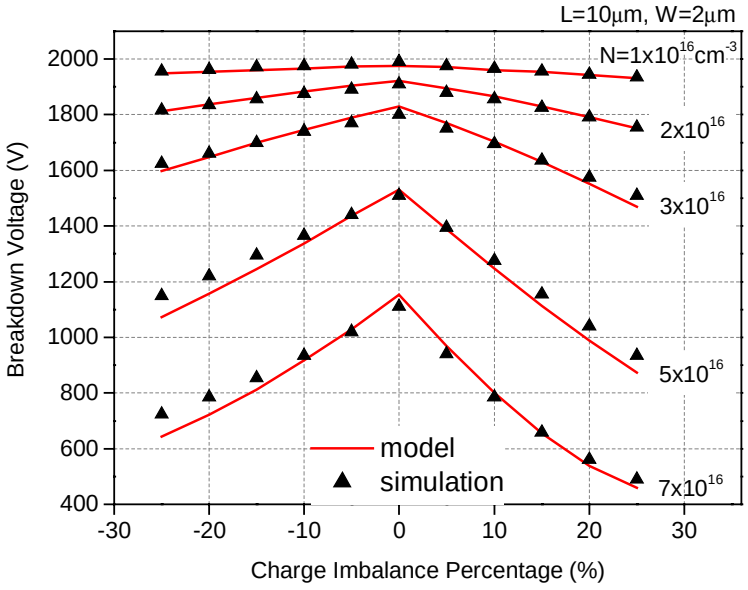


Fig.2.18 Charge imbalance model compared with simulations: The breakdown voltage versus charge imbalance percentage at various doping concentrations for a 4H-SiC super-junction structure with L = 10 μm and W = 2 μm.

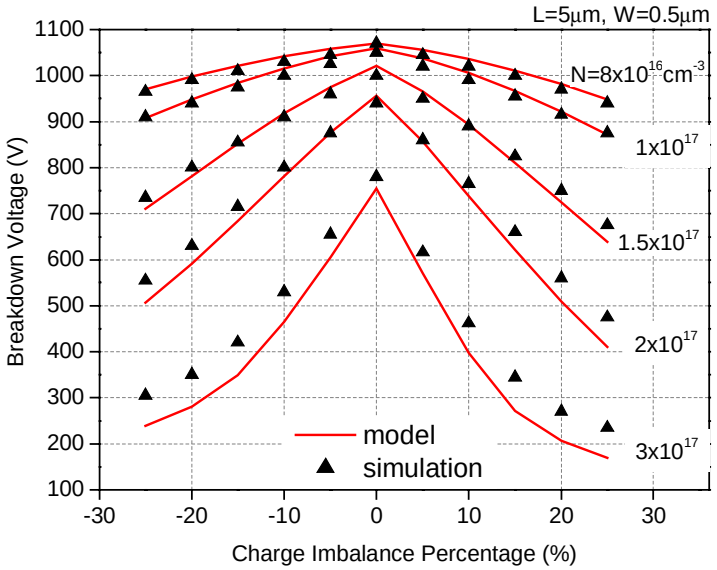


Fig.2.19 Charge imbalance model compared with simulations: The breakdown voltage versus charge imbalance percentage at various doping concentrations for a 4H-SiC super-junction structure with L = 5 μm and W = 0.5 μm.

2.4 Design Optimization

The usefulness of the model developed in this work is in its capability of quickly providing an optimum SiC super-junction design under a given set of constraints, a process that can easily take weeks through numerous 2D numerical simulation runs. As an example, a specific design case is described below.

Assume that one needs to design a super-junction device to block 1000 V. Based on the model developed, the highest P and N doping concentration and the corresponding lowest R_{SP_ON} obtainable for a 1000 V device can be calculated for any given pair of stripe width (2W) and stripe length (L). The results are plotted in Fig.2.20 for L = 5 μm, 6 μm, 7 μm, 8 μm, 10 μm and 15 μm and 2W = 1 μm, 2 μm, 3 μm and 4 μm. It can be seen that, depending on the processing capability of obtaining narrow N/P stripes, one

can achieve different levels of optimal R_{SP_ON}. For instance, if the fabrication process is capable of creating stripe width of 1 μm (regardless of the stripe length), Fig.2.20 shows that the best super-junction design should have L = 6 μm, N = P = 2.65×10^{17} cm^{-3} and the lowest R_{SP_ON} achievable should be 0.075 $m\Omega cm^2$. If the fabrication process only allows N/P stripe width of 3 μm, then the optimum design should be L = 7 μm, N = P = 8.08×10^{16} cm^{-3} and the best R_{SP_ON} achievable becomes 0.185 $m\Omega cm^2$. This still compares favorably to the best obtainable R_{SP_ON} of 0.26 $m\Omega cm^2$ with a conventional parallel-plane P-N junction design.

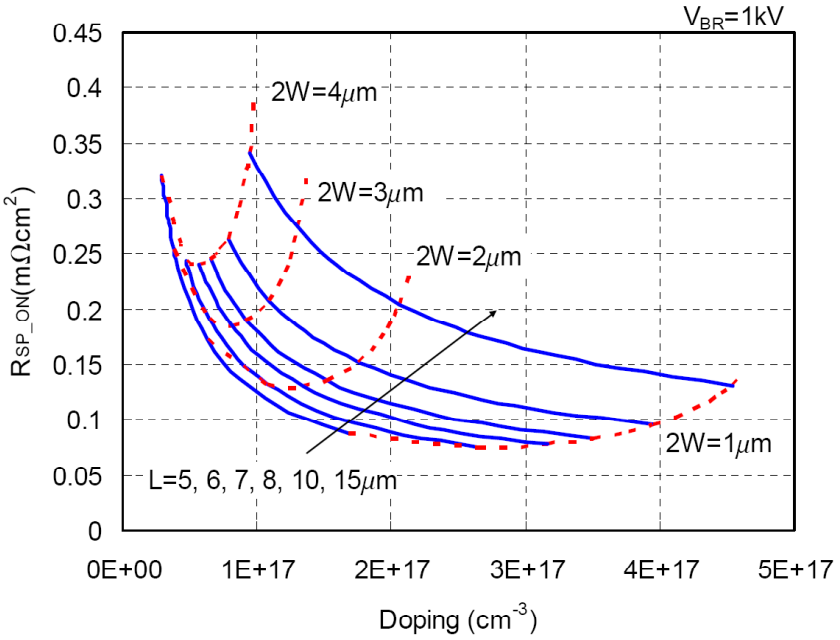
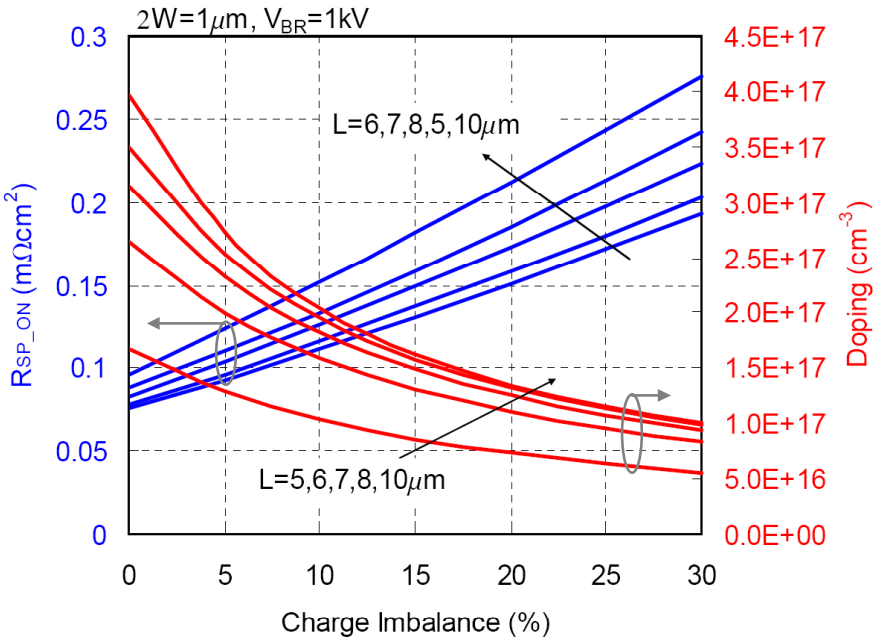


Fig.2.20 Optimization case study: for a given design target V_{BR} = 1 kV, R_{SP_ON} versus doping concentration for various L and W combinations.

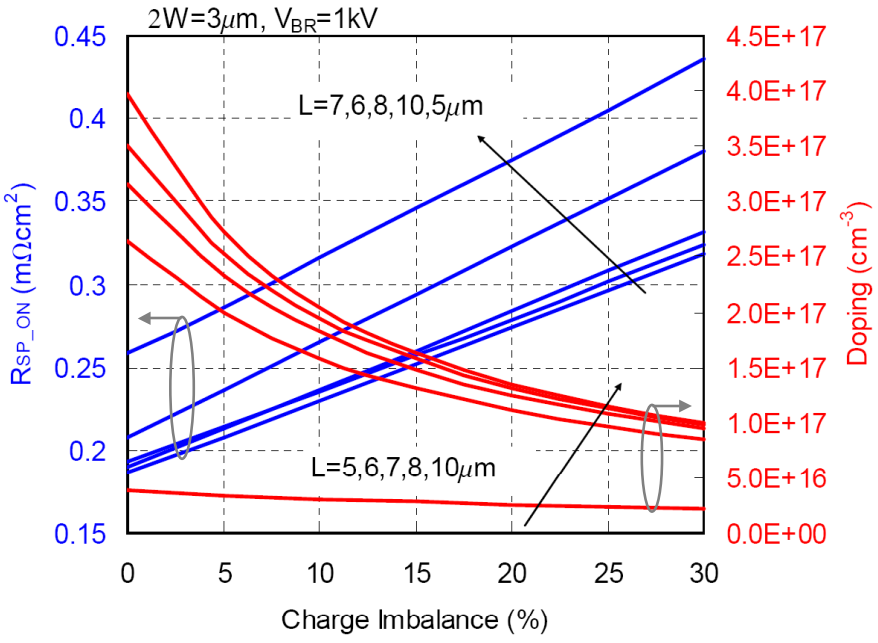
Certainly, in the above calculation, charge imbalance is not considered. In practice, charge imbalance is unavoidable and has to be accounted for. Fig.2.21(a) shows the new design optimization guidelines for the design of the 1000 V device by considering the amount of charge imbalance. In Fig.2.21(a), variations of the highest possible N doping

and its corresponding R_{SP_ON} have been plotted against the charge imbalance percentage for various stripe lengths (L) and the fixed stripe width (2W) of 1 μm. It can be seen that as the charges become more imbalanced, the R_{SP_ON} increases because the doping concentration has to be reduced in order to keep V_{BR} = 1000 V. The figure shows that for a stripe width of 1 μm, regardless of the amount of charge imbalance, L = 6 μm still gives the lowest R_{SP_ON}. With a charge imbalance of 20%, the best structure should have an N doping of 1.11×10^{17} cm^{-3}, less than half of the 2.65×10^{17} cm^{-3} optimum N doping for a perfectly balanced case. The resultant lowest R_{SP_ON} is 0.151 $m\Omega cm^2$, doubling the R_{SP_ON} of 0.075 $m\Omega cm^2$ achievable with perfect charge balance. It is interesting to note the high sensitivity of the optimum R_{SP_ON} on the charge imbalance percentage.

Similarly, if the device designer only has access to a process that gives a stripe width of 3 μm, the design guideline for charge imbalance is plotted in Fig.2.21(b). In this case, L = 7 μm gives the best result. For a charge imbalance of 30%, the highest N doping is 4.29×10^{16} cm^{-3} and the lowest achievable R_{SP_ON} can be found to be 0.319 $m\Omega cm^2$. This is about 71% higher than that achievable on a device with a perfect charge balance (0.186 $m\Omega cm^2$). The sensitivity of the lowest R_{SP_ON} to charge imbalance percentage is significantly less than that for the narrow N/P stripe (2W = 1 μm) devices. Note that the 0.319 $m\Omega cm^2$ with a 30% charge imbalance is already higher than the conventional 1D limit of 0.26 $m\Omega cm^2$, rendering such a super-junction design unattractive.



(a)



(b)

Fig.2.21 Optimization case study: for a given design target V_{BR} = 1 kV, R_{SP_ON} (blue lines) and its corresponding doping concentration (red lines) versus charge imbalance percentage for various L and W combinations. **(a)** 2W = 1 μm **(b)** 2W = 3 μm.

2.5 Considerations for Practical Fabrication

While the simulation and model predict exciting FOMs for the analyzed super-junction structure based on 4H-SiC, it is important to examine its feasibility for realistic device processing. A quick inspection on Fig.2.6 tells that fabrication of a structure with vertical N and P strips throughout the whole device with good control is substantially more challenging than a structure with conventional uniform epitaxial base. A few methods have been proposed to achieve such vertical N and P doping pillars.

The first possible method uses repeated N epi grow-P implantation process. In this method, N epitaxial layer of 0.5 μm to 1 μm thickness is grown on substrate and half of its area is converted to P- type by implantation. After implantation annealing, this epi-implantation-annealing process is repeated many times to give a super-junction drift region with the desired thickness. While this method was successfully used in silicon, it is difficult to be realized in SiC as multiple implantation and annealing processes will greatly degrade the material quality.

The second possible process starts with growing a uniform N-type drift region with the desired thickness. A deep anisotropic etching is then followed to create narrow and deep trenches. The trenches can then be refilled with P-type 4H-SiC material by using selective epi-grow process. The key to this process is a well-controlled selective epi-grow process. At this stage, such a process has not been reported. The cost of this process step is also expected to be high even when it becomes available.

Process flow of the third possible method is shown in Fig.2.22. It is similar to the second method described above in its first two steps. After deep trench etching, instead of using selective epi re-growth, the P type doping can be introduced by tilted ion

implantation. With a well controlled implantation dose, tilt angle and reasonably controllable implantation activation efficiency (note that activation efficiency differs from ionization efficiency which will be 100% when the region is depleted), effective charges in the P-region can be introduced with good accuracy. The trenches can then be covered by a thin thermal oxide layer before being re-filled with insulators.

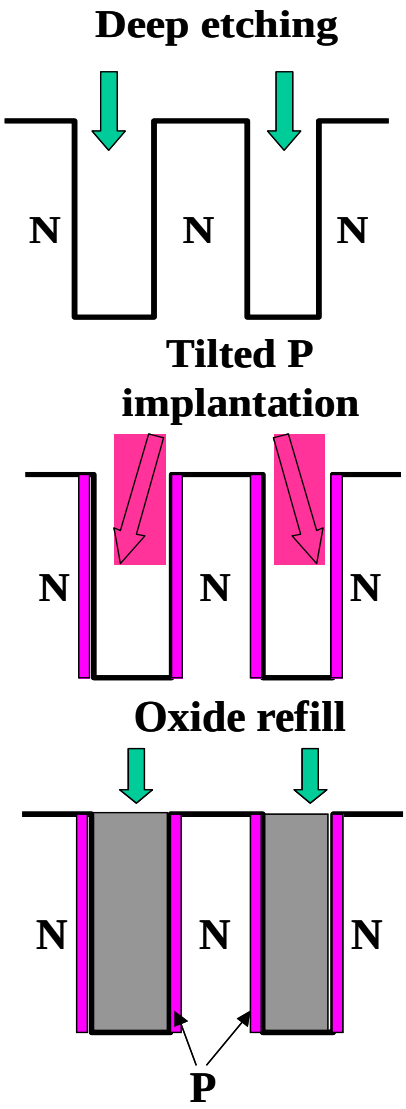


Fig.2.22 Brief flow for a possible fabrication process to realize a super-junction structure in 4H-SiC.

Among the three processes described above, the third process is comparably less challenging. Deep and high aspect ratio trench etching is a key process. A well-controlled trench and implantation process is possible [8]. High aspect ratio (4 μm high and ~1 μm wide) 4H-SiC mesas etched with an anisotropic etching process is available with current processing technology. By using this process, super-junction structures with a drift region length of 5 μm and N/P stripe width of 1 to 2 μm is possible.

Etching of substantially deeper (10 to 20 μm) trenches with similar widths remains as a major challenge. With development of SiC anisotropic etching process, trenches with increasing aspect ratios will be able to be achieved and super-junction structures with more superior FOMs will become practically possible.

2.6 Summary

Possibility of breaking the theoretical unipolar limit of 4H–SiC device by using super-junction structures has been investigated. It was found that with a reasonably large drift region column aspect ratio and optimum doping design, FOMs more than an order of magnitude higher than the theoretical limit could be achieved.

A new analytical model has been developed for super-junction devices in 4H-SiC. The model is concise, simple, and easy to use yet still provides good accuracy in predicting the breakdown voltage and specific on-resistance for a large variety of super-junction structures with different dimensions and doping concentrations. Charge imbalance effects have also been modeled accurately.

The usefulness of the model developed in this work has been demonstrated through a design example of optimizing a 1000-V super-junction device. It has been seen that, for a

given N/P-stripe width that is possible in device processing, the proposed model can quickly provide an optimum structure for what might take weeks through numerical simulations. The model can therefore provide valuable guidelines for future developments of super-junction devices on 4H-SiC.

Practical feasibility of the proposed structure is also discussed. It is pointed out with the currently available technology, a structure which is capable of giving four times lower R_{SP_ON} than the theoretical limit at the same V_{BR}, is achievable.

3 DEVELOPMENT OF A WAFER-LEVEL HALL MOBILITY MEASUREMENT TECHNIQUE

3.1 Introduction

The performance and reliability of MOSFET are strongly limited by the quality of the gate-dielectric/substrate interface. Low quality interface can lead to shifted threshold voltage, high leakage current and low channel mobility. In the development of advanced/novel devices, such as SiC power MOSFETs, high-k based MOSFETs, and III-V channel material based devices, improving channel mobility is often the first and foremost challenge [63-65]. The ability to measure mobility accurately is the prerequisite for a clear understanding on the degradation mechanisms. Split-CV is the most frequently used mobility measurement method. It is not an easy measurement and its accuracy decreases when the device is ultra small [66] or when there is a high level of charge trapping [64, 65]. While correction methods exist for split-CV in those situations [64, 66], the complexity of implementation is further increased. Hall-mobility measurement is an appealing alternative, which is immune to the aforementioned shortcomings. However, other than being used as a calibration for the corrected split C-V measurement [66], it is not often used due to the expensive regular Hall measurement system and tedious sample preparation. In addition to a bulky, expensive and dedicated setup, wafer dicing, wire bonding and device packaging inhibit frequent measurements. Any wide-ranging survey using a large number of samples requires a heroic measurement effort. Fig.3.1 shows the equipment necessary for sample preparation and measurements of regular Hall system. The total cost is well above US$20,000.

In this work, we demonstrated a wafer-level Hall mobility measurement method, which requires neither packaging nor a bulky/expensive system. It greatly reduces the efforts needed for Hall measurements and makes device characterization much more convenient. Fig.3.2 shows a picture of the wafer-level Hall mobility measurement system we developed. Moreover, an AC modulation is employed to improve the signal-to-noise ratio and make the measurement more immune to device drift than the regular Hall measurement method. This is a very important improvement for accurately characterizing novel devices, in which a high level of charge trapping exists.

Fig.3.1 Equipment for sample preparation and measurement of regular Hall measurement system (wafer-dicing machine, wire bonder, electro-magnet and recirculating chiller).

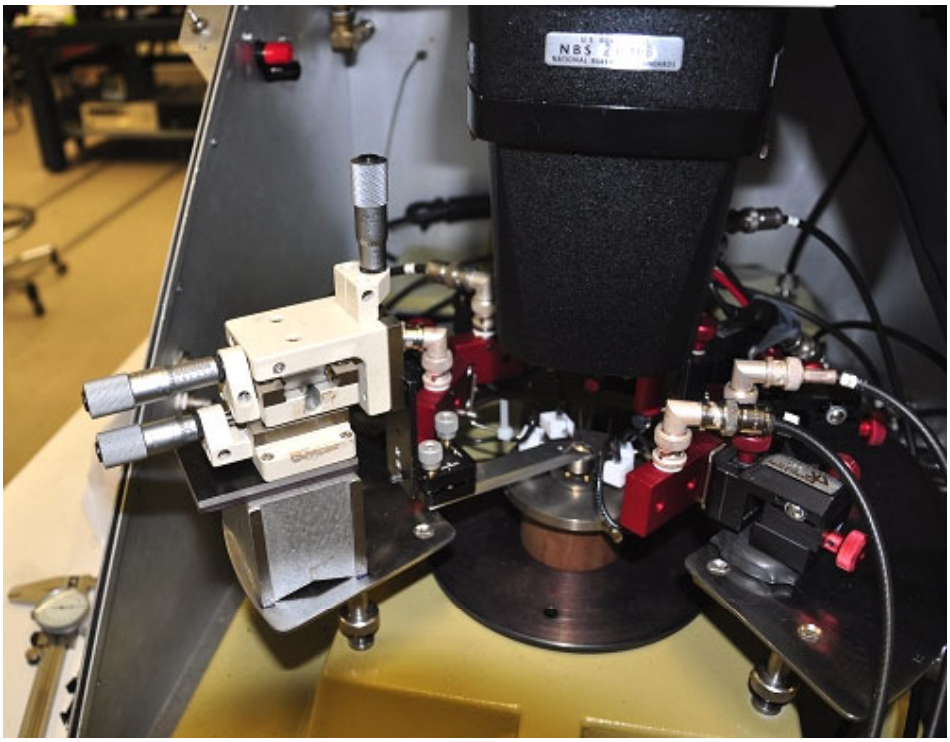


Fig.3.2 Wafer-level Hall mobility measurement system.

3.2 Experiment

3.2.1 Realization of strong and uniform B fields

In Hall measurements, a strong and uniform magnetic field is required. The key of our approach is the realization that such requirement can be satisfied by bringing a permanent magnet very close to the device. In our experiment, a donut-shaped permanent magnet with 3 mm inner diameter is placed above the device under test using a micro-positioner with high precision (25 μm resolution), as shown in Fig.3.3. The probe tips are bended to provide enough room for bringing the permanent magnet very close to the device in order to provide strong magnetic fields. A photo of this customized placement of the magnet is shown in Fig.3.4.

The area of the device is orders of magnitude smaller compared to the size of the permanent magnet, which allows the magnetic field to be very uniform across the device. By bringing the magnet very close to the device, a maximum field of 3200 Gauss is achievable. The relationship between the magnetic field and the vertical separation distance is calibrated by a small (0.016 mm^2 active area) commercial Hall Sensor. As shown in Fig.3.5, three calibrations are performed on different days and different time of the day. The variation between them is well within 10 Gauss (as shown in Fig.3.6), which is comparable to commercial Hall measurement system. This variation takes into account the error caused by manual control of the micro-positioner and the effect of temperature changes in the lab. The magnetic field controlled by the micro-positioner is very repeatable.

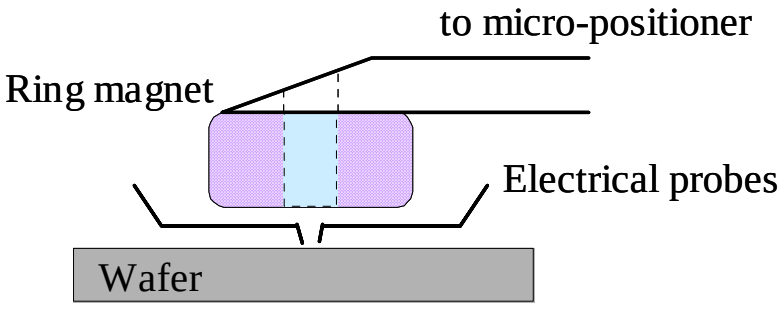


Fig.3.3 Schematic of the realization of a strong and uniform magnetic field.

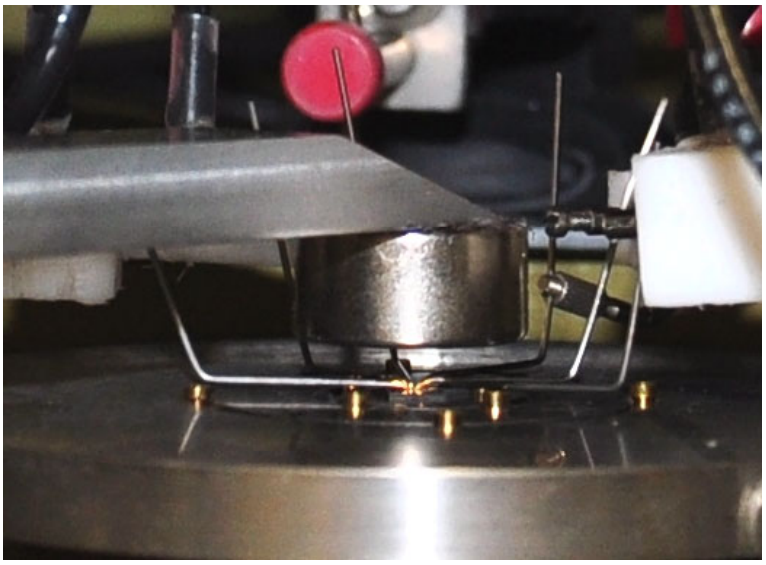


Fig.3.4 Photo of the placement of the magnet and the customized probe tips.

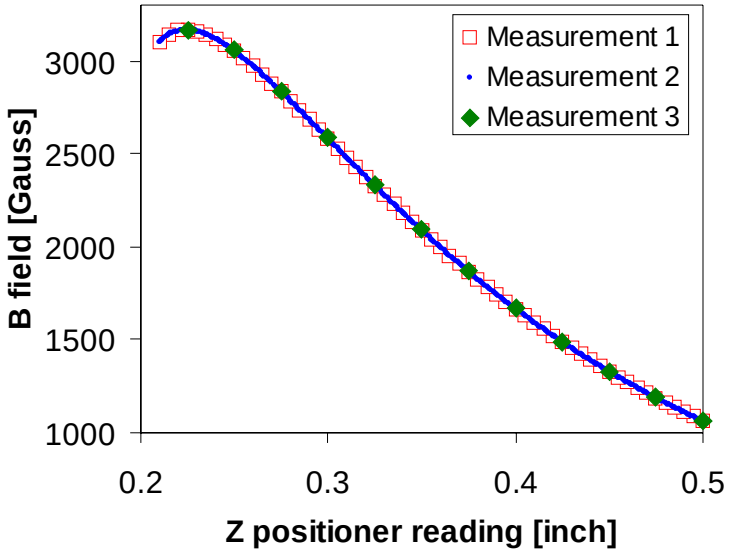


Fig.3.5 Magnetic field calibration as a function of z positioner readings. Three measurements performed on different days and different time of the day agree very well. The variation is well within 10 Gauss.

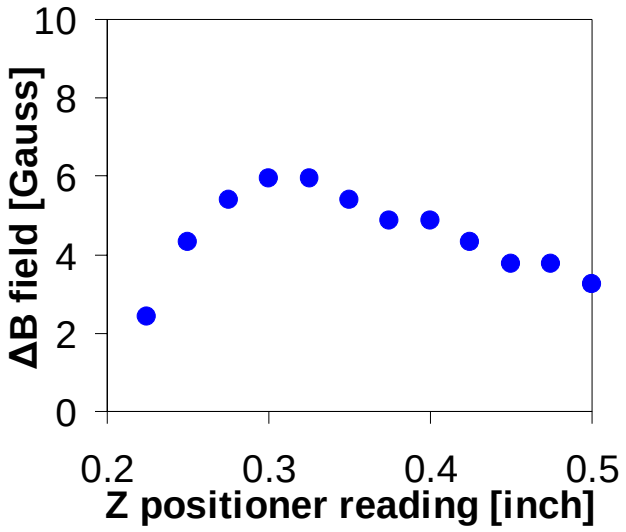


Fig.3.6 B field variation within three measurements performed on different days and at different time of the day.

3.2.2 Measurement of sheet charge density n_s

In this work, we utilize this Hall set-up to examine 4H-SiC n-channel MOS-gated Van der Pauw structures with 150 μm × 150 μm gated area.

In order to get μ_{Hall}, inversion sheet charge density (n_s) and sheet resistance (R_s) are measured separately. In the n_s measurement, the gate is kept at a certain potential, the source and substrate are grounded and the drain voltage is modulated by a square wave with frequency of 127 Hz and 310 Hz and $t_{rise} = t_{fall} = 300$ μs. The differential voltage between the two Hall terminals is measured using the differential amplifier stage inside a lock-in amplifier (100 MΩ input impedance). The gains of the amplifier at different sensitivity levels are measured with a small voltage pulse. The drain to source current is monitored at the source terminal with a current amplifier. The traces of Hall voltage and source current are monitored using an oscilloscope. The set-up is shown in Fig.3.7. The

use of drain voltage modulation allows the signal-to-noise ratio to be improved significantly by averaging. The short measurement time also prevents complications due to device drift during the measurements. This is especially important when measuring SiC MOSFETs, which are known to have significant as-processed charge trapping and de-trapping [67].

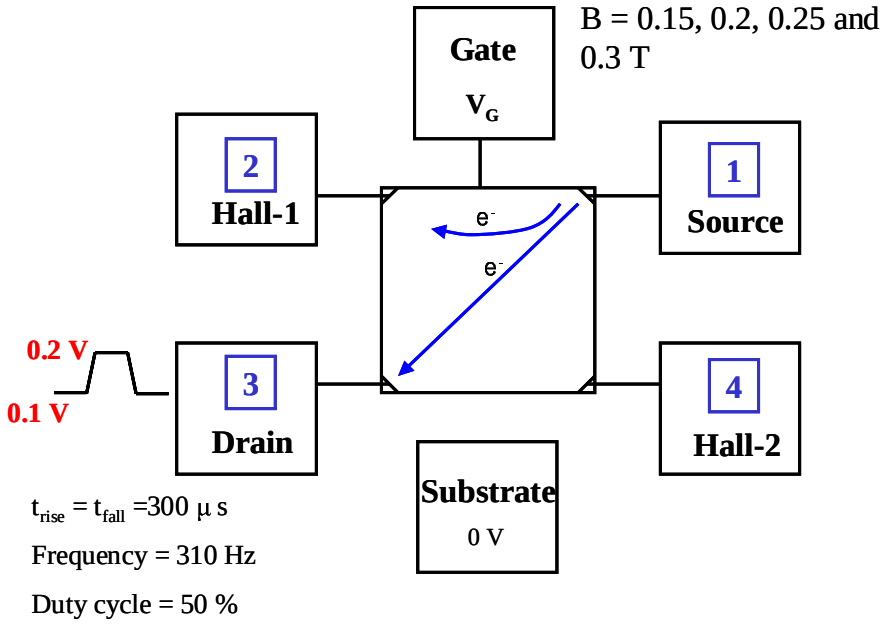


Fig.3.7 Experimental set-up for the measurement of sheet charge density n_s. A gated Van der Pauw structure with 150 μm × 150 μm gate area is employed. An AC drain voltage modulation is used to improve the signal-to-noise ratio.

3.2.3 Measurement of sheet resistance R_s

The sheet resistance (R_s) is measured with standard Van der Pauw procedures [68] modified a bit by employing an AC modulation, which shortens the duration of measurement and helps to improve the signal-to-noise ratio. As illustrated in Fig.3.8, under a certain gate bias, an alternating voltage is forced on terminal 3 and the current

from terminal 3 to terminal 2 (I_{32}) is monitored by a current amplifier. The voltage difference between terminal 4 and 1 (V_{41}) is measured by the differential amplifier stage of a lock-in amplifier. $R_{32,41} = V_{41} / I_{32}$ is calculated. Repeat this measurement on different edges of the device and with forward and reverse current directions. R_s can be determined by the following equations. With n_s and R_s, Hall mobility can be easily calculated using $\mu_{Hall} = 1 / (q \times n_s \times R_s)$.

$$R_A = (R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21})/4 \quad \text{Eq.3.1}$$

$$R_B = (R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32})/4 \quad \text{Eq.3.2}$$

$$\exp(-\pi R_A/R_s) + \exp(-\pi R_B/R_s) = 1 \quad \text{Eq.3.3}$$

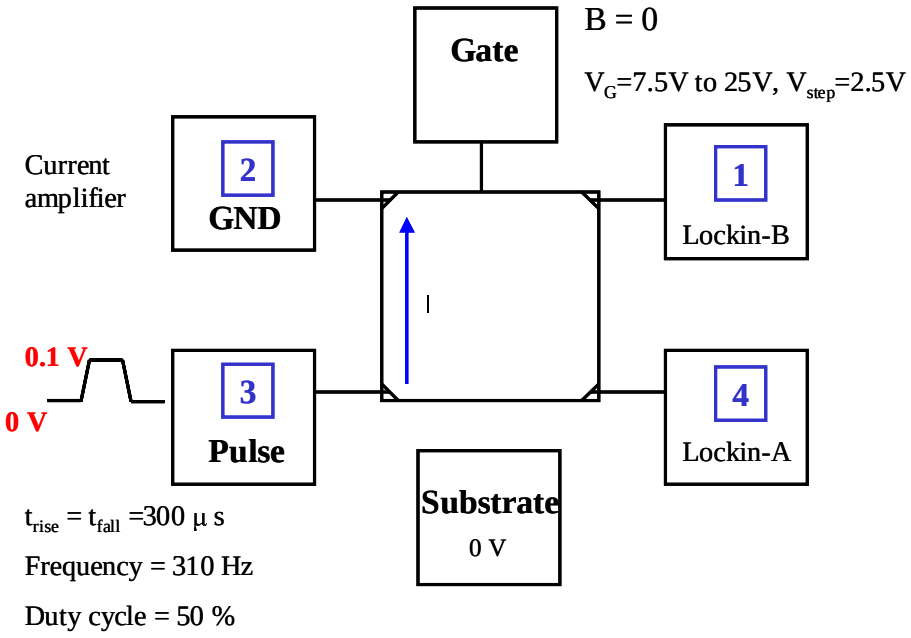


Fig.3.8 Van der Pauw procedure for measurement of sheet resistance (R_s). An AC modulation is used to shorten the measurement time and improve the signal-to-noise ratio.

3.3 Results and Discussions

3.3.1 Hall mobility

Fig.3.9 shows the measured waveforms from the Hall terminals corresponding to the drain voltage modulation at four different magnetic fields and with a constant gate voltage of 20 V. The source current is also plotted on the secondary axis, measured by a current amplifier. The peaks at each transition are due to displacement current arising from the asymmetry in the device geometry as well as the parasitics in the measurement system. A zoom-in view of the upper flat region of the differential voltages is shown in Fig.3.10. As B field increases, the differential voltage measured between terminal 2 and 4 decreases, which is consistent with the electrons build-up at terminal 2 as depicted in Fig.3.7.

The asymmetry also produces an offset voltage in the measured differential voltage, as expressed in Eq.3.4 where V_{diff} is the voltage difference between the Hall terminals, V_o is the offset voltage, B is the magnetic field, I is the drain or source current and q is the electron charge. While the voltage difference between the two flat regions (dV_{diff}) is the sum of the actual Hall voltage change and the offset voltage change, only Hall voltage changes as the magnetic field increases. By measuring the voltage difference at a few magnetic fields, the two contributions can be separated. Fig.3.11 plots dV_{diff}/dI as a function of B field at a constant gate voltage of 20 V. According to Eq.3.5 the inversion sheet charge density n_s can be directly extracted from the slope in Fig.3.11.

$$V_{diff} = V_o + \frac{BI}{qn_s} \qquad \text{Eq.3.4}$$

$$\frac{dV_{diff}}{dI} = \frac{dV_o}{dI} + \frac{B}{qn_s} \qquad \text{Eq.3.5}$$

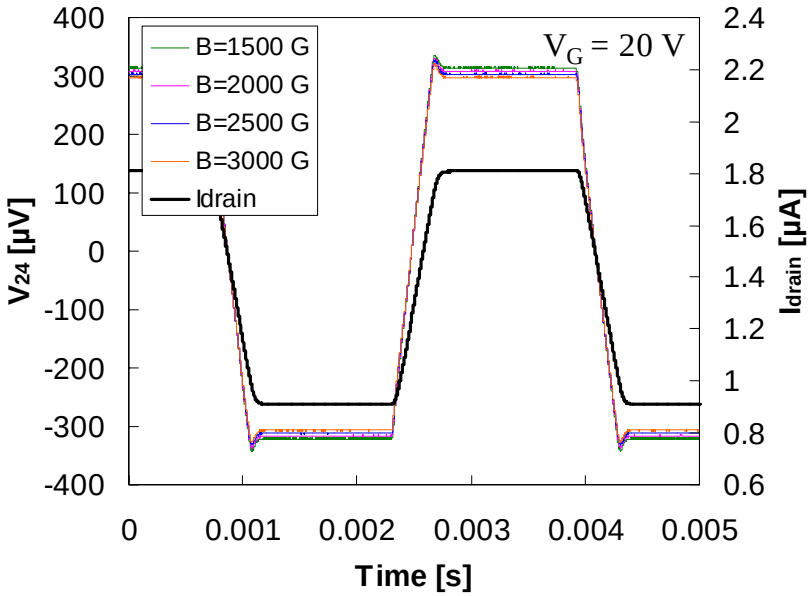


Fig.3.9 Differential voltage waveforms between the Hall terminals corresponding to the drain voltage modulation at four magnetic fields. Source current is measured with a current amplifier and plotted on the secondary y-axis.

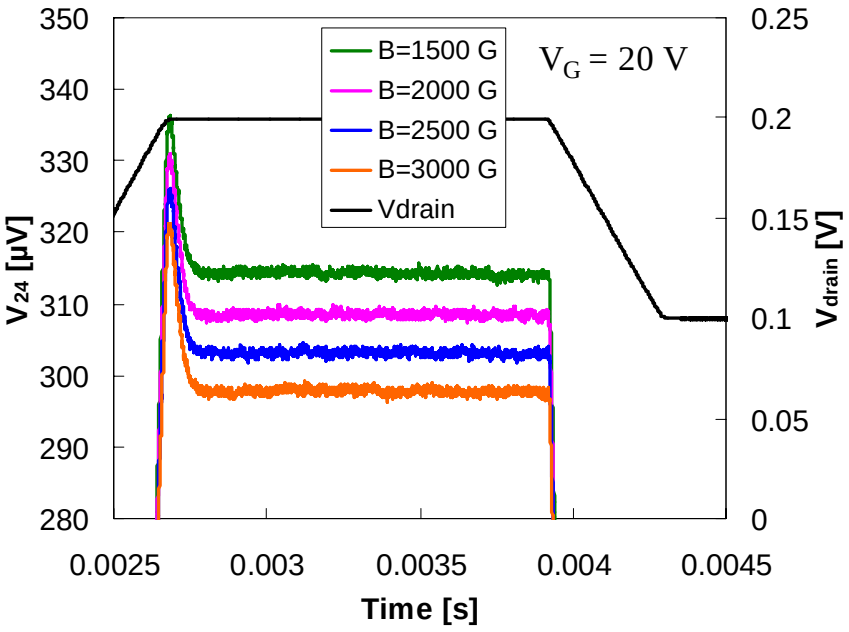


Fig.3.10 Zoom-in view of the change of differential voltage corresponding to the magnetic fields.

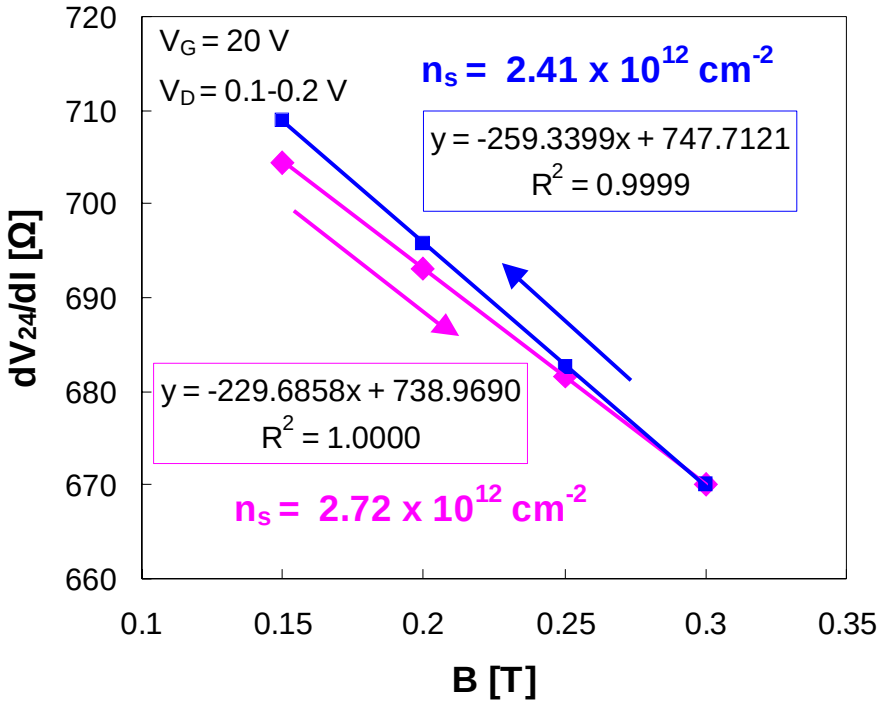


Fig.3.11 n_s extraction from the differential voltage waveforms measured at four magnetic fields. dV_{diff}/dI is plotted as a function of B field. n_s is extracted from the slope. This measurement is done with V_G = 20 V. There is a small amount of drift during the measurement. The error due to drift can be cancelled by averaging the two n_s.

It should be noted that there is a small amount of drift during the measurement. As shown in Fig.3.11, dV_{24}/dI is measured with B field increasing from 1500 Gauss to 3000 Gauss and then decreasing back to 1500 Gauss. The sheet charge density extracted from the two lines has about 10% difference. The cause of this drift is probably due to the amplifier drift. By minimizing the total measurement time, the error caused by the drift could be reduced. Therefore, in the following measurements, only two magnetic fields, 1500 G and 3000 G, are used in order to shorten the total measurement time. Within the short duration of measurement, the drift term can be linearly approximated. Therefore, by

averaging the two sheet charge densities extracted from Fig.3.11 the error due to drift can be cancelled out.

Same measurements and extractions are done with eight gate voltages from 7.5 to 25 V with 2.5 V step. Sheet charge density is plotted as a function of gate voltage in Fig.3.12. Sheet resistance R_s is also plotted in the same figure, measured by the Van der Pauw procedures with AC modulation described in 3.2.3. The Hall mobility is calculated from $\mu_{Hall}=1/(qn_sR_s)$. Fig.3.13 shows the Hall mobility as a function of gate bias. It has very weak dependence on the gate voltages investigated. This is not what one would expect for a high-quality Si-based MOSFET, however for novel devices based on SiC, it is common. Similar dependency has been reported on SiC devices measured by regular Hall measurement systems [69, 70]. The measured mobility is very small compared to the bulk value. This is also well known for SiC MOSFETs.

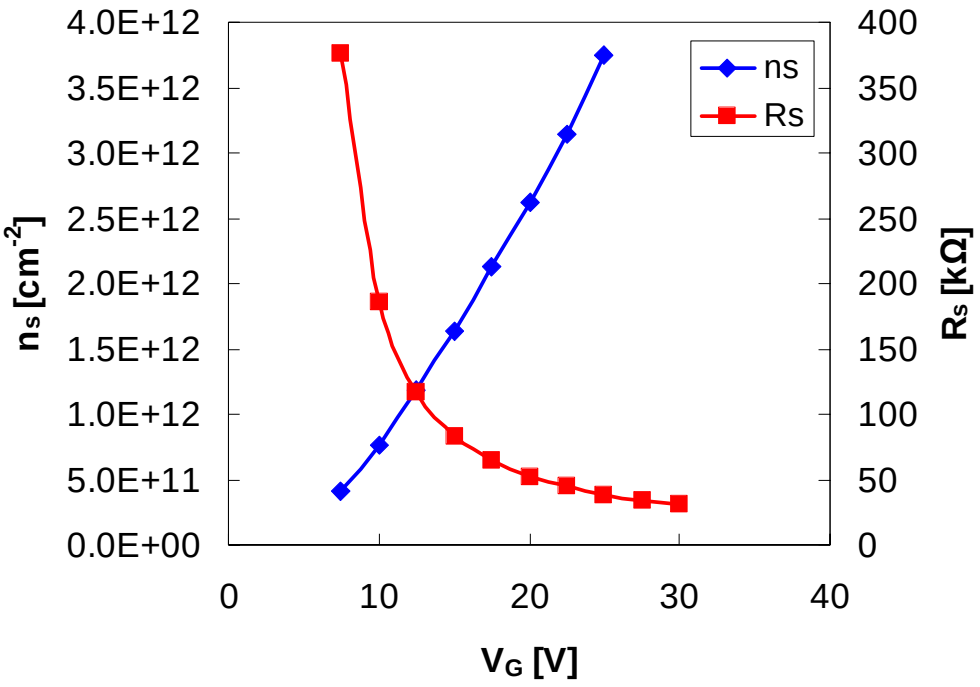


Fig.3.12 Inversion sheet charge density and sheet resistance measured as a function of gate voltage.

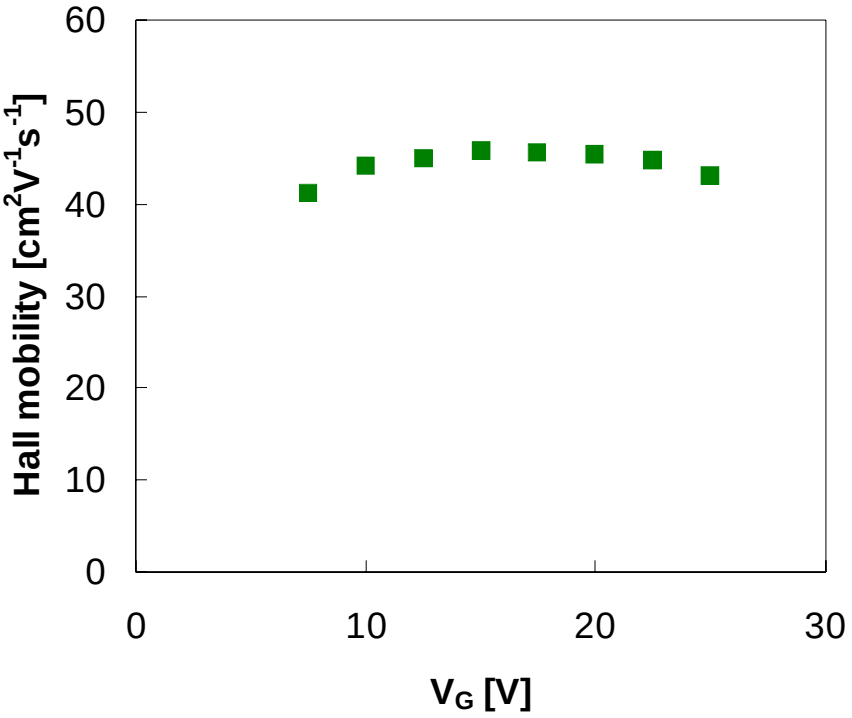


Fig.3.13 Hall mobility calculated from R_s and n_s as a function of gate voltage.

3.3.2 Field effect mobility and effective mobility

Due to the tedious sample preparation as well as the bulky and expensive equipment required by the regular Hall measurement, field effect mobility (μ_{FE}) and effective mobility (μ_{eff}) are most often employed to evaluate the quality of the device. Field effect mobility can be calculated using Eq.3.6. Effective mobility can be calculated with Eq.3.7, where Q_n is often estimated by either C_{ox} and V_{TH} (Eq.3.8) or by split-CV measurement (Eq.3.9). These calculations of Q_n overestimates the sheet charge density because it does not take into account the trapped charge and threshold voltage shift due to charge trapping. The sheet charge density obtained by the Hall measurement and that calculated

using C_{ox} and V_{TH} are compared in Fig.3.14. It can be seen that the sheet charge density calculated from Eq.3.8 is overestimated by a factor of 100% compared to n_s measured by the Hall measurement.

$$\mu_{FE} = \frac{L \cdot g_m}{W \cdot C_{ox} \cdot V_{DS}}, \text{ where } g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}} \quad \text{Eq.3.6}$$

$$\mu_{eff} = \frac{L \cdot g_d}{W \cdot Q_n}, \text{ where } g_d = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}} \quad \text{Eq.3.7}$$

$$Q_n = C_{ox} \cdot (V_G - V_{TH}) \quad \text{Eq.3.8}$$

$$Q_n = \int_{-\infty}^{V_G} C_{GC} \cdot dV_{GS} \quad \text{Eq.3.9}$$

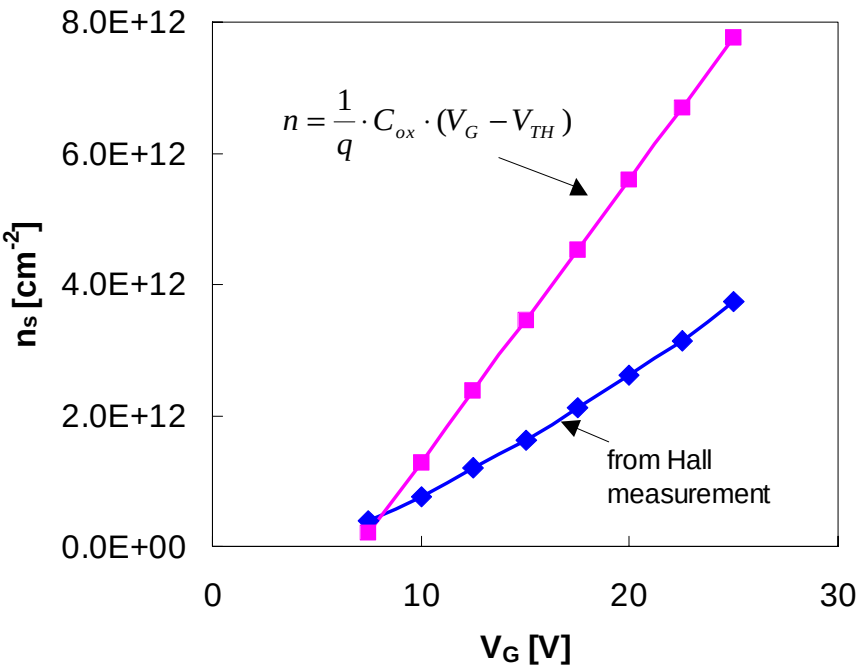


Fig.3.14 Comparison of sheet charge density obtained by the Hall measurement and that calculated with C_{ox} and V_{TH}.

The field effect mobility and effective mobility are calculated based on the I-V curves measured on a 100 μm × 100 μm N-channel MOSFET, which is adjacent to the gated Van der Pauw structure used for the wafer-level Hall measurement. In Fig.3.15, μ_{FE} and μ_{eff} are compared to the Hall mobility as a function of gate bias. They are about half the value compared to μ_{HALL}.

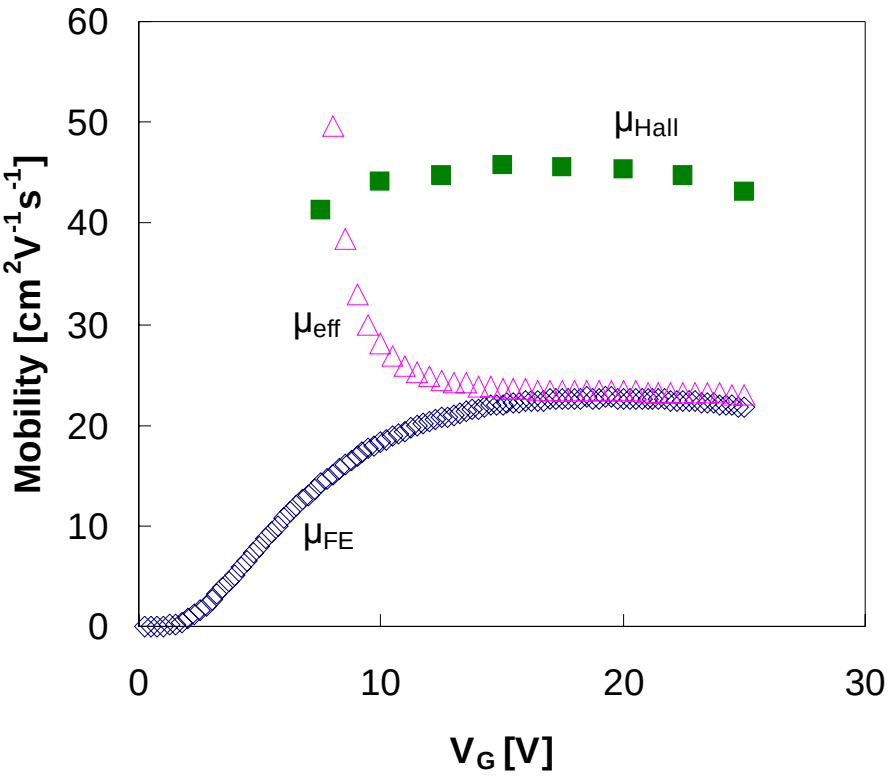


Fig.3.15 Comparison of field effect mobility, effective mobility and Hall mobility as a function of gate bias.

3.3.3 Effects of parasitic capacitance

In the first batch of Van der Pauw structures measured, there was no field oxide underneath the metal pads. Therefore, the transient peaks in the waveforms of the differential voltage have large time constants. These transient peaks limit the maximum

modulation frequency that can be used in the measurement, which limits the signal-to-noise ratio. Fig.3.16 compares the waveforms of differential voltage measured on two Van der Pauw devices with and without field oxide under the metal pads. Measurement accuracy can be improved by minimizing the parasitics. This is especially important for measurements under low gate biases, when the large sheet resistances contribute significantly to the time constants as well.

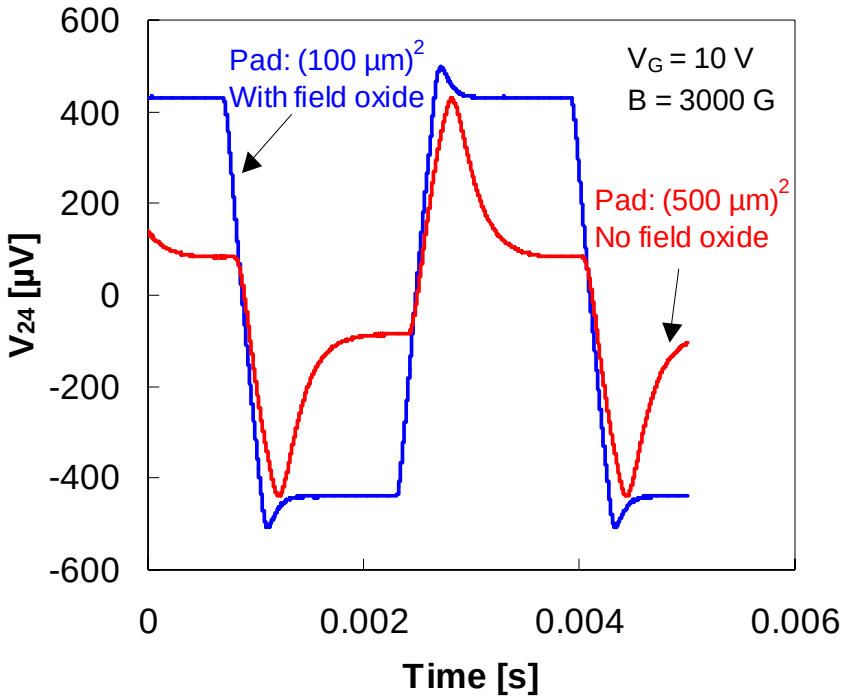


Fig.3.16 Differential voltages measured on devices with different parasitic capacitances (different pad sizes with or without field oxide) at the gate voltage of 10 V and a magnetic field of 3000 Gauss.

3.3.4 Comparison with the regular Hall measurement method

In order to examine the accuracy of the efficient and cost-effective wafer-level Hall mobility measurement technique, a comparison with the regular Hall mobility measurement method is performed. After the wafer-level Hall measurements, the same

device is wire-bonded, packaged and taken to the regular Hall measurement system as shown in Fig.3.1.

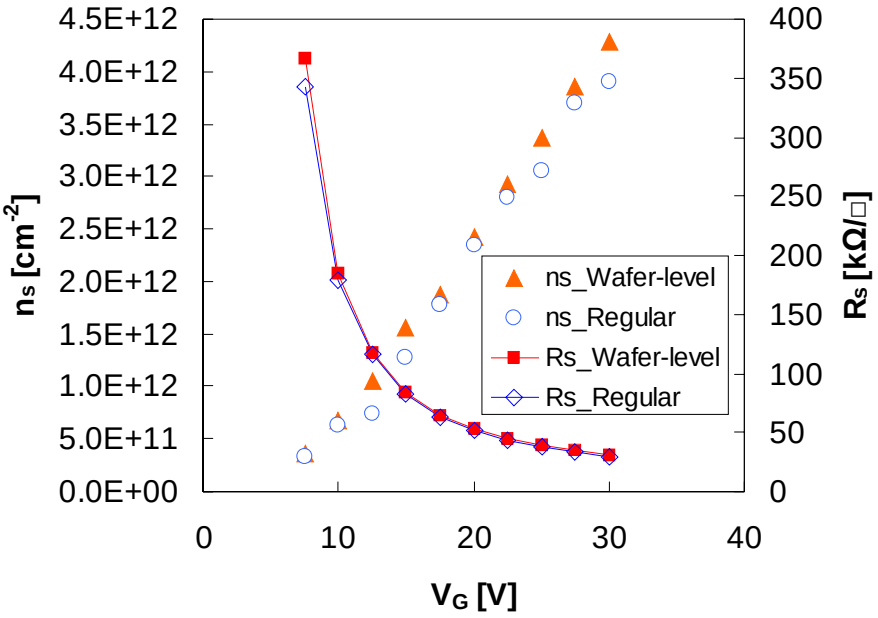


Fig.3.17 Comparison of the sheet charge density (n_s) and sheet resistance (R_s) measured by the regular Hall method (hollow symbols) and our wafer-level Hall mobility measurement technique.

The comparison of the two measurement methods is shown in Fig.3.17 and Fig.3.18. They agree very well except for a few data points. A close examination shows that the disagreement is due to the long measurement time associated with the regular Hall measurement, which is around 20 minutes for each of the data points. While on the other hand, it takes only one minute to measure one data point using the wafer-level Hall measurement technique. In novel devices like SiC MOSFETs, high level of charge trapping contributes significantly to the device drift over time. Therefore, measurement time should be minimized in order to obtain accurate results. The AC modulation employed in the wafer-level Hall measurement improves the signal-to-noise ratio greatly

by averaging. The short measurement time makes this method more immune to device drift than the regular approach.

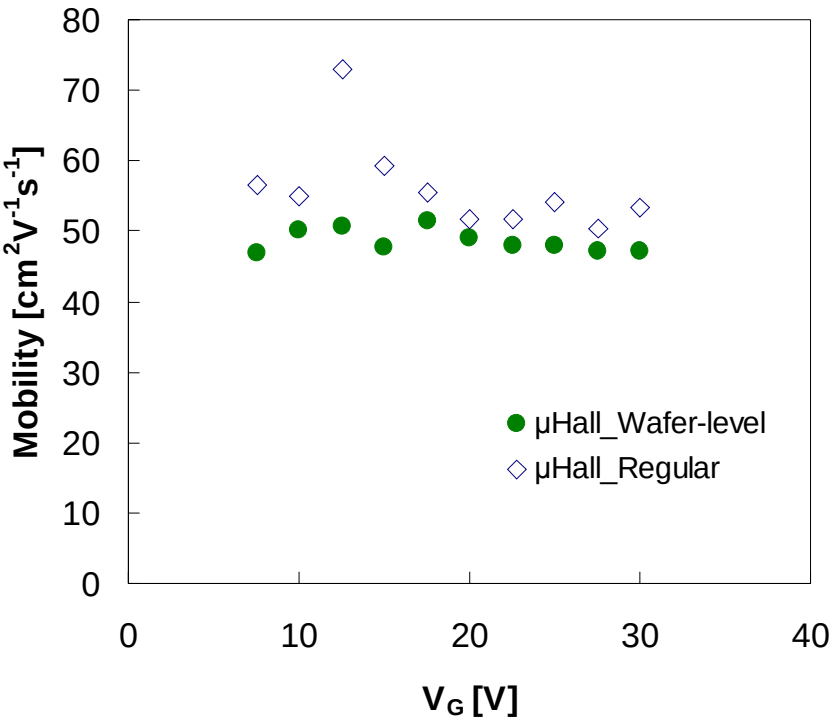


Fig.3.18 Comparison of the Hall mobility measured by the regular Hall method (hollow symbols) and our wafer-level Hall mobility measurement technique.

3.4 Summary

In this work, we have demonstrated a fast wafer-level Hall-mobility measurement method that does not require any wafer dicing, wire bonding, packaging nor the bulky, expensive regular Hall measurement system. This method is very efficient and cost-effective. Device characterization and development are much more convenient by using this technique. Wide-ranging survey of a large number of devices can be performed with much less experimental effort.

An AC modulation is employed to improve the signal-to-noise ratio and make the measurement more immune to device drift than the regular Hall measurement method. This is a very important improvement for accurately characterizing novel devices, in which a high level of charge trapping exists. With this method, further explorations of interactions between interface traps and channel carriers as well as mobility degradation mechanisms become possible.

4 CHARACTERIZATION OF OXIDE RELIABILITY

4.1 Introduction

Harsh environments, mainly high temperature, are expected in a variety of measurement and control applications, such as automotive, aerospace, energy production and other industrial systems. Silicon-based electronics are problematic when ambient temperature exceeds 200 °C due to high internal junction temperature and large leakage currents. The wide-bandgap nature of silicon carbide (SiC) produces a dramatic reduction in the intrinsic carrier density (19 orders of magnitude) and allows for more stable high-temperature electronics. In addition to the outstanding electronic properties, SiC's excellent mechanical and thermal stability as well as chemical inertness and radiation hardness are well suited to gas sensing and UV detection in hostile environments [2, 71-73].

Among all power device structures, the MOS-controlled devices are favorable due to their high input impedance and low switching losses, which make power electronic circuits more controllable with higher efficiency. However, studies of SiC MOSFET reliability raised significant concerns on the long-term operation of SiC MOS-based devices, especially at high temperatures. Lelis et al. [74] demonstrated that the threshold voltage is not stable due to electron tunneling into and out of the oxide traps. Gurfinkel et al. [67] showed that the conventional DC measurement technique underestimated the threshold voltage instability as fast transient trapping and de-trapping events cannot be captured with a slow sweep rate. They also found that post-oxidation annealing in NO

dramatically reduces the instability. Yu et al. [75] reported evidence of channel hot-carrier in SiC MOSFET operated at moderate drain bias.

The most important reliability concern is gate oxide reliability. Early experimental results of insulators on SiC suggested that SiO_2 on SiC was not reliable at high temperatures. Lipkin et al. [42] investigated several dielectric materials as gate insulator on 6H-SiC. All of them showed lifetimes below 1000 seconds at 6 MV/cm and 350 °C. Maranowski et al. [41] performed time-dependent dielectric breakdown (TDDB) measurements of thermal oxides on 6H-SiC. The lifetime distributions showed a large extrinsic population and the mean-time-to-failure (MTTF) extracted from the intrinsic failures suggested that acceptable reliability can only be maintained if the electric field is kept below 5 MV/cm and the temperatures is kept below 150 °C. This precludes most of the high-temperature applications where SiC is expected to excel. Singh and Hefner [38] argued that if Fowler-Nordheim (FN) tunneling is assumed, oxide reliability on SiC is fundamentally limited by its smaller conduction-band offset (Φ_B) compared to Si (2.7 eV versus 3.1 eV of Si). Agarwal et al. [39] studied the temperature dependence of Fowler-Nordheim tunneling current in 6H- and 4H- SiC capacitors and extracted effective barrier height (Φ_{eff}) from the FN plots to be 2.43 eV at 25 °C and reduced significantly to 1.76 eV at 325 °C. With a temperature-dependent flat-band voltage correction, Waters et al. [40] reported even smaller Φ_{eff} of 1.92 eV at room temperature and around 1.1 eV at 300 °C. Serious concerns have been raised about the reliability of SiC power MOS devices operating at elevated temperatures. Long-term TDDB measurements at high temperatures are required to truly understand the reliability of silicon oxide grown on SiC.

Recently, more TDDB measurements of oxide reliability on SiC showed great improvements. Matocha et al. [43] reported a mean-time-to-failure (MTTF) of 2300 hours at 6 MV/cm and 250 °C on MOS capacitors thermally grown with N_2O and NO annealing. Yu et al. [44] reported $t_{63\%}$ of 215 hours measured at 6.4 MV/cm and 375 °C. Using TDDB with constant current stress, Fujihira et al. [45] found that charge-to-breakdown (Q_{BD}) increased from 0.1 C/cm^2 to 10 C/cm^2 by employing N_2O annealing. Ongoing research is being conducted to further improve oxide reliability. Suzuki et al. investigated the oxide reliability on Carbon-face 4H-SiC (000-1) substrate with N_2O nitridation [76] and dry oxidation plus various pyrogenic reoxidation annealing conditions [77]. Fujihira et al. compared the reliability of thermal oxide and chemical-vapor-deposited oxide with constant-current-stress TDDB [78]. Extrinsic failure is also under investigation. Senzaki et al. correlated the oxide reliability with metal impurity concentration in the wafer [79] and basal plane dislocations in the epitaxial layer [80]. While Matocha et al. [46] showed contradictory observations that no correlation was found between oxide breakdown pit and the dislocations in the epitaxial layer. Studies of oxide reliability of DMOSFET showed promising results as well. Krishnaswami et al. [81] performed TDDB measurements on 2 kV 4H-SiC DMOSFETs at 175 °C and extrapolated the MTTF to 3 MV/cm to be longer than 100 years. The lifetime of DMOSFETs was found about two orders of magnitude smaller than that of NMOS capacitor. Matocha et al. [46] also observed lower lifetime on DMOSFETs.

In most of the gate oxide reliability measurements, due to constraints on the total measurement time, high electric fields are used to accelerate oxide breakdown and lifetimes at lower electric fields (normal operation conditions) are extrapolated using the

high-field data. Therefore the field-acceleration model and the field-acceleration factor employed in the lifetime prediction are of crucial importance. The recently observed change of the field-acceleration factor might indicate a change of breakdown mechanisms at around 9 MV/cm for 4H-SiC MOS devices with an oxide thickness of ~50 nm [46]. A natural question would be "Is there any other mechanism change at lower electric fields?" The only way to answer this question is to perform long-term reliability tests at lower electric fields.

In this work, TDDB measurements are performed on 4H-SiC MOS capacitors and DMOSFETs with constant-voltage-stress at various temperatures and electric fields. Long-term stress experiments over 7 months in duration have been done at 6 MV/cm and 300 °C. The results indicate that the high-field data can be extrapolated to lower fields with no change in field-acceleration factor. Weibull slopes (β) with 95% confidence intervals are extracted from the failure distributions and used as an indicator of oxide quality. A more accurate method to extract β using area scaling is also presented. Temperature dependence and thermal activation energy are also reported. Since our reliability data *contradicts* the widely accepted belief that silicon oxide on SiC is fundamentally limited by its smaller conduction band offset compared to Si, a detailed discussion is provided to examine the arguments of the early predictions.

4.2 Experiment

4H-SiC MOS capacitors of various gate areas were fabricated on 4H-SiC, Si-face, 4° off axis, lightly-doped n-type epilayers ($n \approx 1\times10^{16}$ cm^{-3}). A chemical-vapor deposited field oxide was deposited and patterned to form the active area of the capacitors. Next, a

47 nm silicon oxide was thermally grown in N_2O at 1250 °C and NO at 1150 °C, followed by gate electrode formation and patterning.

Constant-voltage-stress TDDB measurements at four temperatures (375 °C, 300 °C, 275 °C and 225 °C) and electric fields between 6 and 10 MV/cm were investigated. For each of the stress conditions, 20 or more devices were tested. The schematic of the test set-up is shown in Fig.4.1. Twenty devices are tested simultaneously on a specially designed hot chuck. A water-cooled probe card with 20 pins connects each of the devices under test to the power supply through a series resistor. Fig.4.2 shows a microscope picture of the pins of the probe card and the capacitors under test. The voltages across each resistor are monitored sequentially using a multi-channel scanner and a digital voltage meter. At device breakdown, the time to failure is recorded and the broken device is disconnected from the voltage source to ensure that the thermal dissipation from the broken device does not interfere its adjacent devices. All the equipments are connected to a computer through GPIB cables.

The times to failures were plotted with Weibull statistics and the characteristic lifetime ($t_{63\%}$, time when 63% of the devices have failed) and Weibull slope (β, an indicator of variations within the sample set) were extracted with 95% confidence intervals calculated using the maximum likelihood estimation.

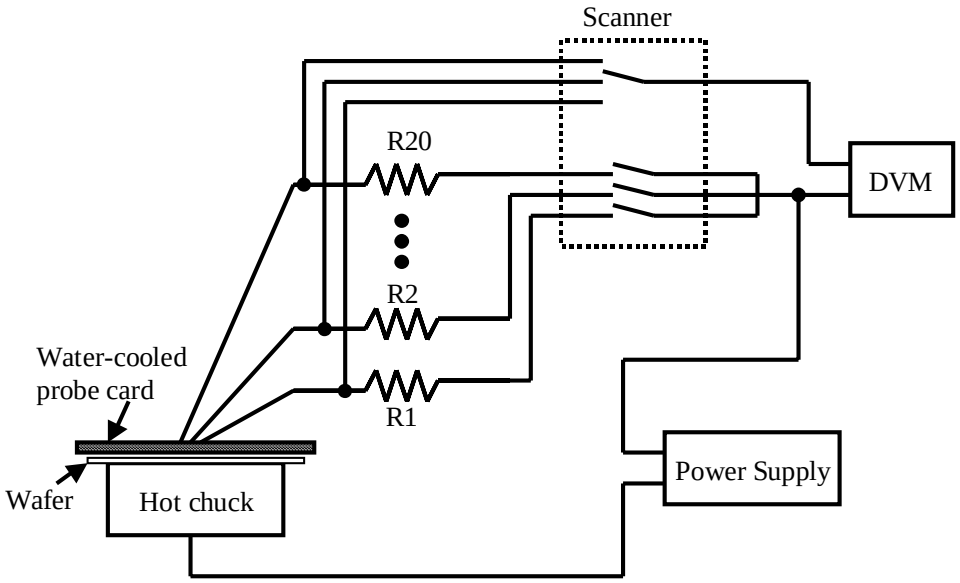


Fig.4.1 Experimental set-up of the time dependent dielectric breakdown measurement.

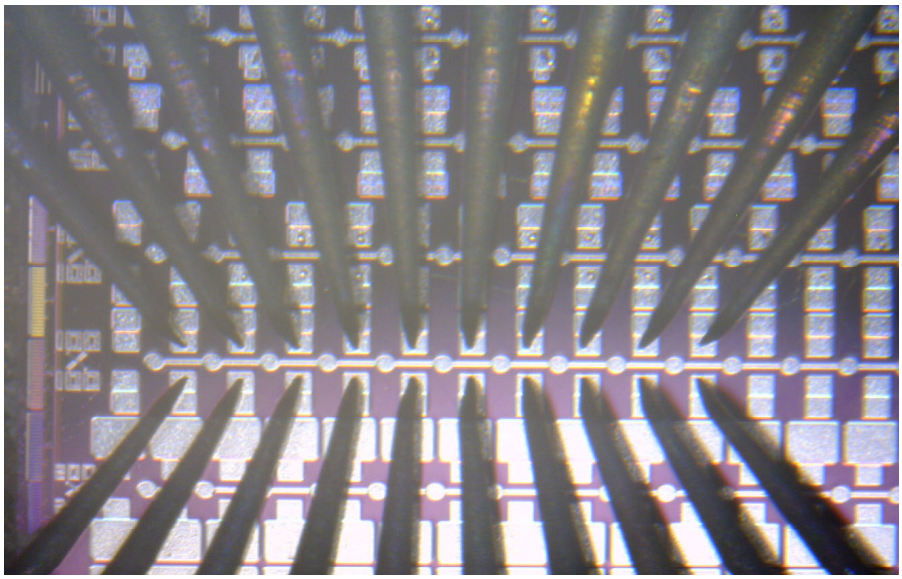


Fig.4.2 Microscope picture of probe card pins and capacitors under test.

4.3 Results and Discussions

4.3.1 Field Acceleration and Lifetime Prediction

Capacitors of size 200 μm × 200 μm were stressed at electric fields between 6 and 10 MV/cm and temperatures between 225 °C and 375 °C. Characteristic lifetimes ($t_{63\%}$) are plotted in Fig.4.3 with 95% confidence intervals indicated by the error bars. Each of the data points is extracted from the lifetime distribution of 20 devices measured by constant-voltage-stress TDDB. Fig.4.4 shows the Weibull distributions at 275 °C with obvious extrinsic failures removed. The Weibull probability distribution is employed in the lifetime projection because although Weibull and lognormal distributions fit data of limited sample number almost equally well, Weibull statistics describe dielectric breakdown of large sample sizes better than the lognormal distribution [82]. As for the field acceleration model, there is a continuing debate over the past three decades in the Si community on the validity of the E model [83] versus the 1/E model [84]. It is still not clear which one is correct. However, the E model is utilized in this work to project lifetime to lower electric fields where devices operate, because it is more pessimistic compared to the 1/E model projection and some experimental data for relatively thick oxide are better fitted by the E model [85, 86].

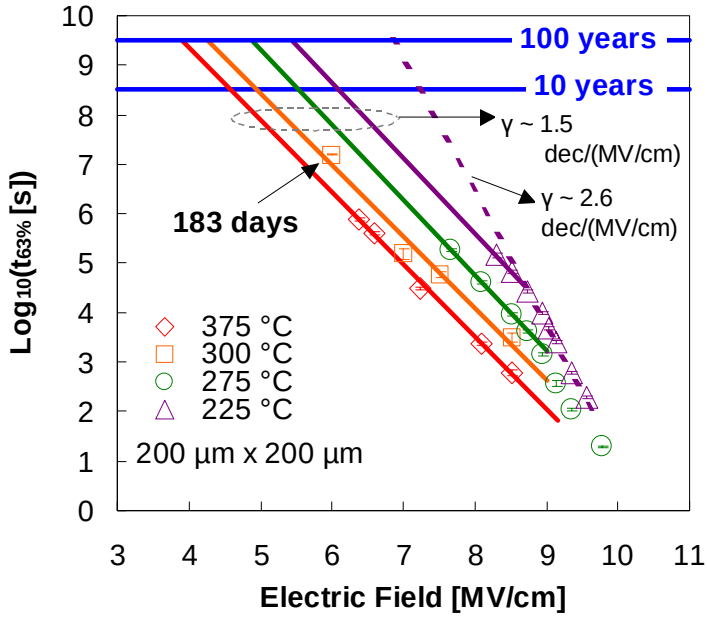


Fig.4.3 Lifetimes are predicted from the measured $t_{63\%}$ using E model. Projection of lifetime is based on data measured below 9 MV/cm. The field-acceleration factor is independent of temperature. Error bars indicate the 95% confidence intervals.

In Fig.4.3, field-acceleration factor changes around 8.5 MV/cm, which is consistent with what Matocha et al. reported [46]. The physics behind this change of field-acceleration factor is still not clear. One possible reason is impact ionization as discussed by Schwalke et al. [87]. The change of field-acceleration factor could also be caused by certain type of extrinsic defect in the oxide, which has a different electric field dependence from the intrinsic field dependence.

Regardless of the mechanism behind the change, lifetimes measured below 8.5 MV/cm all follow a field-acceleration factor of 1.5 decade/(MV/cm) at various temperatures, including one set of devices that lasted more than half a year with stress condition of 6 MV/cm and 300 °C. The projected maximum operation electric field corresponding to lifetimes of 10 years and 100 years are summarized in Table 3.1.

Compared to the experimental data reported ten years ago, the reliability of SiO_2 on SiC has been significantly improved by several orders of magnitude [41, 42].

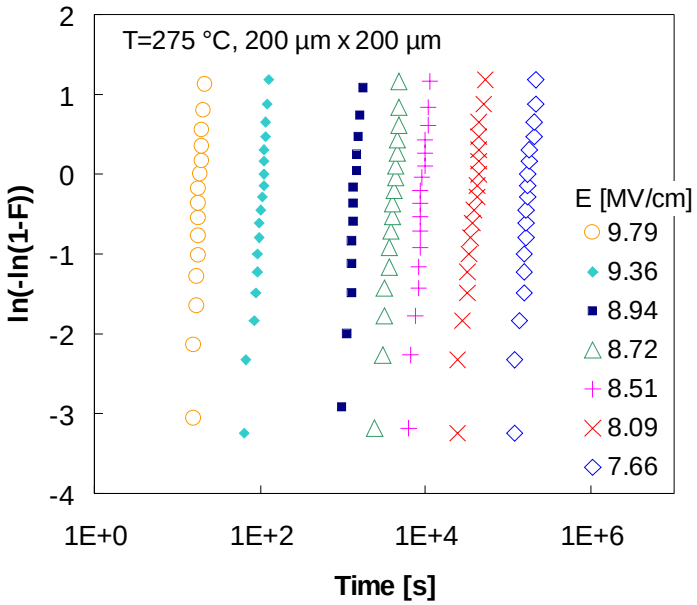


Fig.4.4 Weibull distributions with stress temperature of 275 °C measured on 200 µm × 200 µm capacitors at various electric fields. Obvious extrinsic failures are removed from the distributions.

Table 3.1 Projected Maximum Operation Field

Temperature [°C]	**E_{max} for 10-year life**	**E_{max} for 100-year life**
225	6.1 MV/cm	5.4 MV/cm
275	5.6 MV/cm	4.9 MV/cm
300	5.0 MV/cm	4.3 MV/cm
375	4.6 MV/cm	3.9 MV/cm

A comparison of the TDDB results (measured at 225 °C) between samples provided by two different vendors is shown in Fig.4.5. The basic reliability trends are quite similar. This consistency is a significant milestone. It means, after years of improvements on

fabrication techniques, oxides qualities are converging towards the intrinsic regime. In the silicon community, such consistency was not reached until the mid 1990s.

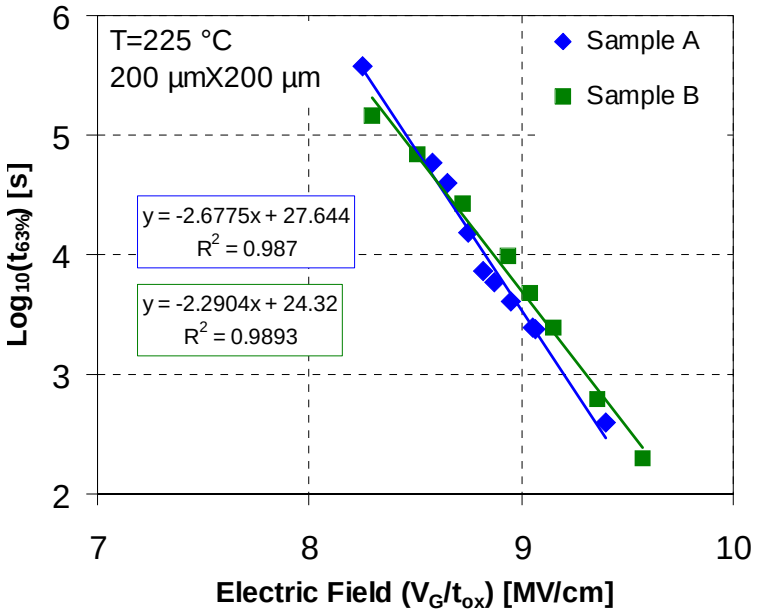


Fig.4.5 Electric field acceleration results (225 °C) of two sets of samples from two different vendors show the same reliability trend.

4.3.2 Weibull Slope and Area Scaling

Are these lifetimes intrinsic yet? Is there still room for further improvement of oxide reliability on SiC? To answer these questions, Weibull distribution of the failures should be examined more closely.

The expression for Weibull distribution is given by

$$F(T_{BD}) = 1 - \exp\left[-\left(\frac{T_{BD}}{t_{63\%}}\right)^{\beta}\right] \qquad \text{Eq.3.10}$$

where F is the cumulative failure, $t_{63\%}$ is the characteristic time when 63 % devices have failed, and β is the Weibull slope. β is an indicator of device variations within the sample set. If the oxides in all the capacitors are intrinsic and only one breakdown mechanism

leads to device failures, a large β value should be expected. The more deviation from the intrinsic quality of oxide or more mechanisms dominate the oxide breakdown, the smaller the β.

Weibull slope is known to be hard to determine accurately without a very large sample size [88]. Fig.4.6 shows failure distributions of MOS capacitors with various areas stressed at 8.09 MV/cm and 275 °C. After a removal of obvious extrinsic failures, the characteristic lifetimes ($t_{63\%}$) and Weibull slopes (β) are plotted in Fig.4.7 with error bars indicating the 95% confidence intervals calculated by maximum likelihood estimation. It can be seen that β has large confidence intervals with a sample size of 20. The large range of β, which varies from 3 to 14, makes it difficult to utilize β as an indicator of oxide quality.

In order to determine β more accurately, area scaling is performed. One unique property of Weibull statistic is that the distributions obtained for two different areas are shifted vertically by a distance proportional to the logarithm of the area ratio as shown by Eq.3.11 [89]. Eq.3.12 derived from Eq.3.11 shows that by plotting $t_{63\%}$ as a function of area in a log-log scale β can be calculated from the inverse of the slope. In Fig.4.7, β determined from area scaling is 7.42. The 95% confidence intervals of $t_{63\%}$ are relatively smaller in a log scale, so β obtained from area scaling of $t_{63\%}$ has substantially smaller error. Using the β value above, Weibull distributions are scaled to the area of 200 μm × 200 μm. As shown in Fig.4.8, all the distributions fall on top of each other, which also confirms the β value determined using the above method is much more accurate than those extracted from the slope of the failure distributions.

$$\frac{t_{63\%}}{t_{63\%}^{'}} = \left(\frac{A^{'}}{A}\right)^{1/\beta} \qquad \text{Eq.3.11}$$

$$\log_{10} t_{63\%}^{'} - \log_{10} t_{63\%} = -\frac{1}{\beta}(\log_{10} A^{'} - \log_{10} A) \qquad \text{Eq.3.12}$$

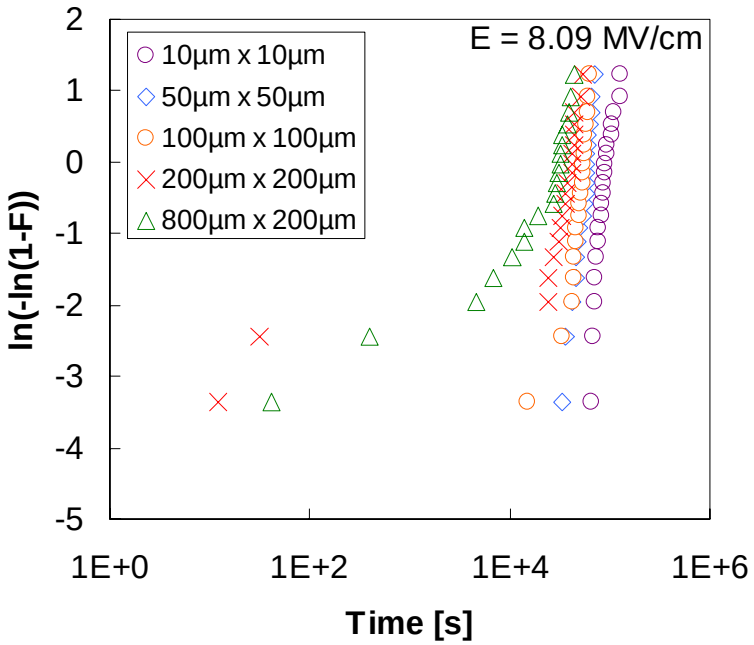


Fig.4.6 Weibull distributions measured on capacitors with various sizes at E = 8.09 MV/cm and T = 275 °C. Devices with larger area exhibit longer extrinsic tails.

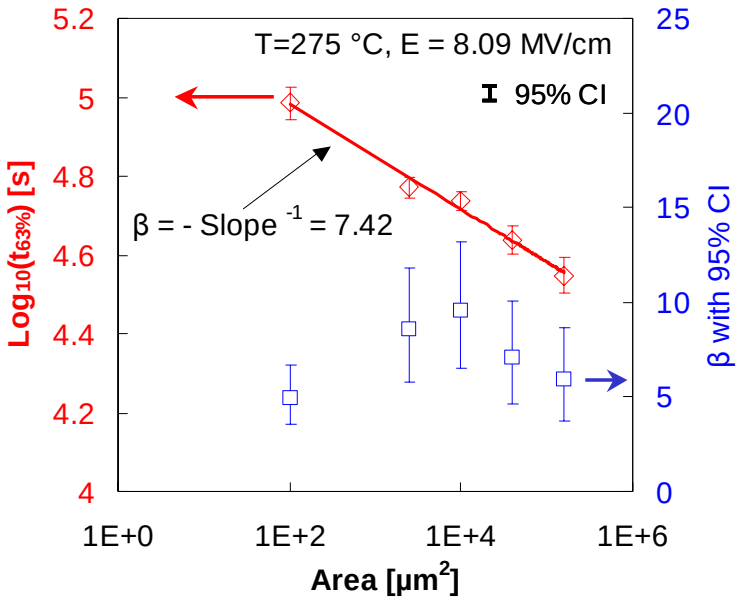


Fig.4.7 A more accurate method to extract Weibull slope β using the area scaling relationship of $t_{63\%}$. β with 95% confidence intervals fitted from Weibull distributions are also plotted on the secondary y-axis for comparison.

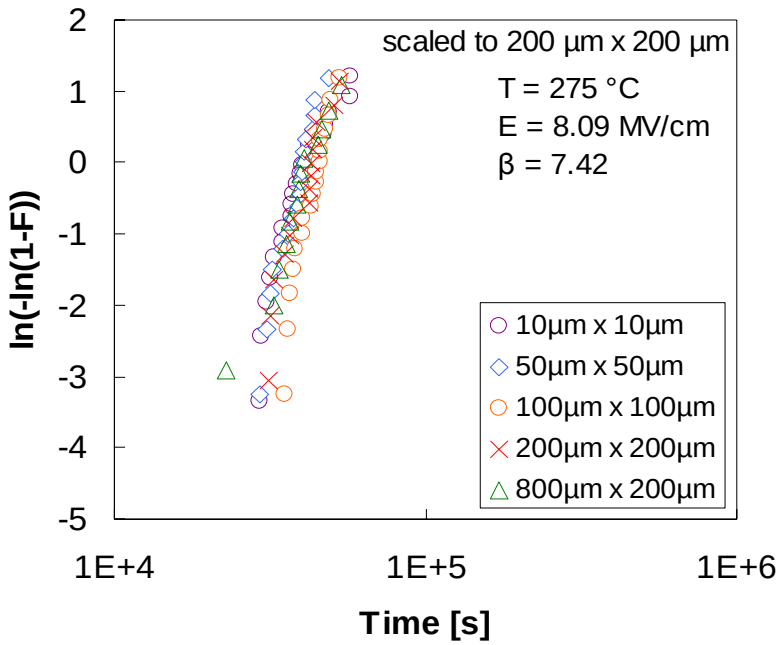


Fig.4.8 Weibull distributions of MOS capacitors of various sizes scaled to 200 μm × 200 μm using a Weibull slope of 7.42. The stress conditions are 275 °C and 8.09 MV/cm.

There is no model that can predict what value β should be for thick oxides with intrinsic quality. Therefore, while the more accurate β obtained above can be used to compare oxide quality relatively between two processes, it still cannot answer the question whether the oxide is intrinsic yet.

Here the area dependence of β is presented as a possible indicator that the good reliability results reported in this paper are still not indicative of intrinsic reliability and there is still room for improvement.

In Fig.4.7, the Weibull slope versus capacitor area is plotted on the secondary axis. Although the 95% confidence intervals are large, there is a trend that β peaks at the area of 100 μm × 100 μm and decreases as the area deviates from the peak point. This trend is not as expected if there is only one extrinsic failure mechanism involved in addition to the intrinsic oxide breakdown, in which case as oxide area shrinks, the chance of involving extrinsic defects should decrease and therefore β should increase for smaller areas. The observed trend does not agree with this expectation and suggests that there might be more than two breakdown mechanisms contributing to the failure distributions. In the case of three breakdown mechanisms, $t_{63\%}^{I} < t_{63\%}^{II} < t_{63\%}^{III}$, $t_{63\%}^{I}$ is related to the obvious extrinsic tail, $t_{63\%}^{III}$ is the characteristic time associate with the intrinsic failures and $t_{63\%}^{II}$ is related to another extrinsic failure mechanism in between. After the obvious extrinsic tail is removed, the Weibull distribution of capacitors with area of 800 μm × 200 μm still contains failures due to mechanism I. As area decreases, the portion of failures due to mechanism I becomes less and hence β increases. As the area further decreases, the intrinsic mechanism III comes into play and makes β smaller again. This

area dependence of β can also be seen by inspecting the Weibull distributions. Another set of area-dependent failure distributions stressed at 9.36 MV/cm and 275 °C is shown in Fig.4.9. As the area decreases from 800 μm × 200 μm to 100 μm × 100 μm, the Weibull distribution becomes steeper (i.e. β increases). And as the area decreases from 100 μm × 100 μm to 10 μm × 10 μm, the failure distributions show more bi-modal behaviors again. This trend is consistent with the above discussions of multiple failure mechanisms. This area dependence of β is observed on all of the three sets of area scaling data measured at different electric fields as shown in Fig.4.10. This repeatedly observed behavior might be an indication that the oxide quality has not reached the intrinsic regime yet, and with continued advances on oxidation processes, the reliability of SiO_2 on SiC can be further improved.

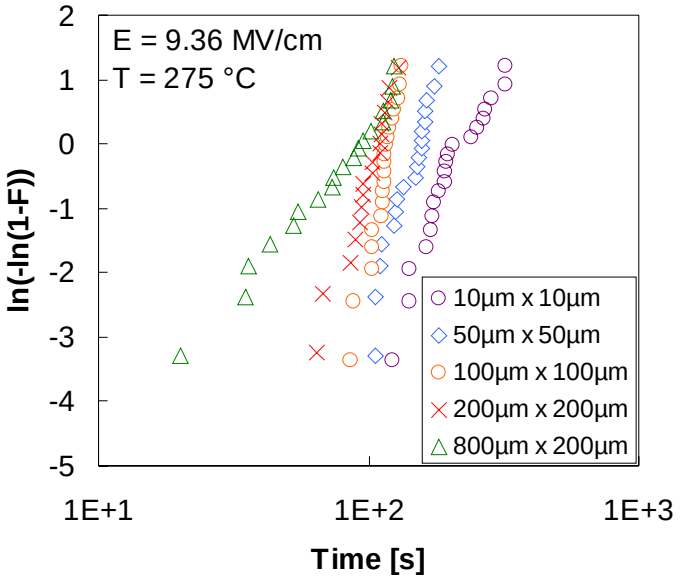


Fig.4.9 Weibull distributions of MOS capacitors with various sizes. The stress conditions are 275 °C and 9.36 MV/cm. As area deviates from 100 μm × 100 μm, the distributions show more bi-modal characteristics.

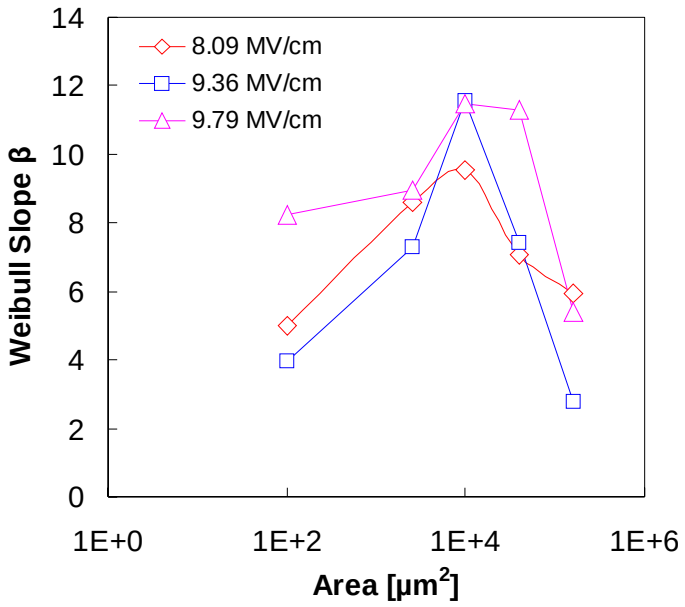


Fig.4.10 Area dependence of Weibull slope β at three different electric fields all show peaks at the area of 100 μm × 100 μm. This dependence is an indication that the oxide on SiC has not reached the intrinsic regime yet.

4.3.3 Kink effect

Due to the constraint of total measurement time in the TDDB tests, it is not practical to measure device lifetimes at very low electric fields. Therefore, in order to answer the question "Will the field acceleration factor change again at low electric fields?", it is of crucial importance to understand the breakdown mechanisms behind the change of field acceleration factor (also called "kink effect") around 8.5 MV/cm as shown in Fig.4.3. In this work, some experimental evidences are found that might indicate that the oxide breakdowns at high electric fields (> 8.5 MV/cm) are caused by impact ionization.

Leakage currents as a function of stress time stressed at 250 °C and different electric fields are shown in Fig.4.11. For electric fields higher than 8.5 MV/cm, the leakage current increases initially and then decreases, indicating hole trapping at the beginning

and followed by electron trapping. Whereas in the leakage current trace stressed at 8.5 MV/cm and below, the leakage current decreases monotonically, indicating no initial hole trapping. The electric field corresponding to this shape change in the leakage current is around 8.5 MV/cm, which is the electric field where the “kink” occurs as shown in Fig.4.3.

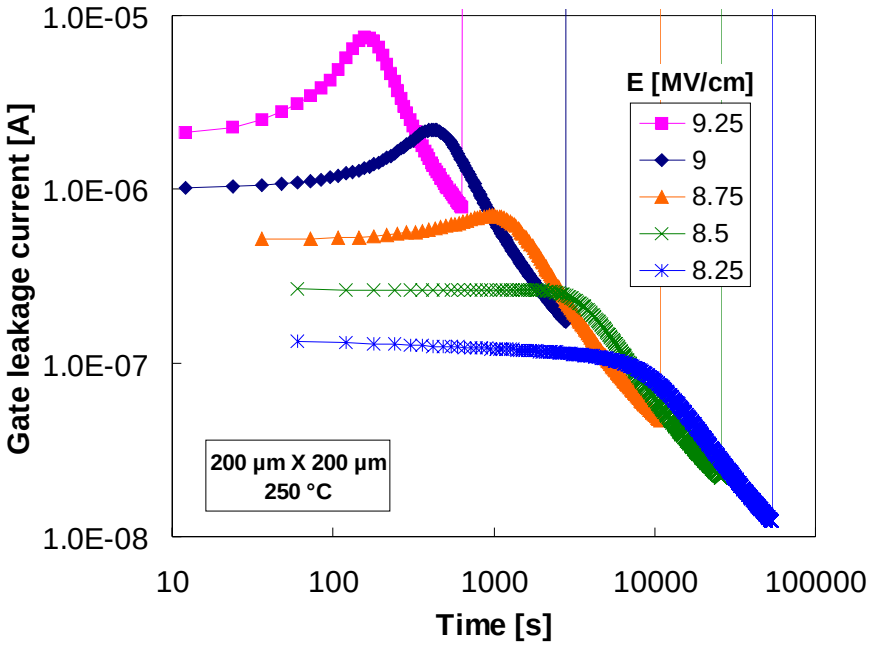


Fig.4.11 Leakage current versus stress time at different electric fields stressed at 250 °C. The shapes of the current traces are different for different stress electric fields.

Hole trapping is an indication of impact ionization. Electrons injected into the oxide by Fowler-Nordheim tunneling are subsequently heated up by the high electric field. Electrons in the high-energy tail of the distribution have enough energy to collide with the lattice and generate electron-hole pairs. Each of these impact ionizations leaves behind a slowly moving hole. Local potential in the oxide is distorted by the holes built up, which enhances the electric field and hence the tunneling current. This effect is schematically drawn in Fig.4.12.

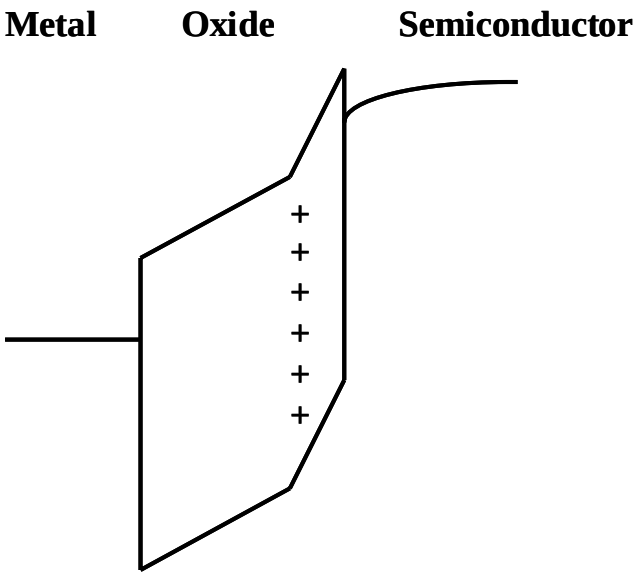


Fig.4.12 Schematic of impact ionization caused hole trapping that enhances the Fowler-Nordheim tunneling current.

At the same oxide electric field, electrons in thicker oxide have higher probability of gaining sufficient energy for impact ionization. Therefore, reliability study on devices with various oxide thicknesses may help to further understand this issue.

4.3.4 Activation Energy

Both the E model and 1/E model assume an Arrhenius temperature dependence in the form of $t_{BD} \propto \exp(E_a/kT)$, where E_a is the thermal activation energy required for oxide breakdown. These models also predict that E_a should be dependent on electric field. In the early studies of SiO_2 on Si, E_a was observed to decrease as a function of applied gate voltage [90-92]. However, not all the oxides exhibit such a voltage dependence, as discussed in [91, 92]. McPherson et al. also developed a model that shows the field-independent activation energy can be the result of two or more disturbed bonding states [93]. While many efforts have been spent on the characterizations of E_a in SiO_2/Si system,

only very few values of activation energy have been reported on SiO_2/SiC system. Senzaki et al. reported that the activation energies for Al gate and Poly-Si-gate thermal oxides to be 0.59-0.79 eV and 0.34-0.72 eV respectively [94].

Fig.4.13 shows the Arrhenius plots for the capacitors with area of 200 μm × 200 μm at the four temperatures investigated. It can be seen that the activation energy is around 0.9 eV for all of the electric fields in the range from 8.09 to 9.36 MV/cm. The activation energy does not exhibit an electric field dependence within the electric field range investigated.

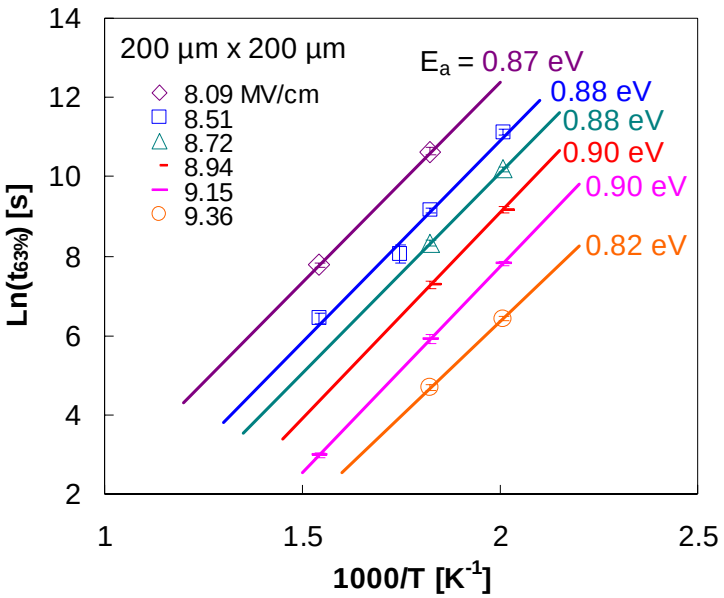


Fig.4.13 Arrhenius plots at various stress fields for capacitors with area of 200 μm × 200 μm. The activation energy does not exhibit dependence within the electric field range shown.

4.3.5 Oxide Reliability of DMOSFET

Studies of oxide reliability of DMOSFET have shown great improvements in recent years. The field-dependent characteristic lifetimes are plotted in Fig.4.14 for DMOSFETs developed in years 2006, 2007 and 2008. The reliability has been improved by two orders

of magnitude. $t_{63\%}$ measured at the same temperature on 200 μm × 200 μm capacitors are also plotted for comparison in Fig.4.14. It can be seen that the reliability of DMOSFET is getting closer to that of the capacitor. It should be noted that the active area of DMOSFET is 5.4×10^{-3} cm^{-2}, and the area of the capacitor is 4×10^{-4} cm^{-2}. If area scaling is performed, the two reliability curves should be even closer.

Weibull slopes extracted from failure distributions of DMOSFETs and capacitors are compared in Fig.4.15 with 95% confidence intervals indicated by the error bars. β in the DMOSFETs are significantly poorer than the capacitors. This can also be seen by inspecting the Weibull distributions shown in Fig.4.16 and Fig.4.17. The Weibull plots of DMOSFETs are more non-linear than capacitors, which is expected because more extrinsic defects might be caused by the extra processing steps necessary to form the structure of DMOSFET. Future work is necessary to minimize the extrinsic failures and improve the reliability of DMOSFETs.

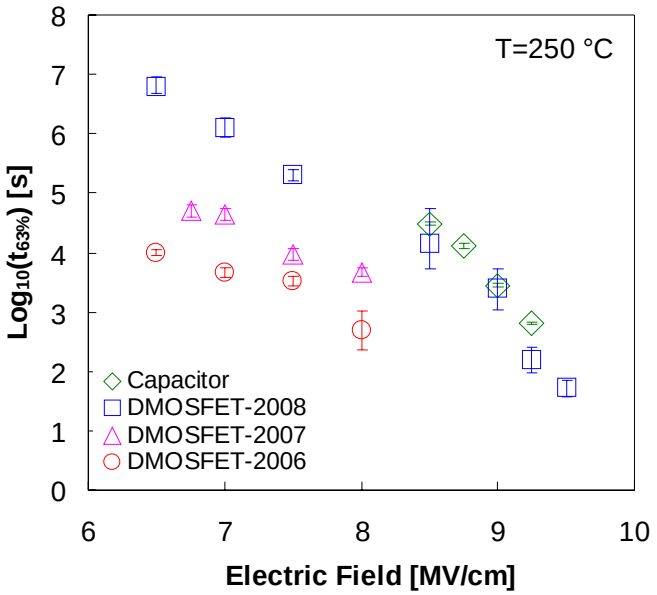


Fig.4.14 Electric-field acceleration of MOS capacitors and three generations of DMOSFETs measured at 250 °C. (Courtesy of GE Global Research)

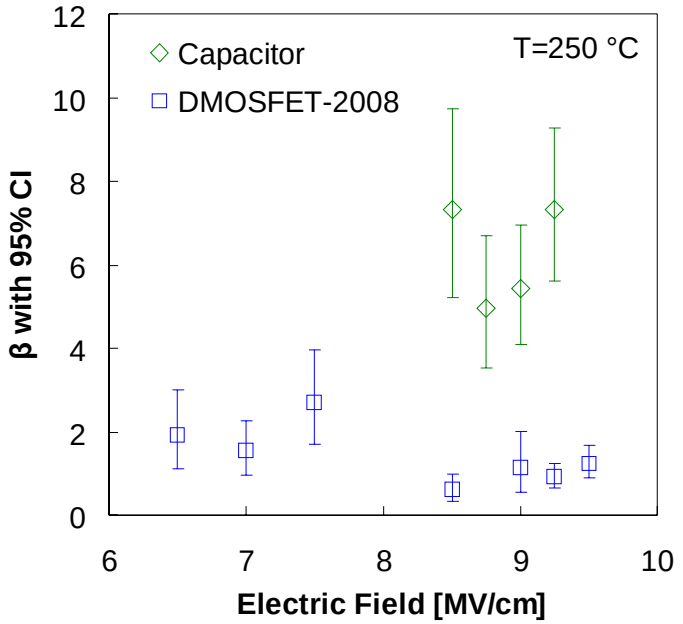


Fig.4.15 Weibull slopes extracted for MOS capacitors and DMOSFET with 95% confidence intervals.

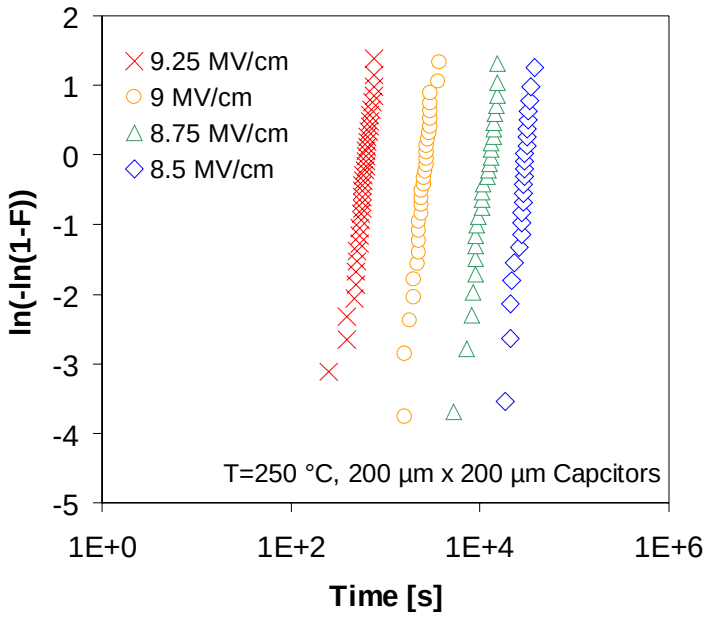


Fig.4.16 Weibull distributions as a function of electric fields measured on SiC MOS capacitors of size 200 µm × 200 µm at T = 250 °C.

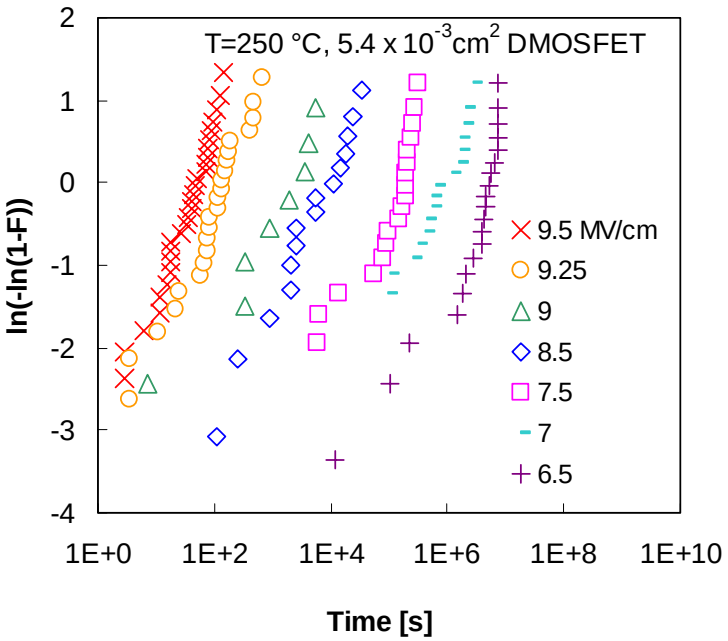


Fig.4.17 Weibull distributions as a function of electric fields measured on SiC DMOSFETs with active area of 5.4×10^{-3} cm^{-2} at T = 250 °C.

4.3.6 Examination of Early Prediction on Oxide Reliability

The observed excellent lifetimes clearly demonstrate that the widespread belief that silicon oxide on SiC will never be reliable at high temperatures is incorrect. Therefore, the arguments that lead to the misconception should be re-examined.

The main observation leading to the belief that silicon oxide cannot not be reliable on SiC is the early experimental data of oxide reliability as discussed in the introduction [41, 42]. However, with continuous advances in processing technologies, oxide lifetime on SiC has been improved steadily in the past 15 years. Fig.4.18 shows lifetime projections with the mean-time-to-failure measured on state-of-the-art MOS capacitors in years 1993, 2006 and 2008 with the same temperature stress of 350 °C. The projected lifetimes at use-condition (3 MV/cm) are 0.5 hours, 3 years and 200 years respectively. Our data measured at 375 °C in this work is also plotted for comparison. The observed good

reliability data is strong evidence that SiO_2 on SiC is reliable. Nothing fundamental is responsible for these improvements other than better processing technology. As mentioned above, even these recent good results are not yet the limit, and additional improvement can be expected.

The smaller conduction band offset compared to Si leads to the concern that oxide reliability on SiC is physically limited. While a smaller conduction band offset should indeed lead to shorter lifetime, the question is "By how much"? Singh et al. [38] projected a reduction by 1.5× based on the reduction of band offset. They further reasoned that since the electric field is kept below 4-5 MV/cm at a rated temperature of 125 °C for commercial Si nMOSFETs, one could expect that the electric field for the SiC system cannot exceed 3 MV/cm. It is not clear what the basis is for the 1.5× reduction prediction. For thick oxides, the intrinsic breakdown process is believed to be a feedback runaway process [95-97]. It depends on two factors: tunneling current density and impact ionization efficiency. Lower field leads to lower impact ionization efficiency. Even neglecting this factor, the field for the same tunneling current for the two barrier heights should be the basis for prediction. Fig.4.19 shows the FN tunneling current for the two barrier heights (assuming identical effective mass in the substrate). If the SiO_2/Si system has a breakdown field of 5 MV/cm, then the SiO_2/SiC system should have a breakdown field of ~ 4.1 MV/cm. If the effective mass and the impact ionization are taken into account, then the field should get even higher. It should also be noted that the 5 MV/cm specification for silicon is ultra conservative, set during the time the silicon industry was still learning to minimize extrinsic defects [98]. More modern data suggest that the silicon system can support higher fields [84, 99].

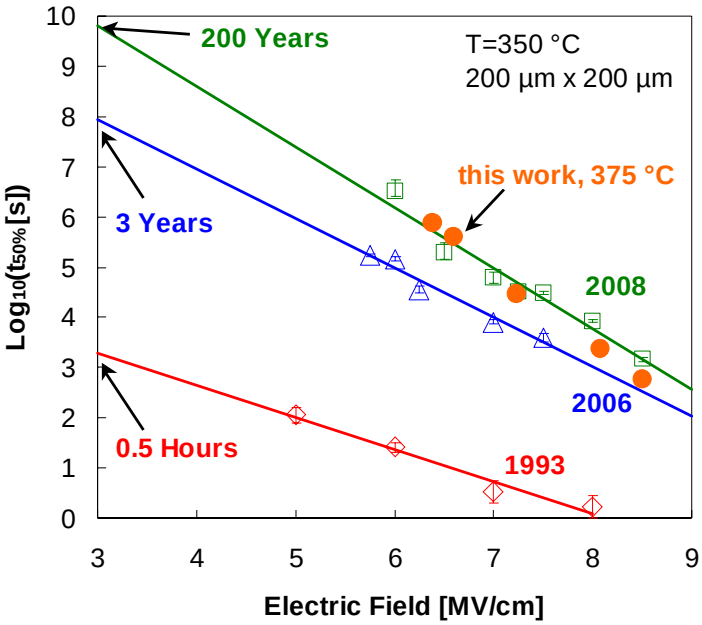


Fig.4.18 Improvements of oxide reliability on SiC over the past 15 years. These data are measured on 200 µm × 200 µm MOS capacitors at 350 °C. (Courtesy of GE Global Research)

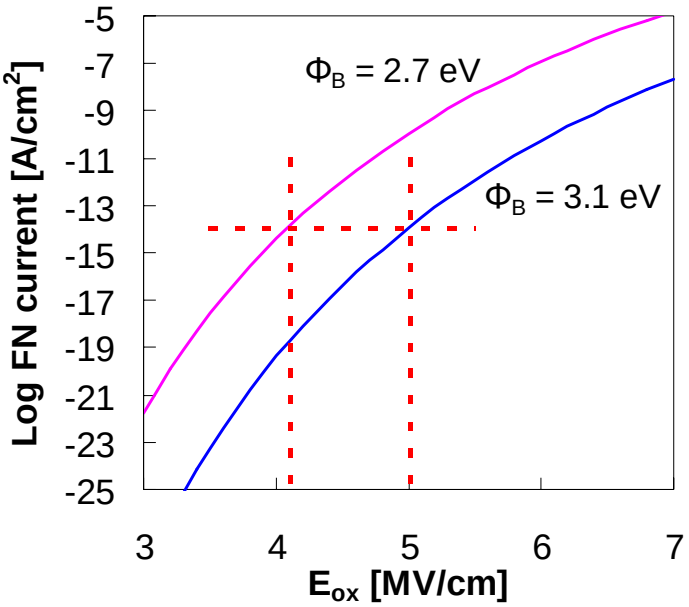


Fig.4.19 Theoretical Fowler-Nordheim tunneling current at Φ_B = 2.7 eV and 3.1 eV for SiC/SiO_2 and Si/SiO_2 systems respectively. $m_{SiC} = 0.37m_0$ and $m_{ox} = 0.42m_0$ are assumed in the calculations.

Considering the concern that the effective barrier height decreases significantly with increasing temperature as Agarwal et al. [39] and Waters et al. [40] reported, I-V characteristics are measured on capacitors at different temperatures and Φ_{eff} are extracted from the FN plot. As shown in Fig.4.20, the FN curves deviate from the expected linear behavior at both low fields and high fields. Therefore, Φ_{eff} varies by fitting different portion of the curve. The bending at high fields is caused by charge trapping. This is further illustrated in Fig.4.21 that two consecutive I-V sweeps on the same device are shown. The leakage current in the second sweep is larger than the initial sweep except at very high voltage. The interpretation is that during the initial sweep charges are trapped in the oxide when the field is high enough and the trapped charge increase the leakage current by modifying the tunneling barrier in the subsequent I-V measurements. The fact that the two curves merge at high voltage indicates that during the initial sweep, the I-V characteristic is already distorted by the trapped charge. The method of using the FN plot to extract Φ_{eff} assumes the leakage current measured is purely due to FN tunneling. This is not true in the SiC-based MOS system, in which substantial amount of oxide traps exist both at the interface and in the bulk. Trap-assisted tunneling as well as distorted electric fields in the oxide due to charge trapping all deviate the FN plot. Therefore, the Φ_{eff} extracted using this FN method is questionable.

Even if this questionable Φ_{eff} extraction method is employed by fitting the FN plot at moderate electric fields, which are less distorted by either charge trapping at high fields or system leakage at low fields, the effective barrier height does not change dramatically at high temperatures. The extracted Φ_{eff} values are 2.57 eV at room temperature and 2.36 eV at 200 °C with $\Delta\Phi_{eff}/\Delta T \sim 1.2$ meV/K, which is much smaller compared to the 2.6

meV/K [39] reported by Agarwal et al. and 3.0 meV/K [40] reported by Waters et al. This much smaller temperature dependence of Φ_{eff} may be the result of the significantly improved oxide quality compared to ten years ago as the amount of traps that distorts the FN tunneling have been reduced greatly.

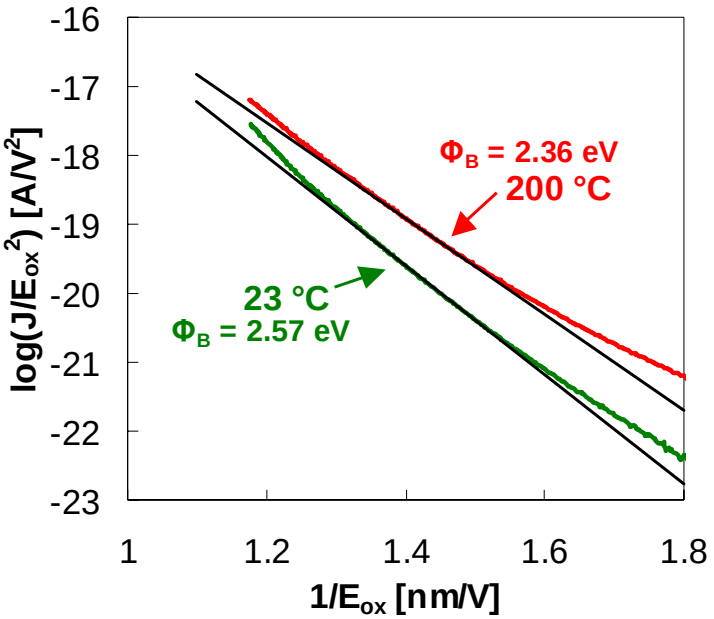


Fig.4.20 FN plots of gate leakage current measured at room temperature and 200 °C. Effective barrier heights are extracted from the middle section of the curves as it is less affected by charge trapping or system leakage.

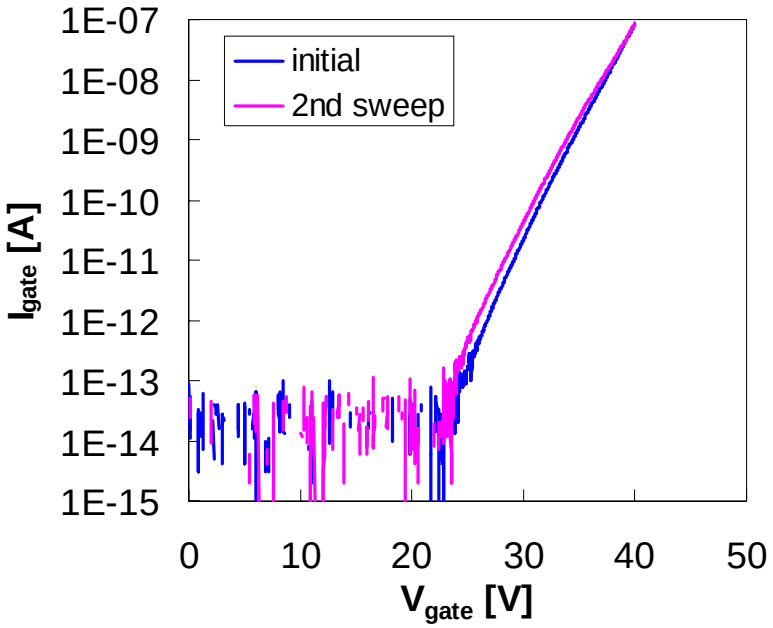


Fig.4.21 I-V characteristics measured on a MOS capacitor with two consecutive sweeps. The larger leakage current in the second sweep is due to charge trapping in the oxide.

4.4 Summary

The reliability of SiO_2 on 4H-SiC has been studied systematically at various stress temperatures and electric fields. Long-term stress as long as 7 months has been performed at 6 MV/cm and 300 °C and the results indicate that the high-field data can be extrapolated to lower field with no change in field-acceleration factor. Weibull slopes (β) with 95% confidence intervals are extracted from the failure distributions and used as an indicator of oxide quality. Area scaling is presented as a more accurate method to extract Weibull slope. Thermal activation energy has been calculated to be ~ 0.9 eV for all the electric fields investigated. There is no obvious electric field dependence in the field range explored.

The “kink effect” is discussed and some experimental evidence is presented indicating that the breakdown mechanism behind the change of field acceleration factor might be impact ionization. This further assures the concerns about possible change of field acceleration factor at use-conditions.

Since our reliability data contradicts the widely accepted belief that the oxide on SiC is fundamentally limited by its smaller conduction band offset compared to Si, a detailed discussion is provided to examine the arguments of the early predictions.

5 CONCLUSIONS

In this thesis work, several main challenges in the development of SiC power MOSFET are addressed from the following aspects.

For power MOSFETs that are required to block very high voltage (> 3 kV), the on-state resistance is dominated by the resistance of the lowly-doped drift region. As a majority carrier device, the specific-on resistance of SiC MOSFETs is intrinsically limited by the unipolar limit. Super-junction structure can break this theoretical limit by the charge compensation idea. In this work, simulations with various combinations of device parameters are performed to show the potential of this SiC-based super-junction structure for breaking the unipolar limit. A simple but accurate model is then developed for both the forward-conduction mode and reverse-blocking mode. Charge imbalance is also considered and included in the model.

For power MOSFETs that target for lower blocking voltage range (< 1 kV), the channel resistance becomes more dominant. In SiC MOSFET, low channel mobility is one of the most challenging problems. Accurate measurement of channel mobility is the prerequisite for further understanding of mobility degradation mechanisms and hence the enhancement of mobility. In this work, a fast wafer-level Hall-mobility measurement method has been demonstrated that does not require any wafer dicing, wire bonding, packaging nor the bulky, expensive regular Hall measurement system. This method is very simple and cost-effective. Device characterization and development are much more convenient by using this technique. With this method, further explorations of interactions

between interface traps and channel carriers as well as channel mobility degradation mechanisms become possible.

Oxide reliability is another big challenge to the development of SiC power MOSFET. It was believed for a long time that oxide on SiC could never be reliable. The reliability of SiO_2 on 4H-SiC has been studied systematically at various stress temperatures and electric fields. Long-term stress as long as 7 months has been performed at 6 MV/cm and 300 °C and the results indicate that the high-field data can be extrapolated to lower fields with no change in field-acceleration factor. Weibull slopes (β) with 95% confidence intervals are extracted from the failure distributions and used as an indicator of oxide quality. Area scaling is presented as a more accurate method to extract Weibull slope. Thermal activation energy has been calculated to be ~ 0.9 eV for all the electric fields investigated. There is no obvious electric field dependence in the field range explored. Since our reliability data contradicts the widely accepted belief that oxide on SiC is fundamentally limited by its smaller conduction band offset compared to Si, a detailed discussion is provided to examine the arguments of the early predictions.

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