A MONOLITHICALLY INTEGRATED POWER JFET AND JUNCTION BARRIER SCHOTTKY DIODE IN 4H SILICON CARBIDE

by

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ABSTRACT OF THE DISSERTATION

A Monolithically Integrated Power JFET and Junction Barrier Schottky Diode in 4H Silicon Carbide

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Efficiency of power management circuits depends significantly on their constituent switches and rectifiers. The demands of technology are increasingly running up against the intrinsic properties of Si based power devices. 4H-Silicon Carbide (SiC) has superior properties that make it attractive for high power applications. SiC rectifiers are already a competitive choice and SiC switches have also been commercialized recently. Junction Barrier Schottky (JBS) diodes, which combine the advantages of PN and Schottky, have higher Figure of Merit (FOM) as rectifiers. Among switches, a robust and mature process has been developed for Silicon Carbide Vertical Junction Field Effect Transistors (VJFETs), which currently gives it the highest unipolar FOM.

Switches are frequently combined with anti-parallel diodes in power circuits. This thesis describes the development of a SiC-based monolithically integrated power switch and diode. Monolithic integration increases reliability and efficiency, and reduces cost. Because of their superior properties and similarities in fabrication, we chose the SiC VJFET and JBS diode as the switch and rectifier. Detailed design,

fabrication and characterization of the integrated switch to block above 800 V and conduct current beyond 100 A/cm^2 is explained. In this process, the first physics-based 2-D compact model is developed for reverse leakage in a JBS diode as a function of design parameters. Since the gate-channel junctions of SiC VJFETs cannot be assumed to be abrupt, an existing analytical model for Si VJFETs is extended to account for graded gate-channel junctions. Using these analytical models, design rules are developed for the VJFET and JBS diode. Finite element simulations are used to find the best anode layout of the JBS diode and optimize electric field termination in the integrated device to ensure their capability to operate at high voltage. Finally, a spin-on glass based process is developed for filling the gate trenches of the VJFET to improve long-term robustness in extreme environments.

The integrated power switch developed in this thesis points to the attractions of monolithic integration in SiC power circuits. Analytical compact design equations derived here will facilitate faster and easier design of switches and rectifiers for desired circuit operation.

To my mother Smt. P. V. Vasanthi

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1. INTRODUCTION

1.1 Power Devices

As we grapple with burgeoning demand for energy, efficiency of power management is often identified as an area for continuous improvement. Electric power inevitably has to go through multiple transformation and management steps between its generation and end-use. In the early days, such systems worked on mechanical, hydraulic, magnetic and later vacuum tube principles. But with the advent of semiconductor electronics, it became cheaper and more efficient to use Silicon-based electronic devices to manage power and deliver it at the voltage, current and frequency required.

Losses in power devices are either static losses when they are in steady state or dynamic losses when they are switching between states. Majority carrier or unipolar devices like MOSFETs and Schottky diodes have negligible switching losses and are hence preferred in power circuits. The ideal device will be unipolar and have low on-resistance, low leakage current while off and high breakdown voltage. These are conflicting requirements because to have a low on-resistance (R_{on}), the drift region of the device should be thin and heavily doped. In that case though, slope of electric field v/s distance from junction in reverse bias shown in fig. 1 is high and the voltage that the device can block (V_B) before the maximum electric field reaches the critical value for onset of breakdown (E_c) is lower. This trade-off between the on-state and off-state static losses leads to a "unipolar limit" for the on-resistance of power devices, which can be expressed as

$$R_{on} \propto \frac{V_B^2}{\varepsilon \mu E_c^3} - - - (1)$$

μ is the mobility of majority carriers and ε the absolute permittivity of the material.

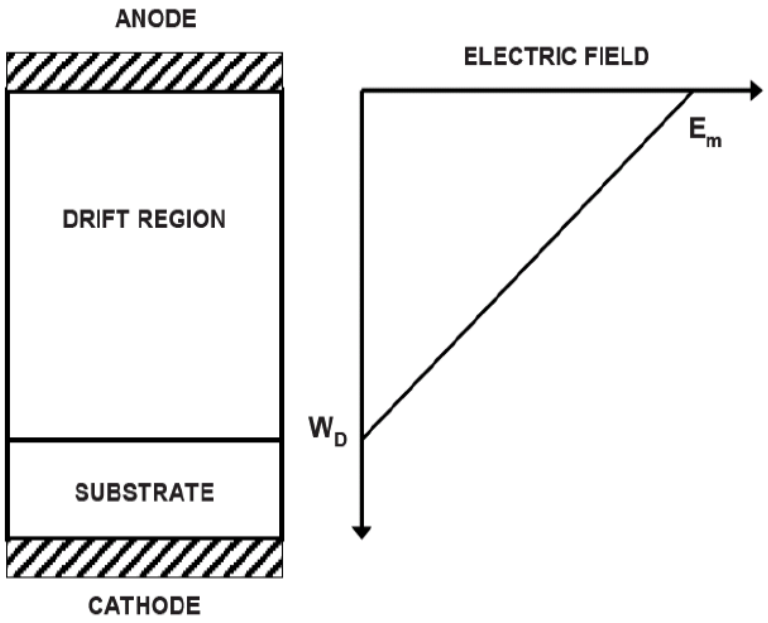

Figure 1 Electric field along the drift region of a semiconductor device [1]

Since R_{on} is proportional to the square of V_B, the on-state loss at high voltages increases prohibitively for unipolar devices. At a certain high voltage, the reduction in R_{on} due to conductivity modulation in bipolar devices outweighs the increased dynamic losses for many applications. So whereas the Si power MOSFET is the most popular power switch up to ~600V, the Si Insulated Gate Bipolar Transistor (IGBT), a bipolar device, is more popular at higher voltages.

To break the unipolar limit of Silicon, either the rate of increase of R_{on} with V_B or the material constants in (1) has to be changed. The former can be achieved by various "charge coupling" methods which utilize 2 and 3 dimensional variation of carrier concentration to make the electric field v/s x plot flat without reducing the drift layer concentration very much. One such technique has been implemented in "superjunction" MOSFETs [2] which have increased the range of useful operation of Si MOSFETs above 800 V. At the basic level, this involves forming p and n columns in the drift layer such that when the charges are balanced and the columns completely

depleted, electric field will be uniform along x. Using this technique, R_{on} can at best be made proportional to V_B rather than V_B^2 [1]. This is impressive but only an incremental improvement over traditional technology. However, by using materials for which the material constants in (1) are much higher, R_{on} can be reduced by orders of magnitude for the same V_B.

1.2 4H-SiC for Power Devices

Many properties of semiconductors relevant to power device operation are given in Table 1. The outstanding properties of 4H-SiC include wide band-gap, high electron saturation velocity and high thermal conductivity [3]. They make 4H-SiC a remarkable material for high power, high temperature and high frequency devices.

Wide band-gap allows 4H-SiC devices to operate at much higher temperatures (up to 600C) compared to Silicon devices without undue leakage current. Wide band-gap also endows 4H-SiC with a critical electric field of 2-3 MV/cm (depending on doping and temperature), which is an order of magnitude higher than that of Silicon. 4H-SiC devices exceed the Si unipolar limit by more than two orders of magnitude, which allow 4H-SiC devices to be designed with a thinner drift layer and hence lower on-resistance than Si for the same blocking voltage requirement. This also allows a single 4H-SiC device to operate beyond the 11 kV range.

High thermal conductivity and inertness also make SiC suitable for applications at high temperature. The power density is higher and cooling demand much lower in SiC, which saves installation cost as well as costs of weight and bulk of the system. This is especially attractive in applications like hybrid cars where weight loss very clearly translates to improved efficiency.

Material	E_g eV	n_i cm^{-3}	ε_r	μ_n $cm^2/V \cdot s$	E_c MV/cm	v_{sat} $10^7 cm/s$	λ W/cm·K	Direct Indirect
Si	1.1	1.5×10^{10}	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4×10^{13}	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8×10^{6}	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7×10^{-1}	11.1	350	1.3	1.4	0.8	I
InN	1.86	$\sim10^{3}$	9.6	3000	1.0	2.5	-	D
3C-GaN	3.27	8×10^{-9} *	9.9	1000	1	2.5	1.3 *	D
2H-GaN	3.39	1.9×10^{-10}	9.0	900	3.3	2.5	1.3	D
3C-SiC	2.2	6.9	9.6	900	1.2	2.0	4.5	I
4H-SiC	3.26	8.2×10^{-9}	10	720[a]	2.0	2.0	4.5	I
				650[c]				
6H-SiC	3.0	2.3×10^{-6}	9.7	370[a]	2.4	2.0	4.5	I
				50[c]				
Diamond	5.45	1.6×10^{-27}	5.5	1900	5.6	2.7	20	I
BN	6.0	1.5×10^{-31}	7.1	5	10	1.0 *	13	I
AlN	6.1	$\sim10^{-31}$	8.7	1100	11.7	1.8	2.5	D

Table 1 Properties of semiconductors for power device applications

High electron saturation velocity allows 4H-SiC devices to be operated at higher current density and frequency when compared to Silicon devices. The applications of 4H-SiC power electronics could lead to lower energy loss and weight of power electronic components. In addition, higher chemical inertness and radiation resistance makes SiC devices suitable for harsh environments like nuclear power systems or outer space.

Other wide band-gap semiconductors which match or exceed the properties of SiC for power applications are GaN and diamond. However, SiC has many advantages over them which include its high compatibility with established Si processing technology, mature substrate and epitaxial growth technology which is already being commercialized and its exclusive (among wide band-gap semiconductors) property of growing natural oxide (SiO_2) on the surface. GaN grown on Si or SiC substrates is an attractive alternative for lateral devices. However, lateral devices have much higher on-resistance than vertical devices, especially at higher voltages. So, while GaN devices are making inroads in high frequency (AlGaN/GaN

High Electron Mobility Transistors (HEMTs)) and low voltage (< 600V) applications, they will not be as competitive at higher voltages until the quality of GaN substrates improves.

Commercially, micropipe defect free 4-inch 4H-SiC wafers with customized epi-layers are provided by many companies, like Cree, Dow Corning and II-VI. 4H-SiC power Schottky barrier diodes and Junction-Barrier Schottky (JBS) diodes are also commercially available up to 1700V from Infineon technologies, Cree etc 4H-SiC JFET is available from SemiSouth, United Silicon Carbide etc and Cree recently commercialized the SiC MOSFET. SiC power switches are nearing a tipping point and is widely predicted to take-off as a serious challenger to the dominance of Si-based devices in power electronics.

1.3 SiC VJFET as Power Switch

The most important characteristics of a good power switch are- high blocking voltage, low specific on-resistance with a small positive temperature coefficient to facilitate paralleling, high current gain and high switching speed. Bipolar devices, with conductivity modulation, are capable of very low on-resistance but they are not able to achieve high switching speed. Unipolar FETs on the other hand, are majority carrier devices which switch much faster and have high current gain. Among SiC unipolar FETs, MOSFETs will ideally be better since they have very high current gain. There has been great progress in power SiC MOSFETs [4, 5]**.** However, the reliability of the gate oxide of SiC MOSFETs under high electric field is still a major concern, which has led to many convoluted designs [6] being proposed that shield the gate oxide from high field but are difficult to manufacture**.** Other problems include poor temperature stability of the gate threshold voltage in the SiC MOSFET and low mobility in the enhancement channel which increases on-resistance. There is a

significant research effort underway to address these issues with the SiC MOSFET [7]. Meanwhile, SiC JFETs are much more reliable and capable of high voltage and current switching with lower power loss. A comparison between the best reported power switches in the 1000-2000 V range is shown in table 2. The SiC VJFET has more than an order of magnitude lower $R_{sp.on}$ compared to charge compensated Si MOSFETs and under current technology performs better than SiC MOSFETs.

Device	Blocking (V)	$R_{sp.on}$ ($m\Omega.cm^2$)
SiC VJFET [8]	1900	2.8
SiC MOSFET [9]	1500	3.7
Si Superjunction MOSFET [10]	1100	54

Table 2 Performance of best reported power switches

With dedicated high temperature packages, 4H-SiC JFETs have been characterized at 450 °C [11] and have demonstrated life of at least 500 hours at 500 °C [12]. This enables SiC JFET switching circuits to operate over extremely wide temperature ranges. A DC-DC converter built with 4H-SiC JFETs and 4H-SiC Schottky diodes was tested at ambient temperature up to 400 °C [13] and 4H-SiC JFET switching experiments down to 30K have been reported [14].

JFETs can be designed, in terms of device structure, to be lateral (source, gate and drain terminals on the front side of the wafer) or vertical (source and gate terminals on the front side and drain terminal on the back side of the wafer). The lateral JFET is suitable for integrated circuits [15] but it is the VJFET that allows higher cell packing density and thus lower on-resistance. Hence it is the structure of choice for a power switch unless it is otherwise necessary that all three terminals are on the front side of the wafer.

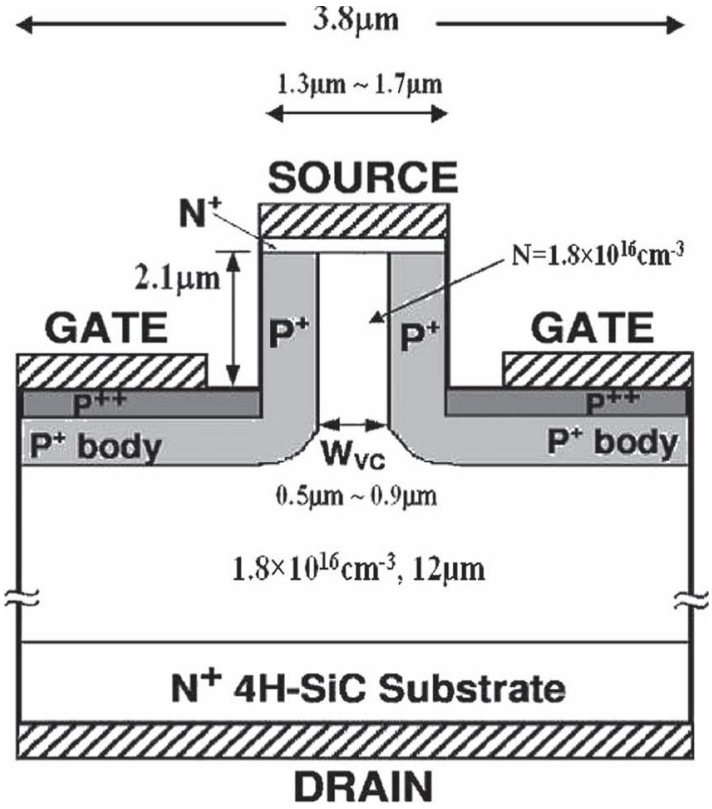

Figure 2 Cross-section of a SiC VJFET [16]

Cross-sectional view of a SiC Trenched and Implanted VJFET (TI-VJFET) is shown in fig. 2. SiC VJFETs need oppositely doped gate and source, which can be fabricated either with epitaxial re-growth or with ion implantation. Epitaxial re-growth in the middle of device fabrication is not desirable since it increases manufacturing costs. So, ion-implantation is preferred and robust processes for tilted ion implantation to form the vertical gate and channel in VJFETs have been developed [17]. Early SiC-VJFETs were developed with a combined vertical and lateral channel but the technology soon improved to realize a purely vertical VJFET, which provides lower on-resistance [16].

SiC VJFETs can be designed either to be normally-on (depletion mode; conducting high drain current at 0V gate bias) or normally-off (enhancement mode; blocking high drain-to-source voltage at 0V gate bias). Normally-on structures are always unipolar and can conduct higher current and provide lower specific on-

resistance than otherwise similar normally-off devices due to the wider channel opening. However, the normally-off structure is preferred for practical applications because it is fail-safe. The normally-off VJFET will not be short-circuited simply because the gate-drive fails. Normally-off devices can also be designed to have low on-resistance under unipolar operation [8].

1.4 SiC JBS Diode as Rectifier

The best power diode is the one that approaches the ideal of an open circuit (high blocking voltage) in one direction, a short circuit (low on-resistance and forward voltage drop) in the other and fast low-energy switching between the two states. The Schottky diode, where current is carried only by electrons (unipolar), is able to switch between the on and off states very fast. With the right choice of metal for the Schottky contact, the Schottky barrier can also be lowered enough to reduce the voltage drop in the on-state. However, the leakage current increases significantly with reverse voltage and for many applications it will be intolerably high well before the breakdown voltage. The 4H-SiC PN diode has much lower leakage current until breakdown but, the forward voltage drop is high and since it is a bipolar device, the switching speed is constrained by minority carrier storage in on-state.

The JBS diode was proposed [18] to combine the good features of both PN and Schottky diodes. As shown in fig. 3, it has closely spaced PN and Schottky junctions such that under forward bias, most of the current is carried across the Schottky junction which has a lower voltage drop and under reverse bias, the depletion regions from the PN junctions widen to cover the Schottky junction and shield it from high electric field and the consequent high leakage current. Although proposed initially for Silicon, this concept is even more suited to SiC where the forward voltage drop of PN diodes is higher and reverse leakage current lower. Many SiC JBS diodes have been

reported [19, 20] over the years and it has now been commercialized in Infineon's second generation SiC Schottky diodes [21].

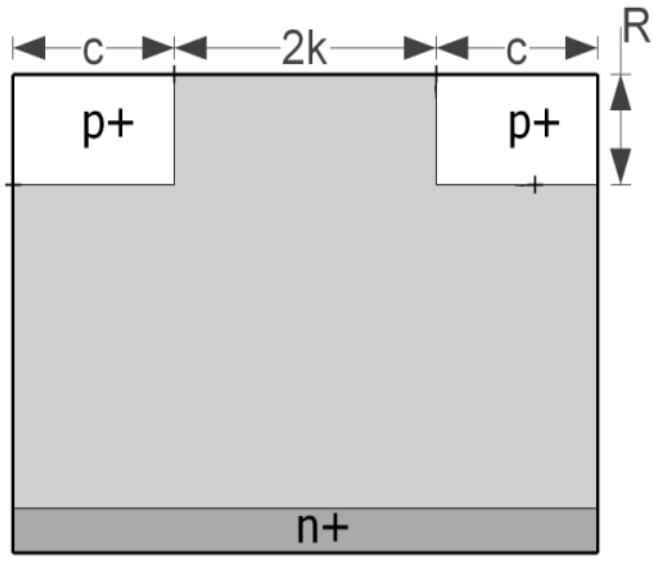

Figure 3 Cross-section of a JBS diode

1.5 Monolithic Integration of Switch and Diode

Power semiconductors are used to manage power delivery to many types of loads, most of which operate with current and voltage out of phase. In particular, the induction motor draws current at a significant lag compared to voltage because of its high inductance. When the switch serving such a load is suddenly turned off, the current only falls gradually. Since this switch itself is then open, a parallel path needs to be provided such that the current can loop through the load and this path. This path needs to be uni-directional since it should not conduct any forward current when the switch is finally in the off-state. So, a diode is connected anti-parallel to the power switch, called the flyback diode or freewheeling diode, in most power circuits like the 3-phase inverter shown in fig. 4.

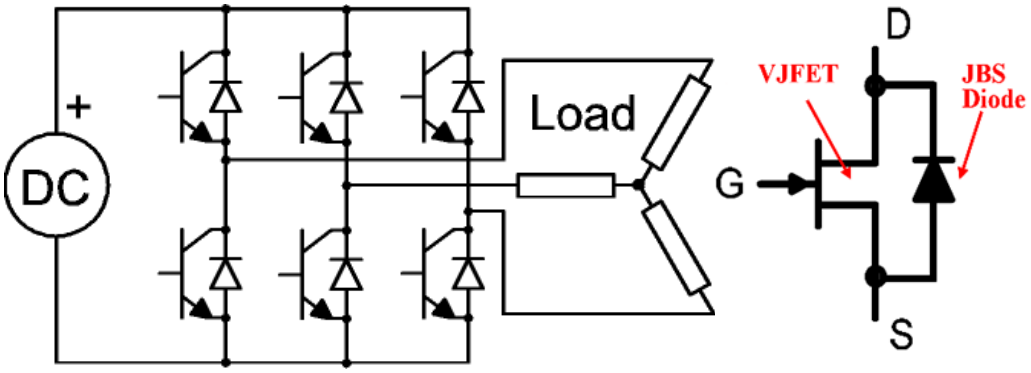

Figure 4 3-phase inverter, a typical power circuit with switch and anti-parallel diode

Another advantage of the switch-antiparallel diode pair is in "synchronous rectification". In this scheme, the switch is turned on when the diode is conducting and turned off when it is blocking such that it can add to the diode's forward current and reduce on-state loss.

The common combination of the power switch and anti-parallel diode has prompted many manufacturers to provide such integrated chips [22]. Such modules reduce chip area and make it easier for manufacturers to parallel smaller area higher yield devices for a particular current rating rather than using higher area devices. To reduce component count, circuit parasitics, cost & chip size and to improve reliability, it is desirable to integrate the power switch and anti-parallel diode monolithically. Such a monolithically integrated power SiC BJT and diode has been reported [23]. Methods for monolithic integration of the SiC VJFET and diode have also been patented [24] but such devices have not yet been demonstrated.

1.6 Field-Termination in Power Devices

Power devices operate at high voltages in the blocking mode. Along the direction of current transport, the space-charge region drops this voltage such that the electric field decreases linearly away from the junction. Under this 1-D

approximation, iso-electric field contours are parallel to the junction. But since a power device is of finite size, edges of the device are formed by cleaving the substrate. If this irregular surface were to be exposed to high electric field, voltage will not be dropped smoothly across the epitaxial layer. So, while the back side (non-junction) contact of a discrete power device covers the entire face, front side contacts cover a smaller area outside which the potential rises to that at the backside. Hence, the high voltage at the junction also has to be dropped across the surface of the device. If no special "edge-termination" schemes are used, this voltage drops abruptly at the edge, causing a high electric field which leads to device breakdown well below the parallel plane breakdown limit. So, various electric field termination schemes have been developed to spread the lateral electric field at the edge of the device over a wide enough region such that lateral breakdown voltage approaches the parallel-plane breakdown voltage [1].

Edge-termination schemes can generally be divided into two types- charge-sensitive and dimension-sensitive. Charge-sensitive edge termination schemes extend the lateral junction using an area with just the right number of implanted carriers at avalanche, the most popular of which is Junction Termination Extension (JTE)[25]. JTE is very sensitive to the implant dose. Dimension-sensitive schemes like implanted field rings [26] or metal rings create multiple PN junctions such that potential is equalized around the rings and gradually dropped from the anode to the edge. Guard ring termination is very sensitive to the width and spacing of the rings. However, it is particularly advantageous for SiC VJFETs and JBS diodes since those devices already use high dose p+ implantation.

When multiple power devices are monolithically integrated, field termination is required not only at the edges, but also between them. For example, when the VJFET

and anti-parallel diode are integrated, the gate of the VJFET has to be isolated from the anode of the diode with field termination structures. The design considerations of such inter-device field termination are different from that of edge-field termination and need to be optimized for each particular case, one example of which will be provided in this thesis.

1.7 **Outline of Ph. D. Thesis**

This thesis aims to advance the field of power devices by designing and demonstrating a monolithically integrated SiC based switch and anti-parallel diode for power electronic applications. In pursuit of that central objective, this work develops

1. The first 2-D compact model for reverse leakage current in high voltage JBS diodes which completes the analytical theory of the JBS diode.
2. A new 2-D analytical model for forward blocking performance of a SiC VJFET with realistic gate-channel junction by extending previous such models for abrupt gate-channel junction.
3. Closed form design equations for the design parameters of the SiC VJFET and JBS diode based on the analytical models presented above.
4. Design of a SiC VJFET with a monolithically integrated JBS diode without adding any steps to the VJFET fabrication process.
5. Design of masks and cleanroom fabrication of the integrated switch to block high voltage, handle high current and exhibit expected “third quadrant” operation as well as synchronous rectification.
6. Static, dynamic and temperature characterization of the fabricated device and analysis of the effects of monolithic integration on electrical characteristics.
7. Development of a novel spin-on glass based process for filling VJFET trenches and demonstration of operation of such a VJFET.

These steps in pursuit of the thesis objective involve original contributions to the current state of the art of power devices and will be detailed in the subsequent chapters of this work.

2 ANALYTICAL MODELING OF VJFET AND JBS DIODE

The advantages of monolithic integration of a 4H-SiC power switch and anti-parallel diode were elaborated in section 1.5. In section 1.3, it was seen that the best developed power switch technology is that of the 4H-SiC VJFET. In section 1.4, the advantages of the SiC JBS diode have been explained. 4H-SiC VJFET and JBS diode are uniquely suited for monolithic integration as a power electronic building block, not only because of their superior properties as power switch and power diode, but also because they share many fabrication steps and the integrated device can be fabricated without any additional process steps from that of the VJFET.

To design optimized power switches and diodes, it is desirable to have relationships between design parameters and electrical characteristics. While finite-element Technology Computer Aided Design (TCAD) simulations are more accurate, they only yield results for particular design parameters and not a continuous relationship showing trends in performance based on device parameters. Analytical continuous models can be developed empirically from TCAD simulations but their validity is doubtful beyond the contours of the specific simulation data from which they were built. Analytical models derived from fundamental laws of physics are inherently more reliable and easier to use within the limits of the assumptions made in their derivation. This chapter develops a new 2-D analytical model for the JBS diode and extends an existing 2-D analytical model for SiC VJFETs.

2.1 Analytical Modeling of JBS Diode

A 1-D analytical model, which provided closed form equations for forward and reverse I-V curves [18] was developed for low voltage Silicon JBS diodes in the

1980s, but the following assumptions made there do not hold at high reverse voltages and high electric fields that are found in wide band-gap devices.

1. Rise of electric field at the Schottky contact was assumed to be independent of the surrounding P-N junctions before pinch-off, where pinch-off is calculated by one-dimensional analysis in the Schottky channel. But electric field at the Schottky contact in a JBS diode actually falls behind that of the corresponding Schottky diode well before such a pinch off point as the effect of P-N junctions increases gradually.
2. After pinch-off, electric field at the Schottky contact was assumed to remain constant as reverse voltage increases, in effect assuming that the entire rise in reverse voltage is absorbed by the potential barrier forming in the channel. But from simulations, it is obvious that electric field at the contact continues to rise smoothly, apparently under the same dynamics as before pinch-off.

For Silicon diodes, the assumptions above, especially 2, don't introduce much error because electric field under reverse bias remains low enough that current conduction is mainly due to thermionic emission which is not very sensitive to the electric field. But wide band-gap diodes, where the avalanche limit is higher, can sustain higher electric fields at which tunneling through the barrier gives much higher current than thermionic emission over it. Tunneling is very sensitive to electric field at the Schottky contact and hence assuming the electric field to be constant post pinch-off leads to unacceptable error. [27] proposes a model that works for high voltage JBS diodes, but it relies on curve-fittings of simulation data rather than physical considerations to arrive at the important relationship between voltage and maximum electric field under reverse bias. That model also has to be re-built as doping of the epitaxial layer changes and it fails to include the effect of punch-through of the drift

layer at high voltages. [28] proposes an analytical model but it ignores punch-through, restricts implantation straggle to a circular profile and assumes the depletion region to have circular symmetry with respect to the P-N junction. This ignores the effect of the Schottky junction on the ionized donors and assumes the electric field to be influenced only by surrounding P-N junctions like in a guard-ring field termination region.

In this work, we develop for the first time a fully analytical model in reverse bias for a high voltage punch-through JBS diode leading to a closed form I-V relationship and validate these design equations using simulations and experimental data from SiC diodes.

2.1.1 Notation

(x, y)- Co-ordinates with reference to origin at the center of the Schottky region with x into the anode surface and y perpendicular to P-N and Schottky stripes.

2k- Width of Schottky region.

b- Distance from anode at which the variation of potential in a JBS diode can be approximated to be one-dimensional.

Φ- Electrostatic potential with reference to zero at the origin.

Φ_p- Poisson component of the electrostatic potential Φ.

Φ_l- Laplace component of the electrostatic potential Φ.

ρ- Local space charge density.

ε- Permittivity of the semiconductor medium.

R- Depth of ion implantation.

$k_{0\text{-}3}$- Integration constants in the solution of Poisson equation.

N_d- Ionized donor concentration in the epitaxial (drift) layer.

V_b- Potential at (b,0).

W- Thickness of the depletion region when the drift layer has not been punched through.

W_d- Thickness of the drift layer.

E_m- Electric field at the junction of a 1-D diode without punch through.

E_{mp}- Electric field at the junction of a 1-D diode after punch through.

E_p- Electric field in a diode after punch through.

V_R- Reverse voltage applied to a JBS diode.

$V_{R'}$- Reverse voltage applied to a Schottky diode at which it has the same V_b as the corresponding JBS diode at reverse voltage V_R.

E_{mps}- Electric field at the junction of a Schottky diode after punch through.

E_{mpj}- Electric field at the junction of a JBS diode after punch through.

(x',y')- Point on the boundary of the P-N junction.

J_{Sch}- Current density over the metal-semiconductor junction due to thermionic emission.

J_T- Current density through the metal-semiconductor junction due to tunneling.

A*- Effective Richardson constant.

T- Temperature in ºK.

q- Charge of electron.

Φ_B- Schottky barrier height.

k- Boltzmann constant.

m_0- Rest mass of electron.

m*- Effective mass of electron in the semiconductor.

$\hbar$ - Planck's constant.

h- Length of a Schottky finger in a striped JBS diode.

I_s- Current carried by one Schottky finger.

J_R- Reverse current density in the JBS diode.

P- Pitch of the interdigitated stripes of P-N and Schottky regions in the JBS diode.

2k'- Width of a Schottky region such that uniform thermionic emission current density across it will yield the same total current as in a JBS diode with the same thermionic emission current density at the center of its Schottky region.

2k"- Width of a Schottky region such that uniform tunneling current density across it will yield the same total current as in a JBS diode with the same tunneling current density at the center of its Schottky region.

α_R- Proportional Schottky area in a JBS diode with interdigitated stripes of P-N and Schottky regions.

α_O- Proportional Schottky area in a JBS diode with honeycomb layout of P-N and Schottky regions with Schottky region outside the hexagon.

c- Ratio of the half-widths of P-N and Schottky regions in a JBS diode with a layout of interdigitated stripes.

m- Distance from center to edge of the hexagonal patterns in a JBS diode with honeycomb layout.

2n- Width of the streets between hexagonal patterns in a JBS diode with honeycomb layout.

d- Ratio of the minimum half-widths of P-N and Schottky regions in a JBS diode with honeycomb layout having Schottky region outside the hexagon.

2.1.2 Reverse Voltage and Electric Field

In a JBS diode under reverse bias, almost all the current conduction takes place through the Schottky junction. Under the high electric field that SiC JBS diodes operate at, thermionic emission current across the Schottky barrier, which by itself is

of a similar order of magnitude as the reverse current across a P-N junction, is enhanced due to image-force induced lowering of the Schottky barrier and quantum-mechanical tunneling, both of which are many orders of magnitude greater than it. So, under reverse bias, current carried across the Schottky junction is significantly larger than that across the P-N junction and hence the error resulting from restricting the analysis to the current flowing across only the Schottky barrier is miniscule. To find the current density in a JBS diode, we find the electric field at the Schottky barrier as a function of the reverse voltage by solving Maxwell's electrostatic equation (Poisson equation) and then relate this electric field to the current. The former approach, by splitting the 2-D Poisson equation, is similar to published analytical solutions of Silicon power FETs and SITs [29] , whereas the latter is based on attempts to form closed-form solutions to SiC Schottky diodes [27, 30].

In cross-section, width of the un-implanted region of the anode is 2k and depth of implantation is R. Electric field at the Schottky contact is expected to be highest at the center of the un-implanted region since it is farthest from the shielding P-N junctions. To find the electric field at the contact, it is sufficient to solve the 2-D Poisson equation in a rectangular region which stretches across the Schottky junction and from the anode to a distance b away, as shown in fig. 5. "b" is the distance from the anode till which the P-N junctions will affect potential distribution. At distances greater than b from the anode, the JBS diode is assumed to have a 1-D potential variation quite like a Schottky diode. Considering the anode to be the zero-potential reference, Dirchlet boundary conditions [31] for voltage in the rectangular domain are zero at the anode, V_p (a function of the cathode voltage) at x=b and on the sides, a voltage which varies with distance from anode.

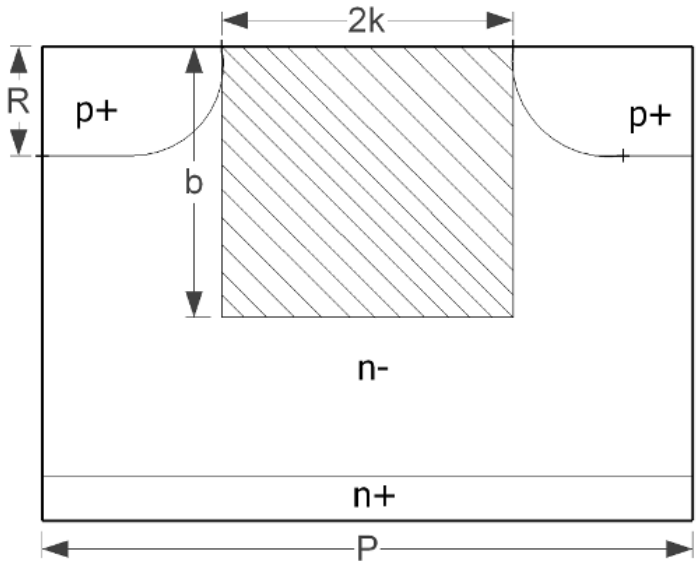

Figure 5 Cross-sectional views of a planar JBS diode

The Poisson equation to be solved is

$$\nabla^2 \emptyset(x,y) = \frac{-\rho(x,y)}{\varepsilon} - - - (2)$$

Numerical solution to this equation using the DESSIS simulator in Synopsys-TCAD Sentaurus [32] yields Φ(x, y) as shown on the vertical axis in fig. 6. In reverse bias, potential under the Schottky junction is always greater than that under the P-N junction for the same value of x. But as x increases, they converge until at x= b they are nearly equal. To solve the 2-D Poisson equation analytically, it can be split into a 1-D Poisson equation along x- axis and a 2-D Laplace equation [29].

$$\emptyset(x,y) = \emptyset_p(x) + \emptyset_l(x,y) - - - (3)$$

Such that

$$\nabla^2 \emptyset_p = \frac{d^2 \emptyset_p}{dx^2} = \frac{-\rho}{\varepsilon} - - - (4)$$

and

$$\nabla^2 \emptyset_l = 0 - - - (5)$$

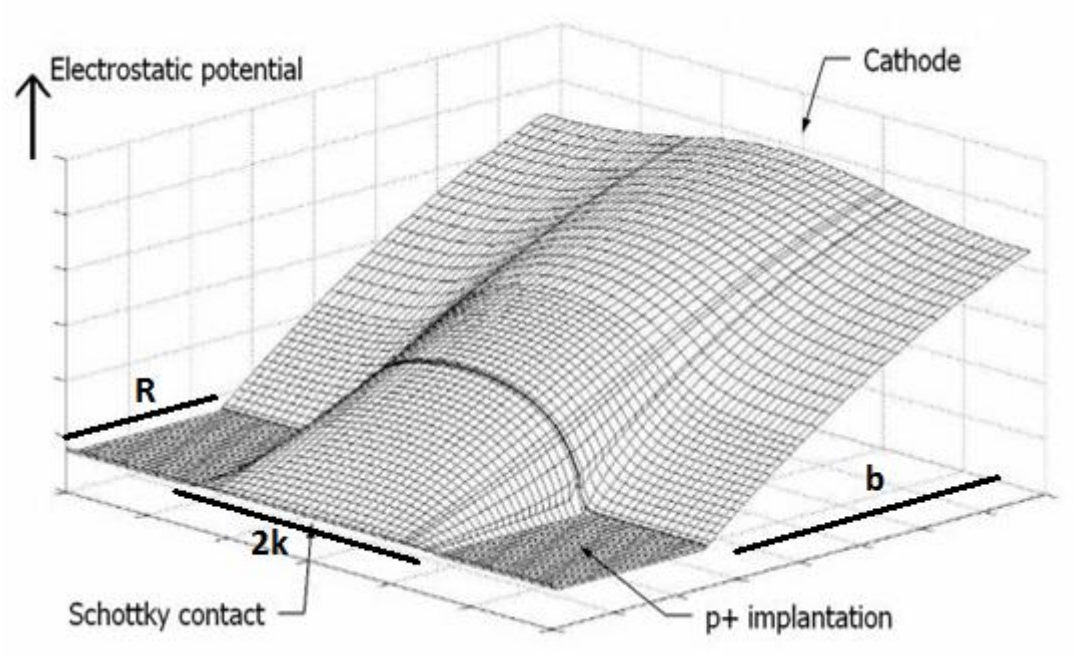

Figure 6 Electrostatic potential near the anode of a JBS diode under reverse bias

Assigning the entire Poisson component to the x- axis is valid due to the mirror symmetry of the problem across the x-axis. This problem has exact solutions, dependent on boundary conditions, as follows.

$$\emptyset_p(x) = k_2 x - \frac{qN_d}{2\varepsilon}x^2 + k_0 - - - (6)$$

and

$$\emptyset_l(x,y) = k_1 Cosh\left(\frac{\pi y}{b}\right) Sin\left(\frac{\pi x}{b}\right) + k_3 - - - (7)$$

Combining the two,

$$\emptyset(x,y) = k_1 Cosh\left(\frac{\pi y}{b}\right) Sin\left(\frac{\pi x}{b}\right) + k_2 x - \frac{qN_d}{2\varepsilon}x^2 - - - (8)$$

In (8), the constant $k_0 + k_3$ has been set to zero to have zero potential at x = 0. Now, the electric field at (x, y), (x, 0) and (0, 0) are

$$\frac{\partial \emptyset}{\partial x}(x,y) = \frac{\pi k_1}{b} Cosh\left(\frac{\pi y}{b}\right) Cos\left(\frac{\pi x}{b}\right) - \frac{qN_d}{\varepsilon}x + k_2 - - - (9)$$

$$\frac{\partial \emptyset}{\partial x}(x,0) = \frac{\pi k_1}{b} Cos\left(\frac{\pi x}{b}\right) - \frac{qN_d}{\varepsilon}x + k_2 - - - (10)$$

$$\frac{\partial \emptyset}{\partial x}(0,0) = \frac{\pi k_1}{b} + k_2 \; - - - \; (11)$$

Electric field here is defined as positive along the negative x direction so as to have a positive electric field under reverse bias. To determine k_1 and k_2, we set the voltage at the bottom of the domain

$$\emptyset(b,0) = k_2 b - \frac{qN_d}{2\varepsilon} b^2 = V_p \; - - - \; (12)$$

(12) relates k_2 and b to the potential V_p at (b, 0). Since effects of the P-N junctions on both sides are confined to x < b, electric field for x > b decreases linearly with increasing x as in a 1-D diode. So, V_p can be found by comparison with a Schottky diode of the same drift layer. The parameter b, a function of 2k and R, is then used to account for the shape of the side-implantation profile. In choosing b, we'll also be guided by simulation results as b is the distance from the Schottky contact up to which the slope of electric field v/s x is different from that found in the corresponding Schottky diode. Finally, k_1 will be found by using the boundary condition that Φ is zero along the p-n junction. Considering a circular P-N interface for the model (other lateral implantation profiles can be modeled by changing b) and assuming that the P-N interface is equipotential with zero potential, k_1 can be suitably designed. Since the Schottky junction is considered the zero potential point, the voltage at the P-N junction will actually be offset by the voltage drops at the metal-p+ contact and the part of the reverse voltage dropped on the p-side of the junction. But these voltages are negligible at high reverse bias for extremely one-sided P-N junctions as are found in high voltage diodes.

To find V_b and b, electric field at the junction of a 1-D Schottky diode is first related to the applied reverse voltage as shown in fig. 7. We consider the drift layer here to already have punched through, which is a fair assumption at the rated reverse

voltage in a JBS diode. The diode before punch through can also be treated in an analogous fashion. Punch through takes place at a reverse voltage given by

$$V_R|_{(W=W_D)} = \frac{qN_dW_D^2}{2\varepsilon} - - - (13)$$

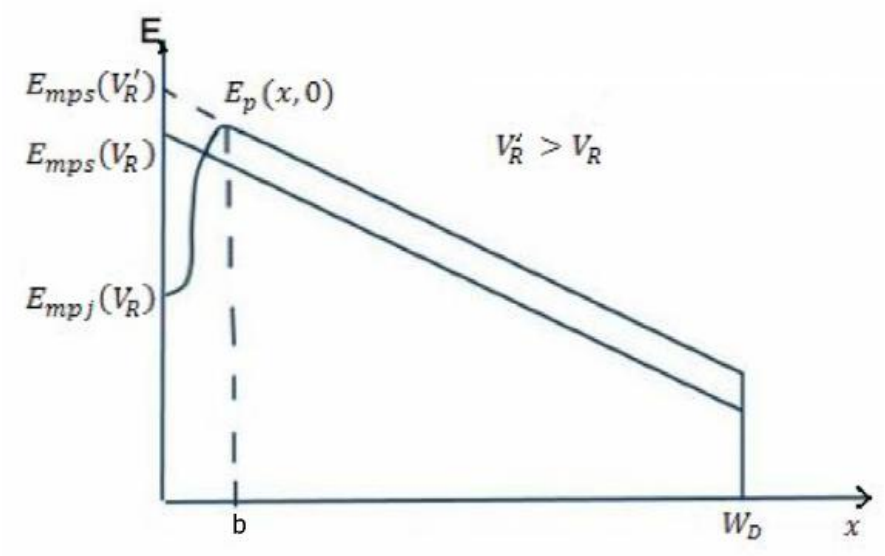

Figure 7 Electric field distribution in corresponding JBS and Schottky diodes

After punch through,

$$\left\{E_{mp} - \frac{qN_dW_d}{\varepsilon}\right\}W_d + \left(\frac{qN_dW_d}{\varepsilon}\right)\frac{W_d}{2} = V_R - - - (14)$$

But from the Poisson equation,

$$E_p(x) = E_{mp} - \frac{qN_dx}{\varepsilon} - - - (15)$$

From (14) and (15),

$$E_p(x) = \frac{V_R}{W_d} + \frac{qN_dW_d}{2\varepsilon} - \frac{qN_dx}{\varepsilon} - - - (16)$$

$$\therefore V(x) = \int_0^x E_p(x)dx = \frac{V_Rx}{W_D} + \frac{qN_DW_Dx}{2\varepsilon} - \frac{qN_Dx^2}{2\varepsilon} - - - (17)$$

Now, V_R' is that voltage at which the corresponding Schottky diode will have the same $E_p(b,0)$ as $E_p(b,0)$ of the JBS diode at V_R. From fig. 7, it is clear that $V_{R'} > V_R$. To arrive at E_{mpj} v/s V_R, starting with the Schottky diode at V_R' from (16),

$$E(b,0) = \frac{V_R'}{W_d} + \frac{qN_d}{2\varepsilon}\{W_d - 2b\} - - - (18)$$

But from (10),

$$E(b,0) = \frac{\partial \emptyset}{\partial x}|_{(b,0)} = \frac{-\pi k_1}{b} + k_2 - \frac{qN_d b}{\varepsilon} - - - (19)$$

From (18) and (19),

$$k_2 - \frac{k_1 \pi}{b} = \frac{V_R'}{W_D} + \frac{qN_D W_D}{2\varepsilon} - - - (20)$$

To uniquely determine k_1 and k_2 in terms of b, we need another relationship involving at least one of them For that, we use the boundary condition of having a zero-potential P-N junction. At a point (x', y') on the circular P-N junction at angle θ from the anode contact,

$$(x', y') = (RSin\theta, k + R - RCos\theta) - - - (21)$$

From (8),

$$\emptyset(x', y') = k_1 Cosh\left(\frac{\pi y'}{b}\right) Sin\left(\frac{\pi x'}{b}\right) + k_2 x' - \frac{qN_D}{2\varepsilon}(x')^2 = 0 - - - (22)$$

A crucial assumption here is the extrapolation of Poisson equation solution from the rectangular domain to its neighbourhood. The trade-off is that for the criterion of constant voltage independent of y at the lower edge of the rectangle to be valid, the rectangle should have a small width (range of y) and for (21) to be valid at (x', y'), the width of the rectangle should be larger. The significance of the errors due to these conflicting requirements will be assessed by comparing results with those from simulation.

We can now derive an equation to calculate E and Φ in the domain as a function of b and reverse voltage V_R'. But E and Φ thus calculated are for another Voltage V_R. To relate V_R and V_R', we use the areas under the curves in fig. 7.

$$\int_0^b E_p dx + \int_b^{W_D} E_p dx = V_R - - - (23)$$

$$or \int_0^b \left[\frac{\pi k_1}{b} Cos\left(\frac{\pi x}{b}\right) - \frac{qN_d b}{\varepsilon} + k_2\right] dx + \int_b^{W_D} \left[\frac{V_R'}{W_D} + \frac{qN_D}{2\varepsilon}(W_D - 2x)\right] dx = V_R - -(24)$$

This becomes

$$\left[\frac{V_R'}{W_D} - \frac{qN_D b}{2\varepsilon}\right](W_D - b) + k_2 b - \frac{qN_d b^2}{\varepsilon} = V_R - - - (25)$$

From (10), (22) and (25), k_1, k_2 and V_R are related to the only remaining parameter b. The two extremes of side-implantation are zero side-implantation (rectangular profile) and 1:1 side-implantation (circular profile). From simulation, there is significant difference in E (0, 0) between the two cases. The parameter b will be used to adjust the model for these two conditions. Since b is the extent of the effect of the P-N junctions on potential, it increases with increasing k and R. For the circular profile, by comparing model and simulation data, the best linear fit is found to be for-

$$b = \frac{k}{2} + 3\,{}^{R}/_{2} - - - (26)$$

For the rectangular profile, it is

$$b = \frac{k}{2} + 2R \; - - - (27)$$

Both (26) and (27) have b > R, and are only valid when R << W_D. Similarity in the effects of R and k on the electric field can also be seen in fig. 8 which presents simulation results from Synopsys Sentaurus [32] for the case with no side-implantation. It is clear that reducing k is as potent in lowering E(0,0) as increasing R. But increasing R increases the on-resistance at a much higher rate than reducing k. The effect of R and k on the on-resistance is shown in (44). Increasing R reduces the drift layer "seen" by the P-N junction, causing the diode to break down at lower

reverse bias. Narrower k is also much easier to fabricate that deeper R. Thus, reduction of electric field at the anode contact is best achieved by reducing k. So, in the validation of this work, we assume a constant R of 0.5μm and vary k to control E(0,0). R = 0.5μm is a depth that is easy to achieve by implantation in SiC and has also been used in the experimental results presented later in this work. However the model we present is appropriate for all $R<<W_D$.

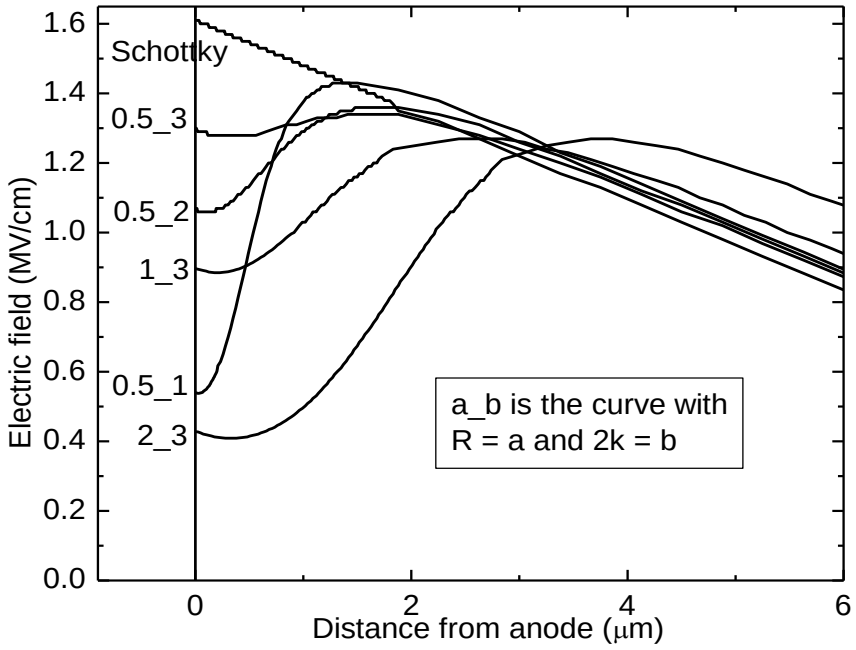

Figure 8 Dependence of the electric field at (x,0) on R and 2k

In (26) and (27), as the coefficient of R is higher without side-implantation, b is greater and reduction in electric field at the Schottky interface is more pronounced. This supports the intuitive understanding that a more rectangular side-implantation profile brings the P-N junctions closer to the channel thereby enhancing the potential barrier created in the channel and shielding the electric field at the Schottky contact better. The value of θ chosen to identify the point (x', y') is not found to affect the model parameters significantly. This is understandable as in the circular implant case

used for the model, with increasing x', both y' and Φ(x', 0) increase. Higher Φ(x', 0) requires a higher y-value for the hyperbolic cosine factor to reduce Φ to zero. For the model solutions found in the next section, θ= 30º is used. Throughout this analysis, we assume abrupt P-N junctions and implantation with constant box profile, i.e. constant p+ and n- doping.

Summarizing the model, to find E(0,0) we use (10) which relates it to k_1 and k_2. Using b from (26) or (27), we solve (20), (22) and (25) simultaneously to obtain k_1 and k_2. This leads to the following closed form relationship, after punch through, between the maximum electric field and reverse voltage.

$$E_{max} = E(0,0) = \frac{k_1 \pi}{b} + k_2 \quad --- (28)$$

The constants k_1 and k_2 are given by

$$k_1 = \frac{V_R + \frac{qN_D}{2\varepsilon}(b^2 + W_D^2 - x' W_D)}{\pi - \frac{W_D}{x'} Cosh\left(\frac{\pi y'}{b}\right) Sin\left(\frac{\pi x'}{b}\right) - \frac{\pi W_D}{b}} \quad --- (29)$$

$$k_2 = \frac{V_R}{W_D} + \frac{qN_D}{2\varepsilon}\left(\frac{b^2}{W_D} + W_D\right) + k_1 \pi \left(\frac{1}{b} - \frac{1}{W_D}\right) \quad --- (30)$$

Before punch-through, appropriate modifications to (20) and (25) will easily give electric field that will now depend on $\sqrt{(V_R)}$ rather than V_R itself. But in that case, while the same method as above gives electric fields at particular reverse voltages, a closed form solution involves solving cumbersome quadratic equations. Since design of JBS diodes requires leakage current at and near rated reverse voltage, which is best designed to be after punch-through, the closed form solution for lower voltages is not explicitly worked out here, although the proposed model can be suitably modified for that purpose. Before punch-through, an approximate closed form solution for E (0, 0) is-

$$E_{max} = E_{max}|_{(W=W_D)} \sqrt{\frac{V_R}{V_{R_{(W=W_D)}}}} - - - (31)$$

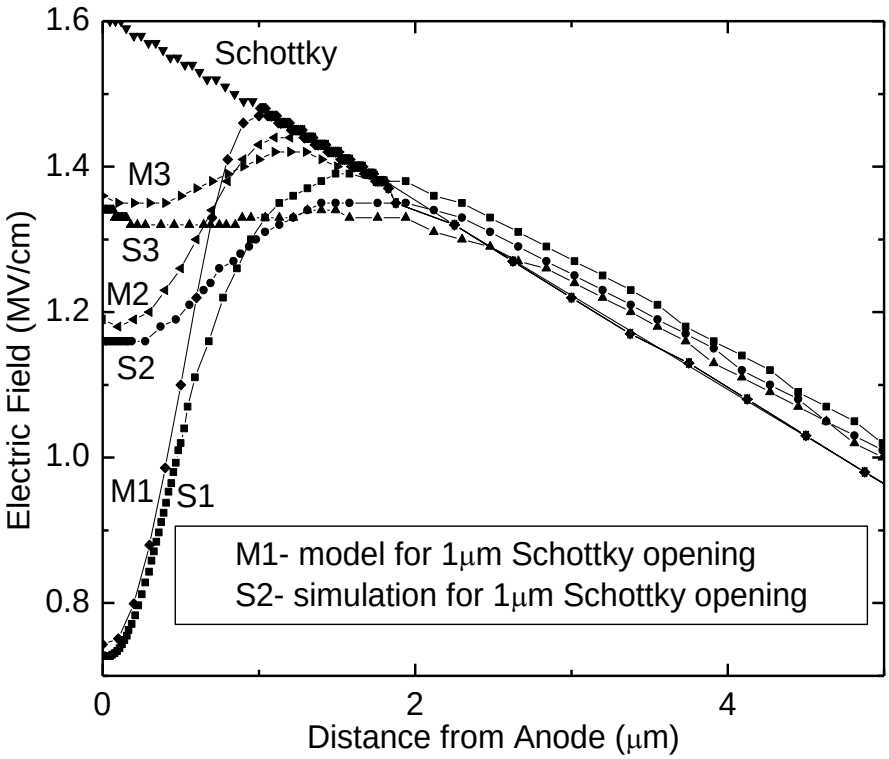

Figure 9 Comparison at V_R=1000V of model (M) and simulation (S)

Electric field at (0, 0) with V_R= 1000V, W_d = 12μm and N_d= 7 X 10^{15}cm^{-3} is compared between the model and simulation results in Table 1 for both the rectangular and circular side-implant profiles. For the latter, E(x, 0) v/s x is also shown near the Schottky junction in fig. 9. Despite discrepancies in the exact shape of E(x, y), the model does predict very well the amount by which electric field reduces at the Schottky junction, which is key to JBS diode operation. In table 3, it is obvious that lateral spread of implantation makes a big difference in the electric field shielding achieved in a JBS diode. Smaller the lateral spread, more the shielding achieved (for the same effective Schottky region width). Practical implantation conditions will all lie between the squared and rounded side-implant assumptions. The simulation and

model results were also compared at V_R=1600V with similar agreement as that obtained at 1000V. So, the validity of model, as expected, is independent of reverse voltage. At a low Schottky opening of 1μm, the maximum electric field "seen" by the Schottky contact is < 50% of the Schottky diode with same epitaxial layer thickness and doping.

2k (μm)	E(0,0) from Simulation (MV/cm)		E(0,0) from Analytical Model (MV/cm)	
	Circular	Rectangular	Circular	Rectangular
1	0.73	0.54	0.74	0.58
1.5	1.00	0.87	1.02	0.86
2	1.16	1.07	1.19	1.05
2.5	1.27	1.19	1.29	1.18
3	1.34	1.30	1.36	1.28
Schottky	1.61	1.61	1.59	1.59

Table 3 Comparison of the maximum electric field at the Schottky contact from the model and simulation for different implantation-straggle profiles at V_R= 1000V

Variation of maximum electric field at the Schottky contact with applied reverse voltage at various Schottky openings, as predicted by the model and from simulation, are shown in fig. 10 for circular side-implantation and in fig. 11 for rectangular side-implantation. There is very good agreement between the model and simulation.

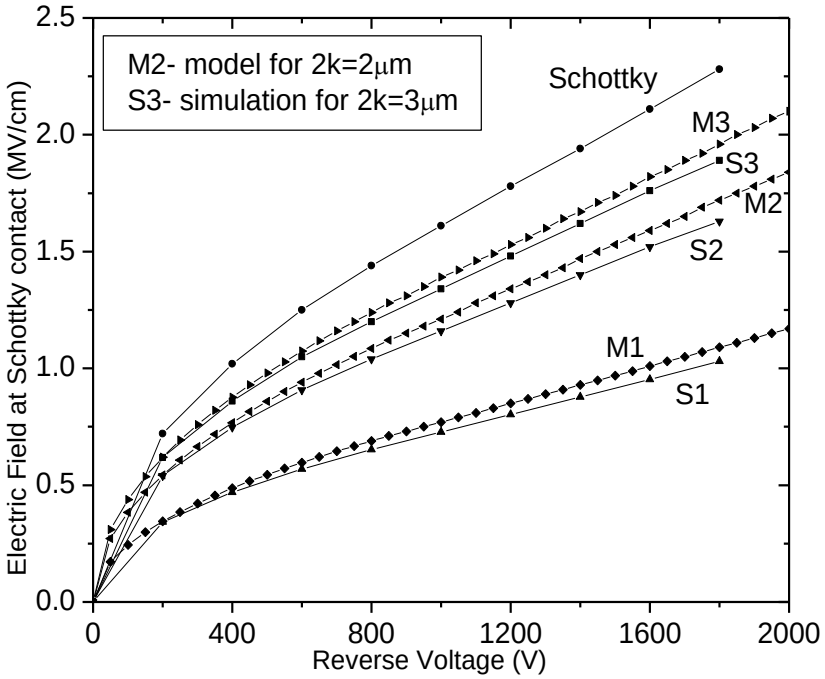

Figure 10 Comparison of model and simulation with circular side-implantation

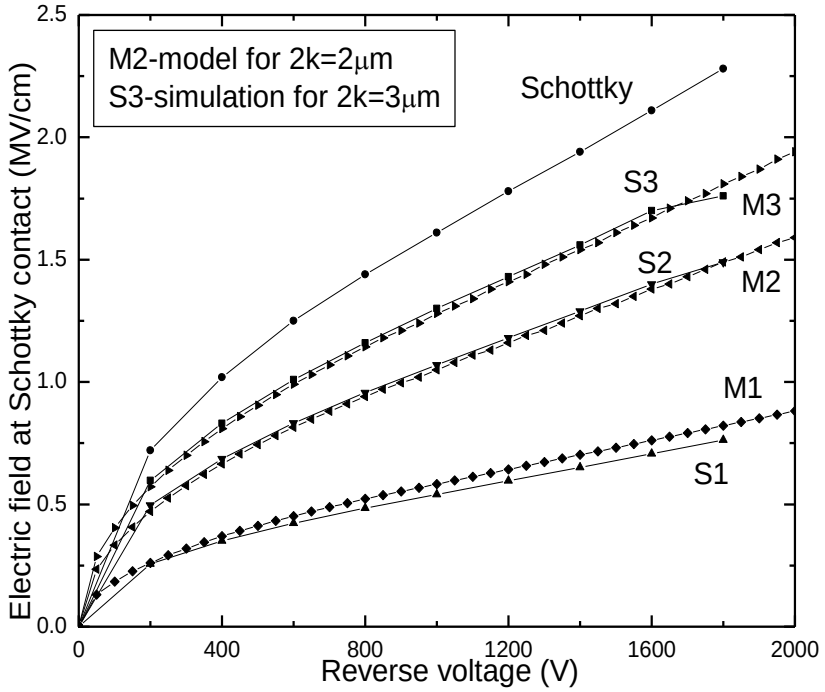

Figure 11 Comparison of model and simulation with no side-implantation

At constant k, lower side-implantation reduces the maximum electric field at the Schottky contact without affecting the area available for forward conduction, which is clearly preferred. In the next section, the relationship between electric field and reverse leakage current is explored, which in combination with the relationship between voltage and electric field leads to final closed form solutions to the leakage current of JBS diodes under reverse bias.

2.1.3 Electric Field and Leakage Current

The mechanisms for reverse current conduction in a JBS diode are thermionic emission across the Schottky barrier and quantum mechanical tunneling through it. Local current density due to thermionic emission is given by

$$J_{Sch} \approx A^{*}T^{2} \exp\left(-\frac{q(\emptyset_B - \sqrt{qE/4\pi\varepsilon})}{kT} \right)\left(\exp\left(\frac{\mathrm{qV}}{\mathrm{kT}}\right) - 1\right) - - - (32)$$

In (32), the latter voltage-varying exponential can be neglected under high reverse bias [18]. At low electric fields, thermionic emission dominates. But, as electric field increases J_{Sch} pales in comparison with the tunneling current density through the barrier, which can be approximated by the Fowler-Nordheim equation [33, 34] as

$$J_T = -CE^2 \exp(-\beta/E) - - - (33)$$

Negative sign in (33) is necessary because current is opposite to the direction of electron tunneling. The constants are

$$C = \frac{q^2 m_0}{16\pi^2 \hbar m^{*} \emptyset_B}\ Amperes/Volts^2 \ - - - \ (34)$$

$$\beta = \frac{4}{3}\frac{\sqrt{2m^{*}}}{q\hbar}(q\emptyset_B)^{\frac{3}{2}}\ Volts/meter \ - - - \ (35)$$

Tunneling in (33) is derived considering electron emission into a dielectric which gives a triangular potential barrier. Due to stored charge in the semiconductor, the potential barrier faced by electrons tunneling through a Schottky barrier is not exactly triangular but might be approximated as that in the interest of a closed-form relationship, especially under high reverse bias. A more accurate relationship can be obtained using WKB approximation [33] of the potential barrier obtained by (8). The ratio m^*/m_0 in (34) and (35) depends on many factors and has been studied at the SiC interface in [35-37]. The combination of J_T and J_{Sch} has been fitted, using m* as a parameter, with experimental Schottky diode reverse leakage currents in [27]. [27] and [28] also use the same approach for the JBS diode, accounting only for the reduced Schottky area in the JBS diode and the reduction in electric field at the center of the Schottky region. In effect, that makes an unjustified assumption that the normal electric field all across the Schottky contact in a JBS diode is the same as that at its center. Fig. 12 shows the variation of the normal component of the electric field at the Schottky contact with y, as predicted by our model and simulation. The abscissa is scaled to vary from -1 to 1 across the Schottky length and the ordinate from 0 to 1 as the normal electric field varies from 0 to its maximum value at the center. Electric field from the model can be re-stated from (9) as

$$E_x(0,y) = k_2 + \frac{k_1\pi}{b} Cosh\left(\frac{\pi y}{b}\right)$$

$$\approx E_x(0,0) * \left(2 - Cosh\left(\frac{y}{l} Cosh^{-1}(2)\right)\right) - - - (36)$$

The approximation in (36) models $E_x(0, y)$ from its maximum at (0, 0) to zero at the P-N interface as a hyperbolic cosine. From fig. 12, the analytical model's prediction is most accurate at smaller 2k, which is due to the same reasons as detailed

in the previous section. At all values of 2k, it models the variation of $E_x(0, y)$ with little error compared to an assumption of independence of $E_x(0, y)$ with y.

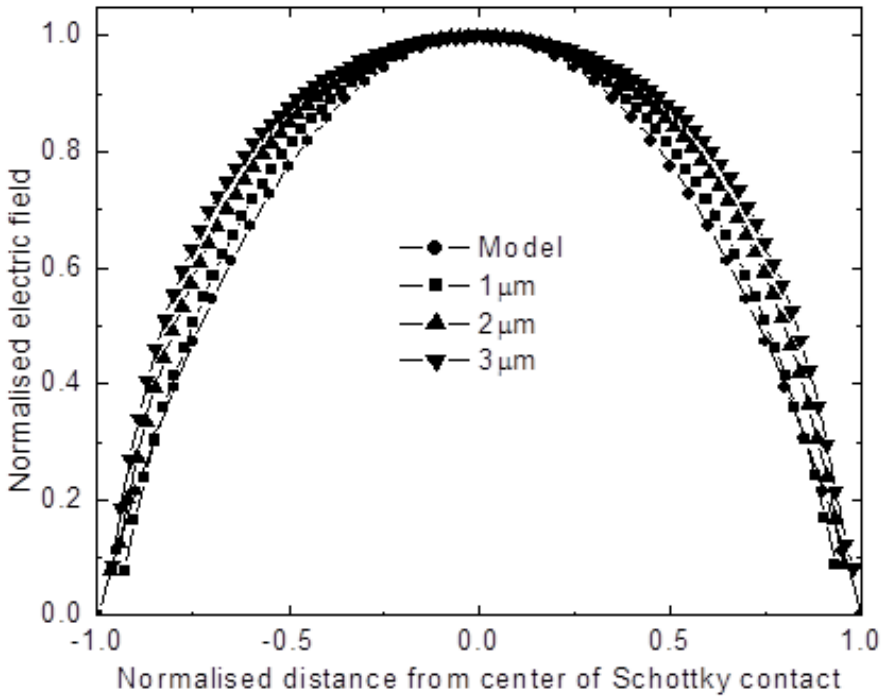

Figure 12 Variation of normal electric field across the Schottky contact

Two distributions of the Schottky and P-N regions that have been favoured at the anode of a JBS diode are interdigitated stripes of P-N and Schottky fingers and a honeycomb structure [20]. Assuming for now that we have interdigitated stripes (other structures will be comparatively evaluated in the next chapter), the total current through one Schottky finger is

$$I_S = \int (J_{Sch} + J_T) dA = \int_{-k}^{k} h(J_{Sch} + J_T) dy \quad --- (37)$$

Then, the reverse leakage current density of the JBS diode is

$$J_R = \frac{I_S}{hP} = \frac{2(k' J_{Sch} + k'' J_T)_{E(0,0)}}{P} \quad --- (38)$$

In (38), 2k' and 2k" are the effective Schottky widths that if E(0, y) = E(0, 0) would give the same J_{Sch} and J_T respectively. From (32), (33), (36) and (37), the integrals to find k' and k" are difficult to solve exactly. First order linear

approximation of the exponential in (36) and (37) are used to simplify the calculation. This is valid because J_{Sch} is a significant part of J_R at lower electric fields when $\sqrt{qE/4\pi\varepsilon} \ll 1$ and J_T is significant only at higher electric fields when $\beta/E \ll 1$. The variation of E(0, y) in fig. 12 can be modeled, for this approximation, as a parabola without much error. Then, we obtain

$$\frac{k'}{k} \approx \frac{1+\frac{\pi}{4}\sqrt{\frac{q^3E}{4\pi\varepsilon(kT)^2}}}{1+\sqrt{\frac{q^3E}{4\pi\varepsilon(kT)^2}}} - - - (39)$$

$$\frac{k''}{k} \approx \frac{\frac{8E}{15}-\frac{2\beta}{3}}{E-\beta} - - - (40)$$

k'/k in (39) is approximately 1 for low electric fields when the thermionic emission component is significant. This agrees with our understanding that thermionic emission current across the Schottky barrier is not very sensitive to electric field at the barrier. At high electric fields starting well below the rated reverse voltage, k"/k for the tunneling component in (40) approaches 8/15. Using these approximations, fig. 13 shows the model's predictions of reverse leakage currents for Schottky diodes and JBS diodes with various Schottky widths and barriers. Suppression of reverse current relative to Schottky diode is seen at barriers of 0.8eV and 1.3eV. The voltage at which tunneling current becomes significant relative to thermionic emission increases when the Schottky barrier increases. The model's predictions for 1.3eV Schottky barrier and 2k= 1μm is not fully accurate as the current is so low that P-N junction leakage current cannot be neglected in comparison to it. But if a JBS diode is so designed, well known P-N junction leakage current formulae can be used to supplement the leakage current across the Schottky barrier.

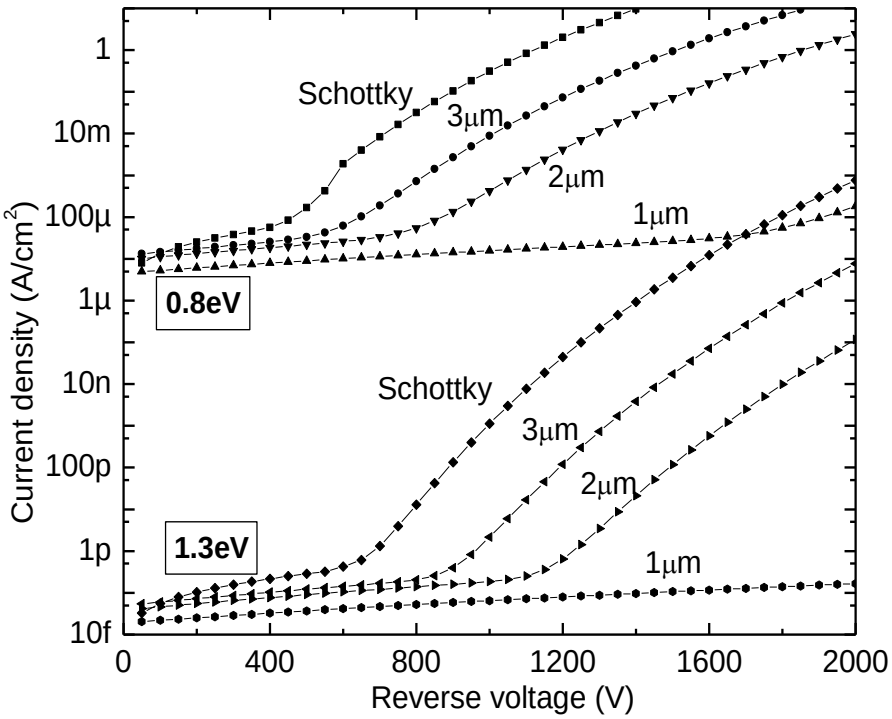

Figure 13 Variation of reverse leakage of JBS and Schottky diodes

2.1.4 Experimental Results

SiC JBS diodes with a drift layer thickness of 12µm, carrier concentration of 7 X 10^{15} cm^{-3}, and 2k of 2µm and 3µm were fabricated. Reverse I-V curves of these devices were then compared with those predicted by the model, as shown in fig. 14. Schottky barrier at the Ti-SiC junction is assumed to be 1eV. As deposited, Ti has a barrier around 0.8eV with SiC but the metal was annealed at 500C for 10 minutes, after which the barrier was expected to have risen to around 1eV [19]. Excellent fit, as shown in fig. 14, is obtained at high voltages with $m^*=0.24m_0$ for 2k of both 2µm and 3µm. While the value of m* in the experimental case considered has previously been reported as $0.33m_0$ [36], agreement of our model with experiment at the same m* for different Schottky openings supports its validity in our case. Divergence at low currents might be attributed to limitations in the accuracy and noise suppression

capabilities of the measurement apparatus. On comparison with the fully analytical Si-JBS diode model in [18], as shown in fig. 15, the proposed model presents great improvements in predicting the I-V curves of high voltage JBS diodes. The 1-D models in [27] and [28] are also included for comparison. Thermionic emission in [27] and [28] are high because E(0,0) predicted by them are high. Using m* reported in them, tunneling current given by [27] is too low whereas that predicted by [28] is too high. Those 1-D models were optimized for a wide variety of 2k, Φ and N_D whereas the proposed 2-D model applies more widely.

Considering the JBS diode as a modified Schottky diode, excellent agreement of the electric field at the barrier between model and simulation suffices as a validation of the JBS diode model. But in practice, predictive power of the model hinges on the accuracy of Schottky diode theory. However, the leakage current of the Schottky junction is extremely sensitive to poorly defined effective mass values. Further investigation into tunneling models for current through the metal-semiconductor junction and accurate measurements of the effective mass of electrons along different crystal directions are needed to improve the reliability of Schottky diode theory.

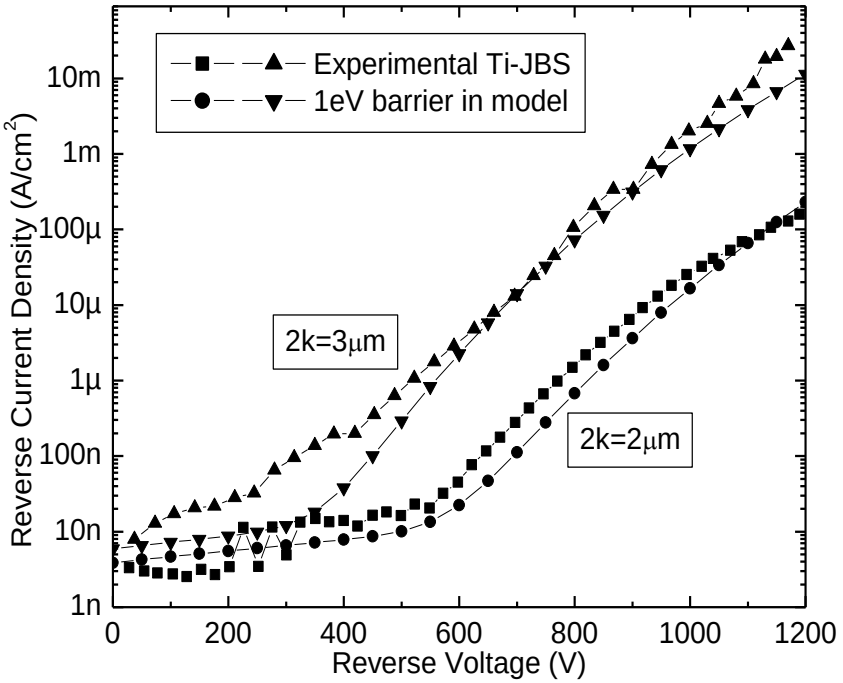

Figure 14 Model and experimental SiC JBS diode reverse I-V curves at 300K

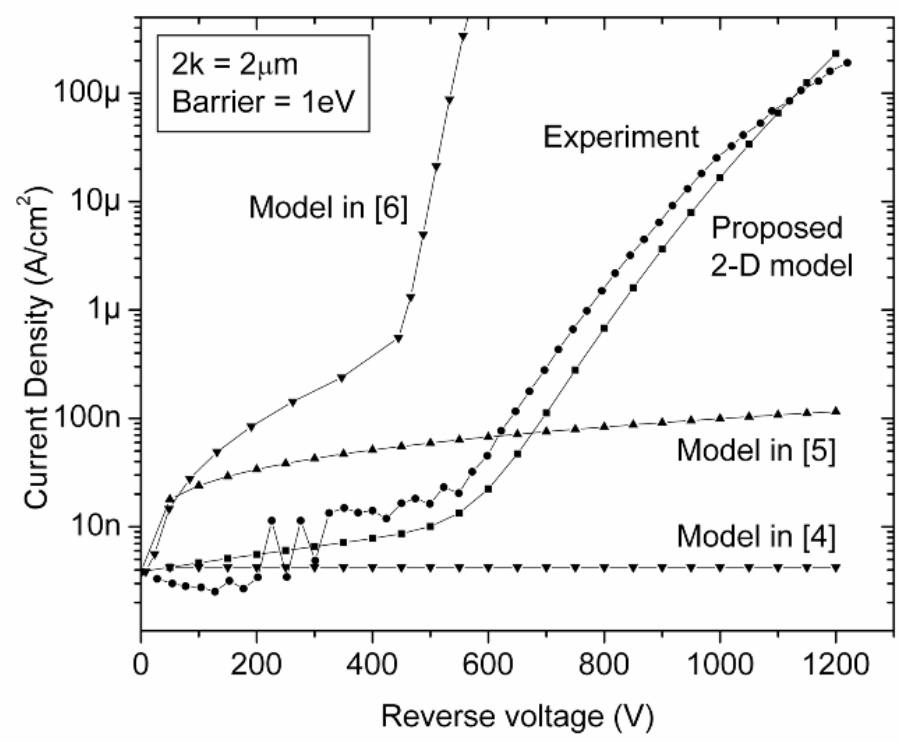

Figure 15 Comparison in reverse bias of the proposed model with other published models

2.1.5 Forward Bias

Besides reverse leakage current, the other circuit design parameter for JBS rectifiers is specific on-resistance. An adequate analytical model for specific on-resistance which has already been provided in [27] and supported by experimental data is reproduced below.

$$R_{sp.on} = R_{channel} + R_{spread} + R_{Drift} + R_{substrate} + R_{contact} - - - (41)$$

$$R_{channel} = \frac{RP}{2q\mu_n N_D(k - W)} - - - (42)$$

$$R_{spread} = \frac{\rho_D P}{2} ln\left(\frac{P}{2(k - W)}\right) - - - (43)$$

$$R_{Drift} = \rho_D \left(W_D - R - \tfrac{1}{2}\big(P - 2(k - W)\big)\right) - - - (44)$$

$R_{sp.on}$ is the specific on-resistance and various subscripts indicate the specific resistance components from the respective regions of the diode. μ_n denotes electron mobility, J_F forward current density, V_F forward voltage and W the part of the Schottky region depleted by the P-N junction even in forward bias. In this breakdown of $R_{sp.on}$, the channel and spreading components depend on the proportion of the area of Schottky regions (k/P) in the diode. When the proportion of Schottky area decreases, the rate at which reverse current density (from (32-37) and fig. 13) is suppressed is faster than the rate at which specific on-resistance increases. So, with good edge termination and material quality, when reverse leakage is due only to thermionic emission and tunneling, a low value of 2k can be chosen to take advantage of JBS action. Active area of the JBS diode can then be increased to achieve the required low on-resistance.

To retain Schottky-diode like switching characteristics, JBS diodes under forward bias should be operated in unipolar mode. Then, the forward current-voltage

characteristics can be modeled as thermionic emission over a barrier that is in series with the specific on-resistance.

$$V_F = \emptyset_B + \frac{kT}{q}\ln\left(\frac{P}{2(k-W)}\frac{J_F}{A^*T^2}\right) + J_F R_{sp.on} - - - (45)$$

2.1.6 Compact I-V model for JBS diode

Physics-based closed form equations connecting reverse current and voltage of a punch-through JBS diode as a function of its design parameters have been developed [38]. For the same Schottky width, lateral spread of implantation is shown to reduce the electric field shielding effect of the JBS diode in reverse bias. Closed form equation derived for maximum electric field at the Schottky contact of the JBS diode helps compare JBS diodes of various Schottky widths. Predictions of reverse IV characteristics made using this model are validated against experimental JBS diode IV curves. In conjunction with the forward bias model in [27], a complete analytical theory for JBS diodes is provided which can easily be used in their design.

An approach similar to that in this work can be employed to form a theory of the Trench MOS barrier Schottky rectifier [39], among other shielded power diodes. A fuller understanding of the metal-semiconductor contact and formulation of accurate Fowler-Nordheim like closed form equation for tunneling at the metal-semiconductor junction will also improve the predictions of the model. Finally, the proposed JBS diode theory will be most successful if the insight gleaned from it on the effects of various design parameters helps introduce refinements that lead to performance improvements.

2.2 Analytical Modeling of SiC VJFET

In an n-channel VJFET, the n+ drain is on the back side and the source and gate are on the front side of the wafer. Under sufficient negative (or zero if the

channel is thin enough) gate bias, there is a potential barrier built up in the channel that prevents current from the source. But as drain voltage increases, the potential inside the channel rises from the drain side and if the channel is short, overcomes the potential barrier before the gate-drain avalanche limit, a phenomenon called drain-induced barrier lowering (DIBL). So, the performance of VJFETs with short channels is controlled not only by gate voltage but also by drain voltage. Hence, they are also called Static Induction Transistors (SIT). While long-channel JFETs can be modeled well using Shockley's classical 1-D analysis [40], the most popular model for Si SITs was provided by Bulucea et al. in 1987 [41] and Spirito et al. in 1990 [29].

SIT models solve Maxwell's electrostatic equation in two dimensions in the JFET channel by assuming some boundary conditions. They provide I-V relationships in the blocking and conduction modes but assume an abrupt gate-channel junction. This assumption might be valid for Silicon devices where fabrication processes are so advanced that a near-abrupt junction can be realized. However, for SiC VJFETs, the analytical model has to be extended to realistic gate-channel doping profiles as obtained from advanced tilted gate implantation used for their fabrication. Fig. 16 shows ProfileCode [42] simulations showing the results of individual and combined tilted implantations at various energies and doses into SiC.

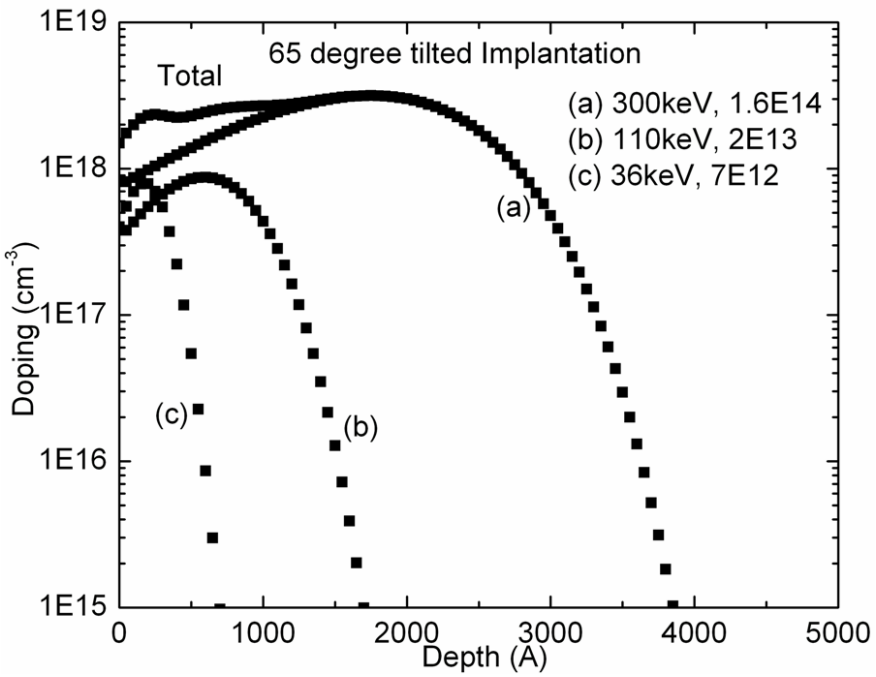

Figure 16 Simulation of doping profiles with implantation into 4H-SiC

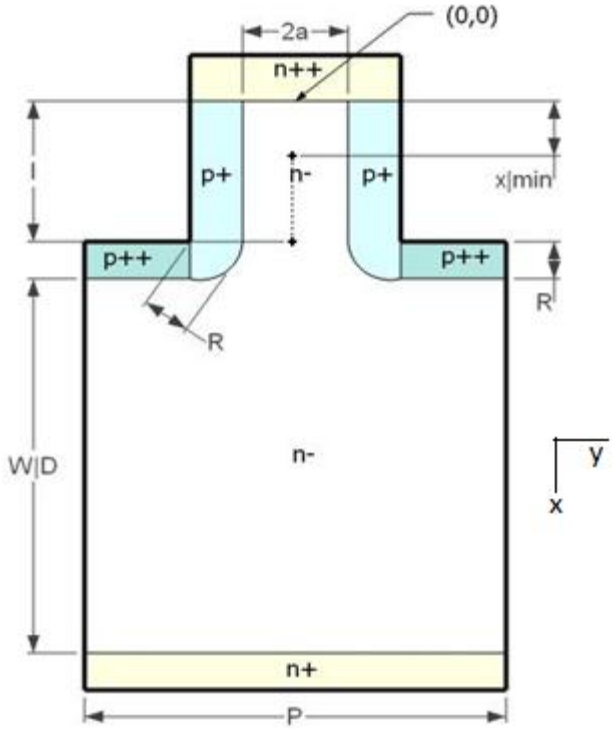

Figure 17 Cross-section of an n-channel VJFET with design parameters

The tail of implanted ions is significant and the gate-channel junction far from abrupt. This can be better modeled as a linearly graded junction than as an abrupt junction. For a linearly graded gate-channel junction with channel half-width “a” and

net acceptor concentration linearly increasing from 0 to N_A between "a" and "b" (the cross section is shown in fig. 17), the acceptor and donor concentrations are given by

$$N_A(y) = \begin{cases} N_A\,;\ y > b \\ N_A\left(\frac{y-a}{b-a}\right); a < y < b \end{cases} \quad ---(46)$$

$$N_D(y) = \begin{cases} N_{ch}\,; y < a - \frac{N_{ch}}{N_A}(b-a) \\ N_A\left(\frac{a-y}{b-a}\right)\ otherwise \end{cases} \quad ---(47)$$

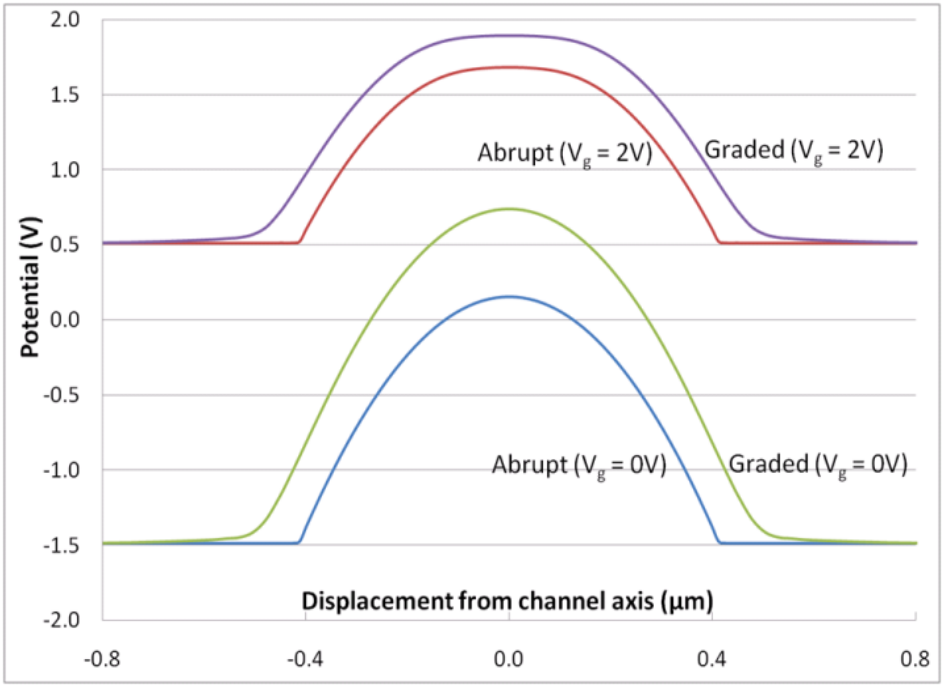

Figure 18 Potential perpendicular to the axis of a VJFET at its saddle point

The thickness of channel required for normally-off operation will then be much less than that designed using an abrupt gate-channel approximation. This is illustrated in fig. 18, in which TCAD simulation results show the variation of potential perpendicular to the axis of a VJFET along its point of minimum potential, which in blocking mode is also called "saddle point" since the curvature of potential along the x and y at this point are in opposite directions. In the graded case, besides potential drop on the p+ side of the gate-channel junction, the potential at the axis of the channel is raised and leveled off. Both of these effects indicate that the potential

barrier in the channel is reduced, or the channel is less turned off. Hence, with graded gate doping, the channel has to be thinner to achieve the same normally off operation as that of an abrupt gate-channel junction.

2.2.1 Blocking Mode- Drain Induced Barrier Lowering

When the channel is turned off, solving the 1-D Poisson equation using these carrier concentrations in (46) and (47) for a linearly graded junction gives

$$E_{max} = -\frac{qN_{ch}}{\varepsilon}\left(a - \frac{N_{ch}}{2N_A}(b-a)\right) - - - (48)$$

The built-in potential at the gate-source junction is obtained by integrating the electric field profile. Since$N_{ch}/N_A \ll 1$, all but its lowest power term can be neglected to a first approximation. After some simplification, we obtain

$$V_{bi} \approx \frac{qN_{ch}a^2}{2\varepsilon}\left[1 + \frac{4\sqrt{2}}{3}\sqrt{\frac{N_{ch}}{N_A}\frac{(b-a)}{a}}\right] - - - (49)$$

Then, the total 1-D potential barrier in the channel is given by adding to V_{bi} the contact potentials between channel & source, source & gate and the applied gate voltage.

$$\emptyset_c = \frac{kT}{q}\left\{ln\left(\frac{N_{ch}N_A}{n_i^2}\right) + ln\left(\frac{N_S}{N_{ch}}\right)\right\} - V_{GS} - V_{bi} - - - (50)$$

As gate-channel junction becomes less abrupt, V_{bi} increases and the 1-D potential barrier Φ_c decreases. The equivalent channel half-width (a_{abrupt}) of a VJFET with abrupt gate-channel junction will be such that Φ_c and hence the blocking performance remains the same. So, we have

$$a^2\left[1 + \frac{4\sqrt{2}}{3}\sqrt{\frac{N_{ch}}{N_A}\frac{(b-a)}{a}}\right] = a_{abrupt}^2 - - - (51)$$

From (51), for a graded gate-channel junction to have the same DIBL

performance as an abrupt junction, it has to be smaller. This is also illustrated in fig. 18 as the potential at the saddle point of the potential plot in a VJFET is higher in the graded case with the same channel width. When the potential at the saddle point rises, the potential barrier seen by electrons in the source falls and DIBL is easier. To maintain the same potential barrier as for abrupt junctions, the channel width of the VJFET will have to be lower.

Substituting (51) in Bulucea and Rusu's model, (relevant parts of which is reproduced in appendix- 1 to arrive at (52)) we have a relationship between design parameters and the potential barrier. When DIBL reduces the potential barrier Φ_{min}, the increasing channel current creates a negative feedback which doesn't allow Φ_{min} to reduce at the same rate [41]. However, that effect can be neglected in order to find an outer bound on the channel design. From their analysis, the 2-D potential barrier in the channel can be calculated

$$-\emptyset_c + 2\sqrt{\frac{\mu_0^2}{(\mu_0^2-1)(\mu_0+1)}\left[\emptyset_c - \frac{V_D^*}{(\mu_0-1)}\right]\left[V_D^* + \left(\frac{\mu_0-1}{\mu_0}\right)P\right]} = \emptyset_{min} - - - (52)$$

$$\mu_0 = \exp\left(\frac{\pi l}{2a}\right) \gg 1 - - - (53)$$

The inequality in (53) is the definition of a long-channel VJFET. If it is many orders of magnitude greater than 1, then Shockley's 1-D analysis will be sufficient and there will be no prospect of DIBL. In more optimized designs, it is still more than an order of magnitude greater than 1. For normally-off operation, the optimum channel is that where channel current due to DIBL at zero gate voltage is significant at the same drain voltage as when gate-drain avalanche current starts. If the channel is longer or narrower, the ON resistance increases without any increase of blocking capability. Setting Φ_{min} = 0.6V for the onset of significant DIBL-induced current and solving (52) and (53), we have the ratio of channel length to channel width

$$\frac{l}{2a} = \frac{1}{\pi} ln\left(\frac{V_D^*(V_D^* + \emptyset_c)}{\emptyset_c(V_D^* + \emptyset_c) - (\emptyset_c + 0.6)^2/4}\right) - - - (54)$$

V_D^* in (54) is defined in [41] as the voltage at the "intrinsic drain", which is at the center of the lower edge of the channel. V_D^* can be related to V_D approximately by assuming that the equipotential line passing through D^* is half the distance from the P-N junction (c) below the center of the gate trench as it is at D^* [29]. Then,

$$2c = \sqrt{(R + a)^2 + R^2} - R - - - (55)$$

After the drift layer has been punched through,

$$V_D^* = V_c = \frac{V_{DS}c}{W_D} + \frac{qN_D W_D c}{2\varepsilon} - \frac{qN_D c^2}{2\varepsilon} - - - (56)$$

(54), (55) and (56) impose an additional constraint on the channel length and width beyond that which follows from the traditional 1-D analysis in order to design for DIBL leading to high current only around avalanche.

The validity of approximations made during this analysis is studied by comparing V_{DS} at the onset of DIBL using (54-56) with that predicted by TCAD software Sentaurus Device for different combinations of "l" and "a" with N_{ch}= 1E16 /cm^3 and W_D= 9.5µm. Fig. 19 shows the variation of the voltage at which TCAD simulations show the onset of DIBL with channel length. Fig. 20 shows the predictions of the analytical model on the potential battier in the channel as a function of channel length. It can be seen that with both a= 0.35um & a= 0.4um and b-a= 0.1um, the onset of DIBL in fig. 19 coincides with the avalanche limit (~1500V) at the same channel length as that when the channel potential barrier falls to ~ 0.6V in fig. 20. Besides supporting the analytical model, these results also support our choice of 0.6V as the minimum potential barrier in (54).

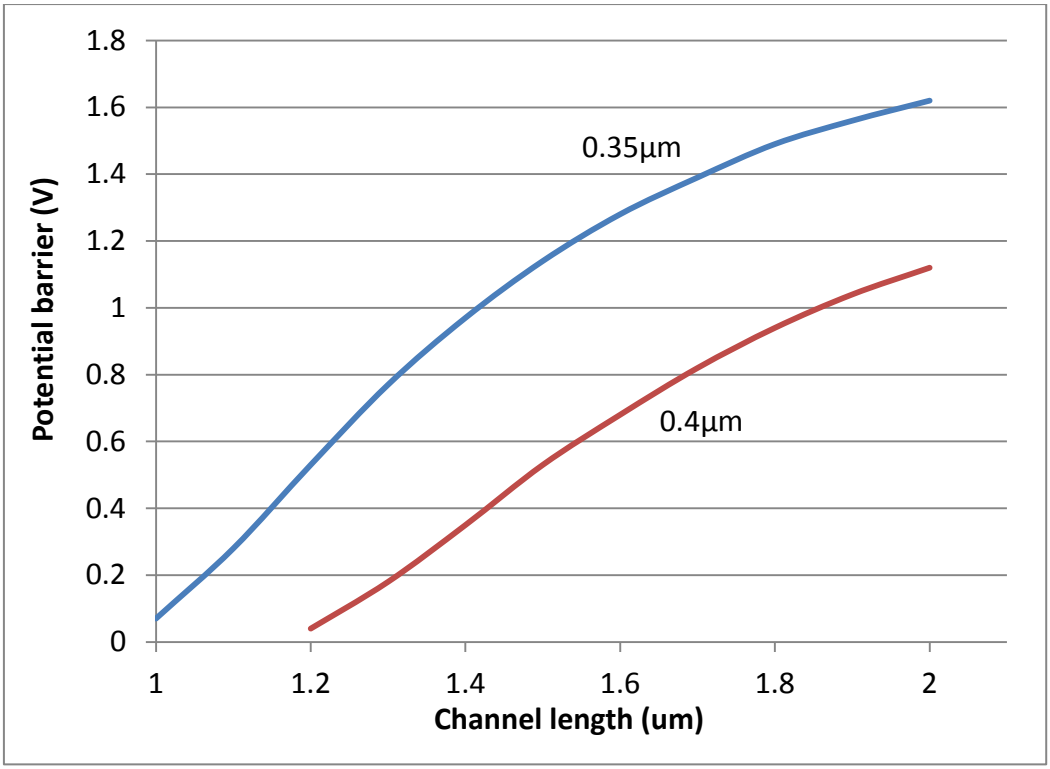

Figure 19 Analytical model of channel potential barrier with channel length at 1500V

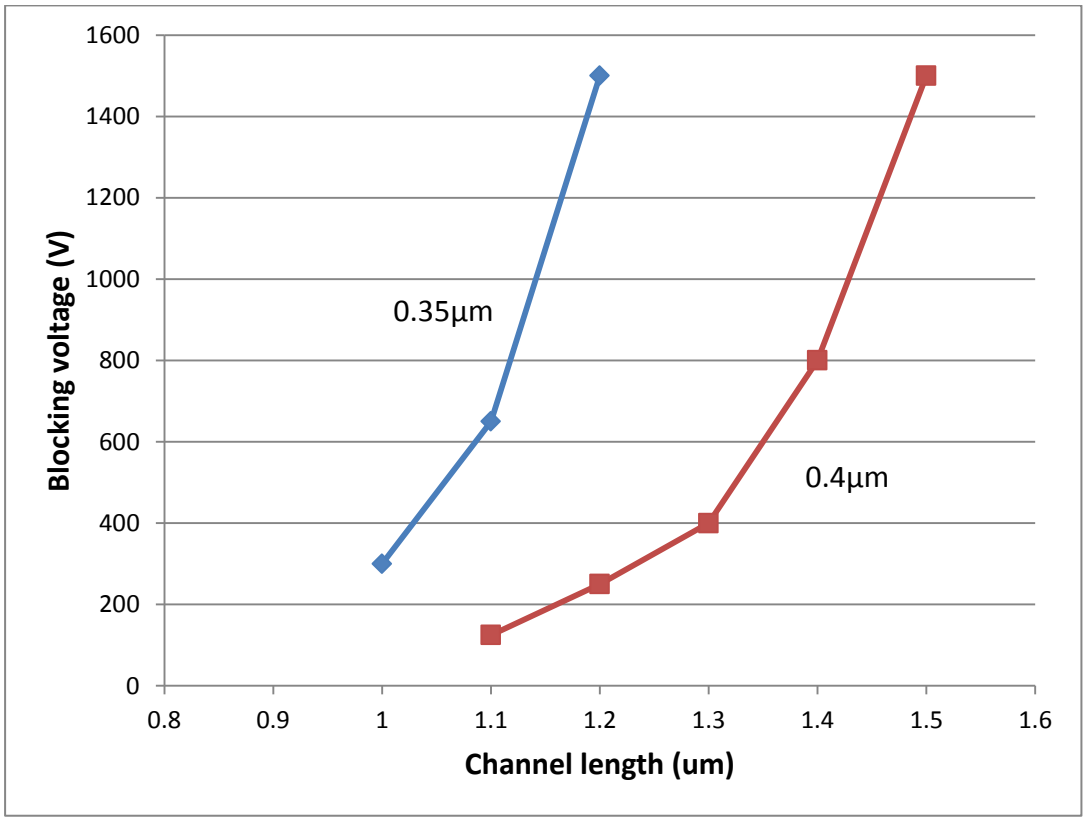

Figure 20 TCAD results showing onset of DIBL versus channel length

2.2.2 Conduction- ON Resistance

When the VJFET channel is completely opened, the ON resistance can be modeled simply as the sum of the resistances of various regions in series, similar to that for the JBS diode in section 2.1.5.

$$R_{sp.on} = R_{channel} + R_{spread} + R_{Drift} + R_{substrate} + R_{contact} - - - (57)$$

$$R_{channel} = \frac{RP}{2q\mu_n N_D(a-W)} - - - (58)$$

$$R_{spread} = \frac{\rho_D P}{2} ln\left(\frac{P}{2(a-W)}\right) - - - (59)$$

$$R_{Drift} = \rho_D \left(W_D - R - \tfrac{1}{2}\big(P - 2(a-W)\big)\right) - - - (60)$$

$R_{sp.on}$ is the specific on-resistance and various subscripts indicate the specific resistance components from the respective regions of the VJFET. μ_n denotes electron mobility and W the part of the channel that is depleted such that a-W is the channel opening.

2.2.3 Compact I-V model for SiC VJFET

The blocking and conduction models developed in section 2.2 extend the analytical theory of VJFETs to account for graded channel doping to the first order. By changing the Poisson component of the 2-D field to account for the graded junction, this improved model introduces the extent of grading as a design parameter and uses it to account for the consequent reduction in channel potential barrier. It provides an equation relating channel length to the barrier and other design parameter such that the channel length can be optimally designed for DIBL to coincide roughly with onset of avalanche breakdown.

3. DESIGN OF VJFET, JBS DIODE AND MONOLITHIC INTEGRATION

Analytical models for the design of VJFET and JBS diode were developed in chapter 2. Using these models the switch and rectifier can be designed for optimum operation. Besides these, for the monolithically integrated VJFET and JBS diode, electric field termination regions also have to be designed. In this chapter, the monolithically integrated switch will be designed by combining the analytical models from chapter 2 and TCAD simulations.

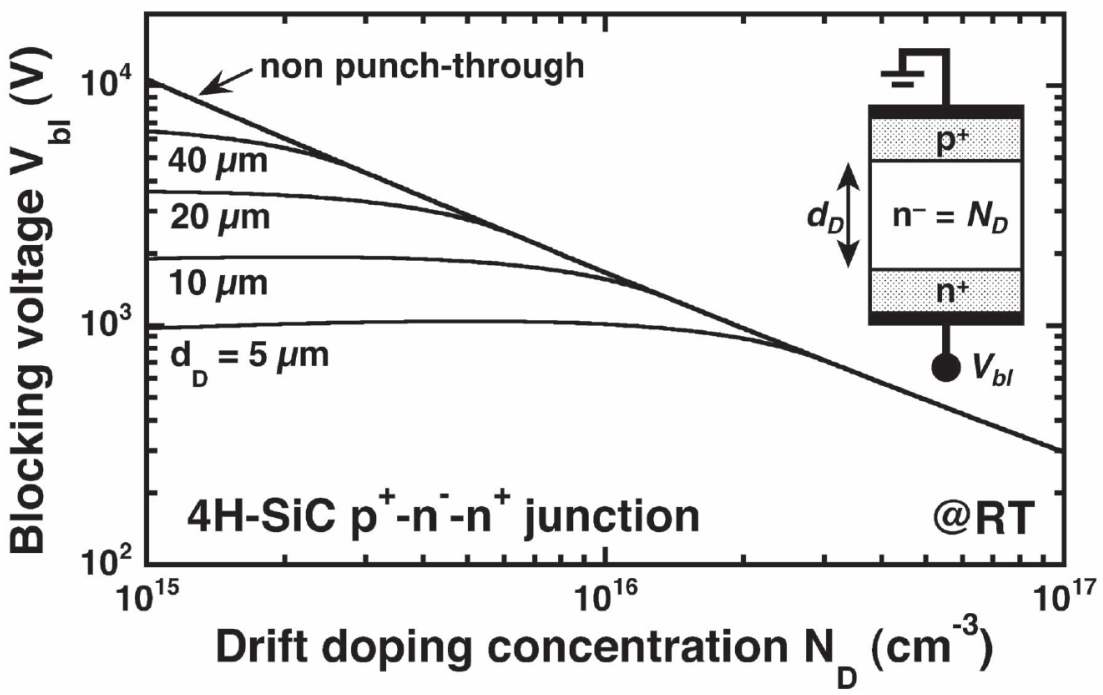

Figure 21Blocking voltage for SiC epitaxial structures [17]

The epitaxial structure of the device is shared between the VJFET and JBS diode and has to be chosen based on the avalanche breakdown capability required from the gate-drain junction of the VJFET. Under the ionization integral formalism [1], avalanche breakdown occurs when the electric field along any path from anode to the cathode increases to such an extent that the integral reaches unity. The coefficients, called impact ionization coefficients, of this integral are very strongly related to the electric field [43].When electric field is high enough (called critical

electric field in a 1-D junction), the criterion for avalanche breakdown is satisfied. From fig. 21, which is based on the impact ionization coefficients reported by Konstantinov et al [44], to block 1200V with some design margin an epitaxial width of 12μm and doping of 7E15/cm^3 will be sufficient.

$$N_D = 7E15/cm^3 - - - (61)$$

$$W_D = 12\mu m - - - (62)$$

3.1 JBS Diode

Let us consider the hypothetical case of designing a diode rated for leakage current less than 100μA at the operational reverse voltage of 800V, maximum reverse blocking capability (as defined by breakdown voltage) of 1500V, forward on-resistance Ron of 50mΩ and forward voltage drop of 1.5V while carrying a current of 10A at room temperature.

Since the required blocking capability is 1500V, using 4H-SiC with a drift layer of doping 7E15/cm^3 and width 12μm, from (16), the maximum electric field at 1500V for such a Schottky diode will be about 2.01MV/cm, which is below the avalanche limit of SiC at this doping level [44]. If we were to choose a Schottky diode with barrier of 0.8eV, then to restrict leakage current below 100μA at a reverse voltage of 800V, its active area cannot be any more than 0.01cm^2 (from (38-40) and fig. 13). But with such a small device, Ron (41-44) is 135mΩ (ignoring contact resistance) and forward voltage (45) at 10A is ~ 1.95V, which are higher than specifications. Instead, if we choose a JBS diode with 2k = 3μm, from (26-40) and fig. 13, the device active area can be 0.1cm2 to have leakage current within specifications. Then, Ron = 16mΩ and forward voltage drop at 10A is ~0.9V, which even adding the resistance and voltage drop at the contact, can be kept well within specifications. It is interesting here to note that while the JBS diode has higher

specific on-resistance than the Schottky diode, its on-resistance is lower because it can tolerate a higher active area while keeping within the leakage current limit. So we have

$$\emptyset_B \approx 0.8eV - - - (63)$$

$$2k = 3\mu m - - - (64)$$

3.1.1 Anode Geometry

In chapter 2, for JBS diodes, a 2-D analytical model was developed which is strictly valid only for anode layouts that have 2-D symmetry like interdigitated stripes. For other 3-D layouts, the 2-D analytical model can be extended using TCAD simulations to form a pseudo 3-D model. To design the best JBS diode, it is also important to compare the different layouts to find the one that gives the best performance.

To compare different layouts of P-N and Schottky junctions at the anode, we propose the figure of merit (λ) - Proportional Schottky area at the anode for a particular maximum Electric field at the Schottky junction (E_{ms}) and particular feature size (c). Higher λ reduces forward resistance for the same reverse leakage current and is hence a better design. At low forward bias, when the voltage dropped in the drift layer is not very significant, the forward current is directly proportional to λ. At higher voltages, the proportionality reduces but current continues to increase with increasing λ. λ is compared for PN and Schottky regions in the anode laid out as *interdigitated stripes, rectangular grid and hexagonal honeycomb* with the Schottky region either inside or outside the polygons. The top-views of these structures are given in fig. 22, which also shows the unit cell for each case. Electric field and current in the unit cell is repeated symmetrically around the whole structure.

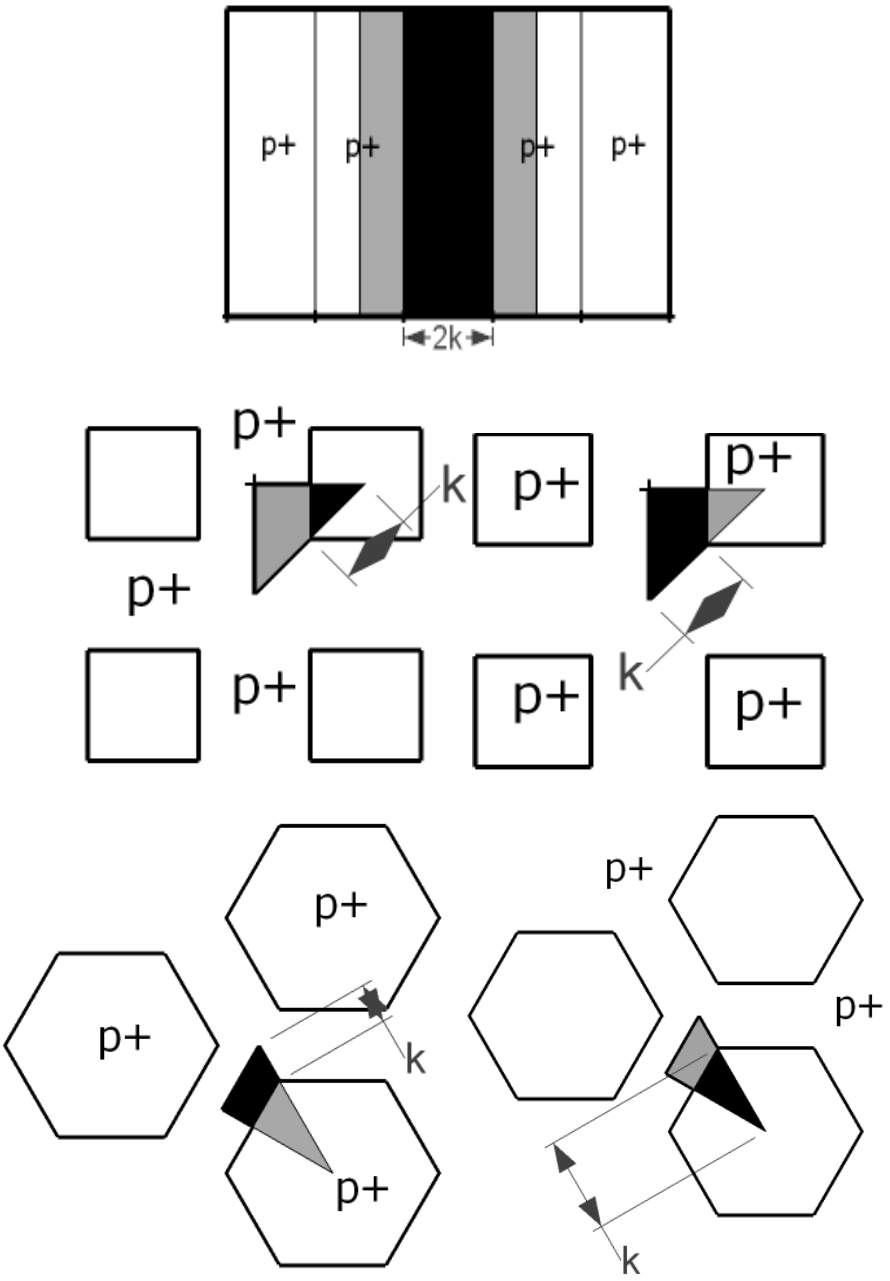

Figure 22 Top views of various anode layouts of JBS diode

To find λ, the relationship between electric field patterns within the unit cells in fig. 22 is necessary. Maxwell's Poisson equation is solved in the cells using the Dessis simulator in Synopsys Sentaurus for a 4H-SiC structure that is otherwise the same in each case. The maximum distance of any point on the Schottky contact from surrounding P-N junctions (k) is varied and the electric field at that point, which is the maximum electric field at the Schottky contact (E_{ms}), is calculated. The variation of

E_{ms} with the Schottky opening (2k) is shown at a reverse bias of 1000V (post-punch through) for an epitaxial structure with carrier concentration of $1X10^{16}cm^{-3}$ and thickness of 10μm is shown in fig. 23.To a first approximation, the horizontal axis (2k) can be scaled by a constant factor, which is shown in table 4, for each layout to have the same E_{ms} as the layout with interdigitated stripes. Analyzing reverse bias before punch-through, the same relationship is observed. When the Schottky junctions are outside the cells in the 3-D layouts, the electric field shielding is less effective for the same k compared to stripes and vice versa for Schottky junctions inside the cells. λ for a particular layout is now the product of the ratio in table. 4 and the proportional schottky area in that layout (α), which can be calculated from geometry as in (65-69).

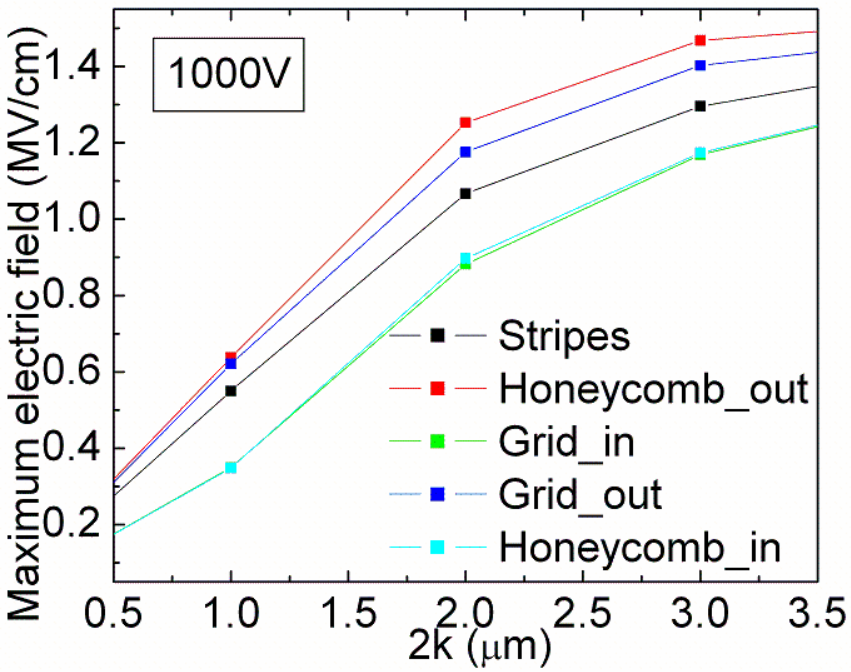

Figure 23 Maximum electric field versus width of Schottky region

$$\alpha_{stripes} = \frac{k}{c+k} - - - (65)$$

$$\alpha_{rectangular_{in}} = \frac{k^2}{(c+k)^2} - - - (66)$$

$$\alpha_{honeycomb_{in}} = \frac{k^2}{(c+k)^2} - - - (67)$$

$$\alpha_{rectangular_{out}} = \frac{2ck\sqrt{2} + k^2}{\left(c\sqrt{2} + k\right)^2} - - - (68)$$

$$\alpha_{honeycomb_{out}} = \frac{4ck\sqrt{3} + 3k^2}{\left(k\sqrt{3} + 2c\right)^2} - - - (69)$$

The figure of merit (λ) for each anode layout, obtained by correcting "k" in the equations for α (65-69) by the relationships in table 4, is plotted in fig. 24.

Layout	$\frac{k}{k_{stripes}}$
Stripes	1
Rectangular (in)	1.28
Rectangular (out)	0.862
Honeycomb (in)	1.3
Honeycomb (out)	0.787

Table 4 Comparison of anode layouts for the same reverse leakage

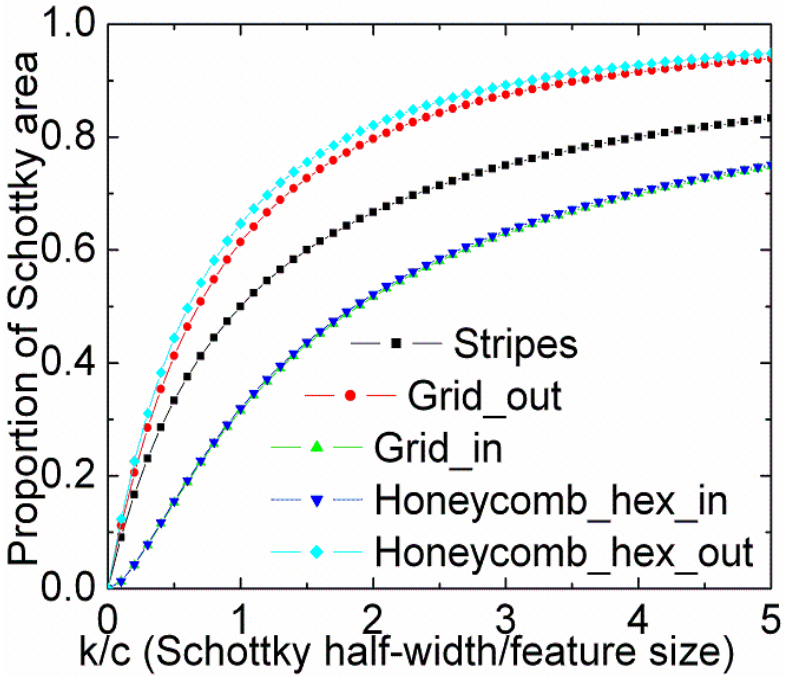

Figure 24 Proportional Schottky area (FOM) of different layouts

The honeycomb layout with Schottky region outside the hexagons has higher λ than the others considered, an improvement of ~20% over interdigitated stripes. The

rectangular grid with Schottky region outside the hexagon follows close behind, which suggests that it is the 3-D layout rather than the exact geometry that improves λ. However, in the 3-D layouts, k is measured from a corner of the implanted region in a diagonal direction rather than from the edges. So, the effect on E_{ms} of uncertainties in fabrication will be magnified compared to that in stripes.

From fig. 24, λ for every layout increases when implanted feature size decreases (i.e. k/c increases). One extreme limit for c is when the p+ regions are just wide enough for the depleted acceptors in it to balance the depleted donors under the Schottky junction, around c/k ~ ratio of carrier concentrations of the drift layer and the implanted p+ layer. However, c is limited well before that by the decreasing breakdown voltage. As c reduces, the curvature of equipotential lines around the p+ implanted region increases (fig. 25), which increases the gradient of electric field near the P-N junction. An approximate analytical solution near the P-N junction yields an inverse relationship between E_{ms} and c for the striped layout and inverse-square relationship for 3-D layouts [45]. Dessis simulations at various c also illustrate this trend. fig. 26 shows electric field across the PN junction in a striped JBS diode for different c compared with the electric field at the Schottky contact at a reverse bias of 1000V. When c = 0.1 μm, the device has already broken down. These results assume abrupt P-N junctions which will not be achieved in practice, especially as c reduces. Yet, the point it illustrates, that reducing c to very low values precipitates onset of avalanche breakdown well below the parallel-plate limit, is applicable in a similar measure to more realistic cases too. Hence, the lower limit of the half-width of p+ implantation should only be around its depth, usually around 0.5 μm.

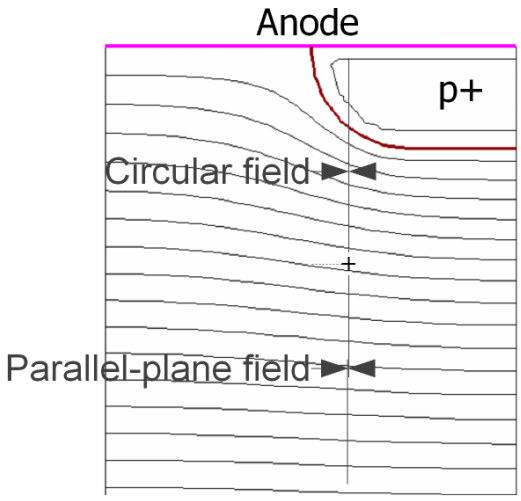

Figure 25 Equipotential lines showing effect of small feature sizes on field

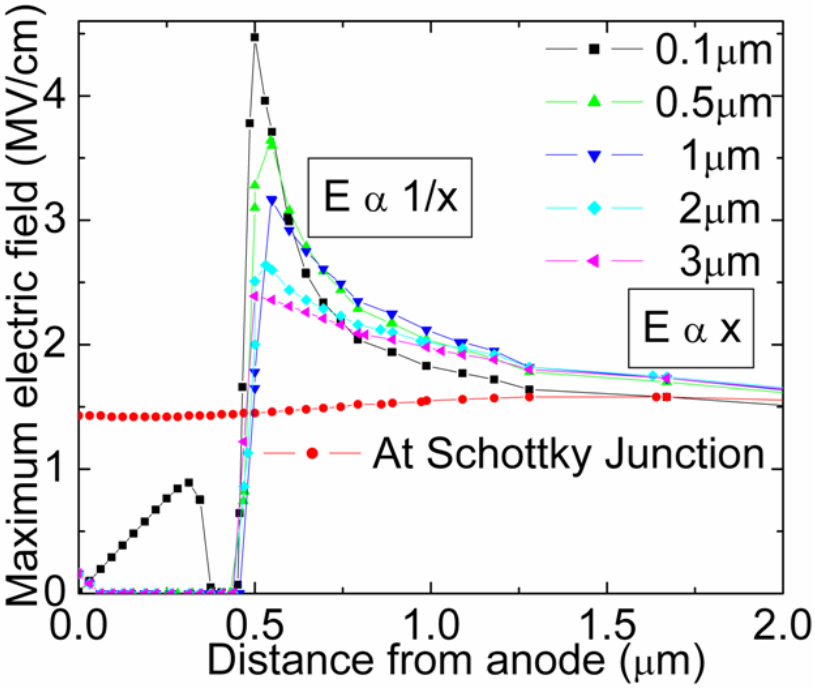

Figure 26 Electric field along a vertical line across the PN junction

From this section, we can use table 4 to extend the 2-D analytical model developed in Chapter 2 for JBS diodes to 3-D geometries. It is clear that 3-D geometries offer better JBS diode performance and that the feature size of p+ implantation should be limited to around the implantation depth [46].

3.2 VJFET

The epitaxial structure of the VJFET and JBS diode has been designed for the desired breakdown capability. In the VJFET, the channel width, doping and length now remain to be designed. In Shockley's 1-D approximation, the carrier concentration in the channel and its width are dependent variables for the same potential barrier in the channel. To avoid an additional epitaxial layer, the channel doping can then be chosen to be the same as that of the drift region unless the consequent channel width will be too small to fabricate. We have seen from figs. 19 and 20 that drain current due to DIBL reaches high values at a channel potential barrier around 0.6V. For normally off operation, we can design the channel to have a potential barrier around 1V at zero drain bias. With $N_{ch} = N_D = 7E15/cm^3$, this gives from (49) and (50),

$$\frac{kT}{q}\left\{ln\left(\frac{N_{ch}N_A}{n_i^2}\right)+ln\left(\frac{N_S}{N_{ch}}\right)\right\}-V_{GS}-\frac{qN_{ch}a^2}{2\varepsilon}\left[1+\frac{4\sqrt{2}}{3}\sqrt{\frac{N_{ch}}{N_A}\frac{(b-a)}{a}}\right]=1-(70)$$

From fig. 16, b-a is approximately 0.1 μm. For a good source ohmic contact, N_S has to be very high so that there is very high tunneling current between the Nickel Silicide contact at the source and the n++ SiC that gives a nearly proportional V-I relationship or an ohmic contact. The gate doping N_A also has to be very high (p++) for work-function matching to nickel silicide at the gate in order to obtain good gate ohmic contact. Substituting $N_S = 2E19/cm^3$ and $N_A = 3E18/cm^3$ into (70), we get a ~ 0.4μm. Substituting this in (54-56) for $V_{DS} > 1400V$ or using figs. 19 and 20, we get l > 1.5μm. So we have

$$a \approx 0.4\mu m - - - (71)$$

$$b \approx 0.5\mu m - - - (72)$$

$$l > 1.5\mu m - - - (73)$$

3.3 Monolithic Integration

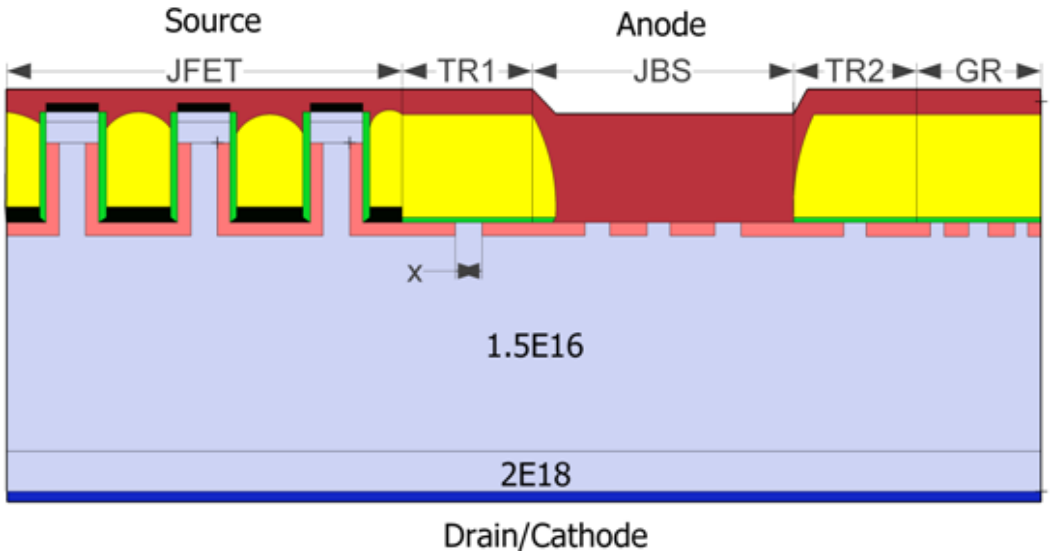

Figure 27 Cross-section of the monolithically integrated device

The method for monolithically integrating the VJFET and JBS diode is shown in fig. 27. The color scheme is- blue for the substrate and epitaxially grown semiconductor, black for Nickel Silicide, pink for ion-implanted regions, green for thermally grown oxide, yellow for other dielectric and brown for the source and diode overlay metal. The source and anode are shorted using overlay metal. “x” in fig. 27 is the width of successive un-implanted rings that are used to terminate field effectively in the gate-anode region.

Since the gate of the JFET and anode of the diode are on the same layer, the major design challenge is to allow the two to take different potentials (avoid shorting) while also largely sharing the same edge-termination. An extreme solution would be to provide for termination of the entire gate-drain and anode-cathode voltages separately in the region between the JFET and diode (TR1 in fig. 27). Then, the surface potential along a line from gate to anode during blocking will rise from gate potential to drain potential and fall back to anode potential. However, this doesn’t take full advantage of the promise of monolithic integration and increases chip area

unnecessarily. Since anode is shorted to source, the transition region blocks the gate-source voltage, which is only around 3V for normally off and under 10V for most normally on TI-VJFETs.

The transition region is designed using successive p+ and n- field rings. While the highly conductive p+ rings equate potential around them, the spacing between them (x in fig. 27) should be large enough that the gate-anode potential barrier is not reduced significantly even at the highest gate-source voltage difference. From a drift-diffusion perspective, the gate-source leakage current through the transition region increases exponentially with reducing barrier height. This was seen also in figs. 19 and 20 where leakage across a barrier increases significantly when it falls to around 0.6V. However the spacing between rings also has to be low enough that surface potential in this region doesn't rise too high with increasing drain voltage. The SDEVICE simulator in Synopsys TCAD Sentaurus was used to simulate I-V curves for the structure. Fig. 28 shows potential contours in a design with two rings of optimized spacing where drain voltage is 850V but surface potential in the transition region is only around 20V. Fig. 29 shows earlier onset of avalanche multiplication as x, and consequently, the surface electric field in the transition region, increases. Maximum blocking voltage is obtained at $x \leq 0.9$ μm. From fig. 30, gate-source leakage increases intolerably below $x = 0.9$ μm, at which increasing the number of rings limits leakage current. Using two rings, gate-anode blocking capability can be increased to 15V without compromising drain blocking capability.

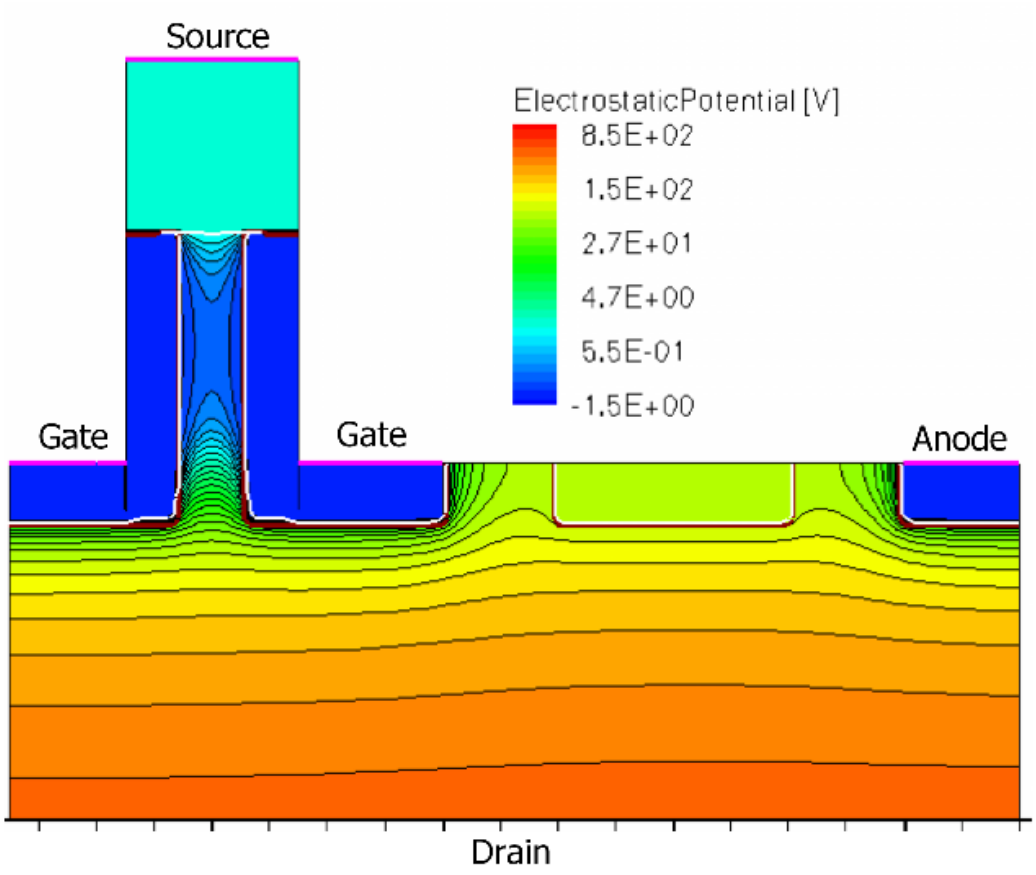

Figure 28 Potential contours in blocking more in the transition region

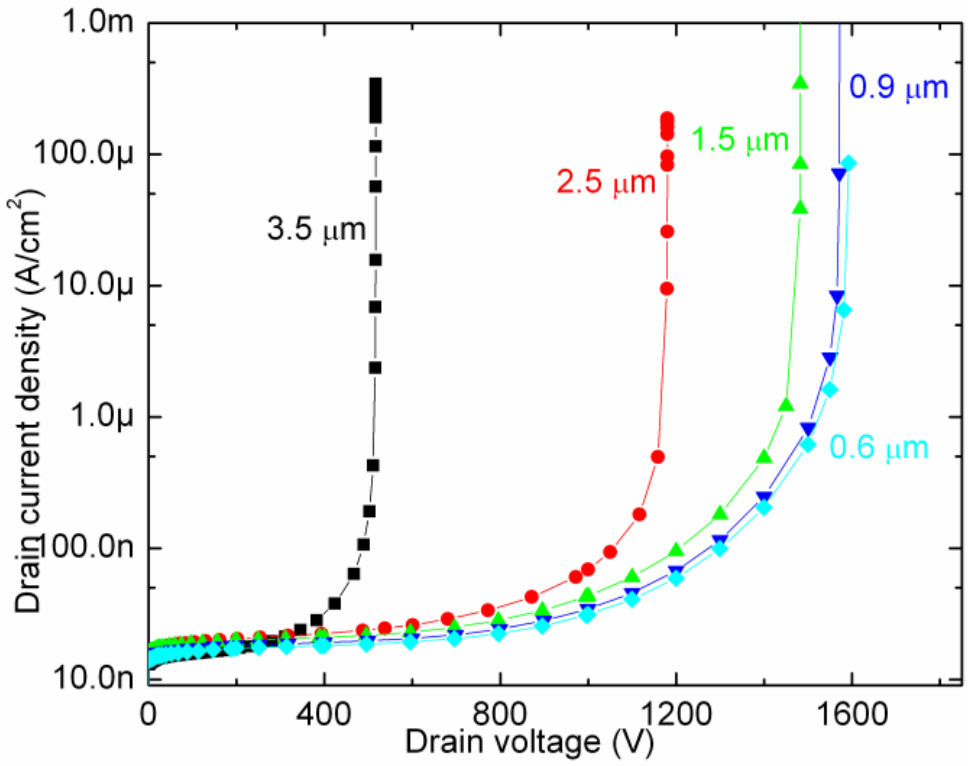

Figure 29 Drain leakage current for different spacings between transition rings

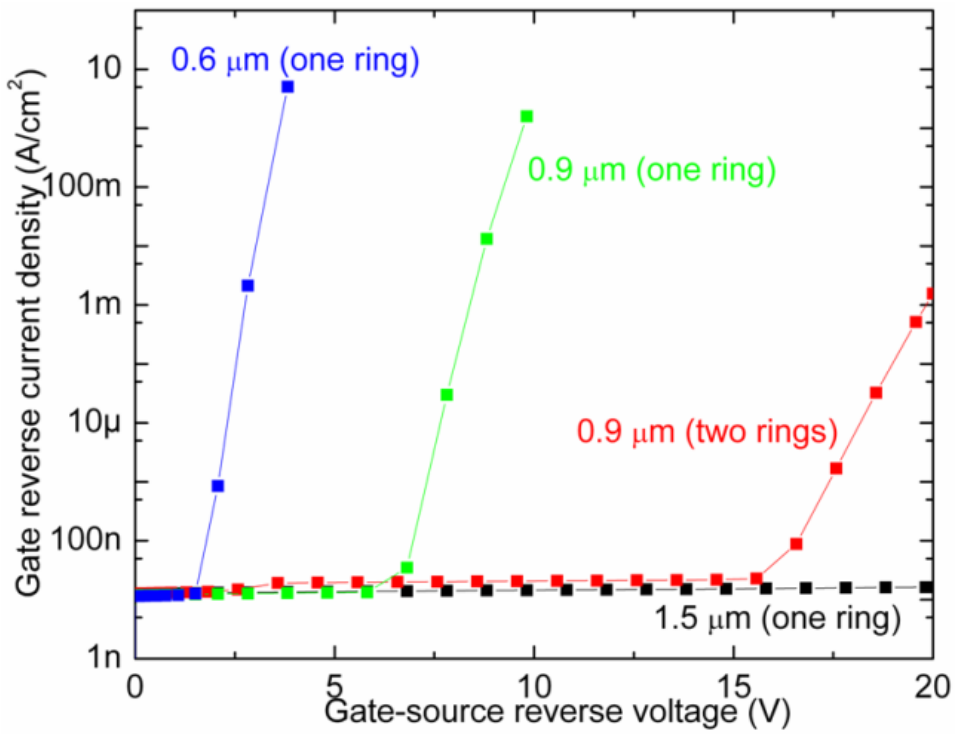

Figure 30 Gate-source reverse leakage cureent for combinations of transition rings

The electric field pattern in the transition region is different from that at guard rings used for edge termination because in the former, the field is terminated in opposite directions from gate and anode. This reversal of surface electric field is evident from the increase and then decrease of potential as we move from gate to anode in fig. 4. So we need at least two rings with

$$0.6\mu m < x \leq 0.9\mu m --- (74)$$

For margin, the device is designed with 4 un-implanted rings, each 0.9 μm wide, between the JFET and the diode; ensuring good gate-anode isolation while also terminating the field from gate and anode [47].

3.4 Edge-Termination

The broad categories of edge termination schemes in power devices were discussed in section 1.6. For the VJFET, dimension-sensitive schemes are more

advantageous because it can then be combined with the p++ gate implantation step without care for implantation dose. The monolithically integrated switch in this thesis is designed with non-uniform implanted field rings or guard rings for edge termination. This involves high dose p+ implants separated by un-implanted regions that block voltage. The p++ regions being highly conductive don't support any voltage but they serve to equalize potential around the ring and hence make the potential contours 1-D (depending only on distance from anode edge).

Distance between successive implanted rings is critical because the un-implanted regions support the potential drop. If this distance between two rings is too large, then successive guard rings are not coupled with each other and breakdown happens at the inner ring. If the distance is too small, then the ability of one un-implanted region to support potential reduces and more rings will be required to support the whole voltage, thus increasing chip area unnecessarily. Optimum spacing between rings is at least a 2-D problem for which analytical models have been proposed [26, 48]. At the corners of the device, the electric field patterns are 3-dimensional which makes optimum design even more complicated [49]. However, if the corner is rounded with radius at least 10-20 times the implantation depth, then the effect of the azimuthal angle in the design problem can be minimized and the analysis restricted to 2 dimensions (vertical dimension in the direction of current flow and horizontal direction away from the edge of the anode).

Multiple guard rings are necessary to reduce the sensitivity of the design to variation in dimension. It is desirable to share the potential drop nearly equally across each of these rings such that the electric fields at all junctions are nearly equal below the critical field. If each successive spacing is of the same dimension, then the electric field at the innermost guard ring junction will be the highest and it will decrease

towards the edge. However, if the spacing between implanted rings increases away from the edge of the anode, the maximum electric field at successive junctions can be made nearly equal [50]. Fig. 31 from [50]shows edge termination using 4 guard rings with non-uniform spacing increasing outward from the edge of the anode. It can be seen that the electric field at all the PN junctions are nearly equal both at the surface and in the bulk of the semiconductor.

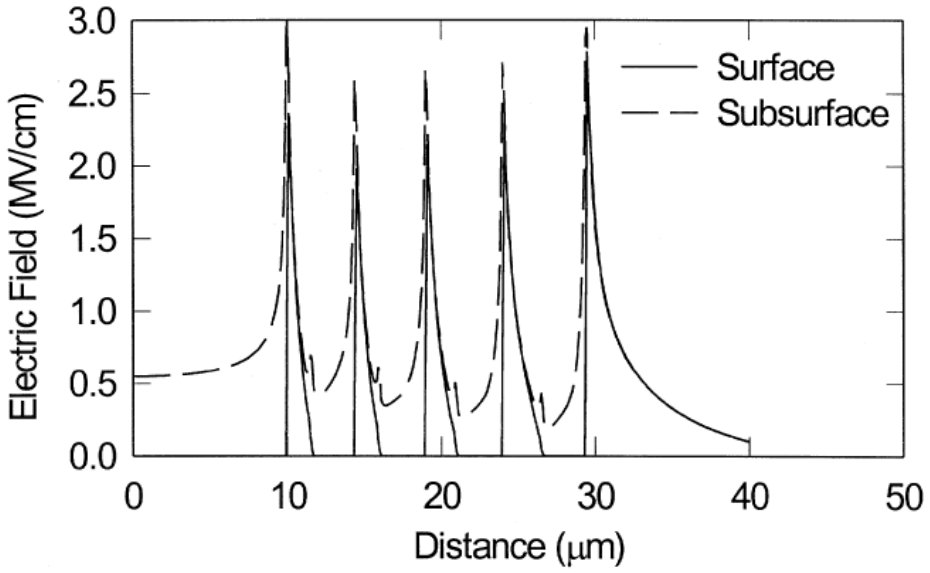

Figure 31 Electric field in non-uniform guard ring termination [50]

TCAD simulations were used to design an optimized guard ring structure for 1200V SiC devices as shown in fig. 32. There is a 16μm wide region between the active area and edge-termination to provide margin for mask alignment. The implanted rings, chosen to be as narrow as practically possible to fabricate, are all 1μm wide. The spacing between rings increases from 1.5μm to 2.9μm. These 14 rings are enough to support the required voltage if the dimensions are accurate. As a safety margin, 6 more rings at a spacing of 2.9μm are added.

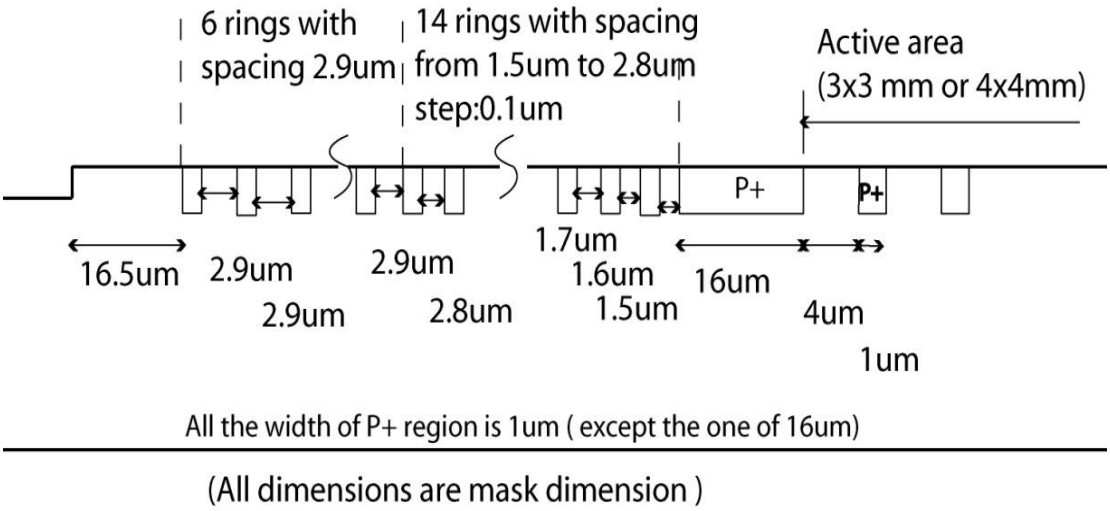

Figure 32 Cross-section of guard rings to block 1200V

The monolithically integrated VJFET and diode is designed to be fabricated with the VJFET at the center, 4 un-implanted field rings between the VJFET and JBS diode, an annular JBS diode region and finally guard rings outside the diode for edge termination as shown in fig. 32.

4. FABRICATION

The monolithically integrated power switch designed in chapter-3 of this thesis was fabricated in the Microelectronics Research Laboratory (MERL) cleanroom at Rutgers University. Photomasks for various lithographic steps in the process were designed using the computer program AutoCAD from Autodesk Inc. licensed to Rutgers University and manufactured to specifications at Photo Sciences Inc. SiC substrates with epitaxially grown layers suitable for device fabrication were provided by Dow Corning Corporation under a sub-contract of ONR contract N00014-08-C-0398 administered by Dr. P. Maki. This chapter details the various steps in the fabrication of the SiC integrated switch.

4.1 Mask Design

The mask was designed to repeat the basic block in fig. 33. It contains one large integrated device of active area 0.095cm^2 which includes about 0.061cm^2 of JFET active area and 0.028cm^2 of diode active area. Including the termination region, the chip area of this device is around 1.25cm^2.

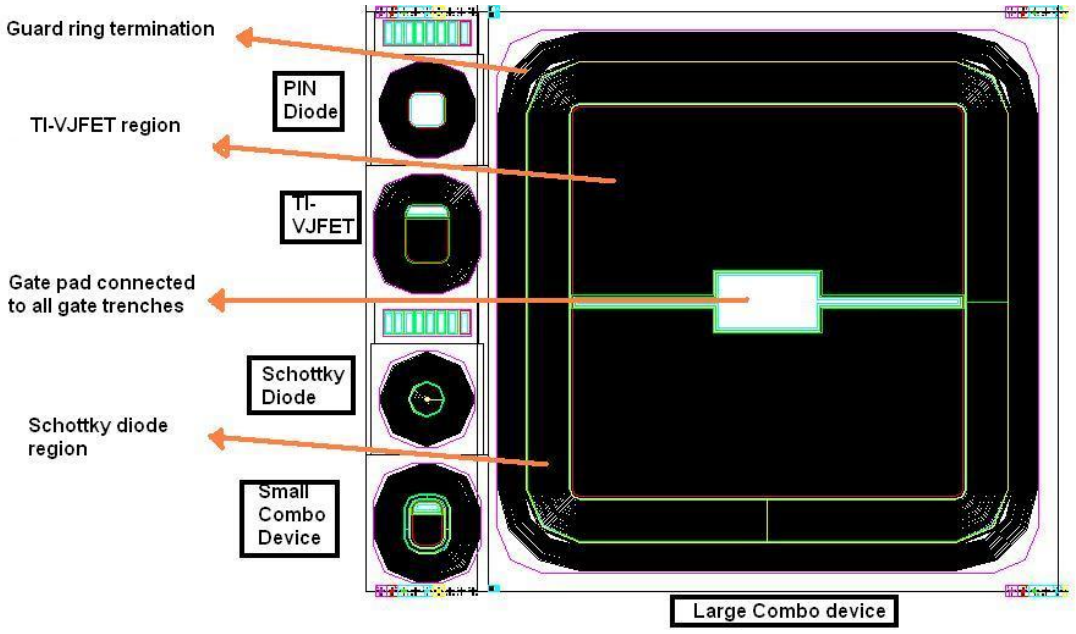

Figure 33 Fundamental block of devices on mask for fabrication

Besides the large device, there is a small-area integrated switch of active area 0.0011cm^2, a Schottky diode of active area 0.000314cm^2, a VJFET of active area 0.0012cm^2 and a PN diode of active area 0.00061cm^2 and TLM patterns to find the specific resistances of source and gate ohmic contacts. These devices are formed using multiple mask layers dictated by the steps in their fabrication process.

The VJFETs in the integrated device are designed on the mask to have 3 different channel openings (0.5µm, 0.7µm and 0.9µm) such that both normally off (at ~0.6m) and normally on operation might be achieved. The JBS diodes are designed to have Schottky opening (2k) of 2µm and 3µm.

There are 5 masks in the fabrication sequence-

1. **Source mesa**

   This mask etches the source mesas and gate trenches in the JFET

2. **Implantation**

   This mask forms the PR mask for Al implantation to form the gate and p+ regions in the JBS diode and guard rings.

3. **JFET window**

   This mask opens the JFET window for source and gate ohmic contact formation.

4. **VIA window**

   This mask opens the gate-pad and anode regions to deposit metal there.

5. **Metal overlay**

   This mask opens the source, anode and gate pad to deposit overlay metal there.

4. **2 Wafer Structure**

The epitaxial structure of the wafers used for device fabrication is shown in fig. 34. Over the n+ substrate, 4 n-type epitaxial layers are grown. The first layer is n-doped at 1.5E16/cm^3 and is 11µm thick, designed to support over 1200V when the

device is blocking. The second layer, which will form the channel of the VJFET is 2.5µm thick and n-doped at 6E16/cm^3. The third layer is n+ doped at 3E18/cm^3 and is 1µm thick. This will form an inter-layer between the gate and source of the VJFET. The 1µm thick layer n++ doped at 2E19/cm^3 is the source where ohmic contact can be formed.

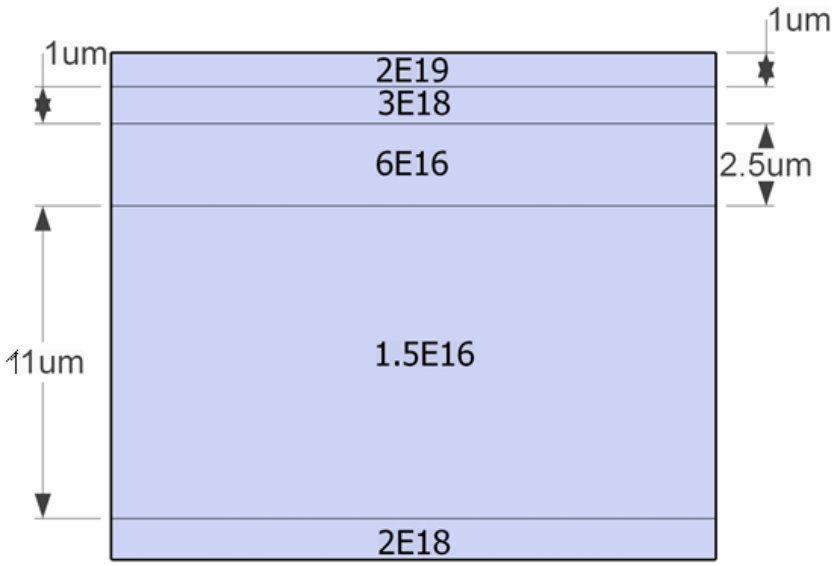

Figure 34 Cross-sectional view of the wafer (not to scale)

Secondary Ion Mass Spectroscopy (SIMS) results on the epitaxial layer of the wafer are shown in fig. 35 to correspond closely to specifications in fig. 34. The succeeding sections will cover fabrication steps on this wafer.

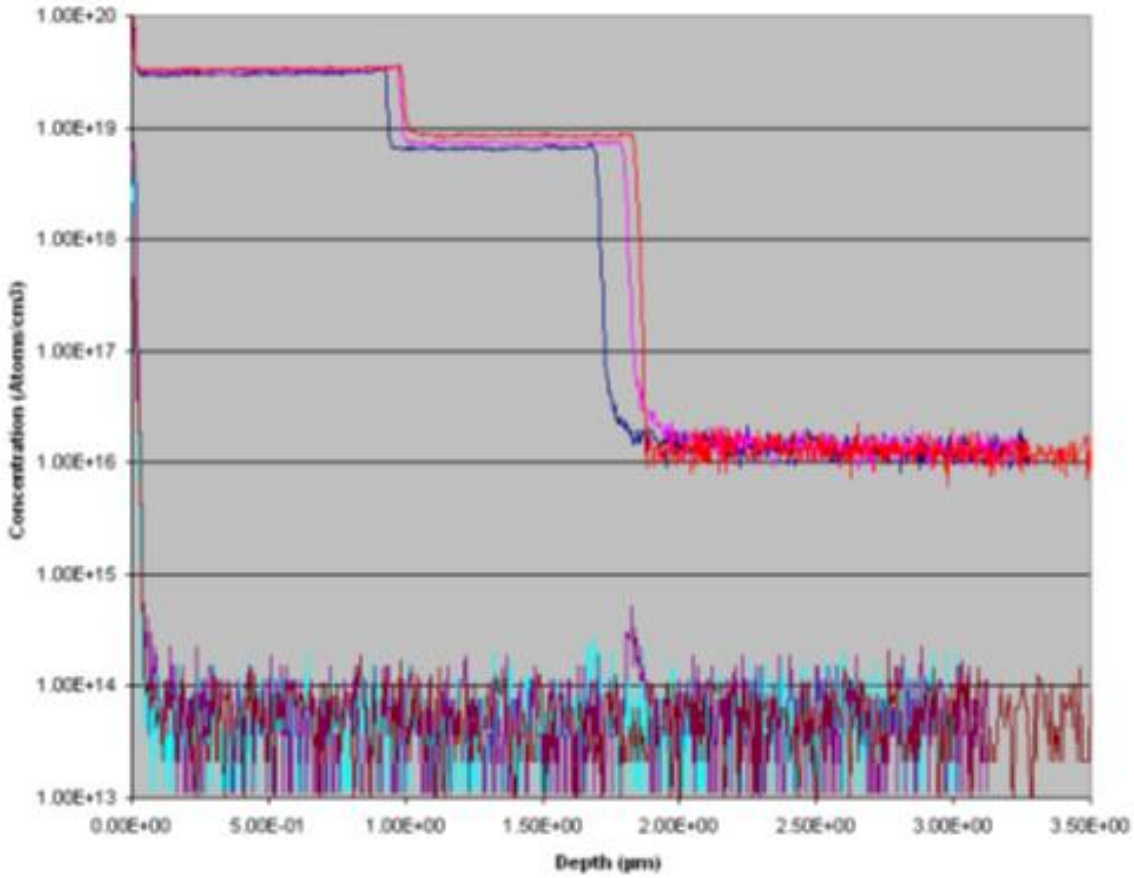

Figure 35 SIMS results on Al concentration in the epitaxial layers

4.2 Source Mesa Etching

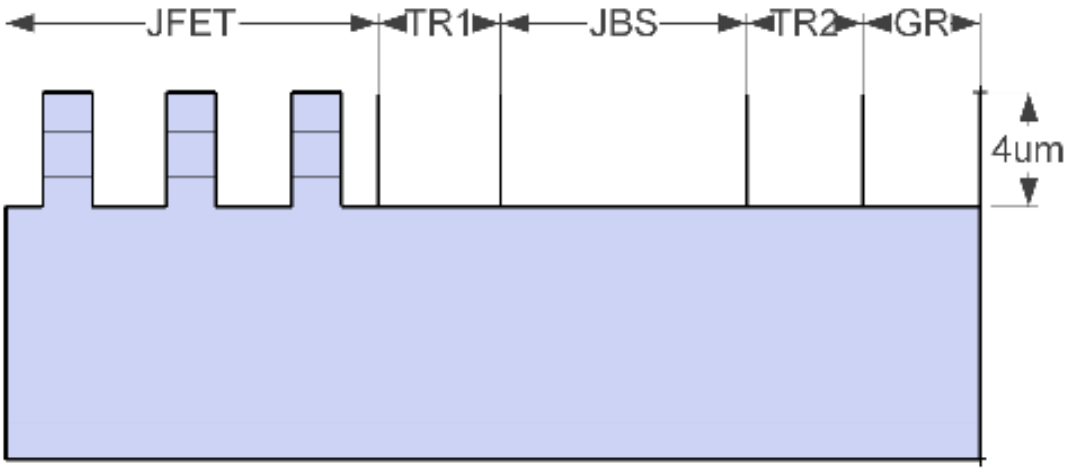

Figure 36 Cross-section after source mesa etching

In this step, SiC will be etched to a depth of about 4μm under such a mask that in the JFET areas, there will be 4μm high mesas on top of which the source will be

formed. The depth of etching will high enough to expose the n- region at the bottom of the trenches In the diode and termination regions, etching will be unmasked such that n- SiC can be exposed that will more readily form a good rectifying contact with typical Schottky metals like Ti than n+ SiC. The cross-section of the wafer after this process is sketched in fig. 36.

After cleaning the wafer with acetone, basic RCA ($NH_4OH+H_2O_2+H_2O$ 1:1:5) in water bath at 80C for 30', acidic RCA ($HCl+H_2O_2+H_2O$ 1:1:5) in water bath at 80C for 30'and 5% HF in ultrasound water bath for 10', 3000A of AlTi (96.5% Al) is sputtered on the wafer. Then, the "source mesa" mask is used to pattern photoresist (PR) 5214E on the wafer. PR is hard baked at 130C for 30' and wet etched using Al etchant II with surfactant to remove Al from the regions that will form the gate trenches. The photoresist is removed using AZ400T at 80C in a water bath. Then, the SiC wafer with the metal mask is subjected to Inductively Coupled Plasma (ICP) etching with O_2 and CF_4 in the Bosch Process [51, 52] to obtain around 4µm deep highly uniform trenches in SiC. An SEM view of the source mesas and gate trenches obtained by this process is shown in fig. 37.

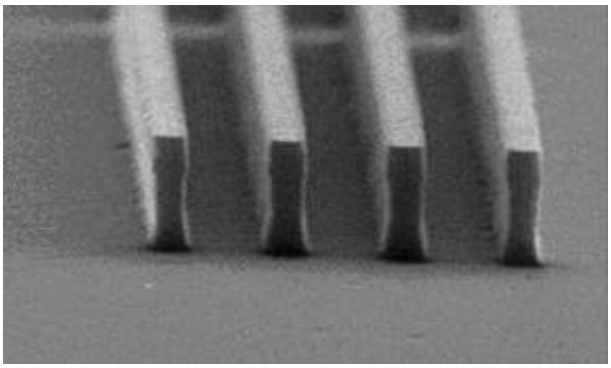

Figure 37 SEM view of trenches in SiC obtained after ICP Bosch etching

4.3 Ion Implantation

Epitaxial regrowth during processing is a cumbersome process. The hardness of SiC also renders doping mechanisms like diffusion impractical. So, ion

implantation is the preferred method of forming device junctions on SiC. Gate needs to be formed at the sidewall and bottom of the trenches. Gate at the trench bottom needs additionally to be able to block the high gate-drain voltage when the device is off. Imlantation conditions were simulated using Profilecode [42] and carried out at Leonard Kroko Inc. The energies and doses used for implantation are shown in table 5. The result of Profilecode simulation for these energies is shown in fig. 16 in chapter 2. The conditions have been chosen to satisfy the twin demands of an implanted carrier concentration around p+ 3E18/cm^3 and depth of implantation around 4000A.

After source mesa etching, PR 4400 was patterned on the wafer using the implantation mask which opens the entire JFET region and parts of the transition, JBS diode and guard ring regions. The PR is them cured by electron beam to harden it to serve as a mask for Al ion implantation. Electron beam curing, while hardening the PR does not deform it like thermal curing does. Since dimensions are very important in the JBS diode and guard ring region, PR patterning and curing are very critical steps of the process. The wafer is now ready for ion-implantation.

The conditions in table 5 are carried out at room temperature. The side-wall implantation (steps 1-2) is carried out first with the sample titled 30 degrees from the vertical. This tilt angle is chosen to be high enough to achieve the required dose normal to the side-wall but also low enough that the implanted ions will reach the bottom of the side-wall under the particular aspect ratio of the trenches. Such tilted implantation is done once each from 4 different sides 90 degrees apart from each other. Subsequently, vertical implantation is used to form the p++ doped gate at the bottom of the trench.

	Ion	Energy (KeV)	Dose (cm^{-2})	Beam angle
1	Al	185	2.2×10^{13}	**Tilt angle** = 30^{o} from the direction normal to the sample surface **Rotation angle** = Four (4) directions: 0^{o}, 90^{o}, 180^{o}, 270^{o} with respect to the wafer major flat. Each implantation needs to be repeated at the four directions
2	Al	120	1.2×10^{13}	
3	Al	360	1.8×10^{13}	**Tilt angle** = 0^{o} (normal to the sample surface)
4	Al	260	6.0×10^{13}	

Table 5 Sequence of Al ion implantation into SiC to form p+ gate

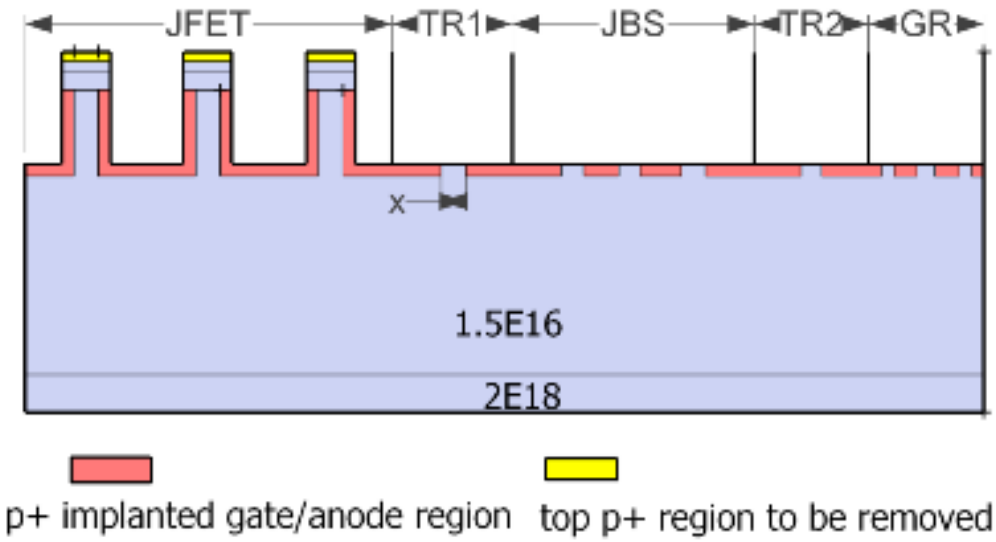

Figure 38 Cross-sectional view after ion-implantation

After ion implantation, the cross section of the device is shown in fig. 38. During the vertical implant, besides the gate, the implanted rings in the transition regions, JBS diode and guard ring region are also formed. Moreover, the tops of the source mesas are un-intentionally implanted by p-type Al ions to a depth of nearly

5000A. This implanted region has to be removed such that source metal contact can be formed here. PR 5214E is spun on the wafer and baked such that the PR thickness is lower on the mesa tops than inside the trenches. Then, the PR is etched isotropically (400W, 0V) in ICP with CF_4 at 10 sccm and O_2 at 20 sccm at a pressure of 10 mtorr to expose the mesatops. Around 4500A-5000A of SiC is etched from the mesa top in ICP anisotropically (200V, 300W) with CF_4 at 10 sccm and O_2 at 20 sccm at a pressure of 10 mtorr to expose n++ source. This is confirmed by electrical tests that show basic rectifying I-V performance between gate and source. The cross-section of the device is now as shown in fig. 39.

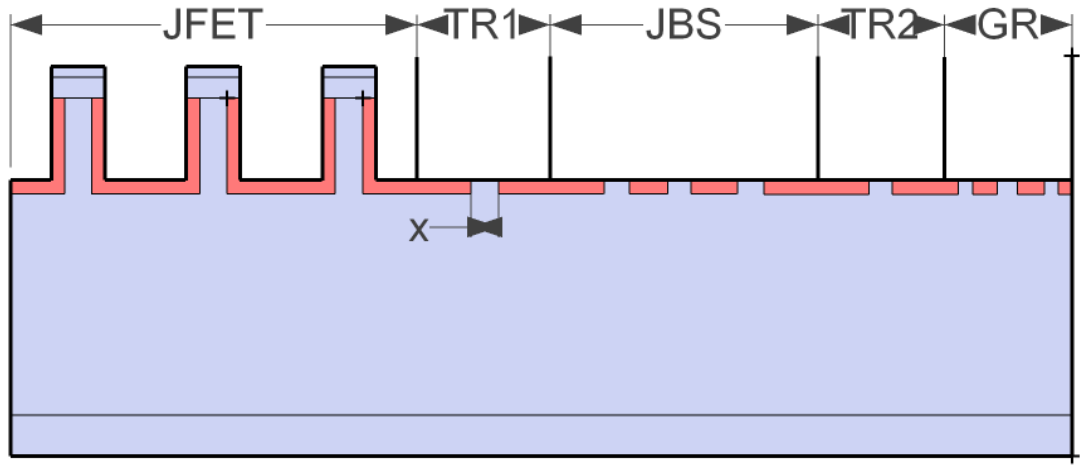

Figure 39 Cross-section after removing p-implanted mesa-top

4.4 Passivation

Charges on the side-wall or in the termination region can affect the performance of the device. It can reduce the efficacy of the inter-layer dielectric and increase gate-source leakage current. It can also change the electric field patterns in the guard ring region and de-optimize the field termination. So, the non-active surfaces of the device have to be “passivated” such that there aren’t any impurities or charges at these surfaces. Silicon dioxide is thermally grown on the entire wafer in an oxidation furnace with dry oxygen. Then, this thermal oxide, also called sacrificial

oxide is removed using HF_4 and the freshly exposed SiC surface re-oxidized in wet oxygen environment for 2 hours at 1100C to grow around 200A-300A of SiO_2. This SiO_2 is annealed in Ar ambient at 1100C for 1 hour and then PECVD Silicon Nitride is deposited on the wafer to protect it from environmental degradation. Both the front and back side of the wafer are now completely covered with dielectric.

4.5 Ohmic Contact

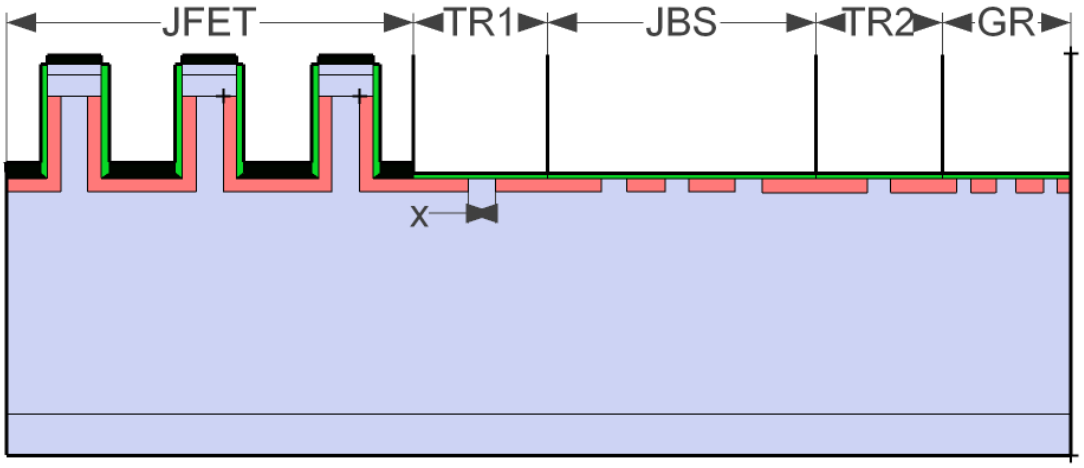

Figure 40 Cross-section after formation of gate and source ohmic contacts

The JFET window mask is used with PR 4400 to open just the JFET region and Silicon Nitride is etched isotropically in ICP (0V, 400W) with CF4 at 40sccm to remove it from the VJFET area. Then, 2000A of PECVD SiO_2 is deposited and etched anisotropically (200V, 300W) in ICP with CF_4 at 40 sccm to remove it from the source mesa tops and trench bottoms while keeping SiO_2 on the side-walls. 1000A of Ni is then sputtered and annealed in a Rapid Thermal Annealing (RTA) furnace at 750C for 3'. This forms Nickel Silicide where Ni is in contact with SiC and Ni remains unreacted where it is in contact with SiO_2. Then, the wafer is subjected to Ni etchant which removes the Nickel from the side-walls and from outside the JFET region but doesn't remove the Nickel Silicide. So, Nickel Silicide is formed on the source and gate without the two contacts being shorted to each other.

However the Nickel Silicide contacts now formed on gate and source are not yet ohmic contacts. This, as well as the lack of shorting between gate and souce can be confirmed now by an I-V test. Then, 250A of AlTi and 3000A of Ni are sputtered on the back side of the wafer to form the drain contact. Then, the wafer is annealed at 1000A in the RTA furnace for 5' to form gate, source and drain ohmic contacts. At this stage, basic 3-terminal switch action is confirmed from the VJFET. The cross-sectional view of the device after forming ohmic contacts is shown in fig. 40.

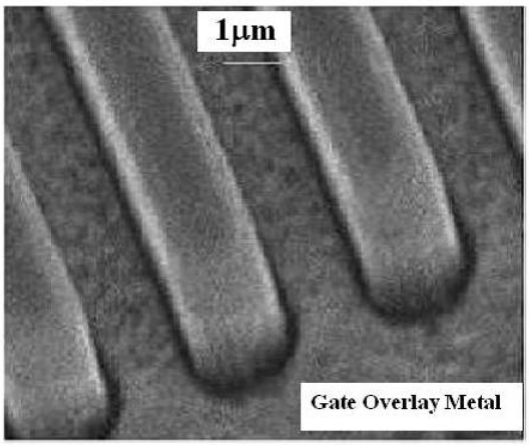

Figure 41 SEM view of mesas after depositing gate overlay [52]

Then, further gate metal is added to decrease gate spreading resistance. 250A of AlTi+5000A of Mo+250A of AlTi are sputtered on the wafer and then patterned using PR and the JFET window mask such that it remains only on top of the gate. For this purpose, the JFET window mask is first used with PR5214E to leave PR just the VJFET region. Then, PR5214E is spun and etched back in a process similar to section 4.3 to expose just the VJFET source while leaving PR in the gate trenches and gate pad. Metal from all but the gate is then removed using Al and Mo etchant. This process should only add gate metal below the p+ implanted side-wall as otherwise gate-source leakage current will increase intolerably. Fig. 41 shows an SEM image of VJFET source mesas and gate trenches after the latter has been partially filled by overlay metal.

4.6 Trench Filling & Planarization

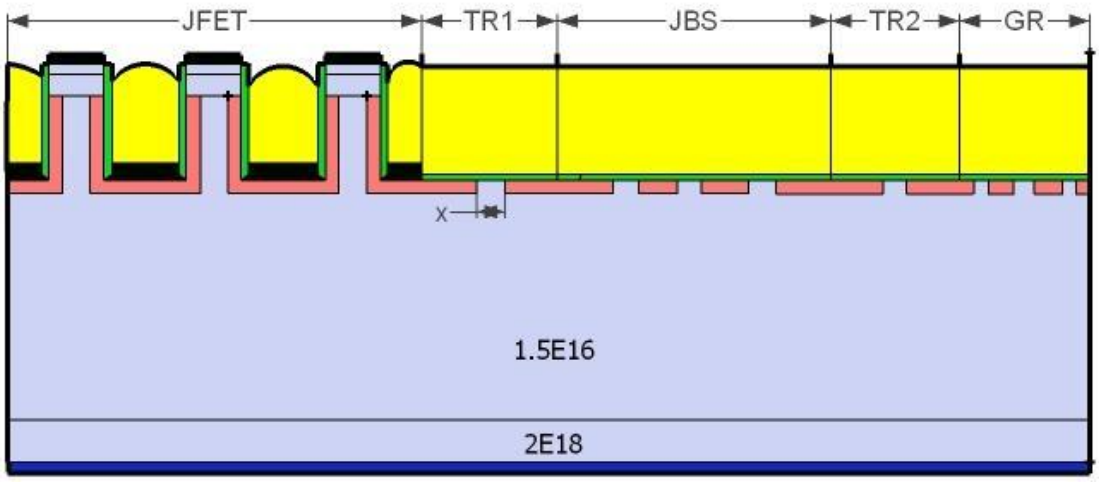

Figure 42 Cross-section after filling VJFET trenches with dielectric

When overlay metal is deposited on the source to connect various fingers, there should be some dielectric filling the gate so that the source and gate are not shorted by this metallization. For this purpose, a polyimide based trench filling process is used. Two rounds of polyimide PI 2562 are spun on the wafer and hard-baked. Then, it is cured at 400C in Argon ambient for 1 hour. The top surface of the VJFET is planarized nearly fully by this process. Then, polyimide is etched back in ICP using O_2 plasma or a combination of O_2 and CF_4 to expose the source. At this point, the source and drain are open but the gate and anode are covered with dielectric. A cross-sectional view of the device after filling VJFET trenches is shown in fig. 42 with the gate dielectric in yellow.

4.7 Overlay Formation

The VIA window mask is used with thick PR4400 to open the gate pad and anode. The polyimide, PECVD Silicon dioxide, Silicon Nitride and Thermal Silicon dioxide are removed by plasma etching in ICP to expose the n- Schottky surface at the anode and gate metal at the gate pad. The cross sectional view of the device at this stage is shown in fig. 43.

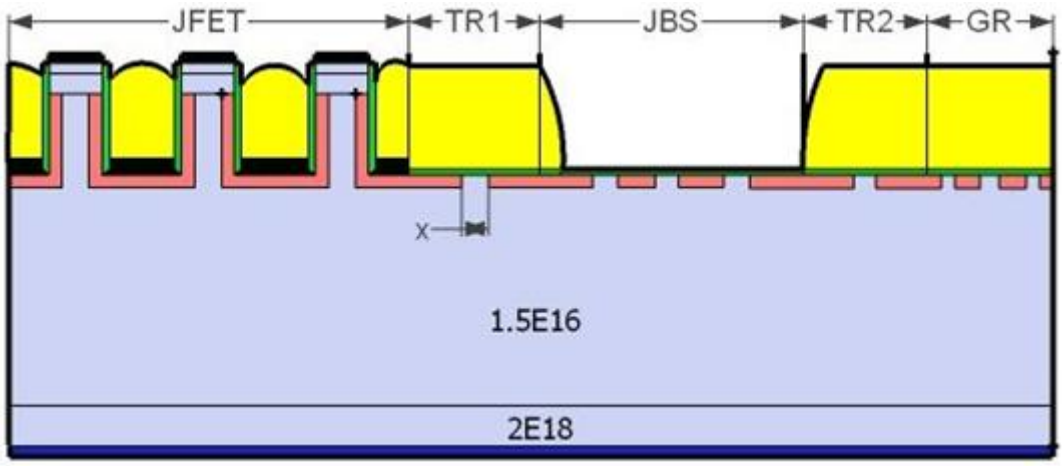

Figure 43 Cross-section of the device just before final metallization

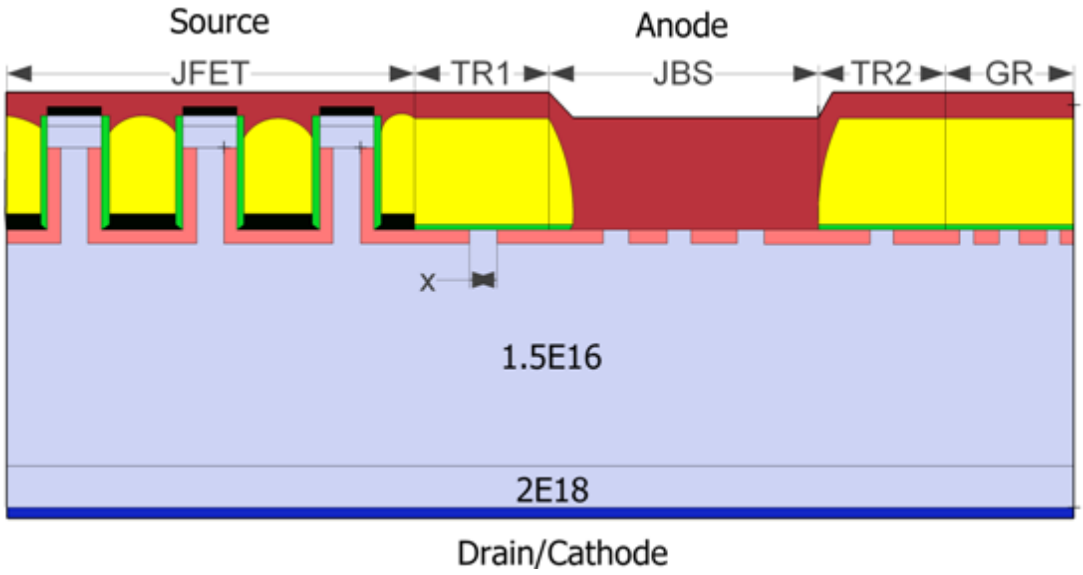

Figure 44 Cross-section of the fabricated integrated switch

Then, the metal overlay mask is used to pattern PR to separate the source & anode from the gate and 800A of Ti and 5µm of Au are sputtered on the wafer. Ti is chosen so that we obtain a Schottky barrier ~0.8eV in the diode. The PR is lifted off in AZ400T at 80C such that gate and anode/source are not shorted. This completes the fabrication process of the integrated switch and the final cross-sectional view is shown in fig. 44. Top view of a fabricated device is shown in fig. 45 with the constituent elements labeled. Fig. 46 shows a picture of a finished 3" SiC wafer with many monolithically integrated power VJFET and JBS diodes.

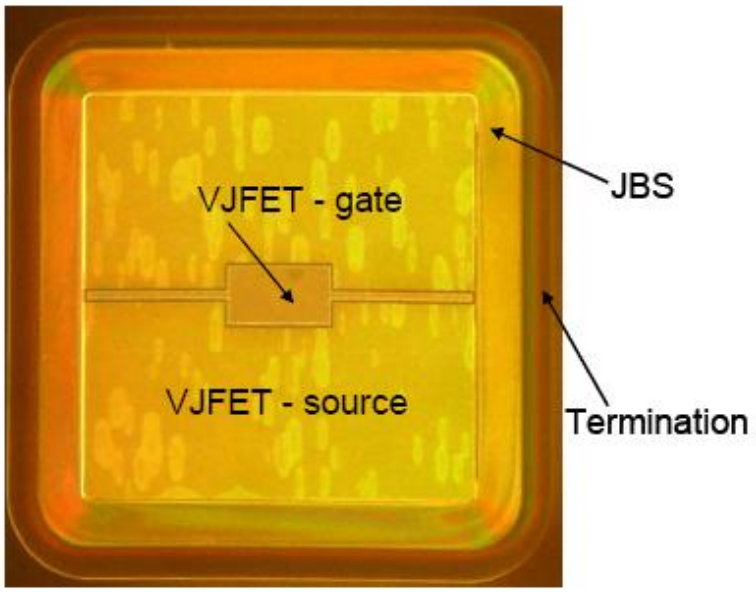

Figure 45 Top view of the integrated switch showing layout of constituent elements

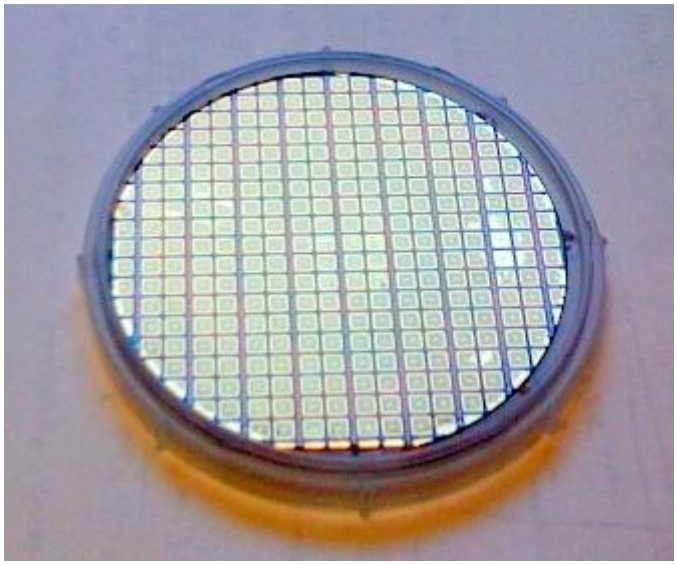

Figure 46 Optical photo of a 3" SiC wafer after device fabrication

5. CHARACTERIZATION AND MODELING

The fabricated device is characterized for its properties in power circuit operation. These include the blocking voltage, on resistance, switching speed and variation of properties with temperature. Static pulsed I-V curves are measured [53]with Tektronix 371A high power curve tracer, Glassman high voltage power supply and Kiethley 6517A electrometer. Temperature characterization is conducted by clamping the wafer to a hot plate whose temperature is measured using a thermocouple arrangement. The switching tests are conducted using Lemsys TRD 0225, which has a built-in gate driver. This chapter covers first the results from device characterization, then TCAD modeling of the devices based on measured device parameters and finally the results of TCAD simulations based on these models to evaluate the electrical advantages of various methods of monolithic integration.

5.1 Static Characteristics

Since VJFETs were designed with different channel lengths, both normally on and normally off devices are expected. I-V curves of a normally-on device are shown in fig. 47. The conduction curves are more clearly shown in fig. 48, which also includes gate current controlled curves. When the gate is fully turned off at V_{gs}= -4V, the device is measured up to 498V at a leakage drain current of 10mA/cm^2. Under this condition, the power dissipation is 4.98W/sq.cm. When gate voltage is increased above 2.5V, the channel is completely open and specific on-resistance is around 7.806 mΩ.cm^2. The conductive power dissipation here is 78.06W/cm^2 (100A/sq.cm at 7.806 mΩ.cm^2). So the power dissipation during blocking is 6.38% of that at conduction, which indicates that 10 mA/cm^2 is not too high a leakage current. The ratio of off-state to on-state current for this switch is 1:10,000.

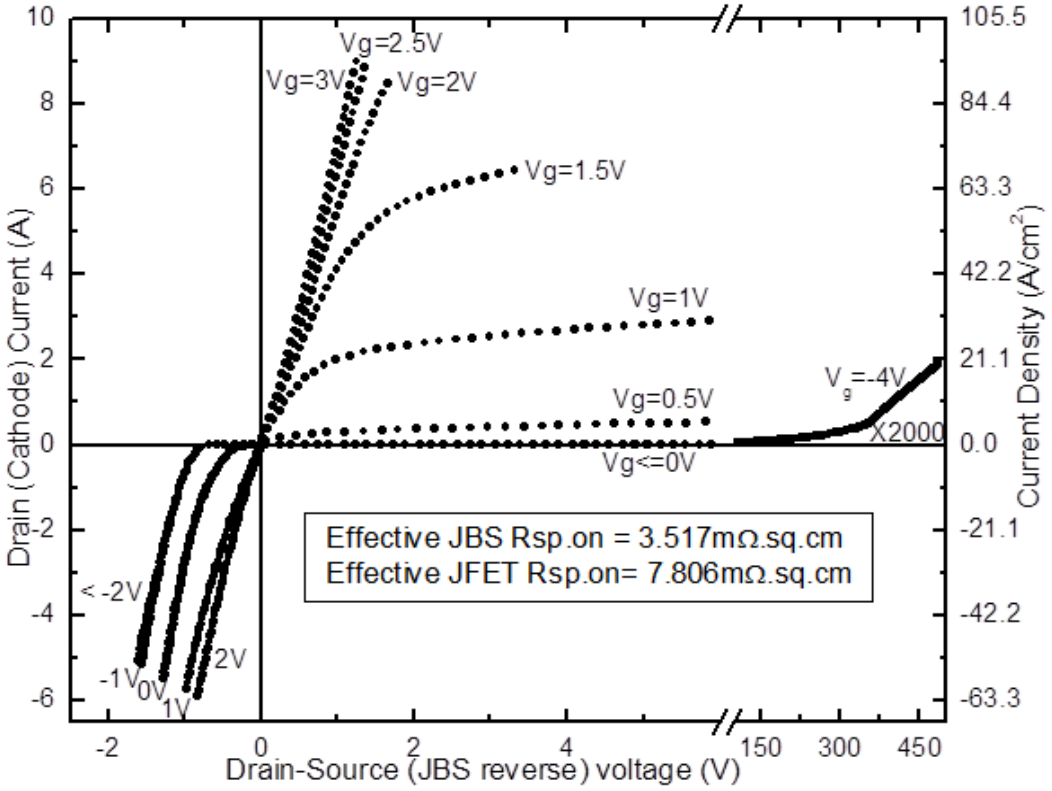

Figure 47 Static I-V curves of normally-on integrated switch

When gate voltage is below 2.7V-3V, it can be assumed that the minority carrier concentration in the channel is much smaller than the background majority carrier concentration. So, conduction is unipolar. At V_{gs}=2.5V, the Unipolar V_B^2/R_{on} is 26.97 MW/cm^2. In bipolar conduction at V_{gs}=3V, the bipolar V_B^2/R_{on} is 31.77 MW/cm^2. The definition of unipolar-bipolar transition in a power switch is a matter of debate in the power device community. Whereas an analysis as above based on the minority carrier concentration is technically most appropriate since it follows the definition of unipolar and bipolar, the ramifications of this transition on the utility of the power switch is best measured in terms of the current gain. The current gain in bipolar conduction is much lower than that in unipolar conduction. There is no current gain that is widely considered to be the lowest acceptable from a unipolar switch but a current gain lower than 100 is clearly seems to be too low in a unipolar switch. From

fig. 48, at V_{gs}=2.5V, the gate current is only around 10mA and when this device operates at 6A of drain current, the current gain is around 600.

In reverse conduction, the anti-parallel JBS diode is forward biased. When gate voltage is less than -2V, there is no significant gate current component at negative drain voltage and all the reverse conduction is through the diode. The specific on resistance of the diode is 3.5177.806 $m\Omega.cm^2$. When gate voltage increases, the gate-drain current adds to the diode current and reduces voltage drop at a particular reverse current density. This exhibits the potential of the device for synchronous rectification.

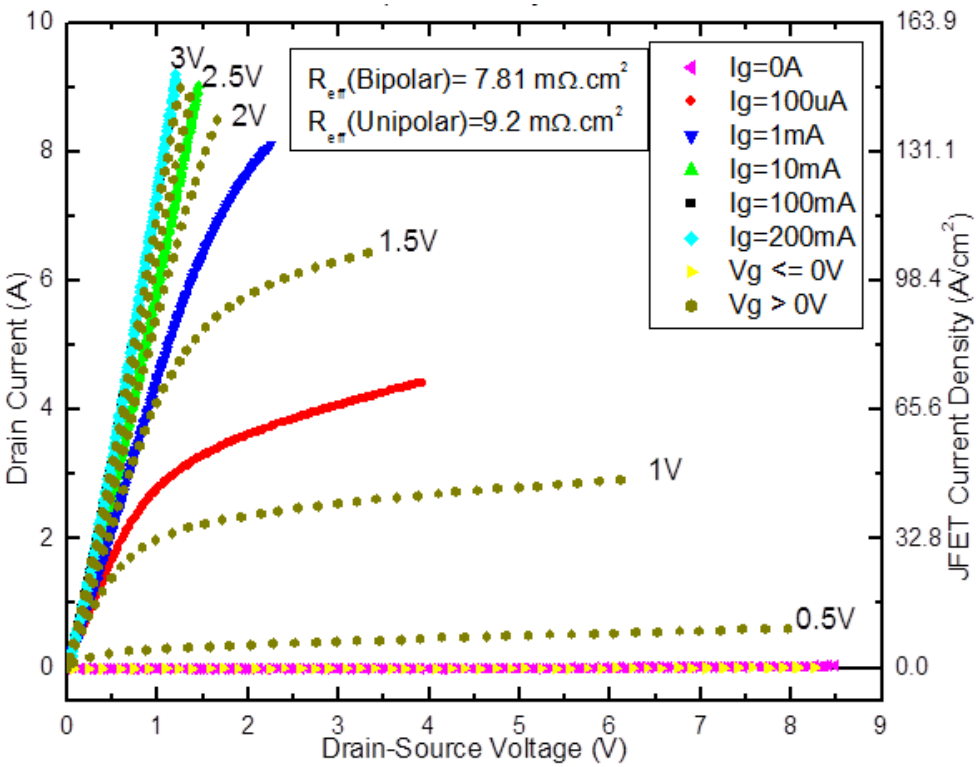

Figure 48 Gate current and gate voltage controlled output curves from fig. 47

The I-V curves of a normally-off device are shown in fig. 49. This device is only truly normally off till around 500V. It is measured up to 737V at V_{gs} = 0V and with negative gate bias of -1V, the device is measured up to a drain bias of 834V while keeping drain leakage current below $10mA/cm^2$. Under truly normally off

blocking operation, the power dissipation is 7.4W/sq.cm. The conductive power dissipation at 100A/cm^2 is 112.9W/cm^2 (100A/cm^2 at 11.29mΩ.cm^2). The power dissipation during blocking is 6.55% of that at rated conduction.

The conduction curves are shown in more detail in fig. 50 which also includes gate current controlled curves and a constant power line at 100W/cm^2. The JFET unipolar $R_{sp.on}$ is 27.45mΩ.cm^2 and the bipolar $R_{sp.on}$ is 9.93mΩ.cm^2. The current gain from fig. 50 is plotted in fig. 51 where the variation of both the drain current and the current gain with gate current is shown. The drain current first increases nearly linearly with gate current, indicating a constant current gain (~130) and unipolar operation. In bipolar mode, the current gain falls precipitously as gate current increases. For the truly normally off case, at V_{gs}=2.5V, the unipolar V_B^2/R_{on} is 19.95 MW/cm^2. At V_{gs}=3.5V, the bipolar V_B^2/R_{on} is 48.5 MW/cm^2.

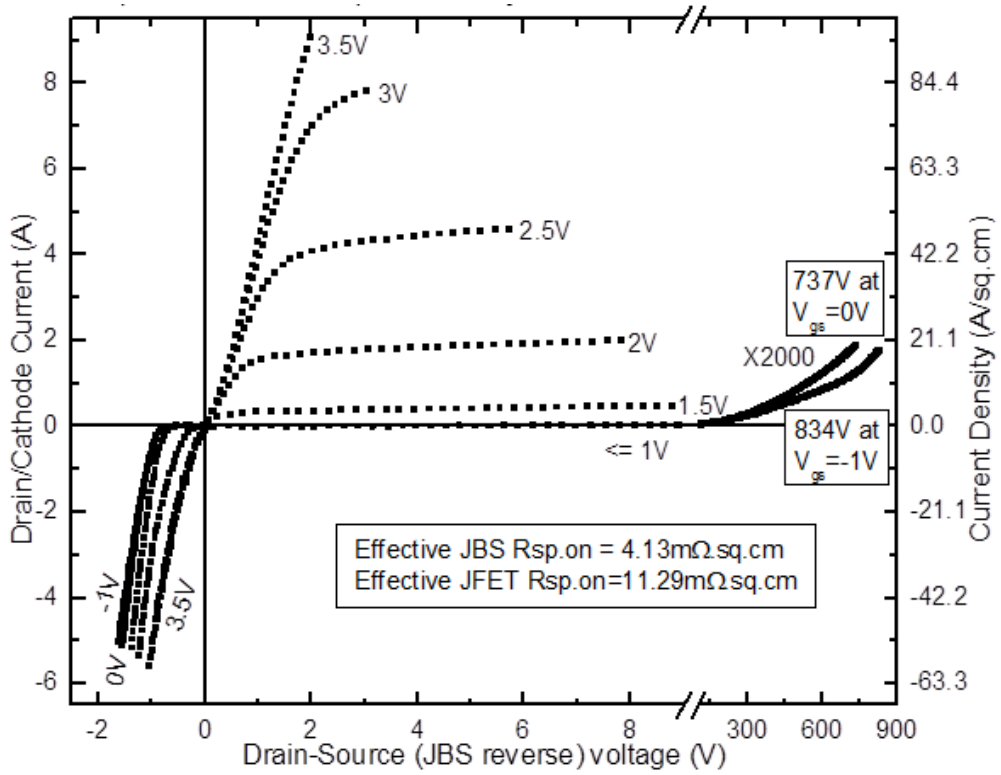

Figure 49 Static I-V curve of normally-on integrated switch

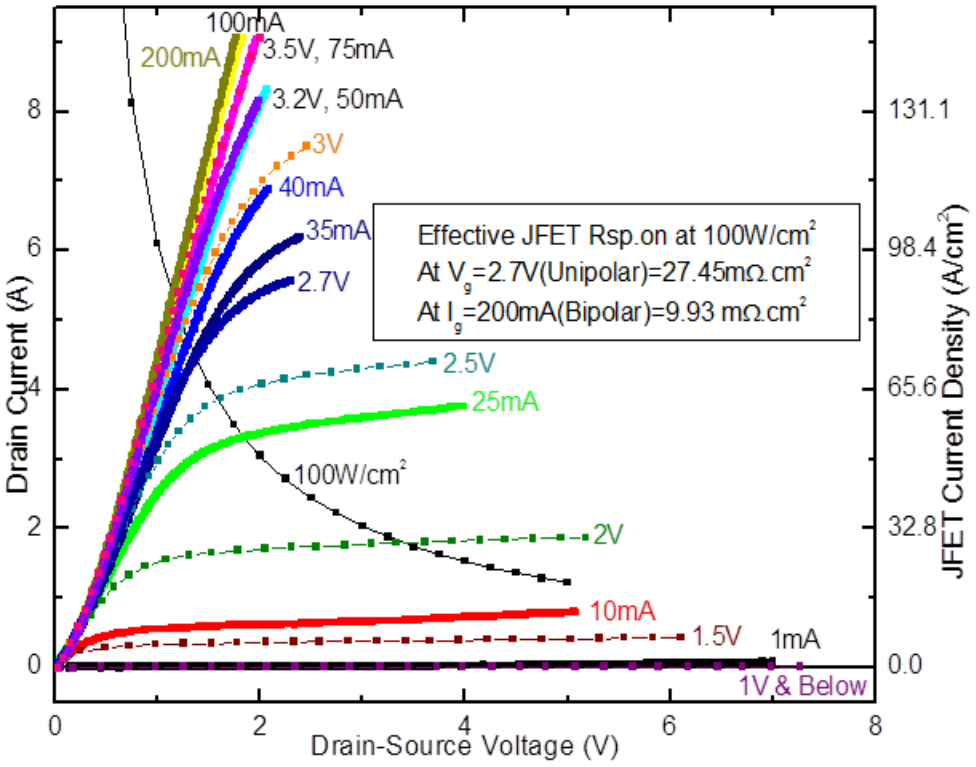

Figure 50 Gate current and gate voltage controlled conduction curves from fig. 49

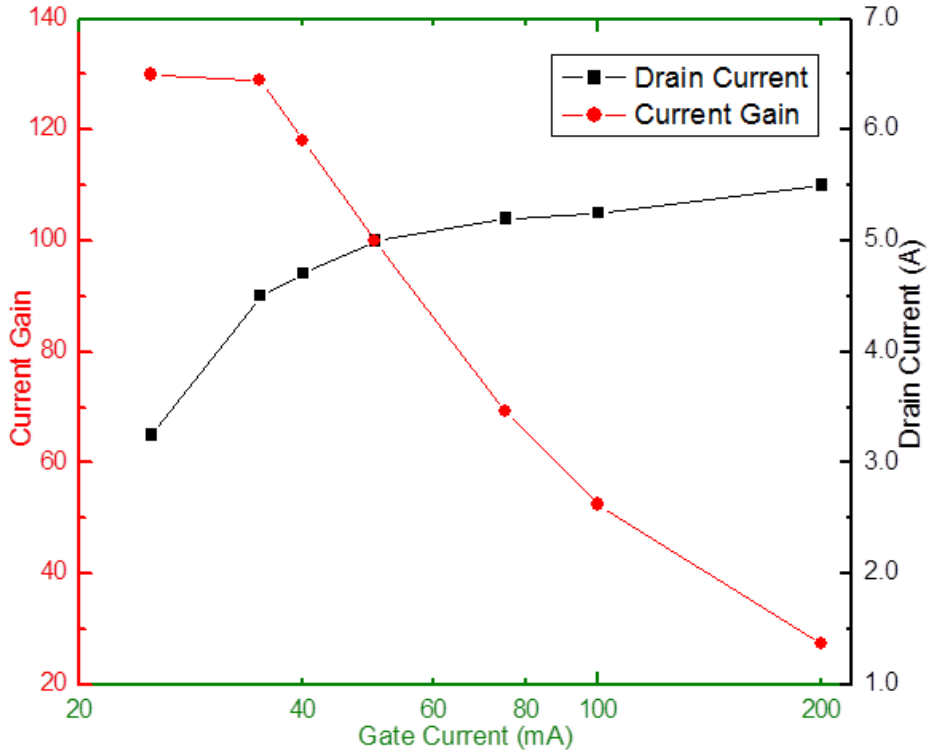

Figure 51 Variation of current gain and drain current in normally off device

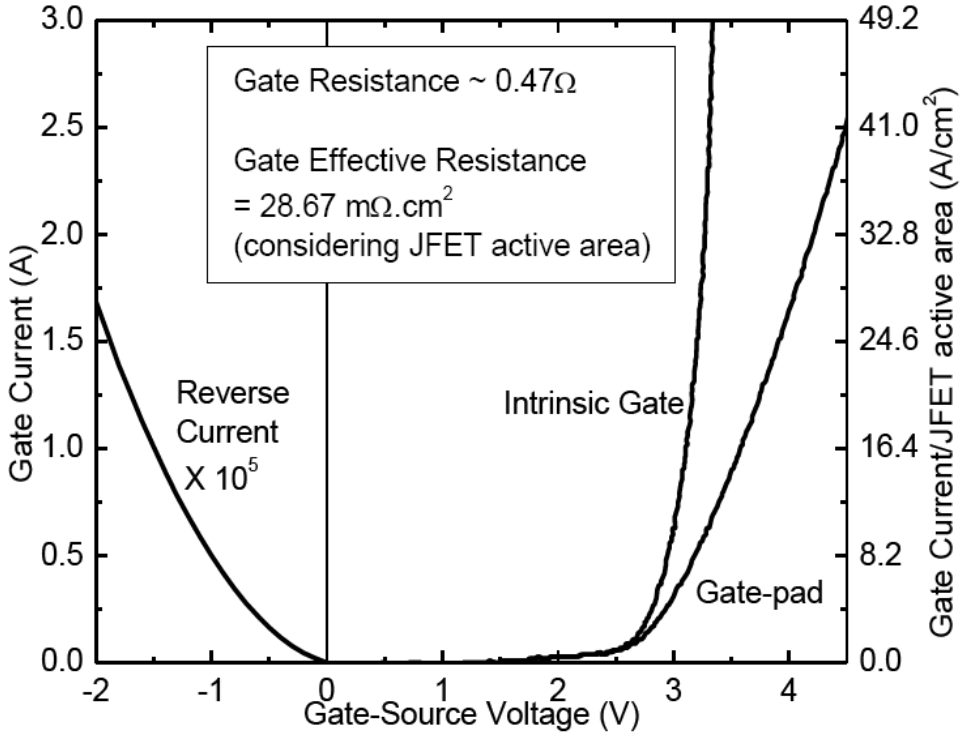

Figure 52 Gate-source I-V of the normally-off device

The gate-source I-V curve of the normally-off device is shown in fig. 52. There is very low leakage current at Vgs=-1V that is required to turn off the channel. When gate-source is forward biased, gate current increases significantly around V_{gs}=2.7V. However, the increase in current soon reduces to a straight line which means that most of the voltage is being dropped ohmically rather than across the semiconductor junction. From the high current slope of the I-V curve, effective gate resistance is calculated to be around 0.47Ω. Reducing the voltage dropped across this resistance, a rough plot of the intrinsic gate-source I-V curve is obtained for each gate current. From this plot, we can see that when gate terminal voltage is 3V, the intrinsic gate voltage is only around 2.7V and when gate terminal voltage is 3.5V, the intrinsic gate only "sees" around 3V. This is why in fig. 50, even at V_{gs}=3.5V, the gate current is only 75mA. Without overlay metallization of the gate, the gate spreading resistance will be even higher that what it is in fig. 52. Optimization of this process will further lower gate resistance and increase switching speed.

Experimental data in fig. 47 and fig. 49 show much higher leakage current than that predicted by simulation. Simulation predicts only tunneling current across the Ti-JBS junction and sub-threshold leakage or DIBL before avalanche breakdown takes place at >1400V. However, experimentally, there is significant leakage current at much lower voltages. The experimental leakage current is only gradually increasing, in a pattern similar to tunneling across the Schottky barrier rather than the sharper increase characteristic of drain-induced barrier lowering or surface breakdown. So most of the leakage current at V_{gs}= -1 V in fig. 49 can be attributed to imperfections in the Schottky contact of the JBS diode.

5.2 Temperature Characterization

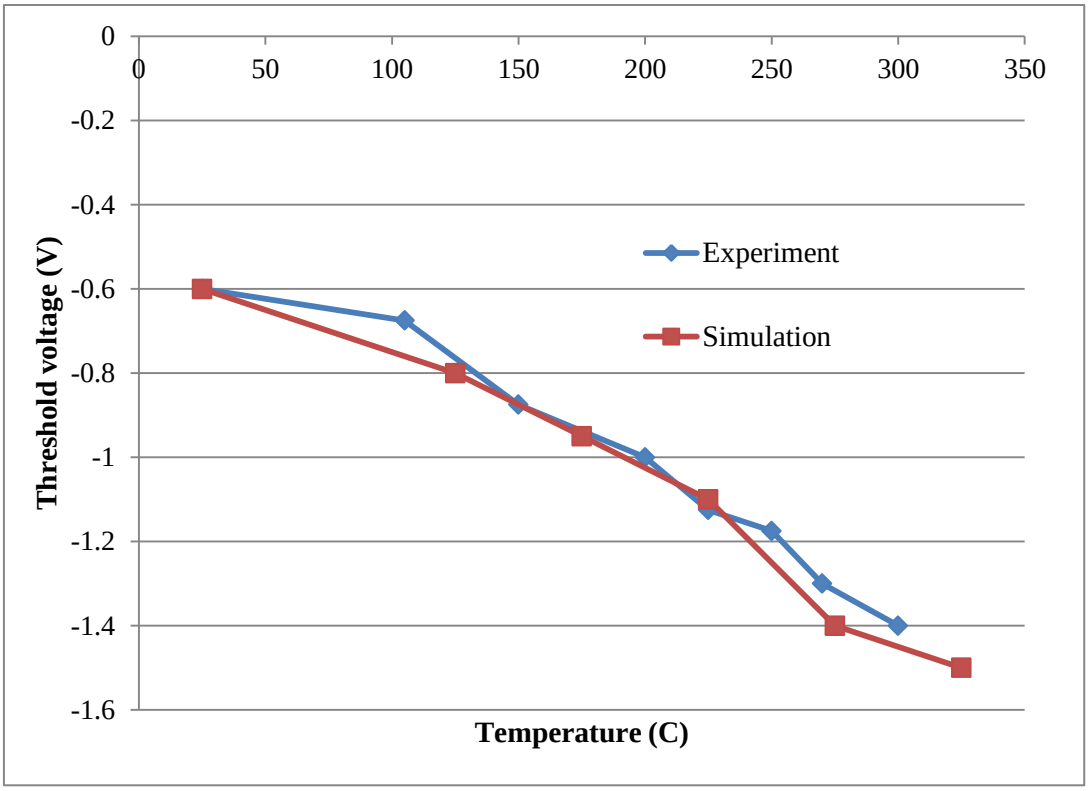

Figure 53 Variation of threshold voltage of VJFET with temperature

Power devices dissipate power during operation which increases their temperature. Increase in their temperature can be controlled by good packaging and heat sinks but they invariably operate at a temperature considerably above room

temperature. The conduction curves of a normally-off device are measured at higher temperatures to analyze the variation of threshold voltage and mobility with temperature. From these conduction curves, the threshold voltage and mobility are extracted. From the variation of threshold voltage with temperature, the zero temperature coefficient (ZTC) gate voltage of the power switch is extracted.

The variation of threshold voltage with temperature is shown in fig. 53, both experimentally and from simulation. The curves follow each other very closely. When temperature increases, the effective band gap of SiC reduces, which reduces the built-in voltage between the p-type gate and n-type source. This reduces the potential barrier in the channel for the same gate voltage. In other words, lesser positive gate voltage will be required to have the same potential barrier in the channel. So, threshold voltage at the gate decreases.

The variation of drain current with gate voltage when drain voltage is kept constant at 5V is shown in fig. 54 for different temperatures. This curve also shows the reduction in threshold voltage shown in fig. 53. From fig. 54, we can identify a gate voltage where variations in temperature do not change the drain current to drain voltage relationship, called Zero Temperature Coefficient (ZTC) point of the switch. For this device, ZTC is at V_{gs}~0.9V.

The existence of ZTC implies that while the reduction in threshold voltage with temperature increased the drain current, some other factor reduces drain current with temperature at higher currents. This is the mobility of the majority carriers in the bulk of the semiconductor. From the saturation current density that is achieved at full channel opening at each temperature, the mobility is calculated under the assumption that there are no parasitic resistances and that the contact resistances are negligible. At low temperatures, this is not a good assumption since mobility is high and contact

resistances are very significant compared to the resistance offered by the bulk of the semiconductor. At higher temperatures, when mobility falls, the resistance of the bulk semiconductor increases and voltage drop in parasitic and contact resistances reduces significantly. This effect is shown in fig. 55 which compares the mobility extracted from static I-V curves of the VJFET to that predicted from an analytical model [54]. As temperature increases, there is greater convergence between the measured and predicted mobilities because the experimentally measured mobility is more accurate.

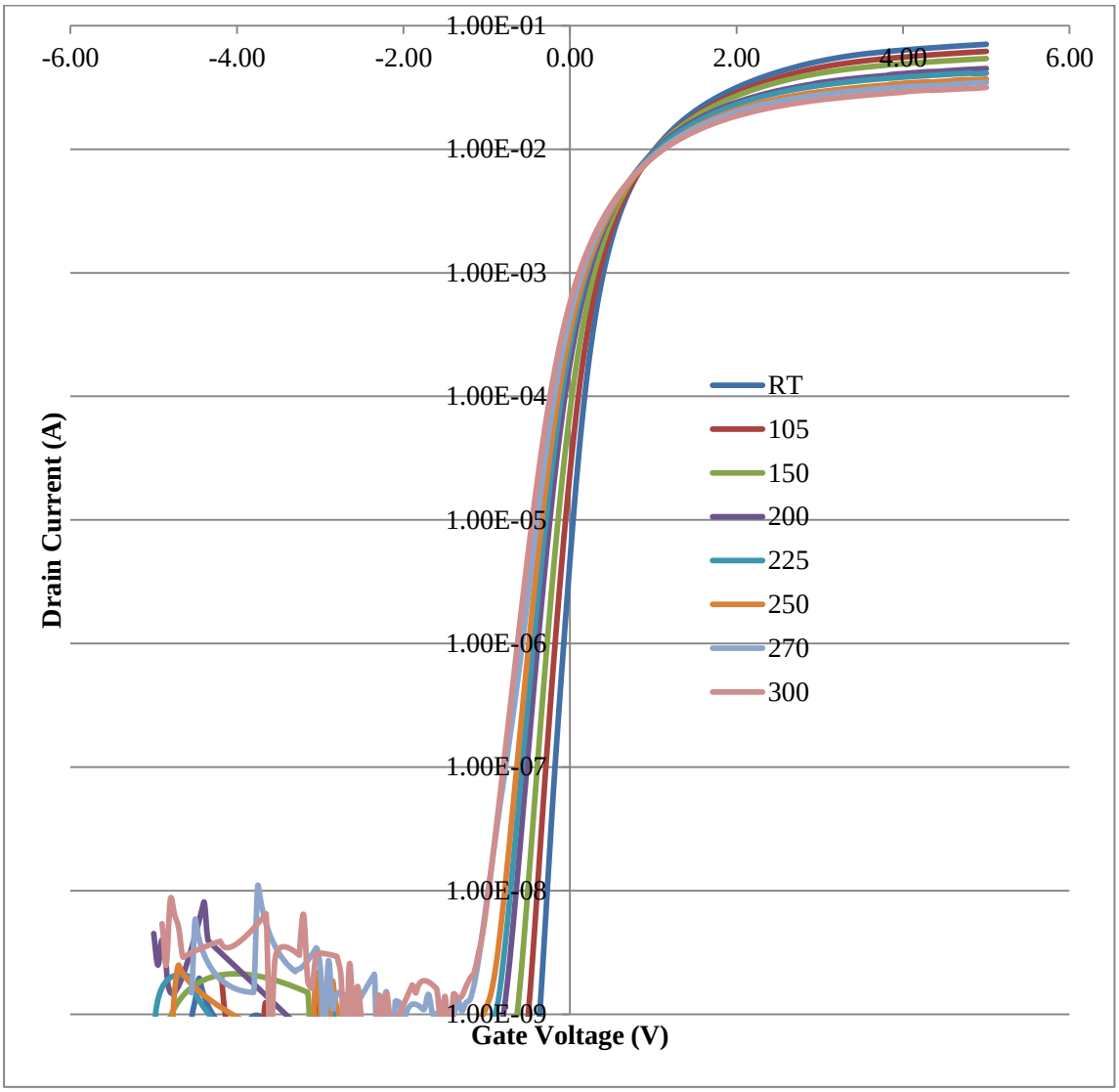

Figure 54 Variation of transfer curve of VJFET with temperature

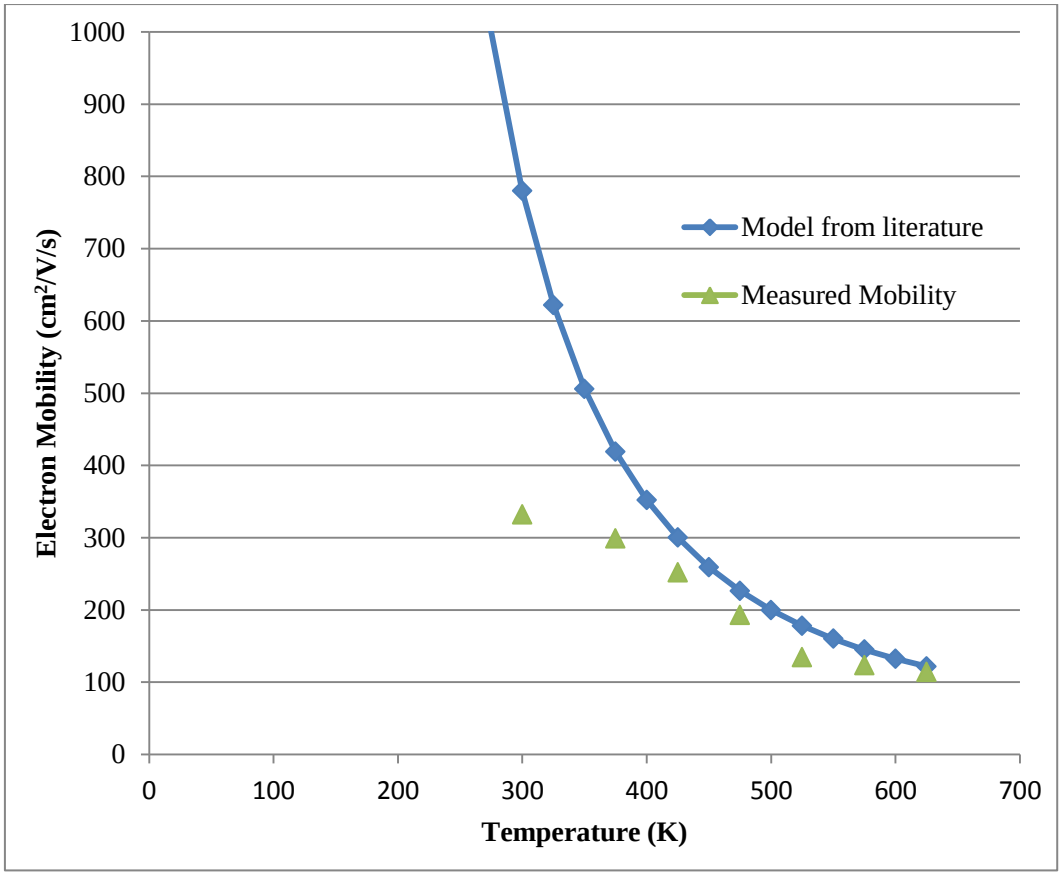

Figure 55 Variation of mobility with temperature from model and experiment

5.3 TCAD Modeling and Dynamic Characterization

In section 5.2, the integrated device was electrically characterized and imperfections in fabrication were found to increase the on-resistance beyond that of just the semiconductor, mainly due to the contact resistance. Considering a threshold voltage around -0.6V, gate resistance of 0.47Ω and source resistance of 9.93 mΩ.cm^2 or 0.163Ω, the device model is as shown in fig. 56. This "real" device that combines "ideal" devices of 0.061cm^2 JFET active are and 0.028cm^2 diode active area and series resistances is modeled in TCAD Sentaurus to find the static and dynamic I-V curves. The static conduction IV curve hence generated are first compared with the measured I-V curves and found to be similar to fig. 49. Then, switching curves are generated for the parallel plane integrated device, parallel plane JFET, parallel plane

JFET and anti-parallel diode, integrated device with edge termination and parallel plane device with edge termination.

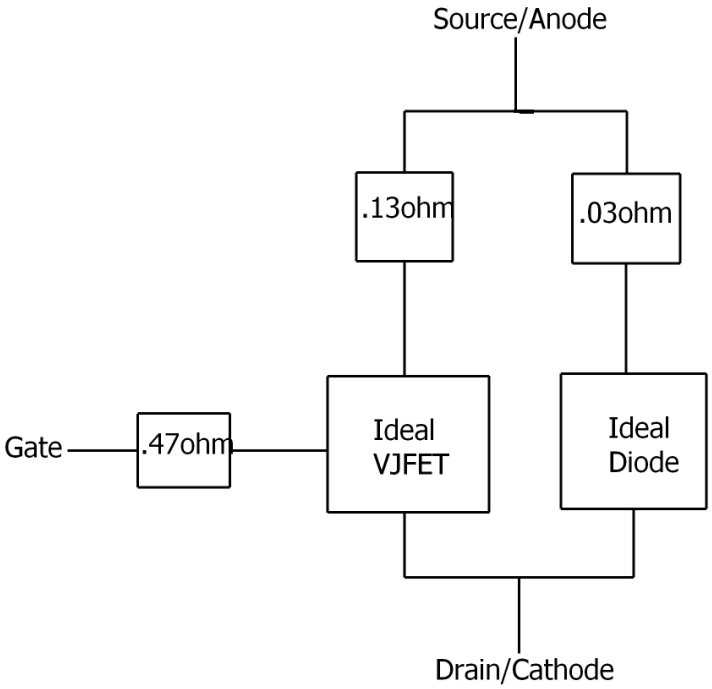

Figure 56 Model of fabricated integrated switch

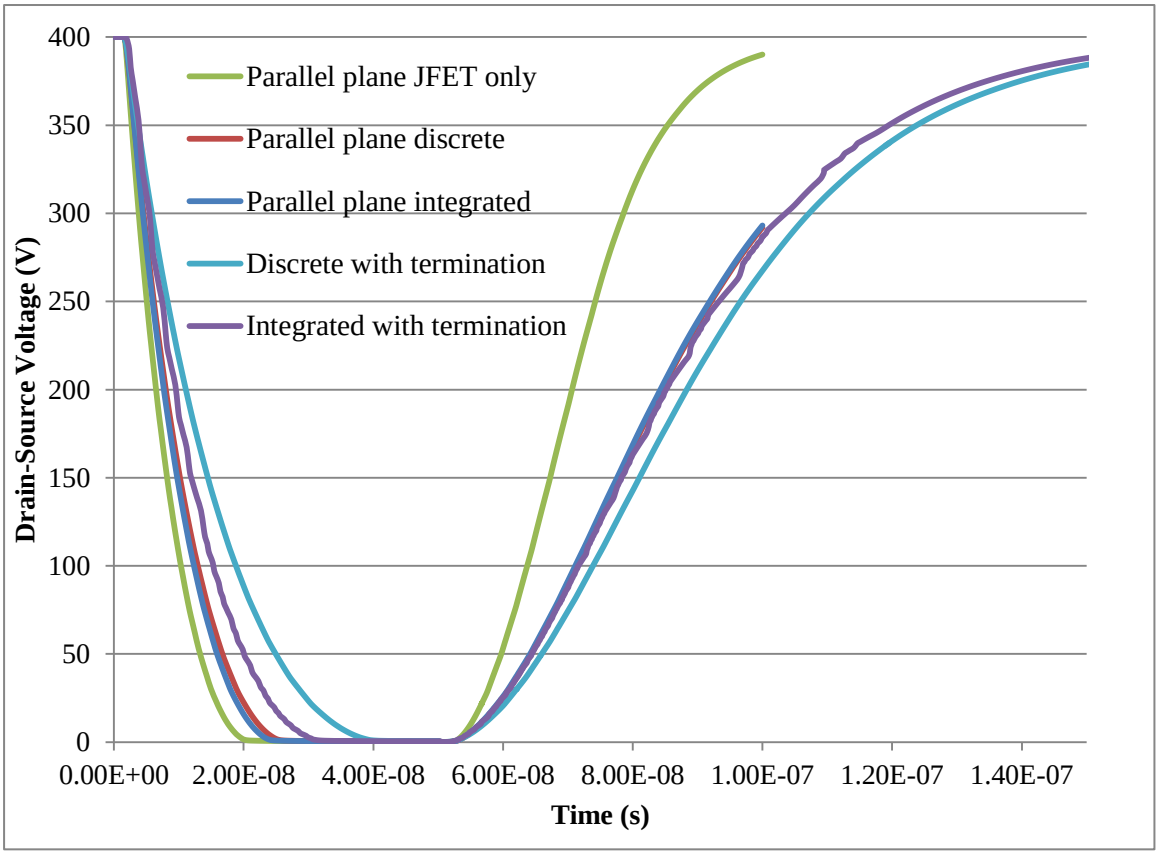

Figure 57 Mixed mode TCAD switching curves under model in fig. 56

From the mixed mode resistive simulation results in fig. 57, it can be seen that the JFET itself switches much faster than the integrated device. This is because when the gate of the JFET switches, the channel and drift layer of the JFET and the drift layer of the diode have to be charged or discharged by the drain current which is limited by the external circuit. When there is no diode present, the net amount of charge required for the charging or discharging is lesser and hence switching is faster. There is no significant difference in switching speed between the integrated parallel plane JFET and diode and discrete parallel plane JFET and diode which is because the total amount of charge stored in the parallel plane devices, whether discrete or integrated is almost the same

In the “real” devices with edge termination region, there is now an additional charge (to be stored in the edge termination region) that has to be cycled during switching, but with the same active area through which current flows and the same current limited by the circuit. Hence, switching time is higher for these cases. In addition, the switching speed of the integrated device with termination is slightly faster than that of discrete devices with termination. This again is because the total termination region as a proportion of active area is smaller in the integrated device compared to the discrete device. This advantage of monolithic integration reduces with increasing active area. However, besides saving on chip area and hence cost of the wafer, monolithic integration is shown here to increase switching speed and thereby reduce switching losses.

The fabricated integrated device was packaged and switched between 400V and 4A without an optimized gate driver circuit and with a resistive load. Fig. 58 shows that the device is capable of switching at over 1 MHz since the combined rise and fall time is around 600ns. Comparing this with the simulated curves in fig. 57, the

experimental curve is much slower, primarily because of imperfections in the gate driver circuit. Simulation assumed that the gate voltage switches in less than 1ns and that the gate driver has the capability to supply Ampere range current at no output resistance. Unclamped Inductive Switching (UIS) with an optimized gate driver is required to further analyze the effect of monolithic integration on the switching speed of the JFET and the flyback diode.

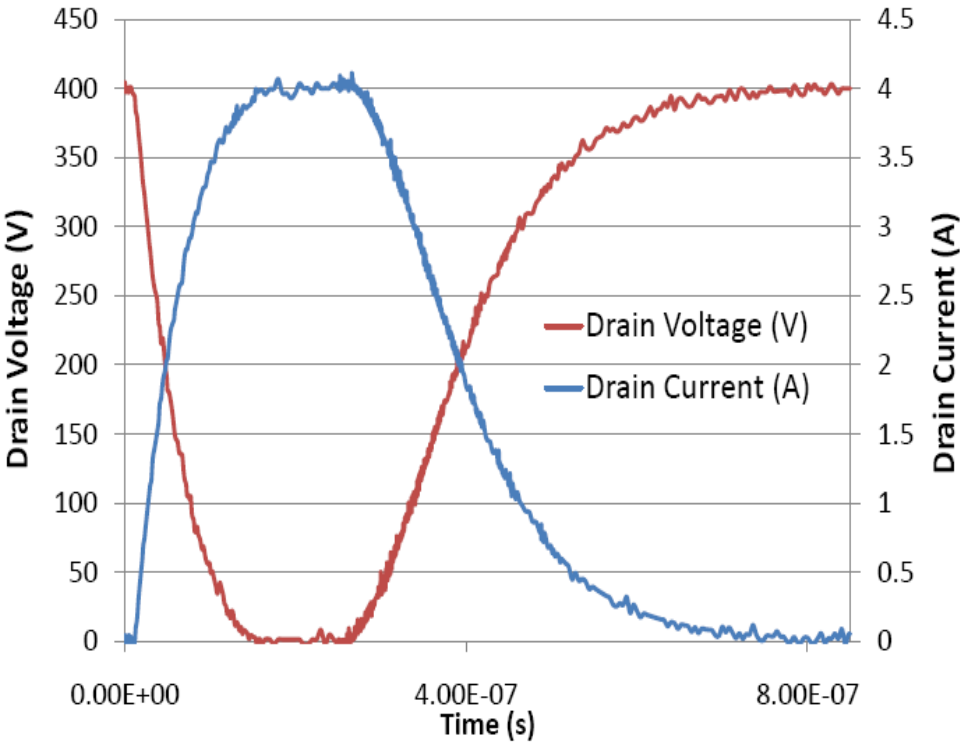

Figure 58 Experimental switching curves of the integrated device

5.4 Methods of Monolithic Integration

Monolithic integration of the VJFET and diode can be carried out in multiple ways. In this section, the scheme proposed in this thesis will be compared with a similar but differently executed method that failed and another successful scheme that is being pursued by Infineon Technologies in their soon to be launched SiC VJFET.

A previous design of monolithic integration of the VJFET and JBS diode [55]that was pursued at Rutgers University is shown in cross-section in fig. 59. Along

with the source mesas of the VJFET, mesas are also etched in the JBS diode region, of which the n+ region from the top is removed later to expose the n-region below to form Schottky contact. This scheme with side-wall implantation also in the JBS region will increase the electric field shielding at the Schottky barrier due to the surrounding PN junctions and reduce leakage current in the JBS diode further. However, the process for fabricating this device includes etching away the top of the JBS diode mesas which leaves them very rough. Subsequently, when a Schottky contact is formed there, there is significant electric field crowding at the Schottky junction which increases leakage current considerably. Although expected JFET/anti-parallel diode conduction curves were obtained, the device could only block around 50V. Besides the rough Schottky junction, another reason for poor blocking performance was that the transition region in fig. 59 between the JFET and diode was not optimally designed. The spacing between implanted rings was fabricated to be 3.5m, which from the analysis in chapter 3 of this thesis is too large for good electric field termination in this region.

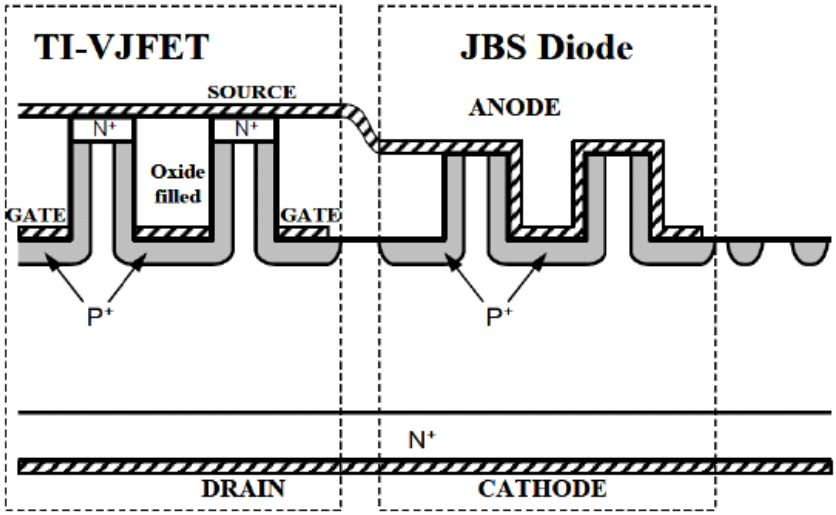

Figure 59 An unsuccessful scheme for integration of VJFET and diode [55]

Another method which results in a monolithically integrated SiC VJFET and anti-parallel diode is being pursued by Infineon Technologies AG [56]. The cross-sectional view of this structure is shown in fig. 60. The dark grey solid region indicates metal, hatched region implanted p+ and the dotted dark grey region n+ source. The VJFET has a lateral channel and the gate metal is on the top layer. The anti-parallel diode can only be a PN diode since it is formed by implanting p+ regions connected to the source through an ohmic contact. It has both advantages and disadvantages compared to the structure proposed in this thesis.

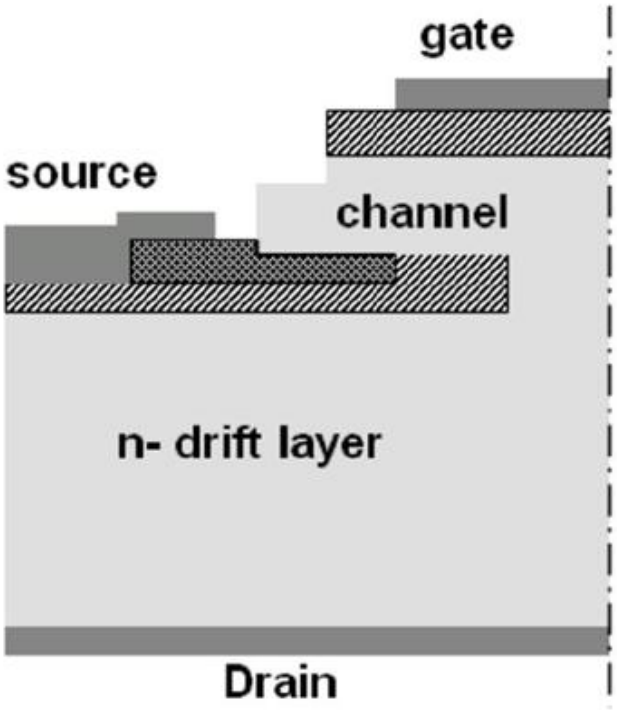

Figure 60 An alternative scheme for integrated SiC JFET and antiparallel diode [56]

The method in fig. 60 does not require JFET diode field termination which is sensitive to variation of dimension and no additional area for the anti-parallel diode is required since it is part of the JFET structure. Also, in the event of avalanche breakdown the high current is carried between source and gate, the output circuit, which is more equipped to carry high current than the gate. However, in the design

proposed in this thesis, gate will carry avalanche current. Also, there is no plasma etched region between gate and source that increases gate-source leakage with surface leakage current unlike in the scheme proposed here.

There are also significant advantages to the design proposed in this thesis. Unlike in fig. 60, there is the choice of having a JBS or Schottky diode instead of PN diode as the flyback diode. This is very significant since SiC JBS diodes have lower Ron and switch much faster than a comparable SiC PN diode. Also, the TI-VJFET has 2-sided gate control unlike one-sided gate control in fig. 60. This increases trans-conductance and reduces on resistance. The vertical channel also allows the TI-VJFET to achieve higher packing density of channel and hence lower on resistance than the lateral channel design in fig. 60. Also, no epitaxial regrowth, a cumbersome and expensive process in the midst of device fabrication, is required in the TI-VJFET. So, while the TI-VJFET design has the definitive advantage of better flexibility in the choice of flyback diode, depending on the weights attached to the other advantages and disadvantages, the design proposed in this thesis or that in fig. 60 might be more suitable for a particular application.

6 SPIN-ON GLASS FOR FILLING VJFET TRENCHES

TI-VJFETs have both the source and gate on the top side of the wafer. The gate is on part of the side-wall of the trenches etched on the top of the wafer and the source is on top of those mesas. Since the ability to have gate-source voltage is central to JFET operation, metallization processes should not short or cause highly conductive paths between gate and source. Gate-source isolation should be robust and resistant to harsh environments. In the TI-VJFET research conducted hitherto and reported in the literature [52], two methods of gate-source isolation have been developed-

1. Thick polyimide is spun-on, cured and planarized with plasma etching. This process is easier and polyimide being thick and viscous planarizes naturally. After plasma etchback to expose the source mesa, a nearly flat top surface is obtained. However, polymide is stable only up to around 300C and even below that temperature; it is not resistant to harsh environments of temperature and humidity for robust operation over a long time. This is the method that has been used in the monolithically integrated switch fabricated in chapter 4 of this thesis.
2. PECVD Silicon dioxide and Silicon Nitride are deposited in the gate trenches. This process doesn't require any curing and Silicon dioxide and silicon nitride have high dielectric strength and resistance to degradation over time in harsh environments. However, planarization with this process is extremely hard since PECVD tends to grow thicker at the top of the side-wall than at the bottom where the vapor concentration is lower. So, even if the difficult process of opening up the source mesas while keeping gate trenches covered with PECVD is achieved, there will be cracks between the trench-bottoms and their dielectric cover that will worsen with thermal cycling. So, the PECVD

based process is much harder to achieve and even if it isolates the gate and source metal layers, it might be vulnerable to damage from thermal cycling.

It is desirable to develop a process that can combine the potential of Silicon dioxide for long-term robust operation and the ease of processing of polyimide. Spin-on glass holds promise in this regard because it can be applied by a spin-on process that like polyimide will planarize naturally by having a higher thickness at the bottom rather than the top of the trenches while also forming silicon dioxide after subsequent curing. Spin-on glass has been used in the Silicon semiconductor industry since the 1970s to form dielectric films and to fill vias. However, spin-on glass is not as viscous as the polyimides that have been used for trench filling and has only been reported to form flat films around 5000A thick.

Spin-on glasses (SOGs) are a class of compounds containing oxygen which undergo condensation polymerization to form plastic-like layers that can be cured at relatively high temperatures (about 400-500C or above) to form inorganic glasses [57]. Polysiloxane polymers are the most widely used SOGs because of their low dielectric constant, good passivation and better SiO_2 like characteristics. For this study, we have chosen the spin-on glass Filmtronix 500F which is a methylsiloxane. It is a dense polymer which yields a minimum shrinkage film and is capable of producing a single film ~6500A thick at spin speeds not low enough to cause significant non-uniformity in thickness. Thick films of up to 2μm can be produced using multiple coats. 500F is cured up to 425C in air without thermal decomposition.

VJFET trenches are about 3.5 μm deep and 2 μm wide, an aspect ratio around 1.75:1. If only SOG were used to fill and planarize the trenches, while the first round might yield 6500A, subsequent rounds of SOG will give diminishing returns since etchback of the source mesa top will become increasingly harder. Using an SOG only

process, we managed to successfully isolate the two metal layers but the source contact region was not planarized completely which makes source wire-bonding difficult. So, the process developed here involves two rounds of a combination of PECVD SiO_2 and SOG such that the SOG fills the uneven gaps that PECVD SiO_2 will inevitably create. This is similar to applications in Silicon semiconductor processing where SOG has mostly found use in filling vias and crevices. Post curing, SOG is supposed to become SiO_2 and the PECVD Silicon dioxide layer in between the two SOG layers is expected to relieve thermal stress while the second SOG layer is cured.

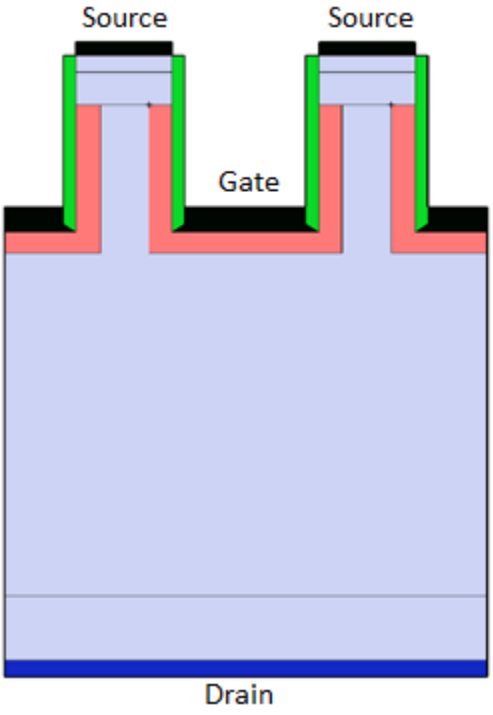

Figure 61 Cross-section of VJFET before trench-filling

The cross-sectional view of the VJFET just before trench filling is shown in fig. 61. The gate and source ohmic contacts (black) are formed there is dielectric (green) covering the side-wall. The p+ implanted gate is shown in pink. Under Dektak profiler measurement, the height of the source mesas from the gate-pad is about

29500A, out of which around 2μm needs to be filled by dielectric to achieve isolation between gate and source. An SEM image of the VJFET trenches is shown in fig. 62.

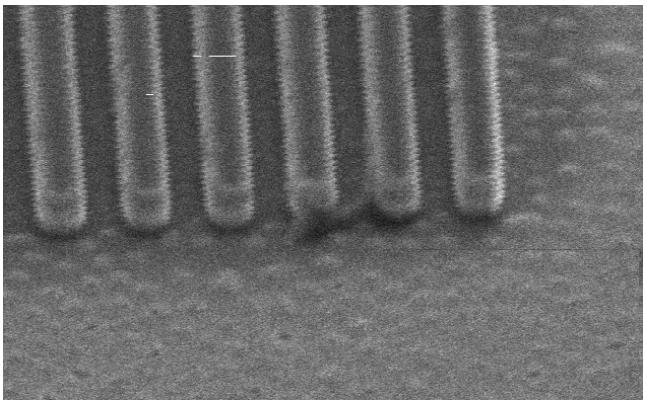

Figure 62 SEM image of VJFET mesas before trench filling

6.1 Trench filling process

6000A of PECVD oxide (2 rounds of 3000A each) is first deposited. Then, 3000A of Al is evaporated on to the wafer and PR 5214E spun and etched back using ICP to expose the source mesas. Then, AZ 327 MIF for 2' followed by Al etch II with surfactant for a total of 4.5' is used to remove Al from mesa tops. PR is then stripped and Silicon dioxide wet etched from mesa top using BOE 30: 1 for 2', then dry etched using CF_4 and O_2 plasma in ICP for 6' followed by BOE 30:1 dip for 1'. Removal of silicon dioxide from the source is visually confirmed at this stage through the microscope and by testing for electrical continuity between different points on top of the same source mesa.

Filmtronix 500F SOG is then spun at 500rpm (5s) + 2000rpm (11s) + 1500rpm (4s). This is expected to give 6400A of spin on glass thickness. Immediately after spinning, SOG is baked at 85C for 1 minute followed by 255C for 1 minute and then allowed to cool down on top of the hot-plate naturally to room temperature (for around 40 minutes). Under microscope, some colors are visible on top of the source mesas at this stage (indicating varying thickness of some thin film). The sample is

then cured in nitrogen ambient at atmospheric pressure. Temperature is ramped at 5C/min to 275C and then at 2.5C/min to 425C, held for 1 hour and the sample is allowed to cool down naturally.

PR 5214E is then spun on the wafer and planarized. PR and spin-on glass are etched back in ICP using isotropic (400W, 0V, CF_4- 40 sccm) process for 5'30". After that, PR is removed using AZ400T. Then, under Dektak, the step between source mesa tops and gate-pad is around 19000A. Although 6000A of Silicon dioxide and 6400A of SoG were thought to be filling the gate-trench, it has only filled up by around 10500A. This might be because some of the silicon dioxide/SoG in the trenches (around 1900A) was also etched back during the process. At this stage, with one layer of SiO_2 and one layer of SOG in the trench, an SEM view is shown in fig. 63 and a cartoon of the trench is shown in fig. 64 with SiO_2 in dark yellow and SOG in light yellow. From the SEM view, it is clear that the trenches are not yet fully filled and planarized, and there are also some cracks visible that SOG has not completely filled. The cartoon in fig. 64 is meant to illustrate how SiO_2 is thicker at the top of the sidewall of the trench and thinner at the bottom and how SOG is expected to reduce this asymmetry by filling up the bottom of the trench more than the top.

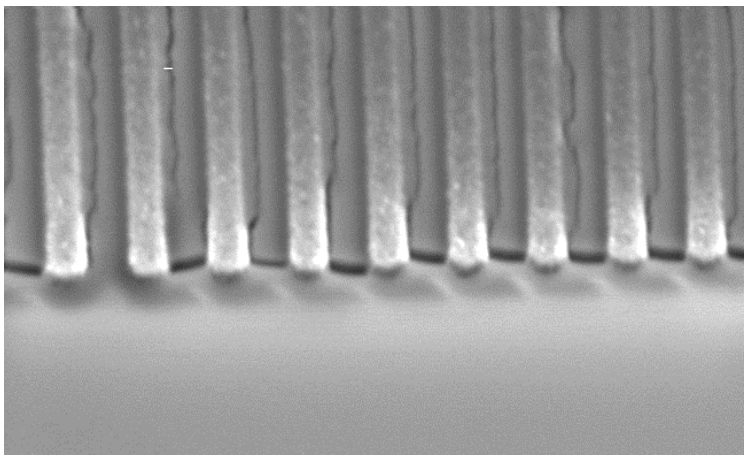

Figure 63 SEM image of VJFET mesas with SOG etched back

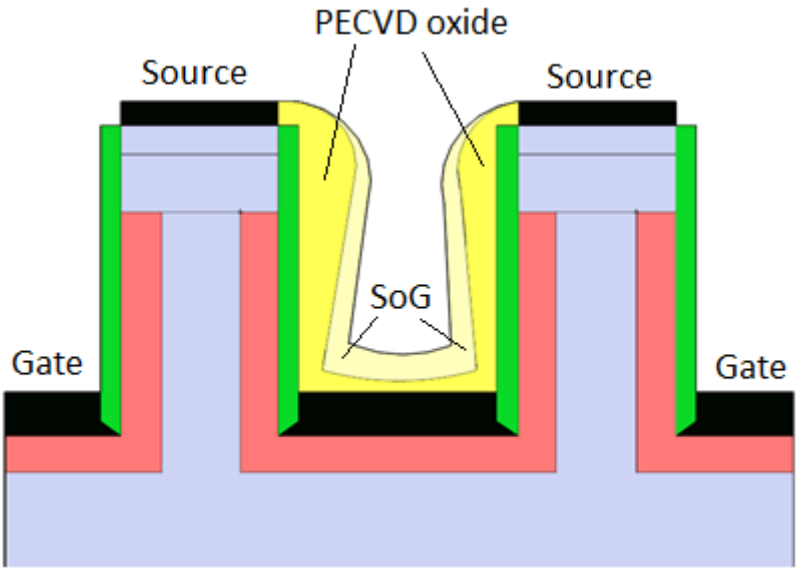

Figure 64 Cartoon of cross-section of VJFET with one layer of SiO_2 and SOG

The same process as for the first layer (6000A of Silicon dioxide filling followed by 6400A of SOG filling) is repeated and now the level between source mesa top and gate in the trenches dropped to around 10200A. So, during the second round, trench has been filled by around 8800A. If there are no cracks in the dielectric filling the trenches, this will be enough to separate the source and gate layers as the gate only extends 2um up the 3.5um deep trenches. So, filling the trenches till there is only 1.02um between source and gate dielectric should have covered the entire gate-sidewall with dielectric. An SEM image of the mesas at this stage is shown in fig. 65 and a cartoon of the cross-section in fig. 66. While the bulk of the trench is filled by PECVD SiO_2, SOG is expected to be crucial in adjusting the profile of the dielectric and planarizing it.

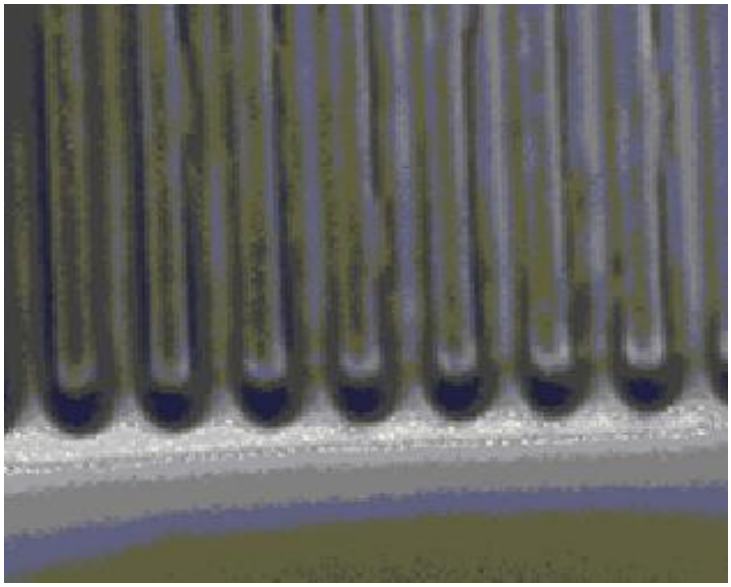

Figure 65 SEM view of VJFET mesas after SiO_2 and SOG planarization

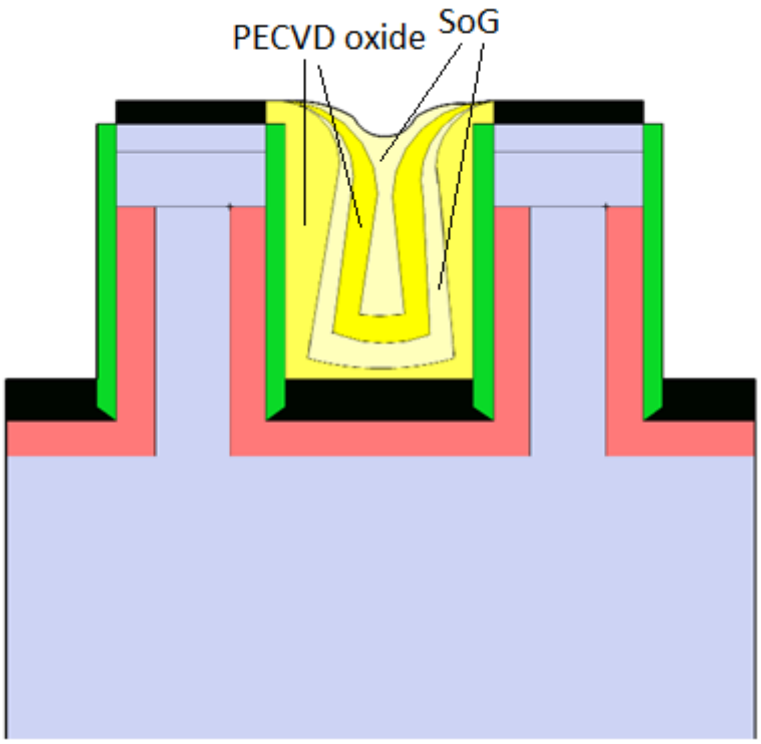

Figure 66 Cartoon of cross-section of VJFET with SiO_2 and SOG planarization

6.2 VJFET Metalization

The via window opening mask from chapter 4 is then used to open the gate-pad region. Lithography with thick PR 4620 opens the window and anisotropic CF_4 and O_2 in ICP (200V, 300W for 11”30”) removes the SOG and SiO_2 from the gate-

pad without attacking PR in the source completely. After stripping PR with AZ400T, the VJFETs (single finger source, gate pad and drain) are tested to see basic JFET operation. At this stage, an SEM image showing the gate trenches still containing dielectric and gate pad cleared of it is shown in fig. 67.

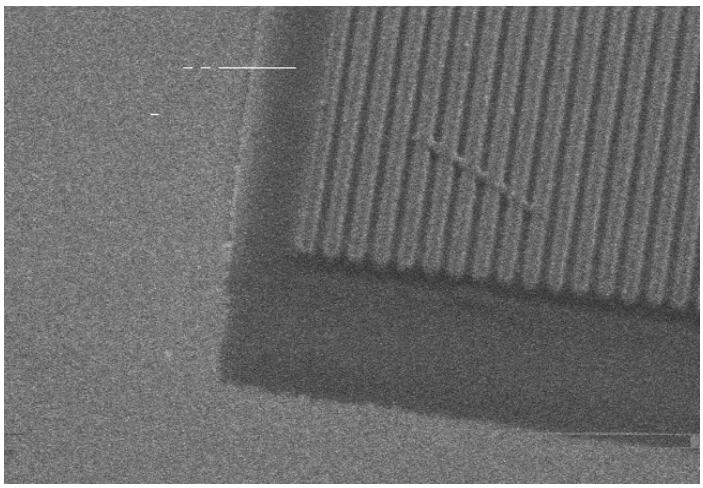

Figure 67 SEM view of gate-pad and trenches in VJFET before final metalization.

Finally, negative PR AZL2035 is used with the metal overlay mask from chapter 4 to open the source and gate metal windows and 1000A of Ti followed by 10000A of Al are evaporated. This is followed by 10000A of Al evaporated on the backside. Then, lift-off in AZ400T separates the gate and source metal layers.

6.3 VJFET Static Characteristics

The VJFETs fabricated with SiO_2 and SOG filling the trenches are electrically tested using Tektronix 371A for blocking and HP 4145 for conduction. The devices on the wafer in consideration have the same design as the VJFETs that are part of the monolithically integrated switch in chapter 4. The static I-V curve of the VJFET which exhibits the best forward conduction among the ones blocking > 1000V is shown in fig. 68. The device is not fully normally off at high voltage but is turned off with negative gate bias. It is clear that gate-source is capable of supporting voltage

and changing channel opening with it. This validates the ability of the trench filling scheme to isolate the gate and source. When the gate is forward biased, the VJFET carries > 100A/cm^2 of current. Both gate current and gate voltage controlled output curves are shown, from which the specific on-resistance is around 20 mΩ.cm^2. This VJFET doesn't perform as well as the ones reported in chapter 4 and in literature [8] but it does exhibit VJFET action and validates the SOG based method for filling SiC VJFET trenches. Scanning with Dektak across source mesas and gate trenches after final metallization (~ 1.1 μm), the result has peak to peak dimensions of around 5500A. During previous studies with polyimide also, scan results were in the 5000A range. This is expected to be suitable for wire-bonding to the source contact.

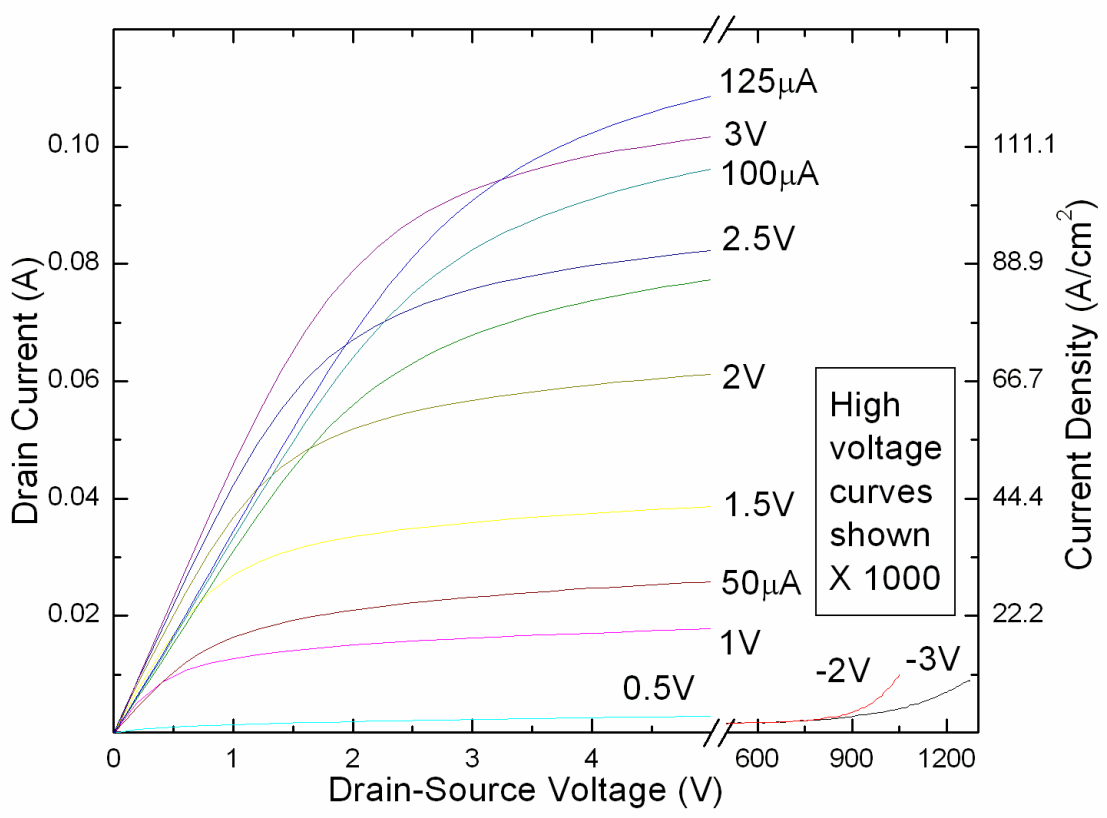

Figure 68 Static I-V curves of a VJFET with SOG-based trench filling

6.4 Summary

Two layers of 6400A SOG Filmtronix 500F separated by PECVD SiO_2 are shown to fill and planarize gate trenches of the TI-VJFET such that source and gate are isolated. JFET operation is demonstrated under these conditions. SOG is an attractive alternative to PECVD-only or polyimide based process for VJFET trench filling as it is more resistant to high temperature and other extreme conditions.

7 CONCLUSIONS AND SUGGESTIONS

7.1 Conclusions

This thesis reviews the state of the art of power semiconductor devices in the context of increasing demands for efficiency in power conversion and identifies SiC based devices as an ideal candidate for building better power circuits. These devices have lower on resistance and switching losses for the same blocking voltage as Si based devices. Discrete SiC switches and rectifiers have been demonstrated that far surpass the best Si devices today. The next logical step in moving the SiC power device research area forward is to build monolithically integrated circuits. One of the most common blocks of multiple devices in power circuits is the power switch and anti-parallel diode. This thesis designs, demonstrates and characterizes the first SiC VJFET with a monolithically integrated anti-parallel diode.

In pursuit of the central objective, this work makes many original contributions to the research area. The first 2-D compact model for reverse leakage current in high voltage JBS diodes is developed which completes the analytical theory of the JBS diode. A new 2-D analytical model for forward blocking performance of a SiC VJFET with realistic gate-channel junction is proposed by extending previous such models for abrupt gate-channel junction. The best anode layout for the JBS diode is identified theoretically to be the 3-D hexagonal honeycomb. A spin-on glass based process for filling gate trenches in the VJFET is also developed and demonstrated as part of this thesis.

The novel analytical models and TCAD simulations were used to propose an optimum design for the integrated switch. The switch and integrated anti-parallel JBS diode thus designed was fabricated and demonstrated to operate at high voltages. The device was measured to block upto 834V and conducted forward current at a specific

on resistance of 7.8mΩ.cm^2. The anti-parallel JBS diode conducted third quadrant current with a specific on resistance of 3.5mΩ.cm^2. Electrical characterization and TCAD simulation yield encouraging results that point to the advantage of SiC monolithic integration in reducing switching power loss and device parasitics, saving on chip area and improving robustness of operation.

7.2 Suggestions for Future Work

This study into SiC power devices and their monolithic integration point to many areas where future research is likely to be productive. An approach similar to that used in this work to form a closed form model for the JBS diode can be employed to form a theory of the Trench MOS barrier Schottky rectifier [39], among other shielded power diodes. A fuller understanding of the metal-semiconductor contact and formulation of accurate Fowler-Nordheim like closed form equation for tunneling at the metal-semiconductor junction will also improve the predictions of the model. The proposed JBS diode theory will be most successful if the insight gleaned from it on the effects of various design parameters helps introduce refinements that lead to performance improvements.

From the JFET model it is clear that on-resistance can be improved by increasing the majority carrier concentration in the channel. To maintain the same potential barrier in the channel, this will necessitate smaller and better controlled channel opening. This is a challenge that can be addressed by improvements in fabrication. The packing density of the VJFET (i.e. the width of the source mesas as a proportion of the pitch of the mesas and trenches) can also be improved with better fabrication techniques. This will improve specific on resistance and hence reduce the chip area of a VJFET designed to carry a particular current.

The identification of 3-D honeycomb layout with Schottky region in the streets as the best anode layout among the ones considered for JBS diodes raises interesting questions regarding the sensitivity of the FOM in each layout to variations in dimension. If the edges of the hexagonal grid are rounded, the effect on field shielding at Schottky contact might be different from that in interdigitated stripes. This effect can be studies using systematic TCAD simulations. The implanted field rings used for field termination between JFET and diode in the integrated device is only one way achieving that goal. Other methods can be investigated that are less sensitive to dimension.

The spin-on glass based trench filling process demonstrates the potential to remove polyimide from the VJFET fabrication process. The process developed here should be further studied at high temperature and stress tested by switching the device over long periods to ascertain its robustness. There is also room to simplify the current spin-on glass process to avoid having two layers of the dielectric which increases fabrication time, cost and complexity and creates room for error. Processes involving thicker spin-on glass or slower spin speed that still gives uniform coating might be pursued.

Experimental and simulation results from this study indicate than monolithic integration reduces switching power loss. This can be futher studied using unclamped inductive switching tests of the device in power circuits like inverters with inductive load. The effect of reduction in device parasitics on circuit parameters will also be revealed by such studies. Data from such switching tests can also be used to create SPICE models for this integrated switch, which can then be studied in more complicated power circuits using simulation tools.

APPENDIX-1 ANALYTICAL MODEL FOR VJFET

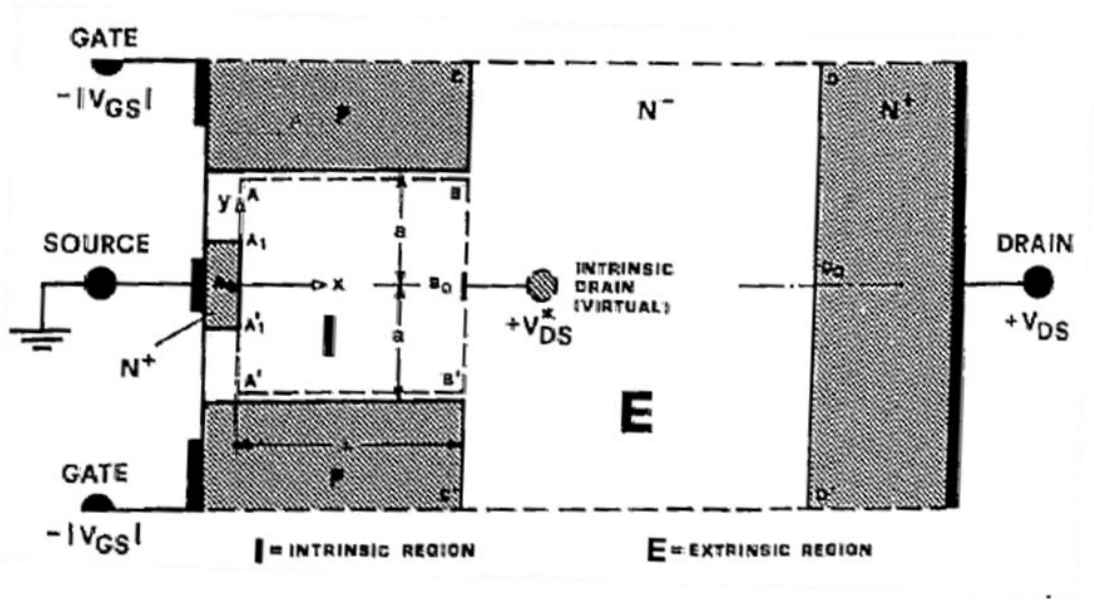

Figure 69 Cross-section of VJFET showing domain of 2-D solution [41]

This appendix reproduces the 2-D analytical model provided by Bulucea and Rusu [41] for a VJFET or SIT with abrupt gate-channel junction. The domain within which the 2-D differential Poisson equation is solved analytically is outlined in fig. 69. The boundary conditions are zero voltage at the source, constant voltage along the top and bottom sides of the domain (gate-channel junctions) and a constant voltage at the point opposite to the source, called the intrinsic drain. The latter is a virtual point and the potential there is a linear combination of the drain-source and gate-source voltages after punchthrough.

Splitting the 2-D Poisson equation into 1-D Poisson along the gate-channel direction and 2-D Laplace equation, the potential in the domain can be solved to be

$$\emptyset(x,y) = -\frac{kT}{q}\left\{ln\left(\frac{N_{ch}N_A}{n_i^2}\right) + ln\left(\frac{N_S}{N_{ch}}\right)\right\} + V_{GS} + \frac{qN_{ch}a^2}{2\epsilon}\left(1-\left(\frac{y}{a}\right)^2\right)$$

$$-\left[V_A \exp\left(\frac{-\pi x}{2a}\right) + V_B \exp\left(\frac{\pi x}{2a}\right)\right] Cos\left(\frac{\pi y}{2a}\right) - - - (75)$$

The constants here mean the same as they do in the VJFET model in chapter-2. In addition,

$$V_A = \left(\frac{\mu_0}{\mu_0 + 1}\right)\left[\left(\frac{kT}{q}\left\{ln\left(\frac{N_{ch}N_A}{n_i^2}\right) + ln\left(\frac{N_S}{N_{ch}}\right)\right\} - \frac{qN_{ch}a^2}{2\epsilon} - V_{GS}\right) - \frac{V_D^*}{\mu_0 - 1}\right] - - - (76)$$

$$V_B = \left(\frac{\mu_0}{\mu_0^2 - 1}\right)\left(V_D^* + \left(\frac{\mu_0 - 1}{\mu_0}\right)\left(\frac{kT}{q}\left\{ln\left(\frac{N_{ch}N_A}{n_i^2}\right) + ln\left(\frac{N_S}{N_{ch}}\right)\right\} - \frac{qN_{ch}a^2}{2\epsilon} - V_{GS}\right)\right) (77)$$

To find the potential barrier in the channel, we have to differentiate the channel potential with respect to x to find its minimum along the x axis. Setting the derivative to zero, we get

$$x_{min} = \frac{a}{\pi}\ln\left(\frac{V_A}{V_B}\right) - - - (78)$$

Substituting this in (75),

$$\emptyset_{min} = -\frac{kT}{q}\left\{ln\left(\frac{N_{ch}N_A}{n_i^2}\right) + ln\left(\frac{N_S}{N_{ch}}\right)\right\} + V_{GS} + \frac{qN_{ch}a^2}{2\epsilon} + 2\sqrt{V_A V_B} - - - (79)$$

Substituting for V_A and V_B from (76-77), (52) in chapter 2 is obtained. This analysis relates potential barrier to gate voltage and voltage at the intrinsic drain. The voltage at intrinsic drain can be related to terminal voltages either using the analysis presented in chapter 2 (55-56) or more accurately as an empirical relationship constructed from experimental data [41].

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