ELECTRICAL CHARACTERISTICS AND STABILITY OF NOVEL $Mg_xZn_{1-x}O$ ($0 \leq x \leq 0.06$) THIN FILM TRANSISTORS

by

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A Dissertation submitted to the

Graduate School-New Brunswick

Rutgers, The State University of New Jersey

in partial fulfillment of the requirements

for the degree of

Doctor of Philosophy

Graduate Program in Electrical and Computer Engineering

written under the direction of

Professor Yicheng Lu

and approved by

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New Brunswick, New Jersey

May, 2013

ABSTRACT OF THE DISSERTATION

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Prof. Yicheng Lu

Thin Film Transistor (TFT) is emerging for large area electronics and systems. TFT applications include displays, photovoltaics, sensors, smart labels, lighting, integrated logic devices, and embedded power sources. However, the conventional amorphous silicon (a-Si) TFTs, which have dominated display technologies as switch devices in control circuitry, are facing severe challenges due to its low electron mobility ($\leqq 1$ $cm^2/V\text{-}s$) and opacity. The advanced display systems demand the new TFT technology with low power consumption, high resolution, large area, and fast refresh rate. There has been increasing interest in the use of oxide-based TFTs as electronic back-plane switching devices for the next generation of large area flat-panel display applications. Zinc oxide (ZnO) has been receiving considerable attention as a promising oxide semiconductor for TFT technology for the future displays due to its higher electron mobility (~10-50 $cm^2/V\text{-}s$), transparency in visible light region, and superior radiation hardness over the a-Si TFTs. To implement ZnO TFTs into novel display systems, stability of ZnO TFTs is the most critical issue and has to be examined.

The aim of this dissertation research is to study and enhance electrical characteristics and stability of ZnO TFTs using the ternary $Mg_xZn_{1-x}O$ ($0 \leq x \leq 0.06$) as the TFT channel layer. The $Mg_xZn_{1-x}O$ (MZO) is grown by Metal Organic Chemical Vapor Deposition (MOCVD) through *in-situ* alloying of MgO and ZnO. Mg composition in the $Mg_xZn_{1-x}O$ is controlled below 6% ($x \leq 0.06$) to avoid alloying disorder induced degradation. In the ternary compound $Mg_xZn_{1-x}O$, the incorporation of Mg into ZnO along with stronger Mg-O bonding effectively suppresses the oxygen vacancy related defects and improves the electrical characteristics of ZnO-based TFTs. The lower subthreshod slope and higher field effect mobility are obtained in MZO TFTs. In addition, MZO TFTs technology exhibits superior thermal stability. Under a negative bias stress (NBS) testing, MZO TFTs show smaller negative shift of threshold voltages than that of the ZnO counterpart, owing to less ionization and migration of oxygen vacancies.

The new MZO TFTs technology presents a great impact on the future classes of low cost and large area electronic applications, such as display systems, sensor arrays, and solar energy conversion.

DEDICATION

To my mentors and my love ones:

Dr. Chiung-Chung Ku, who always acts as role model for me and gives me everything I need to pursue my dreams.

Prof. Yicheng Lu, who gave me this opportunity to polish my skills, knowledge and advises me on research and life.

Ming-Hui Liu, who sacrifices her life to take care of me since the first day I was born.

Clare Tang, who always supports and encourages me since first day we met.

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ACKNOWLEDGEMENTS

First, I would like to express my deepest gratitude to my dissertation advisor, Professor Yicheng Lu, for bringing out my potential, for his unwavering support, guidance, encouragement, and patience. Thank you for laying down the solid foundation for my future career.

I would like to thank my dissertation committee members, Prof. Jaeseok Jeon, Prof. Wei Jiang, Prof. Warren Lai, and Prof. Dunbar P. Birnie for taking time off of their busy schedule to review and critique my dissertation. In addition, I would like to thank Dr. D.C.Look who always gives me his insightful suggestions on my papers.

I would like to thank my colleagues in Prof. Lu's research group, who have provided support throughout my work. Dr. Jian Zhong for training me in microelectronic device fabrication and characterization; Dr. Chung-Chen Kuo for teaching me in mask design and implementing automation software for electrical testing facility; Dr. Pavel .I Reyes for setting up electrical and optical testing facility and Dr. Ziqing Duan for material growth and film characterizations. Mr. Yang Zhang, Mr. Rui Li, Mr. Wen-Chiang Hong and Mr. Tengfei Xu, for their help in the many facets of my work in the group, and the great friendship. Working with you guys is such an honor and I always enjoy the time when we have discussions. I would like to thank other PhD students and post-doctors who help me and discuss with me including Lei Lin, Weiwei Song, Jun Tan, Yi Xu and Dr. Chien-Lan Hseuh. I always enjoy the time we spent together.

I would like to thank my family (my father Chiung-Chung, my mother Ming-Hui , my sister Crystal and my future wife Clare, my aunts and uncles. I would like to thank them for providing me this chance to study abroad and take care of me when I am in US.

This work has been supported in part by the United States Air Force Office of Scientific Research (AFOSR) under Grant No. FA9550-08-01-0452, and by the National Science Foundation (NSF) under Grant No. ECCS 1002178. Research carried out (in part) at the Center for Functional Nanomaterials, Brookhaven National Laboratory, which is supported by the U.S.Department of Energy, Office of Basic Energy Sciences, under Contract No.DE-AC02-98CH10886.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Chapter 1

Introduction

1.1. Motivation

Thin Film Transistor (TFT) is a critically important device for flexible and large area electronics. TFT applications include integrated displays, photovoltaics, embedded power sources, sensing devices, smart labels, lighting, and integrated logic devices. Hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) TFTs are the industry standard for the switching and drive circuitry of monolithic active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED) technology. Overwhelming advantages in favor of poly-Si TFTs are motivated by the need to address low electron field effect mobility (<1 cm^2-$V^{-1}S^{-1}$) associated with a-Si TFTs. However, undesirable large off state leakage current (>10^{-10} A) and high processing temperature are challenges in poly-Si TFT development. As novel displays require low power consumption, high resolution, large area and fast refresh rate, Si based TFTs cannot be utilized in novel 3D and high definition (HD) displays. There has been increasing interest in the use of oxide based TFTs as electronic back-plane switching devices for the next generation large area flat-panel display applications. Zinc oxide (ZnO) is receiving considerable attention as an alternative TFT technology due to high transparency in the visible region, high ON-OFF ratio. ZnO based TFT technology is emerging for flexible and large area electronics and systems. These applications include integrated displays, photovoltaics, embedded power sources, sensing devices, smart labels, lighting, and integrated logic devices.

The aim of this research work is to develop a novel ZnO based TFT technology through metal-organic chemical vapor deposition (MOCVD) technique for channel growth. Particularly, a novel $Mg_xZn_{1-x}O$ (MZO) TFTs technology is proposed and demonstrated utilizing in-situ alloying of MgO and ZnO to form ternary $Mg_xZn_{1-x}O$ ($0 \leq x \leq 0.06$) as the TFT channel layer. The new MZO TFTs feature several advantages including higher field effect mobility, lower subthreshold swing, superior thermal stability and greater negative bias stress stability. This ZnO-based TFT technology can later serve as the active sensing platform for sensor arrays and core building block for the reconfigurable sensing systems. The novel ZnO based TFTs technology will be demonstrated by development and optimization of different processes: (i) high quality growth of ZnO channel layer by MOCVD (ii) improvement of ZnO TFT characteristics by post oxygen annealing for channel layer (iii) further enhancement of ZnO based TFT characteristics via in-situ doping of Mg into ZnO channel layer. The work utilizes MOCVD technique as the channel growth method since it provides a systematic way to study in-situ doping and composition dependent characteristics of ZnO based TFTs. This work seeks to show by utilizing novel in-situ Mg doping, we can achieve high performance ZnO based TFTs for the future large area electronic applications.

1.2. Objectives and Scope of Work

The objective of this research is to design, fabricate and characterize the novel ZnO based TFT technology. The scope of this study covers:

(1) Development, design and characterization of the ZnO TFTs through optimization of MOCVD growth of channel layer in conjunction with TFT structure design.

(2) Improvement of ZnO TFTs including electrical characteristics and negative bias stress stability through post oxygen annealing.

(3) Demonstration of novel Mg doped ZnO (MZO) TFT technology through development of in-situ Mg doping technique and studying associated electrical characteristics and stability issues.

1.3. Organization of the Dissertation

After establishing the motivation and the specific objectives and scope of this research in Chapter 1, a review of the related work on ZnO-based TFT technology is presented in Chapter 2. Chapter 2 also provides a background on stability issues of ZnO TFTs. Chapters 3 through 6 will focus on development ZnO based TFT technology and novel MZO TFT technology. In particular: Chapter 3 demonstrates the fabrication, design and electrical characteristics of ZnO TFTs grown by MOCVD technique. Chapter 4 deals with the improvement of electrical characteristics and stability against NBS in ZnO TFT through post oxygen annealing. Chapter 5 presents the development of MZO TFT technology via in-situ alloying and its thermal stability results. Chapter 6 discusses the enhancement of negative bias stress (NBS) stability in MZO TFTs. Finally, Chapter 7 summarizes the results of the dissertation research and presents further work.

Chapter 2

Technical Background

In recent years, ZnO TFTs have attracted increasing attention due to their high electron mobility, transparency to visible light, and superior radiation hardness. ZnO TFTs are potentially much less expensive than ITO-based TFTs due to materials costs. Currently, the most significant contribution of TFT technology is in large area electronic applications such as displays, photovoltaics, embedded power sources, sensing devices, smart labels, lighting, and integrated logic devices. For application of TFTs as the driver/switch devices in a display system, stabilities such as thermal stability and bias stress stability are key pre-requisites. The brightness of each pixel is determined by the drain current of the driving TFT. TFTs must remain stable over time; any shift in threshold voltage would change the brightness of individual pixels, introducing non-uniformity of displays. Development of stable and high performance ZnO TFTs has recently become one of the most urgent and important focus of ZnO TFTs research. Ongoing research is geared toward ZnO TFTs with high electron mobility, low subthreshold swing, high on-off ratio, and enhanced stability. In this chapter, the role of ZnO in the field of TFT technology will be discussed. ZnO has been proven to be a promising material in fabricating TFT devices as it possesses high electron mobility, capability of low temperature growth on various substrates and ability to perform wet etching process. Various TFT technologies based on ZnO and related stability issues will also be discussed in this chapter.

2.1. Structures and Operations of TFTs

Thin film transistors (TFTs) are a class of field effect transistors in which the current through the channel is modulated on the same basic principle as the MOS transistors. Unlike the MOSFETs where the substrate material is the bulk semiconductor, thin films of the semiconductor materials are deposited on the substrates to form the channel layers of TFTs. In addition, the output current of TFTs is induced by the transportation of majority carriers in the channel while the channel of MOSFETs is an inversion layer consisting of the minority carriers. A typical TFT under normal operation in the linear region and saturation region is shown in Figure 2.1. The application of a positive bias to the gate electrode induces the accumulation of electrons in the channel layer consisting of an n-type semiconductor. At the same time, the positive input voltage at the drain leads to the flow of current as electrons flow from source to the drain.

There are four basic TFT structures: staggered top gate, co-planar top gate, inverted co-planar top gate and inverted staggered bottom gate, as show in Figure 2.2. Electrode placement distinguished the various structures, i.e electrodes are place on opposite sides of semiconductor-insulator interface for staggered structures, while electrodes are place on the same side of the interface for the co-planar structures.

Process integration-related issues can motivate the use of different structures. In both bottom-gate structures, the insulator is deposited first. If the insulator is deposited using a glow discharge process such as RF sputtering or plasma enhanced chemical vapor deposition, the plasma induced damage to the channel layer can possibly be reduced using this structure. In addition, high quality SiO_2 grown by dry oxidation on silicon can be utilized by bottom gate structures where silicon substrates serve as bottom gate. The

co-planar structure is difficult to implement in some technologies such as a:Si-H. a:Si-H TFTs utilize ion implantation to form the ohmic contact to the semiconductor channel. Since the maximum processing temperature of a:Si-H TFTs is ~350° C, damage from implantation cannot be recovered. This implies that the channel must be protected during implantation. If the insulator is used as implantation block, there is no source/drain-to gate overlap. Without this overlap, the series resistance increases and hinders the carrier injection.

Invention of the first thin film transistor, as it is known today, is credited to P.K.Weimer (1962) [3]. These initial n-type TFTs fabricated by Weimer used a top gate staggered structure with microcrystalline CdS deposited by evaporation as the channel layer. SiO (silicon monoxide) grown by thermal evaporation was used as gate dielectric and gold for the gate/source/drain electrodes. All patterning was done via shadow masks, channel lengths of 5 to 50μm were obtained. These early devices showed field effect mobilities of 1.1 cm^2-$V^{-1}S^{-1}$ and on-off ratio of 10^1.

Since Weimer's pioneer work, TFTs based on a wide variety of channel materials including CdS, CdSe, amorphous and polycrystalline silicon have been developed. The most dominant TFT technology is based on hydrogenated amorphous silicon (a-Si:H), which are commonly employed as control circuitry in active matrix liquid crystal displays (AMLCDs). Initially, amorphous silicon was nearly unusable for devices because of very large defect states. In order to reach the goal to produce the full potential of devices built on amorphous silicon, it is important to completely understand and control the defect density. In purely crystalline silicon, there is a complete lack of states within the bandgap and delocalized conduction and valence bands begin abruptly at the band edges. In

amorphous silicon, there is a smooth transition between the localized states (where carriers can become trapped) and the states which extend throughout the lattice. Thus, electrons below the band gap can become trapped in these localized states while electrons with energy above the gap will be able to conduct DC current. Spear and Lecomber discovered that the defect density could be greatly reduced after hydrogenation, and also that a-Si:H could exhibit both n-type and p-type conductivity as dopant were added [4]. Brodski *et. al.* later quantified the importance of hydrogen in the network in 1977 [5]. Hydrogen passivates the silicon dangling bonds and can reduce deep defect density from nearly 10^{19} cm^{-3} to 10^{15} cm^{-3}. As a result of these investigations, amorphous silicon has become widely used in TFT devices and remains a dominant role in driver devices of LCD displays. The benefits of large area and low temperature deposition outweigh the downside of decreased device performance as compared to crystalline silicon in certain applications such as LCD displays. Currently, high performance a-Si:H TFTs typically exhibit field effect mobilities of 1.5 to 2.0 cm^2-$V^{-1}S^{-1}$ with a maximum processing temperature of 300 ^oC [6].

In addition to silicon TFTs, another class of TFTs consists of those which employ organic materials as the channel layer. [7]. Most of these organic channel materials are p-type. These TFTs normally exhibit mobilities of 10^{-3} cm^2-$V^{-1}S^{-1}$. However, the low mobility of these organic TFTs is offset by the low cost deposition such as spin coating or printing. Furthermore, the processing temperature of these TFTs is below 300 $^\circ$ C, allowing devices to be built on plastic substrates.

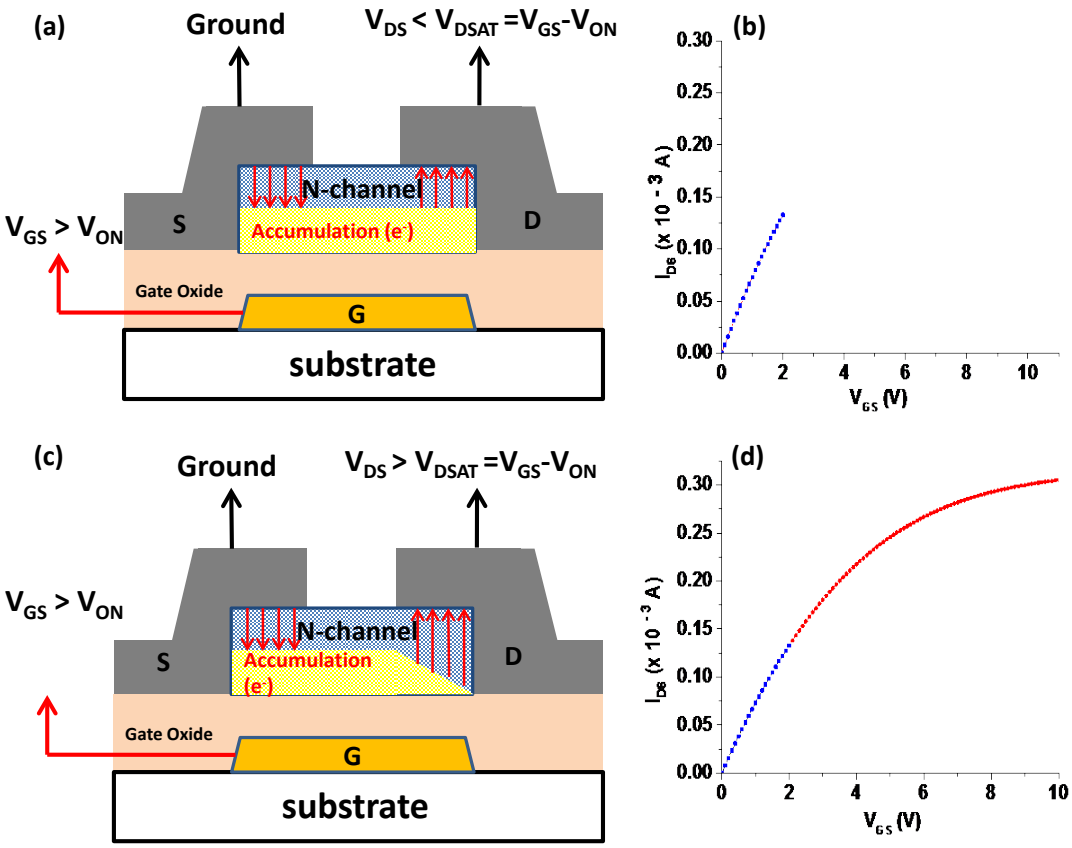

Figure 2.1 Schematics representing (a) TFT operation in linear region (b) I_{ds}-V_{ds} characteristic in linear region (c) TFT operation in saturation region (d) I_{ds}-V_{ds}characteristic in saturation region.

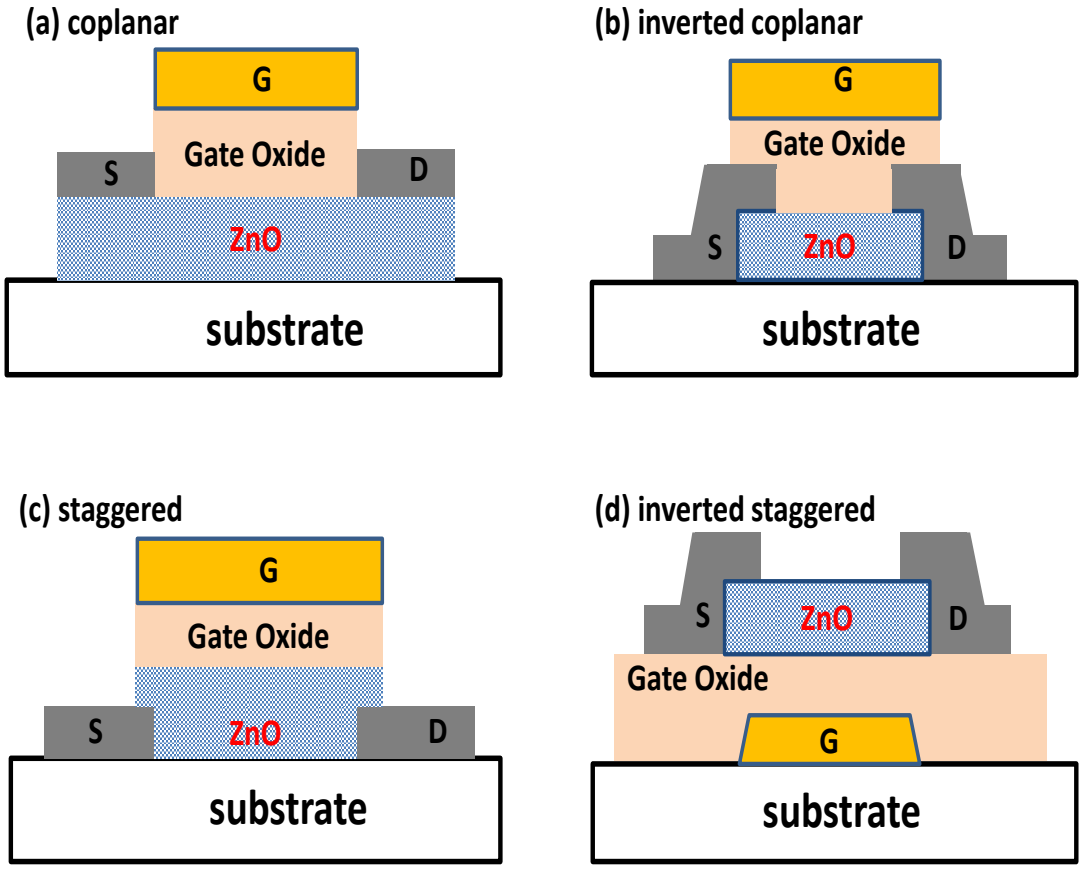

Figure 2.2 The schematic cross-section views of the (a) coplanar top gate (b) inverted coplanar top gate (c) staggered top gate TFT and (d) inverted staggered bottom gate structures.

2.2. ZnO Materials for TFT Active Channel Layer

ZnO has numerous attractive characteristics for electronic and optoelectronic devices. With direct bandgap energy of 3.37 eV, it is transparent in visible light and can be operated in UV to blue wavelength region. The room temperature electron Hall mobility of single crystalline ZnO is ~ 200cm^2- $V^{-1}S^{-1}$ which is lower than GaN, however, ZnO has higher saturation velocity than GaN. ZnO exhibits better radiation resistance than GaN, making it a possible candidate for future applications in space and nuclear power plant. ZnO can be grown on inexpensive substrates such as glass and flexible substrates, at relatively low temperature. The high exciton binding energy of 60m eV as compared to GaN ~ 25 m eV enhances the luminescence efficiency of light emission. The direct bandgap and high exciton binding energy make it attractive for optoelectronic devices such as ultraviolet (UV) photodetectors and blue UV light emitters such as light emitting diodes and laser diodes. Other applications include surface acoustic wave devices, gas sensors, and transparent conducting films for solar cells. The potential of ZnO and its novel devices is further broadened by bandgap engineering. Tuning bandgap via divalent substitution on the cation site to form heterostructures of ZnO has been demonstrated. Bandgap energy of 3.0 eV is achieved by doping with Cd^{2+} while Mg^{2+} increases the bandgap energy to 4.0 eV.

Perhaps one of the most extensive research activities of ZnO associated with display technologies in early days was to replace ITO based transparent conducting oxide (TCO) due to the cost issue. TCO is a class of large band gap (typically Eg>3.1eV due to the large electronegativity of oxygen in n-TCOs) materials that exhibits a high level of optical transparency (80%-90%) and conductivity. Currently, the most dominant

switching and driver devices in displays are silicon based TFTs. Because of the opacity of silicon, the light emitting from backplane is blocked by those devices, reducing the fill factor and effective pixel area. Since the resolution and contrast of displays are highly dependent on the effective area of pixel, it is important to increase the pixel area and its fill factor. Thus, interconnects in displays have been utilized by TCO materials.

Advances in deposition technologies of ZnO thin films open up a new area of ZnO based devices. The ability to control background carrier density in ZnO thin films makes it possible to modulate electron concentration via applied electric field. The modulation of the conductivity in semiconductor layer by applying electric signal is essential to the operation of active devices. Demonstrations of ZnO TFTs were first reported in 2003 and publications related to ZnO based TFTs have tremendously increased. Superior transport properties of ZnO TFTs over silicon TFTs are attributed to the different types of bonding. Figure 2.3 depicts the schematic orbital drawing of carrier transport path in covalent and ionic semiconductors [1].

In typical n-type covalent material such as Si, the conduction band minimum (CBM) is consisted of asymmetric sp orbital while valence band maximum (VBM) is constituted by pure p states. Figure 2.4 shows orbitals, structures and distribution of density of states N(E) of crystalline and amorphous Si [2]. In this case, disorder will affect the angular and the space position of atoms, leading to the localized electrons appeared in the band edges as one moves from ordered to disordered structure such as nanocrystalline silicon. This strong localization leads to an appearance of continuous distribution of density of states between CBM where electrons are delocalized and VBM where holes are delocalized. In highly disordered system like amorphous silicon, the

Fermi level (E_F) is associated with permitted localized states, separating localized fill states from empty ones. In this case, delocalized states and localized states (tail states) are separated by an energy called mobility edge. Carrier mobility drops few orders of magnitude when going from delocalized states to localized states. Defects such as vacancies are associated with disorder highly affecting the distribution of density of states.

The n-type ionic oxide semiconductors such as ZnO exhibit a pronounced metal - like CBM composed of vacant s-orbitals of a cation, and contribution of oxygen 2p orbitals, which are dominant at VBM, is rather small. Figure 2.5 depicts the orbitals, structures and N(E) of ZnO [2]. As the CBM state is more than 90% localized in symmetric s orbitals of metals, its energy is mainly dependent on interaction between second neighboring metal sites and does not depend on interaction between metal s orbitals and oxygen p orbitals. Therefore, the effect of disorder on the conduction band states is found to be weak, and mainly dependent on the variation of metal-metal distance. In addition, the spatial spread of metal s orbitals is so large that direct overlap between s orbitals of neighboring metal atoms is possible in heavy metal oxides, leading to a small electron effective mass in these metal oxides. The direct overlapping of corresponding metal cations ideally results in no localized states. The carriers may retain the mobility as their crystalline counterparts even in highly disordered systems. Contrary to what is observed in covalent semiconductors, disorder does not introduce delocalized states below the band edges and therefore will not affect mobility as strong as with covalent semiconductors such as silicon.

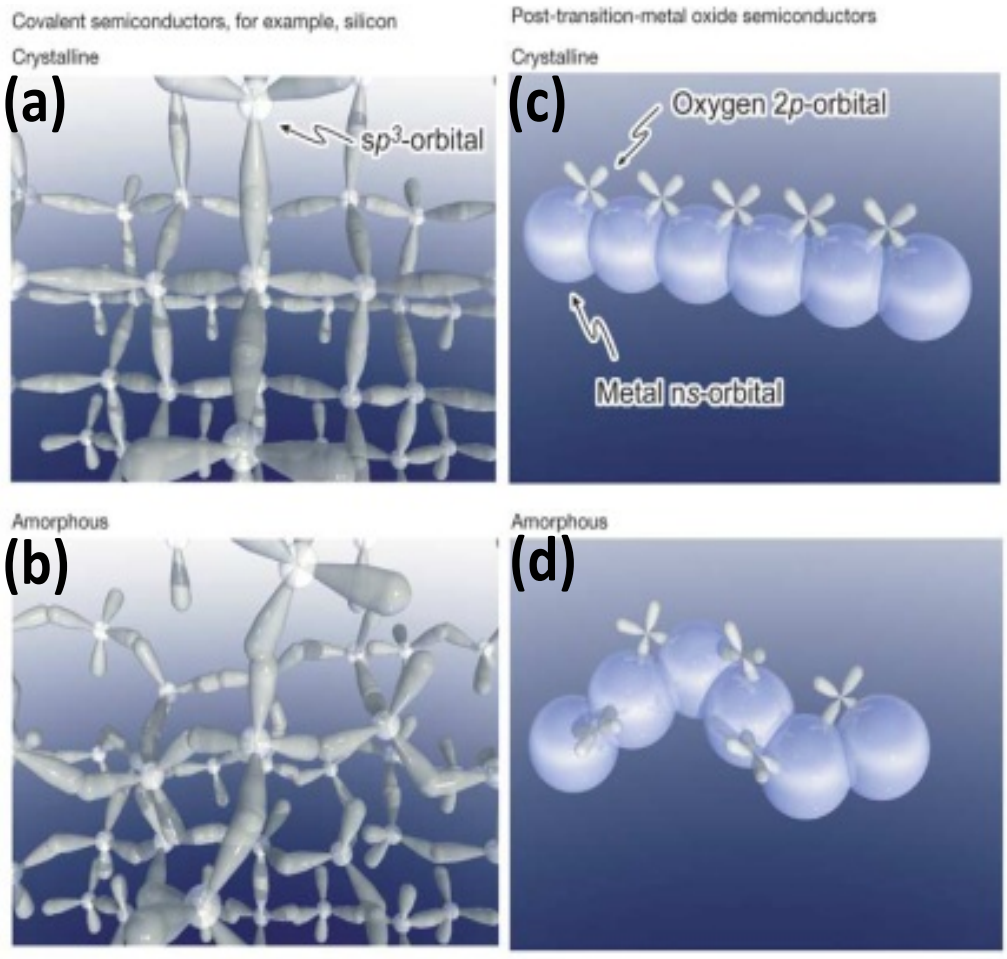

Figure. 2.3 Schematic orbital drawing of carrier transport path in (a) crystalline covalent Si semiconductors (b) amorphous covalent Si semiconductors (c) crystalline ionic oxide semiconductors (d) amorphous ionic oxide semiconductors. (Ref. [1])

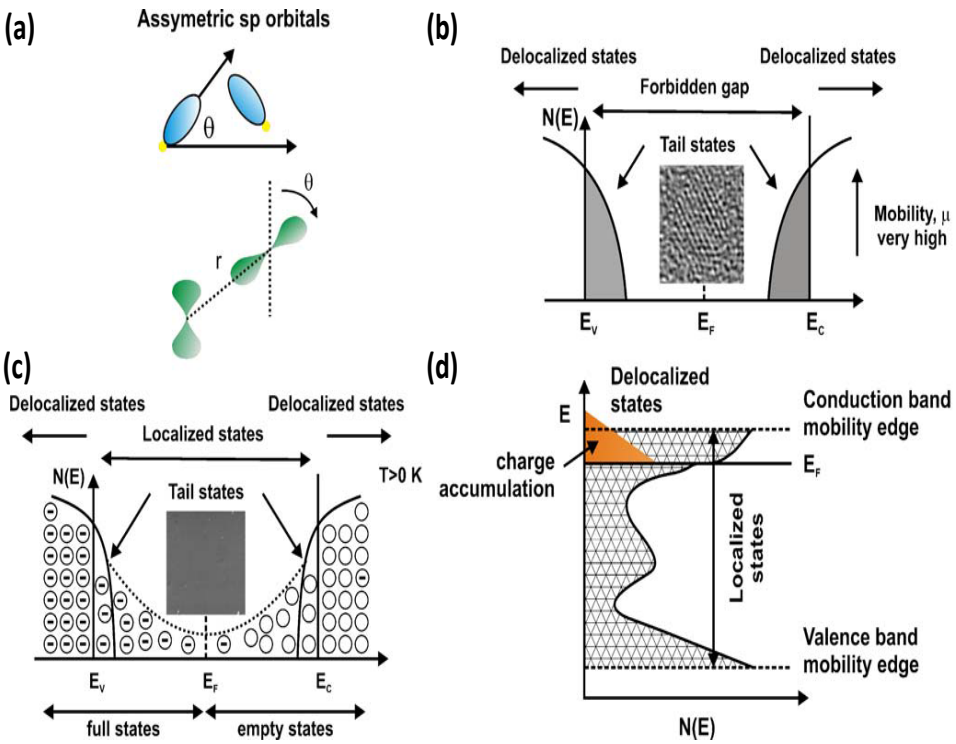

Figure 2.4 Schematic figures representing orbitals, structures and density of states N(E) of covalent Si semiconductor. (a) sp orbitals (b) N(E) distribution of crystalline Si. (c) N(E) distribution of amorphous Si (d) schematic of N(E) gap state distribution in the channel of amorphous Si TFTs. (Ref. [2])

Amorphous silicon (a-Si) TFTs currently dominate the display market due to their uniformity over large area, low cost of fabrication and mature technology. However, the small field effect mobility of a-Si TFTs (< $1cm^2$-$V^{-1}s^{-1}$) cannot drive large size (> 55inches), high resolution and high frame rates (> 120Hz) display systems. To overcome this issue, ZnO based TFTs have been viewed as an alternative approach to realize reliable, high resolution and high frame rates 3D display systems. It is because ZnO based TFTs possess numerous advantages including higher electron mobility (~10-50cm^2/V-s), transparency in visible light region, and superior radiation hardness over amorphous silicon (a-Si) TFTs. To meet requirements for future display systems, reliability issues of ZnO based TFTs such as bias stress stability and temperature stability have to be addressed and improved.

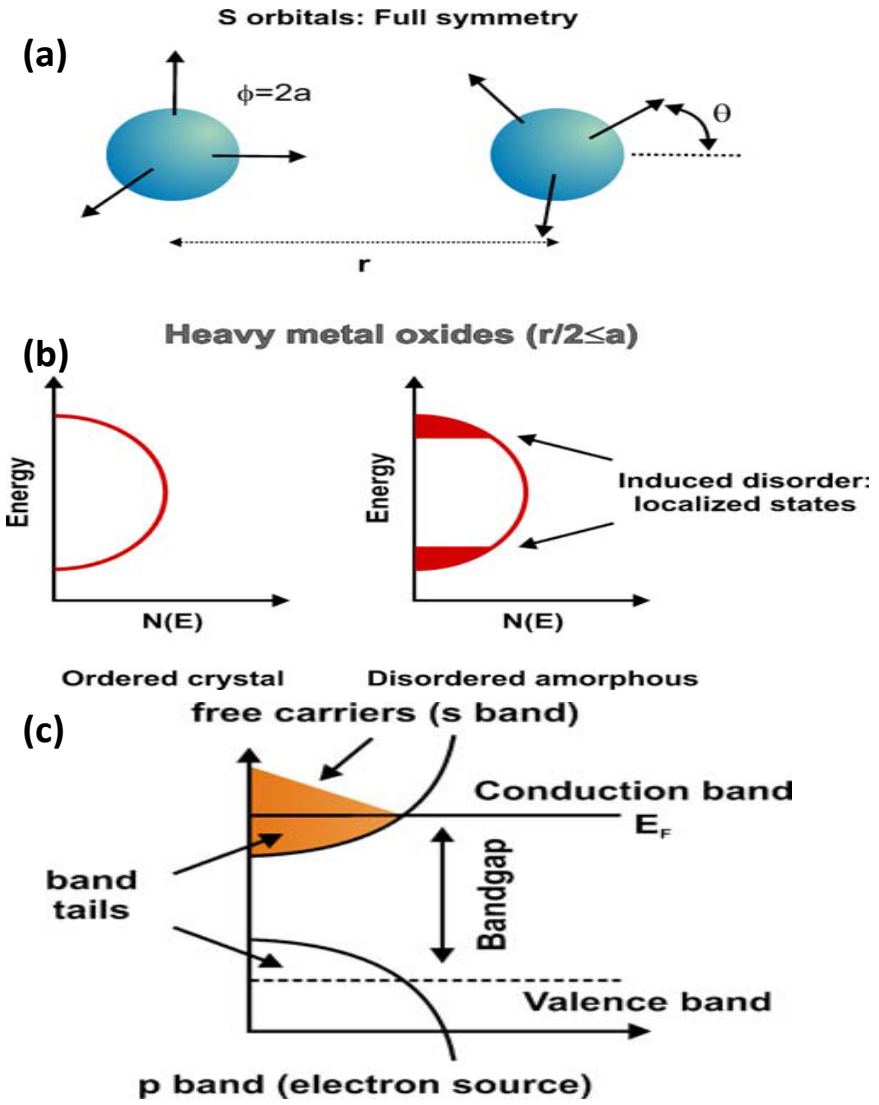

Figure 2.5 Schematics representing (a) symmetric s orbitals (b) density of states of distribution N(E) of ZnO and the role of disorder of it (c) carrier distribution of in ZnO used as channel layer in TFTs. (Ref. [2])

2.3. ZnO TFT Devices Technologies

The first reports on oxide semiconductor TFTs were based on zinc oxide. Demonstration of the ZnO TFTs by Masuda [8], Hoffman [9], and Garcia [10] in 2003 sets the milestone on oxide based transparent TFTs and extensively research activities have been conducted all over the world. Masuda *et al.* fabricated bottom-gate ZnO TFTs by using PLD. The ZnO channel layer was grown at 450 ° C with a gate insulator of SiO_2/SiN_x to reduce the leakage current. The on-off ratio reached to 10^5 with a field effect mobility of 0.03 cm^2-$V^{-1}S^{-1}$. Hoffman *et al.* fabricated ZnO TFTs using ion beam sputtering. The carrier concentration of ZnO channel was reduced after rapid thermal annealing at 600 – 800 ° C in O_2 ambient. On-off ratio of 10^7 with an enhancement mode operation was reported. Threshold voltages of TFTs were 10-20 V with field effect mobilities of 0.3 to 2.5 cm^2-$V^{-1}S^{-1}$. Garcia *et al.* reported on a room temperature process of magnetron RF sputtered ZnO TFT built on glass substrates.

After the first few literatures of ZnO TFTs, other authors have studied ZnO based TFTs with RF sputtering that eliminates post-deposition annealing process. Fortunato [11] *et al.* and Garcia [12] *et al.* optimized the deposition parameters of pressure and power to achieve high performance ZnO TFTs. The electrical characterization of ZnO TFTs is affected by O2 partial pressure. TFTs with field effect mobility of 25 cm^2-$V^{-1}S^{-1}$ were reported. Furthermore, ZnO TFT built on flexible substrates were also demonstrated [12].

Solution based deposition techniques such as sol-gel and chemical bath deposition also have been developed to fabricate ZnO based TFT [13,14,15]. High temperature curing process is usually employed to achieve proper crystallization and to remove the

volatile components in sol-gel samples. Norris *et al.* used sol-gel technology with zinc nitrate and glycine precursor solution to fabricate ZnO TFT and annealed devices at 700 ° C [13]. The channel mobility and on-off ratio of these TFTs are 0.2 cm^2-$V^{-1}S^{-1}$ and 10^7, respectively. Li *et al.* used a precursor solution of zinc acetate dehydrate, 2-ethanolamine and methoxyethanol and optimized respective ratio to obtain high performance ZnO TFTs. Devices annealed at 400-500 ° C showed channel mobilities, threshold voltages and on-off ratios of 5-6 cm^2-$V^{-1}S^{-1}$, 20V and 10^5, respectively [14]. Cheng *et al.* utilized a chemical bath including zinc nitrite and dimethylamineborane at 60 ° C to grow ZnO channel layers. TFTs fabricated with these films exhibited channel mobilities and on-off ration of 0.25 cm^2-$V^{-1}S^{-1}$ and 10^5, respectively [15].

MOCVD also have been explored to deposit ZnO channel layers for TFTs. Our group first reported ZnO TFTs with channel layers grown by MOCVD at 400-500 ° C on both glass and R- sapphire substrates. ZnO TFT built on glass shows an on-off ratio of 10^4 and field effect mobility of 4.0 cm^2-$V^{-1}S^{-1}$. The ZnO TFT grown epitaxially on r-sapphire substrate exhibits field effect mobility of 35 cm^2-$V^{-1}S^{-1}$ and on-off ratio of 10^8 [16]. Jo *et al.* fabricated ZnO TFTs with depletion mode operation and attributed it to the oxygen deficiencies during the MOCVD deposition [17]. By increasing oxidation time during growth, enhancement mode devices with mobility of 15 cm^2-$V^{-1}S^{-1}$, on-off ratio of 10^7 and threshold voltage of 5V were realized. Levy *et al.* demonstrated fabrication of gate insulator and semiconductor channel layer by using ALD [18]. ZnO TFTs were fabricated at relatively low temperature of 200 ° C, showing mobilities of 20 cm^2-$V^{-1}S^{-1}$ without visible hysteresis.

Bayraktaroglu *et al.* reported microwave performance of ZnO TFTs grown by PLD method [19]. ZnO TFTs with W/L ratio of 25μm/2μm and source and drain contact overlap regions of 1μm exhibited high on-off ratio of 10^{12}, low subthreshold slope of 109 mV/dec and high field effect mobility of 110 cm^2-$V^{-1}S^{-1}$. The current gain cut-off frequency (f_T) reached 500MHz with a maximum operating frequency (f_{max}) of 400MHz. With smaller gate length of 1.2μm and smaller source and drain contact overlap regions of 0.5μm, current gain cut-off frequency (f_T) and maximum operating frequency of ZnO TFTs reached 2.45 GHz and 7.45 GHz, respectively [20].

Several groups studied the electron transport behavior and operation of ZnO based TFTs. Hossain *et al.* analyzed the grain boundary effects for polycrystalline ZnO TFTs [21]. The channel layer of ZnO TFTs was simplified as a thin layer with vertical grain boundaries containing a high density of deep level traps, which would capture electrons. This would introduce the depletion of electrons around the grain boundaries hence the exposure of ionized donors, which in turn results in band bending around grain boundaries. As a result, the energy band diagram of grain boundaries forms double Schottky barriers and is treated as main obstacle for current flow in the channel. The simulation showed a decrease in grain boundary barrier height with increasing free carrier concentration and a decrease in channel mobility as the number of grain boundaries in the channel increases. Hwang *et al.* deposited channel layers of ZnO TFTs by using rf magnetron sputtering under different rf power [22]. Different grain sizes of ZnO films were found and analyzed by high resolution TEM. The field effect mobility of ZnO TFTs increased from 0.04 cm^2-$V^{-1}S^{-1}$ to 2.45 cm^2-$V^{-1}S^{-1}$ as grain size increases from 7nm to 16nm. I.P. Steinke *et al.* proposed a “Percolation model” for determining threshold

voltages of ZnO TFTs with nanocrystalline channel layer [23]. Electrons in the channel layer may either populate the conduction band within a grain or be trapped at grain boundary between neighboring grains. The relative distribution of the electrons over these states determines the conductance of the grains and of the grain boundaries. The extracted threshold voltage increased as the energy of trap level decreases and saturates for E_C-E_T ~ $6k_BT$. An increase in trap density at the grain boundaries increased the threshold voltage because a lager applied bias is needed to fill all the trap states. A decrease in temperature also increased the threshold voltage since the carriers are more likely to occupy low energy trap states at the grain boundaries rather than the high energy conduction band states within the grains.

Experiments have been reported on the influence of different gate dielectrics on ZnO TFT properties. The use of high-k dielectrics allows for thicker gate dielectrics leading to reduced gate leakage and increased capacitive coupling between ZnO layer and the gate dielectric. It will enable stable operation of TFTs with high output currents at low operating voltages. There have been several reports on promising alternatives such as Si_3N_4 [24], SiN_x (ε_r=6) [25], (Ba,Sr)TiO_3 (ε_r=16-500) [26,27,28], Al_2O_3 (ε_r=7) [29], HfO_2 (ε_r=30) [30], and $Bi_{1.5}Zn_{1.0}NB_{1.5}O_7$ (ε_r=51) [31]. However, the use of high-k dielectrics does not mitigate electrical degradation caused by carrier trapping at the gate dielectric-channel interface.

As the next generation driver devices in large area electronics, ZnO based TFTs have been employed to active matrix displays. Hirao *et al.* fabricated AMLCD with staggered top gate ZnO TFTs which utilizes a SiN_X gate insulator [32]. These TFTs show channel mobilities of 50 cm^2-$V^{-1}S^{-1}$. Park *et al.* [33] demonstrated a transparent

AMOLED display with coplanar bottom gate ZnO TFTs which utilizes an Al_2O_3 gate insulator. In addition, the ZnO deposition process is compatible with plastic substrates. Yamauchi *et al.* reported on fabrication of an integrated ZnO TFT-OLED device [34]. ZnO channel layer is deposited via sputtering and OLED is deposited directly on different TFT drain materials including AZO and ITO. As ITO is used as the drain material/OLED contact, no luminance is detected indicating that ZnO is essential for electron injection. These prototypes show that ZnO TFTs are promising to be integrated into driver devices of display system.

2.4. Reliability Issues in ZnO-Based TFTs

For the application of TFTs as the driver/switch devices in the display, stability against bias stress is the key pre-requisite. The brightness of each pixel is dependent on the drain current of the driving TFT. TFTs must remain stable over time, since any shift in threshold voltage would change the brightness of individual pixel and introduce non-uniformity of displays. Based on understanding developed for a:Si-H TFTs, bias stressing may lead to instabilities such as charge trapping and defect formation in the active channel, in the gate dielectric or at the channel/dielectric interface. It might also be expected that an increased temperature could lead to additional instabilities. Furthermore, metal oxides are well known as gas sensors, and one might also expect instabilities due to channel surface/ambient interaction

2.4.1. Bias Stress Stability of ZnO Based TFTs

The first bias stressing study on ZnO based TFTs was performed by Cross [35] on staggered bottom gate (SBG) ZnO TFTs consisting of an RF magnetron sputtered 100nm

ZnO channel with a 150 nm thermally grown SiO_2 dielectric. Two mechanisms are accounted for bias stress instabilities. Low field (<1MV/cm) instabilities are result of charge trapping at or near gate dielectric/channel interface coincident with negligible change in subthreshold swing. At high fields (>1MV/cm), instabilities resulted from creation of additional defect state concurrent with degraded subthreshold swing. The demarcation between low field stress and high field stress is found to be ~30 V for devices with 150 nm thick SiO_2 dielectric layer, corresponding to an applied field of 2 MV/cm. The threshold voltage shifted in the direction of the applied voltage, with a positive bias stress inducing a positive shift and a negative bias stress inducing a negative shift. Cross *et al.* also studied on the bias stress stability of ZnO TFTs with two different dielectric layers of SiO_2 and SiN_X deposited at high temperature (>1000 $^\circ$ C) [36]. In these devices, ZnO TFTs with SiN_X appeared to exhibit better stability against bias stress.

Several studies indicated that defects and associated charge carriers in the channel affect electrical instability in ZnO based TFTs. Kamada *et al.* [37] studied channel stoichiometry on bias instability of ZnO TFTs deposited by RF sputtering under different oxygen partial pressures (Zn-rich and O-rich). The TFT with Zn-rich ZnO includes a larger trap density near the conduction band (CB) of ZnO. As a result, the subthreshold characteristic is deteriorated. For O-rich ZnO TFTs under positive bias stress (PBS), the transfer characteristics positively shift as the stress time increases. A linear relationship between V_{th} shift and the logarithmic stress time without degradation of subthreshold swing and field effect mobility suggests that the bias stress instability may be related to the negative charge trapping in the gate insulator and/or channel/dielectric interface. Negatively shifts of transfer characteristics were observed under negative bias stress

(NBS). The origin of ΔV_{th} under NBS was thought to be related to the electrically activation of donor trap defects by the negative bias. On the contrary, transfer characteristics of Zn-rich ZnO TFTs are negatively shifted regardless of the polarities of the gate bias stresses. In addition to charge trapping, the electrically active traps may be also accounted for the bias stress instabilities under PBS. Kim [38] reported the effect of Hf doping on negative bias stress stability in ZnO TFTs. Small amount of Hf with 0.8 atom % was added into ZnO target. The improvement of ΔV_{on} against bias stress was attributed to the reduction of interface trap density between channel and dielectric layer. The reduction of interface trap density may be related to the suppression of oxygen vacancies due to Hf ions acting as oxygen binders.

2.4.2. Surface/Ambient interaction on Bias Stress Stability

It is well known that ZnO is surface sensitive to molecules in the ambient atmosphere. For example, the adsorption of O_2 onto the surface of ZnO introduces an acceptor-like surface state: physisorbed O_2 is neutral when unoccupied and becomes chemisorbed and negatively charged $[O_2]^-$ when it captures (becomes occupied by) an electrons from the CB, As a result, $[O_2]^-$ causes in surface depletion. Similarly, H_2O can act as donor-like surface state whereas the interaction of H_2O with surface is more complex. Other molecules such as H_2, CO_2, ethanol, etc. can also interact with ZnO surfaces to produce changes in conductivity. Depicted in Figure 2.3 are sketches showing surface band bending after chemisorbed $[O_2]^-$ and $[H_2O]^+$. It can be therefore expected that when a staggered bottom gate (SBG) TFT channel is left unpassivated, the surface–adsorbed H_2O or other donors may lead to a parallel parasitic back channel conduction

path as shown in Figure 2.4. Likewise, the removal of adsorbed $[O_2]^-$ can also result in increased surface carrier density and conductivity.

Several studies have demonstrated that surface/ambient interactions can impact the stability of the unpassivated SBG TFTs [39-43]. With reference to simple equations for gas molecule adsorption (O_2 (gas) + $e^- \rightarrow O_2^-$ (ads)), Jeong *et. al.* [39] discuss how positive bias stressing can lead to field induced adsorption of O_2 and desorption of H_2O, as shown in Figure 2.5. Lopes *et al.*[40] report that exposure of unencapsulated 40nm RF sputtered IGZO SBG TFTs with 100nm thermal grown SiO_2 dielectrics to water vapor for 24h resulted in an accelerated V_{th} shift upon subsequent bias stressing as compared to unexposed samples. Liu *et al.* [41] found out that the stability of 50 nm RF magnetron sputtered IZO coplanar bottom TFTs with 300nm Si_3N_4 gate dielectrics is degraded when low field positive and negative bias stressing are conducted in the ambient rather than in vacuum. The authors attributed the enhanced degradation to interaction of O_2 and H_2O at the channel surface. Lee *et al.* [42] also found out that the negative bias stress induced negative V_{th} shifts in unpassivated IGZO SBG TFTs with SiN_X dielectrics were progressively worse for increasing relative humidity levels from 0% to 70% humidity. Because of uncontrolled interaction of the unpassivated channel with the ambient may lead to enhanced degradation of bias stress instabilities. These results indicate that the passivation of channel surface have to be considered for the commercial applications of ZnO based SBG TFTs

2.4.3. Thermal stability

For TFTs serving as driving/switching transistors in display systems, the variation of threshold voltages is critical. The brightness of each pixel is highly dependent on the

drain current of the driving/switching transistor. Any shift in threshold voltage of the driving/switching transistor will introduce non-uniformity of display. In addition, joule heating during TFT operation would cause an effective temperature variation in the range from 300K to 420K. Therefore, the temperature dependent threshold voltage shift in ZnO based TFTs should be studied and minimized.

Jeong *et al.* [44] studied the temperature stability of Al-Zn-Sn-O (AZTO) TFTs with top gate and bottom gate configurations. The bottom gate devices without a passivation layer on the AZTO channel layer showed larger threshold voltage shift after heating it from 298K to 398K. The naturally passivated top gate devices exhibited a smaller threshold voltage shift. It is proposed that the suitable passivation and lower defect density for the top gate TFT are responsible for its superior temperature stability. Ryu *et al.* [45] investigated the effect of the Sn/Zn ratio in Zn-In-Sn-O TFTs. The thermal stability of TFTs with a channel composition of Zn:In:Sn = 0.35:0.20:0.45 was dramatically improved, while those of the TFT devices with Zn:In:Sn = 0.45:0.20:0.35 and 0.40:0.20:0.40 suffered from deep level trap creation in the channel and charge trapping. The enhanced stability of the $Zn_{0.35}In_{0.20}Sn_{0.45}O$ TFT was attributed to low total trap density. The Sn atoms are believed to act as stabilizer of ZITO network. Chang *et al.* [46] observed an abnormal subthreshold leakage current at high temperature in In-Ga-Zn-O TFTs. This was due to trap-induced thermal generated defects accumulating at the source region, leading to barrier lowering on the source side and apparent subthreshold leakage current. To obtain superior thermal stability, N_2O plasma treatment on the channel layer was conducted to reduce defect generation during subsequent fabrication

process. Reducing defect generation suppressed subthreshold leakage current and improved thermal stability in IGZO TFTs.

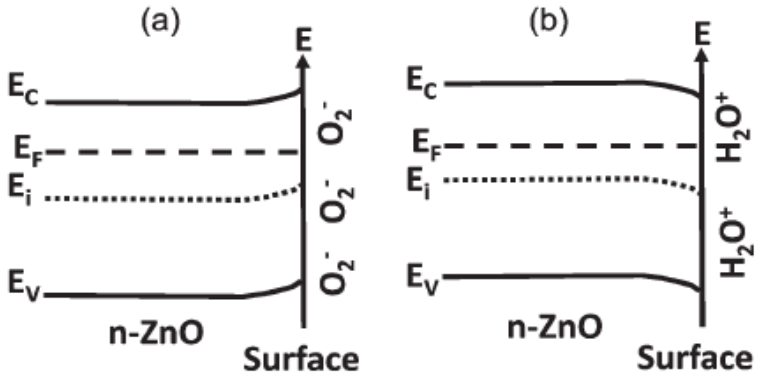

Figure 2.6 Schematic drawing showing the impact of (a) O^{2-} and (b) H_2O^+ adsorption on surface band bending at ZnO TFTs. (Ref. [43] © 2010 IEEE)

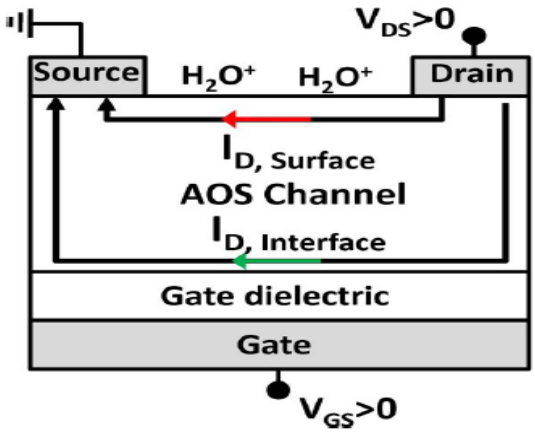

Figure 2.7 Cross sectional schematic of an unpassivated bottom gate TFT device illustrating the formation of a parasitic top gate channel due to surface adsorption. (Ref. [43] © 2010 IEEE)

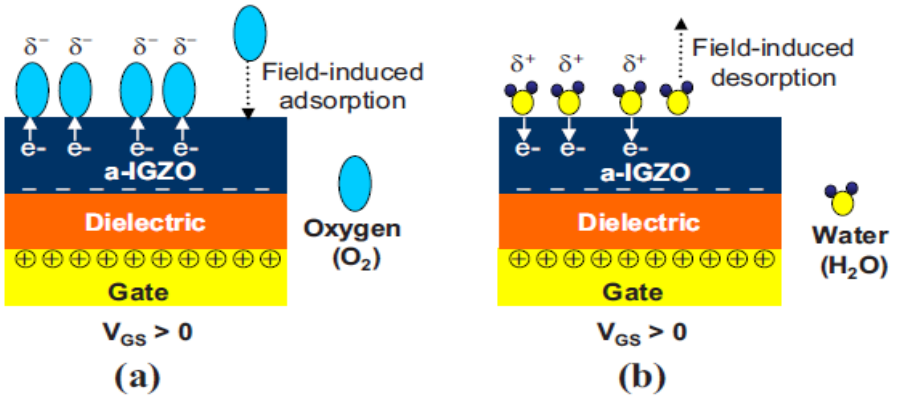

Figure 2.8 (a) Schematic showing the electric-field-induced adsorption of oxygen molecules from the ambient atmosphere under the application of positive gate voltage stress. (b) Schematic showing the electric-field-induced desorption of water molecules into the ambient atmosphere under positive gate voltage stress (Ref. [39])

2.5. Summary and Challenges

In summary we have shown that ZnO and its compounds are highly suitable materials of TFT devices for the next generation large area electronic systems. ZnO based TFTs feature several advantages including high mobility, transparency in visible light region, superior radiation hardness and available growth techniques on various substrates. These advantages could lead to future display systems with light weight, ultra-high resolution and 3D imaging. There are still some crucial problems remaining to be resolved before ZnO based TFTs can be integrated into commercial electronics. Electrical characteristics of ZnO based TFTs are highly affected by the presence of intrinsic defects in the ZnO channel layers. Directly exposure to ambient gas (oxygen, water and hydrogen) could change the distribution of defects in active channel layers due to interaction between channel surface and ambient molecules. Bias stress and temperature stress could also introduce instability in ZnO based TFTs owing to generation of defect states and/or charge trapping at active channel/dielectric interface. The main focus in the dissertation work is to study and improve electrical characteristics and stability issues in ZnO based TFTs which could provide insightful understanding to design and implement ZnO based TFTs technology for the future large area electronics.

Chapter 3

Design and Fabrication of ZnO TFTs

As mentioned in Chapter 2, the electrical characteristics of ZnO TFTs depend on the quality of channel layers of TFT device. For ZnO-based TFTs, n-type carrier concentration is highly affected by the presence of intrinsic defect density. In MOCVD growth technique, the incorporation of hydrogen is inevitable, since all the metal-organic precursors have the hydrogen element. Hydrogen is a shallow donor in ZnO films and it can be trapped at oxygen vacancy site, which is a very common intrinsic donor defect in ZnO. Therefore, background n-type carrier concentration in ZnO films grown by MOCVD (~10^{18} cm^{-3}) is usually two orders higher than that of sputtered ZnO films (~10^{16} cm^{-3}). The high n-type carrier concentration hinders the realization of enhancement mode TFT devices, since the channel is conducting current at zero gate bias and a negative gate bias is needed to turn-off the current. As modern circuits and systems require low power consumption, the active TFT devices operated in enhancement mode are highly desirable.

To overcome this intrinsic issue in MOCVD technique and achieve ZnO TFTs operated in the enhancement mode, we firstly developed a series of growth recipes for ZnO channel layers to accomplish the optimized growth with (i) growth temperature, (ii) Zn/O flow ratio, and (iii) multi-step growth followed by in-situ oxygen annealing. Operation principles of n-type ZnO TFTs are discussed. Next we built a universal numerical model to extract the parameters of ZnO TFTs, including field effect mobility, threshold voltage, and subthreshold swing. Finally, we investigate the performance of ZnO TFTs with different channel layer thickness to determine optimized layer structure.

3.1. Material Characterizations of ZnO channel layer

In this section we present the material characterizations of ZnO films which we have developed for ZnO TFTs. During MOCVD growth, Diethylzinc (DEZn) and high purity O_2 gas are utilized as precursors for Zn and O source, respectively. We employed several tools to investigate the surface morphology and microstructure of ZnO films, including: (i) atomic force microscopy (AFM) and scanning electron microscopy (SEM) for morphological characterizations; (ii) X-ray diffraction (XRD) and transmission electron microscopy (TEM) for microstructural characterizations.

3.1.1. Morphology of ZnO TFT Channel Layer

For a typical n-type TFT device, the output drain current is attributed to electrons transport in the channel layer. A vertical electrical field introduced by a positive gate bias during the TFT operation accumulates high density of electrons in the channel layer, increasing the output drain current. It can be seen that the surface of ZnO channel layer is critical since a rough surface may introduce unwanted scattering events and reduce output drain current. To make the high quality TFT devices, a dense ZnO film with smooth surface is required. Furthermore, the films with columnar structures are also undesirable due to poor lateral field mobility. To prevent the columnar growth, the growth temperature is reduced to 350°C ~400°C. In this low temperature range, ZnO forms dense a polycrystalline film with smooth surface. The scanning electron microscopy (SEM) shows morphology of a ZnO film grown on SiO_2 (Fig. 3.1 (a)). No obvious columnar structure is observed from the SEM picture. Figure 3.1 (b) shows the surface morphology of a ZnO film grown on SiO_2/Si measured by an atomic force microscopy

(AFM). The average surface roughness is estimated to be 2.4 nm, confirming the smooth surface of ZnO films grown on SiO_2/Si.

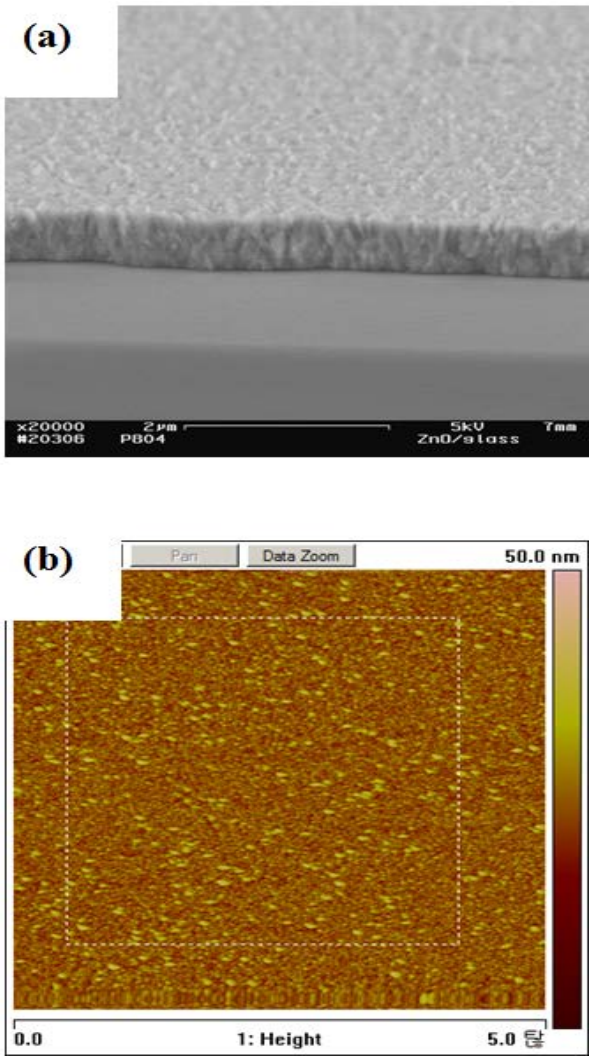

Figure 3.1 (a) SEM morphology of ZnO film grown on SiO_2 template at growth temperature of 350°C. (b) Surface morphology of ZnO film grown at 350°C on SiO_2/Si measured by AFM. The average surface roughness of ZnO film is 2.4nm**.**

3.1.2. Microstructure of ZnO Channel Layer

Microstructural characterizations of ZnO channel layers grown at 350°C are performed by X-ray diffraction (XRD) and transmission electron microscopy (TEM). Figure 3.2 shows the XRD results of a ZnO film grown at 350°C. It features a polycrystalline structure with the preferred orientation parallel to the [0001] c-axis. It is common for ZnO films to exhibit such a preferred orientation since ZnO crystal has a wurzite structure and film growth speed along c-axis is higher than other directions. Figure 3.3 represents the TEM results of a ZnO film. The ring pattern in TEM indicates the polycrystalline structure of the ZnO film, as shown in Figure 3.3 (a). From the dark field image in Figure 3.3 (b), various grains are observed with grain sizes ranging from 10 nm- 20 nm.

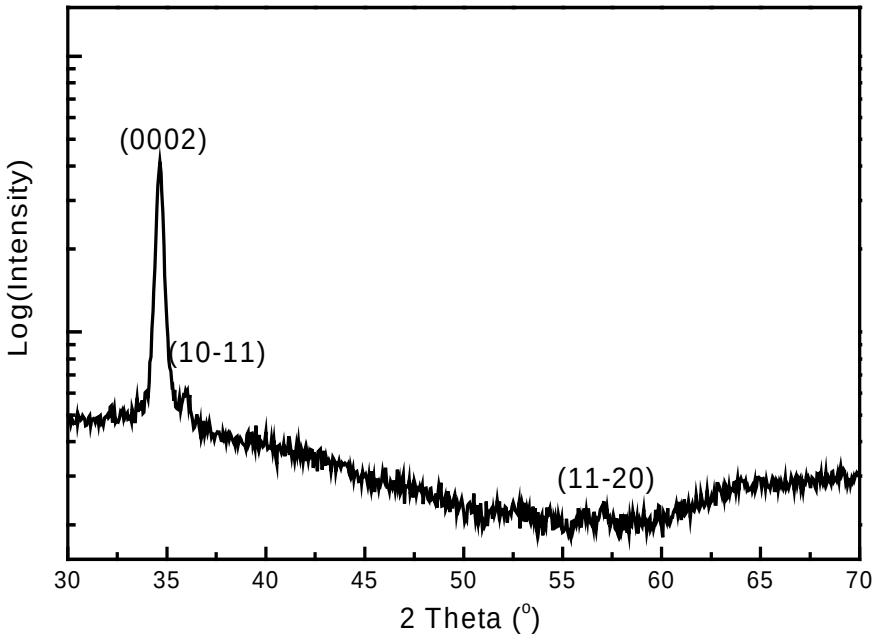

Figure 3.2. XRD results of ZnO thin film grown at 350°C. It shows a polycrystalline structure with [0001] c-axis preferred orientation.

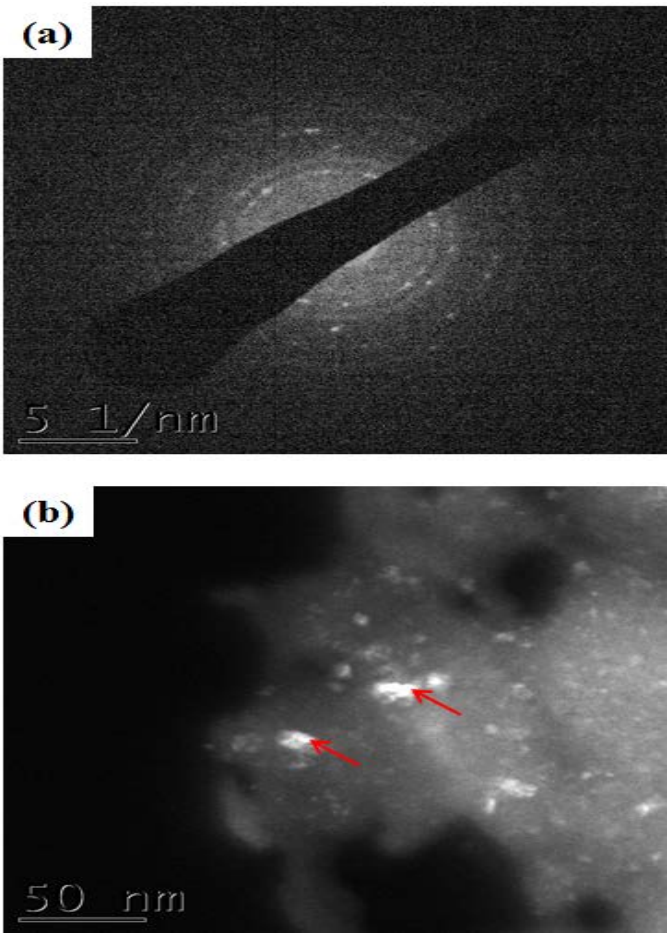

Figure 3.3 TEM results of 50 nm ZnO film grown at 350°C (a) diffraction pattern (b) dark field image.

3.2. Fabrication of ZnO TFT Devices

Throughout this research work, the inverted-staggered bottom gate TFT configuration is adopted. This configuration is the most popular structure in current industry and research work. In addition, the unpassivated top surface of the channel layer can be utilized as a sensing area for the active sensing application. Two different device layer designs are utilized: (i) a common gate structure where a heavily doped Si substrate is used as the gate and a thermally grown SiO_2 film is used as a dielectric layer, respectively; (ii) a patterned gate structure where a TFT is built on a glass substrate with a patterned metal gate and a PECVD deposited SiO_2 film as a dielectric layer, respectively. Figure 3.4 illustrates the two different device configurations.

3.2.1. Fabrication of common gate ZnO TFT devices

Figure 3.5 shows the fabrication process flow chart of common gate ZnO TFT built on Si substrate. A heavily doped n type Si substrate is used as the gate (common gate). After RCA clean, a 50-100 nm SiO_2 dielectric layer is grown by dry oxidation at 1100 °C. Subsequently, the different thickness of ZnO channel layers are grown by MOCVD at 350-450 °C. DEZn (diethyl zinc) and high purity oxygen gas are used as the source of Zn and oxygen. A post annealing process at 600 °C in oxygen ambient can be applied to further improve TFT performance. After channel layer deposition, a mesa process is performed by wet etching process in diluted hydrochloride acid. The source and drain metallizations are formed with 100 nm Ti/50 nm Au by a lift-off process. The active layer is fixed at a width/length (W/L) = 150μm/5μm. To prevent ambient absorption/desorption during the electrical testing, a SU-8 resist is coated on top of the

TFT channel, serving as a passivation layer. A via open process is applied by ICP/RIE dry etching process to enable electrical contact to the bottom Si substrate.

3.2.2. Fabrication of patterned gate ZnO TFT devices

Figure 3.6 shows the fabrication process flow chart of the patterned gate ZnO TFTs built on a glass substrate. A gate metal consisting of Cr 100nm/Au 50nm is first deposited by e-beam evaporation on a glass substrate and then defined by the lift-off process. A 50-100 nm SiO_2 dielectric layer is deposited by plasma enhanced chemical vapor deposition (PECVD) at ~ 400 °C. An annealing process at 450 °C in nitrogen ambient is applied after dielectric layer deposition to reduce trap density of dielectric layer. Subsequently, the different thickness of ZnO channel layers are grown by MOCVD at 350-450 °C. DEZn (diethyl zinc) and high purity oxygen gas are used as the source of Zn and oxygen. A post annealing process at 450 °C in oxygen ambient can be applied to further improve TFT performance. After channel layer deposition, a mesa process is performed by wet etching process in diluted hydrochloride acid. The source and drain metallizations are formed with 100 nm Ti/50 nm Au by a lift-off process. The active layer is fixed at a width/length (W/L) = 150μm/5μm. To prevent ambient absorption/desorption during the electrical testing, a SU-8 photoresist is coated on the top of the TFT channel, serving as a passivation layer. A via opening process is applied by the ICP/RIE dry etching process to make the electrical contacts to the bottom gate electrode. The thermal budget for the patterned gate TFT devices is lower than that of the common gate TFT devices to avoid the excessive diffusion of the Cr/Au metallization into the gate dielectric layer.

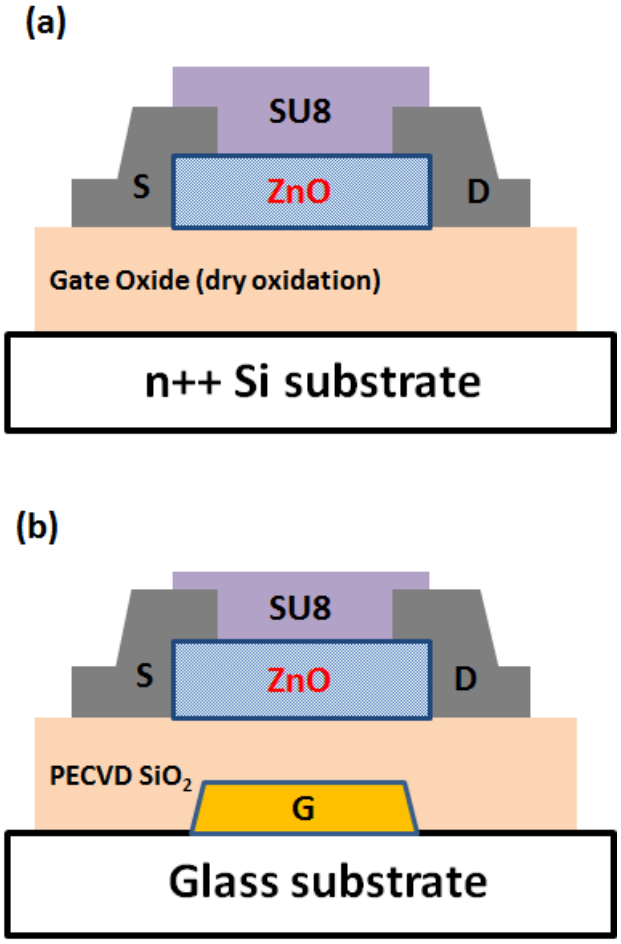

Figure 3.4 Inverted staggered bottom gate TFT structures: (a) a common gate TFT device built on a Si substrate, and (b) a patterned gate TFT device built on a glass substrate.

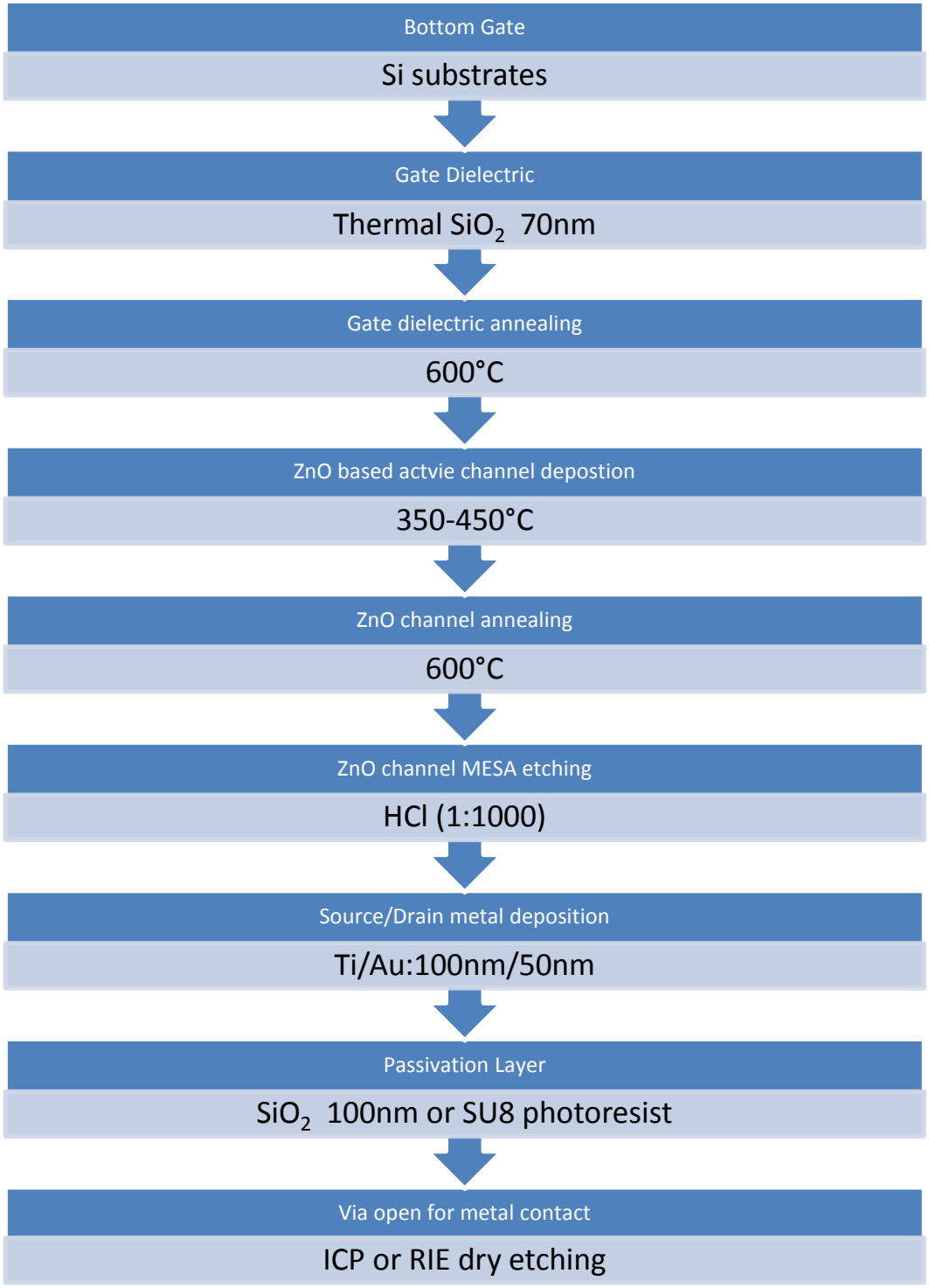

Figure 3.5 A flow chart of the fabrication process of a common gate TFT device built on a Si substrate.

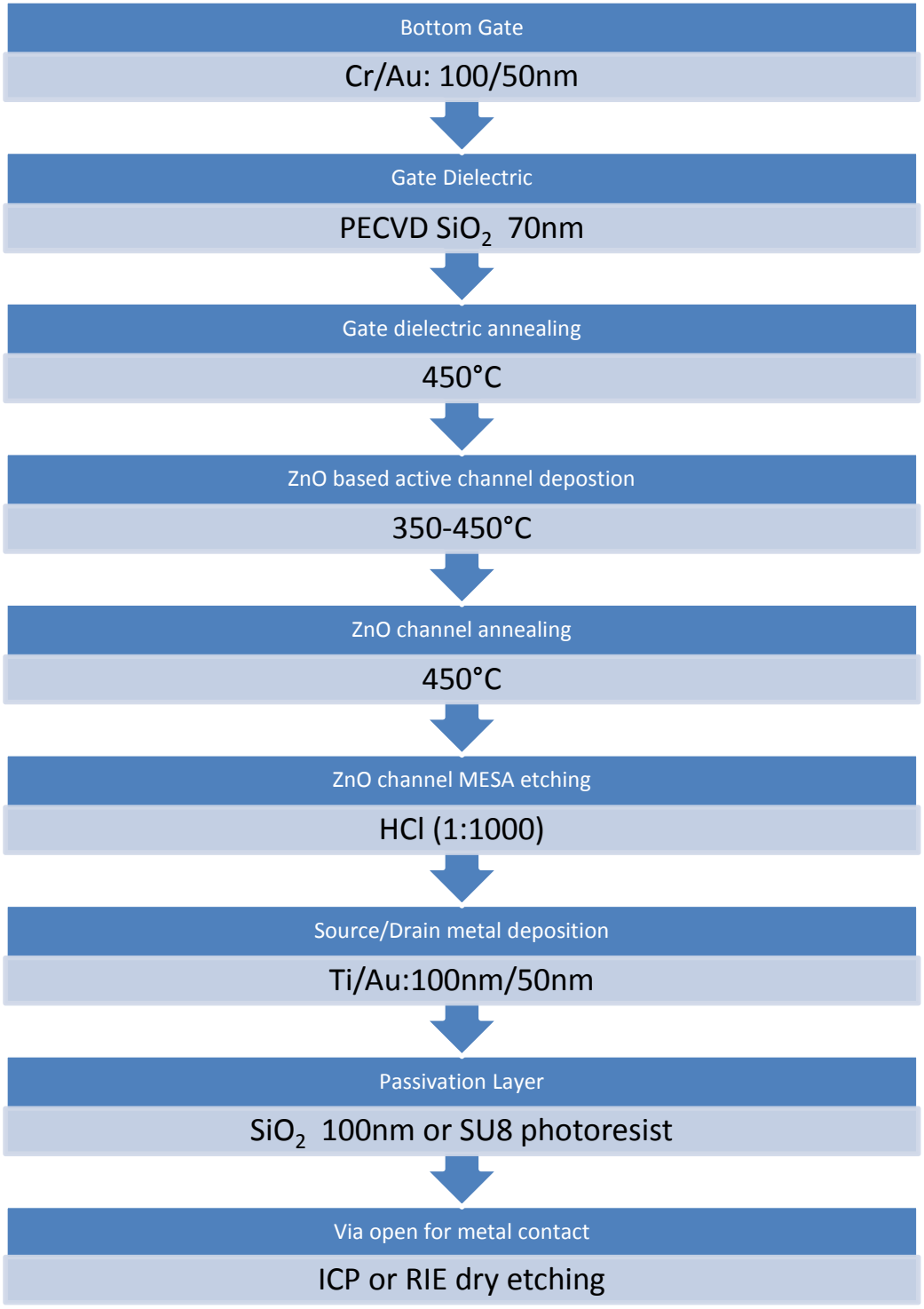

Figure 3.6 A flow chart of the fabrication process of a patterned gate TFT device built on a glass substrate.

3.3 Ideal Model of ZnO TFTs

A quantitative formulation of the ideal n-type TFT operation is giving according to the square-law theory [47], as summarized in Figure 3.8. With the sources is grounded, during the normal operation of a n-type ZnO TFT, a positive gate bias is applied to the drain to attract electrons from the source to the drain. The amount of drain current, I_{DS}, is determined by the presence of electron accumulation layer at the channel/dielectric interface. If gate-source voltage, V_{GS}, is less than the turn on voltage, V_{ON}, no electrons are present in the channel layer. In this situation, output drain current is zero and devices operation is in cut-off region, as shown in Figure 3.7 (a).

If V_{GS} greater than the V_{ON} is applied, while drain voltage is positive, drain current flows. As shown in Figure 3.7 (b), electrons are injected from source to gate-voltage induced electron accumulation layer channel and are transported across this low resistance channel layer, eventually are extracted at the drain contact. For small V_{DS} compared gate overdrive voltage, $V_{DS} << V_{GS}-V_{ON}$, drain current is described by Ohmic's law, i.e, $I_{DS} = V_{DS} / R_{CH}(V_{GS})$, where $R_{CH}(V_{GS})$ is the channel resistance depending on the gate-source voltage. In this linear region, the channel resistance is simply determined by sheet charge density of the accumulation layer.

As the magnitude of positive V_{DS} increases, so that V_{DS} is no longer negligible compared to $V_{GS}-V_{ON}$, I_D deviates from Ohmic's law. Instead, it becomes sublinear and eventually reaches the saturation region when pinch-off occurs at $V_{DS} = V_{GS}-V_{ON} = V_{D,SAT}$. It is assumed that the electron accumulation induced sheet charge density is given by equation 3.1

$$Q_n(y) = C_G[V(y) - V_{ON}] \tag{3.1}$$

where V(y) is the voltage drop at channel-dielectric interface from source to drain, with y = 0 and y = L corresponding the distance along the channel from the source to the drain, respectively. Equation 3.2 represents the charge density at the drain edge.

$$Q_n(L) = C_G[V_{GS} - V_{DS} - V_{ON}] \tag{3.2}$$

When $V_{DS} = V_{GS} - V_{ON}$ occurs, the accumulation layer electron density becomes zero at y = L, and the channel is depleted or pinched-off at the drain edge. The non-linear pre pinch-off to the post pinch-off, i.e. saturation is illustrated in Figure 3.7 (c).

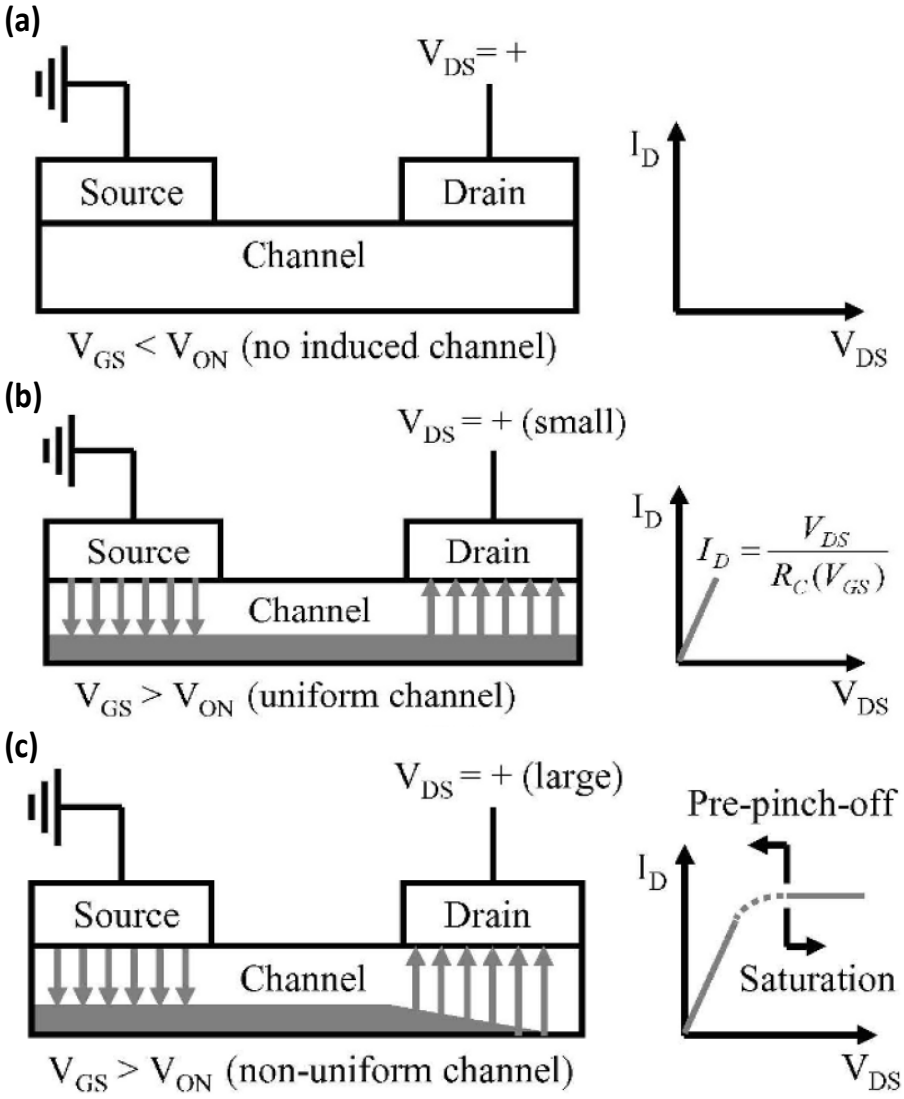

Figure 3.7 Ideal n-channel ZnO TFT operation (a) cut-off region (b) linear region, pre pinched-off and (c) saturation region, post pinched-off. (Ref [44])

Square Law Equation
Cut-off: $V_{GS} < V_{TH}$ $I_D = 0$ Linear Region (pre-saturation): $V_{GS} \geq V_{TH}$, $V_{DS} \leq V_{DSAT}$ $I_D = \frac{W}{L}\mu_{FE}C_{OX}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$ Saturation Region: $V_{GS} \geq V_{TH}$, $V_{DS} > V_{DSAT}$ $I_D = I_{SAT} = \frac{W}{2L}\mu_{FE}C_{OX}(V_{GS} - V_{TH})^2$
I_D, Drain Current (A) $V_{DSAT} = V_{GS}$-V_{TH}, Drain to Source voltage defining onset of Saturation V_{DS}, Drain to Source Voltage (V) V_{GS}, Gate to Source Voltage (V) V_{TH}, Threshold Voltage (V) W, Gate Width (μm) L, Gate Length (μm) μ_{FE}, Field Effect Mobility (cm^2-$V^{-1}S^{-1}$) C_{OX}, gate dielectric capacitance density (F-cm^{-2})

Figure 3.8 A summary of ideal, square law theory n-type ZnO TFT equations.

3.4. Universal Compact Model for ZnO TFTs

It is important to extract TFT parameters such as field effect mobility and threshold voltage to analyze and then optimize the device performance. The ideal formulation of TFT devices based on square law theory is exactly same as MOSFET devices. In MOSFET devices, field effect mobility and threshold voltage can be extracted by fitting the I_{ds}-V_{gs} curve in linear region, as shown in Figure 3.8 (a). The threshold voltage is extracted by the interception at x-axis (gate voltage) and field effect mobility is determined by the slope of the linear fitting curve. A lot of research works in ZnO based TFTs use the same method to extract field effect mobility and threshold voltage. However, by using this fitting method, the extracted threshold voltages could vary in a large range when the different portions of I_{ds}-V_{gs} curves in ZnO based TFTs are selected, as shown in Figure 3.8 (b). This phenomenon has been observed in all the TFT works including TFTs using different materials such as Si, ZnO, and organic semiconductors. The reason for such discrepancy is the non-ideality of channel layers in TFT devices. In MOSFET devices, output current is attributed to the transport of minority carriers in the inversion layer of single crystalline silicon substrates without defects. In contrast to MOSFET, in TFT devices, output current is attributed to the transport of majority carriers in channel layers which are either in polycrystalline or amorphous states. Such polycrystalline and amorphous channel layers contain a high density of defects, which could introduce various charge trapping mechanisms. Therefore, for TFT devices, the extracted parameters deviate largely from the ideal case, depending on the specific fitting regions of I_{ds}-V_{gs} curve.

To consistently extract TFT device parameters, we adopted the “universal compact model” proposed by B. Iniguez *et al* [48]. This model uses the integral operator method to extract the threshold voltage. The model captures the specific behavior observed for all types of TFTs regarding the field effect mobility, which is a power function of the gate voltage overdrive, as shown in equations (3.3) to (3.5). This power behavior is controlled by a parameter γ, which is an indication of crystallinity of the channel material. In a single crystalline device, γ = 0 and the model would correspond to a single crystalline MOSFET. As the degree of crystallinity decreases, parameter γ increases. The model is based on approximating the linear and saturation regions by two straight lines. Figure 3.9 depicts the fitting result of a ZnO TFT based on the universal compact model. It can be seen that the fitting results match well with ZnO TFT results at both linear and saturation regions.

$$I_{SAT} = \frac{\beta V_{gt}^2}{1+\beta R_s V_{gt}+\sqrt{1+2\beta R_s+V_{gt}+(\frac{V_{gt}}{V_L})^2}} \tag{3.3}$$

$$\beta = \frac{W}{L}\, C_{ox}\mu_{FET} = \beta_0(^{V_{gt}}/_{V_{aa}})^{\gamma} \;\; ; \;\; \beta_0 = (^{W}/_{L})C_{ox}\mu_0 \tag{3.4}$$

$$V_L = v_s L/\mu_{FET} \tag{3.5}$$

where I_{SAT} the saturation curremt, V_{gt} the gate overdrive voltage ($V_{gt} = V_{gs} - V_T$), v_s the saturation velocity, C_{ox} the oxide capacitance.

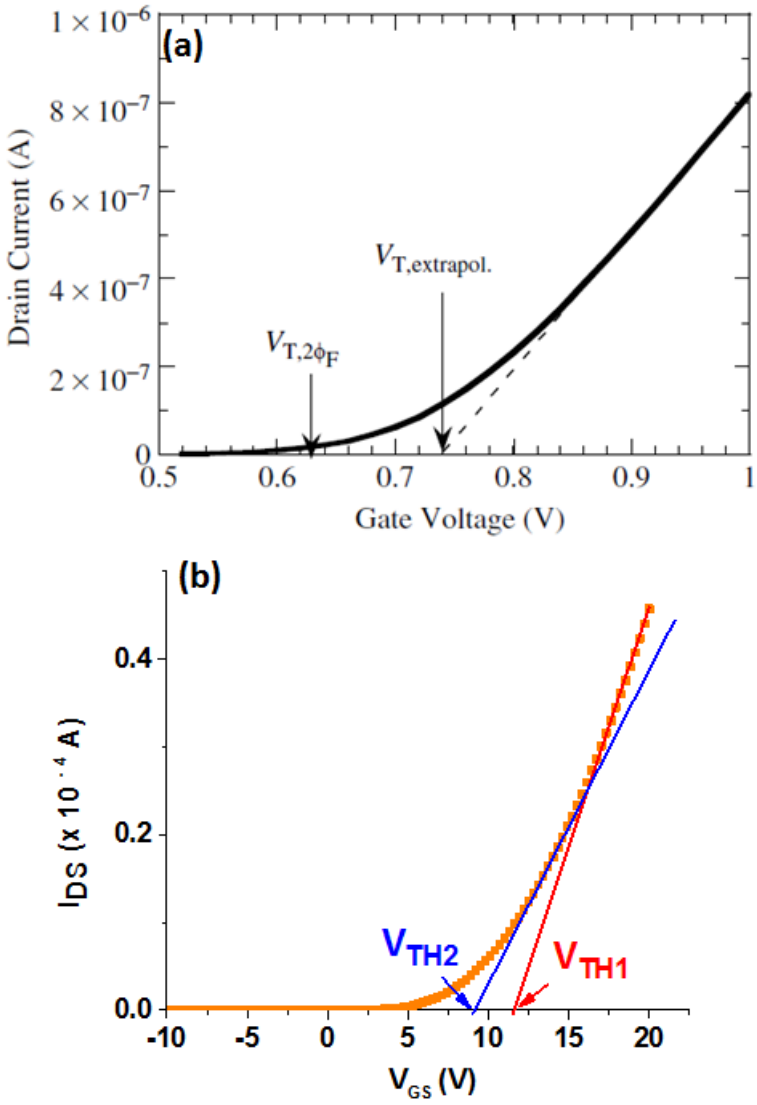

Figure 3.9 Extraction of threshold voltages in linear region for (a) a single crystalline MOSFET device (b) a ZnO polycrystalline TFT device.

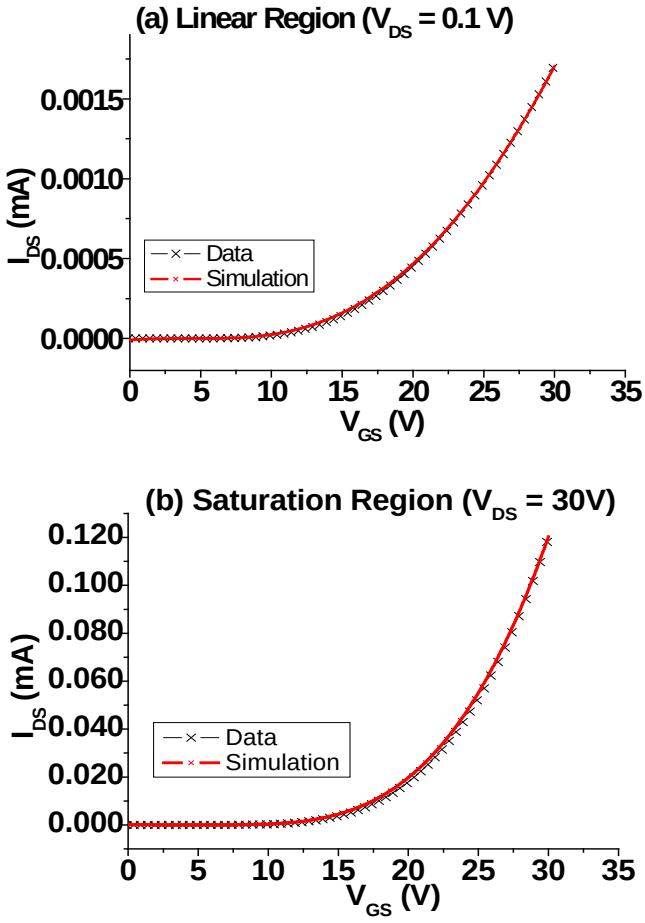

Figure 3.10 Fitting results of the ZnO TFT device at (a) linear and (b) saturation region based on universal compact model.

3.5. Optimization of channel thickness for ZnO TFTs

The effects of ZnO channel thickness on the TFT device performance are also studied. The gate dielectric layer is fixed to be 50nm. For comparison, bottom gate ZnO TFTs were fabricated with three different channel thickness of 70nm, 55nm, and 40nm, respectively. Post-deposition annealing in oxygen ambient is applied to all of ZnO TFTs; details of post-deposition annealing of ZnO TFTs will be presented and discussed in chapter 4. Figure 3.10 shows the transfer characteristic curves of ZnO TFTs with different channel thickness. All devices exhibit the enhancement mode operation, a large current ON/OFF ratio (>10^8) and low leakage current (<10^{-12}A). The extracted threshold voltages of 70 nm, 55 nm and 40 nm channel ZnO TFTs are 2.73 V, 2.36V, and 2.08V, respectively. The substhreshold swing of 70 nm, 55 nm and 40 nm channel of ZnO TFTs are 1.46 V/dec, 1.01 V/dec, and 0.86 V/dec, respectively. The extracted threshold voltage and subthreshold swing of TFTs as a functional of channel thickness are shown in Figure 3.11. The threshold voltage of TFTs [46] can be described by Eq.3.6 [49]:

$$V_T = qN_T t_S (E_F - E_i)_{threshold} / C_i \tag{3.6}$$

where N_T is the bulk trap density, t_s is the channel layer thickness, C_i is the capacitance of gate insulator. By assuming a constant trap density, it is desirable to have a “thin” channel in order to achieve a low threshold voltage. From the slope of Figure 3.11(b), the bulk trap density is estimated ~1.48×10^{18} cm^{-3}/eV, which is comparable to the reported value (1.0×10^{18} cm^{-3}/eV) in amorphous silicon TFT. Our results show that a thinner ZnO channel layer improves the TFT characteristics by decreasing the threshold voltage and the subthreshold swing. The comparison of field effect mobility in ZnO TFTs with different channel thickness is shown in Figure. 3.12. The 55nm and 70nm channel TFTs

have the similar field effect mobility value. However, the 40 nm channel TFT shows the lowest field effect mobility among all the devices. The degradation of field effect mobility for the thinnest channel TFT may result from an increased surface and interface scattering during electron transport along the channel. By comprehensively evaluating the device parameters of threshold voltage, subthreshold swing, and field effect mobility, we choose 55nm as the optimized channel thickness for ZnO TFTs.

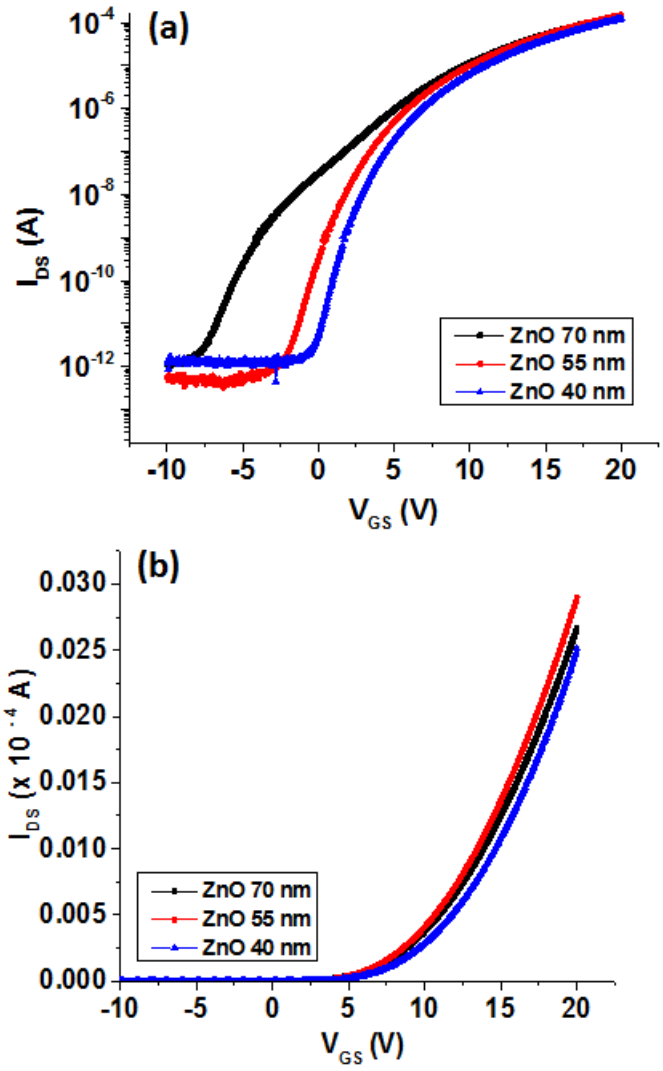

Figure 3.11 Transfer characteristics of bottom gate ZnO TFTs, for gate voltage sweep from +20V to -10V (a) drain voltage is +10V, in log scale and (b) drain voltage is +0.1V, in linear scale.

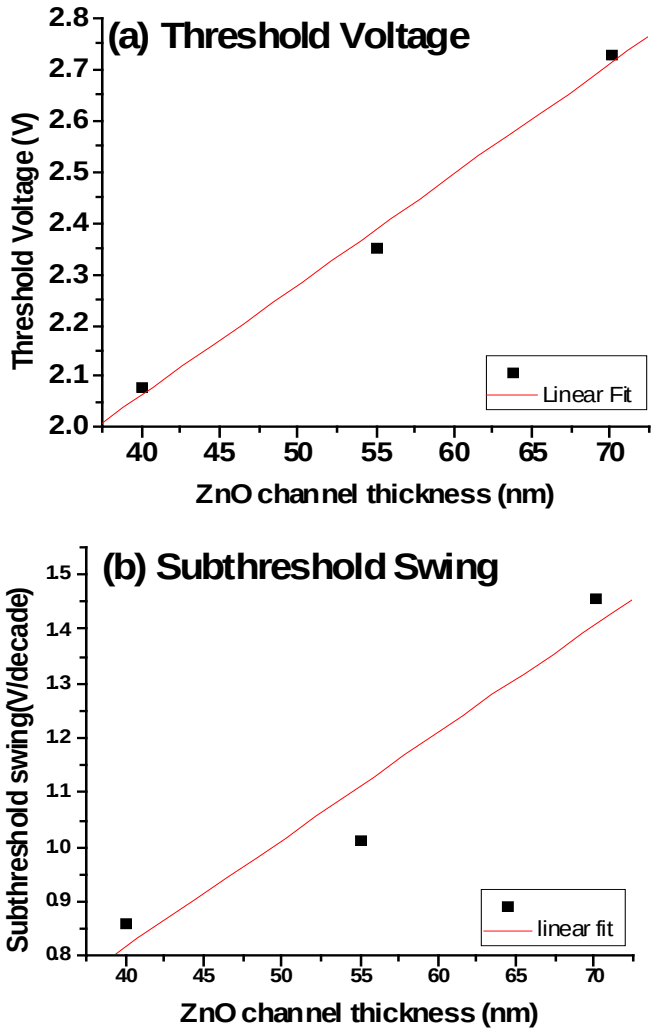

Figure 3.12 Plots of fitting results of (a) threshold voltage and (b) subthreshold swing as a function of channel thickness for ZnO TFTs on SiO_2/Si.

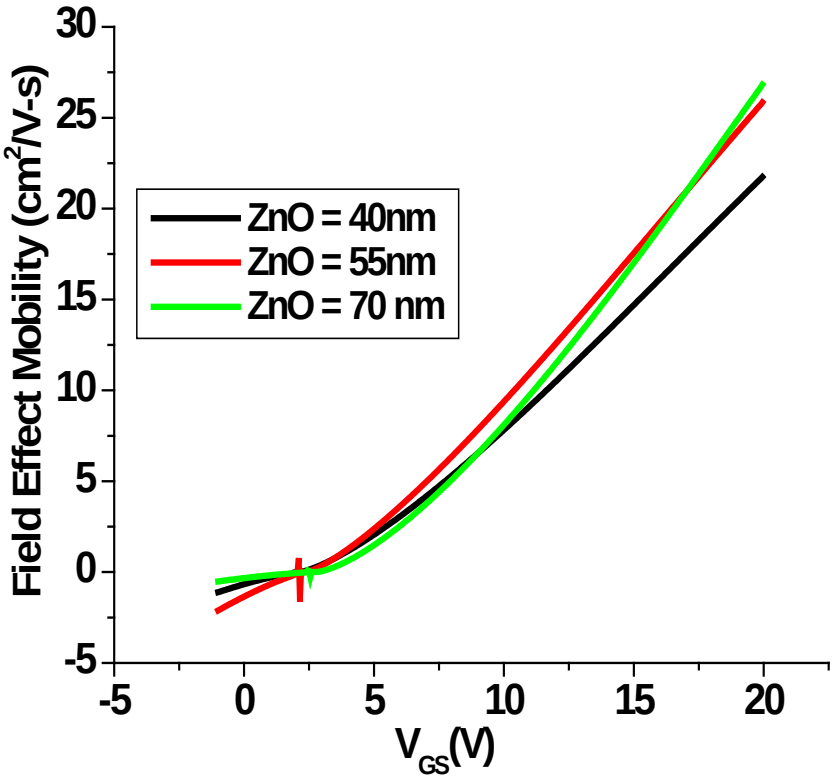

Figure 3.13 Comparison of field effect mobility for ZnO TFTs with different channel thickness of 40nm, 55nm and 70nm.

3.6. Summary

We have grown the ZnO channel layers by MOCVD. Various material characterizations including SEM, XRD, AFM, and TEM are employed to ensure the high quality ZnO films as channel layers for TFT devices. ZnO TFTs operating in enhancement mode has been demonstrated with high on-off ratio, high field effect mobility. A universal compact model is adopted to extract parameters of ZnO TFTs to replace the ideal square law model which has large deviation in fitting the real devices. Three different thickness of ZnO films have been applied as the TFT channel layer to optimize device performance. A ZnO TFT with 55 nm channel layer exhibits the enhancement mode operation with high field effect mobility. All the ZnO based TFTs in this thesis work will benchmark the channel thickness of 55 nm.

Chapter 4

Oxygen Annealing Effect on Improvement of Negative Bias Stress Stability in ZnO TFTs

In the previous chapter, we established the fabrication process and optimization of channel thickness for ZnO TFTs. Starting this chapter we will discuss improvements of ZnO TFTs through post oxygen annealing. As mentioned in Chapter 2 instability issues in ZnO TFTs are still a major research topic that needs to be addressed in order to realize commercial products of ZnO TFTs. Many reports have indicated that intrinsic defects play major roles in determining optical and electrical characteristics of ZnO films. Oxygen vacancy has been widely accepted as the origin of instability of ZnO TFTs. Ionization of neutral oxygen vacancies ($V_O \rightarrow V_O^{2+} + 2e^-$) in ZnO releases free electrons, hence, increasing the density of n-type carriers. This also introduces shifts of I-V characteristics and changes the operation voltages of ZnO TFTs. It is important to develop a process which can reduce the amount of oxygen vacancy present in the ZnO channel layer to improve performance and stability of ZnO TFTs. Annealing in oxygen ambient has been adopted as an effective method by many research groups to reduce oxygen vacancy related defects and improve optical and electrical properties of ZnO films. In this chapter, we investigate effects of oxygen annealing after channel growth and how it impacts the ZnO TFT stability against negative bias stress (NBS).

4.1. Introduction

Thin film transistors using transparent oxide semiconductor such as ZnO are expected to be the future driving devices in high resolution active matrix organic light emitting diode displays (AMOLEDs) and high frame rate/large size active matrix liquid crystal displays (AMLCDs) because they have superior advantages including a high mobility (10 cm^2/V-s), a small subthreshold swing and a low off- current (<10^{-13} A). For practical applications, the reliability and stability are the most important issues. Any instability will introduce shifts of threshold voltages (V_{TH}), affecting the operations of TFT devices.

Previous studies on ZnO films have shown that post-deposition oxygen annealing is an effective way to improve both optical and electrical properties. From photoluminescence (PL) studies, it is found that green band emission or deep level emission (DLE) is reduced and near band edge emission (NBE) is enhanced after post-deposition annealing in oxygen ambient [50]. This is an indication of lower defect density and better crystallinity after post-deposition oxygen annealing. In addition, n type carrier concentration measured from Hall measurement decreases after postdeposition oxygen annealing, making ZnO TFTs easier to reach operation in enhancement mode [51].

In this chapter, oxygen annealing is applied right after growth of ZnO channel layer. Post-deposition oxygen annealing is conducted at 600℃ for 1 hour in a furnace tube. X-ray photoelectron spectroscopy (XPS) is utilized as a characterization method to obtain qualitative results of oxygen related defects including oxygen vacancy for as-deposited and O_2-annealed ZnO channel layers. Electrical characteristics including I-V measurement and negative bias stress (NBS) testing are studied.

4.2. Experimental Procedure and Testing

Bottom gate ZnO TFTs were fabricated on heavily-doped n-type Si wafers with a 40 nm thermally grown SiO_2 as a gate dielectric layer. The 50 nm – ZnO channel layers were grown by MOCVD at 400°C. DEZn (diethyl zinc) and oxygen gas are the precursors for Zn and O, respectively. The O_2 annealing is applied at 600°C for 1 hour after channel deposition. The source and drain metallizations were formed with 100 nm Ti/50 nm Au by a lift-off process. The channel layer dimension is fixed at a width/length (W/L) ratio of 150μm/5μm. A SU-8 resist was coated on top of the TFT channel, serving as a passivation layer to prevent ambient absorption/desorption during the electrical testing. All the electrical/NBS stability tests are conducted in a light-tight probe station using a HP-4156C electrical testing system at room temperature. During NBS stability testing, a constant voltage of -20V is applied to the gate electrode to ensure a uniform electrical field (5MV/cm) distribution along the channel layer while source/drain contacts are shorted together (V_{DS}=0V). The NBS stability testing is conducted over duration of 7,200 sec. I-V characteristics of different devices are immediately recorded by the ICS software after accumulating NBS time reaches different duration (t_{NBS}=300 sec, 1,800 sec, 3,600 sec, and 7,200 sec). Each series of NBS stability testing is performed on the same TFT and thermal annealing (100°C) is applied prior to each new NBS stability testing to ensure consistent TFT initial properties.

4.3. Electrical Characterization

Figure 4.1 (a) and (b) show the atomic force microscopy (AFM) images with scan areas of 5x5 μm^2 for as-deposited and O_2-annealed ZnO channel layers, respectively. The values of root-mean-square (rms) roughness of as-deposited and O_2-annealed ZnO channel layers are 1.45 nm and 2.66 nm, respectively. Increase of surface roughness in O_2-annealed ZnO film is expected, since high temperature process is applied. Both channel layers exhibit similar feature, suggesting a reduced role of surface morphology on electron transport from the source to the drain. The I-V characteristics of as-deposited and O_2-annealed ZnO TFTs with V_{DS}=10V (saturation region) and V_{DS}=0.1V (linear region) are depicted in Figure 4.2 (a) and Figure 4.2 (b), respectively. The threshold voltage (V_{TH}) is defined as the gate voltage value when a drain current (I_{DS}) reaches 10^{-9} A. The field effect mobility (μ_{FE}) is extracted from the linear region. The subthreshold swing (S) is extracted from a 3-decades range in the subthreshold region of the $\log_{10}(I_{DS})$ *vs* V_G curve with V_{DS}=10V:

$$S = \left[\frac{\partial log_{10}(I_{DS})}{\partial V_G}\right] \quad (4.1)$$

The extracted threshold voltages for as-deposited and O_2-annealed ZnO TFTs are -1.65 V and +0.10 V, respectively. The O_2-annealed ZnO TFT exhibits higher μ_{FE} of 30 cm^2/V-s and smaller S of 0.40 V/dec while the as-deposited ZnO TFT shows μ_{FE} of 4 cm^2/V-s and S of 0.86 V/dec. It indicates that post-deposition oxygen annealing improves electrical characteristics of ZnO TFTs. Since all TFTs are built on the same gate and dielectric layers, it can be assumed that the differences of μ_{FE} and S values between the two different TFT channels mainly result from the different bulk trap densities measured

during electrical tests. The maximum bulk trap density (N_{BS}) in the channel can be extracted from the subthreshold swing S [52]:

$$S = log_e 10 * {}^{kT}/_{q} * [1 + q * t * N_{BS}/C_{OX}] \quad (4.2)$$

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, t is the thickness of the channel, and C_{ins} is the capacitance of the insulator. The extracted values of bulk trap density, N_{BS} for as-deposited and O_2-annealed ZnO TFTs are 1.44 x 10^{18} cm^{-3} and 6.38 x 10^{17} cm^{-3}, respectively. It implies that fewer defect states are present in the O_2-annealed ZnO channel layer.

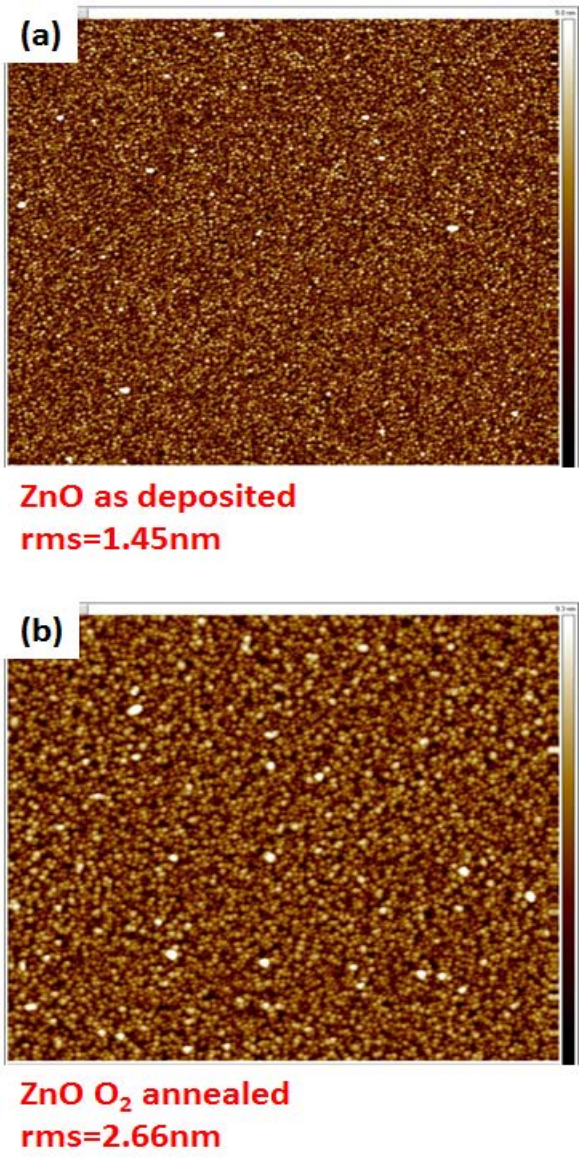

Figure 4.1 AFM images of (a) as-deposited and (b) O_2-annealed ZnO channel layers with scan area of 5x5 μm^2 and the maximum height is 10nm

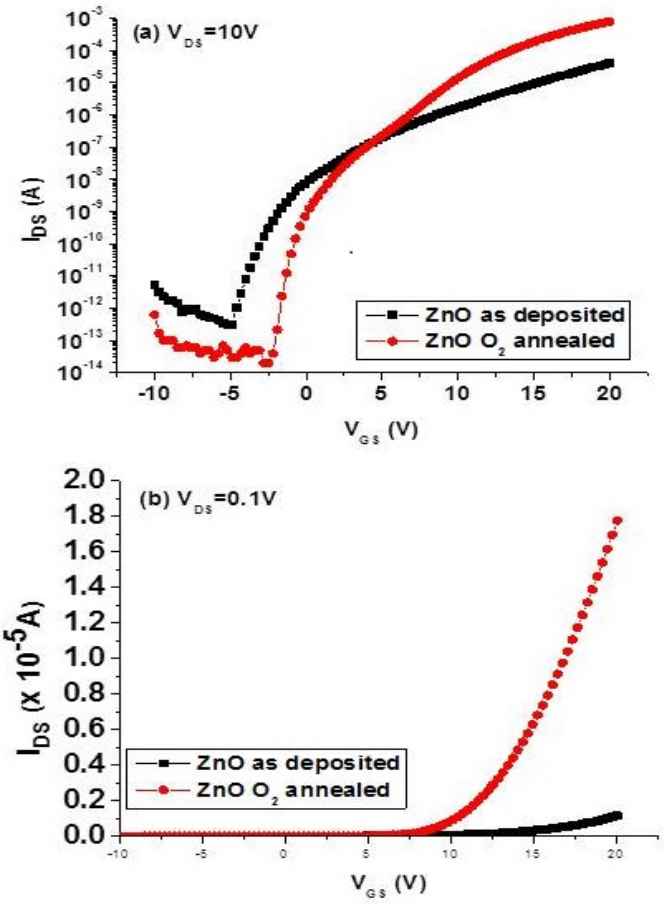

Figure. 4.2 I_{DS}-V_{GS} transfer characteristics of as-deposited and O_2-annealed TFTs (a) in the saturation region (V_{DS} =10V) (b) in the linear region (V_{DS} =0.1V).

4.4. X-ray Photoelectron Spectroscopy Studies of Oxygen Defects

Figures 4.3 (a) and 4.3 (b) show O_{1s} peaks in XPS spectra of O_2-annealed and as-deposited and ZnO thin films, respectively. Gaussian fitting is used in the deconvolution of these O_{1s} peaks. The peak at the lower binding energy ~530 eV (O_I) is attributed to O^{2-} ions present in a stoichiometric wurtzite ZnO structure, whereas the peak at the higher binding energy ~532eV (O_{II}) has been attributed to O^{2-} ions in "oxygen deficient" ZnO [53,54]. Such a double oxygen 1s peak is common for oxides containing cations in multiple valence states. The increase of binding energy of an O_{II} 1s electron relative to that of an O_I 1s electron can be explained by the raising of effective nuclear charge (Z_{eff}) of O_{II}^{2-} 1s electron. The presence of anion vacancy changes the distribution of negative charge density. An electron charge density in the region of V_o reduces, at nearest-neighbor O^{2-} ions, the screening of O^{2-} :1s electrons from their nucleus, thus increasing the effective nuclear charge Z_{eff} (i.e the binding energy) of an O_{II} 1s electron relative to that of an O_I 1s electron. The ratio of peak area (O_{II}/O_{tot}), indicating the relative quantity of this oxygen-related defect, is reduced from 30.7% (for as-deposited) to 23.2% (for O_2-annealed) after postdeposition oxygen annealing is applied. Also, the O_I/O_{II} peak positions shifted to lower binding energies from 530.32/532.08 eV to 530.08/531.8 eV due to a decrease in the number of oxygen vacancies.

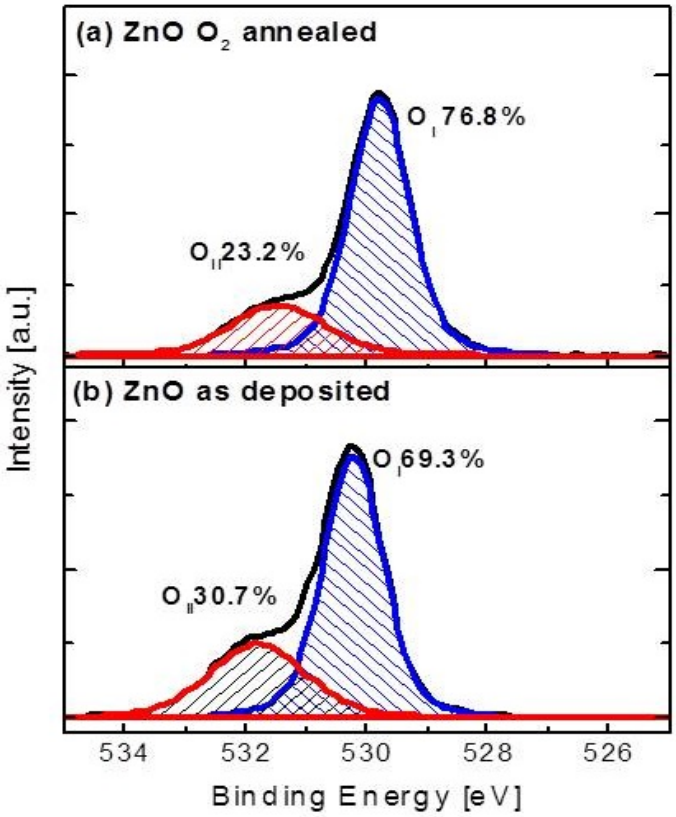

Figure 4.3 The O_{1s} peaks in the XPS spectra of (a) O_2-annealed ZnO and (b) as-deposited ZnO channel layers. The original O_{1s} peaks were deconvoluted by Gaussain fitting into two subpeaks including O_I (oxygen bonded with Zn) and O_{II} (oxygen vacancy related). The peak area of O_{II} /(O_I+O_{II}) is reduced after postdeposition oxygen annealing

4.5. Negative Bias Stress Stability

For application of TFTs as the driver/switch devices in a display system, stability against bias stress is the key pre-requisite. The brightness of each pixel is determined by the drain current of the driving TFT. TFTs must remain stable over time; any shift in threshold voltage would change the brightness of individual pixels, introducing non-uniformity of displays. In addition, switching TFTs in a display are n-type transistors. The device usually operates in the "OFF" state, which lasts more than 500 times longer than the "ON" state. In the "OFF" state, a negative gate voltage is applied to the n-type TFT in order to turn off the transistor and reduce the power consumption of a display. Therefore, it is critical to examine and then improve NBS stability of ZnO based TFTs in order to realized commercialized products.

Figure 4.4 (a) and 4.4 (b) illustrate transfer characteristics for as-deposited and O_2-annealed ZnO TFTs with V_{DS}=10V under NBS stability testing. Negative shifts of transfer characteristic curves are observed with different t_{NBS} for as-deposited and O_2-annealed ZnO TFTs. The TFT instability after NBS is specified as the change of threshold voltage (ΔV_{TH}). The NBS induced ΔV_{TH} after t_{NBS}=7,200 sec for as-deposited and O_2-annealed ZnO TFTs are -6.20 V and -2.00 V, respectively. It is found that for O_2-annealed ZnO TFT the S value changes from 0.40 V/dec to 0.46 V/dec while for as-deposited ZnO TFT the S value degrades from 0.86 V/dec to 0.95 V/dec, respectively. The negative shifts of transfer characteristics for ZnO based TFTs after NBS imply that the trapping of positive charges occurs at channel/dielectric interface. The trapped positive charges at channel/dielectric interface screen the gate electrical signal, leading to negative shifts of I_{DS}-V_{GS} curves. This also means that less gate voltage is required for a

TFT to accumulate the same amount of electrons in the channel layer without NBS. In our case, it is unlikely that holes are the origin of positive charges since concentration and mobility of holes are extremely low in the ZnO based TFT channels. The origin of trapped positive charges could be attributed to the ionization of the existing oxygen vacancies in the channel layer and their subsequent migration to the channel/dielectric interface under NBS. The negative shifts of transfer curves in conjunction with degradation of S values in both as-deposited and O_2-annealed ZnO suggest generation and/or re-distribution of defect states after NBS. It is observed that degradation of subthreshold swing becomes more significant as t_{NBS} increases for both as-deposited and O_2-annealed ZnO TFTs. In addition, degradation of subthreshold swing for the as-deposited ZnO TFT is much larger than that of the O_2-annealed ZnO TFT after NBS. It is possible that ionization and migration of oxygen vacancies during NBS could change the distribution of deep level states, affecting the subthrehold swing. The post-deposition oxygen annealing leads to a reduced amount of oxygen vacancies in the channel and a more uniform (less dispersive) distribution of deep level states. During NBS, slighter shift of threshold voltage and smaller degradation of subthreshold swing are obtained for the O_2-annealed ZnO TFT than that of the as-deposited ZnO TFT.

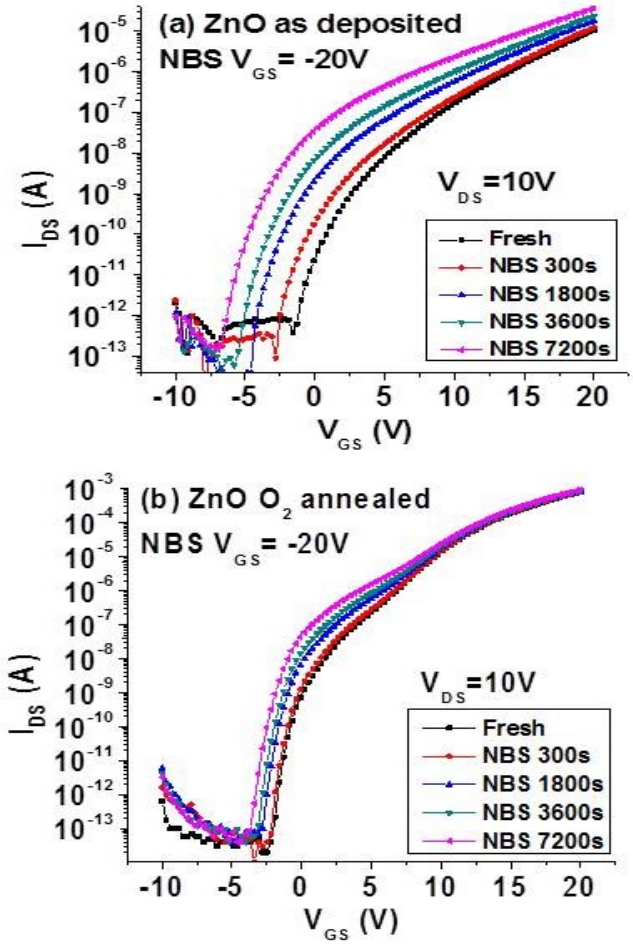

Figure 4.4 The evolution of transfer characteristics (I_{DS} vs. V_{GS}) for V_{DS} =10V during NBS testing of (a) as-deposited ZnO TFT and (b) O_2-annealed ZnO TFT

The shifts of threshold voltages (ΔV_{TH}) with respect to different bias stress times (t_{NBS}) are fitted into the stretched-exponential model [55], as illustrated in Figure 4.5. The stretched-exponential equation during bias stress is defined as

$$|\Delta V_{TH}(t)| = |\Delta V_0|\left\{1 - exp\left[-\left(\frac{t_{NBS}}{\tau}\right)^{\beta}\right]\right\} \quad (4.3)$$

where $\Delta V_{TH}(t)$ represents the threshold voltage shift induced by bias stress, ΔV_0 is effective voltage drop across the gate dielectric layer, β is the stretched exponential exponent, and τ is the characteristic trapping time for carriers. The obtained β values are similar to the two devices: β =0.51 for the as-deposited ZnO TFT and β =0.62 for the O_2-annealed ZnO TFT. The β value represents the distribution of time constants that characterize the trapping process, reflecting the width of involved trap distribution. The value of β ~ 1 indicates a narrow distribution; on the contrary, β < 1 depicts a broader distribution of time constants. The fact that the extracted β values are less than unity in both as-deposited and O_2-annealed ZnO TFTs implies a dispersive carrier transport. Furthermore, a larger β value in the O_2-annealed ZnO TFT suggests that its trap distribution is more uniform than that of as-deposited TFT. The extracted τ values for O_2-annealed and as-deposited ZnO TFTs are 2.58 x 10^5 sec and 6.53 x 10^4 sec, respectively. The larger τ in O_2-annealed ZnO TFT is the indication of less charge trapping during NBS.

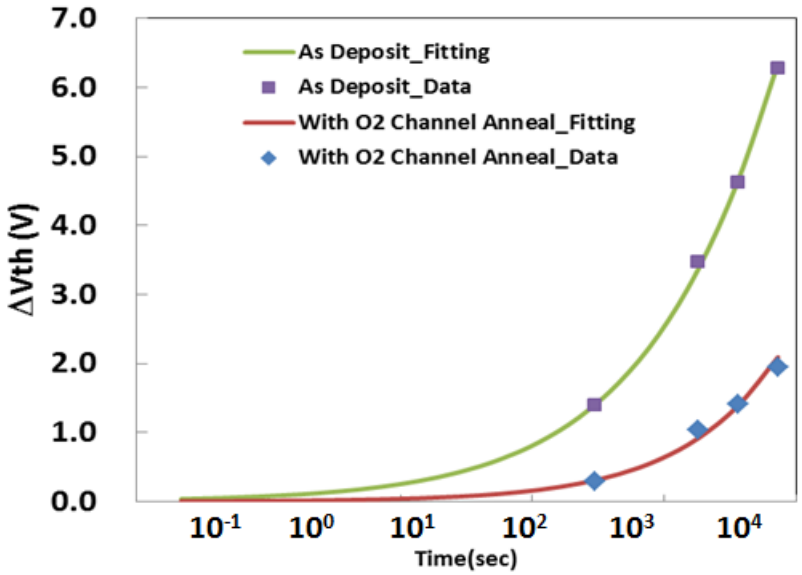

Figure 4.5 Graph of absolute value of ΔV_{TH} with respect to NBS stress time.

The obtained data were fitted into stretched exponential equation (solid lines).

4.6. Results and Discussions

Theoretical calculations show that the oxygen vacancy is a "*negative-U*" center, meaning that charge state transition is directly from +2 (V_o^{2+}) to the neutral (V_o) as the Fermi level moves toward CBM and V_o^{+} is never thermodynamically stable[10]. The transition level is located at ~ 1 eV below CBM and the oxygen vacancy is now widely accepted as a deep level donor rather than a shallow donor in ZnO. The oxygen vacancy assumes the +2 charge state when the Fermi level is near the valence band maximum (VBM) and has relatively low formation energies. The ionization of oxygen vacancy compensates the p-type doping in ZnO, making it very difficult to obtain p-channel operation for ZnO based TFTs. The instability induced by NBS in ZnO based TFTs could be the result of ionization of existing oxygen vacancies in the channel and their subsequent migration toward the dielectric/channel interface. For a fresh device, the Fermi level is near CBM and the oxygen vacancy is at the neutral charge state. During NBS, the depletion region is created in the ZnO channel layer, giving rise to the larger upward bending of energy band. Inside the depletion region, the quasi Fermi level is lowered to near midgap level and becomes closer to VBM, reducing formation energies of ionized oxygen vacancies. The ionization from V_o to V_o^{2+} introduces outward relaxation of neighboring Zn atoms. Due to a high electric field and a long duration under NBS, presence of V_o^{2+} could cause position changes of surrounding atoms, including ones that are distant from V_o^{2+}. In this case, the rearrangement of atomic structure induced by V_o^{2+} increases the energy barrier for returning its initial position [56], leading to the stabilization of V_o^{2+}. As duration of NBS prolongs, the migration of oxygen vacancies takes place. The migration of oxygen vacancies involves in that a nearest-

neighbor oxygen atom in the oxygen lattice jumps into the original vacant site leaving a vacancy behind. The calculated migration energy barrier for V_o^{2+} is 1.7 eV and for V_o is 2.4 eV, making V_o^{2+} more mobile under an electric field [57]. Under NBS, mobile V_o^{2+} can migrate to dielectric/channel interface and become trapped positive charge, which causes NBS instability later.

Before NBS, the amount of oxygen vacancies in the O_2-annealed ZnO TFT is less than that in the as-deposited ZnO TFT due to strengthened atomic bonding. During NBS, a substantial fraction of oxygen vacancies existing in the channel layer are ionized and then migrate toward the channel/gate dielectric interface. Thus, a reduced amount of ionized oxygen vacancies in the O_2-annealed ZnO TFT provides fewer free electrons to the channel and the TFT turn-off will require less negative gate bias. In consequence, a smaller negative shift of threshold voltage is observed and the improvement of NBS stability is obtained for the O_2-annealed ZnO TFT. The ionization and migration of oxygen vacancies in ZnO-based TFT channels could be related to the “loosely bound oxygen”, since it requires lower energy to move a loosely bound oxygen from its original site into a vacant site. The current work demonstrates that the overall improvement of NBS stability in O_2-annealed ZnO TFTs over as-deposited ZnO TFTs mainly arises from the reduction of loosely bound oxygen and oxygen vacancy related defects.

4.7. Summary

In conclusion, the improvement of NBS stability in O_2-annealed ZnO TFTs over pure ZnO TFTs has been demonstrated in terms of less negative shift of threshold voltage and minimized degradation of subthreshold swing. The origin of negative shifts of transfer curves in ZnO-based TFTs after NBS is associated with the ionization and migration of oxygen vacancies. The enhancement of NBS stability in O_2-annealed ZnO TFTs is mainly attributed to the strengthened atomic bonding after applying oxygen annealing to ZnO, leading to the suppression of oxygen vacancies.

Chapter 5

Improvement the Electrical Characteristics and Thermal Stability in $Mg_xZn_{1-x}O$ TFTs

Post-deposition oxygen annealing was demonstrated in previous chapter to effectively improve electrical characteristics and NSB stability of ZnO TFTs. From XPS results, it is found that peak area of O1s related to "loosely bound O^{2-} ions" or "O^{2-} ions in oxygen deficient ZnO " is reduced. It indicates a decreased amount of oxygen related defects such as oxygen vacancy after post-deposition oxygen annealing. However, post-deposition oxygen annealing introduces a high temperature processing (at 600°C), which is not suitable to the fabrication of TFTs on flexible substrates or paper. Thus, the capability of in-situ doping/alloying of MOCVD technique presents an appealing alternative. Unlike RF sputtering technique, where the film composition is highly dependent on targets, MOCVD growth technique provides a systematic method to study composition dependent properties of ZnO based TFT devices. From the experimental results discussed in previous chpater and other studies, it is critical to control the amount of oxygen vacancy related defects in channel layers. An alternative way to do so is to add an element (M) with stonger oxygen affinity than zinc. Once M-O bonds form during the growth, the oxygen vacancy can be suppressed in M-Zn-O channel layers. Mg is one of the promising candidates to serve as the oxygen binder in ZnO mainly, because Mg has similar ionic radii and Mg-O has higher bonding energy than that of Zn-O. In this chpater, we first develope the MOCVD growth technique for $Mg_xZn_{1-x}O$ ($0 \leq x \leq 0.06$) TFT technology. The Mg composition will be optimized according to electrical

characterisrtics of $Mg_xZn_{1-x}O$ (x=0, 0.06 and 0.1) channel layers. Improvements on electrical characterisitcs and thermal stability in MZO ($Mg_xZn_{1-x}O$,$0 \leq x \leq 0.06$) TFTs will be demonstrated and discussed.

5.1. Introduction

Recently, ZnO TFTs have attracted increasing attention due to their high electron mobility, transparency to visible light, and superior radiation hardness. ZnO TFTs are potentially much less expensive than ITO-based TFTs due to materials costs. It has been found that in ZnO based TFTs, the device characteristics, including field effect mobility, on-off ratio, subthreshold swing, and bias stress stability, are strongly impacted by the presence of native defects in the channel layer [58]. First principles calculation shows that the oxygen vacancy in ZnO has the lowest formation energy among the donor-like defects with deep electronic states [59]. Generally, an oxygen vacancy in the n-type ZnO is in the neutral state (V_o). However, under the negative gate voltage, the band bending can create the electron depletion region in the TFT channel. In this region, V_o can be excited to doubly ionized state (V_o^{2+}) and releases electrons into conduction band [60]. Thus, generation of V_o^{2+} from thermally excited V_o in the depletion region under a negative gate voltage increases the conductivity, resulting in the thermal instability of TFTs, including a negative shift of the threshold voltage and an increase of the drain current. In order to suppress oxygen vacancies in ZnO films, annealing in oxygen ambient at high temperature has been widely used [61]. However, the high temperature also leads to excessive interfacial diffusion between the channel and the gate dielectric, resulting in a degradation of the TFT.

It has been reported that the incorporation of Mg into HfO_2 effectively reduces oxygen vacancies [62]. Current understanding is that Mg becomes strongly bonded to oxygen vacancies (V_o^{2+}) in HfO_2, neutralizing this defect. We speculate that the incorporation of certain metal ions (M) that have a stronger oxygen affinity than Zn in ZnO may also suppress the oxygen vacancies since the formation energy of oxygen vacancies depends in part on the M-O/Zn-O bonding energy. Mg can be a good candidate to serve as the oxygen vacancy suppressor in ZnO TFTs. First, the Mg^{2+} substitution in the Zn^{2+} site does not cause significant lattice distortion due to their similar ionic radii (Mg^{2+}:0.57 Å *vs* Zn^{2+}:0.60Å). Second, owing to the strong ionic characteristic of MgO, the bonding energy of MgO (393.7 kJ/mole) is higher than ZnO (284.1 kJ/mol) at 298 K [63]. First principles calculations also indicate that MgO has a higher formation energy per oxygen vacancy (10.08eV) than ZnO (7.01eV) [64]. It has been reported that alloying of Mg into ZnO can reduce deep level luminescence associated with oxygen vacancies in both polycrystalline and epitaxial $Mg_xZn_{1-x}O$ films [65,66]. However, there has been little information on use of Mg alloying in ZnO to form $Mg_xZn_{1-x}O$ TFTs.

Ohtomo, *et al* [67] studied the photo-response of $Mg_xZn_{1-x}O$ TFTs (x=0, 0.1, and 0.3). The field effect mobility was found to decrease from 2.7 cm^2/V-s for ZnO to 0.8 cm^2/V-s for $Mg_{0.1}Zn_{0.9}O$ although no obvious structure change was found from XRD. The degradation of the field effect mobility was attributed to the alloying disorder and increased effective mass of electrons [68]. Recently, Kim, *et al* [69] investigated how Mg alloying affects the bias stress stability of high indium content (molar ratio In:Zn=9:1) sol-gel InZnO (IZO) TFTs. It was found that the energy band gap increased from 3.70 eV up to 3.99 eV with increasing Mg/(In+Zn) ratios up to 0.4. As more Mg was incorporated

into the InZnO matrix, it disrupted the crystal growth of IZO crystals and the grain size was decreased. The improvement of the bias stress stability was attributed to smoother surface morphology, a reduced size of voids both at the interface and in the film, and enlargement of the band gap.

In this chapter, we investigate the effects of Mg alloying on the electrical characteristics and thermal stability of $Mg_xZn_{1-x}O$ TFTs ($x \leq 0.1$). Mg^{2+} ions were incorporated to prevent oxygen out-diffusion and hinder the formation of oxygen vacancies in the TFT channel. The Mg composition is limited to no more than 10% to minimize deterioration of the field effect mobility.

5.2. Experimental Procedure and Testing

Bottom gate $Mg_xZn_{1-x}O$ TFTs were fabricated on heavily-doped n-type Si wafers with a 100nm thermally grown SiO_2. The 50nm - $Mg_xZn_{1-x}O$ (x=0, 0.06 and 0.10) channels are grown by MOCVD at 450°C. DEZn (diethyl zinc) and MCp_2Mg (bis(methylcyclopentadienyl) magnesium) are the precursors for Zn and Mg, respectively. The source and drain metallizations are formed with 100 nm Ti/50 nm Au by a lift-off process. The active layer is fixed at a width/length (W/L) = 150μm/5μm. To prevent ambient absorption/desorption during the electrical testing, a SU-8 resist is coated on top of the TFT channel, serving as a passivation layer [70]. All the electrical tests are conducted in the dark using an HP-4156C electrical testing system with a temperature controlled chuck.

5.3. Electrical Characterization

The Mg composition values x in the $Mg_xZn_{1-x}O$ are extracted from the absorption curves (α^2 vs $h\nu$), as shown in Figure 5.1. The extracted Mg compositions are x =0.06 and x =0.1, respectively. Figures 5.2 (a) and 5.2 (b) show the I_{DS}-V_{GS} characteristics in the linear and saturation regions for three TFTs with different Mg concentrations. The field effective mobilities of these three TFTs are extracted from the linear region. All of the TFTs show high on-off ratios (>10^9). The extracted threshold voltages (V_{th}) for ZnO, $Mg_{0.06}Zn_{0.94}O$, and $Mg_{0.1}Zn_{0.9}O$ TFTs are 2.1V, 3.5V, and 4.5V, respectively. For the ZnO TFT, a field effect mobility μ_{FE} of 30cm^2/V-s and a subthreshold swing S of 0.54V/dec are obtained. Severe degradation of mobility (μ_{FE}=8cm^2/V-s) and subthreshold swing (S=1.9V/dec) is observed for the $Mg_{0.1}Zn_{0.9}O$ TFT, resulted from alloying disorder and an increased effective mass of the electrons. Similar results were observed by Ohtomo, et al [67]. However, in contrast to the high Mg composition (10%) case, the $Mg_{0.06}Zn_{0.94}O$ TFT shows the highest field effect mobility (μ_{FE}=40cm^2/V-s) and lowest subthreshold swing (S=0.25V/dec). Figure 5.2 (c) shows the hard saturation behavior in the I_{DS}-V_{DS} curve. The maximum bulk trap density (N_{BS}) in the channel can be extracted from the subthreshold swing value, S [71] :

$$S = log_e 10 * {}^{kT}/_{q} * [1 + q * t * N_{BS}/C_{\text{ins}}] \quad (5.1)$$

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, t is the thickness of the channel, and C_{ins} is the capacitance of insulator. The extracted values of N_{BS} for ZnO and $Mg_{0.06}Zn_{0.94}O$ TFTs are 3.53x10^{17} cm^{-3} and 1.37x10^{17} cm^{-3}, respectively. Different density of oxygen vacancies in the channel layer would significantly affect the subthreshold swing value and bulk trap density of ZnO based TFTs [71]. The decrease in bulk trap density indicates that the electron traps associated

with oxygen vacancies in the ZnO channel are reduced after alloying of 6% Mg to form $Mg_{0.06}Zn_{0.94}O$.

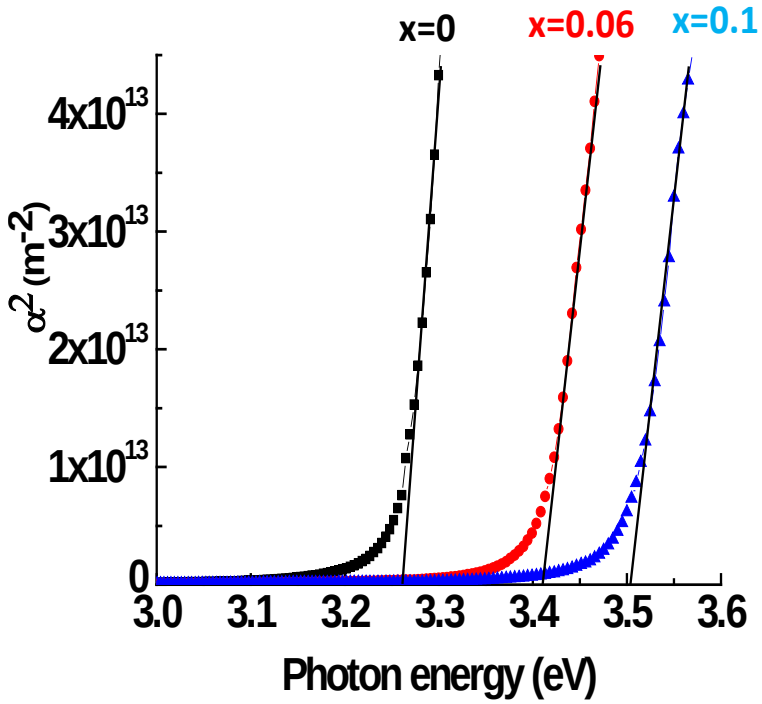

Figure 5.1 The α^2 vs *hv* curves of ZnO, $Mg_{0.06}Zn_{0.94}O$ and $Mg_{0.1}Zn_{0.9}O$ obtained from the transmission results.

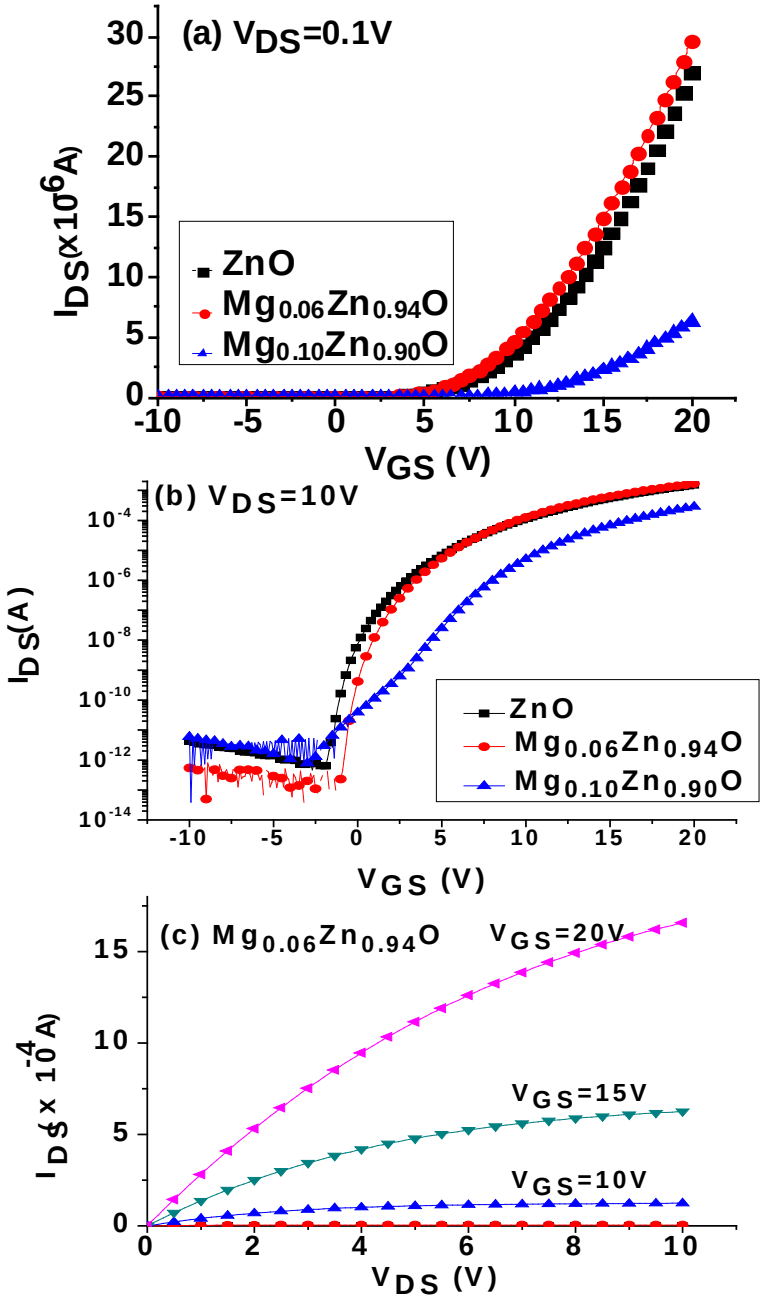

Figure 5.2. I_{DS}-V_{GS} transfer characteristics of ZnO, $Mg_{0.06}Zn_{0.94}O$ and $Mg_{0.1}Zn_{0.9}O$ TFTs: (a) in the linear region; (b) in the saturation region; and (c) the I_{DS}-V_{DS} characteristics of $Mg_{0.06}Zn_{0.94}O$ TFTs.

5.4. X-ray Photoelectron Spectroscopy Studies of Oxygen Defects

Figures 5.3 (a) and 5.3 (b) show O_{1s} peaks in XPS spectra of ZnO and $Mg_{0.06}Zn_{0.94}O$ thin films, respectively. Gaussian fitting is used in the deconvolution of these O_{1s} peaks. The peak at the lower binding energy ~530 eV (O_I) is attributed to O^{2-} ions present in a stoichiometric wurtzite ZnO structure, whereas the peak at the higher binding energy ~532eV (O_{II}) has been attributed to O^{2-} ions in "oxygen deficient" ZnO [72,73]. Such a double oxygen 1s peak is common for oxides containing cations in multiple valence states. The increase of binding energy of an O_{II} 1s electron relative to that of an O_I 1s electron can be explained by the raising of effective nuclear charge (Z_{eff}) of O_{II}^{2-} 1s electron. The presence of anion vacancy changes the distribution of negative charge density. An electron charge density in the region of V_o reduces, at nearest-neighbor O^{2-} ions, the screening of O^{2-} :1s electrons from their nucleus, thus increasing the effective nuclear charge Z_{eff} (i.e the binding energy) of an O_{II} 1s electron relative to that of an O_I 1s electron. The ratio of peak area (O_{II}/O_{tot}), indicating the relative quantity of this oxygen-related defect, is reduced from 19.3% (for ZnO) to 15.6% (for $Mg_{0.06}Zn_{0.94}O$) after 6% Mg is alloying into the ZnO thin film. Also, the O_I/O_{II} peak positions shifted to lower binding energies from 530.32/532.08 eV to 530.08/531.8 eV due to a decrease in the number of oxygen vacancies.

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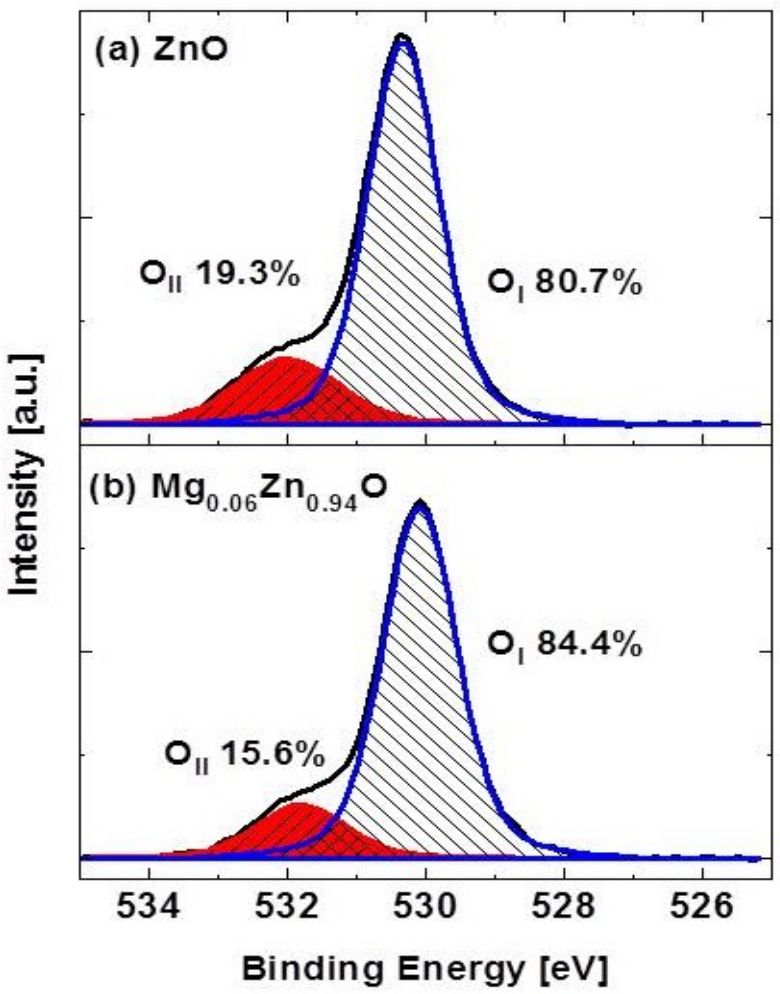

Figure 5.3 The O_{1s} peaks in the XPS spectra of (a) pure ZnO and (b) $Mg_{0.06}Zn_{0.94}O$ channel layers. The original O_{1s} peaks were deconvoluted by Gaussain fitting into two subpeaks including O_I (oxygen bonded with Zn) and O_{II} (oxygen vacancy related). The peak area of O_{II} /(O_I+O_{II}) is reduced after incorporation of 6% Mg into the ZnO.

5.5. Thermal Stability

Figures 5.4 (a) and (b) illustrate the evolution of the transfer characteristics of ZnO and $Mg_{0.06}Zn_{0.94}O$ TFTs at different temperatures, ranging from 300K to 375K. Both TFTs exhibit a negatively shifted threshold voltage V_{th} with increasing temperature: ΔV_{th} of ZnO TFT and $Mg_{0.06}Zn_{0.94}O$ TFT are 1.5 V and 0.5V, respectively. The subthreshold drain current of ZnO TFT increases from $2.2x10^{-10}$A to $8.6x10^{-8}$A with a V_{GS} of -2V. In contrast to the ZnO TFT, the subthreshold drain current of $Mg_{0.06}Zn_{0.94}O$ TFT only increases from $2.3x10^{-10}$A to $8.0x10^{-9}$A with a V_{GS} of 1.5V. Under a negative gate voltage, neutral oxygen vacancies (V_o) in the depletion region of ZnO channel can be thermally excited to ionized state (V_o^{2+}). Ionized oxygen vacancies would release electrons into the conduction band. The higher channel conductivity and lower V_{th} are induced by the formation of ionized oxygen vacancies. The simulation of the depletion width for deep traps at high concentration [74] shows that with a negative gate voltage of 5V, the entire channel of the ZnO TFT can be fully depleted under the assumption of trap density $N_T = 10^{16}$ to 10^{18} cm^{-3}.

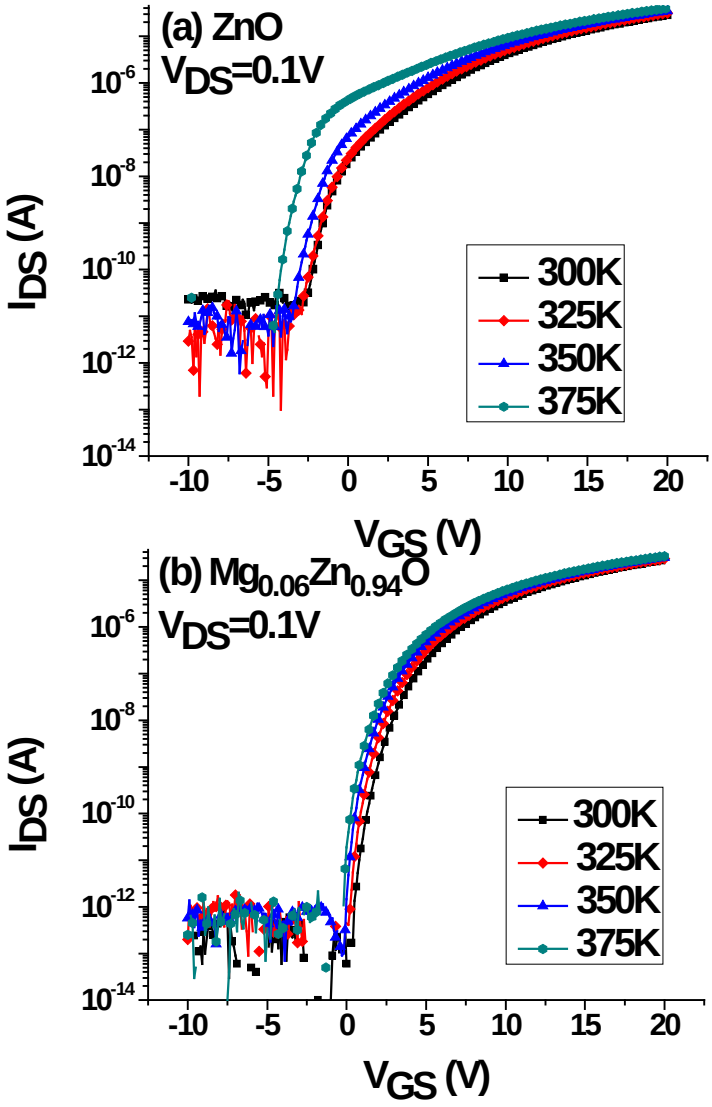

Figure 5.4 The evolution of transfer characteristics of (a) ZnO TFT, and (b) $Mg_{0.06}Zn_{0.94}O$ TFT at different temperatures, ranging from 300K to 375K.

5.6. Results and Discussions

The activation energy of the drain current extracted from an Arrhenius plot is used to approximately track the position of Fermi level ($E_A = E_C - E_F$) in the bandgap. Figure 5.5 shows the activation energy (E_A) of the drain current as a function of V_{GS}. The maximum activation energy of ZnO TFT is 0.85eV while for $Mg_{0.06}Zn_{0.94}O$ TFT it is 1.15 eV. The increase of activation energy of $Mg_{0.06}Zn_{0.94}O$ TFT cannot be explained only by the increase of the energy bandgap since the optical bandgap only increases by ~ 0.15eV. The higher energy barrier of $Mg_{0.06}Zn_{0.94}O$ TFT may result from the stronger bonding of Mg-O as compared to Zn-O, meaning that the formation of oxygen vacancies is suppressed and the density of oxygen vacancies is also reduced. A smaller variation in the threshold voltage value after annealing to higher temperature in 6% Mg doped ZnO TFT is observed ($\triangle V_{th} = 0.5V$) while for pure ZnO TFT $\triangle V_{th}$=1.5V. In addition, the activation energy (E_A) of the $Mg_{0.06}Zn_{0.94}O$ TFT decreases faster as a function of V_{GS}. The falling rate of E_A with respect to V_{GS} is correlated to the filling of traps in the active layer and the gate insulator/active layer interface [75]. For a TFT with a large trap density (N_{tot}), the decrease of E_A with V_{GS} is approximately inversely proportional to the N_{tot}. Because all TFTs are fabricated on the same thermally grown SiO_2/Si film, it can be presumed that most of the contribution of N_{tot} comes from bulk trap density (N_{BS}) of the channel. The faster decrease of E_A (0.9eV/V) with respect to V_{GS} in the $Mg_{0.06}Zn_{0.94}O$ TFT compared to ZnO TFT (0.3eV/V) suggests that the N_{tot} in $Mg_{0.06}Zn_{0.94}O$ TFT is diminished by roughly 3 times relative to a ZnO TFT. This inference is consistent with the value of N_{BS} extracted from the subthreshold slope. Thus, the improved thermal stability and electrical characteristics of $Mg_{0.06}Zn_{0.94}O$ TFT can be mainly attributed to a

reduced density of oxygen vacancies and the associated electron traps by incorporation of Mg ions into ZnO.

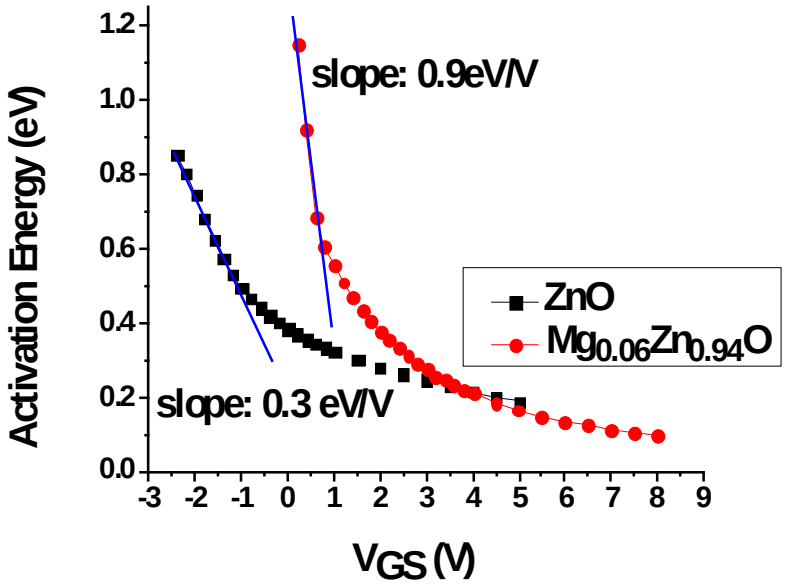

Figure 5.5 The extracted activation energies as a function of V_{GS} for ZnO and $Mg_{0.06}Zn_{0.94}O$ TFTs.

5.7. Summary

In summary, with 6% Mg incorporation into a ZnO channel, the field effect mobility and subthreshold swing values are improved. A smaller (negative) shift of threshold voltage and higher activation energy are observed. XPS results imply a reduced amount of oxygen related defects including oxygen vacancy after Mg incorporation. The improved electrical characteristics and thermal stability of $Mg_{0.06}Zn_{0.94}O$ TFT are mainly attributed to the suppression of oxygen vacancies by introducing stronger Mg-O bonding in the channel layer.

Chapter 6

Improvement of Negative Bias Stress Stability in $Mg_xZn_{1-x}O$ TFTs

We demonstrated that Mg incorporation into ZnO improves electrical characteristics and thermal stability of $Mg_xZn_{1-x}O$ ($0<x<0.06$) TFTs in the previous chpater. This is attributed to the reduction of oxygen vacancies in $Mg_xZn_{1-x}O$ ($0<x\leq0.06$) TFTs. In this chpater, we further investigate the effects of Mg incorporation on negative bias stress stability in $Mg_xZn_{1-x}O$ ($0<x\leq0.06$) TFTs. Typically, bias stress instability is defined as the shift of threshold voltage after bias stress testing. For application of TFTs as the driver/switch devices, stability against negative stress bias is very critical. Since n-type TFTs possess higher mobility than p-type TFTs, switching devices in large area electronics are made of n-type TFTs. In this case, negative gate bias voltages are required to turn off n-type TFTs to reduce power consumption of the system. For display systems, n-type TFTs are usually operated in the “OFF” state, which lasts more than 500 times longer than the “ON” state. The instability introduced after bias stress can result from charge trapping at channel/dielectric interface, defect re-distribution and defect creation. Despite intensive studies of ZnO based TFTs, there are still few reports on the enhancement of bias stress stability via in-situ doping/alloying. In this chapter, we demonstrate the improvement of negative bias stress stability in $Mg_xZn_{1-x}O$ ($0 < x \leq 0.06$) TFTs and explore its mechanism. The composition of Mg in this study is 3% which deviates from the Mg composition (6%) in previous chapter. Despite deviation in Mg composition is oberved, the electrical characteristics and stablity in $Mg_{0.03}Zn_{0.97}O$ TFT

are improved. The results for $Mg_{0.06}Zn_{0.94}O$ TFTs and $Mg_{0.03}Zn_{0.97}O$ TFTs are representative for each other.

6.1. Introduction

Since the first appearance in 2003, zinc oxide (ZnO) based TFTs have attracted intense attention due to its promising potential as the driving/switching devices used in large area display systems, such as active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs). ZnO based TFTs possess advantages including higher electron mobility (~10-50cm^2/V-s), transparency in visible light region, and superior radiation hardness over the amorphous silicon (a-Si) TFTs which have dominated current display technologies as switch devices in control circuitry. However, the conventional a-Si TFTs are facing severe challenges due to low electron mobility ($\leqq$1 cm^2/V-s) and opacity. It was analyzed that a-Si TFTs would be difficult to drive liquid crystal displays with a size larger than 55 inches or with a frame rate higher than 120Hz [76]. As new display systems demand low power consumption, high resolution, large area, and fast refresh rate, ZnO based TFT technology has been emerging as a promising candidate of the future displays.

For application of TFTs as the driver/switch devices in a display system, stability against bias stress is the key pre-requisite. The brightness of each pixel is determined by the drain current of the driving TFT. TFTs must remain stable over time; any shift in threshold voltage would change the brightness of individual pixels, introducing non-uniformity of displays. In addition, switching TFTs in a display are n-type transistors. The device usually operates in the “OFF” state, which lasts more than

500 times longer than the “ON” state. In the “OFF” state, a negative gate voltage is applied to the n-type TFT in order to turn off the transistor and reduce the power consumption of a display. Therefore, it is critical to examine and then improve NBS stability of ZnO based TFTs.

Several studies indicate that defects and associated charge carriers in the conducting channel could introduce electrical instability in ZnO TFTs. Kamada [77] *et al.* studied the effect of channel stoichiometry on bias instability of ZnO TFTs, of which the conducting channels were deposited by RF sputtering under different oxygen partial pressures. Negative shifts of TFT’s transfer characteristics were observed under NBS. The origin of a shift in threshold voltage (ΔV_{TH}) under NBS was related to the electrically activated donor trap type of defects by the negative bias. Kim [78] *et al.* reported the effect of Hf doping on NBS stability in ZnO TFTs grown by RF sputtering. A small amount of Hf (0.8 atom %) was added into the ZnO target. The improvement of ΔV_{TH} against bias stress was attributed to the reduction of trap density, which is related to the suppression of oxygen vacancies due to Hf ions acting as oxygen binders. We have reported that Mg can effectively suppress oxygen vacancy related defects in $Mg_xZn_{1-x}O$ ($x\leq0.06$) (MZO) TFTs, leading to improved electrical characteristics and thermal stability[4]. In $Mg_xZn_{1-x}O$ ($x\leq0.06$), the Mg-O exhibits stronger bonding energy (393.7 kJ/mole) than that of Zn-O (284.1 kJ/mol). Furthermore, Mg^{2+} substitution in the Zn^{2+} site does not cause significant lattice distortion owing to their similar ionic radii (Mg^{2+}:0.57 Å *vs* Zn^{2+}:0.60Å). Thus, it requires more energy to form an oxygen vacancy in $Mg_xZn_{1-x}O$ ($x\leq0.06$) [79,80]. It is desired to have the oxide TFTs with high performance and superior stability (including NBS stability). The newly developed TFT technologies using

InGaZnO or InZnO as the channel material are promising. On the other hand, the stable MZO TFT technology could be another attractive candidate because the elimination of Indium in the TFTs would significantly reduce the product cost, in particular, for large area electronic products such as displays. In this thesis chapter, we report the effect of a small amount of Mg in the MZO TFT channel on NBS stability. The amount of Mg incorporation is kept low in $Mg_xZn_{1-x}O$ (x=0.03) to avoid the degradation of TFT electrical characteristics from the alloying induced scattering and disorder.

6.2. Experimental Procedure and Testing

The device fabrication procedure can be referred to chapter 5.2. All the electrical/NBS stability tests are conducted in a light-tight probe station using a HP-4156C electrical testing system at room temperature. During NBS stability testing, a constant voltage of -20V is applied to the gate electrode to ensure a uniform electrical field (5MV/cm) distribution along the channel layer while source/drain contacts are shorted together (V_{DS}=0V). The NBS stability testing is conducted over duration of 7,200 sec. I-V characteristics of different devices are immediately recorded by the ICS software after accumulating NBS time reaches different duration (t_{NBS}=300 sec, 1,800 sec, 3,600 sec, and 7,200 sec). Each series of NBS stability testing is performed on the same TFT and thermal annealing (100°C) is applied prior to each new NBS stability testing to ensure consistent TFT initial properties.

6.3. Electrical Characterization

Figure 6.1 (a) and (b) show atomic force microscopy (AFM) images with scan areas of 5x5 μm^2 for $Mg_{0.03}Zn_{0.97}O$ and ZnO channel layers, respectively. The values of root-mean-square (rms) roughness of $Mg_{0.03}Zn_{0.97}O$ and ZnO channel layers are 2.90 nm and 2.70 nm, respectively. Both channel layers exhibit similar feature, suggesting a reduced role of surface morphology on electron transport from the source to the drain. The I-V characteristics of ZnO and $Mg_{0.03}Zn_{0.97}O$ TFTs with V_{DS}=10V (saturation region) and V_{DS}=0.1V (linear region) are depicted in Figure 6.2 (a) and Figure 6.2 (b), respectively. The threshold voltage (V_{TH}) is defined as the gate voltage value when a drain current (I_{DS}) reaches 10^{-9} A. The field effect mobility (μ_{FE}) is extracted from the linear region. The subthreshold swing (S) is extracted from a 3-decades range in the subthreshold region of the $\log_{10}(I_{DS})$ *vs* V_G curve with V_{DS}=10V:

$$S = \left[\frac{\partial log_{10}(I_{DS})}{\partial V_G}\right] \quad (6.1)$$

Both ZnO and $Mg_{0.03}Zn_{0.97}O$ TFTs have the same threshold voltage of -2V. The $Mg_{0.03}Zn_{0.97}O$ TFT exhibits higher μ_{FE} of 30 cm^2/V-s and smaller S of 0.28 V/dec while the ZnO TFT shows μ_{FE} of 20 cm^2/V-s and S of 0.40 V/dec. It indicates that a small amount of Mg added into ZnO channel layer improves electrical characteristics of TFTs.Since all TFTs are built on the same gate and dielectric layers, it can be assumed that the differences of μ_{FE} and S values between the two different TFT channels mainly result from the different bulk trap densities measured during electrical tests. The

maximum bulk trap density (N_{BS}) in the channel can be extracted from the subthreshold swing S [81]:

$$S = log_e 10 * {}^{kT}/_{q} * [1 + q * t * N_{BS}/C_{\text{ins}}] \quad (6.2)$$

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, t is the thickness of the channel, and C_{ins} is the capacitance of the insulator. The extracted values of bulk trap density, N_{BS} for ZnO and $Mg_{0.03}Zn_{0.97}O$ are 6.14 x 10^{17} cm^{-3} and 3.97 x 10^{17} cm^{-3}, respectively. It implies that fewer defect states are present in the $Mg_{0.03}Zn_{0.97}O$ channel layer. From our previous XPS results, intensity of O_{1s} spectrum associated with oxygen related defects in $Mg_xZn_{1-x}O$ ($x \leq 0.06$) is reduced [82]. Because of higher Mg-O bonding energy in comparison with that of Zn-O, the incorporation of Mg into ZnO would increase the formation energy of oxygen vacancy, resulting in a decreased amount of oxygen vacancies in the channel layer.

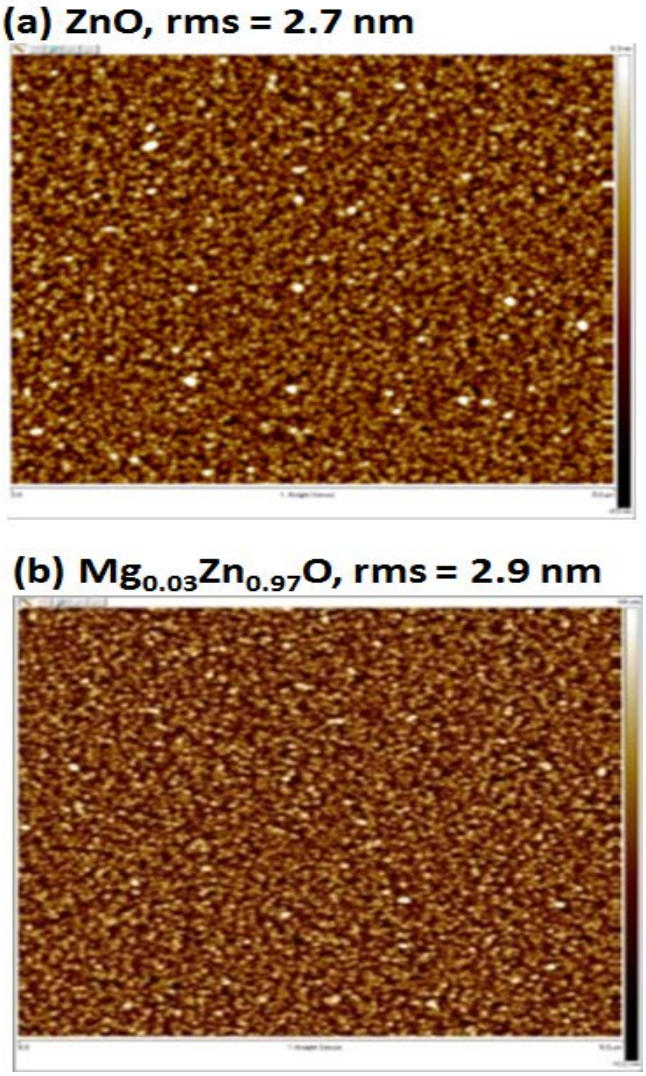

Figure 6.1 AFM images of (a)ZnO and (b) $Mg_{0.03}Zn_{0.97}O$ channel layers with scan area of 5x5 μm^2 and the maximum height is 10nm.

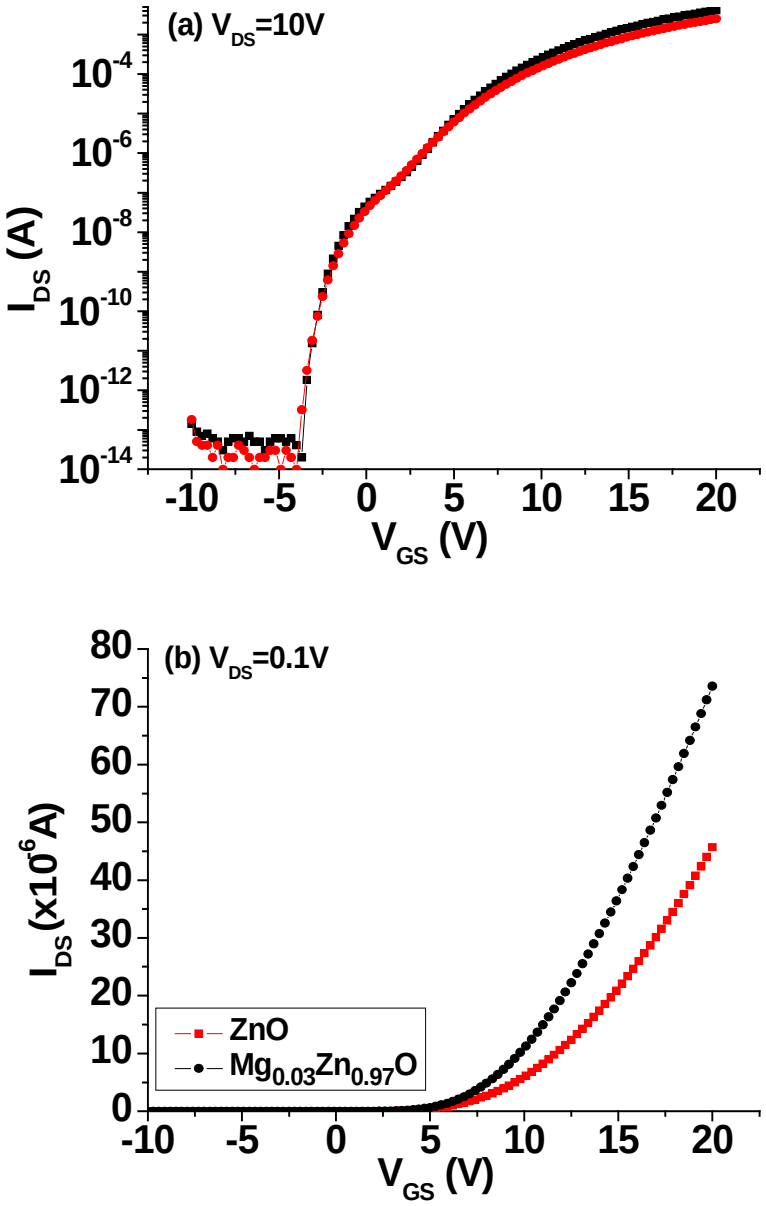

Figure 6.2 I_{DS}-V_{GS} transfer characteristics of ZnO and $Mg_{0.03}Zn_{0.97}O$ TFTs (a) in the saturation region (V_{DS} =10V) (b) in the linear region (V_{DS} =0.1V).

6.4. Negative Bias Stress Stability

Figure 6.3 (a) and (b) illustrate transfer characteristics for $Mg_{0.03}Zn_{0.97}O$ and ZnO TFTs with V_{DS}=10V under NBS stability testing. Negative shifts of transfer characteristic curves are observed with different t_{NBS} for $Mg_{0.03}Zn_{0.97}O$ and ZnO TFTs. The TFT instability after NBS is specified as the change of threshold voltage (ΔV_{TH}). The NBS induced ΔV_{TH} after t_{NBS}=7,200 sec for $Mg_{0.03}Zn_{0.97}O$ and ZnO TFTs are -2.97V and -5.76V, respectively. It is found that for $Mg_{0.03}Zn_{0.97}O$ TFT the S value changes from 0.28 V/dec to 0.29 V/dec while for ZnO TFT the S value degrades from 0.40 V/dec to 0.49 V/dec, respectively. The negative shifts of transfer characteristics for ZnO based TFTs after NBS imply that the trapping of positive charges occurs at channel/dielectric interface. The trapped positive charges at channel/dielectric interface screen the gate electrical signal, leading to negative shifts of I_{DS}-V_{GS} curves. This also means that less gate voltage is required for a TFT to accumulate the same amount of electrons in the channel layer without NBS. In our case, it is unlikely that holes are the origin of positive charges since concentration and mobility of holes are extremely low in the ZnO based TFT channels. The origin of trapped positive charges could be attributed to the ionization of the existing oxygen vacancies in the channel layer and their subsequent migration to the channel/dielectric interface under NBS. Field effect mobility corresponding to different t_{NBS} is obtained from time evolution of I_{DS}-V_{GS} curves for $Mg_{0.03}Zn_{0.97}O$ and ZnO TFTs at V_{DS}=0.1V, as shown in Figure 6.3 (c) and (d). Throughout NBS stability testing, no degradation on field effect mobility is observed for MZO and ZnO TFTs. The negative shifts of transfer curves in conjunction with degradation of S values in both $Mg_{0.03}Zn_{0.97}O$ and ZnO TFTs suggest generation and/or re-distribution of defect states

after NBS. These defect states may exist in deep levels rather than shallow levels since they affect accumulated electrons before the Fermi level approaches to conduction band minimum (CBM) without deterioration of μ_{FE}. It is observed that degradation of subthreshold swing becomes more significant as t_{NBS} increases for both ZnO and $Mg_{0.03}Zn_{0.97}O$ TFTs. In addition, degradation of subthreshold swing for the ZnO TFT is much larger than that of the $Mg_{0.03}Zn_{0.97}O$ TFT after NBS. It is possible that ionization and migration of oxygen vacancies during NBS could change the distribution of deep level states, affecting the subthrehold swing. The introduction of Mg leads to a reduced amount of oxygen vacancies in the channel and a more uniform (less dispersive) distribution of deep level states. During NBS, slighter shift of threshold voltage and smaller degradation of subthreshold swing are obtained for the $Mg_{0.03}Zn_{0.97}O$ TFT than that of the ZnO TFT.

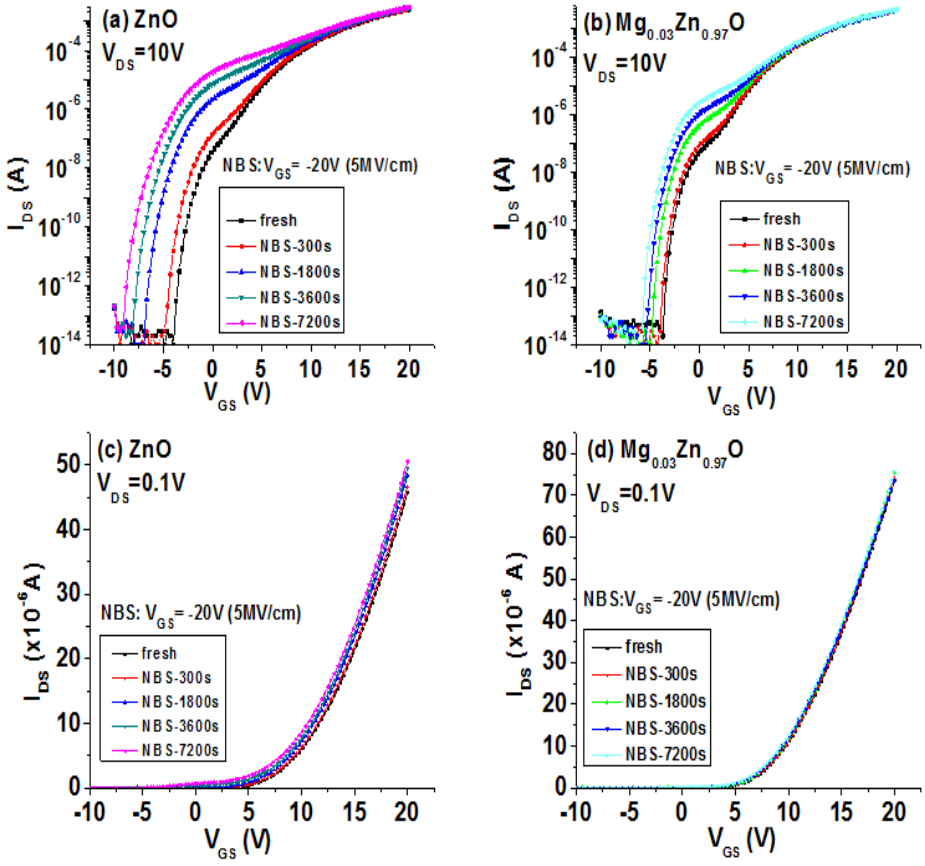

Figure 6.3 The evolution of transfer characteristics (I_{DS} vs. V_{GS}) for V_{DS} =10V during NBS testing of (a) ZnO TFT and (b) $Mg_{0.03}Zn_{0.97}O$ TFT; the evolution of transfer characteristics for V_{DS} =0.1V during NBS testing of (c) ZnO TFT and (d) $Mg_{0.03}Zn_{0.97}O$ TFT.

The shifts of threshold voltages (ΔV_{TH}) with respect to different bias stress times (t_{NBS}) are fitted into the stretched-exponential model [83], as illustrated in Figure 6.4. The stretched-exponential equation during bias stress is defined as

$$|\Delta V_{TH}(t)| = |\Delta V_0| \left\{ 1 - exp\left[-\left(\frac{t_{NBS}}{\tau} \right)^{\beta} \right] \right\} \quad (6.3)$$

where $\Delta V_{TH}(t)$ represents the threshold voltage shift induced by bias stress, ΔV_0 is effective voltage drop across the gate dielectric layer, β is the stretched exponential exponent, and τ is the characteristic trapping time for carriers. The obtained β values are similar to the two devices: β =0.59 for the $Mg_{0.03}Zn_{0.97}O$ TFT and β =0.56 for the ZnO TFT. The β value represents the distribution of time constants that characterize the trapping process, reflecting the width of involved trap distribution [84]. The value of β ~ 1 indicates a narrow distribution; on the contrary, β < 1 depicts a broader distribution of time constants. The fact that the extracted β values are less than unity in both $Mg_{0.03}Zn_{0.97}O$ and ZnO TFTs implies a dispersive carrier transport. Furthermore, a larger β value in the $Mg_{0.03}Zn_{0.97}O$ TFT suggests that its trap distribution is more uniform than that of ZnO TFT. The extracted τ values for $Mg_{0.03}Zn_{0.97}O$ and ZnO TFTs are 1.26 x 10^5 sec and 4.07 x 10^4 sec, respectively. The larger τ in $Mg_{0.03}Zn_{0.97}O$ TFT is the indication of less charge trapping during NBS.

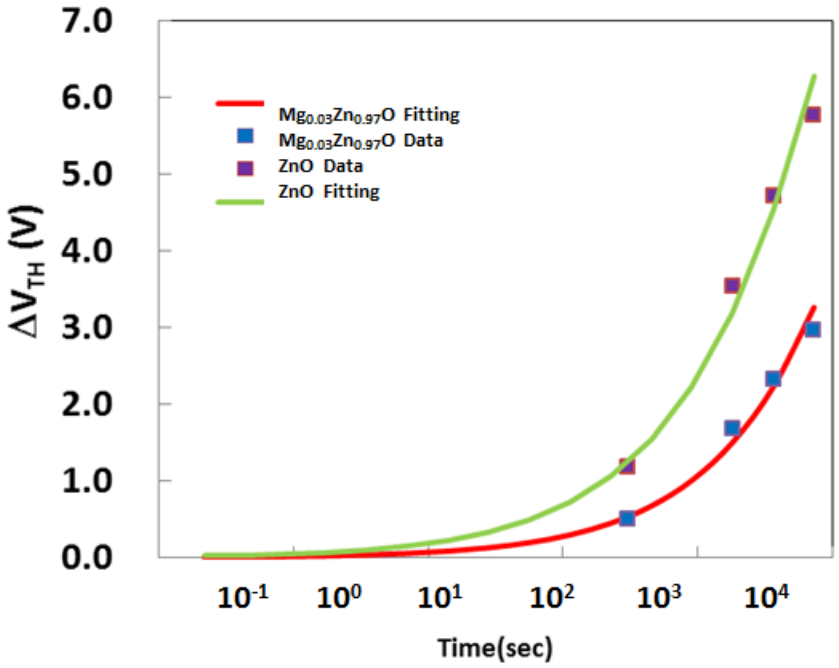

Figure 6.4 Graph of absolute value of ΔV_{TH} with respect to NBS stress time. The obtained data are fitted into stretched exponential equation (solid lines).

6.5. Results and Discussions

Theoretical calculations show that the oxygen vacancy is a "*negative-U*" center, meaning that charge state transition is directly from +2 (V_o^{2+}) to the neutral (V_o) as the Fermi level moves toward CBM and V_o^{+} is never thermodynamically stable [85]. The transition level is located at ~ 1 eV below CBM and the oxygen vacancy is now widely accepted as a deep level donor rather than a shallow donor in ZnO. The oxygen vacancy assumes the +2 charge state when the Fermi level is near the valence band maximum (VBM) and has relatively low formation energies. The ionization of oxygen vacancy compensates the p-type doping in ZnO, making it very difficult to obtain p-channel operation for ZnO based TFTs.

The instability induced by NBS in ZnO based TFTs could be the result of ionization of existing oxygen vacancies in the channel and their subsequent migration toward the dielectric/channel interface. For a fresh device, the Fermi level is near CBM and the oxygen vacancy is at the neutral charge state. During NBS, the depletion region is created in the ZnO channel layer, giving rise to the larger upward bending of energy band. Inside the depletion region, the quasi Fermi level is lowered to near midgap level and becomes closer to VBM, reducing formation energies of ionized oxygen vacancies. The ionization from V_o to V_o^{2+} introduces outward relaxation of neighboring Zn atoms. Due to a high electric field and a long duration under NBS, presence of V_o^{2+} could cause position changes of surrounding atoms, including ones that are distant from V_o^{2+}. In this case, the rearrangement of atomic structure induced by V_o^{2+} increases the energy barrier for returning its initial position [86], leading to the stabilization of V_o^{2+}. As duration of NBS prolongs, the migration of oxygen vacancies takes place. The migration of oxygen

vacancies involves in that a nearest-neighbor oxygen atom in the oxygen lattice jumps into the original vacant site leaving a vacancy behind. The calculated migration energy barrier for V_o^{2+} is 1.7 eV and for V_o is 2.4 eV, making V_o^{2+} more mobile under an electric field [85]. Under NBS, mobile V_o^{2+} can migrate to dielectric/channel interface and become trapped positive charge, which causes NBS instability later.

Figure 6.5 (a)-(d) depict the energy band diagrams of ZnO and $Mg_{0.03}Zn_{0.97}O$ TFTs in "fresh" state and under NBS. Before NBS, the amount of oxygen vacancies in the $Mg_{0.03}Zn_{0.97}O$ TFT is less than that in the ZnO TFT due to higher Mg-O bonding energy. During NBS, a substantial fraction of oxygen vacancies existing in the channel layer are ionized and then migrate toward the channel/gate dielectric interface. Thus, a reduced amount of ionized oxygen vacancies in the $Mg_{0.03}Zn_{0.97}O$ TFT provides fewer free electrons to the $Mg_{0.03}Zn_{0.97}O$ channel and the TFT turn-off will require less negative gate bias. In consequence, a smaller negative shift of threshold voltage is observed and the improvement of NBS stability is obtained for the $Mg_{0.03}Zn_{0.97}O$ TFT.

The ionization and migration of oxygen vacancies in ZnO-based TFT channels could be related to the "loosely bound oxygen", since it requires lower energy to move a loosely bound oxygen from its original site into a vacant site. Our previous studies in X-ray photon emission spectra (XPS) showed that a small Mg composition introduced into the ZnO channel layer would strengthen the atomic bonding. The current work demonstrates that the overall improvement of NBS stability in $Mg_{0.03}Zn_{0.97}O$ TFTs over ZnO TFTs mainly arises from the reduction of loosely bound oxygen and oxygen vacancy related defects.

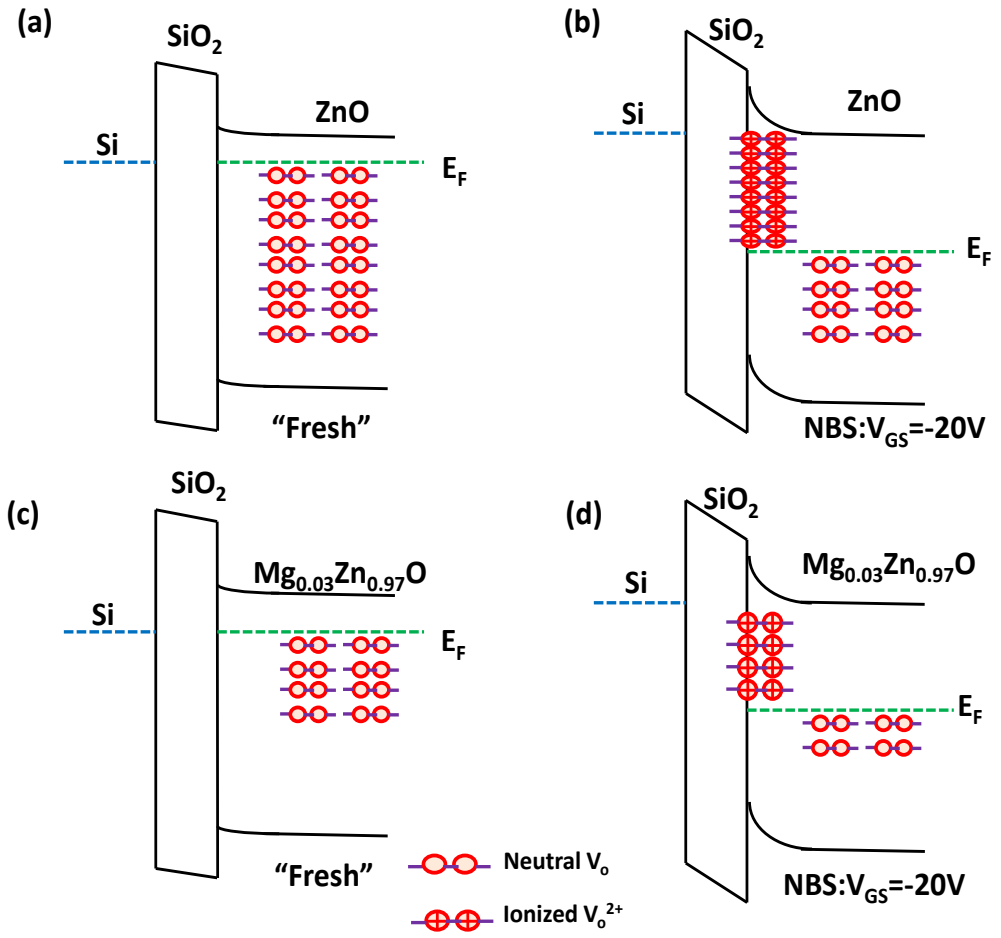

Figure 6.5 The schematic energy band diagrams of a ZnO TFT (a) at fresh state, (b) under NBS; and of a $Mg_{0.03}Zn_{0.97}O$ TFT (c) at fresh state, and (d) under NBS. The neutral oxygen vacancies are ionized and migrate to the channel/dielectric interface during NBS.

6.6. Summary

In conclusion, the improvement of NBS stability in $Mg_{0.03}Zn_{0.97}O$ TFTs over pure ZnO TFTs has been demonstrated in terms of less negative shift of threshold voltage and minimized degradation of subthreshold swing. The origin of negative shifts of transfer curves in ZnO-based TFTs after NBS is associated with the ionization and migration of oxygen vacancies. The enhancement of NBS stability in $Mg_{0.03}Zn_{0.97}O$ TFTs is mainly attributed to the strengthened atomic bonding after introduction of a small Mg composition into ZnO, leading to the suppression of oxygen vacancies.

Chapter 7

Conclusion and Suggestions for Future Work

7.1. Conclusion

ZnO is a wide bandgap semiconductor that has excellent properties such as high electron mobility, transparency in visible light region, and superior radiation hardness for TFT applications. ZnO films can be grown on various substrates including glass and Si at relative low temperature, which is critical for TFT technologies. The potential applications of ZnO TFTs include high definition (HD) and 3D display systems, transparent electronics, flexible electronics and large area sensor arrays. To implement ZnO TFTs into commercial electronics, several issues have to be studied and resolved. First, the intrinsic defect density in ZnO active channel layer has to be reduced in order to reach high performance TFT devices. Second, the instability of threshold voltages caused by temperature and bias stress must be improved since any variation in threshold voltages would change the operation voltages of ZnO TFTs.

The goal of this dissertation project is research and improvement of ZnO based TFT technology with high performances and stability. The project focuses on (i) design and growth of ZnO thin films as the channel layers to realize enhancement mode ZnO TFTs, (ii) reduction of intrinsic defects such as oxygen vacancies by applying post-annealing, (iii) development of *in-situ* alloying of MgO into ZnO to form the ternary $Mg_xZn_{1-x}O$ ($0 < x \leq 0.06$) as the new channel material for TFTs for improvements of electrical characteristics and thermal stability, and (iv) development of $Mg_xZn_{1-x}O$ ($0 < x \leq 0.06$) TFTs for the enhancement of negative bias stress stability.

In this dissertation, we designed and fabricated the inverted staggered bottom gate ZnO TFTs on Si and glass substrates. To account for non-ideality of ZnO based TFTs, the universal compact model is utilized throughout this thesis work to consistently extract TFT parameters. Polycrystalline ZnO films as TFT active channel layers are grown by MOCVD at 350°C. Thickness of ZnO channel layer is optimized to be 55nm because of high mobility. ZnO TFTs exhibit enhancement mode of operation with high on-off ratio ($>10^8$), large field effect mobility (20-25 cm^2/V-s) and low subthreshold swing (0.8V/dec). Post-deposition annealing in oxygen ambient further boosts electrical characteristics of ZnO TFTs. The subthreshold swing is decreased from 0.86 V/dec to 0.40 V/dec, indicating a reduced amount of defect density. The XPS results suggest that the amount of oxygen ions related to oxygen vacancy is suppressed after oxygen annealing. O_2-annealed ZnO TFTs exhibit superior NBS stability over as-deposited ZnO TFTs with smaller negative shift of threshold voltage. The enhancement of electrical characteristics and NBS stability in O_2-annealed ZnO TFTs is mainly attributed to the strengthened atomic bonding after applying oxygen annealing to ZnO, leading to the suppression of oxygen vacancies.

For the first time, we demonstrated the new MZO ($Mg_xZn_{1-x}O$, $0 < x \leq 0.06$) TFT technology by utilizing in-situ alloying of MgO and ZnO to form the ternary MZO as the TFT channel layer. The novel MZO TFTs feature superior electrical characters..In MZO TFTs, Mg^{2+} ions are incorporated to prevent oxygen out-diffusion and hinder the formation of oxygen vacancies in the TFT channel due to higher bonding energy of MgO than that of ZnO. The Mg composition in this work is limited to no more than 10% to minimize deterioration of the field effect mobility due to alloy disorder. With 6% Mg

incorporation into a ZnO channel, the field effect mobility is increased from 30 cm^2/V-s to 40 cm^2/V-s and subthreshold swing is reduced from 0.54 V/dec to 0.25 V/dec.

The novel MZO TFT technology also offers the better thermal stability and the negative biasing stress (NBS) stability over the ZnO counterpart. The instability issue of threshold voltages in ZnO based TFTs is critical for many applications. For example, in a display system, any change in threshold voltage would change the operation voltages and brightness of pixels. The instability of threshold voltages may arise from temperature variation or bias stress. The thermal stability is investigated in MZO TFTs. A smaller (negative) shift of threshold voltage and higher activation energy are observed as temperature increases, indicating better thermal stability in $Mg_{0.06}Zn_{0.94}O$ TFTs. XPS results shows a reduced amount of oxygen related defects including oxygen vacancy after Mg incorporation. During NBS testing, a smaller shift of threshold voltage is observed in MZO ($Mg_{0.03}Zn_{0.97}O$) TFTs. The NBS induced ΔV_{TH} after t_{NBS}=7,200 sec for $Mg_{0.03}Zn_{0.97}O$ and ZnO TFTs are -2.97V and -5.76V, respectively. The origin of negative shifts of transfer curves in ZnO-based TFTs after NBS is associated with the ionization and migration of oxygen vacancies. The enhancement of electrical characteristics, thermal stability and NBS stability in MZO TFTs is mainly attributed to the strengthened atomic bonding after introduction of a small Mg composition into ZnO, resulting in the suppression of oxygen vacancies.

It is worth to note that the MZO TFT technology eliminates the high temperature oxygen annealing process of ZnO TFTs. The lower thermal budget makes this technology particularly suitable for the applications of flexible electronics and system on glass (SOG).

7.2. Suggestions for Future Work

Even with the extensive research that has been done in ZnO-based TFTs, the field is still in its early stages. In order to be integrated into commercial electronics, instability issue of threshold voltage in ZnO-based TFTs needs to be resolved. We have shown that in-situ alloying of Mg in MZO TFTs enable to improve the thermal stability and NBS stability. However, the fundamental mechanisms remain to be investigated in order to improve and then implement this novel MZO TFT technology. Moreover, more studies have to be made in creating system on glass (SOG) consisting of ZnO based TFTs so that logical functions along with pixels can be embedded onto the same glass substrate and the need for bulky components is removed. As we move on to mobile electronics with lower power consumption, lighter weight and ultra-high definition display system, a more complicate design is needed for the TFT integration and material growth. The following new generation of ZnO-based TFT devices and platforms should be studied:

Further Improvement of MZO TFTs: To implement MZO TFT devices for the display system, continuous improvement in MZO TFTs has to be conducted. First, electron transport mechanism during TFT operation must be investigated. Intrinsic defects in MZO channel layers play important roles to determine the I-V characteristics. Our results suggest suppression of oxygen vacancy improves TFT performance. However, different intrinsic defects may also be activated during various TFT operation modes. More sophisticated techniques such as conductance-voltage, capacitance-voltage, pulse I-V, PL, charge pumping, low frequency noise measurement have to be applied to gain insightful understanding of electron transport and charge trapping mechanisms during TFT operation. Charge trapping at grain boundaries in the polycrystalline active channel layers

is critical. Any change in distribution of grains in the active channel layer would affect electrical characteristics dramatically. Therefore, TEM and XRD have to be employed to monitor the distribution of grains under different growths of channel layers. Second, the high quality interface between dielectric/active channel layers should minimize charge trapping and scattering of MZO TFTs. High-K dielectric layers could lead to superior and controlled interface properties. In particular, the integration of high quality MgO dielectric layer onto MZO active channel layer offers major advantages including continuous growth of multi-layered MgO/MZO film stack and capability of energy band engineering in MZO TFTs. Third, the source/drain Ohmic contacts have to be improved. It is important to reduce contact resistivity by ion implantation to form n+ source/drain region in order to boost the drain currents of MZO TFTs. Both implanted species and activation process have to be studied.

Integration of ZnO-based TFTs: The inverter is the basic building block in the modern digital system. Unlike complementary metal oxide semiconductor (CMOS) technologies, there is no p-type TFT in ZnO material system. Therefore, only Enhancement Load/Enhancement Driver (E-E) inverter and Depletion Load/Enhancement Driver (D-E) inverter can be utilized. E-E inverters are simple and easy to fabricated, but the gain of E-E inverters is usually low. High gain D-E inverters are very attracting with much complicated fabrication process. The main challenge is to create two active channel layers with different n-type carrier concentrations in D-E inverters. A possible solution could be the selective doping. In this case, both active channel layers of load and driver transistors are first made of enhancement mode ZnO TFTs. Only active channel layers of load devices later are subjected to n-type doping, leading to depletion mode TFTs with

increased n-type carrier concentration. Other digital circuits such as encoders/decoders and shift registers can be implemented based on D-E inverters.

Exploitation of MZO TFT Applications: The high field effect mobility of MZO TFTs makes it suitable for SOG application. However, the main challenge is to design and simulate various circuit blocks in the system. Similar to modern very large scale integrated (VLSI) circuits, the signal integrity, power consumption and propagation delay of every circuit block has to meet the specific design. Therefore, device level models and circuit level models have to be created. To account for non-ideality in MZO TFTs, many parameters must be added into SPICE models. These parameters can only be extracted from device I-V characteristics. As mentioned earlier, various sophisticated electrical characterization techniques have to be applied in order to create high level circuit SPICE models. Basic circuit blocks in the digital system such as NAND/NOR circuits, shift-registers, encoders/decoders, etc can therefore be fabricated and validated. In addition to display systems, large sensor arrays based on ZnO TFTs could also be implemented by extending of SOG concept. ZnO material has been shown to possess superior capability of bio-sensing and UV-sensing. To combine the advantages of ZnO material with TFT technologies, ZnO based TFTs are suitable for large area bio-sensor arrays or UV-imaging systems. In addition, TFT devices is a class of active devices with internal gain, active sensors built on TFT devices also provide high sensitivity. Our preliminary results have demonstrated functionalities of both bio-sensor and UV-sensor based on ZnO TFT devices. The next step will be focus on implementation of sensor arrays. Eventually, basic function blocks in a digital system including I/O core, memory, register bank and logic unit have to be designed and integrated together.

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Publications

1. **Chieh-Jen Ku**, Ziqing Duan, Pavel I. Reyes, Yicheng Lu, Yi Xu, Chien-Lan Hsueh, and Eric Garfunkel *"Effects of Mg on the electrical characteristics and thermal stability of $Mg_xZn_{1-x}O$ thin film transistors"* , APPLIED PHYSICS LETTERS **98**, 123511 ,2011
2. Pavel Ivanoff Reyes, **Chieh-Jen Ku**, Ziqing Duan, Yicheng Lu, Aniruddh Solanki, and Ki-Bum Lee *"ZnO thin film transistor immunosensor with high sensitivity and selectivity"*, APPLIED PHYSICS LETTERS **98**, 173702, 2011
3. Yang Zhang, Ziqing Duan, Rui Li, **Chieh-Jen Ku**, Pavel I. Reyes, Almamun Ashrafi, Jian Zhong, and Yicheng Lu, "*FeZnO based resistvie switching Device*", accepted by TMS & IEEE J. Electron. Mater
4. Pavel Ivanoff Reyes, **Chieh-Jen Ku**, Ziqing Duan, Yi Xu, Eric Garfunkel and Yicheng Lu
   "*Reduction of Persistent Photoconductivity in ZnO Thin Film Transistor based UV photodetector*" APPLIED PHYSICS LETTERS **101**, 031118, 2012
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