DESIGN AND FABRICATION OF 4H SILICON CARBIDE GATE TURN-OFF THYRISTORS

by

LEI LIN

A Dissertation submitted to the

Graduate School-New Brunswick

Rutgers, The State University of New Jersey

in partial fulfillment of the requirements

for the degree of

Doctor of Philosophy

Graduate Program in Electrical and Computer Engineering

written under the direction of

Professor Zoran Gajic

and approved by

_____

_____

_____

_____

_____

_____

New Brunswick, New Jersey

OCTOBER, 2013

ABSTRACT OF THE DISSERTATION

Design and Fabrication of 4H Silicon Carbide Gate Turn-off Thyristors

By Lei Lin

Dissertation Director:

Prof. Zoran Gajic

Power electronics systems require robust power switches to operate at high temperatures to meet the demand for smaller and higher power density systems. The improvement in material technology has made 4H–Silicon Carbide (SiC) a promising material for power electronics applications. This is because SiC has superior properties such as high electric breakdown field, high thermal conductivity and high bandgap. Compared to other devices made on SiC, such as BJTs and IGBTs, SiC gate turn-off thyristors (GTOs) are favorable devices for power electronic applications due to their ability to operate at high current and high voltage levels under high temperature, which is attributed to conductivity modulation in the drift layer of the device. Furthermore, SiC GTOs offer several advantages over Si thyristors and Si GTOs such as compactness, higher current density, faster switching, and higher temperature operation.

This dissertation presents the design, fabrication and characterization of 4H-SiC GTOs, along with the study of the multistep junction termination extension (MJTE) for high power 4H-SiC devices. The physics-based MJTE design and optimization via numerical simulations has been studied. The 3-step MJTE with the maximum blocking voltage of 7630 V, which is 90% of the ideal breakdown voltage, has been demonstrated.

The design of MJTE has been applied to the fabrication of GTOs. 0.1 cm^2 4H-SiC greater than 6 kV GTOs have been demonstrated with MJTE utilized successfully. A relatively large area, high voltage 4H-SiC GTO that exhibits encouraging characteristic at the on- and off-state, low leakage current and high yield is presented. Initial pulse testing results shows that the fabricated GTOs can handle both the high current density and the high turn-off speed.

DEDICATION

To my family

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my dissertation advisor, Professor Zoran Gajic, for bringing out my potential, for his unwavering support, guidance, encouragement, and patience. I would like to thank Prof. Yicheng Lu, Prof. Kuang Sheng and Prof. Jian Zhao, for their technical guidance and continuous support, and for laying down the solid foundation for my future career. I would like to thank my dissertation committee members, Prof. Jaeseok Jeon, Prof. Wei Jiang, Prof. Leonard Feldman and Prof. George Celler for taking time off of their busy schedule to review and critique my dissertation.

I would also like to take this opportunity to thank Prof. Athina Petropulu, Prof. George Shoane and Prof. Warren Lai for valuable insight gained from much technical discussion over years. I also appreciate the friendship and kindness of many current and former graduate students at Rutgers whom I have had the pleasure to work with including Dr. Xiaobin Xin, Dr. Xueqing Li, Dr. Yongxi Zhang, Dr. Yuzhu Li, Dr. Petre Alexondrov, Dr. Hujun, Dr. Jianhui Zhang, Dr. Jian Wu, Dr. Rahul Radhakrishnan, Dr. Leonid Rursin, Dr. Ziqing Duan, Mr. Chieh-Jen Ku, Mr. Yang Zhang, Mr. Rui Li, Mr. Weiwei Song and Mr. Jun Tan. They all contributed in myriad ways to help my research along.

Finally, I would like to acknowledge financial support provided by Navy under the project of the SiC-based AC-link power converter, and APAR-E under the project of the completely new type of SiC bipolar switch (15kV-20kV) for utility scale inverters.

TABLE OF CONTENT

LIST OF TABLES

LIST OF ILLUSTRATIONS

CHAPTER 1 INTRODUCTION

1.1 Silicon Carbide for Power Devices

Power devices constitute the heart of modern power electronic apparatus. Depending on the specific application, power devices can be classified in terms of their current and voltage handling requirements as shown in Fig. 1-1, where the boxes indicate the device voltage and current ratings that the system requires [1]. Typically, a specific power device structure is only suitable for a certain voltage or power range application. The high-power end of this chart is dominated by power thyristors, like gate turn-off thyristors (GTOs). In the medium voltage range of 300 to 30 kV, insulated gate bipolar gate transistors (IGBTs) are usually an optimal choice with significant current handling capability. Power MOSFETs are normally used at lower voltage ratings for higher frequency applications, [1] .

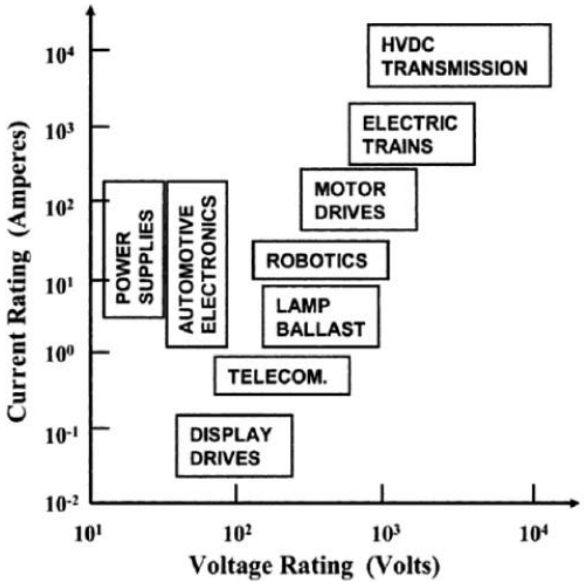


Fig. 1-1 Applications of power semiconductor devices, [1].

There is no doubt that silicon (Si) is the most commonly used semiconductor material in manufacturing power devices because of its high availability and a low production cost. However, devices based on Si are not able to operate at temperatures above 200 ^{o}C, because of excessive junction leakage currents. This limitation becomes even more severe when high operating temperatures are combined with high-power, high-frequency and high-radiation. High temperature circuits are used in various applications, such as aerospace applications, nuclear power instrumentation, space exploration, and automotive electronics. Wide band-gap materials have to be used in order to build devices capable of operation at high temperatures and high power under high frequencies. Some of the main materials of interest for such applications are shown in Table 1-1. The Baliga figure-of-merit (BFOM = $\varepsilon_r \mu E_C^3$ [2]) values for all materials in the table have been standardized to that of silicon.

Table 1-1 Material properties of the well-known semiconductors [3,4]

Material	E_g (eV)	ε_r	μ_n (cm^2/V s)	E_c (MV/cm)	v_{sat} (10^7cm/s)	λ (W/cm K)	BFOM
Si	1.12	11.8	1350	0.3	1.0	1.5	1
Diamond	5.5	5.5	2200	5.6	2.7	20.0	4260
GaN	3.39	9.0	900	3.3	2.5	1.3	676
4H-SiC	3.23	9.7	720	3.0	2.0	4.9	450

Notes: E_g – bandgap, ε_r – dielectric constant, μ_n – electron mobility, E_c – breakdown electric field, V_{sat} – saturated electron velocity, λ – thermal conductivity

From this comparison, we can see that the popular wide band-gap semiconductors are at least hundreds of times better than silicon for power devices. Even though, they do

not yet challenge silicon's existing dominance in this market, their increasingly maturing technology is expected to lead to a great commercialization success in the years to come. Power devices based on wide band-gap semiconductors have following advantages:

- The intrinsic temperature, i.e., the temperature where the intrinsic carrier concentration becomes comparable to the doping concentration, is extremely high. For example, assuming a doping concentration of 10^{15} cm^{-3}, the intrinsic temperature, at which the intrinsic carrier concentration reaches $2x10^{14}$ cm^{-3}, is approximately 1100 ^{o}C for 4H-SiC, as compared to 245 ^{o}C for Si. This makes wide band-gap semiconductors extremely attractive for high-temperature application; a suitable high temperature semiconductor technology could allow bulky aircraft hydraulics and mechanical control systems to be replaced with heat-tolerant control electronics. On-site electronics, actuators, and sensors would reduce complexity and increase reliability.
- Because the wide band-gap does not degrade the electronic properties of wide band-gap semiconductors, so the power devices based on wide band-gap materials can be useful in aerospace applications with a reduced radiation shielding.
- Because of the high electric breakdown field, the drift region can be much thinner than that of their Si counterparts for the same voltage rating, thus a much lower specific-on resistance could be obtained. With a lower specific-on resistance, the wide band-gap based power devices have lower conduction losses and higher overall efficiency.

- Because of the high-saturated drift velocity, the power devices based on wide band-gap materials could be switched at higher frequencies than their counterparts. Moreover, the charge in the depletion region of a diode can be removed faster if the drift velocity is higher, and therefore, the reverse recovery time is shorter.
- Higher thermal conductivity allows heat generated in the power devices to be more easily transmitted to the case, heat-sink and then to the ambient. Thus power devices based on wide band-gap materials have high thermal stability.

Among these wide band-gap semiconductors, diamond is often cited as the ultimate materials [5], which is readily explainable by the BFOM criteria. However, the extreme difficulties in a single crystal growth and shallow doping have kept diamond from the successful electronics development for many years.

GaN, on the other hand, has been a notable alternative to SiC and is under active research worldwide by many teams. However, the difficulty in the GaN native substrate technology and the high defect density in GaN epilayers still raises serious concerns and questions, making it less successful than SiC for power device applications.

In short, although Silicon Carbide (SiC) does not possess the highest BFOM in the group, it is by far the most matured and commercially available wide bandgap material compared to its alternatives. In addition, 4H-SiC, the most commercially available polytype of SiC, offers more favorable properties compared to the others, such as 3C-SiC and 6H-SiC. Today's SiC material suppliers like Cree are already offering zero-micropipe density 4H-SiC wafers up to 100 mm in diameter. Given the vastly improved material technology as of today and the superior properties of SiC over silicon, we

strongly believe that this is the right time to engage in the development of novel power device and integrated circuit technologies on 4H-SiC.

1.2 4H-SiC Bipolar Switching Devices

There has been a rapid improvement in SiC materials and power devices during the last few years SiC unipolar devices such as Schottky diodes, JFETs and MOSFETs have been developed extensively and advantages of insertion of such devices in power electronic systems have been demonstrated [6, 7]. However, unipolar devices for high voltage systems suffer from high drift layer resistance that gives rise to high power dissipation in the on-state. For such applications, bipolar devices are preferred due to their low on-resistance.

1.2.1 SiC BJTs

SiC power BJT has been developed in recent years due to its unique properties such as low on-resistance, normally-off nature, positive temperature coefficient of the on-state resistance, negative temperature coefficient of the current gain, and fast switching speed. Fig. 1-2 [8] shows a typical 4H-SiC power BJT structure. Because of the high breakdown electrical field in 4H-SiC, both the base layer and the drift-layer can be much thinner and the doping could be much higher than in Si-BJT. The thinner drift layer leads to a lower specific on-resistance, a thinner base helps to get a higher current gain. Higher doping in the drift layer is important to prevent the secondary voltage breakdown.

SiC BJTs can address the device requirements in the 600 V to 10 kV range [8,9,10, 11]. It is currently the only normally-off device in SiC which could achieve an on-resistance comparable to Silicon CoolMOS in the 600–900 V range, and exhibit the superior high temperature operation capability. Due to the absence of a gate oxide, SiC

BJTs are expected to operate in a stable manner at higher temperatures.

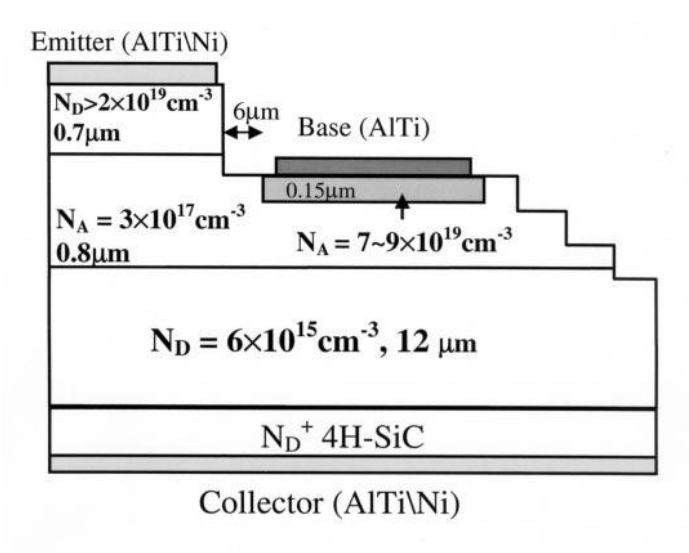


Fig. 1-2 Simplified cross-sectional view of the npn 4H-SiC BJT, [8].

The above advantages of SiC BJTs allow the system to work at higher frequencies resulting in the reduced size and cost of the passive component. This is very attractive for applications that demand a higher power density or operating temperature, such as the traction drive used in hybrid electric vehicles and power supplies. SiC BJTs have several distinguishing features: (1) Compared to SiC MOSFETs, SiC BJTs have a lower on-resistance, are free of gate oxide problem and the fabrication cost is currently less than for MOSFETs; (2) SiC BJTs exhibit a positive temperature coefficient of the on state resistance and a negative temperature coefficient of the current gain, which allow easy paralleling of SiC BJTs; (3) SiC BJTs have demonstrated a square Reverse Bias Save Operating Area (RBSOA) boundary without second breakdown; (4) the conductivity modulation of the drift layer in SiC BJTs is very minimal, which allows the device to

operate at high frequency. Moreover, a current gain of 50–70 has been routinely achieved on SiC BJTs, which can significantly simplify the gate drive circuits. [12]

The obstacle for commercialization of SiC BJTs is the presence of degradation in the on-resistance and current gain. The recombination-induced stacking faults (SFs) have been identified as a prime cause. When nucleation sites are available, SF development results in the performance degradation in SiC BJTs. These SFs originate from basal plane dislocations (BPDs). A high density of SFs corresponds to an on resistance increase after electrical stress and a significant current gain reduction. When SiC BJTs are operated in the saturation region, the base and collector regions of the transistor are flooded with electron-hole pairs. It was speculated that the recombination of electron-hole pairs in the emitter, base, and collector regions gives rise to SFs. These SFs reduce the lifetime of the minority carriers in the emitter and base, which in turn results in the reduced current gain. The increase in the on-resistance of the BJT can be explained by SFs as follows: In the drift region, SFs act as carrier traps, effectively providing local areas of increased resistivity, thereby increasing the spreading resistance of the device; in the base region, SFs significantly suppress the conductivity modulation, thus dramatically increasing the base resistance, [13].

1.2.2 SiC IGBTs

While SiC BJTs do not show substantial conductivity modulation, SiC IGBTs depend upon it for a low forward drop for more than 10 kV switches. IGBT is desirable due to its simple gate drive requirement and its great success in the silicon world. There are two types of IGBTs based on the channel polarity. A p-IGBT is composed of a p-channel MOS structure and a wide-base NPN transistor. On the other hand, an n-IGBT is

composed of an n-channel MOS structure with a wide-base PNP transistor. For typical power circuits, gate drive circuits usually reference the gate control signal to the cathode. However, in the case of p-IGBTs, the gate is referenced to the anode terminal. Technically, the SiC MOS structure has been demonstrated with high breakdown strength and a low interface charge density in recent years, paving the way for possible demonstration of IGBTs.

Both n-channel and p-channel IGBTs have been demonstrated on 4H-SiC with high blocking voltages [14, 15, 16]. Thanks to the great effort and progress made on SiC MOSFETs, n-IGBTs have been demonstrated with an excellent device performance for static and dynamic characteristics. On the contrary, p-IGBTs have taken a little longer because of the immaturity of p-MOS based design and fabrication. Theoretically, complementary SiC IGBTs should have identical specific on-resistances. With respect to the switching speed, n-IGBTs should be faster due to a much lower current gain of backside P+NP transistor than that of N+PN in p-IGBTs as shown in Fig. 1-3 [12]. However, the switching performance of p-IGBTs could be improved by optimization of the field-stop layer doping concentration, thickness and lifetime. One concern with n-IGBTs is the temperature coefficient of the forward voltage drop. The n-IGBT power handling capability might be significantly reduced at high temperatures due to the low hole mobility, [12].

After near 20 years of research since the first report of SiC IGBT, the gate oxide on SiC still continues to be the major reliability concern, especially if SiC IGBTs are to be operated at higher temperatures, although a great progress has been made for SiC MOSFETs [17]. It is widely know that the gate oxide reliability problem in actual power

switches, especially under the high electric field and temperature [18,19,20], is far from being solved because the source of the problems are fundamental: (i) hot carriers can more easily get into the gate oxide and be trapper because of the substantially smaller conduction band discontinuity in SiC/SiO_2 structure; (ii) oxidation of SiC does not lead to near perfect SiO_2 (unlike oxidation of Si) because C atoms always remain in SiO_2 while oxidation of Si leads to perfect SiO_2 (without C atom problem); (iii) n-channel carrier mobility is very low, in the range of 15 to 30 $cm^2/V/s$ when it should be in the range of 400 $cm^2/V/s$ (p-channel mobility is even lower, only about 1/8 of the n channel mobility).

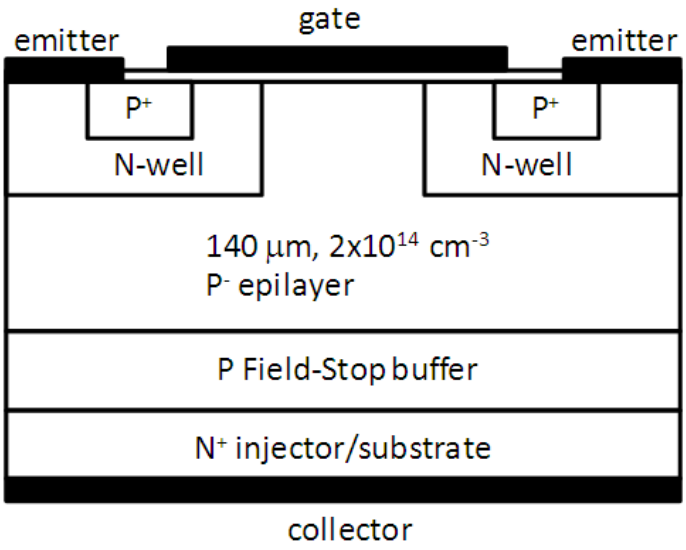


Fig. 1-3 SiC IGBT structures for p-channel, [12].

1.2.3 SiC GTOs

Some high voltage SiC MOSFETs and IGBTs have demonstrated performances superior to that of Si devices. However, the on-resistance of SiC MOSFETs and n-channel IGBTs increase significantly as the blocking voltage (≥ 5 kV) and the operating

junction temperature increase [21,22] because of the MOS reliability issue. In contrast, the SiC GTO, which not only does not have the gate oxide rupture issue, but also has the double-side carrier injection and the strong conductivity modulation in the drift region, can maintain a low forward voltage drop at high temperatures at the 10 kV to 30 kV blocking voltage level. The high voltage (10 kV-25 kV) SiC GTOs will have an important impact on the future utility applications because they can greatly reduce the number of series connected devices when compared to the silicon devices, leading to a huge reduction of the power electronic system size, weight, control complexity, cooling cost, as well as providing an improvement of the system efficiency and reliability. Therefore, 4H-SiC GTO is a very attractive device for high voltage, high power, high temperature application.

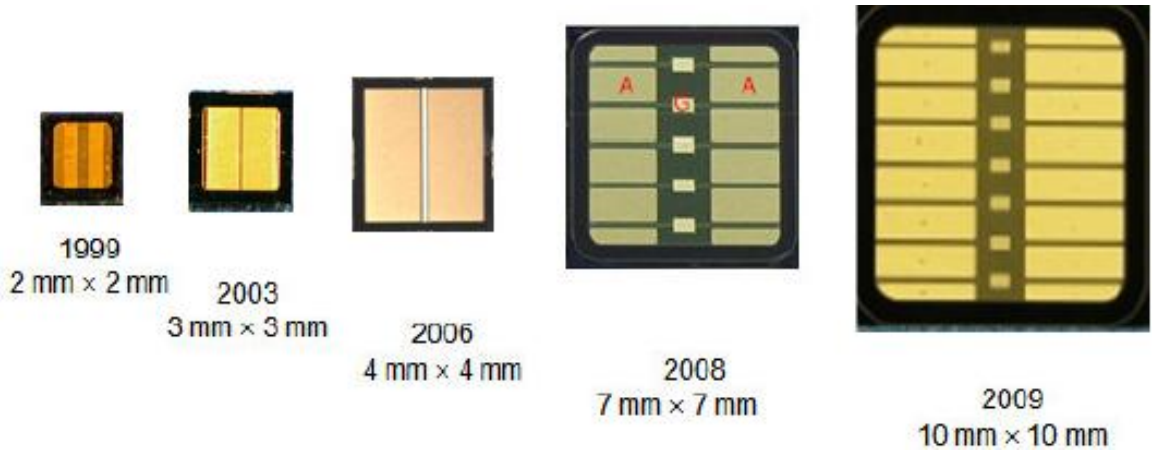


Fig. 1-4 Increase in SiC GTO chip size over the past ten years demonstrated at CREE, [26].

4H-SiC GTOs have been demonstrated by CREE, Inc., Northrop Grumman, and few universities since the late 90s for very high voltage applications in utility (for example - Fault Current Limiters) and pulse power applications [23,24,25]. The devices were made

on n-type 4H-SiC substrates resulting in an npnp structure, which is inverse of the conventional pnpn structure used in the silicon technology. This is necessary in SiC due to the high resistance of the p-type SiC substrates. The limitations on the epilayer thickness and the device footprint have generally limited these results to a few thousand volts of the blocking voltage and several amps. The small size was partially attributed to the presence of the high density of micropipes in the SiC crystal. In the last several years, the SiC technology has made tremendous strides in reducing the defect density which has enabled larger SiC GTO chip sizes as shown in Fig. 1-4 [26]. The micropipe density (MPD) has been reduced from more than 10 cm^{-2} in 90s to less than 1 cm^2 in early 2005, and eventually zero MPD published in 2008 [27]. The blocking voltage of SiC GTOs is dependent upon the thickness and doping concentration of the drift layer. As the recent improvements in the growth process of the thicker epilayer, the blocking voltage has been steadily increases from 5 kV in 2003, 6 kV in 2007 to 9 kv in 2009.

1.3 4H-SiC GTO Fundamentals

A typical device cross-section of SiC GTO is shown in Fig. 1-5. As a result, unlike silicon GTOs, SiC GTOs have anode on the top and cathode on the bottom. The gate is referenced to the anode. The anode layer is formed by epitaxial growth as in SiC BJTs since ion-implantation of p+ will cause too much damage and reduce the current gain of the PNP transistor.

To turn-on the GTO, the anode is grounded. A negative voltage is applied to the cathode and a gate current (electron current) is injected into the base resulting in the forward biasing of junction J_3 and turning on the upper PNP transistor. Its collector current provides the base current for the lower NPN transistor. The injected electrons

from the cathode region diffuse across the P- drift region and get collected by junction J_2 as the base current of PNP transistor. Once this happens, the two transistors are coupled, the thyristors latches and allows on-state current conduction without the gate signal.

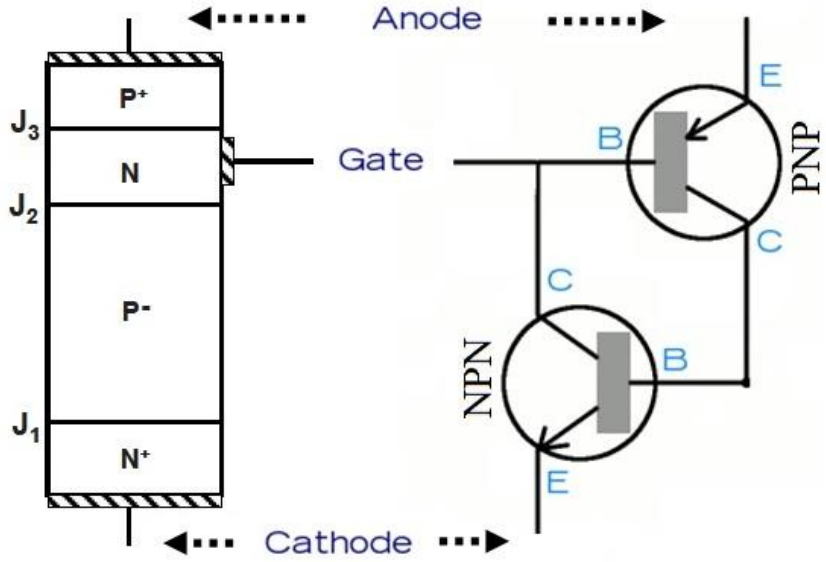


Fig. 1-5 Cross-section of a GTO cell with circuit symbols.

In Fig. 1-5 the current amplification factor of transistor PNP is called a_{pnp}, and that of transistor NPN, a_{npn}. If reverse current I_{GQ} flows through the gate, base current I_B at transistor PNP is reduced when I_{GQ} is increased. This relationship can be expressed by the following equation:

$$I_B = I_K a_{npn} - I_{GQ} \qquad \text{Eq. 1-1}$$

where I_K is the cathode current.

On the other hand, hole current I_{RB}, which disappears due to the recombination in the PNP base layer, can be expressed as follows:

$$I_{RB} = (1 - a_{pnp})I_A \quad \text{Eq. 1-2}$$

where I_A is the cathode current.

The relationship between GTO anode current I_A and cathode I_K current is expressed by the following equation:

$$I_A + I_{GQ} = I_K \quad \text{Eq. 1-3}$$

To turn off the GTO, I_B must be smaller than I_{GQ}. The magnitude of the reverse-bias current can be calculated by the following equation:

$$I_{GQ} = \frac{a_{PNP} + a_{NPN} - 1}{a_{PNP}} \times I_K \quad \text{Eq. 1-4}$$

As can be seen from what has been discussed, it is possible in theory that a GTO can carry out the turn-off if an adequate magnitude of the reverse bias current is supplied to the gate. The most important parameter during the turn-off is the gate resistance since the maximum electron current extracted from the base is dependent on the reverse blocking capability of J_3. Under this condition, the electron current conducting underneath the anode layer causes a voltage drop along the base resistance which makes J_3 in reverse bias. The maximum gate current is given by Eq. 1-5 [12]:

$$I_G = \frac{nV_{GR}}{R_B} \quad \text{Eq. 1-5}$$

where V_{GR} is the breakdown voltage of the gate-anode junction; R_B is the base resistance. n is a constant which is related to the cell design of the device.

Three important features for SiC GTOs should be noted: (i) the maximum I_G for SiC is much higher than in Si due to a higher V_{GR}; (ii) n-GTO has a much lower maximum gate current than p-GTO due to the much higher p-type base resistance; (iii) the uniformity of the base resistance is crucial to achieving a uniform turn-off of GTO,

especially for big size devices. Since the anode finger is formed by dry etching, the etching rate uniformity will directly affect the base resistance.

1.4 Edge Termination in Power Devices

Power devices operate at high voltages in the blocking mode. Along the direction of current transport, the space-charge region drops this voltage such that the electric field decreases linearly away from the junction. Under this 1-D approximation, iso-electric field contours are parallel to the junction. But since a power device is of a finite size, edges of the device are formed by cleaving the substrate. If this irregular surface were to be exposed to high electric field, voltage would not be dropped smoothly across the epitaxial layer. So, while the back side (non-junction) contact of a discrete power device covers the entire face, the front side contacts cover a smaller area outside which the potential rises to that at the backside. Hence, the high voltage at the junction also has to be dropped across the surface of the device. If no special “edge-termination” schemes are used, this voltage drops abruptly at the edge, causing a high electric field which leads to the device breakdown well below the parallel plane breakdown limit. So, various electric field termination schemes have been developed to spread the lateral electric field at the edge of the device over a wide enough region such that the lateral breakdown voltage approaches the parallel-plane breakdown voltage [1].

SiC, with its superior properties of the high breakdown field and the high thermal conductivity, is an attractive material for high-power and high-temperature applications. To utilize the high breakdown field in a high-voltage device, an efficient junction termination is needed. Among different high-voltage junction termination techniques, the

multistep junction termination extension (MJTE) has been considered as a preferred method due to its simple design and processing technique [32]. The design and optimization of MJTE for high power SiC devices will be considered in this thesis

1.5 Outline of the Dissertation

In the introduction, material properties of 4H-SiC, 4H-SiC bipolar switching devices research status, and GTO theory are reviewed. In the following chapters of this dissertation aim to further investigate these crucial issues in 4H-SiC power GTO device design and fabrication process, optimize them, and improve the overall performance of 4H-SiC GTOs.

Chapter 2 discusses the details on physics-based 2-D 3-step MJTE design and optimization by using numerical simulation and demonstrates 3-step MJTE for more than 7 kV NPN structure for high power GTOs.

Chapter 3 focuses on the design and simulation of more than 6 kV GTO. Static and dynamic characteristics will be analyzed by 2-D simulation. Then the design of GTO mask sets will be introduced after the discussion of device simulation.

Chapter 4 introduces a detailed process on GTO fabrication from the mesa etch to the metal overlay formation. Then, the dissertation presents and analyzes the static and dynamic characterization of the fabricated devices.

Chapter 5 summarizes the achievements in this research and the knowledge gained through the technology developed. A discussion on the remaining challenges and suggestions for future work are also given in this chapter.

CHAPTER 2 DESIGN AND DEMONSTRATION OF MJTE FOR 4H-SiC GTO

The edge termination is a critical technology for power devices. An effective edge termination technique makes the electric field distribution more uniform at the edge of device, in order to approach the ideal breakdown voltage capability of the epitaxial layer used. In the past, various termination techniques, which include field plate (FP) [28], guard ring (GR) [29], multizone junction termination [30] and MJTE [31], have been employed for SiC power devices. High voltage FP techniques are constrained by the need for thick oxide layers to reduce the high oxide field, and are often limited to less than 2 kV to ensure a reliable operation. The disadvantage of GR based devices is that they need accurately optimized ring spacing. In comparison to the multizone ion implantation, which requires a multistep implantation for the edge termination, the MJTE could be advantageous since no extra implantation step is needed when utilized in SiC devices with an implanted anode structure, and the extra dry etch steps can be performed by using AlTi as the etch mask, a process that is much simpler in comparison to the process for multistep ion implantation. Among all of these edge termination structures, the MJTE has become one of preferred methods due to its simple design, processing technique, and ability to achieve close to 100% of the ideal parallel junction breakdown voltage [32]. However, fundamental studies on the edge termination structure for such high voltage devices (more than 6 kV) are still limited. The effects of reducing the electric field crowding should strongly depend on the JTE etching depth. To study the effect of different etching depths of 3-step MJTE on breakdown voltage and to optimize the design, 2-D device simulation have been carried out by using Synopsys Sentaurus [33] and

compared with experimental results. In addition, by employing the 3-step MJTE, a more than 6 kV 4H-SiC GTO is experimentally demonstrated, which will be introduced in following chapters.

2.1 Junction Termination Extension (JTE)

The junction termination extension (JTE) technique [34] can give almost parallel plane breakdown voltage (up to 95%). It is convenient, because no complicated photolithography steps are needed and the amount of introduced charge can be precisely controlled by ion implantation. The JTE region should be totally depleted at the required blocking voltage applied. Key parameters of The JTE are length L_{JTE}, depth d_{JTE}, and doping concentration N_{JTE}. A schematic view of a p-n junction with the JTE region is shown on Fig. 2-1.

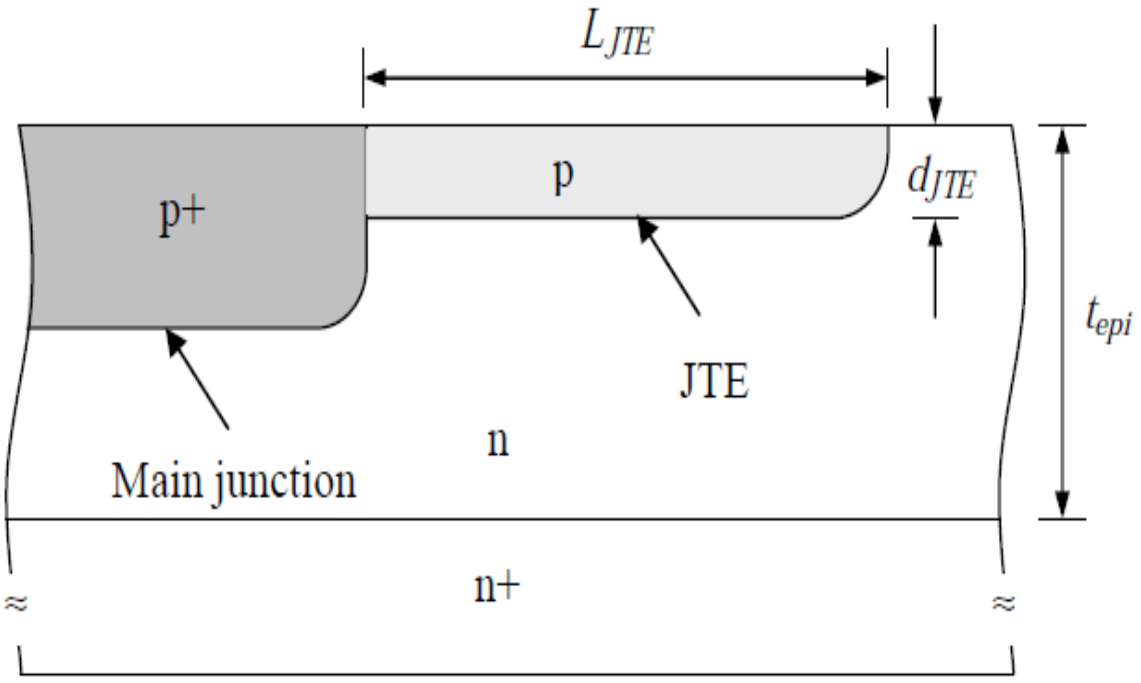


Fig. 2-1 Schematic cross section of a p-n junction with junction termination extension.

The length of the JTE is one design aspect that has a significant effect on the breakdown voltage, and it is important effect on breakdown voltage and thus is important in maximizing the available structure area. Templet et al. [35] has investigated the required JTE length through breakdown experiments with diodes of various extension length, and they have fit their results to the following empirical formula:

$$\frac{V_{BR}}{V_{BR_{ideal}}} = 1 - \exp\left(-\frac{L_{JTE}}{t_{epi}}\right) \qquad \text{Eq. 2-1}$$

where the factor (L_{JTE}/t_{epi}) is the JTE length normalized to the substrate critical depletion width. Eq. 2-1 is plotted in Fig. 2-2, which indicates that in order to achieve close 100% of the parallel plane breakdown value, the JTE length must be at least four times the substrate depletion width. Our results suggest that the JTE length be extended to about five times t_{epi}.

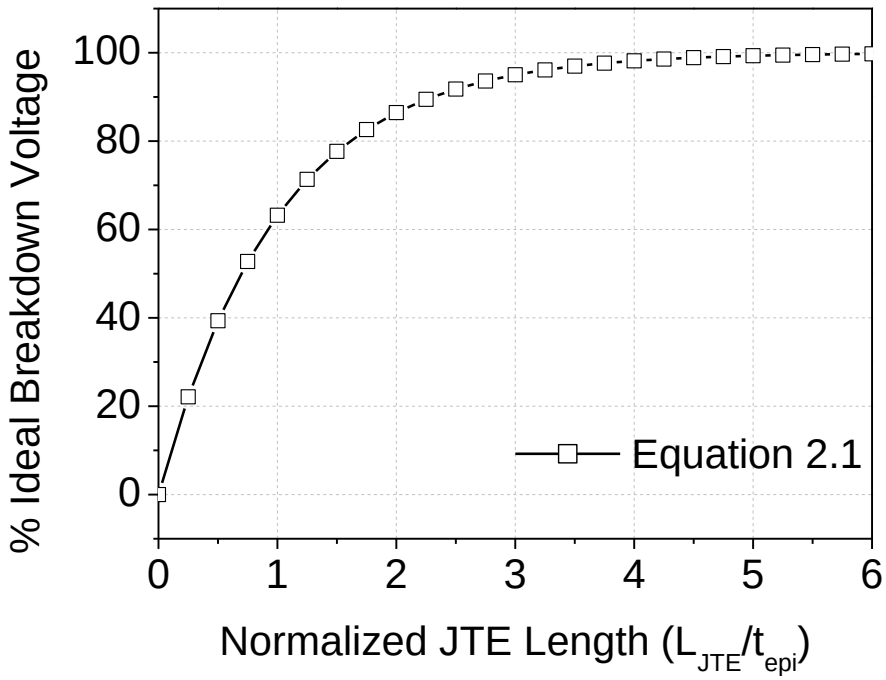


Fig. 2-2 Dependence of the breakdown voltage on the normalized JTE length.

The length should be chosen to be larger than the epilayer thickness in order to reduce the field at the surface by supporting the same voltage with a larger depletion width. However, it should not be much larger than the epilayer thickness in order to save valuable wafer space. The implanted dose D:

$$D = N_{JTE} \times d_{JTE} \quad \text{Eq. 2-2}$$

is determined by the maximum electric filed and it is equal to: $(\mathcal{E}_s \cdot E_c)/q$. If we express it in terms of the epilayer parameters it is:

$$D = N_D \times t_{epi} \quad \text{Eq. 2-3}$$

where N_D and t_{epi} are the epilayer doping and thickness respectively. Once we choose the dose, we can decide about d_{JTE} and N_{JTE}. Numerical analysis shows that for a given doping level of the junction extension, the breakdown voltage increases and then decreases, going through a maximum when the depth of the junction extension increases [36,37].

One problem with the JTE structure in SiC is the uncertainty in dopants activation, which can lead to ineffectiveness of the termination. A practical approach to realize a JTE structure is to implant it and then remove as much of the implanted thickness as needed to achieve the right charge balance. This reduces the number of photomasks needed, eliminates the uncertainty in the dopant activation efficiency, as the actual JTE charge can be adjusted by etching after implantation and dopant activation. A multiple-zone JTE structure is more effective than a single-zone JTE. The different zones are formed by additional etching steps.

In the multiple-zone JTE fabrication, the key step is to achieve an accurate dose of the implanted charge that becomes completely depleted close to the surface at the desired

breakdown voltage, thereby reducing the maximum electric field in the edge region. However, any implantation step is strongly dependent on the activation of implanted dopants that can differ with the annealing temperature and time. Furthermore, defect generation during implantation and surface degradation during the post-implantation annealling affect the device performance.

In this chapter, a mesa-etched 3-step MJTE with different etching depth has been designed and demonstrated by controlled etching into the epitaxially grown p-doped layer as a modification to the implanted etched JTE termination. Although this method is based on a precise etch-depth control and can be affected by variations in thickness and doping profile of the epitaxial layer, it may provide a less sensitive processing technique by introducing 3-step MJTE that can act as a controlling tool for compensation of any possible variation in the processing condition.

2.2 Design of 3-Step MJTE

A typical device cross-section of a NPN structure with 3-step MJTE is shown in Fig. 2-3. d_1, d_2 and d_3 are etching depths for JTE1, JTE2 and JTE3, respectively. Each JTE step has been designed of the same length of 100um. As shown in Fig. 2-3, the NPN structure was designed on an n^+ 4H-SiC substrate. The first layer on n^+ 4H-SiC substrate is an n^+ buffer. Next, a high doping p type buffer layer has been designed in order to form a punch-through structure. The above p drift layer of 60 μm thick doped to $9x10^{14}$ cm^{-3} is used to support the high blocking voltage. Finally, n-type layer with the thickness of d_{MJTE} is on the top of the p^- drift layer. Two metal contacts were designed on top n-type layer and bottom n-type substrate, respectively.

The etching depths of MJTE prove to be the most critical, since etching depths can control the charge distribution and therefore alleviate electric field crowding at the edge of the junction. The optimum etching depths of each MJTE step need to be determined by two steps: (1) 2-D device simulation and (2) experimental verification.

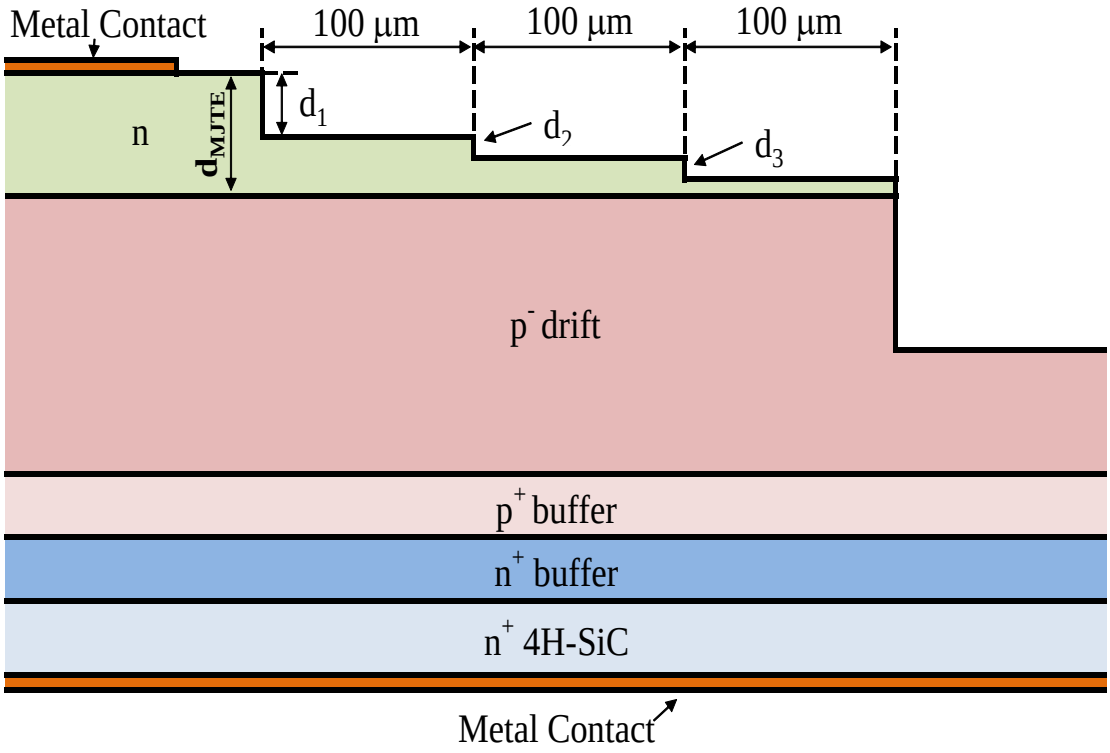


Fig. 2-3 Schematic cross-section of a NPN structure with 3-step MJTE.

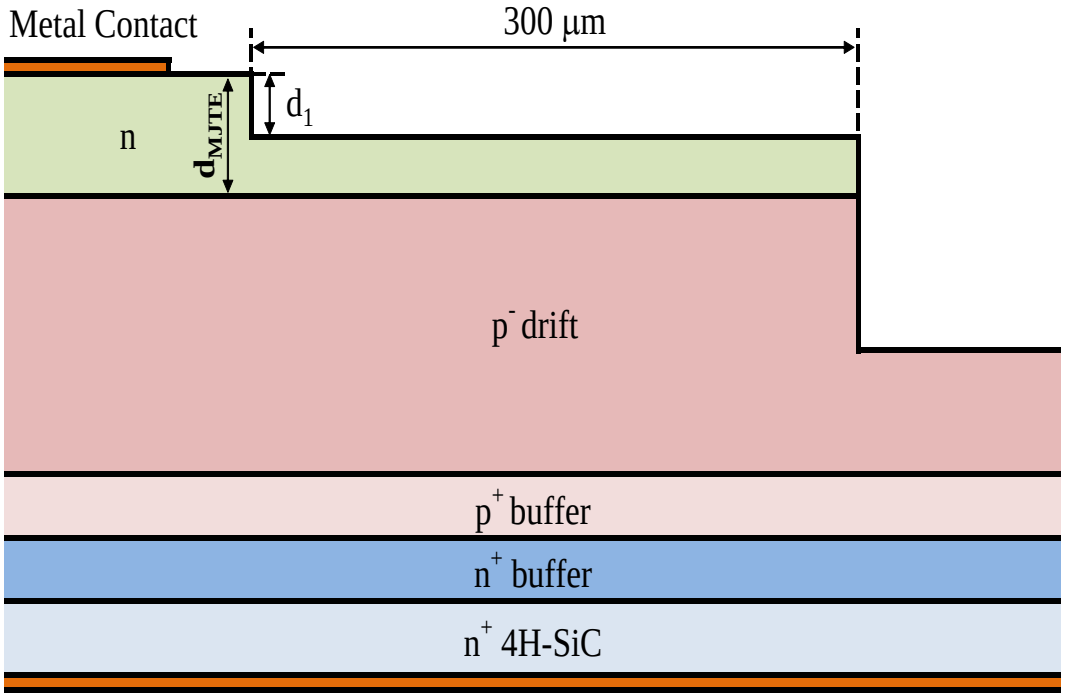
2.3 Simulation of 3-Step MJTE

2.3.1 Breakdown Voltage

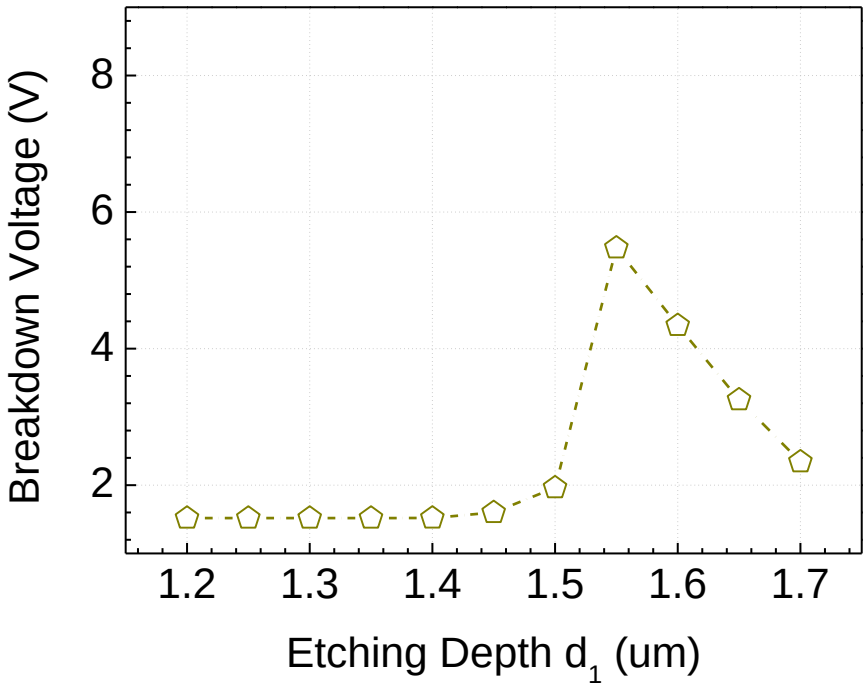
- 1-step JTE

The simulation was conducted from single step JTE structure, which is shown in Fig. 2-4 (a). With a single step 300μm long JTE, it is not possible to independently control

both the peak bulk field and the peak surface field because the charge in the 1-step JTE zone is too far from the point of peak curvature field to have a maximal effect. As shown in Fig. 2-4 (b), 1-step JTE NPN structure can reach the breakdown voltage of 5.7 kV, which is below 0.8 fraction of the ideal breakdown voltage of 8.4 kV, at the optimum point. Since a further reduction in the JTE charge to decrease the peak surface field would result in a significant lost in the blocking voltage for 1-step JTE structure, it is necessary to design a new structure with more than one JTE steps to allow further control of the peak field without compromising the breakdown voltage.



(a)

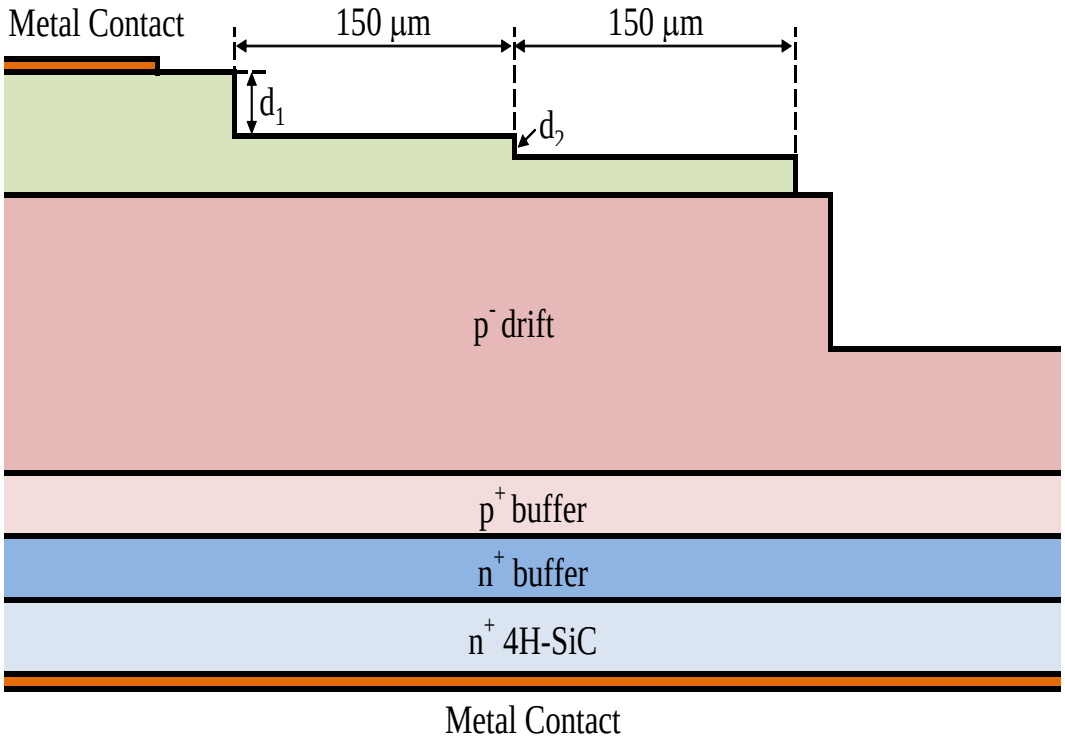


(b)

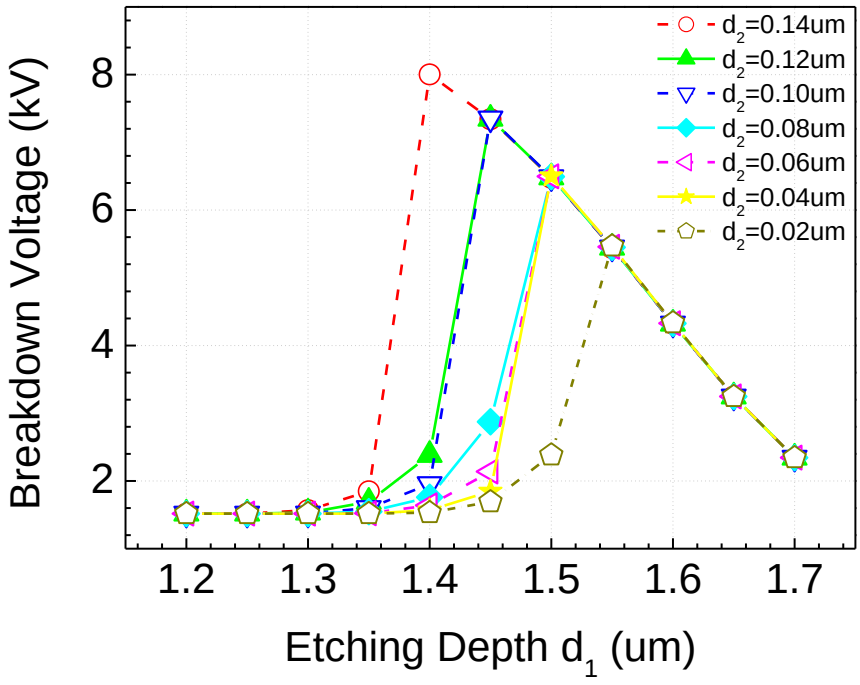
Fig. 2-4 1-step JTE structure cross section view and the breakdown voltage as a function of extents on etching depth d_1.

- 2-step JTEs

Single step JTE structure is not possible to independently control both the peak bulk field and the peak surface field of a high voltage device. Hence, 2-step MJTEs, as shown in Fig. 2-5 (a) has been designed to continue MJTE studying. 2-step MJTEs show over 95% ideal breakdown voltage at $d_1 = 1.4$ μm and $d_2 = 0.14$ μm, which indicates that the JTE2 has been fully depleted prior to the designed breakdown voltage, moving a second peak field to the junction of JTE1 and JTE2, thereby reducing the overall surface field.



(a)



(b)

Fig. 2-5 2-step JTE structure cross section view and the breakdown voltage as a function of extents on etching depth d_1.

It should be pointed out that 2-step MJTE, like 1-step JTE, is sensitive with respect to d_1, which plays a major role in control of the charge distribution in MJTE. ±5% variation of optimum etching depth d_1 will result in a premature breakdown either at the outmost JTE edge or at the corner of the main junction. Fig.2.6 shows the simulated equipotential lines at a reserve voltage of 7 kV on a 2-step MJTE with the optimum design and Fig. 2-6 (a) shows details at the encircled resign with the equipotential lines starting to curve at the MJTE edge. Accordingly, Fig. 2-6 (b) shows the high field of almost 3MV/cm at the edge of 2-step MJTE, which indicates there is no too much room for improvement for 2-step MJTE with high blocking capability by tuning the etching depth. However, the surface filed and leakage current, while reduced, are not particularly well controlled for 2-step MJTE with less than 0.1 μm safe window in the actual process to have over 80% ideal breakdown voltage as shown in Fig. 2-5

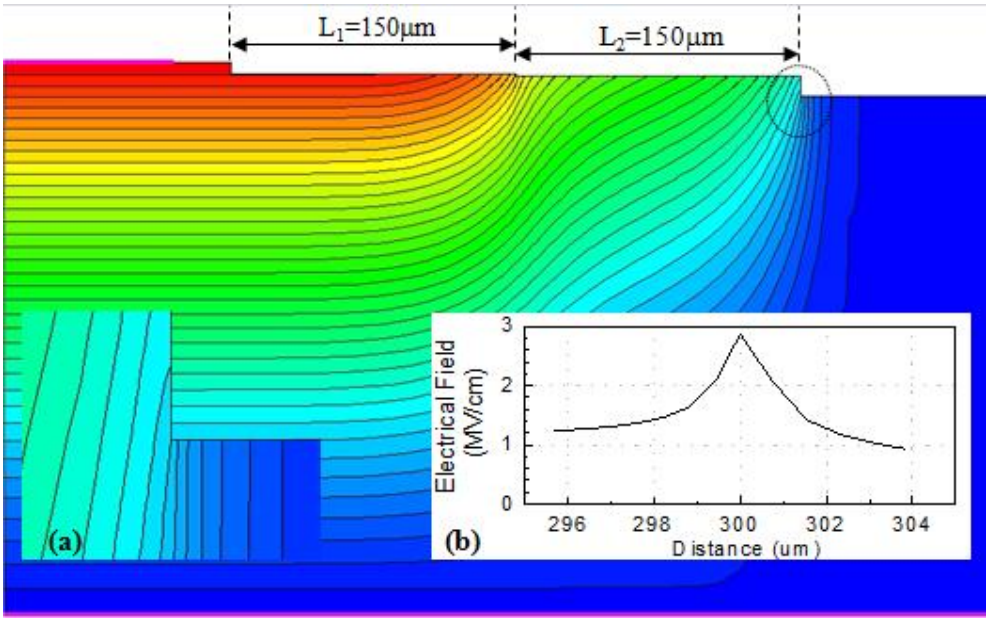


Fig. 2-6 Simulated equipotential lines (pitch: 200V) for 2-step MJTE with d_1 = 1.4 μm and d_2 = 0.14 μm. Insert (a) and (b) are details and field distribution at the encircled region.

- 3-step JTEs

The 2-step MJTE design can't offer enough room in actual fabrication. Hence, it is necessary to develop 3-step MJTE to increase process windows, especially for JTE1 etching depth d_1. Table 2-1 lists the key parameters for MJTE design:

Table 2-1 Key parameters for MJTE design

Step	Length	Depth
1-step	$L_1 = 300$ μm	d_1; $d_2 = d_3 = 0$ μm
2-step	$L_1 = L_2 = 150$ μm	d_1; d_2; $d_3 = 0$ μm
3-step	$L_1 = L_2 = L_3 = 100$ μm	d_1; d_2; d_3

Fig. 2-7 shows the simulated breakdown voltage of the NPN structure with 3-step MJTE as the function of extents on etching depth d_1 for different etching depths of d_2 and d_3, and indicates that the broad MJTE etching depth d_1 window can be achieved by increasing the value of d_2 and d_3. For $d_2 = d_3 = 0.08$ μm, the breakdown voltage increases, and reaches the maximum value of 8.2 kV (97% of ideal value) at $d_{JTE1} = 0.42$ um, then decreases sharply with increasing JTE1 thickness d_{JTE1} ($d_{JTE1} = d_{MJTE}-d_1$). The narrow optimum MJTE depth window makes a big obstacle in the real devices fabrication, since it is difficult to shoot this peak point. Although the etching depth can be precisely controlled, the dopant profile is not totally constant through the epitaxial n-layer. In addition, the electric field distribution in the MJTE region can be perturbed by the fixed charge near the SiC surface as well as inside the passivation layer, which can vary across the wafer. This can result in a variation of the breakdown voltage across the wafer. So the more than 0.8 μm etching depth of d_2 and d_3 have been simulated and the optimum

window of etching depth d_1 has be extended. In the case of $d_2 = d_3 = 0.14$ μm, the range of the optimum etching depth is from 1.26 μm to 1.46 m with the breakdown voltage of over 80% of the ideal value, as shown by full stars in Fig. 2-7.

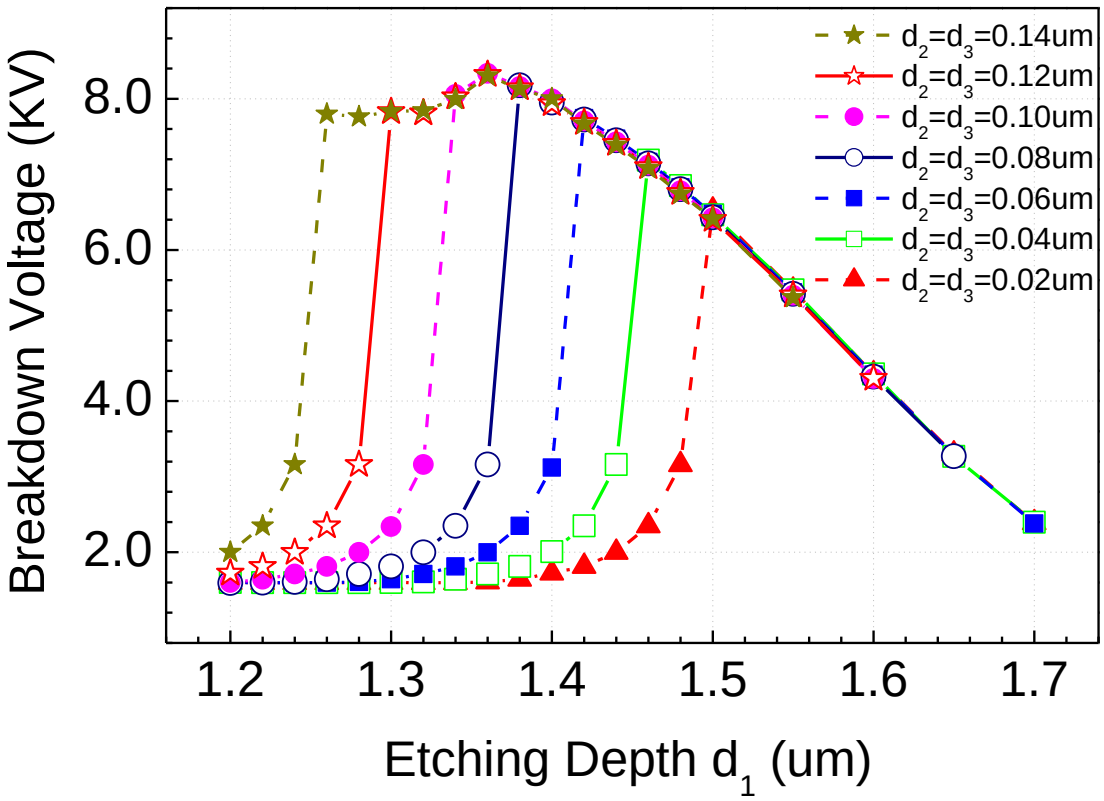


Fig. 2-7 MJTE breakdown voltage as a function of extents on etching depth d_1 with various d_2 and d_3.

In the MJTE design with $d_2 = d_3 = 0.14$ μm, the optimum range of d_1 can be about 0.2 μm with the breakdown voltage of over 80% of the ideal value, which is achievable in actual device fabrication. In order to exactly locate the range of the JTE1 etching depth, d_1 was simulated from $d_1 = 1.1$ μm to 1.7 μm while keeping $d_2 = d_3 = 0.14$ μm. It is clearly seen in Fig. 2-8 that the breakdown voltage increases, reaches a maximum, and then decreases as the JTE1 etching depth d_1 is increased. The highest breakdown voltage

is 8.3 kV, which is from the design of d_1 = 1.36 μm and $d_2 = d_3$ = 0.14 μm. Table 2-2 lists the maximum breakdown voltage and the percent of ideal breakdown voltage of 8.4 kV for the MJTE design with d_1 increasing from 1.2 μm to 1.6 μm and $d_2 = d_3$ = 0.14 μm.

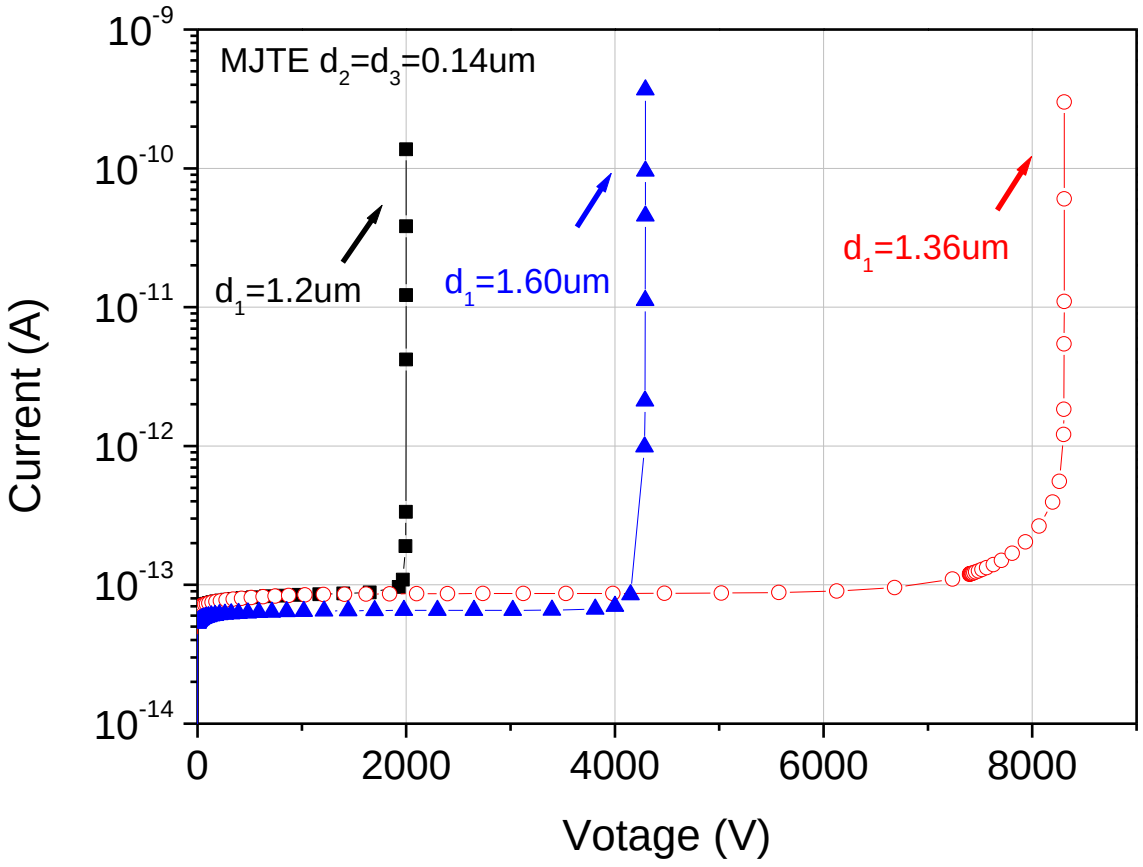


Fig. 2-8 MJTE determination simulation on the NPN structure at $d_2 = d_3$ = 0.14 μm.

Table 2-2 Breakdown voltage and the percent of the ideal breakdown voltage for MJTE design with $d_2 = d_3$ = 0.14 μm

d_1 (μ m)	1.20	1.25	1.30	2.35	1.40	1.45	1.50	1.55	1.60
BV (kV)	1.7	7.6	7.9	8.2	8.0	7.3	6.4	5.3	4.2
% of ideal BV	20	91	94	98	95	86	76	64	50

2.3.2 Equipotential Lines

For the case of $d_2 = d_3 = 0.14$ μm, the breakdown voltage is less than 50% of the ideal value at $d_1 = 1.6$ μm with $d_{JTE1} = 0.2$ μm, which is a relatively thin MJTE layer compared to $d_1 = 1.2$ μm with $d_{JTE1} = 0.6$ μm. The thin MJTE region completely depletes at the low reverse voltage, and the equipotential lines severely curve at the corner of main junction at point ① in Fig. 2-9 (a) at which the electric field crowding takes places, hence leads to a premature breakdown.

On the other hand, the thick MJTE layer makes difficult to deplete even in the outmost step of MJTE at high reverse voltages and hence the potential lines are concentrated at the outmost edge of the MJTE region for $d_1 = 1.2$ μm as shown at point ② in Fig. 2-9 (c). The electric field crowding is at the outmost edge of the MJTE that involves the device to reach prematurely the blocking voltage, too.

For maximum effectiveness, the charge in the MJTE layer is typically designed by etching depth control so that at the desired blocking voltage, the dopants in the MJTE layer are fully depleted and act as a high resistivity layer in which support the high surface and bulk fields. In the case, the maximum breakdown voltage of 8.3 kV is revealed in the MJTE structure of $d_1 = 1.36$ μm, $d_2 = d_3 = 0.14$ μm, approaching 100% of the ideal parallel-plane breakdown voltage. Fig. 2-9(b) indicates the high efficiency of MJTE in spreading the equipotential lines near the edge of the junction at 8.3 kV reverse bias.

Table 2-3 Relation between d_1 and d_{JTE1} at $d_2 = d_3 = 0.14$ μm

d_1 (μ m)	1.20	1.36	1.60
d_{JTE1}(μ m) = d_{MJTE}- d_1	0.60	0.44	0.20

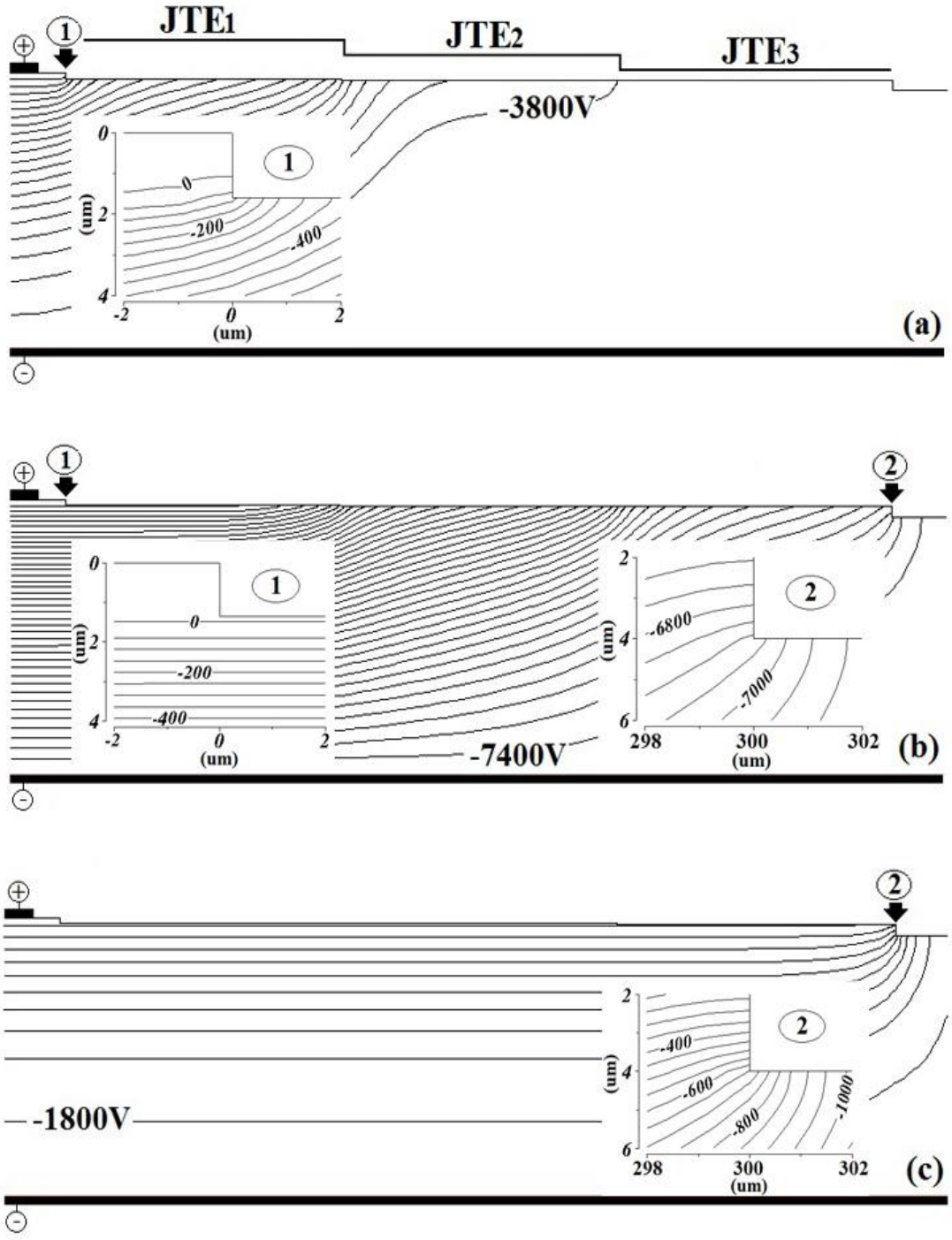


Fig. 2-9 Simulated equipotential lines (pitch: 200V) at 90% breakdown voltage for 3-step MJTE NPN structures with $d_2 = d_3 = 0.14$ μm and (a) $d_1 = 1.2$ μm; (b) $d_1 = 1.36$ μm and (c) $d_1 = 1.6$ μm. Inserts are detail at ① and ②.

2.3.3 Electric Field

The successful application of the solid state technology to power control required the development of GTOs capable of operating at a high voltage. It is apparent that it is necessary to design edge terminations which promote the bulk breakdown. 3-step MJTE has been designed and simulated in the previous sections. For a non-optimum design, equipotential lines were curved at the corner of the main junction or at the outmost edge of the MJTE region, at which the electric field crowding takes place. The high surface field in high voltage 4H-SiC devices can lead to the excess leakage and a premature breakdown at the surface of the devices.

Fig. 2-10 shows the electric field distribution observed vertically from points of ① at X = 0 μm and ② at X = 300 μm in Fig.2.9, respectively. The optimum design with d_1 = 1.36 μm and $d_2 = d_3$ = 0.14 μm can independently control both the peak bulk field and the peak edge field. Compared with the d_1 = 1.6 μm design, the optimum designed 3-step MJTE effectively suppress the peak electric field at the main junction edge from 3 MV/cm to 1 MV/cm, which is about 60% of the value of the peak bulk electric field on the optimum design as shown in Fig. 2-10 (a). Hence, the breakdown voltage can be increased by about 100% from 4.3 kV at d_1 = 1.6 μm to 8.3 kV at d_1 = 1.6 μm.

In contrast to the d_1 = 1.2 μm design, as shown in Fig. 2-10 (b), the optimum design provides a balanced electric-field at both the inner and outer edges of the 3-step MJTE and significantly reduces the peak electric field at the outmost edge of MJTE by 40%, where JTE_3 is fully depleted prior to the designed breakdown, moving the peak field into the junction of JTE_2 and JTE_3 and then the junction of JTE_1 and JTE_2, thereby reducing the overall peak surface field and resulting in nearly the ideal breakdown voltage.

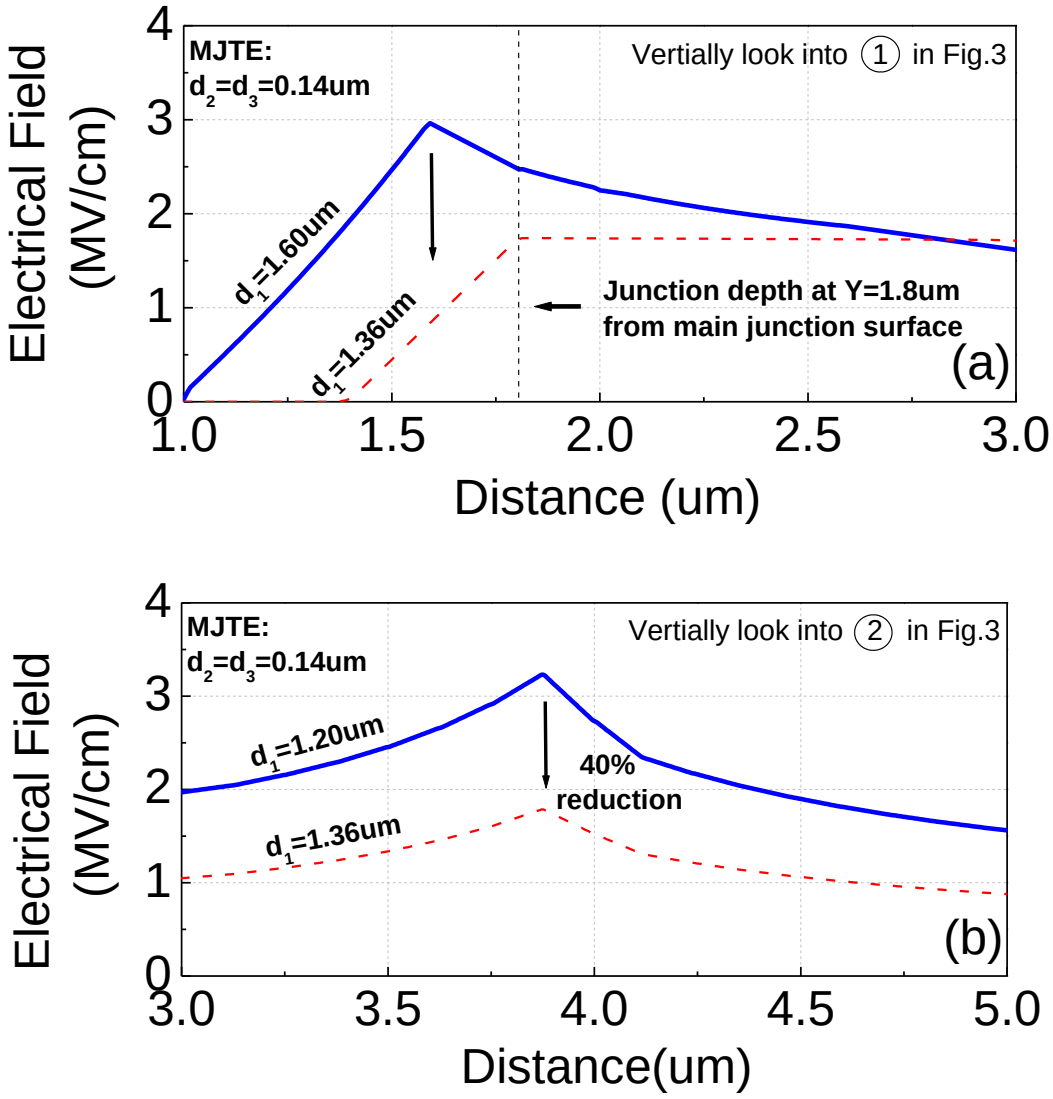


Fig. 2-10 The electrical field is observed vertically (a) along the main junction edge at X = 0 μm and (b) along the outmost edge of MJTE at X = 300 μm.

2.4 Mask Layout for the NPN Structure

The 3-step MJTE test cells were designed as single-mesa concentric circular NPN structures. There are 4 layer masks for MJTE test cell fabrication, including ISOLATION mask, JTE1 mask, JTE2 mask and JTE3 mask. Detailed fabrication steps will be introduced in the next section.

There are two types of 3-step MJTE cells. Both type cells have the same innermost JTE diameter of 200 μm. The small cell has 50 μm JTE step length and 500 μm outer diameter; the large one has 100 μm JTE step length and 800 μm outer diameter cell. Fig. 2-11 shows one group of the circular NPN structures. Large cells are designed at the outside two rows and small ones are drawn at the central two rows. Detailed dimension for a single cell is illustrated in Fig. 2-12. Correspondingly, the cross sectional diagram of the circular structures is demonstrated at the bottom part of Fig. 2-12.

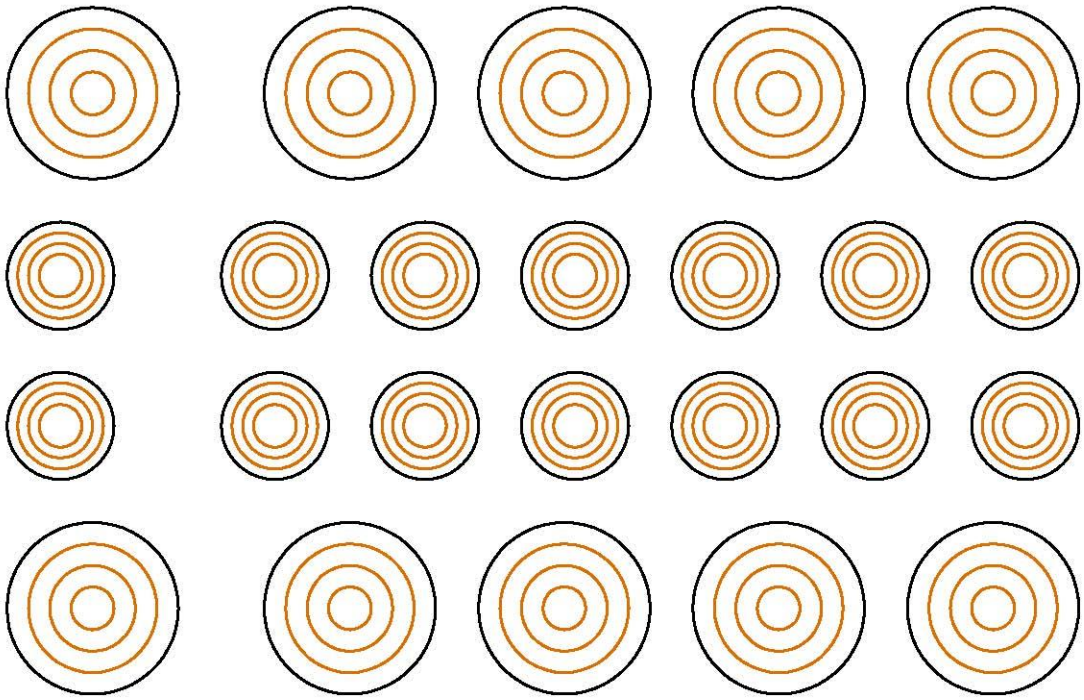


Fig. 2-11 A group of JTE testing concentric circular NPN structures. The innermost JTE diameter is 200 μm. The length of a JTE step is 50 μm for smaller cells and 100 μm for larger cells. The outmost blue rings on each cell are isolation mask layer

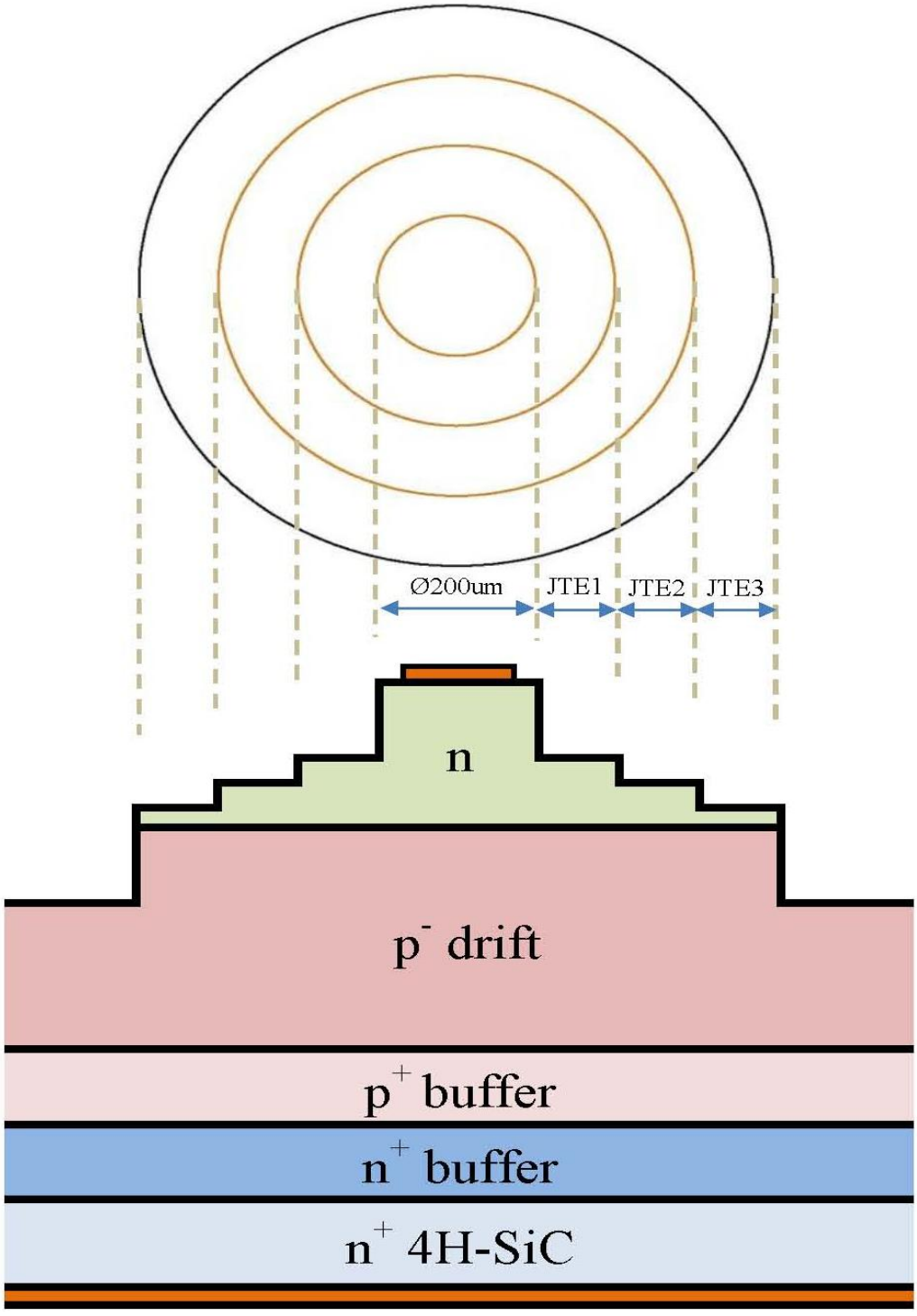


Fig. 2-12 Top and cross-sectional view of a circular NPN structure with MJTE. For small cell, $JTE_1 = JTE_2 = JTE_3 = 50$ μm; For large cell $JTE_1 = JTE_2 = JTE_3 = 100$ μm.

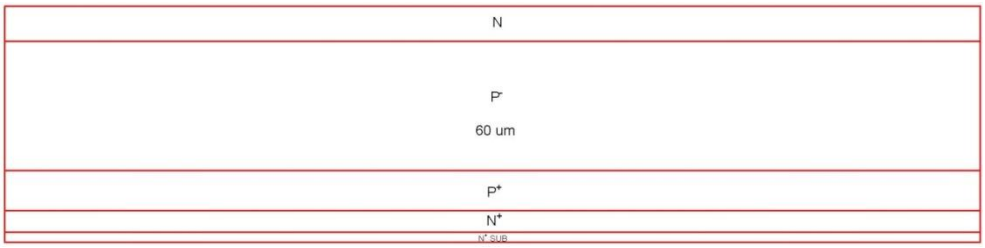
2.5 Fabrication of the NPN Structure with MJTE

Based on the above simulation results, the mask layout for the NPN structure with 3-step JTE has been designed. The total MJTE length is 300 μm with 100 μm or 150 μm with 50 μm for each step length, as shown in Fig. 2-12. All of the 4H-SiC samples used in the current experiments have been cut from the same N- type 4H-SiC substrate with 60μm P- drift layer of 9x1014cm-3 doping, which has been designed for GTO devices and purchased from Cree, Inc. $N_{MJTE} = 2.3 \times 10^{17}\ cm^{-3}$ has been selected as the target of the doping concentration for the MJTE layer. The MJTE region has to be thinned down by dry etching in order to achieve the charge balance that will yield the desired field suppression at the device periphery. First, the outer two steps have been etched with $d_2 = d_3 = 0.14$ μm. Next, the innermost step depth d_1 was gradually increased by repeated Inductively Coupled Plasma (ICP) etching in CF4+O2 plasma, while the reserve I-V characteristics have been monitored at every etching run.

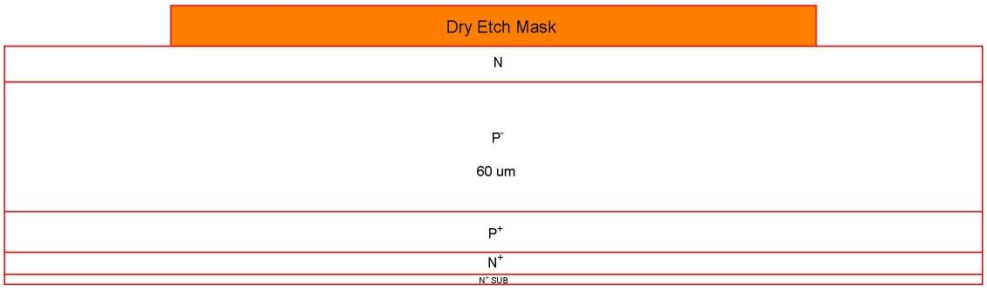
The major fabrication steps for the NPN structure with MJTE are as follows (Fig. 2-13):

- Wafer cutting and cleaning (Fig. 2-13 (a))
- Lithography, metal Sputtering and wet etching for isolation dry etch mask formation (Fig. 2-13 (b))
- ICP dry etch to form isolation mesa of the NPN structure (Fig. 2-13 (c))
- Lithography, metal Sputtering and wet etching for JTE3 dry etch mask formation (Fig. 2-13 (d))
- ICP dry etch to form JTE3 of the NPN structure (Fig. 2-13 (e))

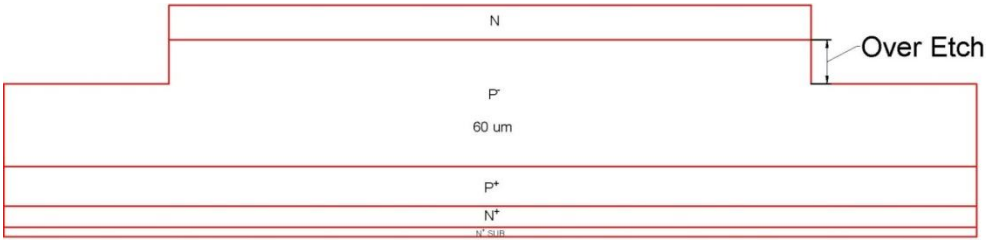
- Lithography, metal Sputtering and wet etching for JTE2 dry etch mask formation (Fig. 2-13 (f))
- ICP dry etch to form JTE2 of the NPN structure (Fig. 2-13 (g))
- Lithography, metal Sputtering and wet etching for JTE1 dry etch mask formation (Fig. 2-13 (h))
- ICP dry etch to form JTE1 of the NPN structure (Fig. 2-13 (i))



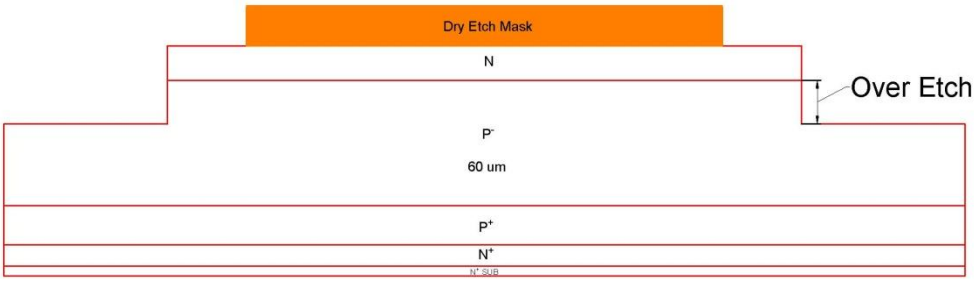
(a) Wafer cutting and cleaning



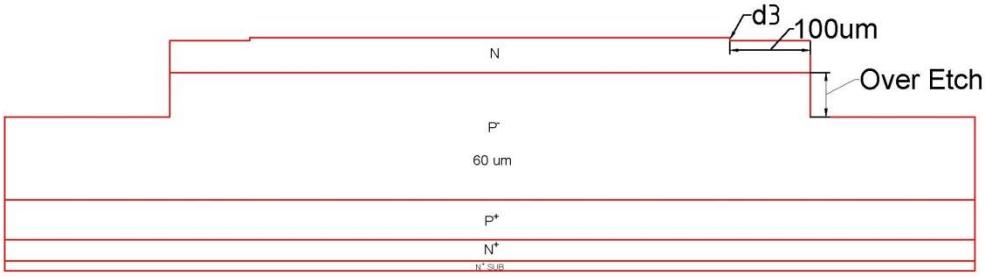
(b) Dry etch mask formation for Isolation



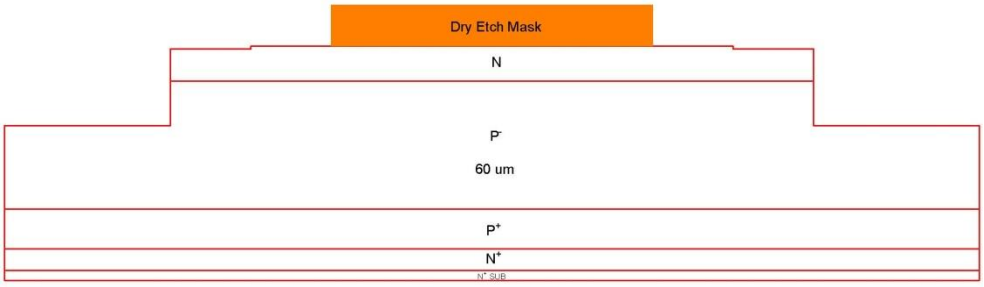
(c) Isolation mesa of NPN structure formation



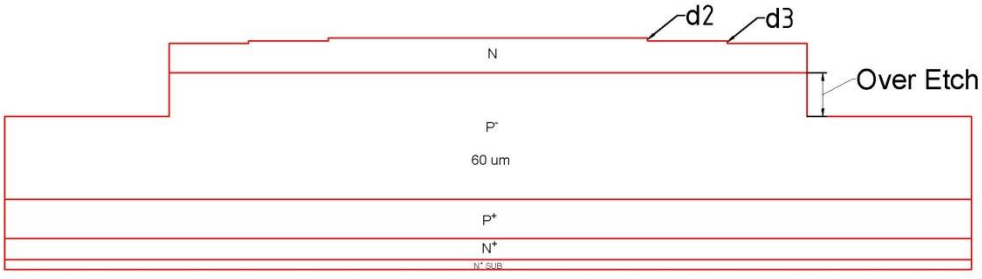
(d) Dry etch mask formation for JTE3



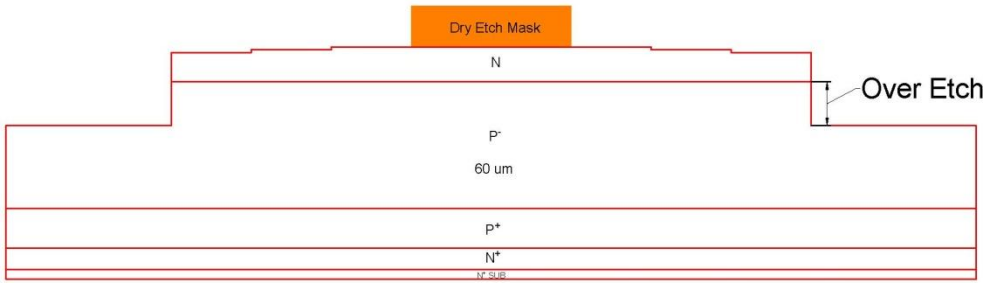
(e) JTE3 of NPN structure formation



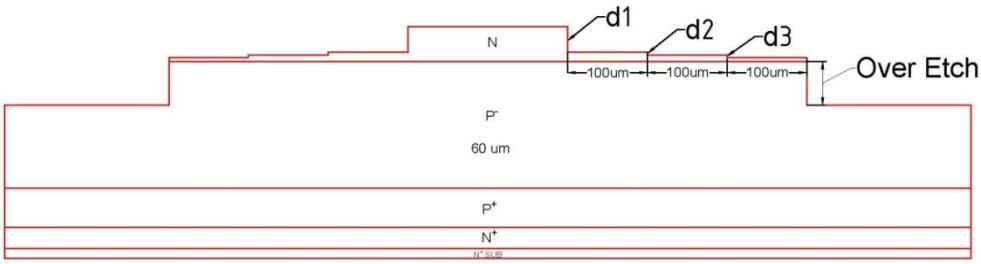
(f) Dry etch mask formation for JTE2



(g) JTE2 of NPN structure formation



(h) Dry etch mask formation for JTE1



(i) JTE1 of NPN structure formation

Fig. 2-13 (a)-(i): Fabrication steps of MJTE with the NPN structure.

2.6 MJTE Optimization

The MJTE structure has been optimized on a separate test samples. The MJTE structure has three stages, including JTE1, JTE2 and JTE3, each stage 100 μm wide. The depths of outer two JTE stages were 0.14um each. The depth of the innermost step has been gradually increased by repeated ICP etching while the reversed I-V characteristics have been monitored at every etching run. The results are shown in Fig. 2-14. The optimum blocking voltage/reverse leakage corresponded to about 1.3 μm etching depth for innermost JTE step. For MJTE steps etching were done with AlTi etching masks of 6000 Å in thickness patterned by photolithography and standard Al etchant.

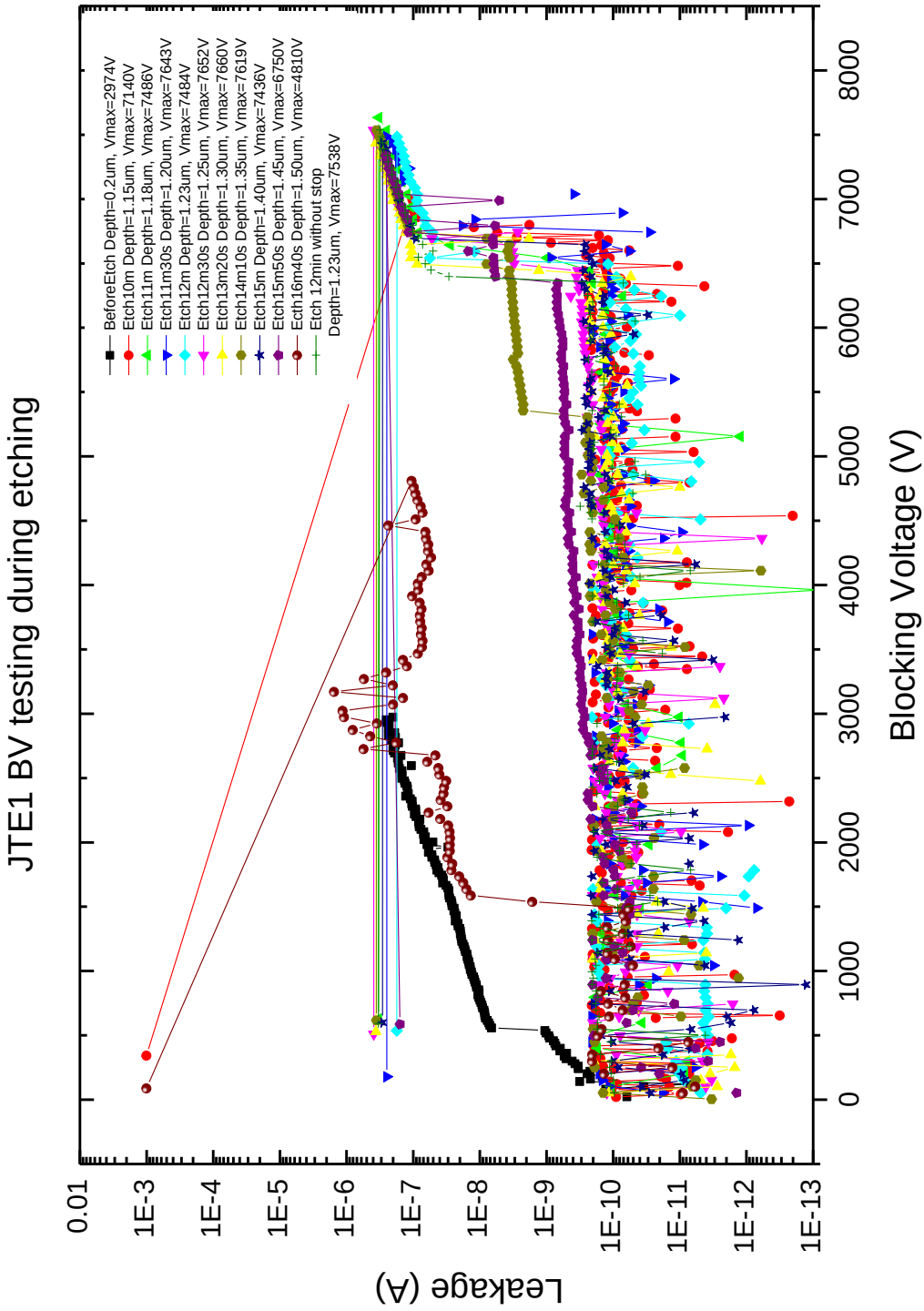


Fig. 2-14 Reverse I-V characteristics of NPN structure with 3-step MJTE measured at different stages of the JTE determination process.

Fig. 2-15 represents the dependence of the experimental normalized breakdown voltage on the etching depth d_1, measured at room temperature. Open circles denote the experimental results for 3-step MJTE with $d_2 = d_3 = 0.14$ μm. The maximum blocking voltage of 7630 V is obtained, which approaches 90% of the breakdown voltage of the corresponding ideal parallel-plane junction. The result of experiment indicates that the depth of d_1 has a broad window from 1.15 μm to 1.45 μm with breakdown voltage over 7 kV (more than 80% of the ideal breakdown voltage), which means the design of 3-step MJTE has enough tolerant window for actual devices fabrication.

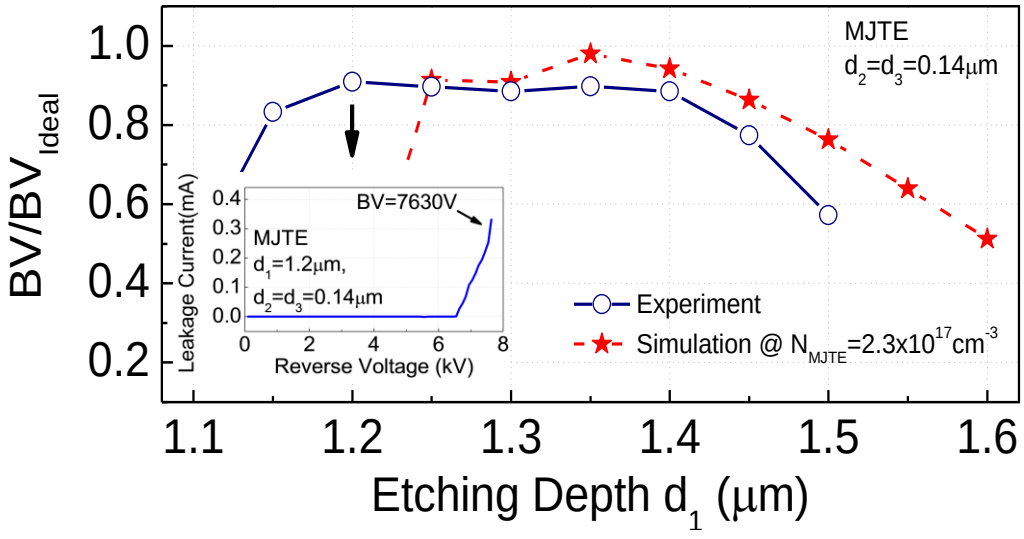


Fig. 2-15 Simulated and experimental normalized breakdown voltage as a function of extents on etching depth d_1. The ideal breakdown voltage is 8.4 kV.

The simulated results are also plotted in the same figure. The experimental results showed a good agreement with the simulated results. The difference between the simulated results and experimental results may be due to the facts that the actual doping

concentration of the blocking layer is different from its specification value and the actual MJTE implantation profile is different from the doping profile used in the simulations.

2.7 Summary

Using 2-D numerical simulations, 3-step MJTE techniques for 4H-SiC power devices have been investigated. Compared with 1- and 2-step MJTE, the 3-step MJTE design can improve the blocking performance, balance electric-field, and decrease the sensitivity of the breakdown voltage to JTE etching depth while keeping the total JTE length constant. The simulation results were confirmed by the fabrication of 3-step JTE NPN structure with the maximum blocking voltage of 7630V, which is 90% of the ideal breakdown voltage. The design methodologies discussed in this study are believed to be useful in designing the edge terminations structures for other range of the breakdown voltage.

CHAPTER 3 DESIGN OF 4H-SiC GTOs

High power systems require robust power switches to operate at high temperatures to meet the demand for smaller and higher power density systems. 4H–SiC has unique material properties that enable it to be far superior to silicon (Si). Benefits of 4H–SiC compared to Si include three times wider band gap (3.2 eV), ten times higher critical field ($3.0x10^6$ V/cm), and three times higher thermal conductivity (4.9 W/cm K) [3,4]. Compared to other devices made on SiC, such as BJTs, JFETs, MOSFETs, and IGBTs, SiC GTOs are the favorable devices for pulsed power applications due to their ability to operate at high current and high voltage levels, which is attributed to conductivity modulation in the drift layer of the device. Furthermore, SiC GTOs offer several advantages over Si thyristors and Si GTOs such as compactness, higher current density, faster switching, and higher temperature operation.

The considerable improvement of materials quality and the refinement of fabrication process resulted in the remarkable increase in the blocking voltage of SiC GTOs from below 1 kV to over 10 kV [26, 38, 39, 40]. For a current density of 500 A/cm^2, the GTO (fabricated at Rutgers University) shows a forward on-state voltage of 5.74 V at the room temperature. The GTOs have also demonstrated fast switching and high current capability. In addition to the blocking voltage, total current, and switching time, the on-state voltage drop V_F and the current density that can be turned off are two of the important parameters characterizing the performance of GTOs. In this chapter, the design of more than 6 kV 4H-SiC GTOs will be presented, which includes the 4H-SiC GTO structure design, simulation of static and dynamic characteristics. The GTO mask design will be considered in the last part of this chapter.

3.1 Design of the GTO Structure

Fig. 3-1 shows the NPNP device structure grown on an n+ 4H-SiC substrate. As a result, unlike silicon GTOs, the SiC GTOs have the anode on the top and the cathode on the bottom. All the epilayers were grown in a single run and designed for a high turn-on gain. The device has an asymmetrical structure with the blocking in the forward direction only. A fine pitch design is used to facilitate high di/dt and dv/dt performances required for pulsed power applications.

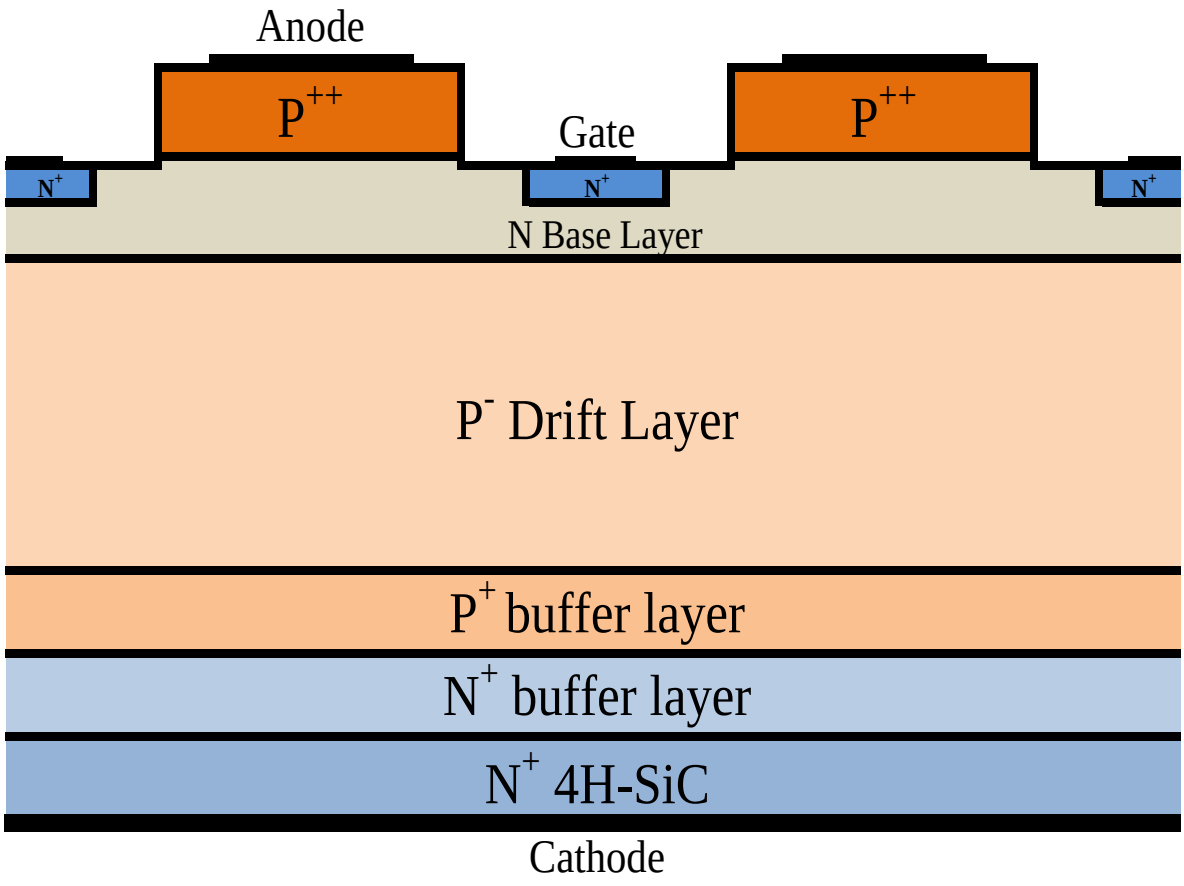


Fig. 3-1 Cross-sectional view of 60 μm the 4H-SiC GTO structure

A 60 μm thick, lightly doped ($N_A = 9x10^{14}$ cm^{-3}) P-base layer is used to achieve high blocking voltage (more than 6 kV). The GTOs are terminated by a three-zone, N-type junction Termination Extension (JTE). Fabrication details on MJTE have been introduced in the previous chapter. The control gate was formed on the n-based layer, and anode and cathode were formed on the p^{++} top layer and n^+ substrate, respectively.

The top p^{++} layer should be doped as high as possible (> $1x10^{19}$ cm^{-3}), so as to increase the emitter efficiency of the pnp transistor as well as the ohmic contact quality. The thickness can't be too thin. Otherwise the contact metal might spike through to the beneath n layer and cause a problem. A 2 μm thick p^+ layer is chosen here. Increasing the p^{++} layer thickness further only increases the series resistance and is not good.

The n-base layer thickness and doping concentration have to be in the right range. If the thickness is too large or the doping concentration is too high, the emitter efficiency (or current gain) is low and it might be difficult for the GTO to turn on. If the thickness is too small or the doping concentration is too low, the depletion region might punch trough to the top p^+ layer when the device is working in the forward blocking state, and the GTO forward blocking capability is reduces. The thickness and doping concentration are chosen here to be 2 μm and doping concentration of $2.3x10^{17}$ cm^{-3}, respectively. We will see in the later sections that this choice is experimentally proven to be appropriate.

The doping and thickness of the drift layer are determined by the device blocking voltage. For 4H-SiC, the dependence of the critical field on the doping concentration can be described as Eq. 3-1 [42]. The dependence of the critical field on the doping concentration is shown in Fig. 3-2.

$$E_{cr} = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log_{10}(\frac{p_{drift}}{10^{16}})} \quad \text{Eq. 3-1}$$

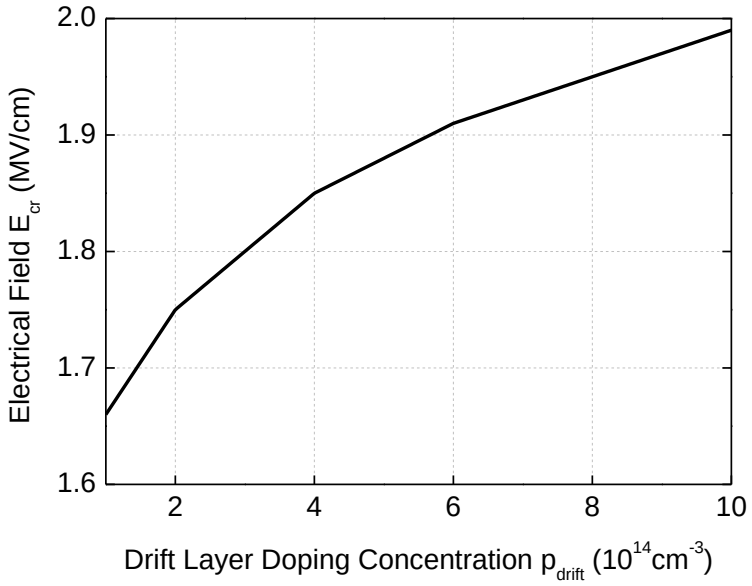


Fig. 3-2 Dependence of the critical field on the drift layer doping concentration

Ignoring the effect of the current spreading layer on the breakdown voltage, the breakdown voltage V_{PT} determined by the critical field and the drift layer doping concentration is obtained as in Eq. 3-2 [12]:

$$BV_d = \frac{E_{cr} W_d}{2}\left(\frac{2W_{cr} - W_d}{W_{cr}}\right) \quad \text{Eq. 3-2}$$

where W_d is the drift layer thickness; W_{cr} is the depletion width at the critical field with uniform doping p_{drift}, which is given by

$$W_{cr} = \frac{\varepsilon_0 \varepsilon_{SiC} E_{cr}}{q p_{drift}} \qquad \text{Eq. 3-3}$$

The dependence of the breakdown voltage on the drift layer doping concentration is obtained from Eq. 3-5 and Eq. 3-2 as shown in Fig. 3-3. It indicates that for more than 8 kV GTOs, the drift layer should be doped as low as $p_{drift} < 1.2 \times 10^{15}$ cm^{-3}. A 60 μm thick, lightly doped (N_A=9x10^{14} cm^{-3}) P-base layer was selected for more than 6 kV GTOs.

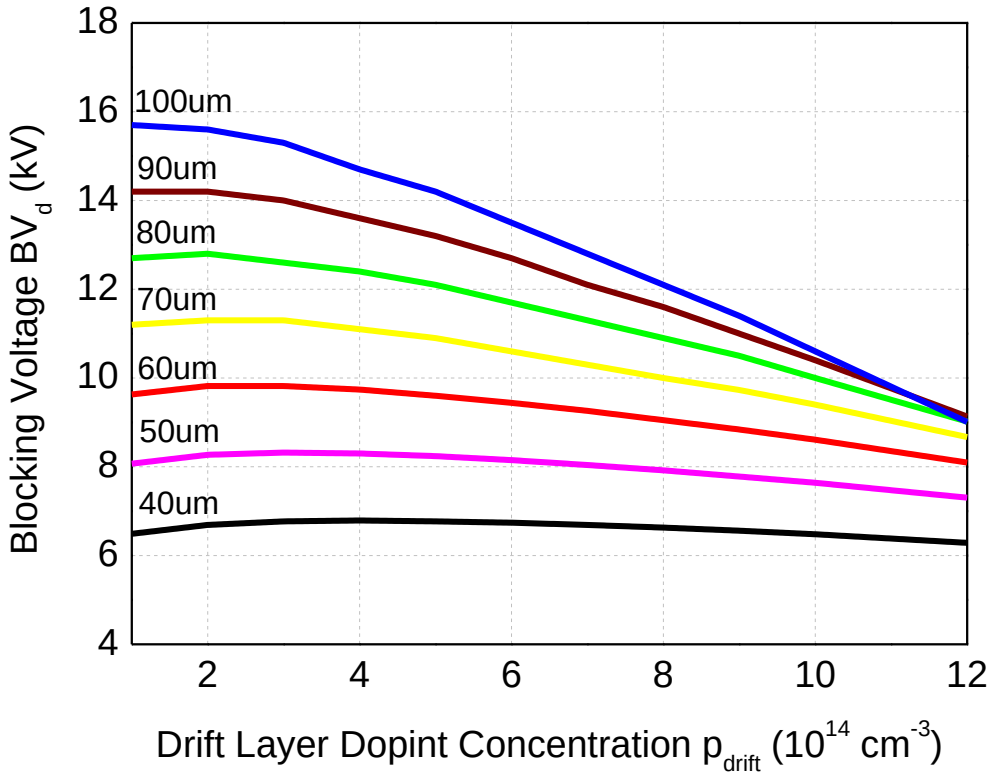


Fig. 3-3 Dependence of the critical field on the drift layer doping concentration

The p buffer layer used to make electric field profile in the blocking layer more uniform and the thyristor blocking voltage can be increased. The difference between

GTO structures with/without a p buffer layer is shown in Fig. 3-4. For the structure shown in Fig. 3-4 (b) to have the highest blocking voltage for a given blocking layer thickness, d_{drift} the blocking layer doping concentration, p_{drft}, has to be chosen to make the electric field at the blocking junction close to the critical field E_{cr} and at the same time let the depletion region reaches the n^+ substrate. The blocking voltage is then roughly equals to [41]:

$$V_B = \frac{1}{2} \times d_{drift} \times E_C \qquad \text{Eq. 3-4}$$

For 4H-SiC the critical field dependence on the doping concentration is described by Eq. 3-1 [42]. For the structure shown in Fig. 3-4 (a), with the p buffer layer, the optimal design is somehow different. Here, the doping concentration of the blocking layer should be lower than that of Fig. 3-4 (b), so as to make the field distribution more uniform. The blocking voltage is given by [43]:

$$V_B = \frac{1}{2} \times (E_C + E_1) \times d_{drift} \qquad \text{Eq. 3-5}$$

E_1 can be close to E_c. The blocking voltage of the structure with the p buffer also makes the GTO turn-off easier and turn-on more difficult, since it decreases the gain of the npn transistor. Hence a trade-off has to be made here and the thickness and doping concentration of the buffer layer have to be also in the right range. The p buffer epilayer was designed to have a thickness of 2 μm and doping concentration of $2x10^{17}$ cm^{-3}.

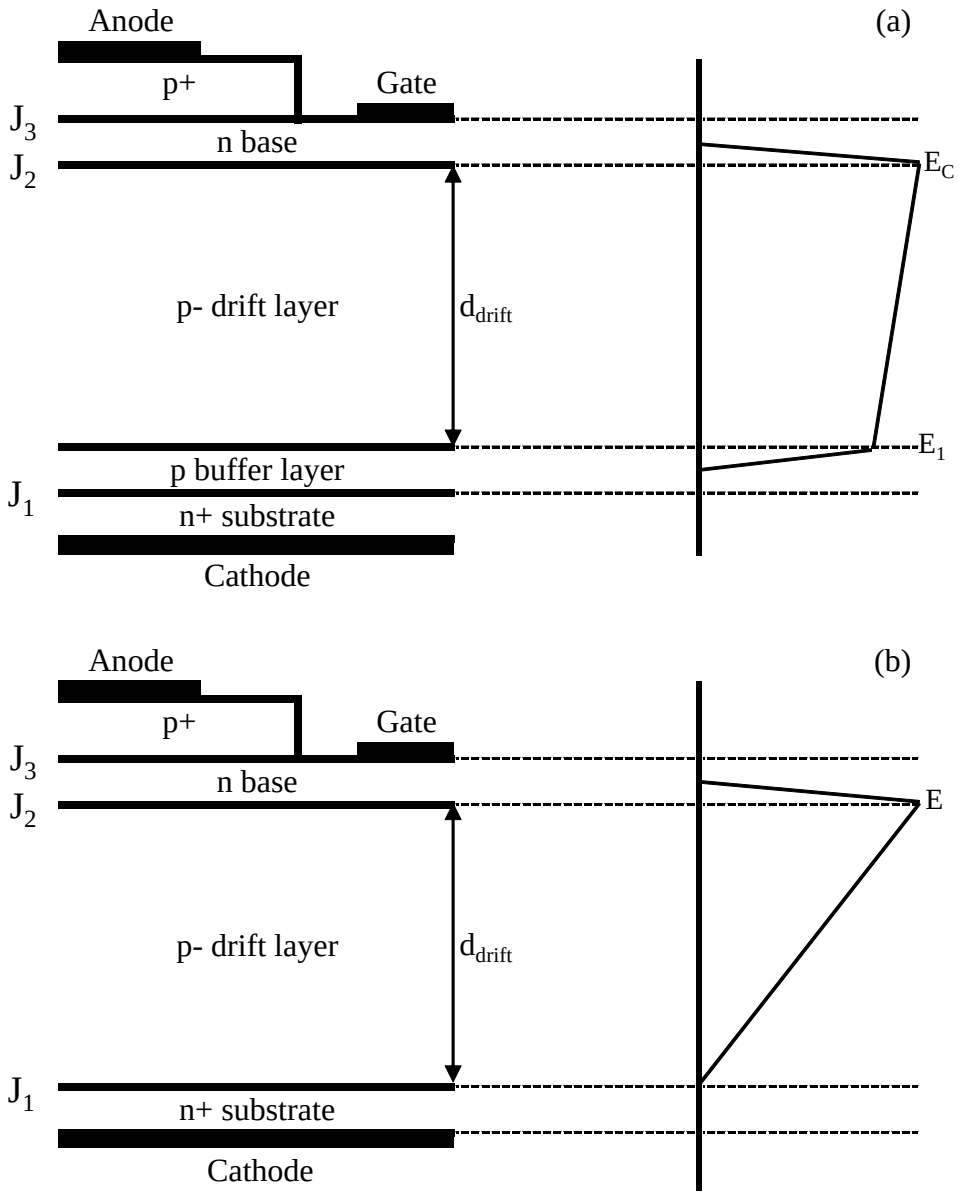


Fig. 3-4 Comparison between two structures: (a) with a p buffer layer, (b) without a buffer layer. The structure (a) can block higher voltage than (b) for the same thickness and doping p-drift layer.

3.2 Simulation of GTO

The designed GTO has been simulated by Synopsys Sentaurus [33]. The simulated structure is shown in Fig. 3-5. Each anode finger has a width of 12.5 μm. The spacing between anode mesa edge and the gate finger is 8 μm and each gate finger has a width of 5 μm.

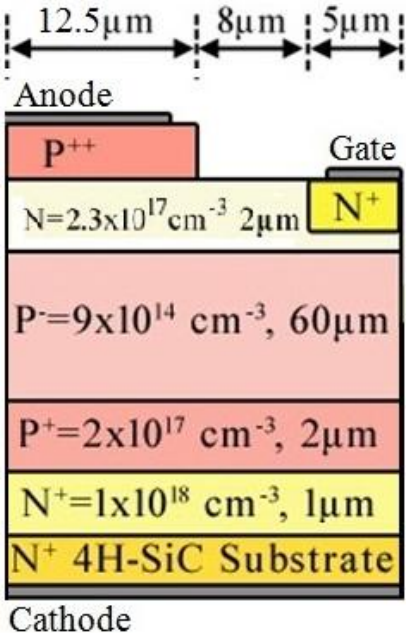
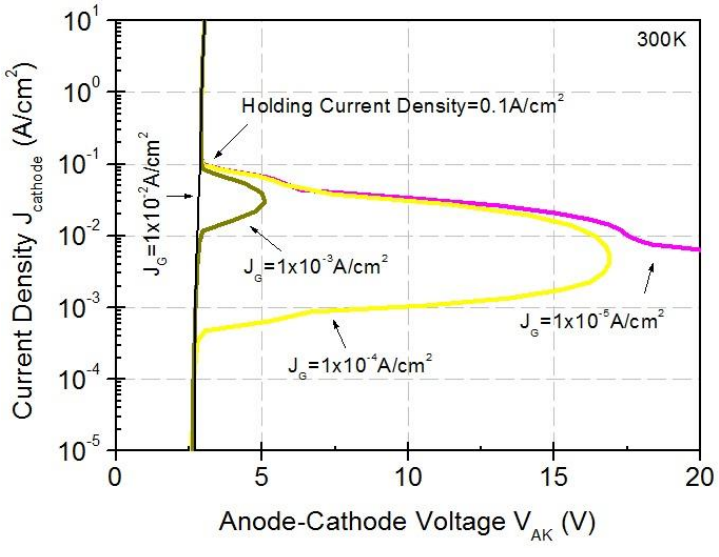


Fig. 3-5 Simulated GTO structure.

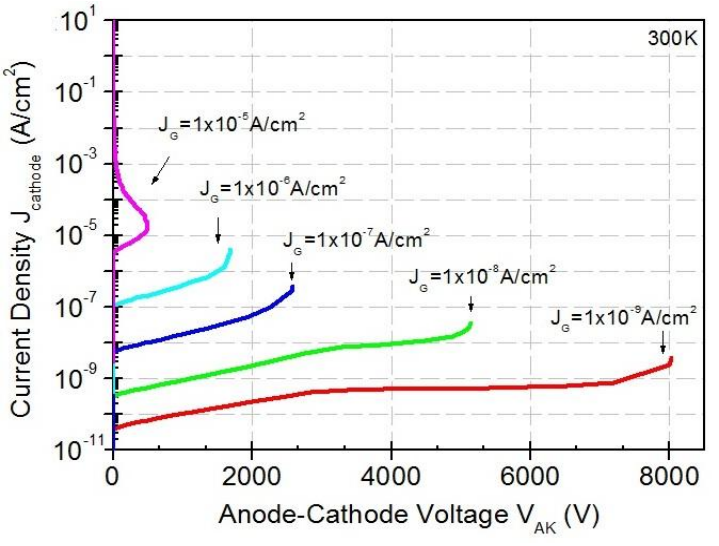
3.2.1 Static Characteristics

Fig. 3-6 shows the influence of the gate current at the room temperature forward I-V characteristics of 8 kV 4H-SiC GTOs with a minority carrier lifetime τ_{no} of 1us. As expected, the forward blocking region shrinks with increase in the gate current. The GTO can block more than 8000 V when the gate current density is $1x10^{-9}$ A/cm^2. When it is blocking around 500 V, a gate current density of approximately $1x10^{-5}$ A/cm^2 is needed to

turn on GTO device. The holding current, which is defined as the current level below which the device is unable to maintain self-sustaining current conduction, is approximately 0.1 A/cm^2. The GTO latches on with no snap back at gate current density of 1x10^{-2} A/cm^2 yielding an operating current density of more than 500 A/cm^2 at the voltage drop of 3.5 V.



(a)



(b)

Fig. 3-6 Blocking characteristics of larger than 6 kV 4H-SiC GTO with a minority carrier lifetime τ_{no} of 1us at room temperature.

3.2.2 Dynamic Characteristics

The simulated switching characteristics of the GTO were analyzed by applying the circuit in Fig. 3-7. A gate pulse generator generates series gate pluses which consist of both negative and positive voltage pulses. The negative voltage pulse with a pulse duration of 0.22 μs is used to turn on the GTO with an anode to cathode bias of 3500 V, whereas the positive voltage pulse of 1.75 μs in duration is used to turn off the device. The interval between these two pulses is 0.28 μs. The inductor is used to limit the di/dt rate. The simulation is done at 300 K. The on-state current is limited by 20 Ω resistance.

Fig. 3-8 shows a set of GTO voltage and current waveforms. These waveforms show the GTO's switching characteristics, such as the turn-on/off delay, turn-on/off time, and voltage drop. These characteristics are important in determining during the actual application.

The GTO can be triggered from the forward-blocking mode to the on-state by the application of a gate drive current. The gate drive current flows from the gate terminal to anode. The voltage drop between P+ anode and N gate due to the gate current flow forward biases the J_3 junction in Fig. 3-7, producing the injection of holes from P+ anode. This does not immediately produce the cathode current flow. The injected holes diffuse through the n-base region in a finite time interval referred to as the delay time t_d. Once the holes cross the N gate/P drift junction J_2 initiated a current flow through the devices. Consequently, the cathode current begins to flow after a delay time interval, which is about 7 ns.

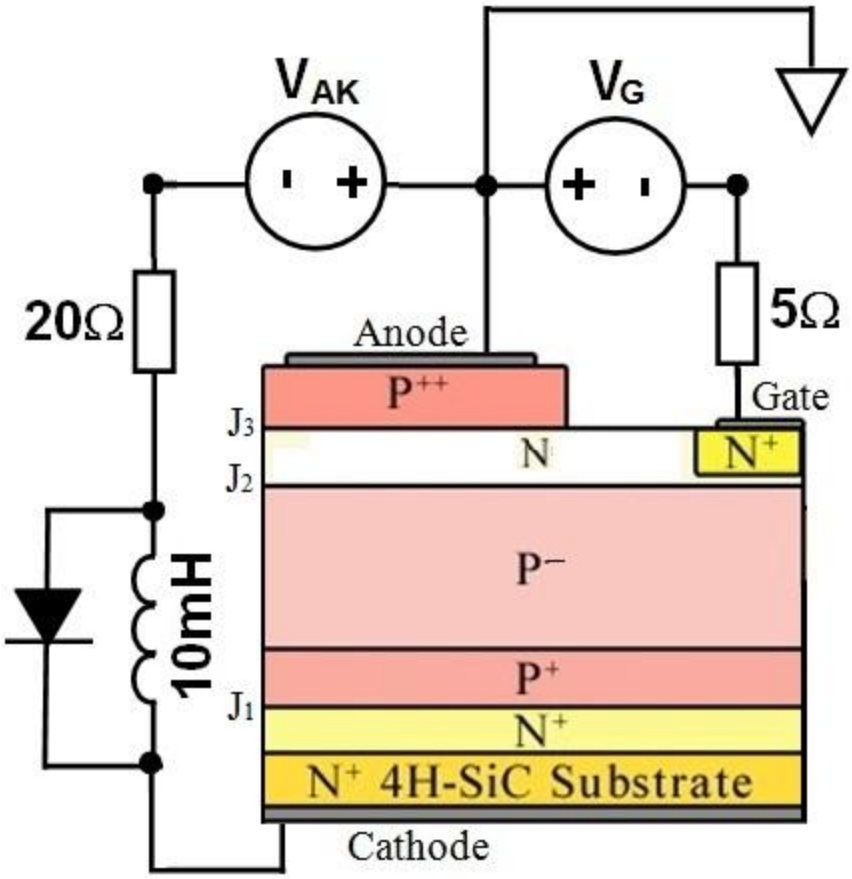


Fig. 3-7 60 μm 4H-SiC GTO switching testing circuit.

During the turn-on process, a high concentration of electrons is injected into the P-drift region from the N+ cathode region and a high concentration of electrons is injected into the P-drift region from P+ cathode region. Those will increase the stored carriers in N-base and P-base region. The cathode current will grow exponentially (as shown in Fig. 3-8) to the on-state value after a rise time t_r, which is about 80 ns. Therefore, the turn-on time at 300 K is $t_{on} = t_d + t_r = 87$ ns.

During the on-state operation, the regenerative coupling between the inherent N-P-N and P-N-P transistors within the GTO produces the current at the N-base/P-drift junction. The collector current for the P-N-P transistor provides the base drive current for the N-P-

N transistor while the collector current for the N-P-N transistor provides the base drive current for the P-N-P transistor. The regeneration action can be disrupted by the application of a reverse gate current that deprives the P-N-P transistor of its base drive current. If a sufficient gate drive current is applied, the regenerative action will be interrupted leading to the turn-off of the GTO.

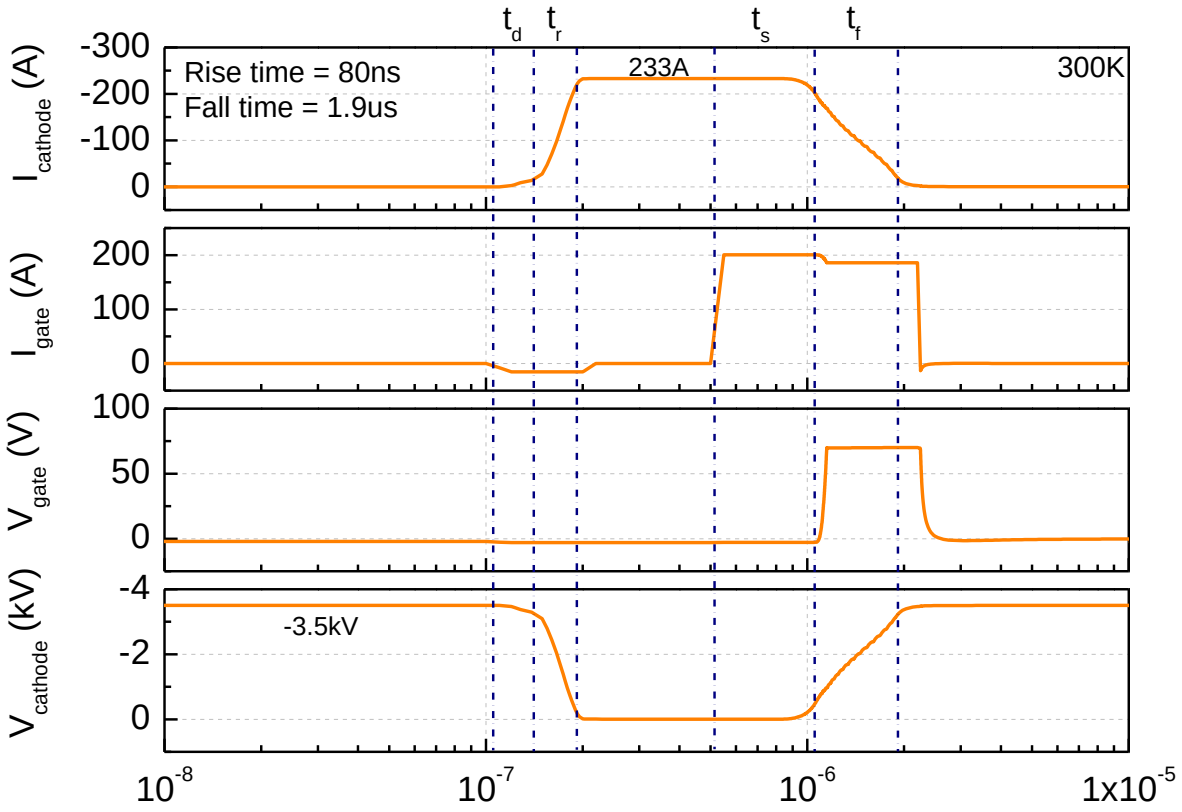


Fig. 3-8 Turn-on and turn-off transients of the 4H-SiC GTO.

The regenerative action in the GTO does not cease right after the application of the reverse gate current until a time interval called the storage time (t_s) has elapsed. The storage time (about 0.5 μs) is determined by the reversed gate current removing all the

stored charged within the N-base region. The storage time can be reduced by decreasing the lifetime and increasing the gate drive current [1].

Once the stored charge in the N-base region has been removed by the reverse gate drive current, the N-base/P-drift junction begins to support voltage across a space-charge region. During the cathode voltage increasing, the stored charge is continuously extracted. The time taken for the cathode voltage to reach -3500 V defined as the fall time t_f, which is 1.9 μs. Hence, the turn-off time is 2.4us ($t_s + t_f$).

3.3 Mask Design

3.3.1 3-inch GTO Mask

The mask set for more than 6kV is designed for the 3-inch wafer process. Fig. 3-9 shows the layout of the mask and a typical wafer position.

The primary-size device in the mask set is 190-finger 5.0mm x 3.0mm GTO (Type A and Type B area). Four groups of 2.2mm x 1.5mm testing GTO cells together with Transfer Length Method (TLM) patterns are embedded among the primary size GTO cells with label a in Fig. 3-9. Four groups of areas with label b in Fig. 3-9 are for MJTE testing diodes, which have been introduced in Chapter 2.

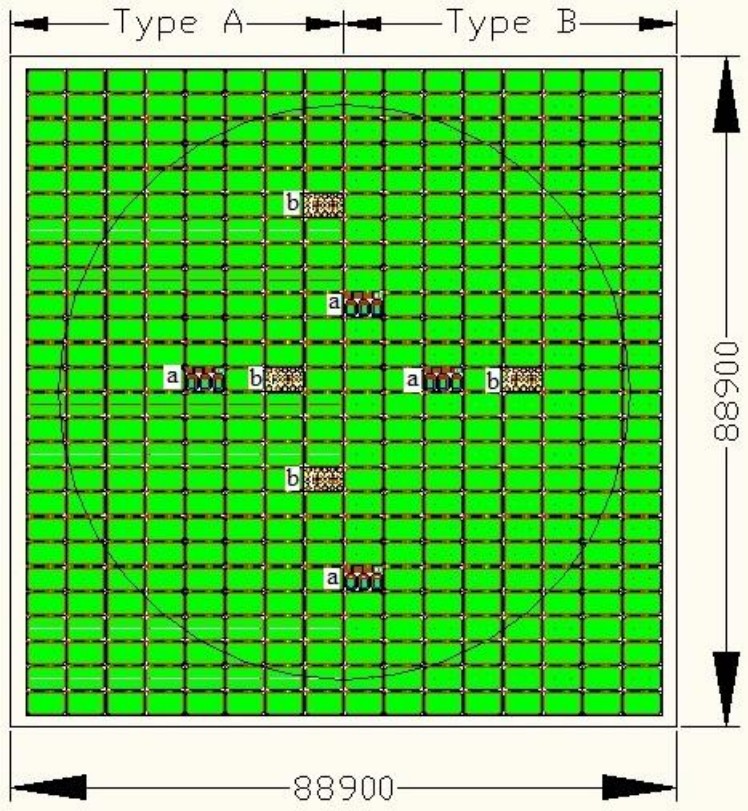


Fig. 3-9 Top view of GTO mask layout (unit: μm)

3.3.2 Interdigitated Design

It has been pointed out that the gate resistance is the key parameter to determine the uniform turn-off of all GTO anode regions simultaneously. Since GTOs handle a huge amount of anode current in the on-state, any non-uniformity in the gate resistance will cause the current crowding in a few anode fingers while the rest of the device turns-off. It is desirable to design GTO cells with identical length and width. With respect to the cell design, either uniform array or interdigitated anode-gate fingers are used in the more than 6 kV GTO mask drawing. An example of such a GTO is shown in Fig. 3-10.

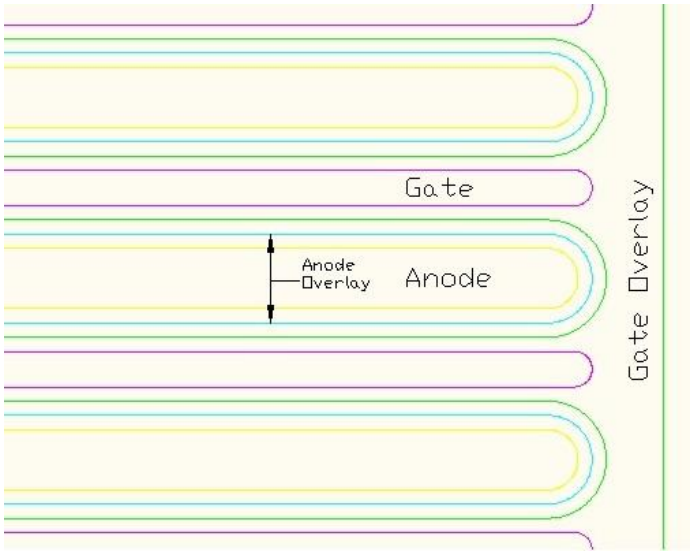


Fig. 3-10 GTO layout with the interdigitated anode and gate fingers.

3.3.3 0.1cm^2 GTO Design

The complete device layout design includes an active area containing a number of anode lines fingers surrounded by a gate region, three-step JTE region, metal overlay for the anode and gate, and finally wire-bond pads. The smallest dimensions designed are the gate width: 10 μm. Fig. 3-11 and Fig. 3-12 show design of different primary-size cells with the active area of 0.1cm^2 realized in the drawing. It is the full interdigitated design, which is expected to give a better device performance for the larger GTO devices. The anode finger is 1032 μm x 17 μm. The gate trench width is 34 μm, with the gate contact finger width of 10 μm. The space between the anode contact and the gate contact is 12 μm. In each primary-size cell, it includes one center gate pad which is sandwiched by two anode pads, which are at the edge of the active area. The probing pads were designed to be used with standard commercially available RF probes. The width of each JTE step is 100 μm, with a total width of 300 μm. The dimensions of the probing and wire-bonding pad were minimized to reduce the parasitic capacitance.

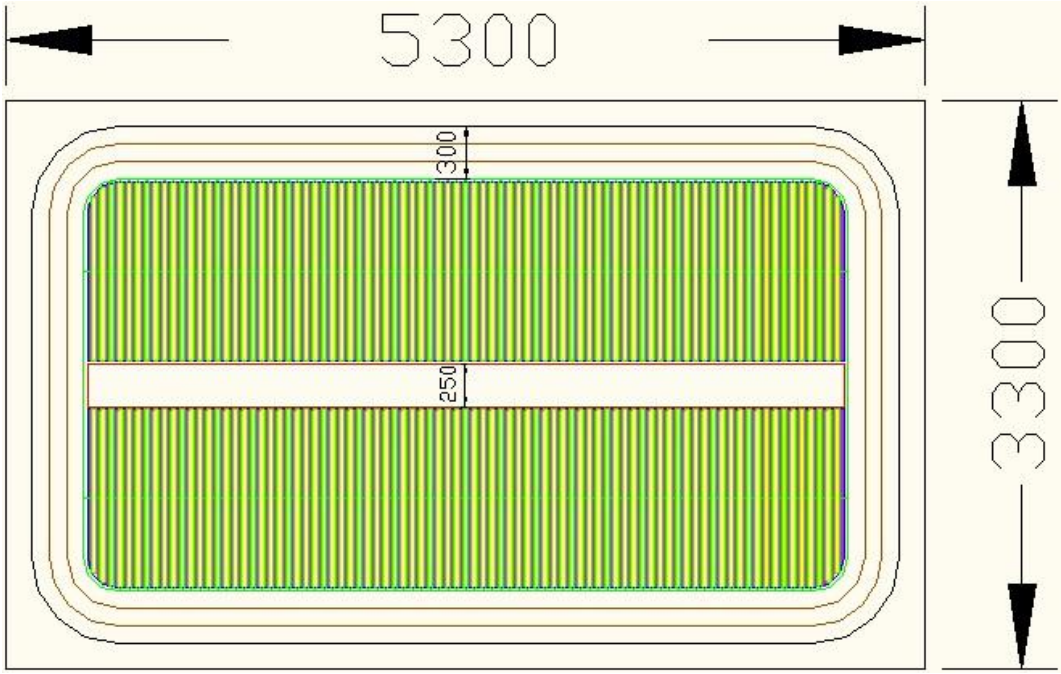


Fig. 3-11 Top view of type A GTO design showing rectangle-shape gate bonding

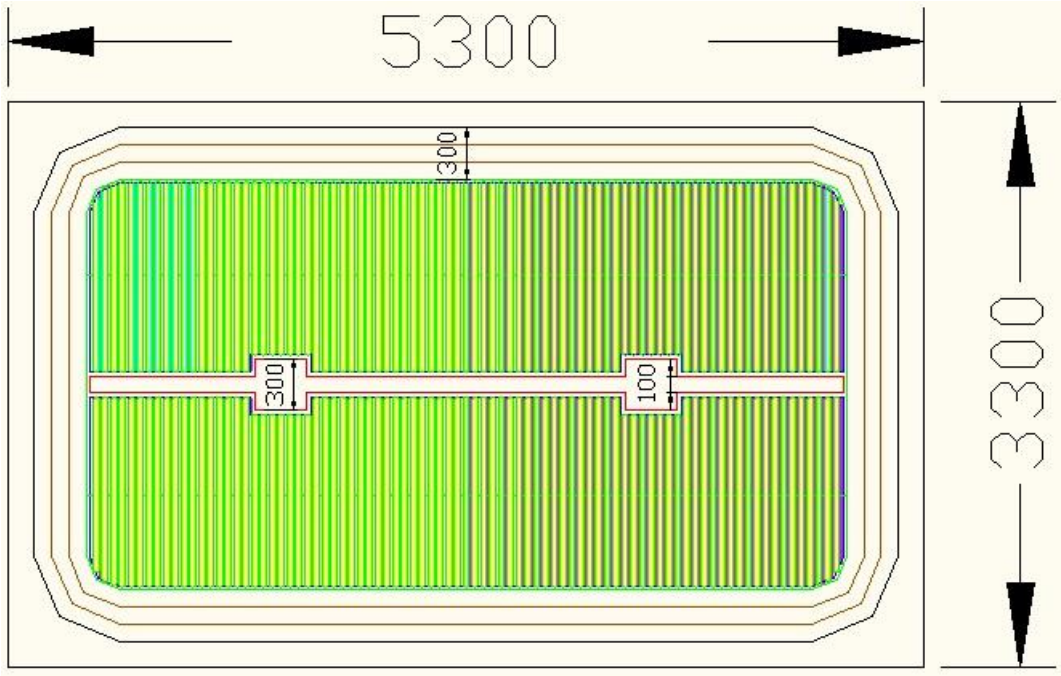
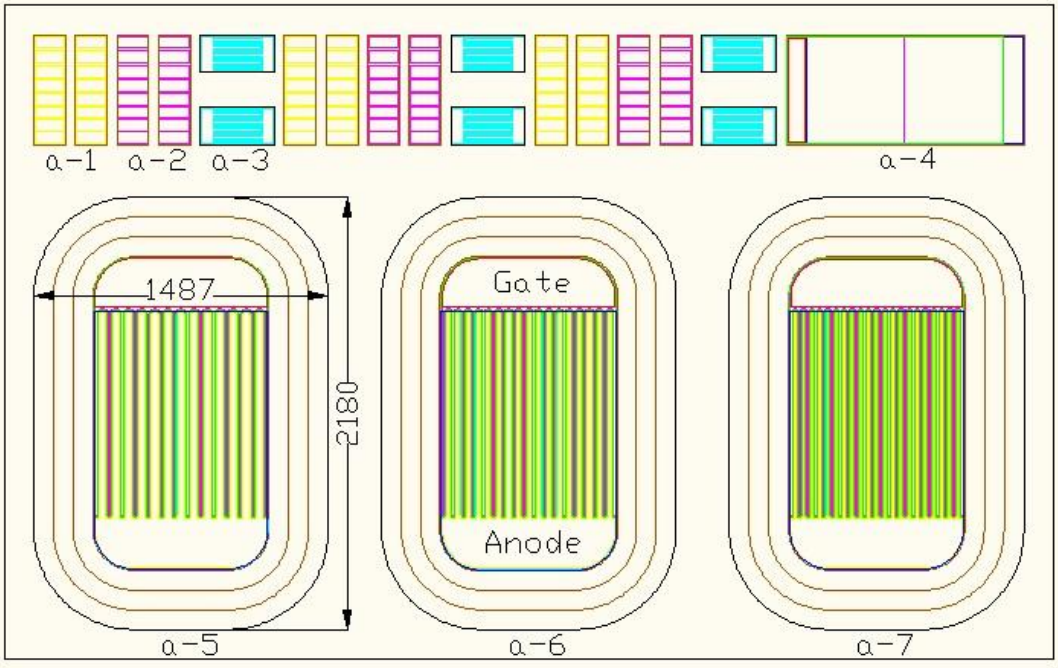


Fig. 3-12 Top view of type B GTO design showing barbell-shape gate bonding

3.3.4 Small GTO and Testing Pattern design

As shown in Fig. 3-9 with label a, four groups of small testing GTOs, TLM structures and some additional test structures were embedded in the GTO mask set to evaluate the effectiveness of the interdigitated design, mesa etching, termination, and quality of the Ohmic contacts.

The small GTOs, shown in the lower part of Fig. 3-13, with area of 1.487 mm x 2.18 mm have an active area of 1.4 mm^2. The finger length is 1032 μm, which is exactly the same as 0.1 cm^2 large GTOs. The width of the small GTOs' finger includes 32 μm (type a-5: 13-finger cell), 17 μm (type a-6: 17-finger cell) and 7 μm (type a-7: 21-finger cell) to test the influence of different anode/gate finger geometry. A gate pad and an anode pad were designed at the top and bottom sides in the small GTO cells.



(a)

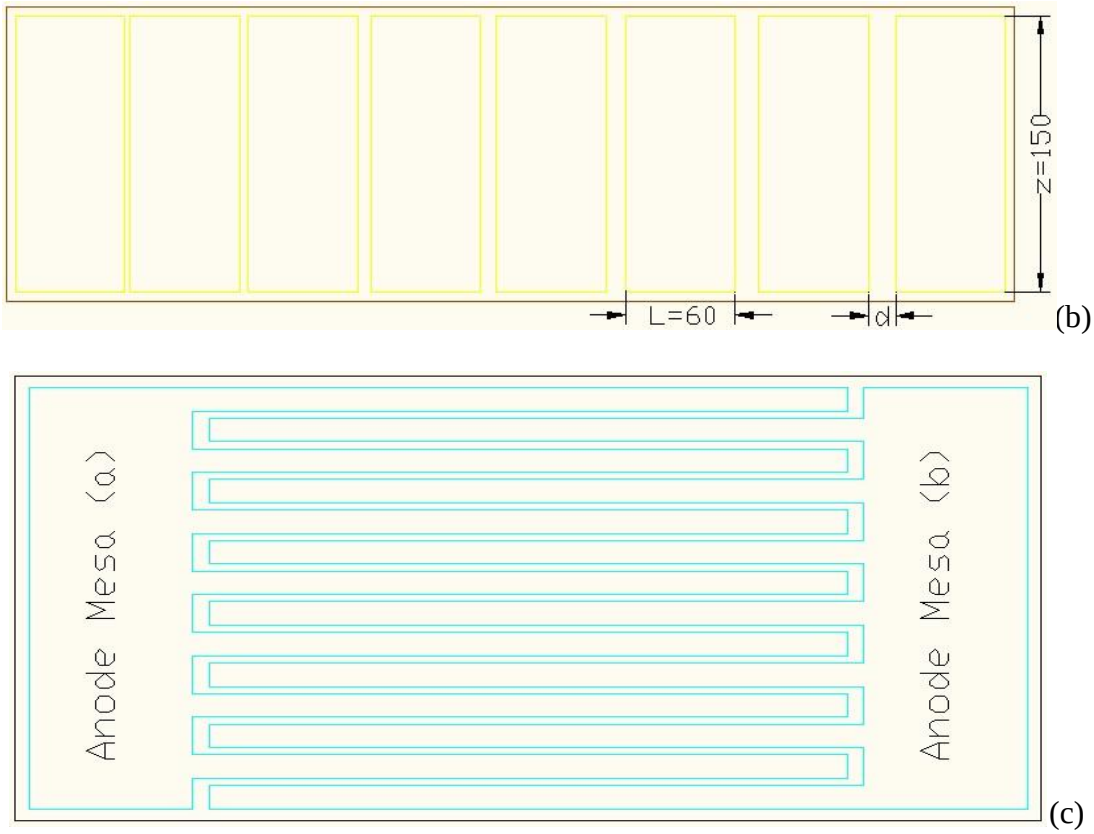


Fig. 3-13 (a) Top view of small GTOs and testing patterns (unit: μ m), details in (b) TLM design and (c) mesa etching monitor

The specific contact resistances were estimated by using TLM. In the TLM method, two masks are usually needed. One is to define TLM patterns like a-1 (for anode Ohmic contact) and a-2 (for gate Ohmic contact) shown in Fig. 3-13 (a) and detail in (b). The other one confines the current in one dimension either by mesa etching or junction isolation. Each TLM pattern has 8 rectangular shaped pads, which are intended to for a metal contact. The width of the mesa is z = 150 μm and the distance between two adjacent pads is d, which increases from 3 μm to 15 μm by 2 μm.

The anode mesa etching is the one of the challenge processes in the fabrication of the GTO devices. Since the epilayer thickness could vary ± 10% from the specification, the

etching depth needs to be precisely controlled and monitored by I-V measurements from the adjacent p-type SiC mesa. If p-type SiC remains in the gate trench after the anode mesa etching, the anode-gate junction is shorted and the device will not work. At the same time, too much over etching of the n-type gate layer could lead to the low blocking voltage because the remaining n-type epilayer also serves the JTE purpose. Therefore testing patterns a-3, as shown in Fig. 3-13 (a) and detail in (c), was designed to serve the purpose of the mesa etching monitor. The two adjacent testing mesa patterns can be probed to measure the conductivity between them to tell when will be the exact stop point for mesa etching.

Testing Pattern a-4 in Fig. 3-13 consisting of rectangle-shape drawings was designed for metal thickness measurements and a surface morphology monitor during metal deposition.

3.4 Summary

A 4H-SiC asymmetrical GTO has been designed and simulated with the maximum blocking voltage above 8 kV with a blocking layer thickness equal to 60 μm. Excellent turn-on and turn-off characteristics are noted at V_{AK} = 3500 V for an cathode current of 233 A with a turn-on/off time of 87 ns and 2.4 μs, respectively.

A major effort was put into the design of a set of 6 kV 4H-SiC GTO masks suitable for high power, high temperature, and high switching speed applications. Photo masks for various lithographic steps in the process were designed using the computer program AutoCAD from Autodesk Inc. licensed to Rutgers University and manufactured to specifications at Photo Sciences Inc. The set of masks is listed in Table 3-1.

Table 3-1 GTO mask set

No.	Mask	Function
1	**Anode mesa**	This mask forms the AlTi mask for the formation of anode mesas and gate trenches in the GTO.
2	**Gate implant**	This mask is for N implantation to form the gate Ohmic contact and pattern the gate contact metal.
3	**Isolation mesa**	This mask forms the AlTi mask for etching isolation of GTO cells.
4	**JTE 3**	This mask forms the AlTi mask for etching JTE3 region of GTO cells.
5	**JTE 2**	This mask forms the AlTi mask for etching JTE2 region of GTO cells.
6	**JTE 1**	This mask forms the AlTi mask for etching JTE1 region of GTO cells.
7	**Anode contact**	This mask is to pattern the anode contact metal.
8	**Gate overlay**	This mask opens the gate pad to deposit overlay metal there.
9	**Anode overlay**	This mask opens the anode pad to deposit overlay metal there.
10	**Gate pad**	This mask is to pattern the gate wire bonding pad.

CHAPTER 4 FABRICATION AND CHARACTERIZATION OF 4H-SiC GTO

The 4H-SiC GTO devices designed in Cchapter 3 of this dissertation were fabricated in the Microelectronics Research Laboratory (MERL) clean room at Rutgers University. Photo masks for various lithographic steps in this process were designed using the computer program AutoCAD from Autodesk Inc. licensed to Rutgers University and manufactured to specifications at Photo Sciences Inc. SiC substrates with epitaxially grown layers suitable for device fabrication were provided by CREE. This chapter details the various steps in the fabrication of the SiC GTO devices, including:

- ✧ Wafer cleaning
- ✧ Anode mesa formation
- ✧ Gate formation by n^+ implantation and dopant activation annealing
- ✧ Isolation and MJTE formation by ICP etching
- ✧ Surface passivation by SiO2 and Si3N4
- ✧ Ohmic contact formation
- ✧ Metal overlay formation
- ✧ GTO devices package

The fabricated GTO devices are characterized for their properties in the power circuit operation. These include the blocking voltage, on resistance, switching speed and variation of properties with temperature. Static pulsed I-V curves are measured with Tektronix 371A high power curve tracer, Glassman high voltage power supply, and Kiethley 6517A electrometer. The temperature characterization is conducted by clamping the wafer to a hot plate whose

temperature is measured using a thermocouple arrangement. The switching test is conducted using a modified trigger board from Princeton Power Systems, Inc. (PPS).

4.1 Device Fabrication

4.1.1 Wafer Structure

The starting 4H-SiC wafer from Cree, Inc. includes five epilayers grown on an n-type substrate, as shown in Fig. 4-1. All the epilayers were grown in a single run and designed for a high turn-on gain. A 60 μm thick, lightly doped ($N_A = 9x10^{14}\ cm^{-3}$) P-base layer is used to achieve the high blocking voltage (more than 6kV). The underneath p+ buffer layer of 2 μm doped to $2x10^{17}\ cm^{-3}$ is used to stop the field in the blocking mode and to improve the quality of the blocking layer. It also makes the electric field profile in the blocking layer more uniform. The other two layers are $2.33x10^{17}\ cm^{-3}$ doped n-base layer of 2 μm and p^{++} top layer.

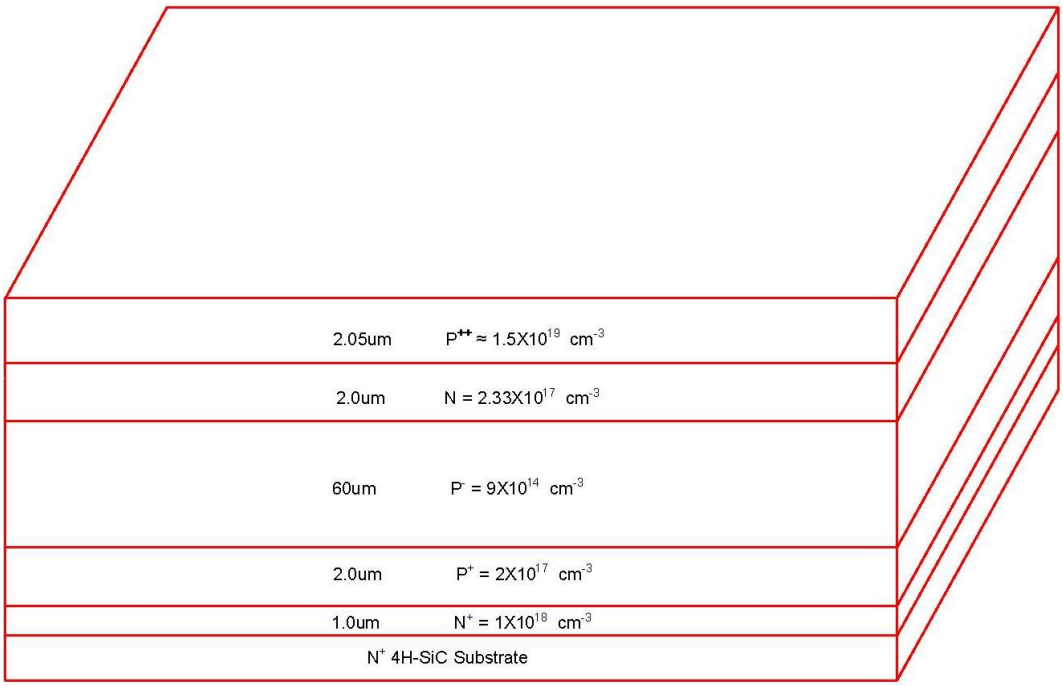


Fig. 4-1 Schematic of 4H-SiC wafer structure 3D view

Wafer fabrication starts with a full cleaning of the ordered wafer, including the following steps:

(1) Acetone ultrasonic: This is a general cleaning that removes dust and some contaminations on the wafer.

(2) Mixture of sulfuric acid and hydrogen peroxide: 98% H_2SO_4 (sulfuric acid) is mixed with 30% H_2O_2 (hydrogen peroxide) at the volume ratio of 4:1 and heated to 85^{o}C. The SiC wafer is then immersed in this solution for 30 minutes for the removal of possible gross organic materials, such as photo resist, polymer or other contaminants. These contaminants are destroyed by the wet-chemical oxidation effect of the mixed solution.

(3) RCA cleaning: This procedure was developed at RCA forty years ago, and has been widely used for silicon wafer cleaning, [44]. First, a mixture of deionized (DI) water

(H_2O), hydrogen peroxide (H_2O_2) and ammonium hydroxide (NH_4OH) is prepared at the volume ratio of 5:1:1 and heated up to 80^oC. This solution is commonly called SC-1. The SiC wafer is placed in the SC-1 solution for up to 30 minutes. SC-1 is intended to remove organic contaminants that are attacked by both the solvating action of NH_4OH and the powerful oxidizing action of the alkaline H_2O_2. NH_4OH also removes certain metals such as Cu, Au, Ag, Zn, Cd, Ni, Co and Cr by complexing them. After this, an acidic solution commonly called SC-2 is prepared by mixing DI H_2O, H_2O_2 and hydrochloric acid (HCl) at the volume ratio 5:1:1. This solution is also heated to 80^oC for a 30-minute cleaning of the SiC wafer. The SC-2 is designed to dissolve and remove alkali residues and any trace metals, such as Au and Ag, as well as metal hydroxides, including $Al(OH)_3$, $Fe(OH)_3$, $Mg(OH)_2$ and $Zn(OH)_2$.

(4) 10% hydrofluoric (HF) acid: The full cleaning procedure is completed with an ultrasonic cleaning in diluted hydrofluoric acid, refreshing the SiC surface by removing the top oxide layer.

4.1.2 Mesa Formation

After wafer cleaning, anode mesas were etched in an inductively-coupled plasma (ICP) chamber by a SiC dry etching process based on CF_4 and O_2 gas chemistry. In CF4+O2 gas mixture for SiC etching, the following reactions are proposed to take place: [45]

$$CF_4 + O_2 \rightarrow CF_X + F + O + (CO, CO_2) \quad \text{Eq. 4-1}$$

$$Si + xF \rightarrow SiF_X \quad \text{Eq. 4-2}$$

$$C + xF \rightarrow CF_X \quad \text{Eq. 4-3}$$

$$C + xO \rightarrow (CO, CO_2) \quad \text{Eq. 4-4}$$

A 300nm AlTi layer was deposited on the wafer by sputtering to serve as the etching mask layer. Photolithography using AZ5214 resist followed by wet etching in a commercial Al Etch II solution created the mesa etching mask patterns. The lithography recipe is listed in Table 4-1. AlTi mask etching was finalized by an Al residue cleaning procedure in highly diluted hydrofluoric acid (3%x3%x3%) for one minute. After this, photo resist was removed in heated AZ400T stripper at 80^{o}C for 20 minutes.

Table 4-1 Photolithography recipe for mesa etching mask using AZ5214

Dry Bake	130^{o}C, 30 minutes
PR Spin-coat	PR AZ5214 Spin at 4000 RPM for 40 seconds
Soft Bake	90^{o}C, 20 minutes
Exposure	UV exposure, 5 seconds
Develop	AZ 1:1 developer, 90 seconds
Hard Bake	130^{o}C, 30 minutes

After the deposited metal film patterned by the photo mask “Anode Mesa”, the gate trenches were etched in an ICP etcher in plasma. The etching was done in several runs and the final etched depth was 2.25 μm. The resulting 3D view after mesa etching is illustrated in Fig. 4-2.

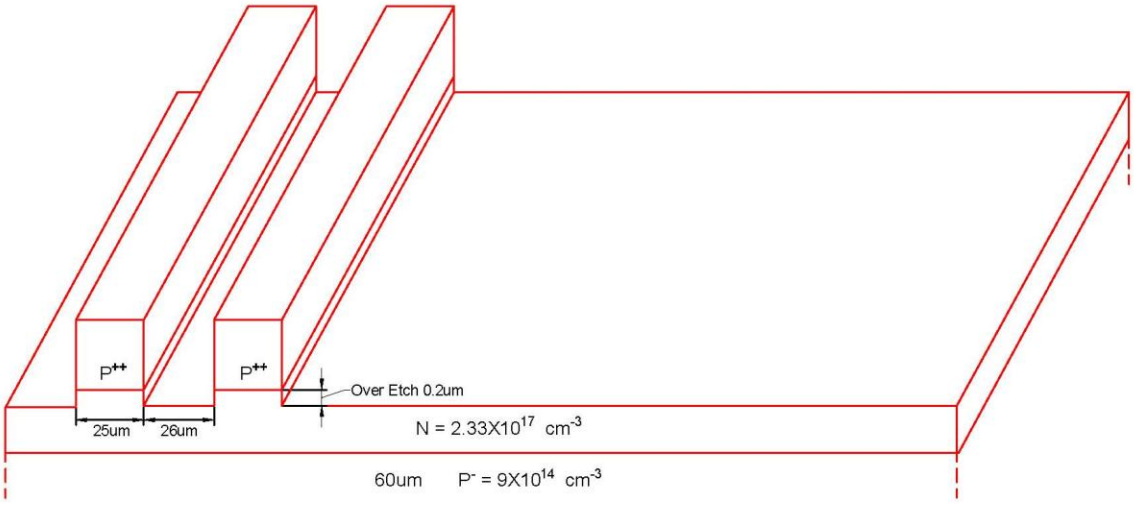


Fig. 4-2 Schematic of the anode mesa 3D view

4.1.3 Gate Implantation and Post-implantation Annealing

In order to create n^{++} regions in the gate of GTOs, we requested a group of nitrogen (N) doses with a 0^{o} incidence angle. The implantation simulation was carried out by Profile Code with Person IV distribution assumption [46]. The tail of Nitrogen (N) vertical ion implantation profile was modeled by a linear degradation of 100 nm per decade on a semi-log plot, as shown in Fig. 4-3 (a). The implantation depth was defined by the intersection of the implantation tail and the background doping. The simulation result indicates that the n^{++} doping is about $3x10^{19}$ cm^{-3} and the implanted depth is 350 nm when the implantation tail decreases to the background N doping of $2.33x10^{17}$ cm^{-3}. Molybdenum (Mo) was design as a metal mask for N ion implantation. Fig. 4-3 (b) indicates that the depth of N ion implantation in Mo is about 5000 Å, so that the 1.1 μm Mo mask layer should be safe for N ion implantation.

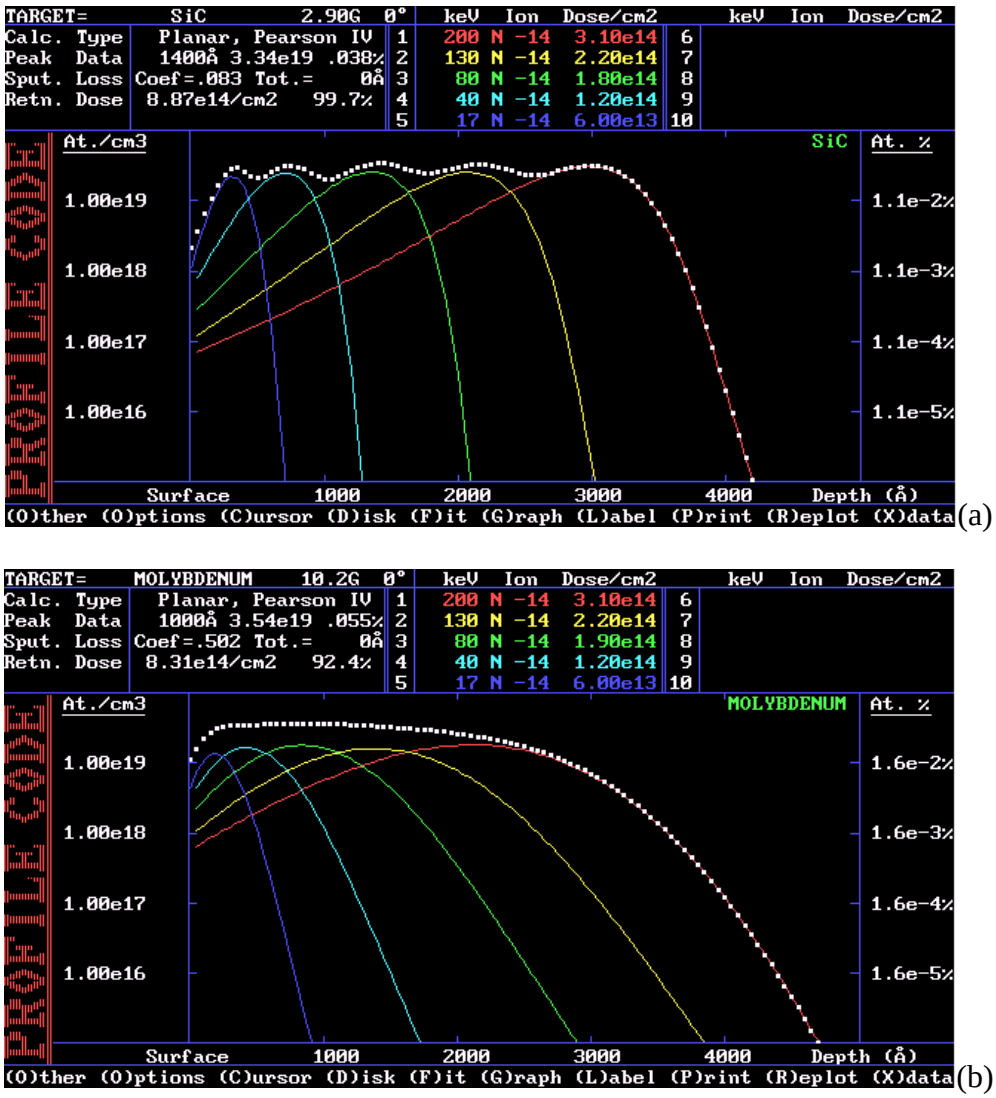


Fig. 4-3 N^+ doping profile of the Gate vertical implantation in: (a)4H-SiC and (b) Mo.

To create the N ion implantation mask, 1.1-μm thick Mo was sputtered and patterned by the lithography with one exposures of a Gate Implant mask, and then by the following wet etching (Al Etch II). AZ4400 thick photo resist was defined on the wafer prior to the wet etching to transfer the photo patterns to Mo. The lithography condition for PR AZ4400 is listed in Table 4-2. The schematic of the implantation mask is plotted in Fig. 4-4 (a). The wafer with Mo mask was sent to Leonard J. Kroko, Inc. for Nitrogen (N) ion

implant service. A vertical N ion implantation was done to form n^{++} layer for better gate Ohmic contacts. The detail implantation specifications have been listed in Table 4-3.

The sample returned from gate implantation was ready for implant activation. The implantation mask was removed by Al-etchant II. Then we performed full cleaning of the wafer in sulfuric acid, RCA SC-1, RCA SC-2 and hydrofluoric acid. Then it is annealed in argon ambient at 1550 ^{o}C for 30 min to electrically activate the implanted nitrogen dopants. A 3D view of the GTO after gate implantation is shown in Fig. 4-4 (b).

Table 4-2 Photolithography recipe for the mesa etching mask using AZ4400

Dry Bake	130 ^{o}C, 30 minutes
PR Spin-coat	PR AZ4400 Spin at 3500 RPM for 40 seconds
Soft Bake	100 ^{o}C, 20 minutes
Exposure	UV exposure, 30 seconds
Develop	AZ 1:1 developer, 4 minutes
Hard Bake	130 ^{o}C, 30 minutes

Table 4-3 N implantation specification

Step	**Ion**	**Energy**	**Dose (cm^{-2})**
1	N	190	3.1e14
2	N	130	2.2e14
3	N	80	1.8e14
4	N	40	1.2e14
5	N	17	6.0e13

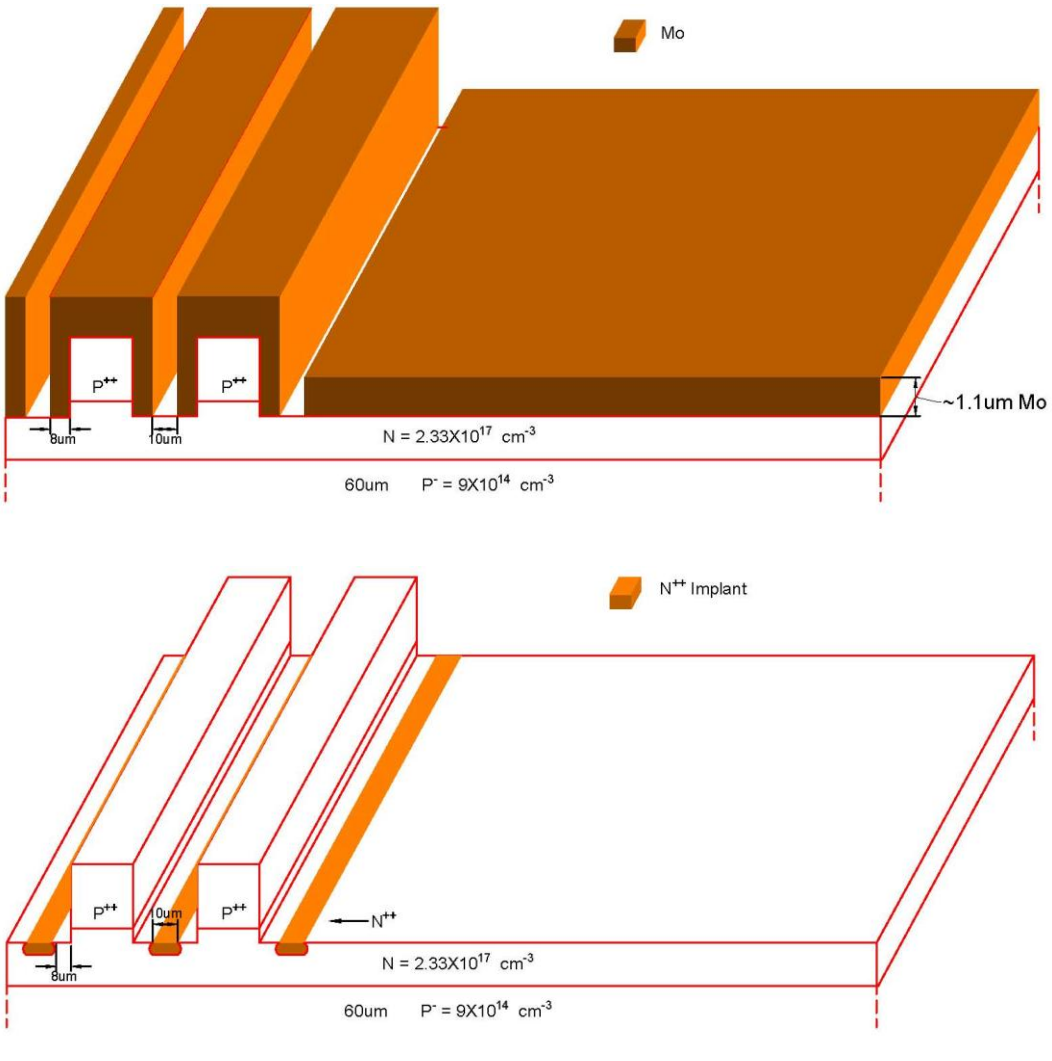


Fig. 4-4 Schematics of 3D view on (a) Mo mask and (b) Implanted gate after Mo removal

4.1.4 Isolation and MJTE formation

Device isolation for the GTOs was accomplished by etching more than 2 μm-deep peripheral trenches around the active devices. Trench etching used a 600 nm-thick AlTi mask, patterned by wet etching in Al Etch II solution. AZ4400 thick photo resist was defined on the wafer prior to the wet etching to transfer the Isolation Mesa mask patterns to AlTi. The lithography condition for AZ4400 is listed in Table 4-2. Following the photo

resist removal, ICP etching was used to create the trenches in SiC. Schematics of 3D view on the isolation mask and isolation formation are included in Fig. 4-5. This process step was completed with a hydrofluoric acid cleaning of the AlTi etching mask.

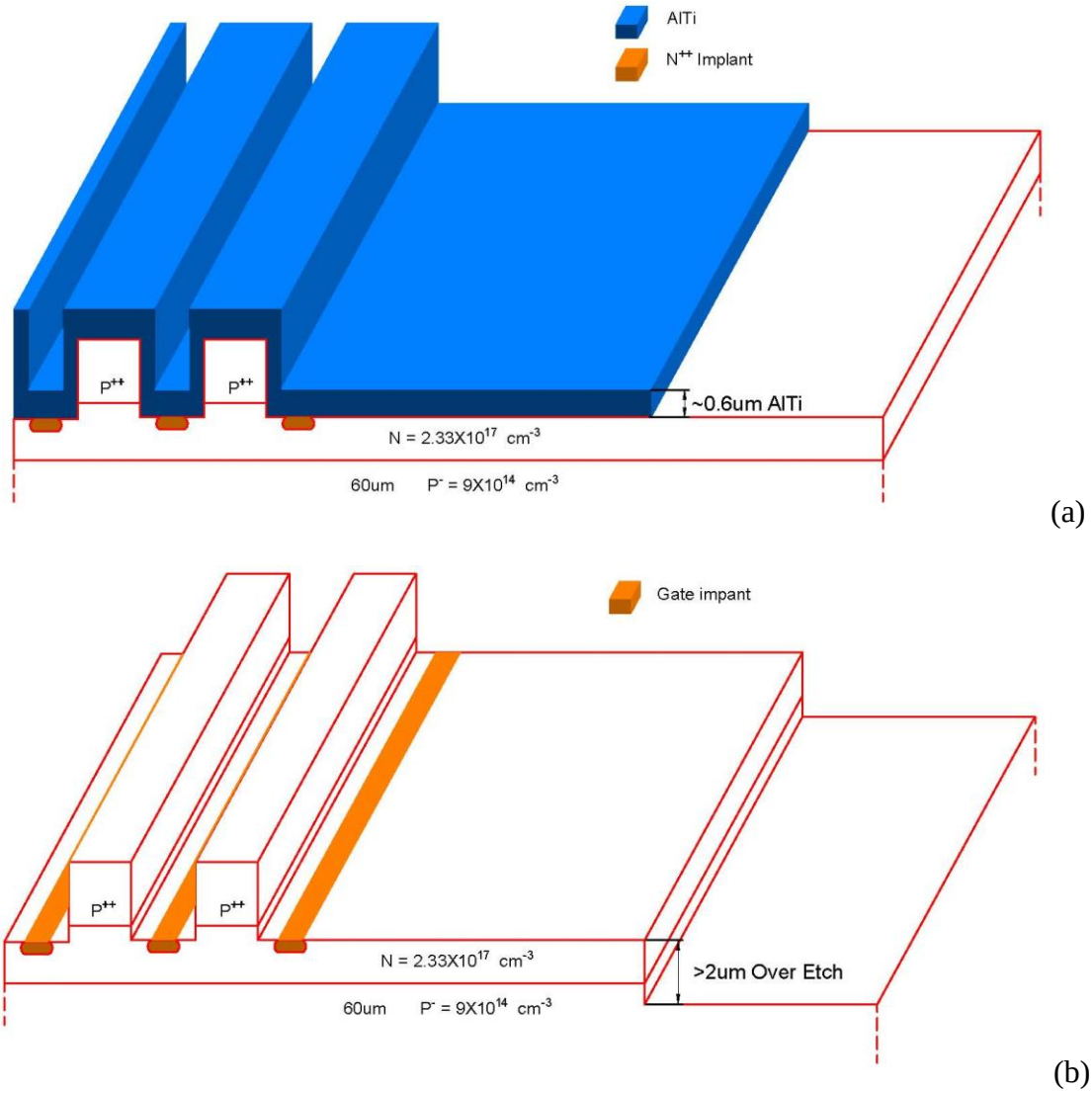
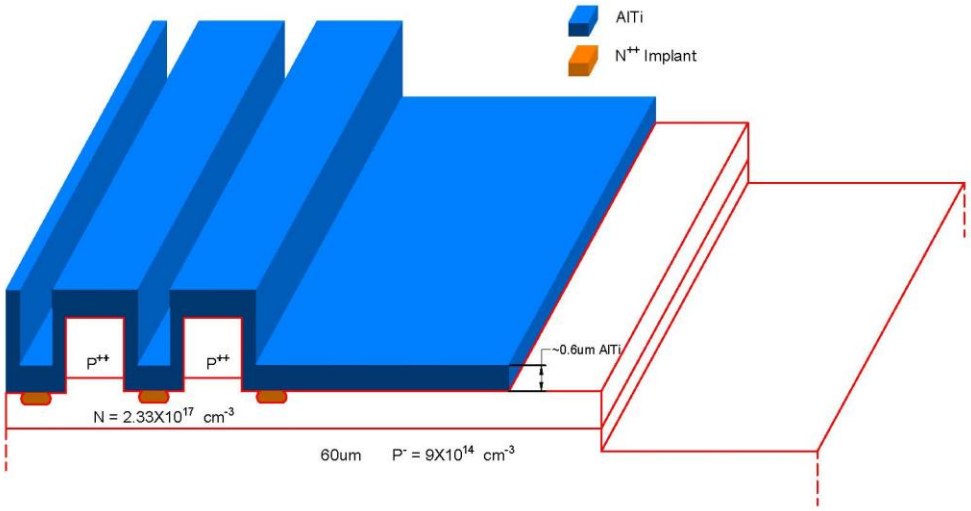


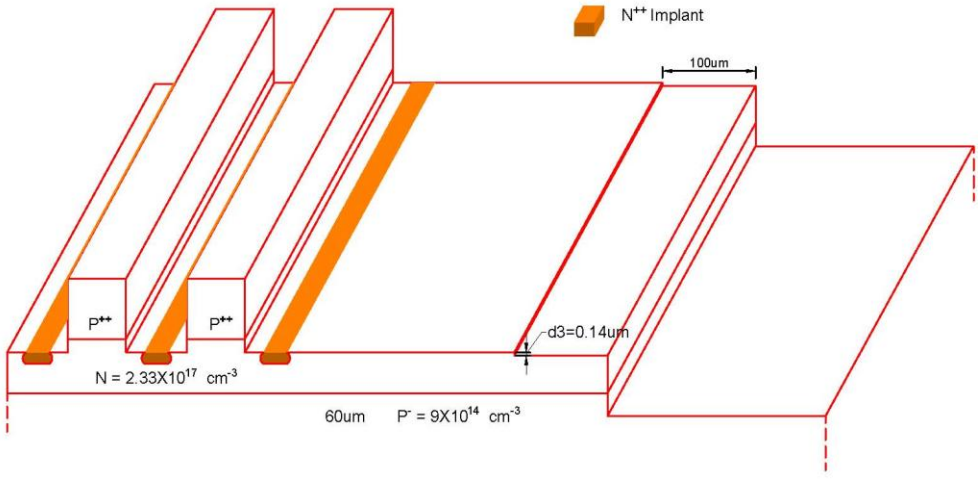
Fig. 4-5 Schematics of 3D view on (a) AlTi mask and (b) isolation after AlTi removal

After isolation formation, 3-step MJTE was employed to reduce the electric field at the device periphery. The JTE region needs to be thinned down by dry etching in order to

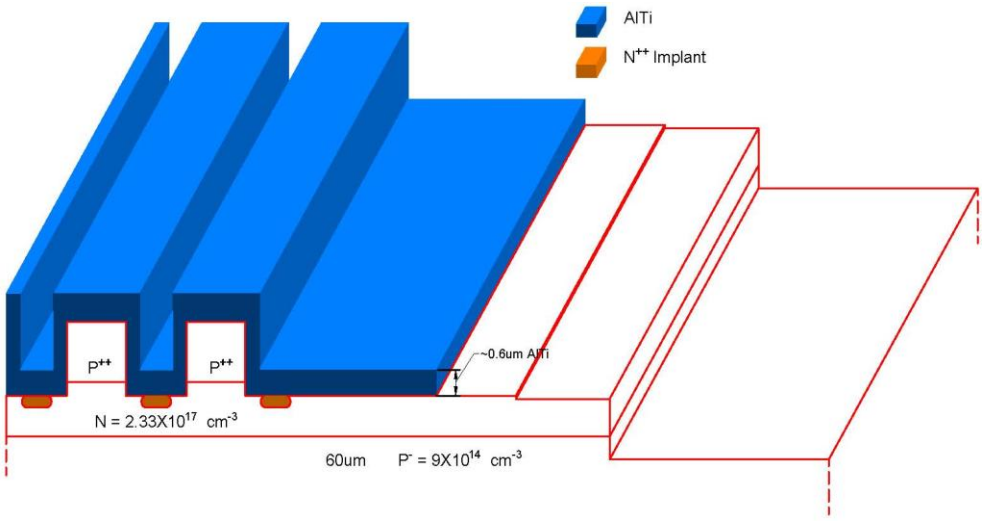
achieve the charge balance that will give the desired field suppression at the device periphery. The MJTE region was processed to have NPN structure with 3-step MJTE with the step width of 100 μm. The outer two steps were etched to 0.14 μm and the inner step depth was etched to 1.4 μm. The detail on MJTE design has been discussed in Chapter 2. The process condition on MJTE formation was similar to isolation formation except applying different photo masks, including JTE3, JTE2 and JTE1 masks. The fabrication steps on MJTE formation have been illustrated in Fig. 4-6.



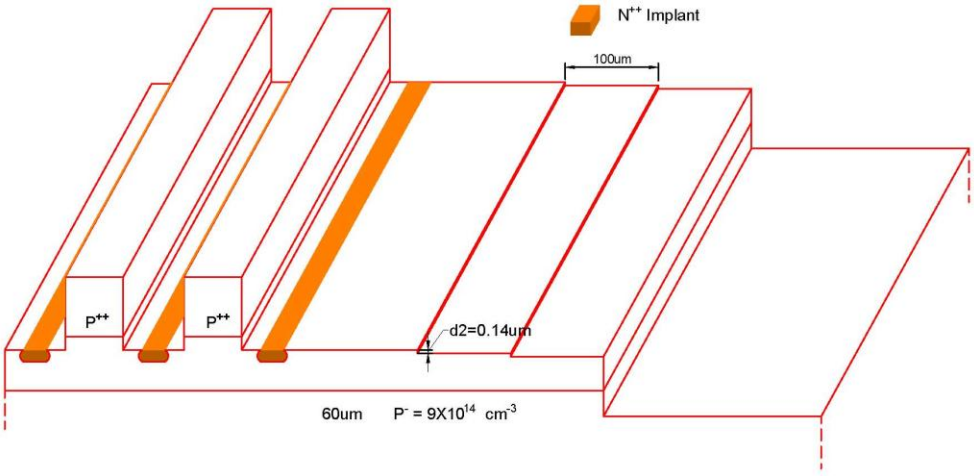
(a)



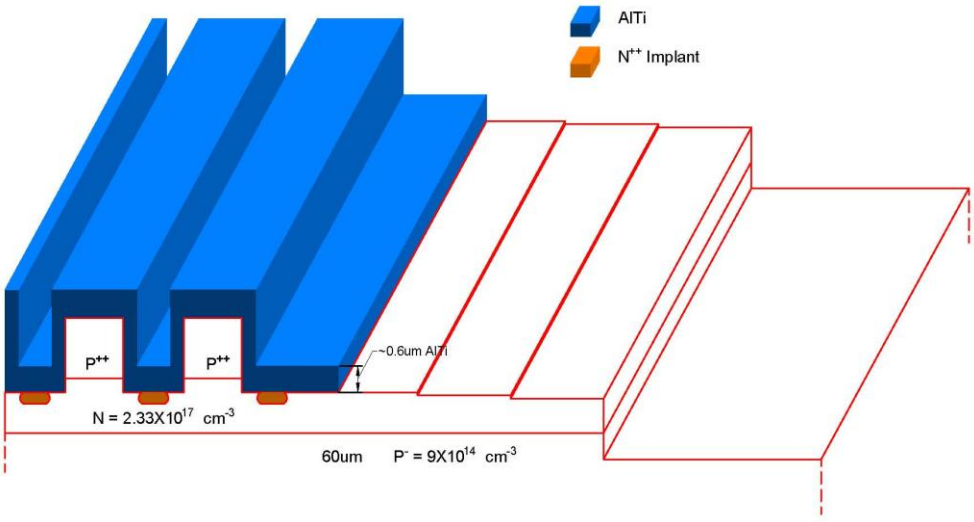
(b)


AlTi
N++ Implant
P++
P++
~0.6um AlTi
N = 2.33X10^17 cm^-3
60um
P- = 9X10^14 cm^-3

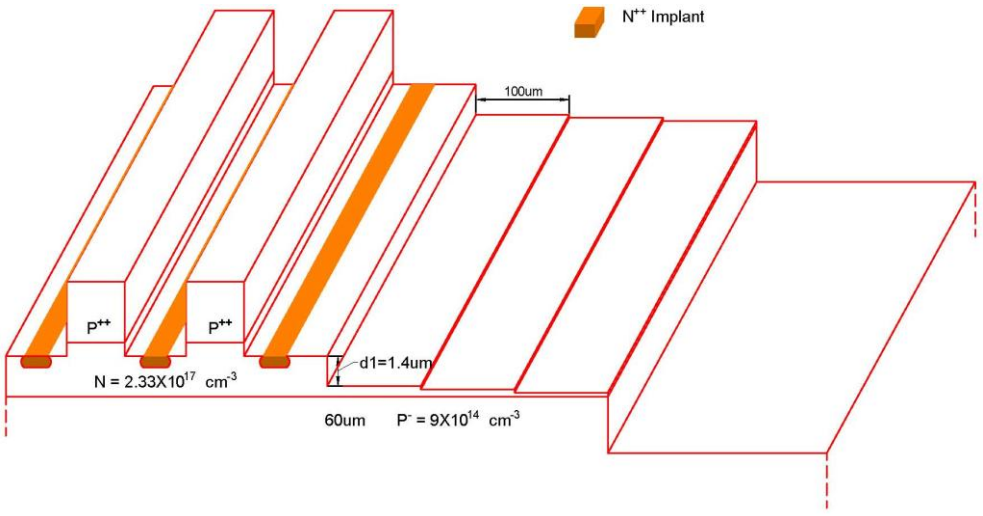
(c)


N++ Implant
100um
P++
P++
d2=0.14um
60um
P- = 9X10^14 cm^-3

(d)


AlTi
N++ Implant
P++
P++
~0.6um AlTi
N = 2.33X10^17 cm^-3
60um
P- = 9X10^14 cm^-3

(e)



(f)

Fig. 4-6 Schematics of 3D view on (a) JTE_3 mask; (b) JTE_3 after AlTi removal; (c) JTE_2 mask; (d) JTE_2 after AlTi removal; (e) JTE_1 mask and (f) JTE_1 after AlTi removal

4.1.5 Oxidation and Passivation

Before oxidizing the samples to form the passivation needed, the wafers were cleaned using a thorough cleaning procedure. The cleaned samples were then thermally oxidized at 1100^{o}C for 30 minutes in wet O_2 ambient to form a sacrificial oxide. The sacrificial oxide was then removed by diluted hydrofluoric acid, together with certain surface defects and damages caused by ion implantation and plasma etching processes. Immediately after that, the wafer was reloaded to the oxidation chamber for surface passivation at 1100^{o}C for 3 hours in a wet oxygen ambient to form a permanent layer of thermal SiO_2. The oxide is then annealed at 1100 ^{o}C for 1 hour in Ar. The oxide thickness is estimated to be about 600 Å. The chemical reactions responsible for SiC oxidation includes: [47]

$$SiC + \frac{3}{2}O_2 \rightarrow SiO_2 + CO \qquad \text{Eq. 4-5}$$

$$SiC + O_2 \rightarrow SiO_2 + C \qquad \text{Eq. 4-6}$$

The SiC-SiO_2 interface in SiC JFETs is not critical as compared to SiC MOSFETs. While carbon clusters and other defects formed during the oxidation process may be a serious concern for SiC MOSFETs, it does not pose a problem for the GTOs.

Following the oxide passivation, a 300 nm layer of PECVD silicon oxide is additionally deposited. Silicon nitride is commonly used to passivate silicon devices because it provides an extremely good barrier to the diffusion of water and sodium. [48] Then a layer of PECVD Si_3N_4 with thickness of 0.25 μm was deposited. These thin films typically have less tensile stress but also dielectric strength. Fig. 4-7 shows the devices after the final stage of passivation.

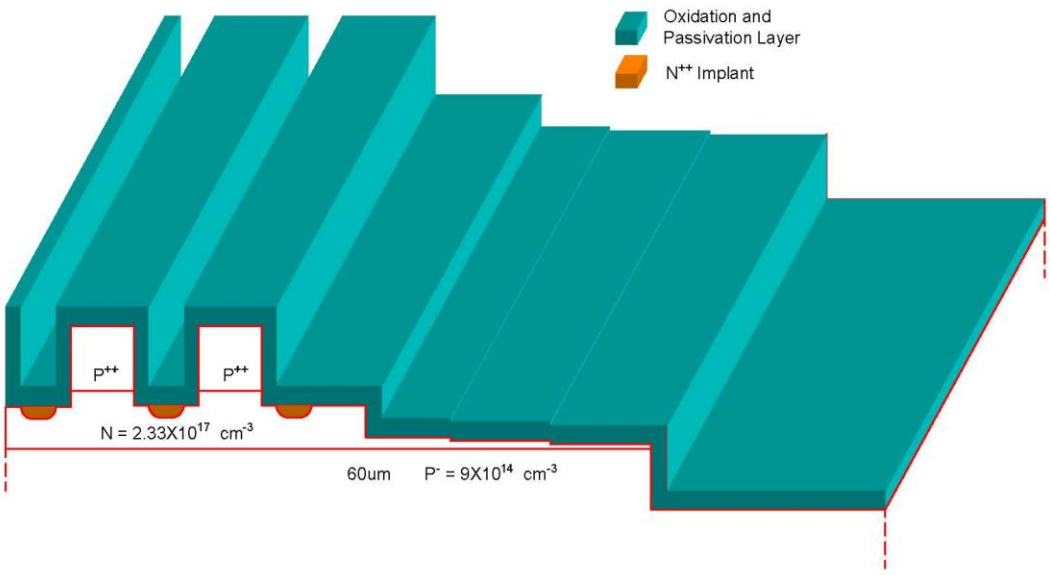


Fig. 4-7 Schematic of 3D view on one GTO device after the formation of passivation layers

4.1.6 Ohmic Contact

A good Ohmic contact is crucial for most semiconductor devices since the voltage drop across on the contact could significantly influence the device performance. The contact resistance needs to be negligible compared to the device on-resistance in order to reveal the intrinsic device character. Ohmic contact formation typically included a metal deposition followed by a high temperature annealing process which forms a metallic intermediate layer in the 4H-SiC surface.

After surface passivation, the contact windows are firstly opened by ICP etching using AZ4400 as the dry etching mask. Since the oxide etching rate is slower than silicon nitride, the thermal oxide and some PECVD oxide remain after the dry etching. The remaining oxide was etched by buffered oxide etchant just before metal deposition. This wet etching process leaves a more ideal silicon carbide surface, and it also makes the lift-off process much easier due to some undercut below the nitride. And the most important, this wet etching process leaves a small gap between the oxide and the deposited metal which avoids the possible metal/oxide contact to prevent the metal spill-over problem in the oxide.

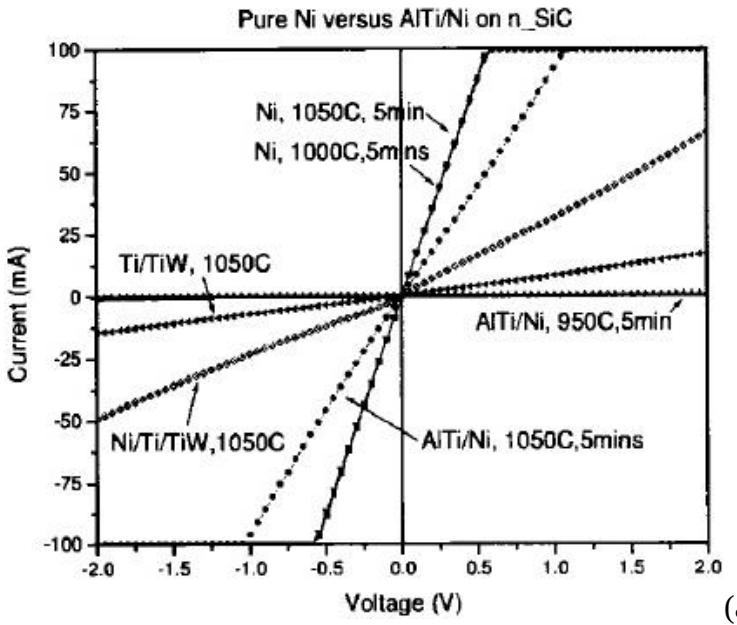
The contact metals are sputtered right after the wet-etching of the oxide. After the lift-off, the contact metal remains on the n-type gate or the p-type anode regions. The backside n-type contact metal is also sputtered after n-type gate metal deposition. The contact annealing was done in a rapid thermal annealing (RTA) system. The RTA process provides excellent temperature control, high throughput, and a much better protection of the sample from being oxidized.

To better protect the sample from oxidation, forming gas, including 5% hydrogen and 95% argon, was connected to the RTA system during the RTA process. The forming gas not only gives a better protection on the metal surface, but also could improve the SiO_2/SiC interface [49]. After the RTA process, the Ohmic contact resistance and sheet resistance can be measured from the TLM patterns, which were designed within Ohmic contact masks.

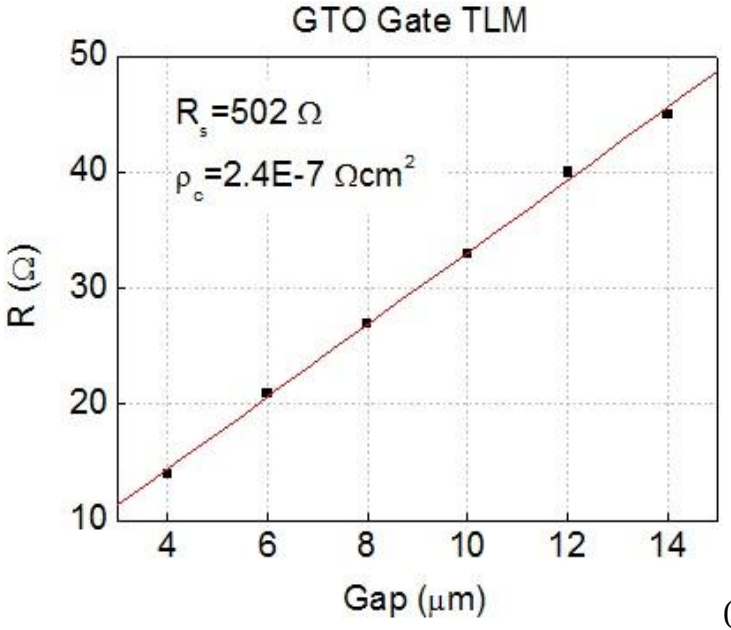
- **n-type 4H-SiC Ohmic contact**

The N-type SiC Ohmic contact on anode is critical to achieve low on-state resistance although the n-type contact resistance is usually much lower than p-type SiC. Normally, the n-type contact metal includes AlTi/Ni, Ni, Ti/TiN and Fig. 4-8 (a) [50] shows a comparison among n-type contact metals on the same n-type substrate, which indicates that pure Ni gives the best contact on n-type 4H-SiC and higher temperature than 1000 ^{o}C is necessary to obtain the optimum low contact resistance.

Therefore, pure Ni was selected for the n-type Ohmic contact metal for GTO devices. Right after 1500Å Ni deposition, the GTO wafers was annealed in the RTA chamber at 1050 ^{o}C for 5 minutes. The I-V curves measured from n-type TLM patterns are perfectly linear as shown in Fig. 4-8 (b), which indicates that the excellent n-type Ohmic contact are formed with Gate specific contact resistance of 2.4×10^{-7} $\Omega\cdot cm^2$. The detail process for gate contact formation is shown in Fig. 4-9.



(a)



(b)

Fig. 4-8 (a) n-type Ohmic contact metal [50] and (b) n-type TLM test plot after 1050 ^{o}C annealing.

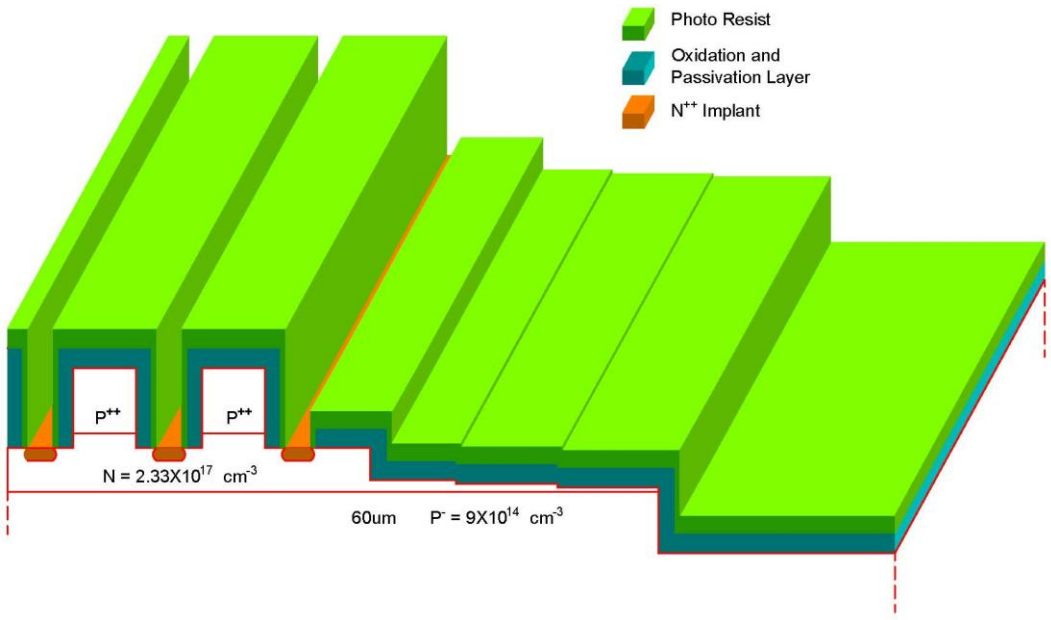
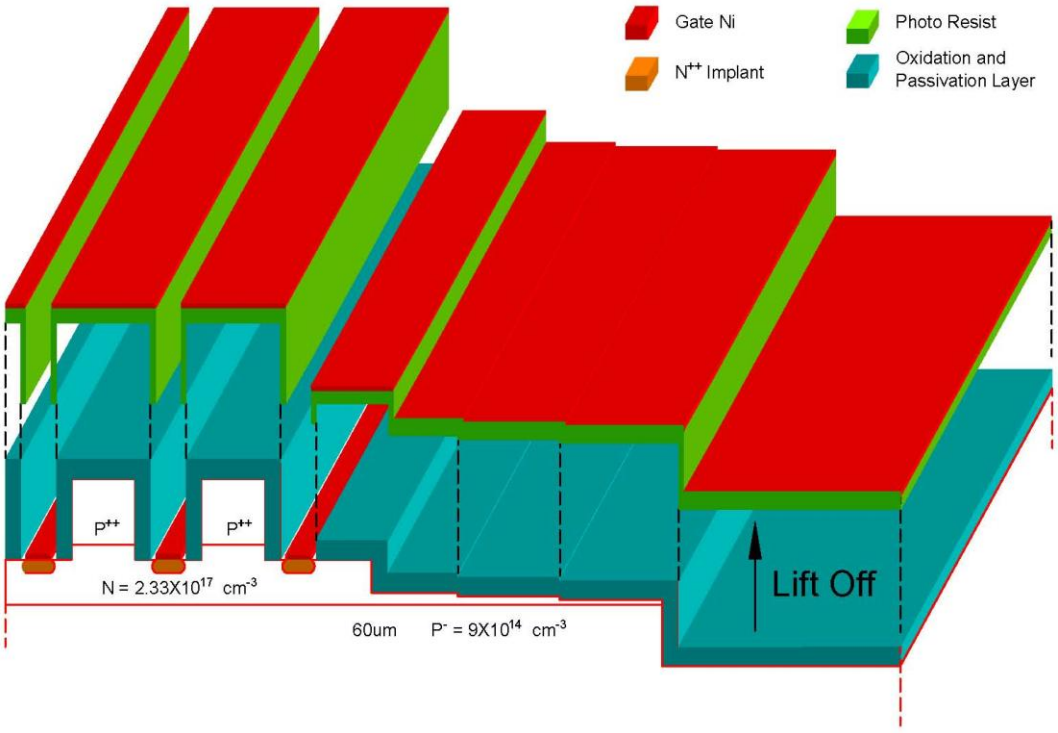
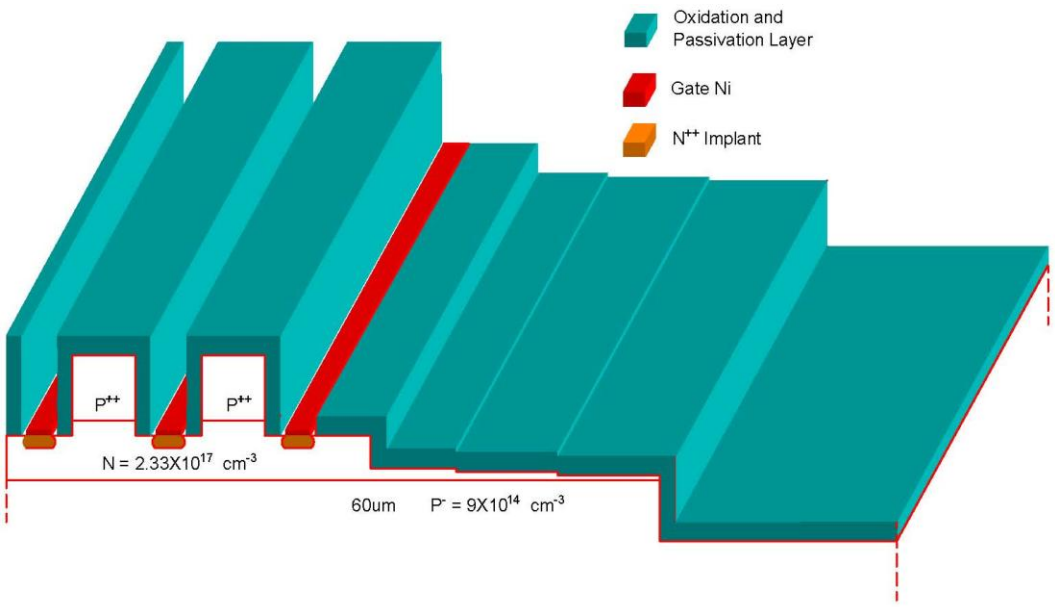


Photo Resist
Oxidation and Passivation Layer
N++ Implant
P++
P++
N = 2.33X10^17 cm^-3
60um
P- = 9X10^14 cm^-3

(a)


Gate Ni
N++ Implant
Photo Resist
Oxidation and Passivation Layer
P++
P++
N = 2.33X10^17 cm^-3
60um
P- = 9X10^14 cm^-3
Lift Off

(b)



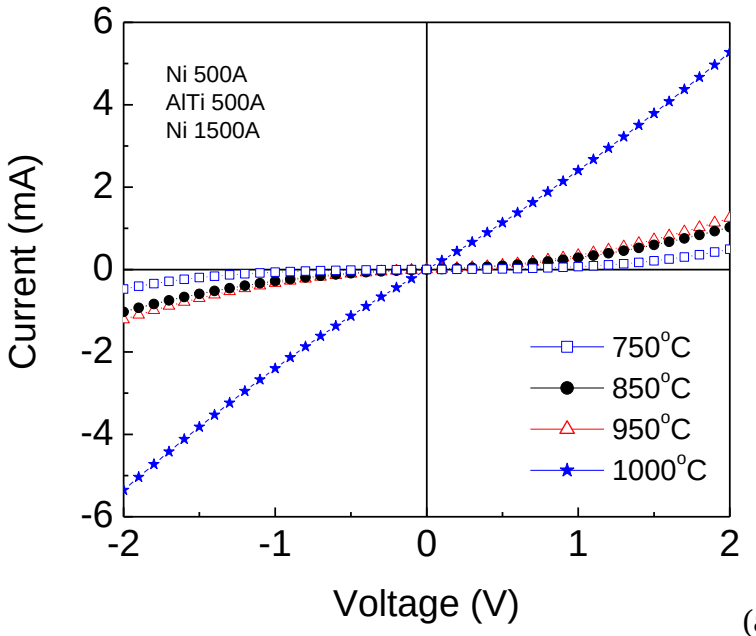
(c)

Fig. 4-9 Schematics of 3D view on (a) Gate contact window open, (b) Metal lift-off and (c) Gate metal contact formation

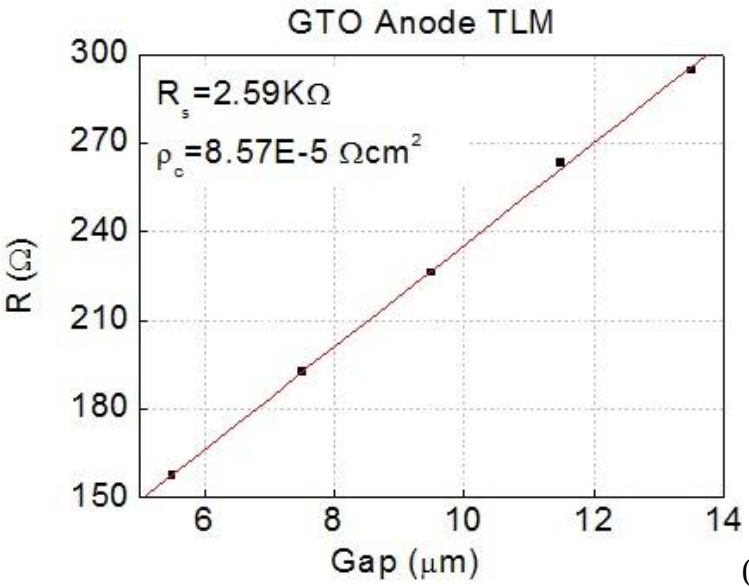
- **p-type 4H-SiC Ohmic contact**

The p-type anode Ohmic contact is an open challenging issue. One reason is the high energy barrier between the contact metal and the p-type 4H-SiC. Moreover, in 4H-SiC GTO, a large portion of the anode current flows vertically from the anode contacts to the cathode area. In this case, anode contact resistance is more determined by the specific contact resistance, independent of the metal contact area, because of the current crowding at the metal edge [51]. The anode Ohmic contact metal scheme was developed in this study, based on Ni/AlTi/Ni and RTA annealing. Ni/Al and Ni/Ti/Al Ohmic contact is reported to gives a good p-type Ohmic contact at vacuum annealing [52]. The first layer Ni is to react with SiC to form Ni_2Si at temperature as low as 500^{o}C. More Si vacancies are speculated to be available when Al diffused into the SiC surface during the high temperature annealing. Ti is added to avoid the melting of the Al-layer, and also to

prevent the formation of the un-reacted interfacial carbon atoms. The top Ni layer serves as a cap layer to prevent the oxidation of the AlTi layer in RTA process.



(a)



(b)

Fig. 4-10 (a) p-type Ohmic contact metal I-V measurement between 15 μm TLM pads and (b) p-type TLM test plot after 1000 °C annealing.

Fig. 4-10 (a) shows Ni(500Å)/AlTi(500Å)/Ni(1500Å) p-type Ohmic contact dependence on different annealing temperature, indicating that 1000 ^{o}C is necessary to obtain the optimum low contact resistance. An excellent p-type TLM measurement result after 1000 ^{o}C annealing for 5 minutes in the RTA system is shown in Fig. 4-10 (b), giving a specific contact resistance in the $10^{-5}\Omega.cm^{2}$ range. The anode contact formation is shown in Fig. 4-11.

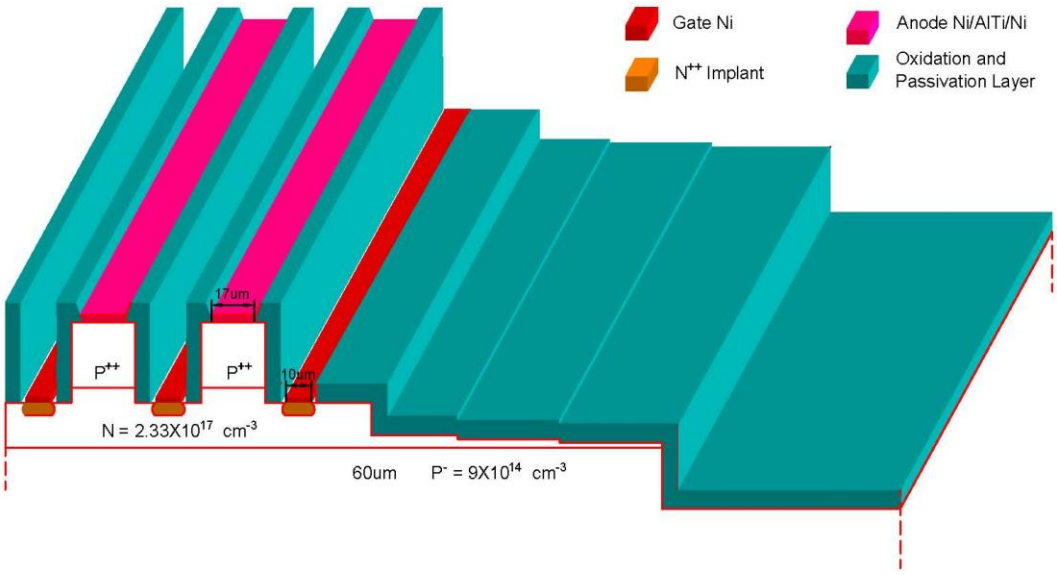


Fig. 4-11 Schematics of a 3D view on anode metal contact formation

4.1.7 Overlay Metallization and Dielectric Layer Filling

This fabrication step consists of three phases: (a) gate overlay metal formation (b) thick dielectric layer deposition and (c) anode overly metal formation.

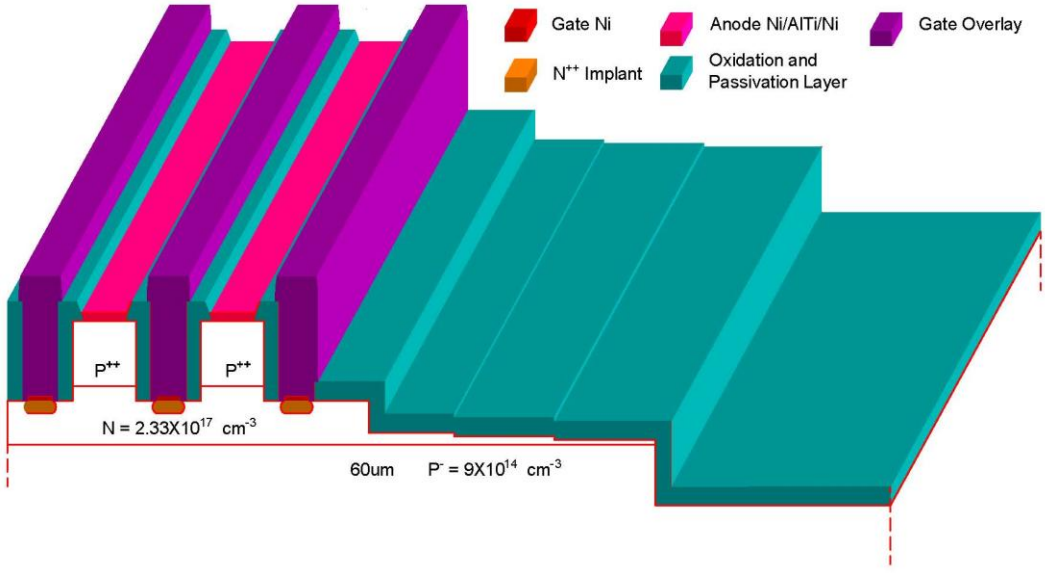
In order to reduce the gate series resistance, 3.5 μm Al was sputtered on the surface of a GTO wafer. Gate overlay pattern was then defined by a lithography process with the

mask of Gate Overlay and wet chemical etching using aluminum etchant, as shown in Fig. 4-12(a).

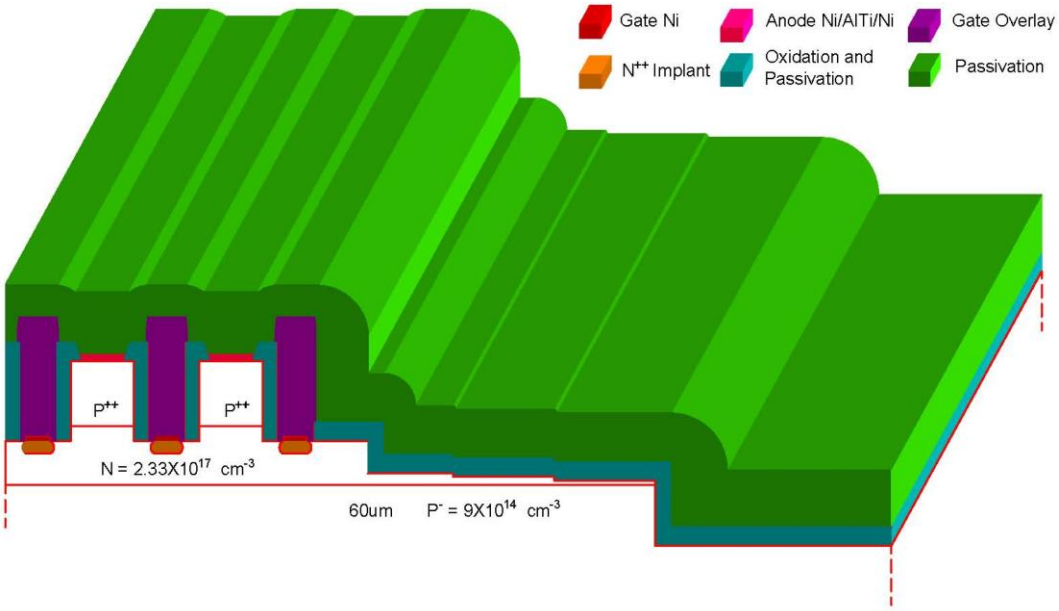
After gate overlay formation, a thick dielectric layer is formed by multiple layers of PECVD silicon dioxide and silicon nitride to prevent the top emitter overlay metal from contacting the gate overlay metal, shown in Fig. 4-12 (b).

The following step is to open windows in the dielectric layer for anode overlay metal deposition. Photolithography was done with mask "Anode Overlay", using AZ4400 photo resist. The dielectric layer was etched by ICP etching, using CF_4 plasma. The anode overlay metal Al/Au with the total thickness of 3.5 μm was deposited by sputtering on the sample surface. The metal was patterned by a lift-off process in a photo resist stripper. The anode overlay formation is shown in Fig. 4-12 (c). Finally, a gate pad was formed after photolithography with "Gate Pad", ICP drying etch, metal sputtering and lift-off to provide all electrical connections from gate overlays.

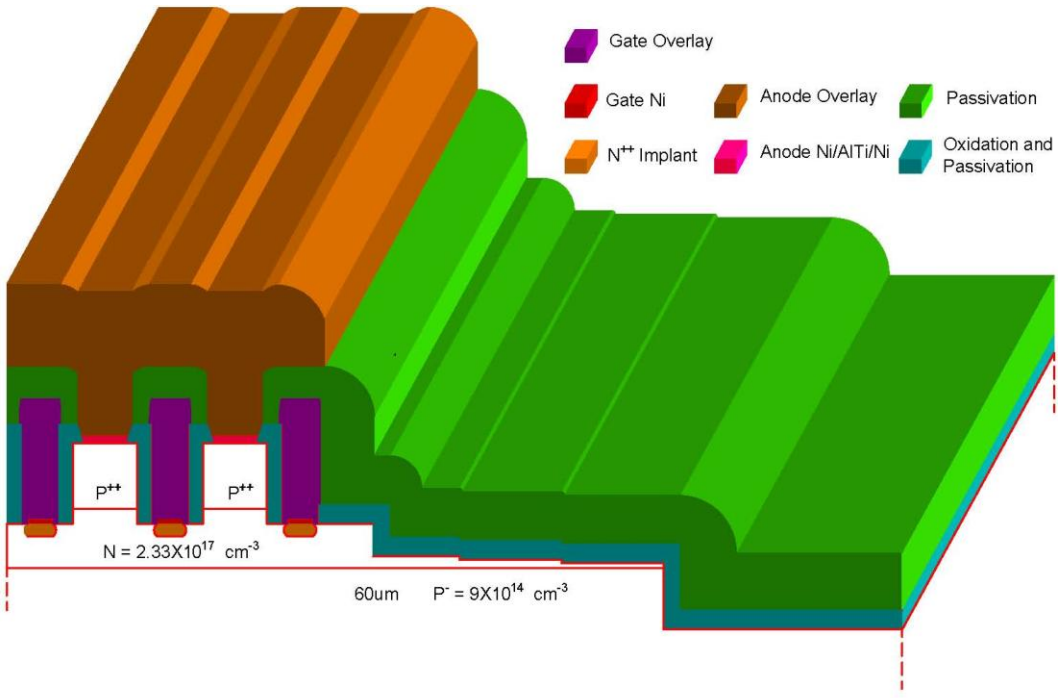
The last step of overlay metallization is cathode overlay, which is at the back side of the GTO wafer. After AZ4400 photo resist covering front side of the GTO wafer, the wafer was loaded into the ICP chamber with upside down to perform a two steps dry etching process, including O_2 plasma for 30 seconds to remove photo resist and the CF_4 plasma for 2 minutes to remove the dielectric layer. Then, the wafer was dipped into BOE for about 30 seconds to remove oxidation residual. A metal layer consisting of 1000 Å Ni and 1000 Å Au was sputtered on the back side the GTO wafer to finish overlay metal process. Fig. 4-13 shows a picture of a finished 3 inch SiC wafer with many GTO power devices.


Gate Ni
Anode Ni/AlTi/Ni
Gate Overlay
N++ Implant
Oxidation and Passivation Layer
P++
P++
N = 2.33X10^17 cm^-3
60um
P- = 9X10^14 cm^-3

(a)


Gate Ni
Anode Ni/AlTi/Ni
Gate Overlay
N++ Implant
Oxidation and Passivation
Passivation
P++
P++
N = 2.33X10^17 cm^-3
60um
P- = 9X10^14 cm^-3

(b)



(c)

Fig. 4-12 Schematics of 3D view on (a) gate overlay formation, (b) dielectric layer filling and (c) anode overlay formation

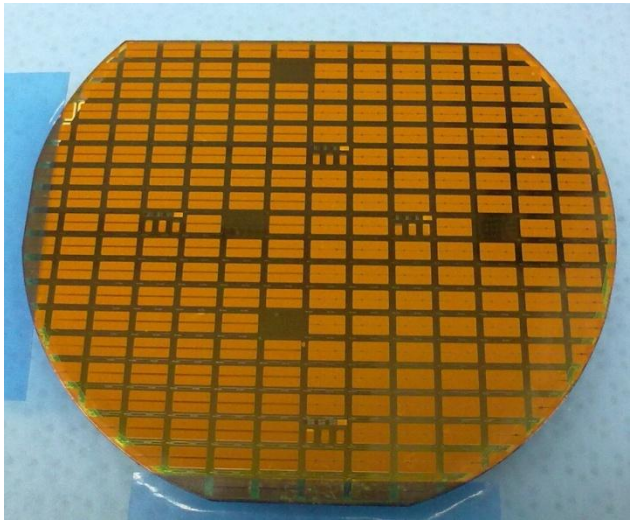


Fig. 4-13 Optical photo of a 3 inch SiC wafer after GTO devices fabrication

4.1.8 Package

After gold overlay on the bonding pads was completed, functional chips have been cut from the sample by a dicing saw. The chip is then mounted on a hermetic package by silver nano paste [53] followed by 325^{o}C curing for 1.5 hour. Then 1-mil thick gold wires are used for bonding. Refer Fig. 4-14 for packaged SiC power GTOs.

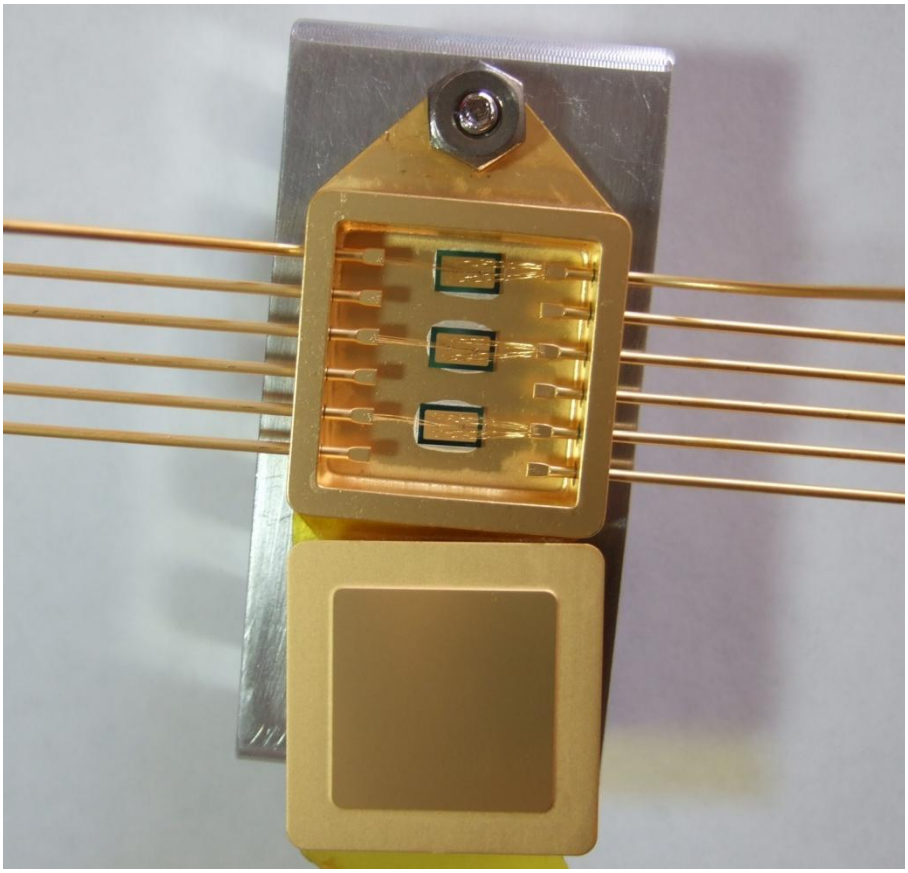


Fig. 4-14 An optical photo for the 4H-SiC power integrated circuits after packaging.

4.2 Device Characterizations

4.2.1 Off-State Characteristics

After fabrication, around 170 chips were tested at the wafer level at room temperature using a high-voltage probe station. The forward blocking characteristics of GTOs were measured by using a Glassman high-power voltage source and a Keithley 6517 digital electrometer. The measurement was done at room temperature by immersing the GTO wafer in Fluorient™. A histogram of the forward blocking voltage measured on devices is shown in Fig. 4-15. The blocking voltage mapping of 0.1 cm^2 GTOs is shown on Table 4-4. It is found that 63% of all 0.1 cm^2 devices blocked voltages in excess of 3 kV, with 28 devices blocking over 5 kV and 10 devices blocking over 6 kV. Generally, there is a larger variation on the blocking capabilities of 0.1 cm^2 GTO devices across the wafer. The reason for this is that a large device performance is limited by both wafer defects and process-introduced localized defects.

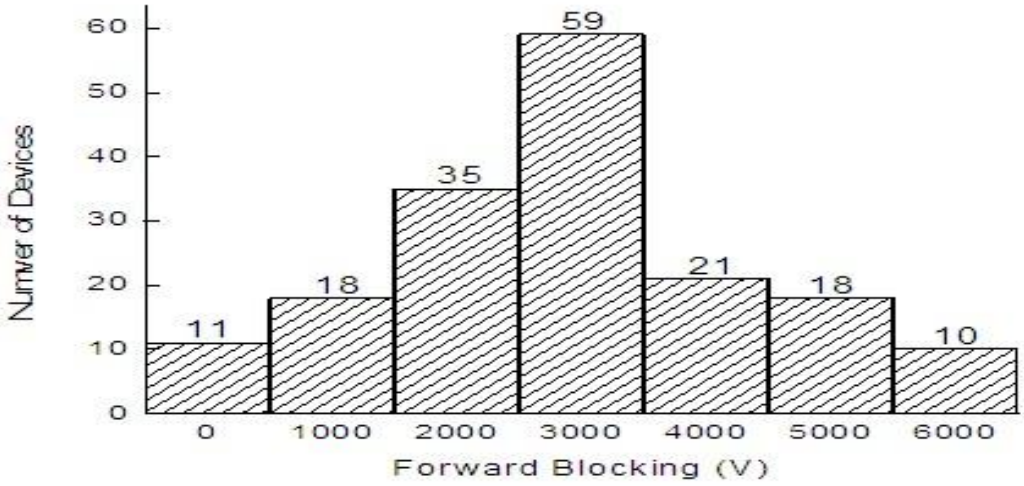
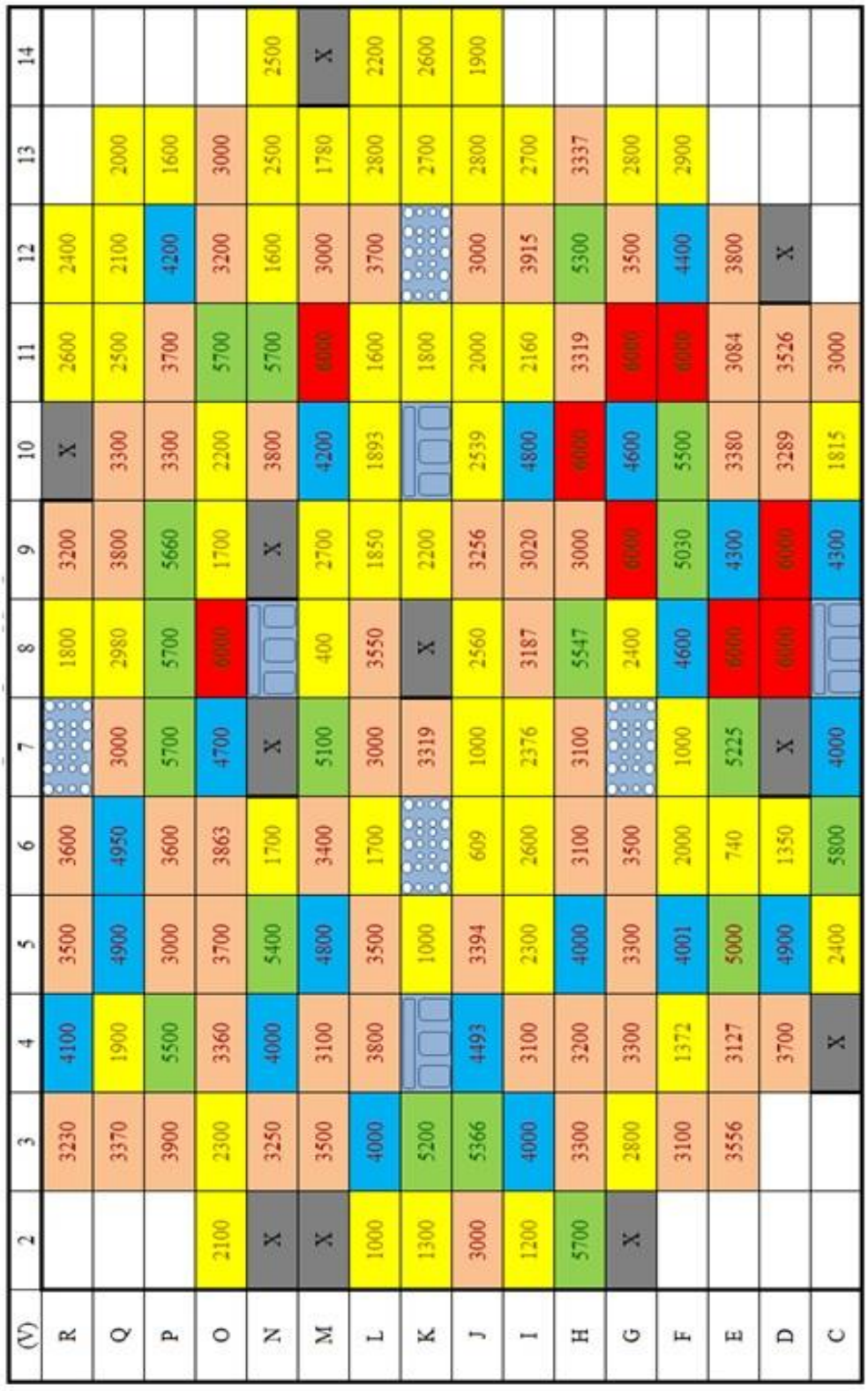


Fig. 4-15 Histogram of forward blocking voltages measured on 0.1 cm^2 GTOs.



(V)	2	3	4	5	6	7	8	9	10	11	12	13	14
R		3230	4100	3500	3600		1800	3200	X	2600	2400		
Q		3370	1900	4900	4950	3000	2980	3800	3300	2500	2100	2000	
P		3900	5500	3000	3600	5700	5700	5660	3300	3700	4200	1600	
O	2100	2300	3360	3700	3863	4700	6000	1700	2200	5700	3200	3000	
N	X	3250	4000	5400	1700	X		X	3800	5700	1600	2500	2500
M	X	3500	3100	4800	3400	5100	400	2700	4200	6000	3000	1780	X
L	1000	4000	3800	3500	1700	3000	3550	1850	1893	1600	3700	2800	2200
K	1300	5200		1000		3319	X	2200		1800		2700	2600
J	3000	5366	4493	3394	609	1000	2560	3256	2539	2000	3000	2800	1900
I	1200	4000	3100	2300	2600	2376	3187	3020	4800	2160	3915	2700	
H	5700	3300	3200	4000	3100	3100	5547	3000	6000	3319	5300	3337	
G	X	2800	3300	3300	3500		2400	6000	4600	6000	3500	2800	
F		3100	1372	4001	2000	1000	4600	5030	5500	6000	4400	2900	
E		3556	3127	5000	740	5225	6000	4300	3380	3084	3800		
D			3700	4900	1350	X	6000	6000	3289	3526	X		
C			X	2400	5800	4000		4300	1815	3000			

Table 4-4 The blocking voltage mapping on 4H-SiC GTO devices

Fig. 4-16 shows the forward current vs. blocking voltage for a 60 μm GTO that blocked over 6 kV. The measurement was done at room temperature by immersing the GTO in Fluorient^{TM} with a leakage current of less than 10^{-7} A (10^{-6} A/cm^2) at 6 kV. This represents more than 75% of the theoretical breakdown voltage of ~8kV for the p-epilayer used for fabrication.

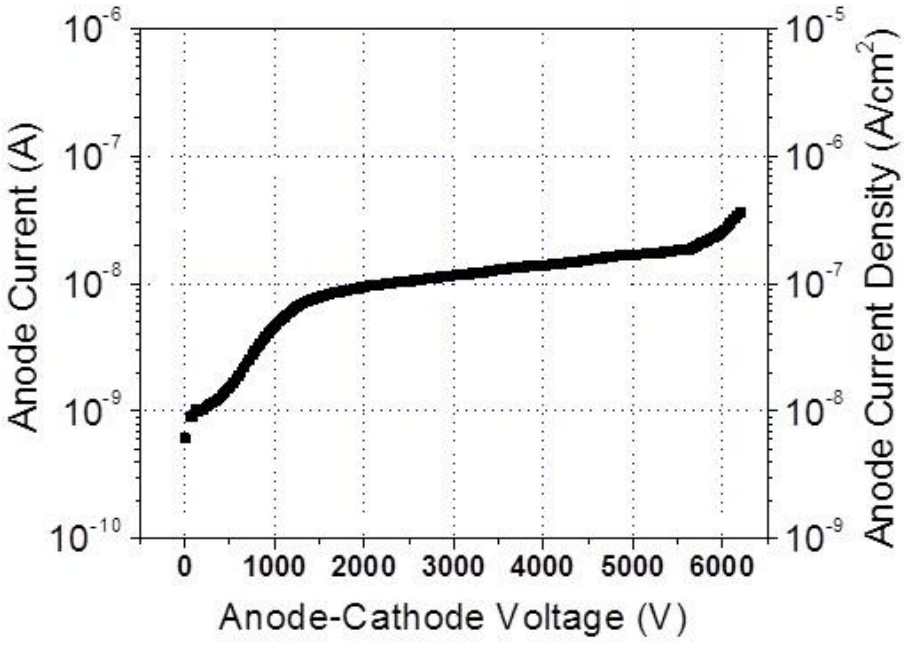
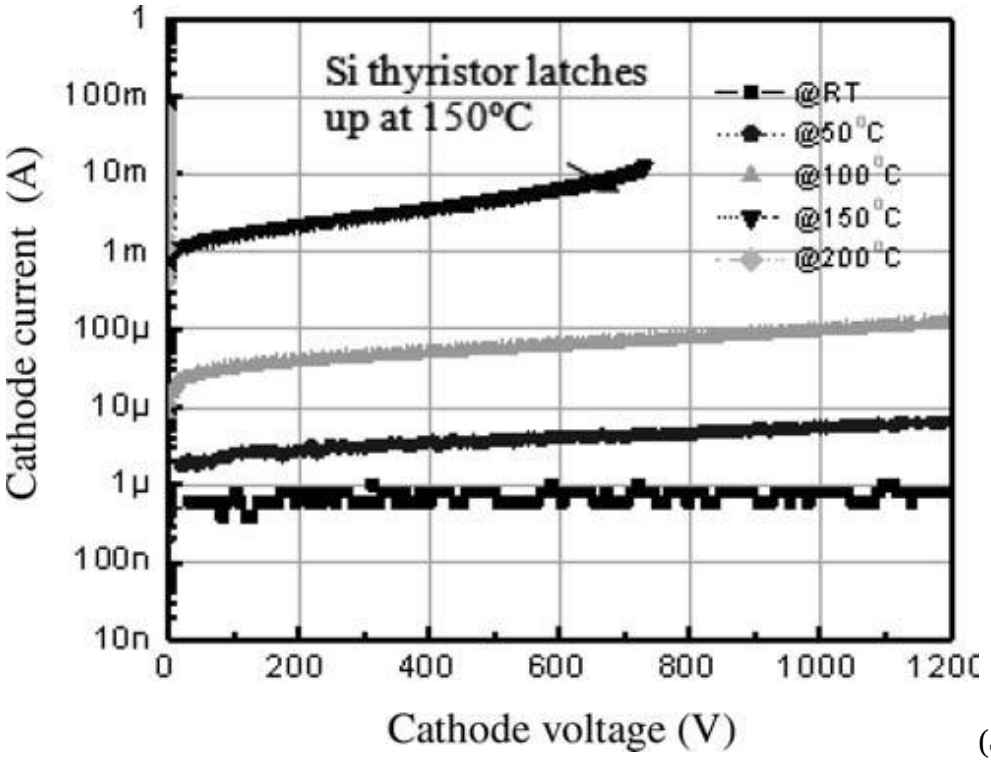


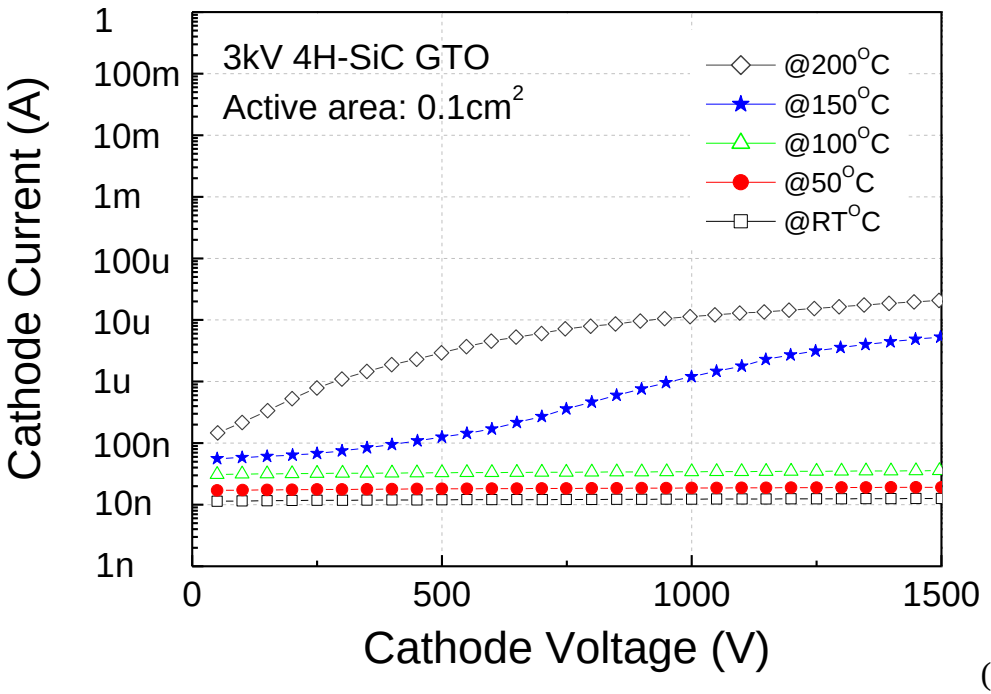
Fig. 4-16 Forward I-V curve of a GTO with for over 6kV blocking.

Due to the much lower intrinsic carrier concentration on SiC than that on Si, the power devices made on SiC exhibit a much lower leakage current even at the elevated temperatures. To compare the thermal runaway capability, the latch-up Si and SiC GTOs has been studied. A 50 A 3 kV SiC GTO with an active area of 0.1 cm^2 was mounted on a hot plate and measured in pulsed mode up to V_{AK} = 1500 V with a Tektronix 371B curve tracer. The leakage current through the device at 1500 V and the temperature of the hot

plate were monitored. The silicon thyristor catastrophically fails when it reaches a temperature of approximately 170 ℃ due to latch up induced by very high leakage currents – in excess of 100 mA [54]. On the other hand, the SiC GTO has been absolutely stable up to 200 ℃, with leakage currents below 100 μA. The leakage currents for Si and SiC Thyristors are shown in Fig. 4-17 (a) [12] and (b). The advantages of wide bandgap of SiC are clearly evident in the extremely low leakage currents of SiC thyristor, which stay low at elevated temperatures.



(a)



(b)

Fig. 4-17 The leakage currents for (a) Si and (b) SiC Thyristors at elevated temperatures.

4.2.2 On-State Characteristics

GTO chips were packaged in a customized package and the on-state static I-V characteristics are shown in Fig. 4-18. The packaged devices were measured in the pulsed mode up to I_{AK} = 50 A and gated with I_G = -0.25 A with a Tektronix 371B curve tracer. The forward voltage drop of V_{AK} = 5.74 V @ I_{AK} = 50 A (J_{AK} = 500 A/cm^2) was recorded including the lead and contact resistances. It shows that the GTO is capable of handling high pulse power with capability of at least 300kW power. Meanwhile, the differential on-resistance of Rsp-on = 4 mΩ-cm^2 illustrates that the GTO has significant conductivity modulation of the p-drift region and the achievement of low contact resistances, especially for the p+ anode contacts with specific contact resistance of 9 x 10^{-5} Ω·cm^2. At 500 A/cm^2 the anode contact contributes only 0.045 V to the total on-state voltage drop.

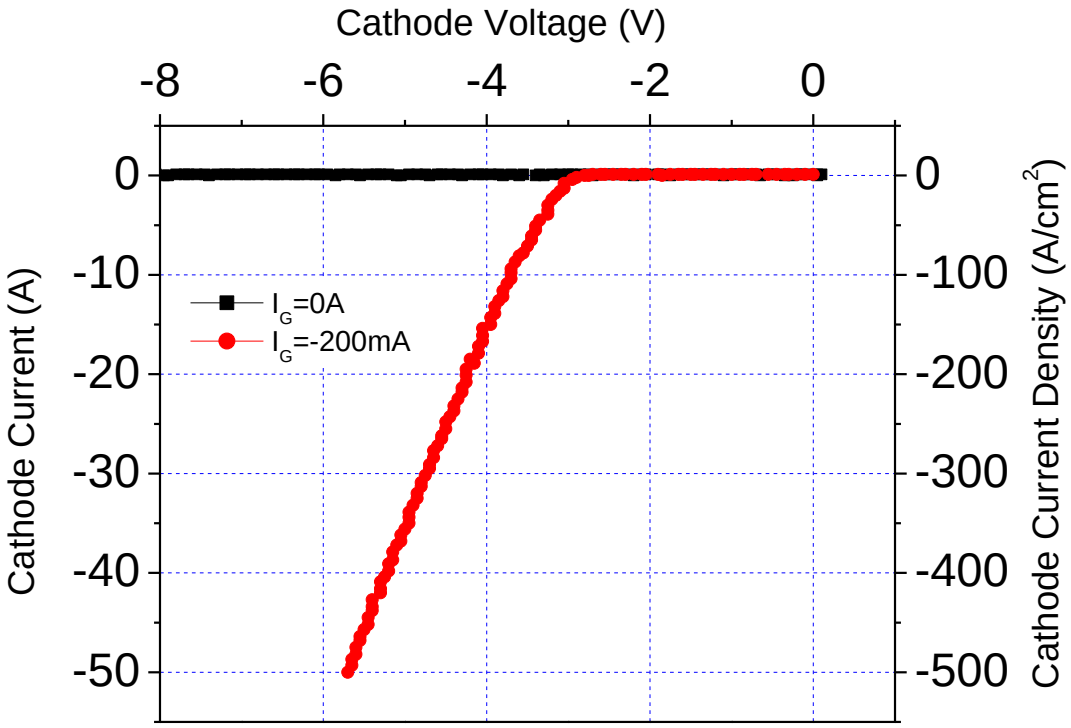


Fig. 4-18 Static IV characteristics. Insert shows the packaged GTO devices for tests.

The 4H-SiC GTOs exhibit excellent high temperature forward conduction characteristic due to the bidirectional carrier injection and conductivity modulation. The forward conduction characteristics are shown in Fig. 4-19 as a function of temperature. At 20 A of the anode current (~200 A/cm^2), the forward voltage drop of the SiC GTO increases from 5.2 V at 25 ^{o}C to 5.5 V at 225 ^{o}C with I_G = -200 mA. The voltage drop increases with temperature as a consequence of reduced mobility. A very useful feature of this device is that at high current densities (more than 200 A/cm^2), a positive temperature coefficient in the differential on-resistance is obtained which allows for a stable parallel operation to achieve a high current handling capability.

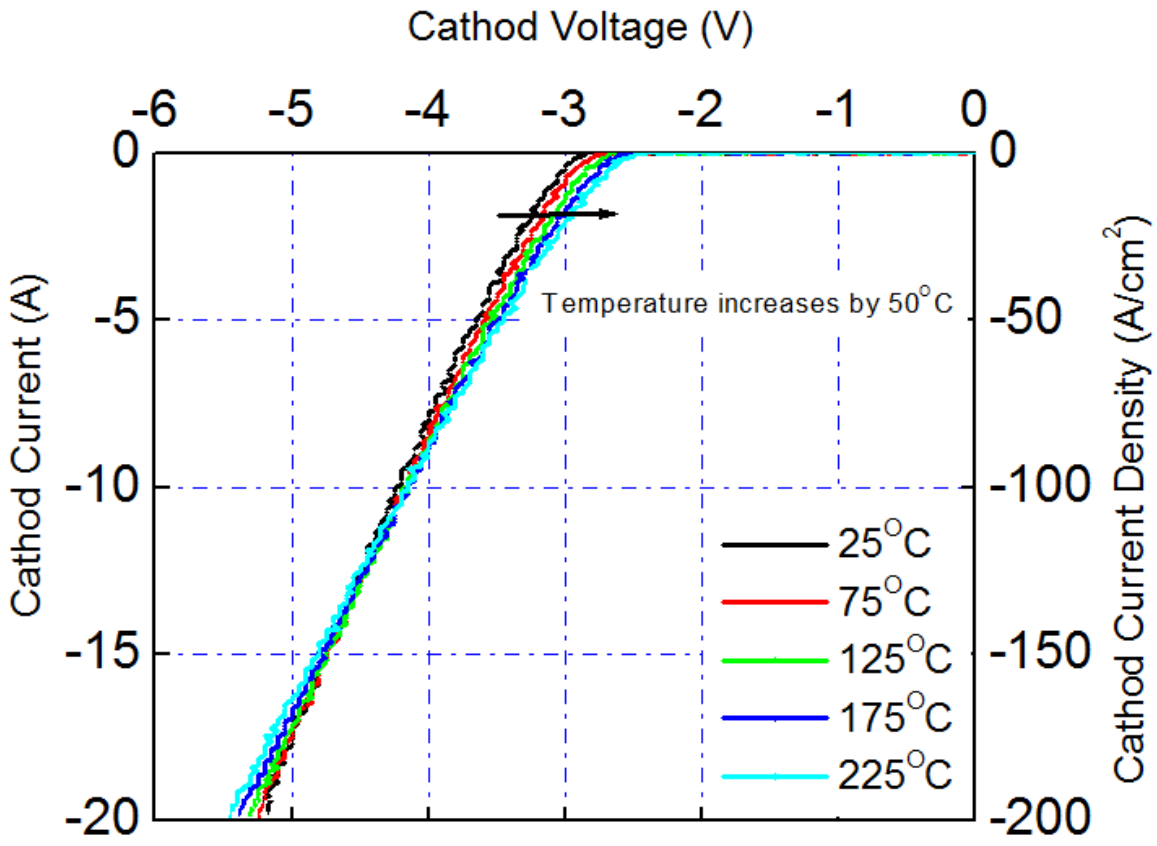


Fig. 4-19 Output characteristics of a 2 kV SiC GTO at different temperature with I_G = -20 mA. Device active area: 0.1 cm^2.

4.2.3 Dynamic Characteristics

A negative voltage pulse with pulse duration of 4 μs was applied to turn on the GTO with an anode to cathode bias, and a positive pulse was used to turn off the device. The testing setup is illustrated in Fig. 4-20. The gate current I_G, gate-anode voltage V_{GA}, cathode current I_K, and anode-cathode voltage V_{AK}, were monitored by a Tektronix multi-channel oscilloscope. The switch-on current was limited in the testing circuit to avoid a premature device failure by adjusting the value of power resistance R. For 18 A, 800 V switching tests, the value of R is 46.2 Ω.

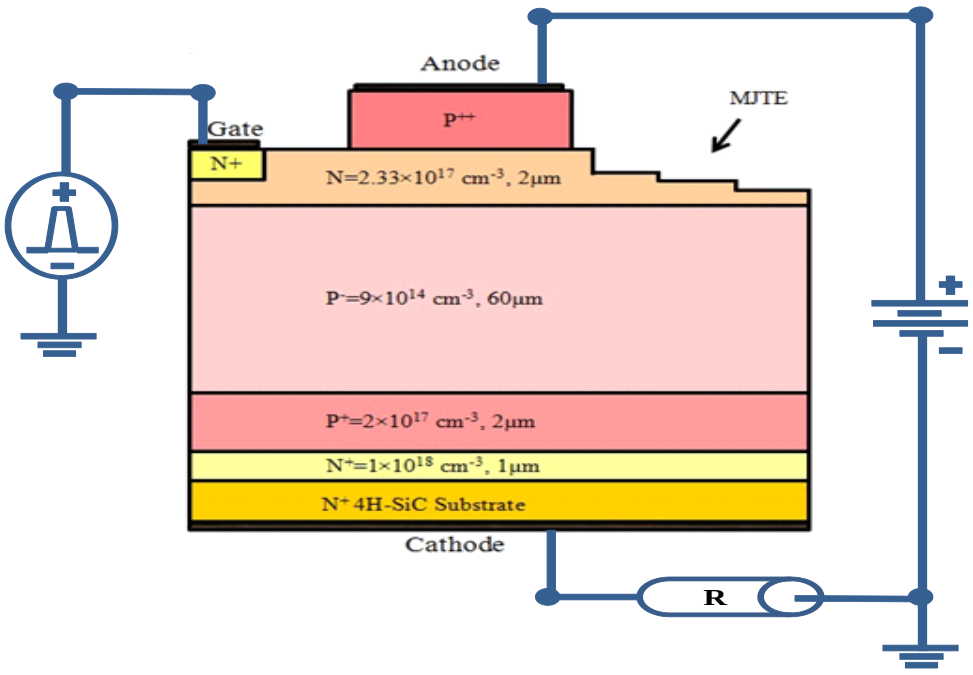


Fig. 4-20 GTO switching testing circuit.

The switching testing result is shown in Fig. 4-21. The top trace represents the cathode current of the device, which conducts 18 A when the device is on. The second trace from the top is the gate current. The third and fourth traces from the top represent the voltage of gate and the voltage of anode to cathode, respectively. The device could be turned-on when a 1 A current was applied to the gate. An on-current of 18 A and a rise time of less than 0.2 μs has been observed. Turn-off of the device has been demonstrated by reverse biasing of the gate-anode p-n junction. The peak gate turn-off current is 13 A, which is 72% of the controllable current. Therefore the current gain (β) is around 1.4. The maximum turn-off gain (β_m, defined by Eq. 4-7) can be enhanced by reducing the injection efficiency of the bottom npn transistor in the GTO. It is from Eq. 4-7 that the advantage of the P+ buffer layer is most easily seen, since it acts to reduce the injection

efficiency (and thus the base transport factor) of the bottom npn transistor. Although decreasing α_{npn} increase β_m, one disadvantage is that it increases V_F.

$$\beta_m = \frac{\alpha_{\mathrm{pnp}}}{\alpha_{pnp} + \alpha_{\mathrm{npn}} - 1} \qquad \text{Eq. 4-7}$$

The 18 A current was turned off at a V_{AK} of 800 V (DC), which corresponds to a current density of 180 A/cm^2. The resulting fall time was a little bit longer and was about 0.4 μs. The switching time of commercially available 6 kV Silicon GTOs is an order of magnitude slower, and operated at a lower current density of about 45 A/cm^2. The 4H-SiC GTO could be repeatedly turned on and off in a rapid succession at the room temperature while the temperature of the testing die was naturally heated to much higher than the room temperature. This shows the potential of higher temperature capability of the SiC GTO which allows significantly higher number of shots. This is crucial for applications such as rapid firing rail guns.

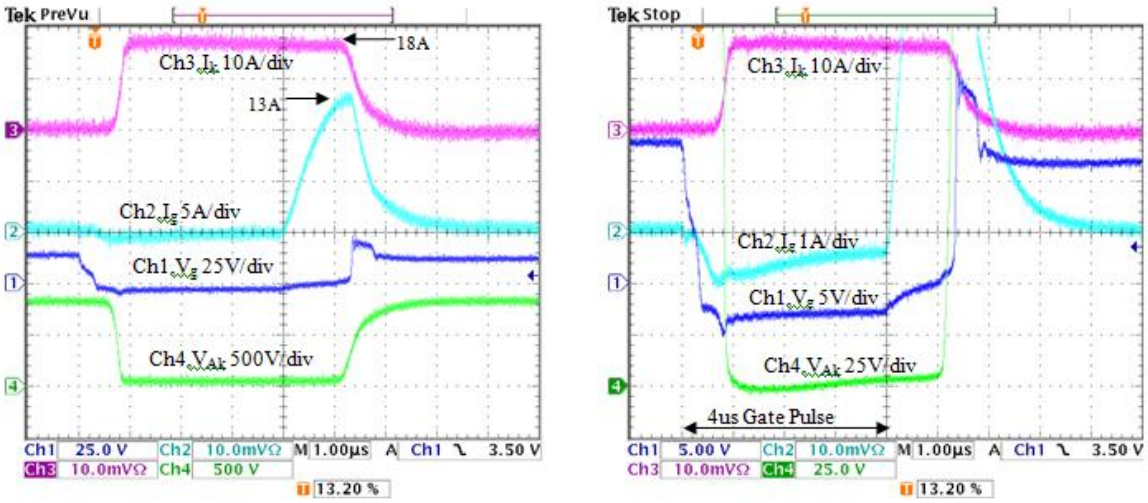


Fig. 4-21 Hard-switching with a resistive load at 800 V-18 A (left) and detailed wave-forms (right)

4.3 Summary

0.1 cm^2 SiC asymmetrical GTOs have been designed and fabricated with MJTE utilized successfully. The maximum blocking voltage above 6 kV with lower than10^{-7} A (10^{-6} A/cm^2) leakage current was realized for the GTO with a blocking layer thickness equal to 60 μm. Excellent turn-on and turn-off characteristics were noted for an anode current of 18 A (180 A/cm^2) with a turn-off time of 0.4 μs and turn-off gain of 1.4. The superiority of switching time and peak current handling capability makes the SiC GTOs a promising candidate for high power application. The GTO fabricated in this work were distinguished by their low Rsp-on = 4 mΩ-cm^2 (normalized to the active area), greater than 75% of the theoretical breakdown voltage and fast switching.

CHAPTER 5 SUMMARY AND FUTURE WORK SUGGESTIONS

5.1 Conclusion

This dissertation briefly reviews the SiC materials properties, 4H-SiC bipolar switching devices, and edge termination extension technologies in Chapter 1. The Physics-based MJTE design and optimization by using numerical simulations has been studied in Chapter 2. The GTO structure design, simulation and mask design were then described in Chapter 3. The fabrication of GTOs was successful and devices with a superior performance were demonstrated in Chapter 4. The major achievements of this thesis work include:

[1] Using 2-D numerical simulations, 3-step MJTE techniques for 4H-SiC power devices have been investigated. Compared with 1- and 2-step MJTE, 3-step MJTE design can improve the blocking performance, balance electric-field, and decrease the sensitivity of the breakdown voltage to JTE etching depth while keeping the total JTE length constant. The simulation results were confirmed by fabrication of the 3-step JTE NPN structure with the maximum blocking voltage of 7630 V, which is 90% of the ideal breakdown voltage. The design methodologies discussed in this study are believed to be useful in designing the edge terminations structures for other ranges of breakdown voltages.

[2] 0.1 cm^2 SiC asymmetrical GTOs have been designed and fabricated with the MJTE utilized successfully. The maximum blocking voltage above 6 kV with the lower than10^{-7} A (10^{-6} A/cm^2) leakage current was realized for the GTO with a blocking layer thickness equal to 60 μm. Excellent turn-on and turn-off characteristics were noted for an anode current of 18 A (180 A/cm^2) with a turn-off time of 0.4 μs and

turn-off gain of 1.4. The superiority of the switching time and peak current handling capability makes the SiC GTOs a promising candidate for high power applications. The GTOs fabricated in this work have been distinguished by their low Rsp-on = 4 mΩ-cm^2 (normalized to the active area), more than 75% of theoretical breakdown voltage, and fast switching.

5.2 Suggestion for Future Work

For GTOs, Between the GATE and ANODE is a PN junction, which needs to be fully forward biased to cause a large current to go through GTO. Hence, GTO is a current controlled device. GTO is often used with a unity gain, i.e., GATE current is the same as the GTO switch current. For a GTO current of 500 amp, it will require near 500 amp current to "gate" or control the current (i.e. unity gain, especially if higher switching speed is desired). A gate circuitry handling 500amp at high speed is itself bulky and costly as well as energy consuming. SiC IGBT uses a metal/oxide (MOS) gate to control the current through the channel. The MOS gate, however, has serious problems due to hot carrier trapping in the oxide, which causes a VTH drift and ultimate oxide rupture, and low channel carrier mobility due to interface and near interface charge scattering [55].

It needs a new design on power bipolar switching device, which will be able to combine the best features of SiC GTOs (free of gate oxide reliability and V_{TH} drift) and SiC IGBTs (voltage gating without a high gate current) to get rid of the high gate current. If such a switch can be conceived and developed, such a new power switch would solve the problems of both SiC IGBTs and GTOs and can be expected to find very widespread applications, not just limited to utility scale inverters.

Voltage-Gated Bipolar Transistor (VGBT), shown in Fig. 5-1, combines the best features of GTO and IGBT while eliminating the weaknesses of SiC GTO and IGBT: VGBT vertical channel width is "gated" or controlled by the GATE-COLLECTOR PN junction exactly as in a junction field effect (JFET) transistor. The self-aligned formation of the vertical N+ side walls makes VGBT normally-off and with extremely high channel carrier mobility (more than 500 $cm^2/V/s$ [56], unlike ~15 to 30 cm2/V/s [57] in SiC IGBTs or MOSFETs). The conceptual breakthrough of VGBT lies in the realization that a buried N+ COLLECTOR (buried under SiO_2) would make bipolar mode voltage-gated power switch possible for the first time without using the MOS gated structure, which would overcome the shortages of both IGBT and GTO.

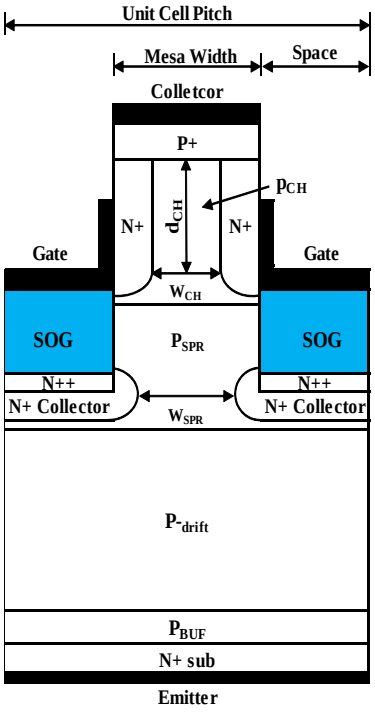


Fig. 5-1 Cross sectional view of normally-off SiC VGBT

REFERENCE

[1] B. J. Baliga, “Fundamentals of Power Semiconductor Devices”, Springer, New York, 2008.

[2] B. J. Baliga, "Semiconductors for high-voltage, vertical channel FET’s," J. Appl. Phys, vol. 53, pp. 1759–1764, 1982.

[3] T. Paul Chow, “High-voltage SiC and GaN power devices”, Microelectronic Engineering, Vol. 83, pp.112-122, 2006.

[4] M. N. Yoder, “Wider bandgap semiconductor materials and device”, IEEE Transactions on Electron Devices, Vol. 43, No. 10, pp. 1633-1636, 1996.

[5] H. Shiomi, Crystal growth of diamon and its application for semiconductor devices, Electronics and Communications in Japan, Part 2, vol. 82, No. 7, pp. 68-79, 1999.

[6] S. E. Saddow and A. Agarwal, “Advances in Silicon Carbide processing and Application (Artech Hourse, 2004), pp. 177.

[7] J. A. Cooper and A.K. Agarwal, “SiC power switching devices-the second electronics revolutions?”, Proc. IEEE 90, pp. 956-968, 2002.

[8] J. Zhang, Y. Luo, P. Alexandrov, L. Fursin, and J. Zhao, “A high current gain 4H-SiC NPN power bipolar junction transistor, IEEE Electron Device Lett, Vol.24, pp.327-329, 2003.

[9] J. H. Zhao, J. Zhang, P. Alexandrov, X. Li, and T. Burke, “A high voltage (1750 V) and high current gain (24.8) 4H-SiC bipolar junction transistor using a thin (12 μm) drift layer”, Mater. Sci. Forum Vol. 457-460, pp.1173-1176, 2003.

[10] S. Balachandran, T. P. Chow, A. Agarwal, C. Scozzie, and K. A. Jones, “4 kV 4H-SiC epitaxial emitter bipolar junction transistors”, Proceedings of the 17th International Symposium on Power Semiconductor Devices & ICs (ISPSD), 2005, pp. 291–294.

[11] Qingchun (Jon) Zhang, Robert Callanan, Anant Agarwal, Albert Burk, Michael O Loughlin, John Palmour, and Charles Scozzie, “10 kV, 10 A bipolar junction transistors and darlington transistors on 4H-SiC”, Mater. Sci. Forum Vol. 645-648, pp.1025-1028, 2003.

[12] Qingchun (Jon) Zhang and Anant K. Agarwal, “Design and technology considerations for SiC bipolar devices: BJTs, IGBTs, and GTOs”, Phys. Status Solidi A, Vol. 206, No. 10, pp. 2431-2456, 2009.

[13] Q. Zhang, A. Burk, F. Husna, R. Callanan, A. Agarwal, J. Palmour, R. Stahlbush,

and C. Scozzie, “4H-SiC bipolar junction transistors: From research to development - A case study: 1200 V, 20 A, stable SiC BJTs with high blocking yield”, presented at ISPSD’09, Barcelona, Spain, June 14-17, 2009.

[14] Q. Zhang, C. Jonas, J. Sumakeris, A. Agarwal, and J. Palmour, “12 kV 4H-SiC p IGBTs with record low specific on-resistance”, International Conference on Silicon Carbide and Related Materials (ICSCRM), Otsu, Japan, 14-19 October 2007.

[15] M. Das, Q. Zhang, R. Callanan, C. Capell, J. Clayton, M. Donofrio, S. Haney, F. Husna, C. Jonas, J. Richmond, and J. J. Sumakeris, “A 13 kV 4H-SiC N-Channel IGBT with low $R_{diff,on}$ and fast switching”, International Conference on Silicon Carbide and Related Materials (ICSCRM), Otsu, Japan, 14-19 October 2007.

[16] Y. Sui, X. Wang, and J. A. Cooper, “High-voltage self- aligned p-channel DMOS-IGBTs in 4H-SiC”, IEEE Electron Device Lett. Vol. 28, pp. 728-730, 2007.

[17] Yu, L.C., Dunne, G.T., Matocha, K.S., Cheung, K.P., Suehle, J.S., Kuang Sheng, "Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments", Device and Materials Reliability, IEEE Transactions on, On page(s): 418 - 426, Volume: 10 Issue: 4, Dec. 2010.

[18] M. Treu, R. Rupp, P. Blaschitz, K. Rüschenschmidt, Th. Sekinger, P. Friedrichs, R. Elpelt, D. Peters, “Strategic considerations for unipolar SiC switch options: JFET vs. MOSFET”, Industry Applications Conference, 2007. 42nd IAS Annual Meeting.

[19] A. J. Lelis, R. Green, D. Habersat, and N. Goldsman, "Effect of on-state stress on SiC DMOSFET subthreshold I-V characteristics, " Materials Science Forum, vols. 645-648, pp. 983-986, Apr. 2010.

[20] Gurfinkel, M., Horst, J.C., Suehle, J.S., Bernstein, J.B., Shapira, Y., Matocha, K.S., Dunne, G., Beaupre, R.A., "Time-dependent dielectric breakdown of 4H SiC MOS capacitors", Device and Materials Reliability, IEEE Transactions on, On page(s): 635 - 641, Volume: 8 Issue: 4, Dec. 2008.

[21] S. H. Ryu, S. Krishnaswami, B. Hull, J. Richmond, A. Agarwal, and A. Hefner, “10 kV, 5A 4H-SiC power DMOSFET,” Power Semiconductor Devices and IC’s, 2006. IEEE International Symposium on, ISPSD ’06, IEEE, June 2006, pp. 1–4.

[22] M. Das, Q. Zhang, R. Callanan, C. Capell, J. Claytou, M. Donfrio, S. Haney, F. Husna, C. Jonas, J. Richmond, and J. J. Sumakeris, “A 13 kV 4H-SiC n-channel IGBT with low $R_{diff,on}$ and fast switching,” Int. Conf on Silicon Carbide and Related Mat. 2007 (ICSCRM), Oct. 2007, pp. 1183–1186.

[23] A. K. Agarwal, J. B. Casady, L. B. Rowland, S. Seshadri, R. R. Siergiej, W. F. Valek, and C. D. Brandt, “700-V asymmetrical 4H-SiC gate turn-off thyristors (GTO’s),” IEEE Electron Device Letters, v. 18, No. 11, pp. 518-520, November 1997.

[24] P. A. Ivanov, M. E. Levinshtein, S. L. Rumyantsev, A. K. Agarwal, and J. W. Palmour "Turn-off operation of a MOS-gate 2.6 kV 4H-SiC GTO thyristor" Solid- State Electronics, v. 44, N 12, pp. 2155-2159, 2000.

[25] A. K. Agarwal, P.A. Ivanov, M.E. Levinshtein, J.W. Palmour, and S. L. Rumyantsev "Dynamic performance of GTO thyristors", International Conference on Silicon Carbide and Related Materials ICSCRM 2001, Oct. 28 – Nov. 02, 2001, Ibaraki, Japan, pp. 660-661.

[26] A. Agarwal, C. Capell, Q. Zhang, J. Richmond, R. Callanan, M. O'Loughlin, A. Burk, J. Melcher, J. Palmour, V. Temple, H. O¢Brien and C. J. Scozzie,"9 kV, 1 cm×1 cm SiC super GTO technology development for pulse power", Pulsed Power Conference, 2009. PPC '09. IEEE , pp 264 – 269.

[27] M. O'Loughlin, K. Irvine, J. Sumakeris, M. Armentrout, B. Hull, C. Hallin, and A.Burk, Jr., "Silicon carbide hot-wall epitaxy for lLarge-area, high-voltage devices", Mater. Res. Soc. Symp. Proc. Vol. 1069, 2008.

[28] V. Saxena, J. N. Su, and A. J. Steckl, "High-voltage Ni– and Pt–SiC Schottky diodes utilizing metal field plate termination," IEEE Trans Electron Dev, 46 (1999) 456–464.

[29] D.C. Sheridan, G. Niu, J. N. Merrett, J. D. Cressler, C. Ellis, C. C. Tin, "Design and fabrication of planar guard ring termination for high-voltage SiC diodes", Solid-State Electron, 44 (2000) 1367-1372.

[30] D. C. Sheridan, G. Niu, J. D. Cressler, "Design of single and multiple zone junction termination extension structures for SiC power device", Solid-State Electronics 45 (2001) 1659-1664.

[31] R. Ghandi, B. Buono, M. Domeij, G. Malm, C. M. Zetterling and M. Ostling, "High voltage 4H-SiC PiN diodes with etched junction termination extension", IEEE Electron Dev Lett, 30 (2009) 1170-1172.

[32] X. Li, K. Tone, L. Fursin, J.H. Zhao, T. Burke, P. Alexandrov, M. Pan and M. Weiner, "Multistep junction termination extension for Sic power devices", Electron Lett, 37 (2001) 392-393.

[33] Synopsys TCAD Sentaurus 2-D and 3-D device simulator (2008–09).

[34] B. J. Baliga, "Modern Power Devices", New York: Wiley, 1987.

[35] V.A.K. Temple, W. Tantraporn, "Junction termination extension for near-ideal breakdown voltage in p-n junctions", IEEE trans Electron Dev, 33(10) (1986) 1601-1608.

[36] D. Planson, M. L. Locatelli, S. Ortoland, J. P. Chante, H. Mitlehner, D. Stephani, "Periphery protection for silicon carbide devices: state of the art and simulation",

Materials Science and Engineering, B46 (1997) 210-217.

[37] X. Li, K. Tome, L. Cao, P. Alexandrov, L. Fursin, and J. Zhao, "Theoretical and experimental study of 4H-SiC junction edge termination", Material Science Forum, 338-342 (2000) 1374-1378.

[38] L. Cao, "4H-SiC Gate Turn-off Thyristor and Merged P-i-N and Schottky Barrier Diode" Doctoral Dissertation, Department Electrical and Computer Engineering: Rutgers University, 2000.

[39] Q. J. Zhang, A. Agarwal, C. Capell, L. Cheng, M. O'Loughlin, A. Burk, J. W. Palmour, S. Rumyantsev, T. Saxena, M. Levinshtein, A. Ogunniyi, H. O′Brien and C. J. Scozzie, "12 kV, 1 cm^2 SiC GTO thyristors with negative bevel termination", Materials Science Forum, Vol. 717-720, pp.1151-1154, 2012.

[40] L. Lin and J. Zhao "Fabrication and characterization of 4H-SiC 6kV gate turn-off thyristor", Materials Science Forum, Vol. 717-720, pp.1163-1166, 2012.

[41] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices", IEEE Transactions on electron devices, vol ED-40, pp. 645-655, 1993.

[42] A. O. Konstantinov, Q. Wahab, N. nordell and U. Lindefelt, "Ionization rates and critical electric field in 4H silicon carbide", Applied Physics Letters, Vol. 71, pp.90-92, 1997.

[43] B. J. Balliga, "Power Semiconductor Devices", PWS Publishing Company, 1995.

[44] K. A. Reinhardt, and W. Haber, "Handbook of Silicon Wafer Cleaning Technology", 2nd edition, William Andrew, Norwich, 2008

[45] J. Sugiura, W. J. Lu, K. C. Cadien, and A. J. Steckl, "Reactive ion etching of SiC thin films using fluorinated gases", Journal of Vacuum Science and Technology B, 4 (1) pp. 349-354, 1986

[46] K. Tone, "Silicon Carbide Vertical Junction Field-Effect Transistors," Doctoral Dissertation, Department Electrical and Computer Engineering: Rutgers University, 2002.

[47] C. M. Zetterling, Process Technology for silicon carbide devices, IEE Inspect, London, 2002

[48] J. R. Williams, et al, "Passivation of the 4H-SiC/SiO2 interface with nitric oxide", Materials Science Forum, vols. 389-393, pp. 967-972, 2002

[49] J. Campi, Y. Shi, Y. Luo, F. Yan and J. H. Zhao, "Study of interface state density and effective oxide charge in post-metallization annealed SiO2/SiC structure", IEEE Trans on Electron Devices, Vol. 46, No. 3, pp. 511-519, 1999.

[50] J. Zhang, “Design and fabrication of 4H silicon carbide power bipolar junction transistors,” Doctoral Dissertation, Department Electrical and Computer Engineering: Rutgers University, 2006.

[51] Helmuth Murrmann, Dietrich Widmann, “Current crowding on metal contacts to planar devices”, IEEE Trans. Electron Devices, Vol. 264-268, pp. 1022-1024, 1969.

[52] Ryohei Konishi, Ryuichi Yasukochi, Osamu Nakatsuka, Yasuo Koide, Miki Moriyama, Masanori Murakami, “Development of Ni/Al and Ni/Ti/Al Ohmic contact materials for p-type 4H-SiC”, Materials Science and Engineering B98, pp. 286-293, 2003.

[53] J. G. Bai, Z. Z. Zhang, J. N. Calata, and G. Q. Lu, "Low-temperature sintered nanoscale silver as a novel semiconductor device-metallized substrate interconnect material," Components and Packaging Technologies, IEEE Transactions on [see also Components, Packaging and Manufacturing Technology, Part A: Packaging Technologies, IEEE Transactions on], vol. 29, pp. 589-593, 2006.

[54] Qingchun Zhang and Anant K. Agarwal, “Design and technology considerations for SiC bipolar devices: BJTs, IGBTs, and GTOs,” Phys. Status Solidi A Vol. 206, pp2431-2456, 2009.

[55] J. Wu, J. Hu, J. H. Zhao, X. Wang, X. Li, L. Fursin, and T. Burke, “Normally-off 4H-SiC trench-gate MOSFETs with high mobility,” Solid State Electronics, Vol. 52, pp. 909-913, 2008.

[56] P. Sannuti, X.Li, F.Yan, K. Sheng and J.H.Zhao, “Channel electron mobility in 4H-SiC lateral junction field effect transistors”, International Journal of Solid-State Electronics, Vol. 49, No. 12, pp. 1900-1904, 2005.

[57] J. Wu, J. Hu, J. H. Zhao, X. Wang, X. Li, L. Fursin, and T. Burke, “Normally-off 4H-SiC trench-gate MOSFETs with high mobility,” Solid State Electronics, Vol. 52, pp. 909-913, 2008.

CURRICULUM VITA

Lei Lin

09/2007-10/2013	Ph.D. in Electrical and Computer Engineering Rutgers, The State University of New Jersey New Brunswick, New Jersey, USA
09/2011-10/2012	M.S. in Mathematics Rutgers, The State University of New Jersey New Brunswick, New Jersey, USA
09/2006-05/2007	Graduate studies in Electrical Engineering University of Oklahoma Norman, Oklahoma, USA
07/2005-06/2006	Process Integration Engineer in Fab 3 Advanced Semiconductor Manufacturing Corporation Shanghai, China
04/2004-06/2005	Process Integration Engineer in TD center Semiconductor Manufacturing International Corporation Shanghai, China
09/2001-03/2004	M.S. in Material Science and Engineering Zhejiang University Hangzhou, Zhejiang, China
09/1997-06/2001	B.S. in Material Science and Engineering Jilin University Changchun, Jilin, China

PUBLICATIONS

1. **Lei Lin** and Jian Zhao, "Simulation and Experimental Study on the 3-Step Junction Termination Structure for High-Voltage 4H-SiC GTOs", Solid State Electronics, 86, 2013, page 36-40.

2. Jun Hu, **Lei Lin,** Xiaobin Xin, Jian H. Zhao and David K. Gaskill, "Demonstration of 4H-SiC Ultraviolet Avalanche Phototransistor", (Manuscript in preparation).

3. **Lei Lin** and Jian Zhao, "Fabrication and Characterization of 4H-SiC 6kV Gate Turn-Off Thyristor", MSF 717-720, 2012, page 1163-1165.

4. Petre Alexandrov, Jianhui Zhang, **Lei Lin**, Leonid Fursin, Xueqing Li, Xiaohui Wang, Christopher Dries, Jian H. Zhao, Terence Burke, Fritz Kub, "Development of silicon carbide high-voltage switches for power converters and solid-state disconnects", GOMACTech–11 Government Microcircuit Applications and Critical Technology Conference @ Orlando, FL, USA, 2011, page 167-170.

5. Jingru Zhang, Shaurya Prakash, Yogesh Jaluria, and **Lei Lin**, "An experimental study on the effect of configuration of multiple microchannels on heat removal for electronic cooling", Proceedings of the International Heat Transfer Conference @ Washington D.C., USA August 8-13, 2010, page 1-8

6. **Lei Lin**, Xiangyang Ma, Ling Zhong and Deren Yang, "Effects of rapid thermal processing on oxygen precipitation in Czochralski silicon wafer", Semicond. Sci. Technol. 19, 2004, page1-4

7. Xiangyang Ma, **Lei Lin**, Daxi Tian, Liming Fu and Deren Yang, "Effect of rapid thermal processing on high temperature oxygen precipitation behavior in Czochralski silicon wafer", J.Phys.: Condens. Matter 16, 2004, page 3563-3569.

8. **Lei Lin**, Deren Yang, Xiangyang Ma, Liben Li and Duanlin Que, "Dissolution of Oxygen Precipitates in Silicon Treated by Rapid Thermal Process", Chinese Journal of Semiconductors 25, 2004, page 1273-1276.