4H-SILICON CARBIDE MOSFET INTERFACE STRUCTURE, DEFECT STATES AND INVERSION LAYER MOBILITY

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ABSTRACT OF THE DISSERTATION

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Silicon carbide is the only wide band gap semiconductor that has a native oxide, and a leading candidate for development of next-generation, energy efficient, high power metal-oxide-semiconductor field effect transistors (MOSFETs). Progress in this technology has been limited by the semiconductor-dielectric interface structure and its effect on the inversion layer mobility. The major objective of this dissertation is to study and improve 4H-SiC MOSFET interface structure, defect states and inversion layer mobility on the $(11\bar{2}0)$ crystal face of SiC (a-face), employing nitrogen and phosphorous passivation. We also use these results to explore the effect of reactive ion etching on the a-face, an important aspect of processing optimum power devices. We correlate electrical measurements, i.e. current-voltage (I-V) and capacitance-voltage (C-V) with physical characterization including X-ray photoelectron spectroscopy (XPS), atomic force

microscopy (AFM), transmission electron microscopy (TEM), secondary ion mass spectrometry (SIMS) and medium energy ion scattering (MEIS).

A significant phosphorus induced inversion layer mobility enhancement of ~125 cm^2/V-s is achieved, and the revisited effect of NO on the a-face of 4H-SiC yields an impressive mobility of ~85 cm^2/V-s. These results indicate that N and P improves the interface both by passivation and by interfacial counter doping, with the latter mechanism more effective on the a-face than the Si-face. Interface trap density (N_{it}) and the mobility-temperature dependence both indicate coulomb scattering is no longer the limiting factor for the N and P annealed a-face inversion layer mobility.

The second major part of this dissertation reports the use of hydrogen annealing to implement the successful recovery of the a-face ($11\bar{2}0$) crystal structure and the inversion layer mobility following degradation by reactive ion etching (RIE). The results impact the processing of SiC trench MOSFETs where the a-face sidewall forms a significant portion of the conducting semiconductor channel.

DEDICATED TO

My beloved family.

ACKNOWLEDGEMENTS

Table of Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 *Comparison of 4H-Silicon Carbide and Silicon: Basic materials properties*

SiC is a wide band gap semiconductor potentially useful in applications which are not possible with silicon. In this section the basic materials properties of 4H-SiC are described and compared to silicon, highlighting those characteristics which provide access to such specialized applications.

4H-Silicon Carbide is a wide band semiconductor, ~ factor of 3 greater than Si, with high electric breakdown (critical) field, Ec , (~7× Si) and excellent thermal conductivity (~3× Si). It also has reasonable electron mobility (~0.6× Si), hole mobility (~0.25× Si), electron effective mass (~0.4× Si), hole effective mass (~1.2× Si) and saturation carrier velocity (~2× Si). These properties make SiC a good candidate for high temperature and power switching applications. The Baliga figure of merit ($\varepsilon_S \mu E_c^3$) for high power operation is almost 400× greater for 4H-SiC than for Si. Silicon carbide is the only wide band gap semiconductor that has a native oxide, and is a leading candidate for development of next-generation, energy efficient, power metal-oxide-semiconductor field effect transistors (MOSFETs) [1].

1.2 *4H-SiC crystal structure and faces*

1.2.1 Polytypes

The SiC crystal is composed of bilayers of tetrahedrally bonded silicon and carbon atoms. For each bilayer, there are three possible occupation sites denoted by A, B and C, and a variety of stacking sequences along the stacking direction (c-axis) leads to different crystal structures, called polytypes, with the same stoichiometry. Popular polytypes for electronic applications include 3C (Cubic), 4H, 6H (hexagonal) and 15R (rhombohedral) (Figure 1.1), with 4H the most commercially available.
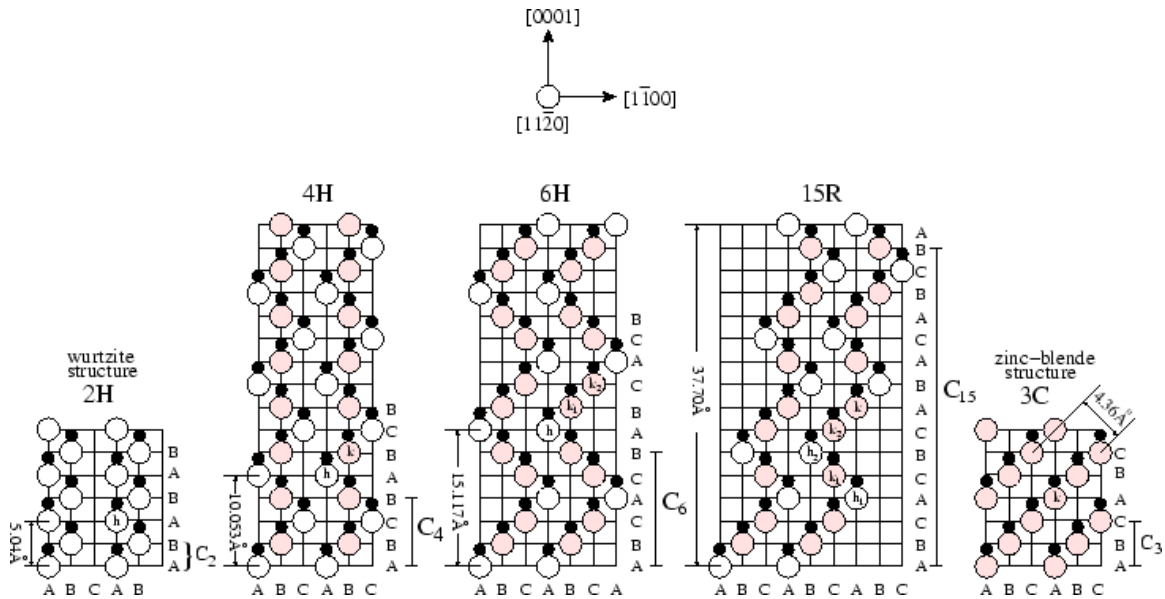
Figure 1.1 Stacking sequences for different SiC polytypes in the (11$\bar{2}$0) plane. Large empty circles are silicon atoms and small filled dots are carbon atoms. The height of the unit cell c is 10.05 Å for 4H-SiC. In 4H-SiC all the A Si-C double layers reside in quasi-cubic environments ("k" sites) with respect to their immediately neighboring above and below bilayers, and all B and C sites are quasi-hexagonal "h" sites [2].

1.2.2 Bandgap vs lattice constant

Table 1.1 Correlations between hexagonal unit cell (Wurtzite) polytypes and energy gaps [3].

SiC Polytype	2H	4H	6H	8H
Energy gaps [eV] at 300K	3.33	3.23	3.0	2.86

As shown in Table 1.1, different polytypes result in different energy gaps. Calculations using first principles methods have explained these values [3]. The trend can be qualitatively understood in the following way. Within the same type of unit cell, hexagonal for example, the spacing of planes perpendicular to c-axis are the same regardless of polytypes. The polytype is then determined by the planes stacking sequence, for example ABCBA for 4H. This determines the periodicity of the structure (Figure 1.1). Larger periodicity implies a wider potential well in quantum mechanics, leading to a lower energy level. This explains the general trend that E_g decreases monotonically from 2H to 8H-SiC.

1.2.3 4H-SiC polar/non-polar Faces

As shown in Figure 1.2, the hexagonal structures may be described as having polar faces,

i.e. (0001) Si-face and (000$\bar{1}$) C-face; and non-polar faces, i.e. (1$\bar{1}$00) m-face and (11$\bar{2}$0)

a-face. The a-face is a major device orientation explored in this dissertation. Currently,

the 4H-Si-face is the most explored crystal face for MOSFET fabrication. Nevertheless,

we note that the a-face is also of significant technical importance. In fact, in one variation

of the device, the U_MOSFET, usually fabricated on (0001) SiC, the trench walls may

correspond to the a-face and comprise the major part of the sensitive MOSFET channel

region.
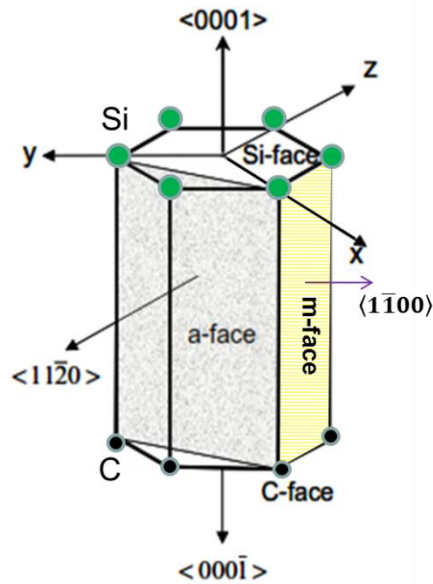
Figure 1.2 crystal faces in a 4H-SiC unit cell.

1.3 *4H-SiC Power Devices*

For low and medium power applications, 4H-SiC is used in Schottky diodes as rectifiers, and switching devices including current controlled devices, e.g. Bipolar Junction Transistor (BJT), and voltage-controlled devices, e.g. Metal Semiconductor Field Effect Transistor (MESFET), Junction Gate Field Effect Transistor (JFET) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Many of the devices are commercially available.

Due to its high critical field, high blocking voltages can be realized in 4H-SiC Schottky diodes, which are unipolar devices operating with majority carriers, and do not have the large storage time that exist in Si bipolar pin diodes, leading to much faster turn on and off.

The BJT, a bipolar device, has collector layer conductivity modulation, leading to a significantly reduced specific on-resistance. However, due to its low current gain, it requires complex and expensive gate drive circuits.

MESFET's applications on high-voltage and high-temperature power switching are limited by the fact that its gate is a Schottky contact, with a much smaller barrier height than the SiC bandgap.

A most desirable device is, of course, a SiC MOSFET. However, due to the poor semiconductor/dielectric interface, the 4H-SiC MOSFET has not been realized until very recently. There has been more interest in SiC JFETs for power applications, a device that is not dependent on the critical interface. Nevertheless, a SiC power MOSFET has many inherent advantageous over other power devices for low and medium power applications.

Compared to JFETs and BJTs, power MOSFETs have the advantage of extremely low gate current because of the insulating gate oxide, which greatly simplifies the gate driver circuits. As a majority carrier device, the power MOSFET has two major advantages over bipolar power BJT.

1) It avoids the minority carrier storage time, and is capable of operating at much higher frequencies than that of power BJT.

2) For a non-coulomb scattering limited device, it has positive temperature coefficient of the on-resistance, thus avoiding thermal runaway behavior.

1.4 *4H-SiC power MOSFET interface problem*

1.4.1 Internal resistances
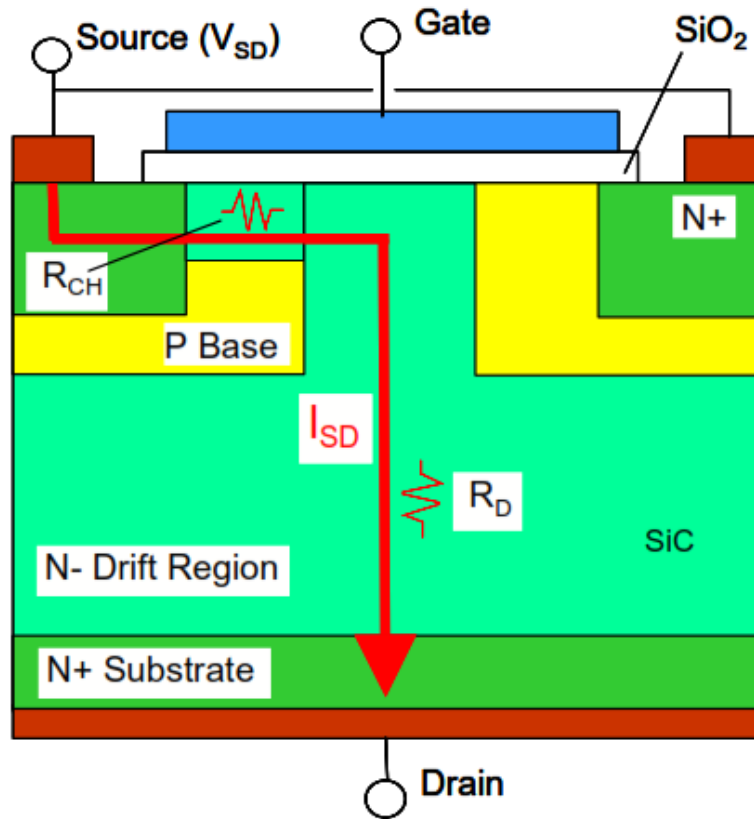
Figure 1.3 schematic of n-channel DMOSFET

A schematic diagram of an n-channel planar double-implanted MOSFETs (DMOSFETs)

is shown in Figure 1.3. In the on-state the conduction current from source to drain

experiences two resistances, first through the lateral inversion channel (R_{CH}), where the

switching control is applied by the gate voltage, and through a vertical drift layer

(R_{drift}) (the high voltage blocking layer in the off-state). So the total resistance to current

flow is represented by the 'on-resistance' R_{ON}, which determines the total internal power loss in the device and the maximum current rating of a device.

$$R_{ON} = R_{CH} + R_{drift} = \frac{L}{W Q_N \mu_{inv}} + \frac{V_B^2}{\mu_{bulk} \varepsilon_S E_C^3}$$

where L and W are the length and width of the inversion channel respectively; Q_N is the inversion layer free carriers charge and μ_{inv} is the mobility of the electrons in the inversion channel. For R_{drift}, V_B is the voltage blocked by the MOSFET, μ_{bulk} is the bulk carrier (often an electron) mobility in the drift layer vertically (along c-axis), ε_S is the permittivity of SiC and E_C is the critical field. For a given a material and blocking voltage V_B, drift region resistance R_{drift} is determined by fundamental and unchangeable materials parameters.

Ideally $R_{CH} \ll R_{drift}$, however, due to the SiO₂/SiC interface quality problem, both Q_N and μ_{inv} are very small , increasing R_{CH} and R_{ON}. This problem becomes overwhelming at medium or low voltage power applications, e.g. in electrical vehicles, as lower V_B leads to low R_{drift}, leaving R_{CH} as a large portion of R_{ON}.

This dissertation work focuses on improving the interface quality and inversion mobility, and better understanding the limiting mechanisms. Concentrating on R_{CH}, (instead of the power device in Figure 1.3), we use basic planar n-channel MOSFET structures, without a vertical drift region, as test devices for mobility, in combination with n-type MOSCAPs for measuring interface trap density (D_{it}), to study various passivations, and correlate the electrical measurements with physical characterizations, e.g. X-ray photoelectron spectroscopy (XPS), Secondary ion mass spectrometry (SIMS), and Medium-Energy Ion

Scattering (MEIS) etc, to study the atomic scale structures and interfacial solid state chemistry.

1.4.2 a-face and Trench MOSFET

The Si-face of 4H-SiC is currently the most widely commercially used device orientation due to substrate and epilayer growth efficiency and quality issues. In addition to the Si-face DMOSFET, development of high performance trench power structures are extremely desirable for next-generation SiC power MOSFETs, as the trench structure inherently offers lower conduction-losses compared to the current commercial 4H-SiC DMOSFETs [4], as illustrated by 600V class devices comparison in Figure 1.4 [5].
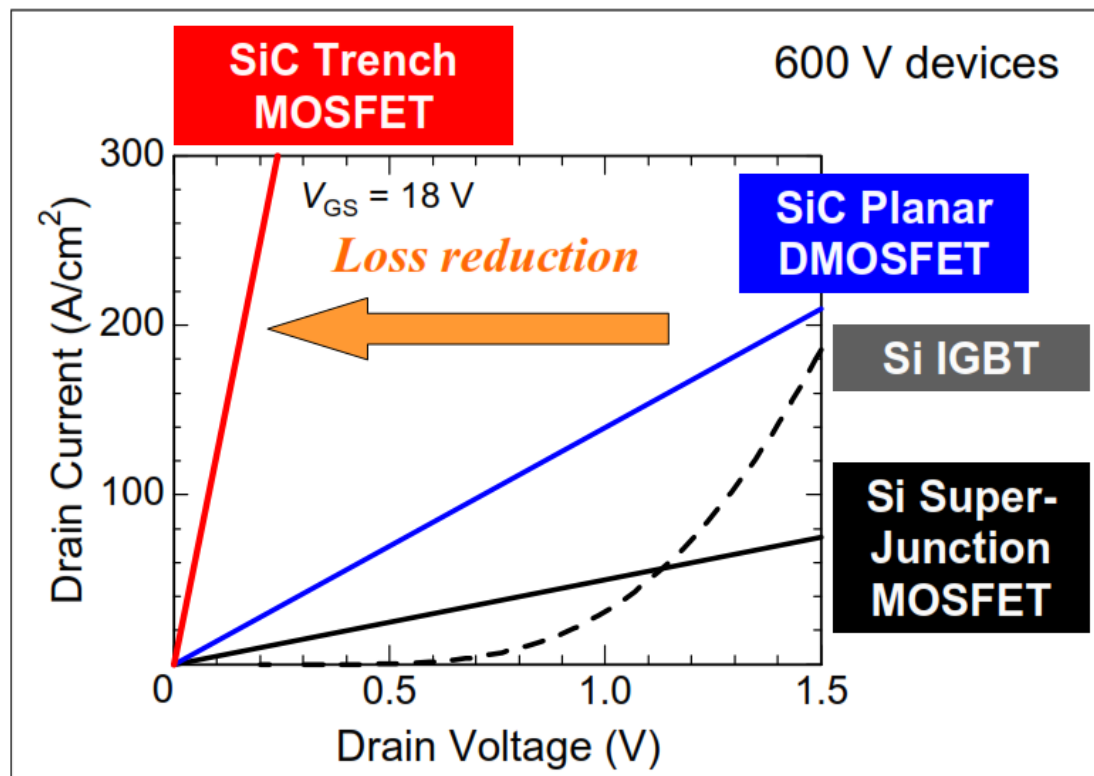
Figure 1.4 On-state characteristics for various 600V class devices at V_{GS} = 18V [5].

In trench devices, using commercial Si-face wafers, the inversion channel is located on the side wall of trenches (Figure 1.5), i.e. nonpolar faces such as the a-face. Thus, effective interface passivation for high mobility on the a-face is critical for development of trench MOSFETs.
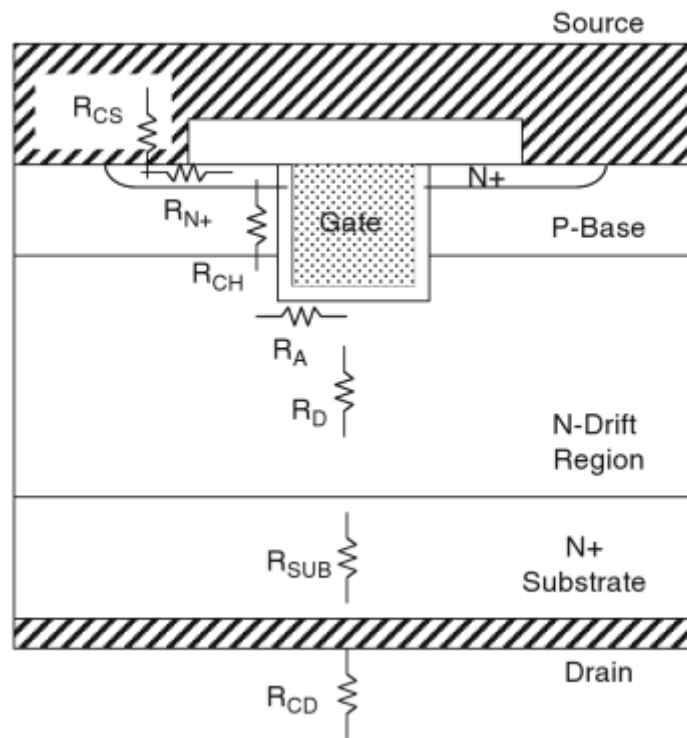
Figure 1.5 power trench MOSFET structure with its internal resistances [4].

1.5 *Inversion layer mobility limiting factors in Si*

Historically, silicon MOSFET also went through similar low μ_{inv} problem, so it would be

illuminating to review the history and the essential findings.
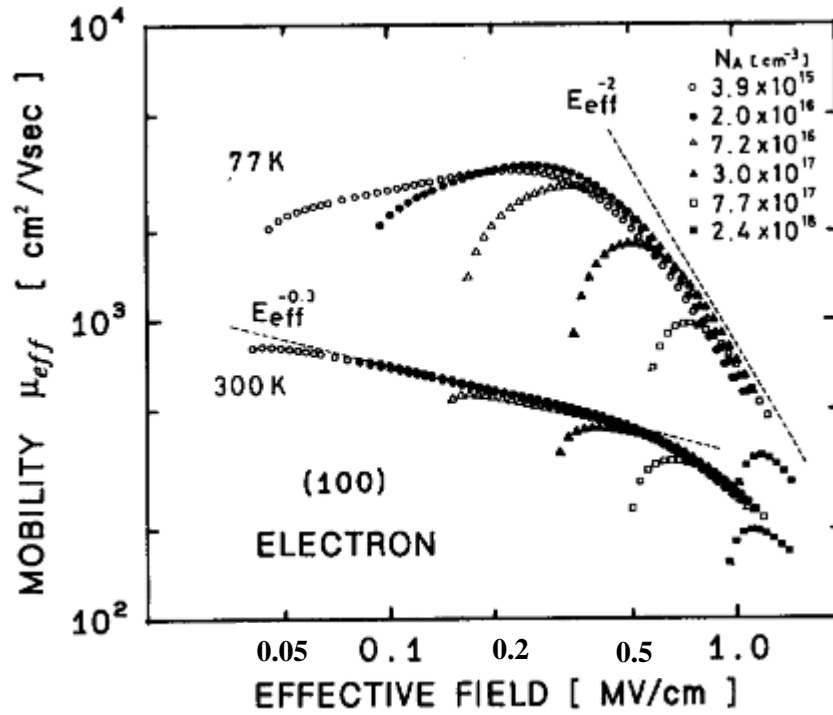
Figure 1.6 Universal mobility curve on n-channel Si MOSFET [6]

Figure 1.6 shows a typical n-channel Si MOSFET Universal mobility curve for electrons,

consisting of the effective mobility μ_{eff} vs. effective field E_{eff},

$$E_{eff} = \frac{1}{\epsilon_s} * \left(\frac{Q_{inv}}{2} + Q_B \right) \text{ (1.1)},$$

where $Q_{inv} = qN_{inv}$ is inversion layer free carrier charge, and Q_B is depletion charge per

unit area. (For future reference note that at 300K, the intrinsic bulk electron mobility for

Si is 1450 cm^2/v-s, and that for 4H-SiC parallel to the c-axis: 900 cm^2/V-s, and

perpendicular to c-axis: 800 cm^2/V-s.)

Various scattering centers have been identified that may contribute to the inversion

mobility μ_{inv}. Following Matthiessen's rule:

$$\frac{1}{\mu_{inv}} = \frac{1}{\mu_b} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{c\_Dit}} + \frac{1}{\mu_{c\_in\_Qf}} + \frac{1}{\mu_{sr}} + \cdots (\mathbf{1.2})$$

Where μ_b represents bulk mobility, μ_{ph} surface phonon scattering, μ_{c_Dit} coulomb

scattering from interface state charges, $\mu_{c\_in\_Qf}$ coulomb scattering from charges trapped

in SiO_2 and μ_{sr} surface roughness scattering.
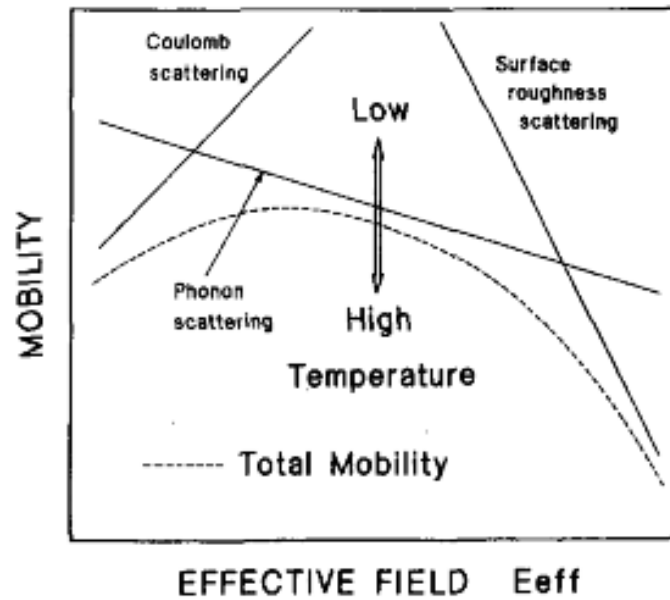
Figure 1.7 schematic of major scattering mechanisms in Universal mobility curve on n-channel Si

MOSFET [6]

For the Si MOSFET, different mechanisms dominate depending on E_{eff}, i.e. Coulomb

scattering at low E_{eff}, phonon scattering μ_{ph} at medium E_{eff} and surface roughness

scattering μ_{sr} at high E_{eff}, as illustrated in Figure 1.7. Coulomb scattering centers can be

further divided into three types, i.e. ionized dopants μ_{c_dp}, interface state charges μ_{c_Dit}

(charged defects induced and related to D_{it}) and charges trapped in the dielectric SiO_2, $\mu_{c\_in\_Qf}$ (very close to interface, excluding those in bulk oxide). Various empirical formula have been proposed to fit the universal curves and describe their dependences on E_{eff}, absolute temperature T and the specific scattering center properties.

The low-field bulk mobility depends largely on bulk acoustic phonon and ionized impurity scattering,

$$\mu_b = \left(\frac{1}{\mu_{c\_imp}} + \frac{1}{\mu_{ph\_bk}} \right)^{-1} = \frac{\mu_{max}\left(\dfrac{300}{T}\right)^{\eta_B}}{1 + \left(\dfrac{N_D^+ + N_A^-}{N_{ref}}\right)^{\gamma_B}} \quad \text{[7]} \quad (1.3)$$

Where $N_D^+ + N_A^-$ is the ionized doping concentration, μ_{max} is the maximum bulk low-field mobility, η_B, γ_B and N_{ref} are fitting parameters.

Surface acoustic phonon scattering, (power factor of T slightly varies through literatures)

$$\mu_{ph} = A \cdot E_{eff}^{-0.3} \cdot T^{-1.75} \text{[6]} \ (1.4)$$

Surface roughness scattering

$$\mu_{sr} = B \times E_{eff}^{-\gamma} \text{[6]} (1.5)$$

Surface Coulomb scattering

$$\mu_{Cit} = \frac{\Gamma_{Cit} T}{N_T} \left(\frac{n_s}{n_0}\right)^{\xi} \text{[7]} (1.6)$$

Where T is temperature, n_s is the electron surface density, n_0 is a proportionality factor, ζ is an empirical parameter, Γ_{Cit} is a coefficient as a function of effective mass and dielectric constants, N_T is the sum of all surface charge densities, including both fixed oxide charge and trapped interface charge density.

The interface state density D_{it} of a Si MOS after a H_2 anneal is shown in Figure 1.8 [8]. This is of special interest for the SiC MOS as elaborated in section 1.6, where it can be seen that, NO anneal reduces D_{it} at the conduction band edge to a level close to that in Si.
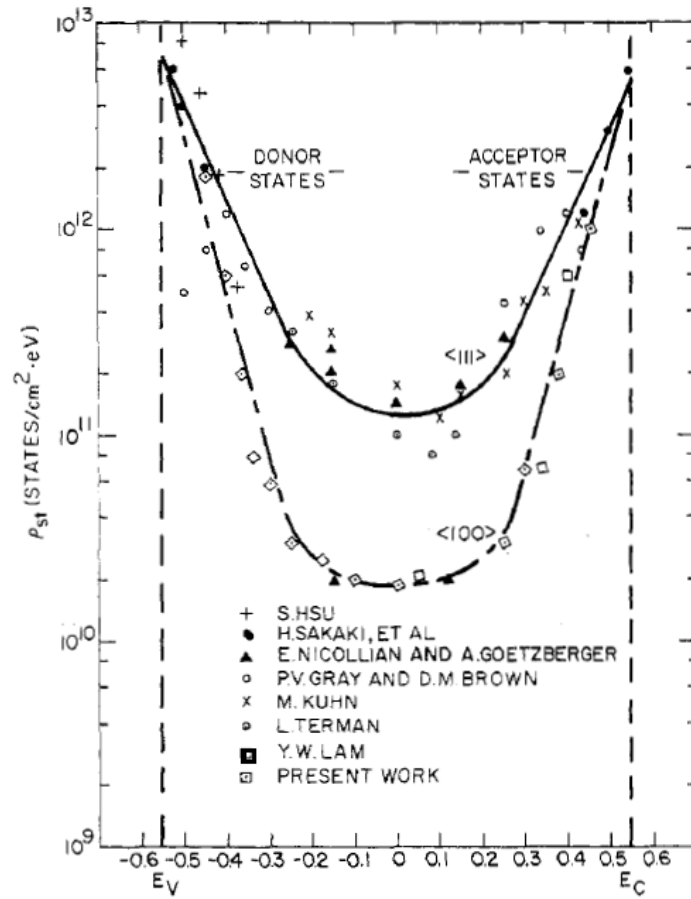
Figure 1.8 D_{it} in Si/SiO2 system [8].

Regardless of specific scattering centers, mobility can be more generally described in the following way [9],

$$\mu = \frac{q\tau_m}{m^*} = \frac{q\lambda_m}{m^* v_{th}}, \quad (1.7)$$

where the mean free path

$$\lambda_m = v_{th}\tau_m \quad (1.8)$$

is defined by in terms of mean free time τ_m between scattering event as and the thermal

velocity $v_{th} = \sqrt{\frac{3kT}{m^*}}$. The measured velocity $\sim 2\times10^7$ cm/sec is used for 4H-SiC.

For future reference, $\lambda_m = \frac{m^* v_{th}}{q}\mu$ is reduced to

$$\lambda_m = 3.41 \times 10^{-2} * u[nm] \quad (1.9) \, ,$$

with μ the mobility given in the conventional unit of $\left[\frac{cm^2}{V*s}\right]$. So for example, $\mu =$

$125 \left[\frac{cm^2}{V*s}\right]$ lead to mean free path λ_m=4.26[nm].

1.6 *4H-SiC MOS interface improvement review*

1.6.1 On Si-face

Continual research and development over the past two decades have led to 4H-SiC power MOSFETs to be on the verge of commercialization. However, further improvement is desirable in several areas. One of the critical issues is the channel resistance, which is currently very high due to the low mobility of inversion channel electrons. The field-effect mobility (μ_{FE}) has improved from<5 to ~40 cm^2/V-s, at typical operating voltages as a result of improvements in dielectric processing, but further improvement is definitely desirable [10].

Following Si MOSFET's technology, dominant scattering mechanisms need to be identified to improve mobility. For the unpassivated interface, Coulomb scattering has been considered as the limiting factor. And for the Si-face, nitric oxide (NO) post-oxidation annealing is the most established interface passivation process which results in a field-effect mobility μ_{FE} of ~40 cm^2/V-s. As shown in Figure 1.9, the mobility increases monotonically with reduction of D_{it}.
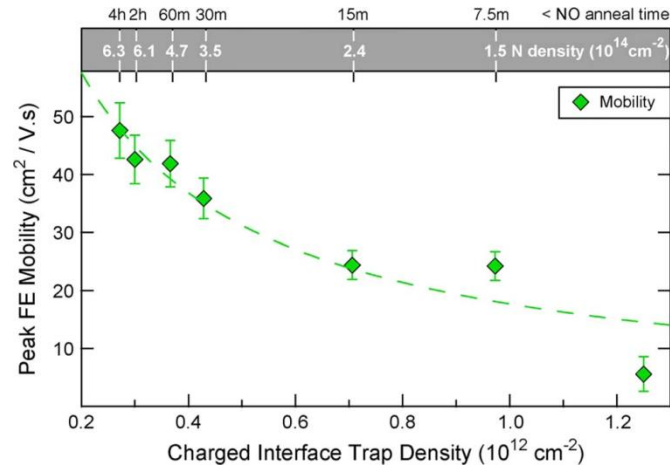
Figure 1.9 Peak field-effect mobility is plotted as a function of various NO annealing times (upper axis), which yield distinct densities of charged interface states (lower axis) in the ON-state of the MOSFETs. The N density at the interface is measured by SIMS [11].

Most recently it has been shown that a phosphorus passivation process can result in still higher inversion layer mobility of ~ 75-100 cm^2/V-s, phosphorus oxychloride ($POCl_3$) in [12] and phosphosilicate glass (PSG) in [1], and the polar PSG causes negative threshold voltage shift at temperature and positive bias (Figure 1.10).
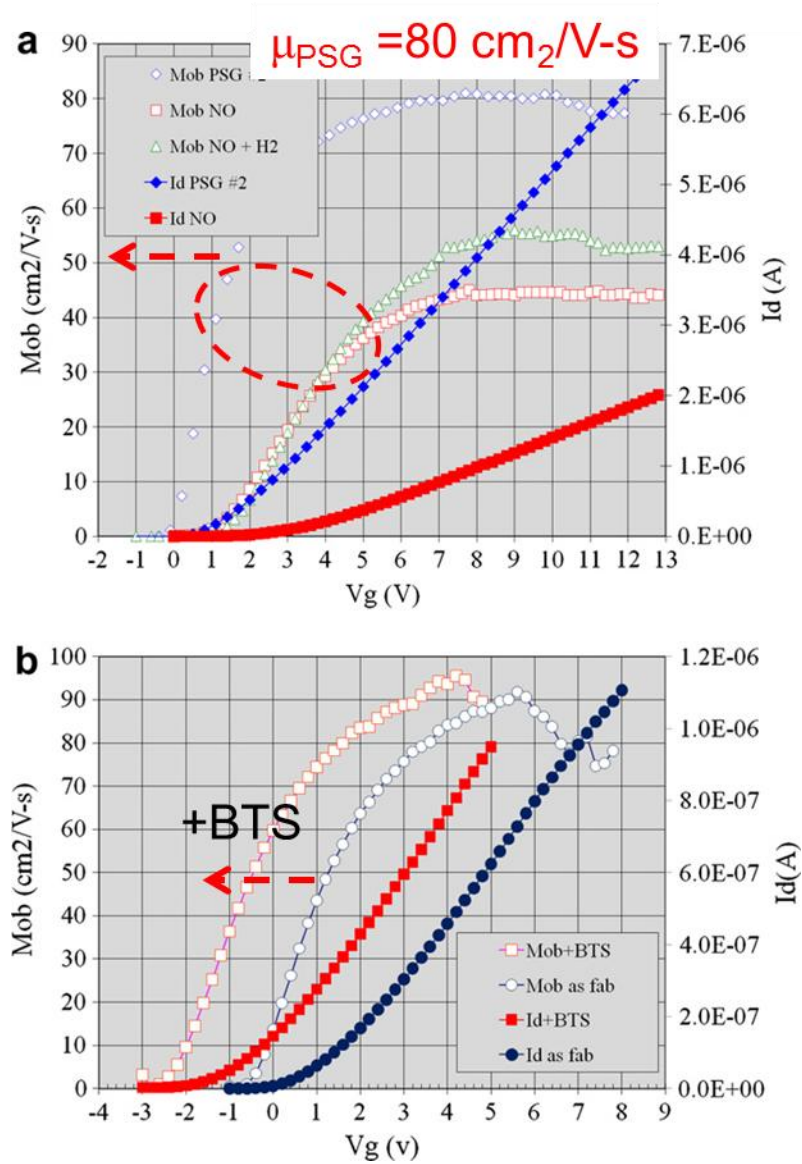
Figure 1.10 (a) Field effect mobility vs. gate voltage, with NO and PSG anneal, (b) effect of positive bias-temperature stress on threshold voltage for a phosphorous MOSFET [1].

In general the Si face mobility increases monotonically with a decreasing band-edge interface trap density (D_{it}) [1], [11] (Figure 1.11), which seems to result from a modification or passivation of the surface, although the precise mechanisms are not yet satisfactorily understood [13]. This suggests the coulomb scattering is the limiting factor to inversion mobility.
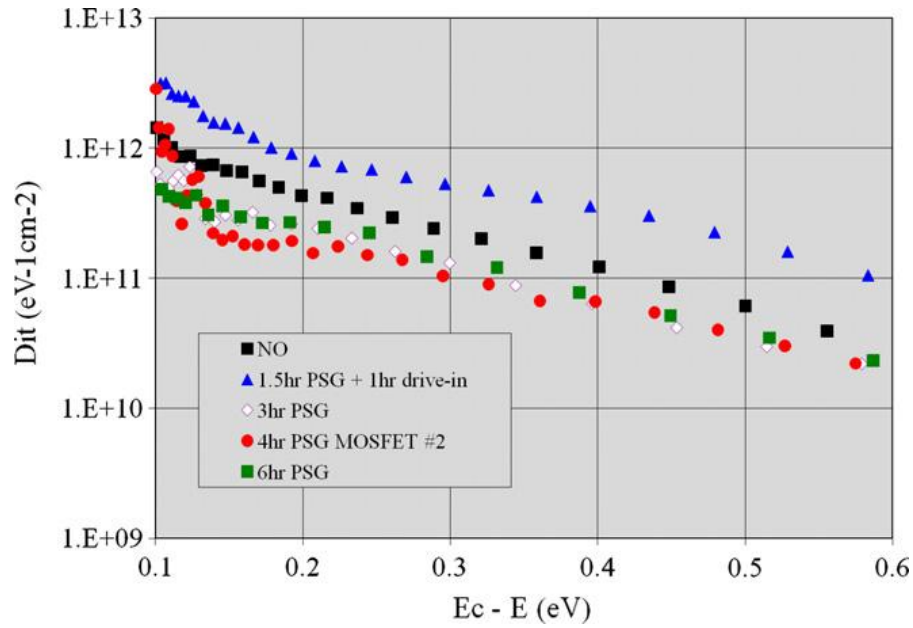
Figure 1.11 D_{it} vs. energy 0.1 to 0.6 eV below the conduction band (E_C), extracted from 'hi-low' C-V measurements, with NO anneal and PSG anneal [1].

1.6.2 On a-face

Interestingly, the a-face constantly yields higher mobility than Si-face, with similar

passivations, e.g. with wet oxidation and H_2 anneal, on $(11\bar{2}0)$ face, $\mu_{FE\_<0001>}$ =27.6

cm^2/V-s and $\mu_{FE\_<1-100>}$ =28.4 cm^2/V-s, compared with on (0001) Si-face, $\mu_{FE\_<1-100>}$

=5.59 cm^2/V-s [14], where <xxxx> represents the measured current flow direction on that

face. Even higher result has been reported with similar process, i.e. μ_{FE} =110 cm^2/V-s

[15], but has not been reproduced in the literature.

The N passivation method results in significantly improved performances on a-face.

Figure 1.12 [16] and Figure 1.13 [17] both compare D_{it} and mobility across the three

faces with N_2O oxidation at 1300°C and dry oxidation + NO at 1175°C respectively, and

they both show that the a-face as the highest mobility but not the best D_{it}. This suggests that coulomb scattering from interface states may not be the limiting factor to mobility on the a-face, contrary to the Si-face.
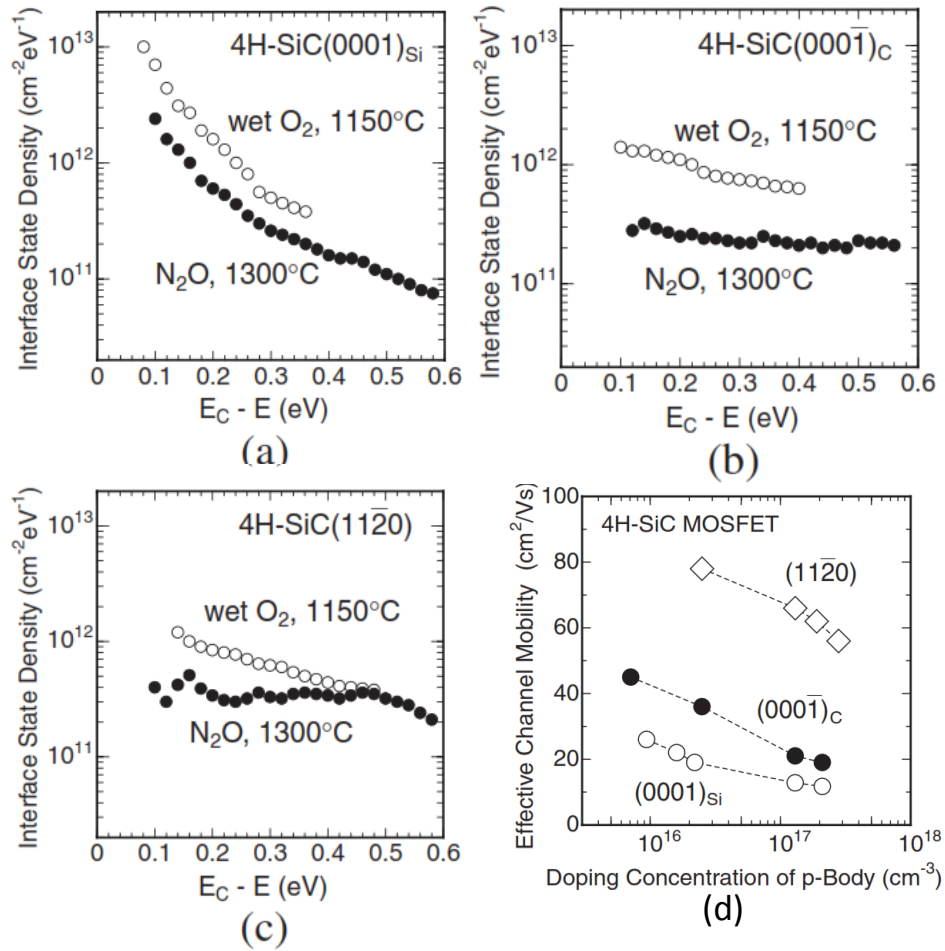
Figure 1.12 Comparison of D_{it} with wet O2 and N_2O on (a) Si-face, (b) C-face and (c) a-face, and dependence of effective mobility on p-doping with N_2O oxidation at 1300°C [16].
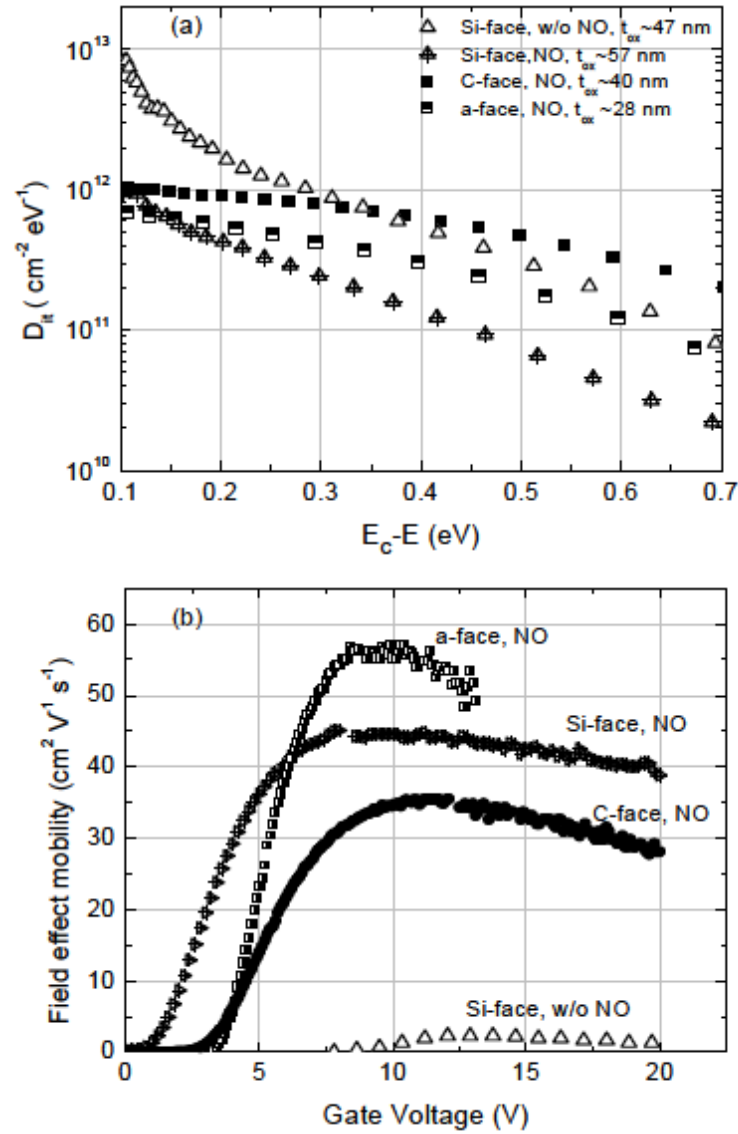
Figure 1.13 D_{it} and mobility of a-face, Si-face and C-face with dry oxidation and NO

anneal at 1175 °C for 2hr [17].

The mobility of a-face with NO anneal is the highest among the polar (0001) Si-face,

(000$\bar{1}$) C-face and non-polar (1$\bar{1}$00) M-face [18]. Therefore it is of interest and the main

topic of this dissertation is to explore the passivations on a-face in comparison with Si-

face, trying to better improve mobility (Chapter 2), to understand its limiting mechanisms (Chapter 3), as well as the N uptake on a-face (Chapter 4).

1.6.3 Reactive Ion Etching effect on a-face mobility

A second major part of this dissertation deals with the manipulation of the a-face structure as used in a trench MOSFET. A summary of previously reported work is given below. In the trench devices, a-face surfaces are on the side walls are usually formed by Reactive Ion Etching (RIE), from the Si-face of SiC wafer. And the perfection of the side wall a-face is typically not as good as the as-grown planar epi condition.

It is reported that in a practical high voltage UMOSFET, very large roughness (RMS =5.3 nm) on the sidewall after RIE, and even worse (11nm) after implant activation anneal, which cannot be recovered by standard sacrificial oxidation [19].

In other works, short channel (typically a few μm long) mobilities on trench sidewalls formed by RIE are directly studied, with H_2 or NO post oxidation anneals. And as shown in Figure 1.14 and Figure 1.15, mobility is dependent on the crystal faces, even though they are equivalent in the hexagonal crystal structure, and also sensitive to the off angle of the starting surface plane [20][21] [22].
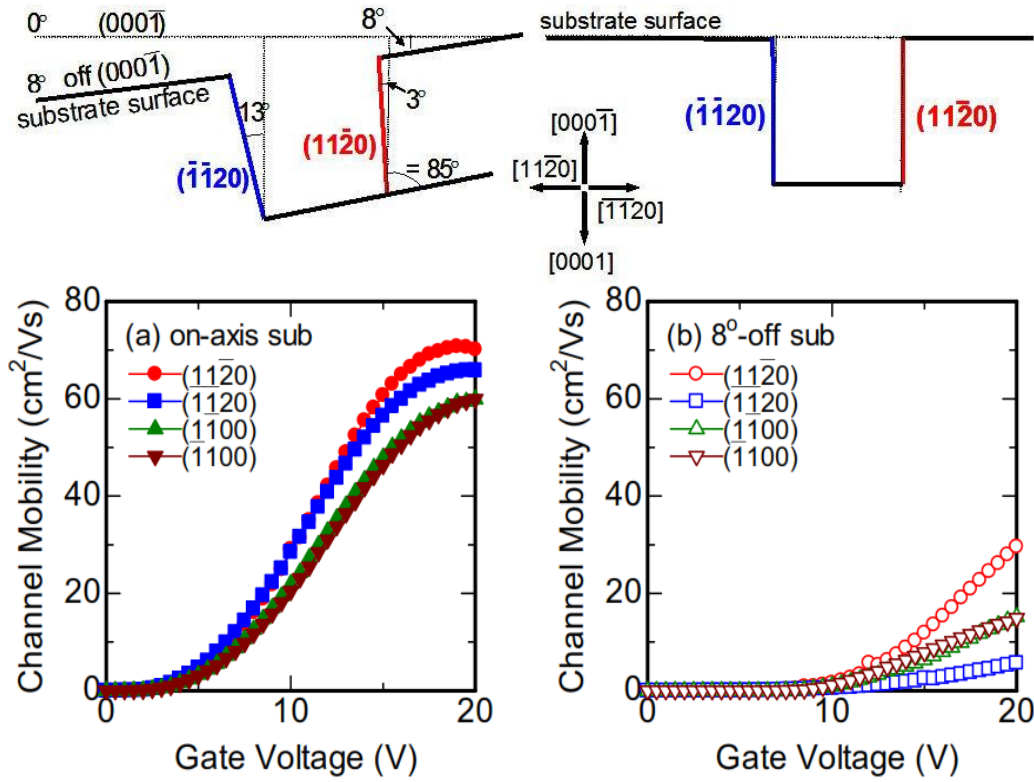
Figure 1.14 Channel L=2.75µm, Sacrificial oxidation, NO at 1150°C for 1hr [20].
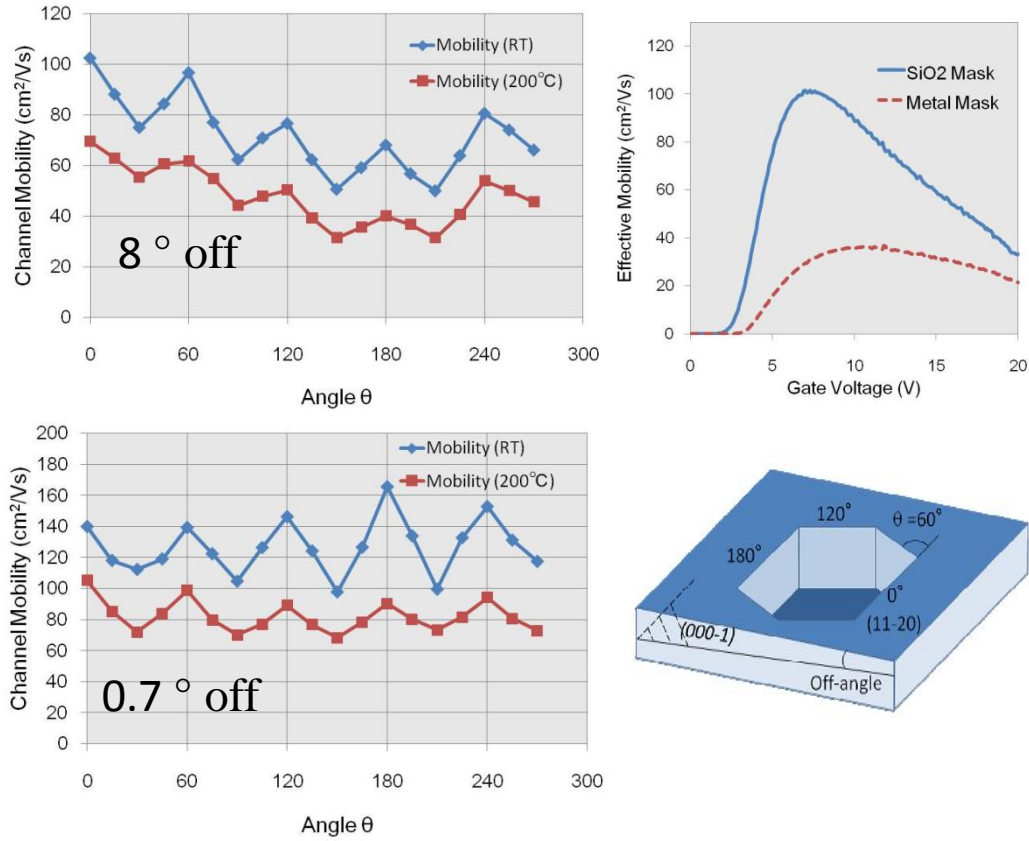
Figure 1.15 Channel L=1.5µm, H$_2$ etch 1500°C, wet oxidation +H$_2$ 800°C anneal. Off angle and angle θ are defined at lower right [22].

H$_2$ etch has also been used in [22] , in hope to improve side wall surface quality, but no surface characterizations are included to correlate to electrical results.

1.7 *References in Chapter1*

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Chapter 2 Interface state density and inversion layer mobility of a-face 4H-SiC MOS type devices

In this chapter, we present new results of the inversion channel mobility on the $(11\bar{2}0)$ a-face crystal face of 4H-SiC. This face is both technologically important and has fundamental interest as it may reveal other limiting mechanisms to the mobility. In section 2.1 , the fabrication process of the test devices is described. The interface trap density (D_{it}) is extracted by the 'hi-low' technique in section 2.2 and by 'C-ψ_s' in section 2.3 . Record high mobility with P and N anneals is reported in section 2.4, and their chemical bonding at the interface is discussed in section 2.5. The unique temperature dependence of mobility on a-face with NO anneal is compared with that on Si-face in section 2.6. Surface roughness is also studied and compared for different crystal faces and anneal methods in section 2.7.

2.1 *Fabrication*

Si-face (4° off axis) and a-face (on-axis) n-type 4H-SiC samples with ~10 um epitaxial layers doped with nitrogen at ~ $1\mathrm{x}10^{16}\,\mathrm{cm}^{-3}$ were used to fabricate MOS capacitors for D_{it} measurements. Following a standard RCA cleaning process, samples underwent dry oxidation at 1150°C for different times depending on crystal orientation. For phosphorous passivation, a planar diffusion source (PDS) anneal was used for 4hr at 1000°C, converting the oxide layer to phosphosilicate glass (PSG) [1]. For nitridation, samples were subjected to NO annealing at 1175 °C for 2 hr. Gate metallization was performed by sputtering or evaporating molybdenum. Trap density measurements were

performed using the simultaneous high (100 kHz)-low frequency CV technique at room temperature.

Long channel (150um) lateral test MOSFETs were fabricated on a-face p-type epitaxial layers (Al doping ~1 x 10^{16}cm^{-3}), using the same gate oxidation and passivation procedures described above. The source and drain regions were formed using nitrogen implantation at 700°C and activated at 1550°C for 30 min in Ar, with the surface protected by a graphite cap . Source/Drain ohmic contacts were formed by evaporation of Al. Room temperature μ_{FE} was extracted from measurements of drain current as a function of gate voltage for a fixed drain voltage (0.1V).

2.2 *Interface trap density (D$_{it}$) extracted by 'hi-low' technique*

There are numerous techniques to measure the interface trap density (D$_{it}$), including

Quasi-static) Methods, Conductance, High Frequency Methods, Charge Pumping,

MOSFET Sub-threshold Current etc [2]. The 'hi-low' technique is one of the most

commonly used in the SiC MOS field. The D$_{it}$ is given by $D_{IT} = \frac{(C_D + C_{IT})_{QS} - (C_D + C_{IT})_{HF}}{Se^2}$,

where (C$_D$+C$_{IT}$)$_{QS}$ and (C$_D$+C$_{IT}$)$_{HF}$ are the capacitances with quasi-static (QS) and 100kHz

(HF) probing frequencies, and C$_{OX}$ and Z components are mathematically subtracted

from the C-V measurements results on the MOSCAP (Figure 2.1). S is the area of the

gate electrode.

The gate voltage, V$_G$, needs to be translated into the surface potential ψ_s by

$\psi_s(V_G) = \int_0 \left(1 - C_{QS}/C_{OX}\right) dV_G + \psi_0$ [2], where the integration constant ψ_0 is typically determined

by the flat band capacitance in high frequency measurements.
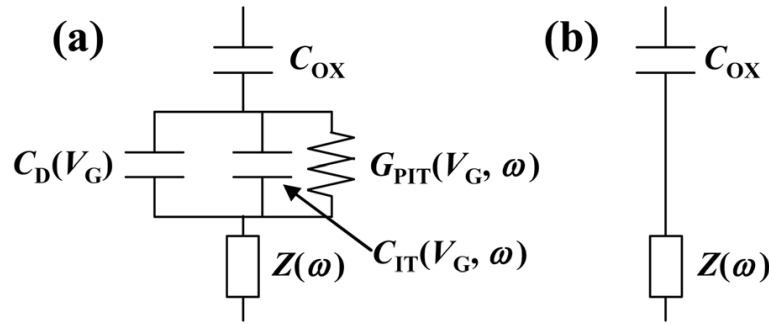
Figure 2.1 Equivalent circuits for a MOS capacitor in (a) depletion to weak accumulation and (b)
strong accumulation, consisting of the oxide capacitance C$_{OX}$, the semiconductor capacitance C$_D$, the
interface-state capacitance C$_{IT}$, the interface-state conductance G$_{PIT}$ and the series parasitic
impedance Z [3].

Figure 2.2 shows that the conversion of the thermally grown oxide to PSG reduces D_{it} on the a-face from 1.3×10^{13} cm^{-2}eV^{-1} to ~ 6×10^{11} cm^{-2}eV^{-1} at 0.2 eV below the conduction band of 4H-SiC. This value is very similar to the D_{it} of the NO annealed Si-face and a-face. In fact, PSG on the Si-face has the lowest D_{it}. The results are consistent with previously published reports, as shown in Figure 1.11 [1].
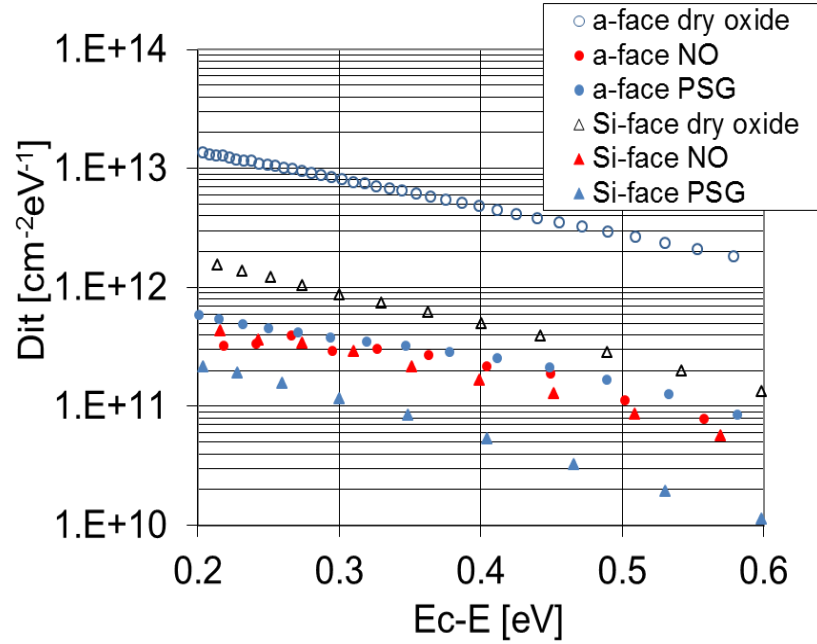
Figure 2.2 D_{it} vs. energy 0.2 to 0.6 eV below the conduction band (E_C), extracted from 'hi-low' C-V measurements. Circles are a-face samples, triangles are on Si-face. Unfilled points are unpassivated, filled red are NO annealed and, filled blue are PSG annealed devices.

2.3 *Interface trap density (D_{it}) extracted by 'C-ψ_s' technique*

It is evident from Figure 2.3 that some fast-interface-states still respond to the 'hi' probing frequency (typically 100 kHz) that is used in traditional hi-low technique, as a result, the D_{it} is under-estimating the density of these fast-interface-states. Also ψ_0,

determined based on the flat band capacitance in high frequency measurements, may be affected by these fast-interface-states.
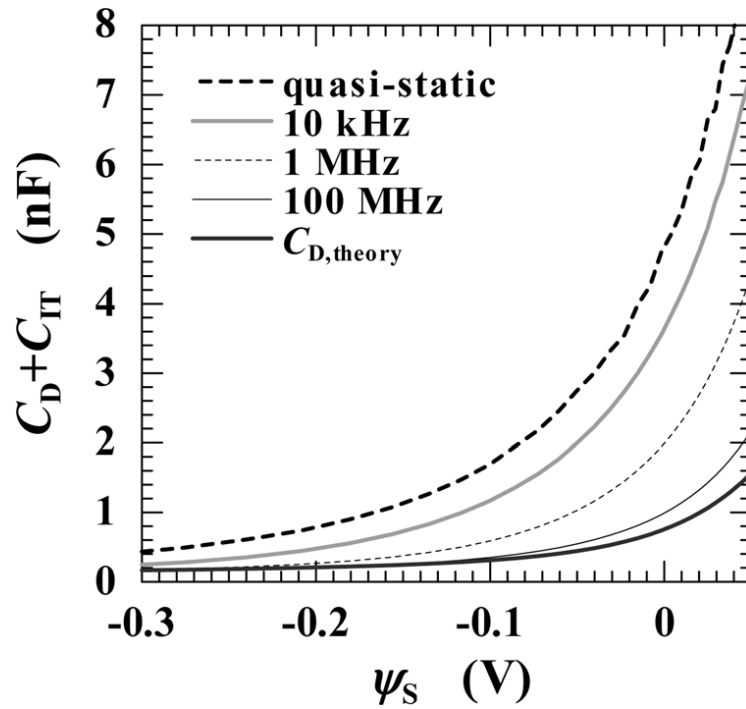
Figure 2.3 C_D+C_{IT} (semiconductor capacitance and the interface-state capacitance) versus surface potential (ψ_s) at various frequencies for an n-type Si-face SiC MOS capacitor, with dry oxidation at 1300°C, without POA [3].

To address this problem, T. Kimoto et al. proposed a method called C-ψ_s [3][4][5]. For

the D_{it} extraction, the basic idea is to replace the 'hi' capacitance $(C_D+C_{IT})_{HF}$ that is used

in hi-low method by a theoretically calculated semiconductor capacitance ($C_{D,theory}$) that

does not contain any interface states. The $D_{IT} = \frac{(C_D+C_{IT})_{QS}-C_{D,theory}}{Se^2}$ [3], so that D_{it}

contains interface states in all frequency range, as compared in Figure 2.4.
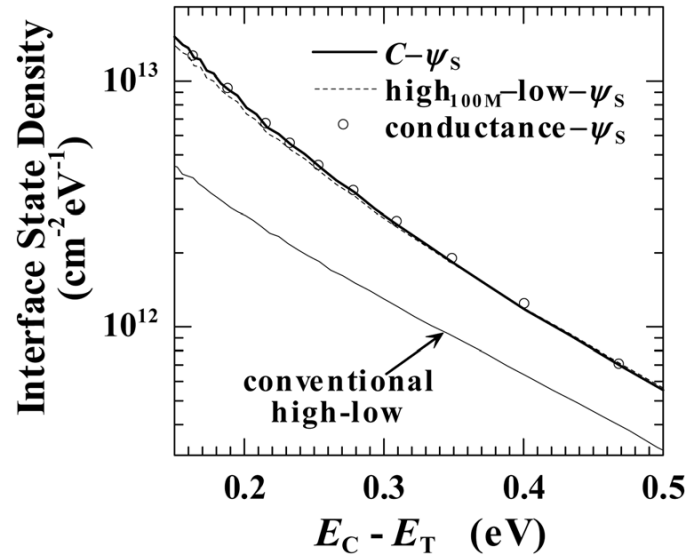
Figure 2.4 D_{it} comparison from C-ψ_s, hi (100MHz)-low-ψ_s, conductance and conventional hi-low

methods [3].

For the surface potential ψ_s calculation, at depletion with high enough probing frequency,

$\frac{1}{(C_D+C_{IT})^2} \approx \frac{1}{C_{dep}^2} = -\frac{2\psi_s}{S^2\varepsilon_{SiC}eN_D}$, so a linear plot of $(C_D+C_{IT})^{-2}$ vs. ψ_s is used to decide ψ_0

[3].

Clearly the C-ψ_s method includes more fast-state traps than hi-low, but the two big

questions to be answered are,

(1) do fast-interface-states affect inversion mobility?

(2) both hi-low and C-ψ_s method assume uniform doping profile, however, as pointed out later on in Chapter 3, counter doping exists after the N and P anneal, and their effects as the interface doping delta function remains a question.

We applied the C-ψ_s method to the same set of samples in section 2.2. Figure 2.5 compares the C_D+C_{IT} curves measured by Quasi-Static (QS), 100 kHz (HF) and the ideal C_{IT} that is theoretically calculated, on the same n-type a-face SiC MOS capacitor, after a 2 hr NO anneal at 1175°C. The corresponding D_{it}'s are compared between the two methods in Figure 2.6. As expected, C-ψ_s yields a higher D_{it}, mostly attributed to the additional fast-state traps that are excluded in hi-low. Similar trend exists on all other samples.
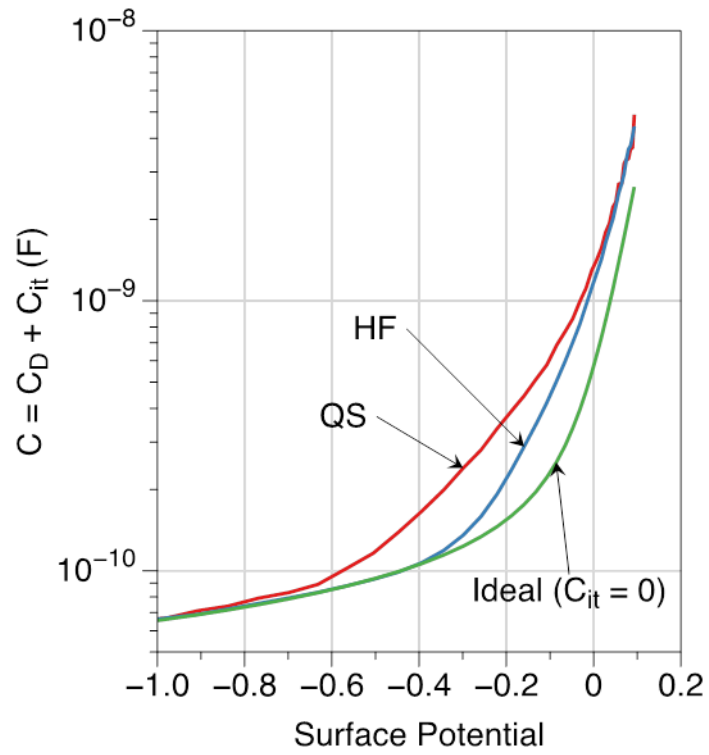
Figure 2.5 C_D+C_{IT} versus surface potential (ψ_s) at various frequencies for an n-type a-face SiC MOS capacitor (2 hr NO anneal at 1175°C)
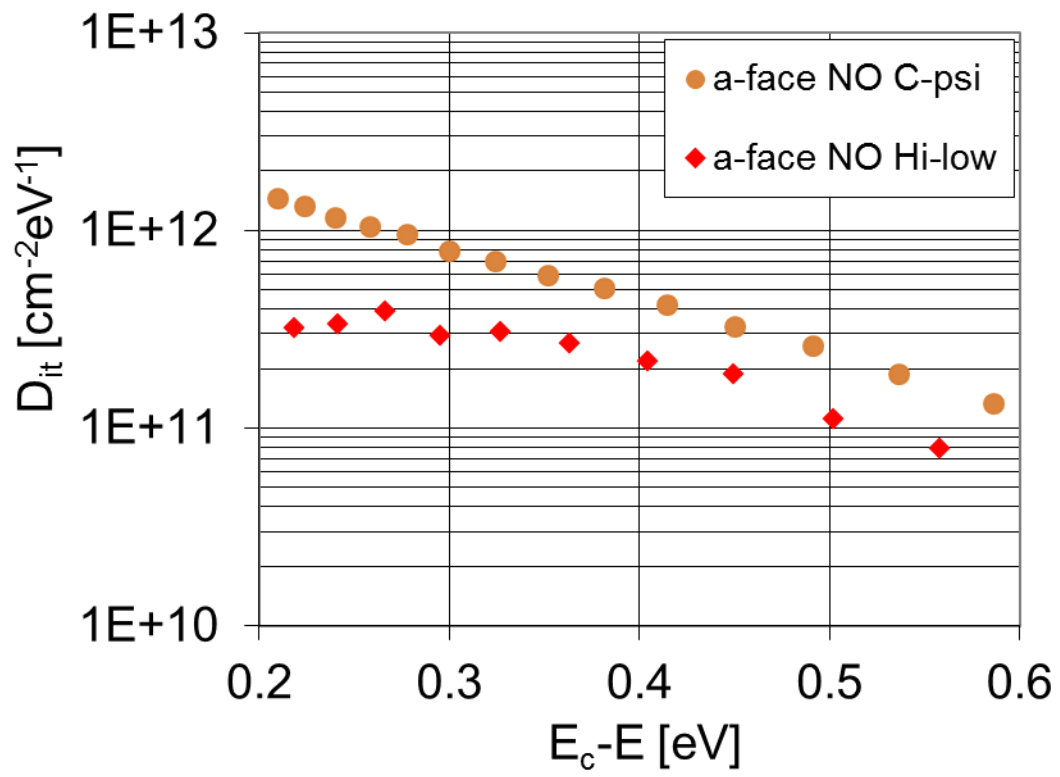
Figure 2.6 Dit comparison between hi-low and C-ψ_s methods, on n-type a-face sample with 2 hr NO anneal.

Figure 2.7 compares all C-ψ_s D_{it}'s for a-face PSG, NO and Si-face PSG, NO. The

corresponding N_{it}'s in the 0.2-0.6 eV interval are 2.33, 2.10, 2.25 and 2.84×10^{11} cm^{-2}.

Compared to the interface state density extracted by the hi-low technique (Figure 2.2), all

curves show increased densities, and relative positions are also changed, but a-face PSG

and NO continue to be close to each other. This should be compared to the large

difference in mobility as given in Figure 2.9.
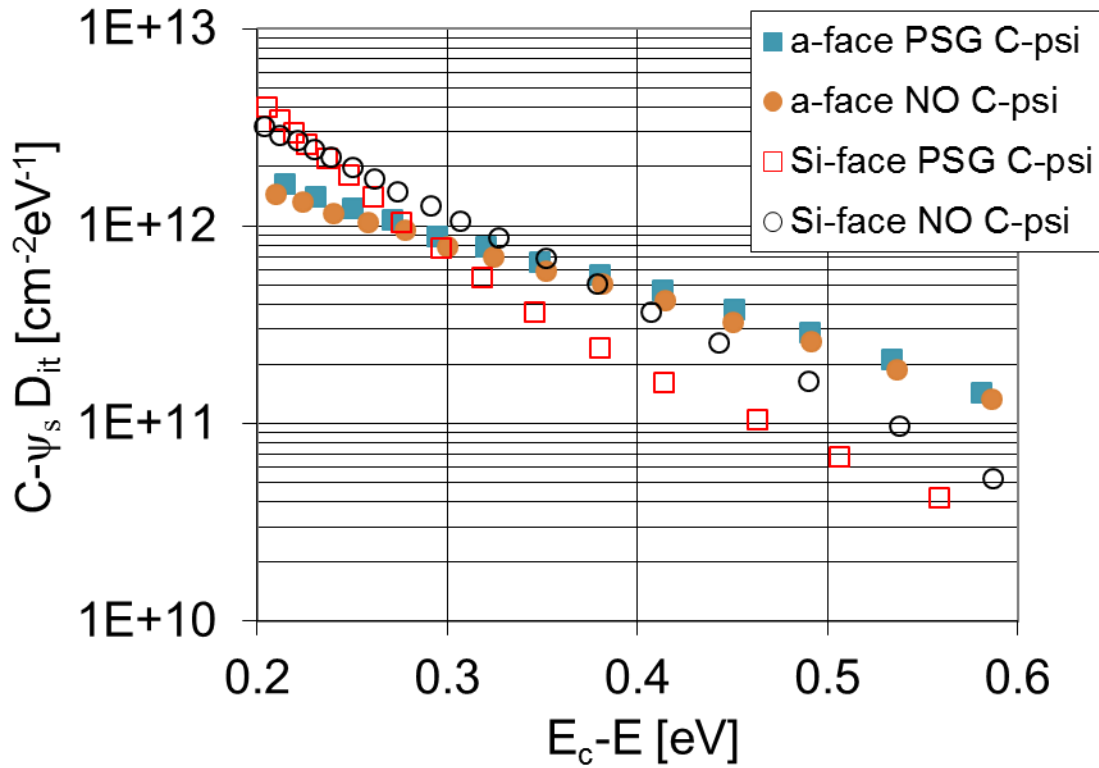
Figure 2.7 D_{it} extracted from C-V by C-ψ_s method, for a-face PSG, NO and Si-face PSG, NO. The corresponding N_{it}'s in 0.2-0.6 eV interval are 2.33, 2.10, 2.25 and 2.84×10^{11} cm^{-2}.

2.4 *Field effect mobility, μ_{FE}*
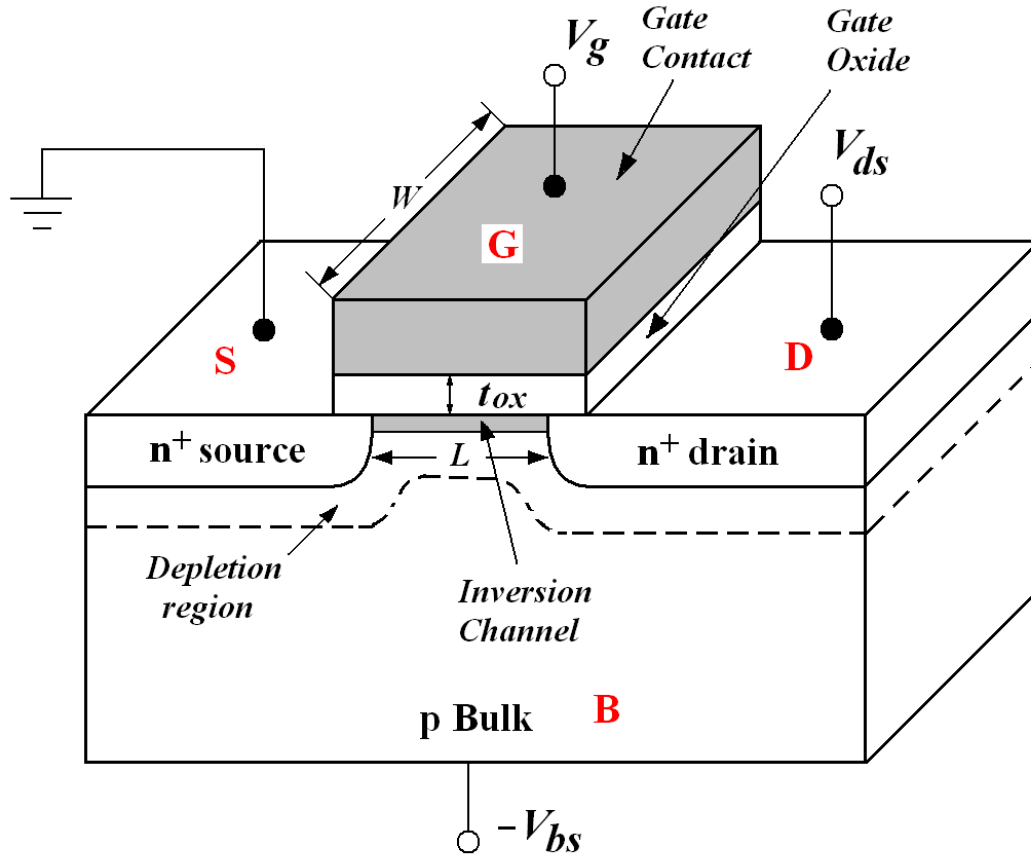
Figure 2.8 Cross section of a n-channel MOSFET.

The *field effect mobility μ_{FE}* is obtained from the MOSFET trans-conductance I_D-V_{GS}

measurement, as follows $\mu_{FE} = \frac{L}{WC_O V_D} \left(\frac{dI_D}{dV_G}\right)\Big|_{V_D \to 0}$ [2], where the device channel length

L=150um, channel width W=290um, V_D=0.1V, gate capacitance C_O in F/cm^2 is directly

measured from C-V measurement and related to the different oxide thicknesses T_{ox}, by

$C_O = \frac{\epsilon_{ox}}{T_{ox}}$, and T_{ox}=84nm for a-face PSG, 56nm for a-face NO, 96nm for Si-face PSG and

96nm for Si-face NO. The values of T_{ox} are also confirmed by profilometer and

ellipsometer measurement.

Figure 2.9 shows that the a-face inversion channel mobility, μ_{FE}= ~125 cm^2/V-s with

PSG and ~85 cm^2/V-s with NO anneal are both significantly higher than the recently

reported mobility on Si-face with the same passivation methods [1]. For comparison, μ_{FE}

without passivation on Si-face is < 10 cm^2/V-s, and on the a-face ~ 28 cm^2/V-s [6].

Threshold voltages for a-face PSG, NO and Si-face PSG, NO are 3.6 V, 4.1 V and 1.2 V,

3.2 V, respectively.
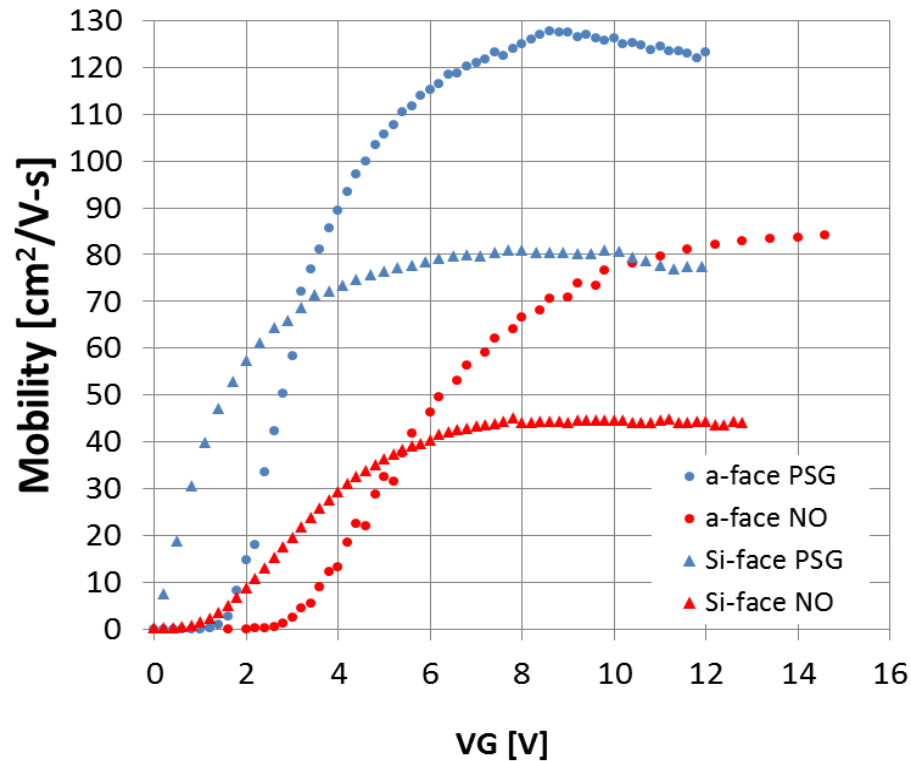
Figure 2.9 Field effect mobility, μ_{FE}, of n-channel MOSFETs made on a-face (circles) and Si-face (triangles, [1]), with PSG (blue filled) and NO (red filled) anneal respectively.

To our knowledge, the a-face PSG value is the highest inversion layer mobility reported on a SiC MOSFET using stable passivating agents, as illustrated by Figure 2.10 from a recent review paper [7].
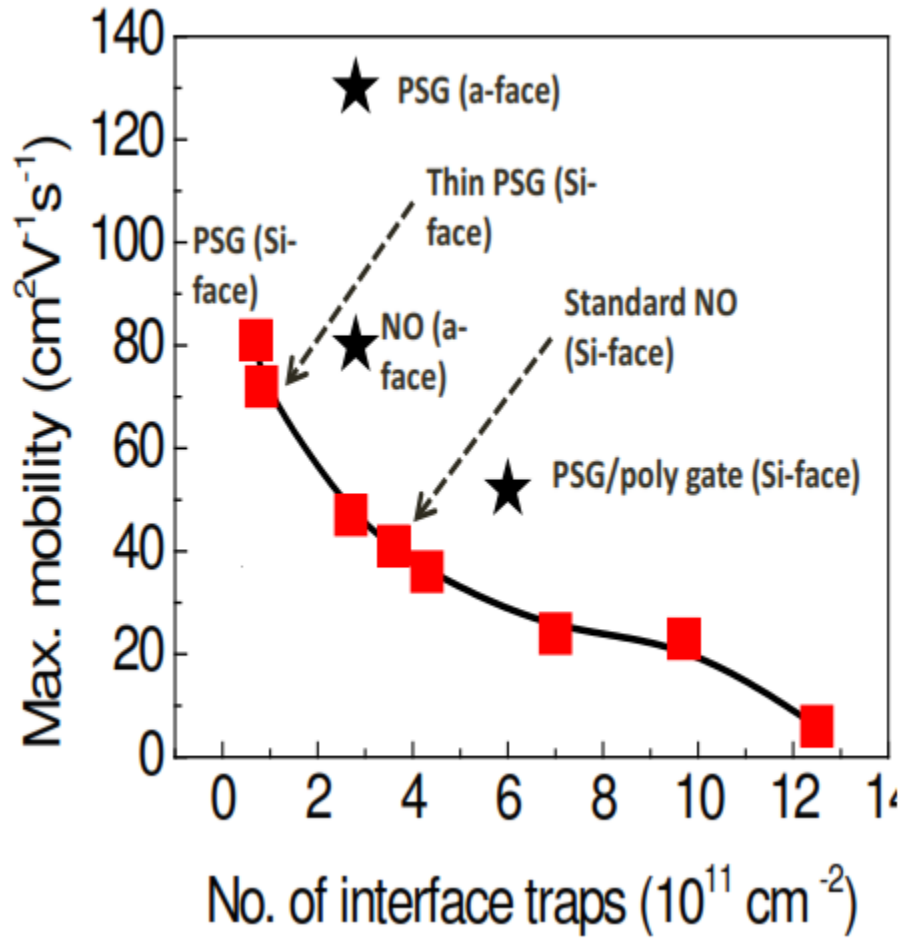
Figure 2.10 Maximum field-effect mobility versus N_{it} between 0.2-0.6 eV below E_c. The star symbols indicate this work results that do not exhibit the scaling [7].

2.5 *Chemical bonding study by X-ray photoelectron spectroscopy (XPS)*

Interfacial chemical bonding on both the a-face and the Si-face with the two different passivations were studied by X-ray photoelectron spectroscopy (XPS). The XPS energy spectra can provide critical information including the element species, its chemical binding and its areal density, among many other properties. We use XPS on the n-type capacitor samples with the gate metal removed, and the oxides completely etched off by BOE. Both in the case of P and N a measurable amount of the passivating agent is retained after etching, indicating a different chemistry for the species than interfacial N at the Si/SiO_2 interface. These species are possibly associated with the surface passivation and may even penetrate slightly into the bulk. XPS spectra are shown in Figure 2.11.
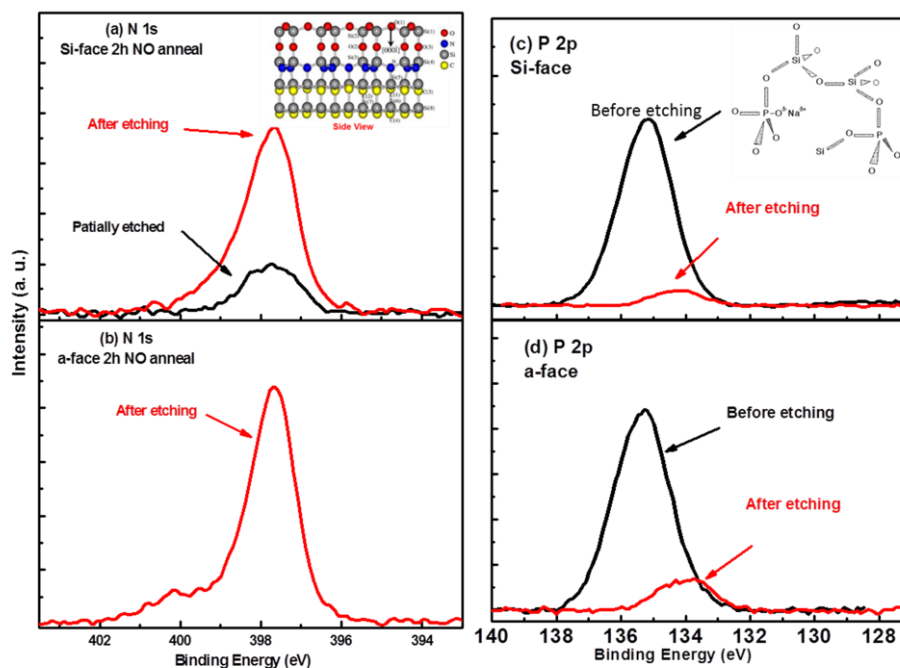
Figure 2.11 XPS spectra of N 1s on (a) Si-face and (b) a-face, and P 2p on (c) Si-face and (d) a-face, before and after oxide etch, except (b). N and P bonding crystal structures are in insets.

Both in the case of P and N a measurable amount of the passivating agent is retained after etching (Table 2.1), indicating a different chemical bond structures than N or P simply included within the oxide [8], [9]. Other methods, without oxide etching (MEIS and SIMS), show that almost all N and P are retained after etching.

Table 2.1 Surface coverage of nitrogen or phosphorous by XPS

Species	a-face	Si-face
P	1.2×10^{14} cm^{-2}	1.4×10^{14} cm^{-2}
N	6.9×10^{14} cm^{-2}	4.2×10^{14} cm^{-2}

Surface coverage of a species, e.g. N, is calculated based on XPS peaks (Figure 2.12) in

the following way, $N_N = \left(\frac{I_N}{I_{Si}} \cdot \frac{\sigma_N}{\sigma_{Si}}\right) \cdot N_{Si} \cdot \lambda$, where $\frac{I_N}{I_{Si}}$ is the intensity ratio of N and Si,

$\frac{\sigma_N}{\sigma_{Si}}$ is ratio of the cross section for ejecting a photoelectron from the N 1s and Si 2p

orbitals (0.025/0.011), N_{Si} is Si atomic density in SiC (4.9×10^{23} cm^{-3}) and λ is the mean

free path for electron escape [10]. A mean free path of 2.2nm is used in SiC, calibrated by

MEIS on a same piece of sample. Typically the k-alpha XPS system yield the N and Si

intensities automatically corrected by their corresponding cross sections, so $N_N =$

$\left(\frac{I_N}{I_{Si}} \cdot \frac{\sigma_N}{\sigma_{Si}}\right) \times 1.09 \times 10^{17} \text{cm}^{-2}$ [9]. (Note numbers in Table 2.1 are corrected by 0.76× from

that published in EDL [11], by a more accurate mean free path, i.e. 2.2 nm instead of 2.9

nm).
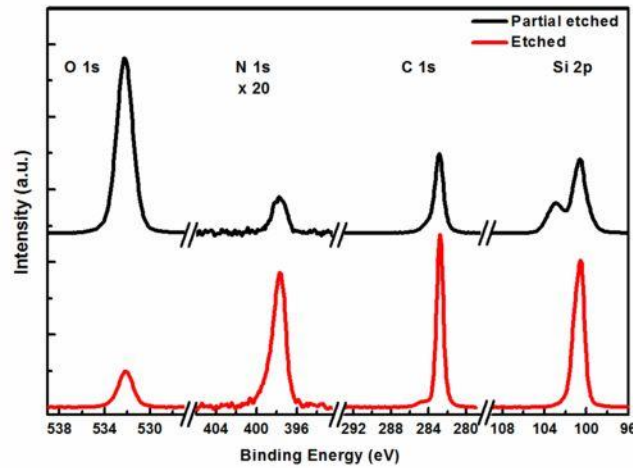
Figure 2.12 Wide energy range XPS spectra of a NO annealed SiO$_2$/SiC sample partially etched (black) to ~1.5 nm of oxide on SiC and completely etched (red), with the N 1s intensity magnified 20 times [9].

2.6 *Temperature dependence of Mobility*

As discussed earlier in section 1.5, different mobility limiting mechanisms feature distinct temperature dependences, e.g. acoustic phonon scattering has negative temperature dependence, and Coulomb scattering has a positive temperature dependence. Mobility increases with temperature because carriers with higher thermal velocity are less deflected by Coulomb scattering. And the actual mobility will be combining the various mechanisms by Matthiessen's rule as in eqn. (1.2). As a result, the actual mobility temperature dependence will be a signature of its limiting mechanism.

Mobility on the Si-face with an NO anneal have positive temperature dependences of both mobility and inversion carrier concentration, suggesting that the limiting mechanism is Coulomb scattering [12] (Figure 2.13). The latter also contribute to mobility improvement by screening effect.
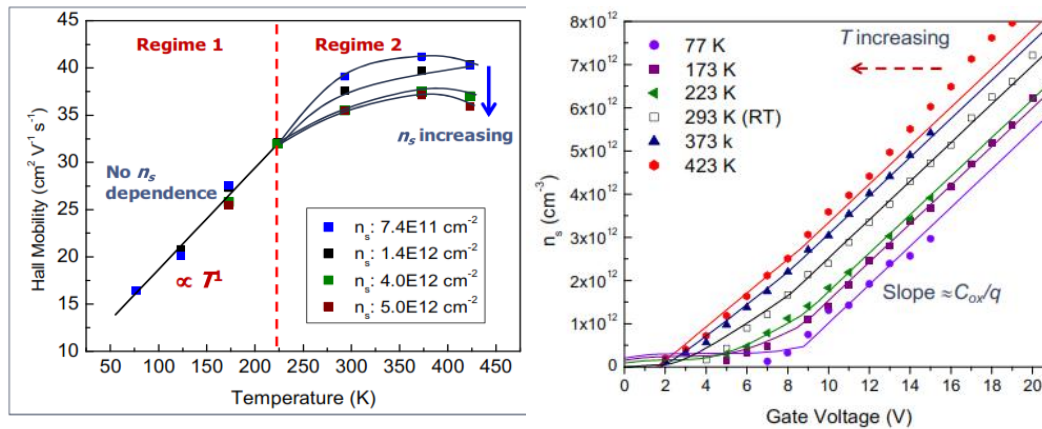
Figure 2.13 Si-face NO positive temperature dependence of Hall Effect mobility (μ_H) and free electron concentration [12].

However, on the a-face NO anneal sample, mobility has negative dependence on temperature, or mobility decreases with higher temperature, as shown in Figure 2.14, which is the same as that in Si MOSFET. This is a strong indication that coulomb scattering is no longer a dominant factor at this mobility range. The temperature dependence of peak mobility roughly follows $T^{(-3/2)}$ trend, consistent with the Si MOSFET report [13], suggesting that phonon scattering may being playing a more important role among other factors. The Si-face PSG has similar trend.
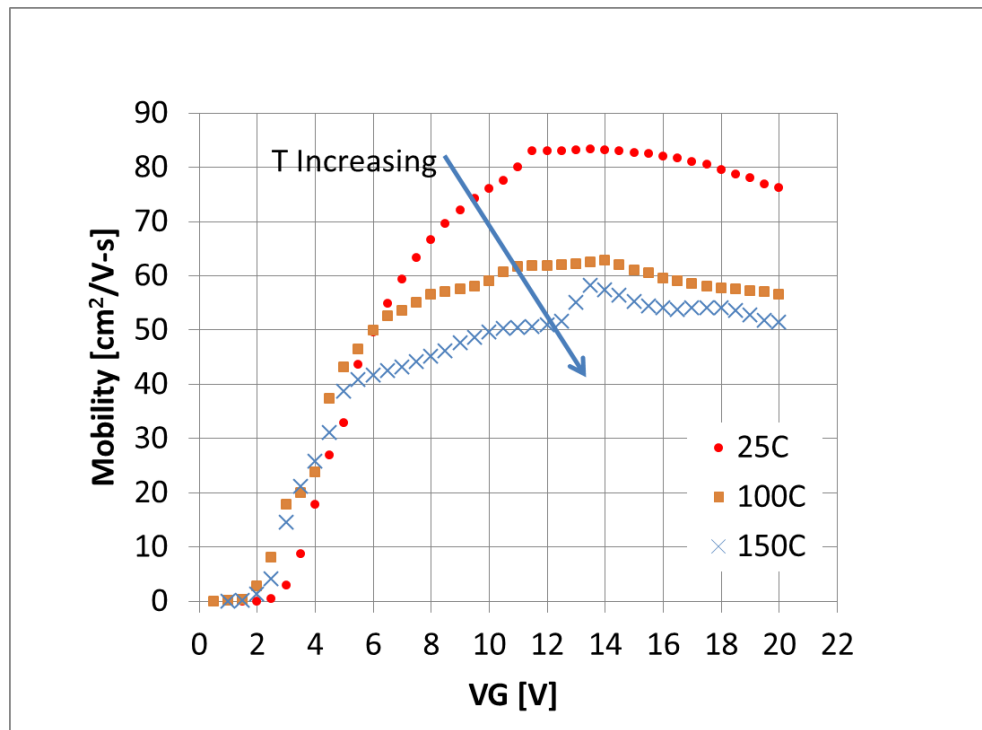
Figure 2.14 a-face negative temperature dependence of field effect mobility μ_{FE} .
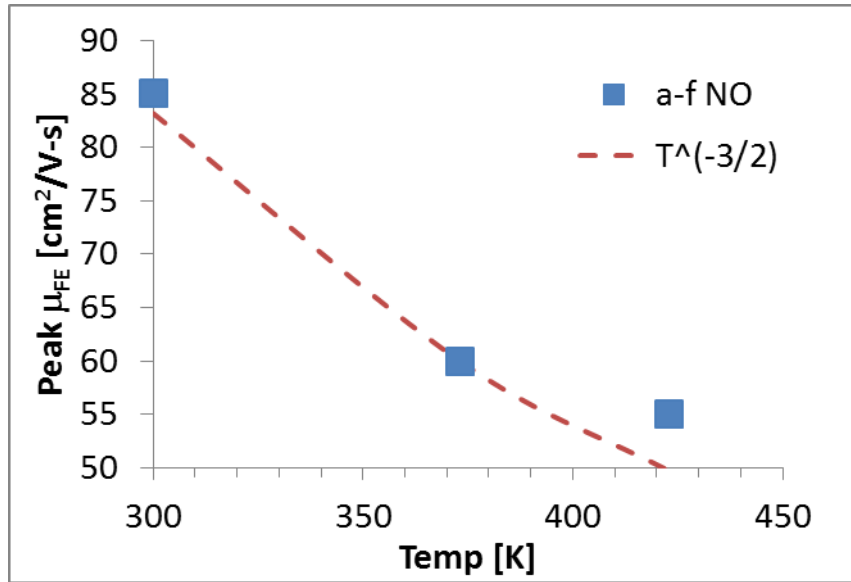
Figure 2.15 Peak mobility on a-face NO at different temperatures (filled squares) and fitting line proportional to T$^{(-3/2)}$.

2.7 *Surface Roughness*

Surface roughness is one of the various features that contribute to the actual mobility. To test for this, Atomic Force Microscopy (AFM) scans are done after gate oxide removed by HF on the set of 4 samples as shown in Figure 2.16. Surface Rq (RMS) values are similarly small for all cases except for PSG on the a-face, where dots with large height are scattered over the surface, despite the highest mobility in this case.
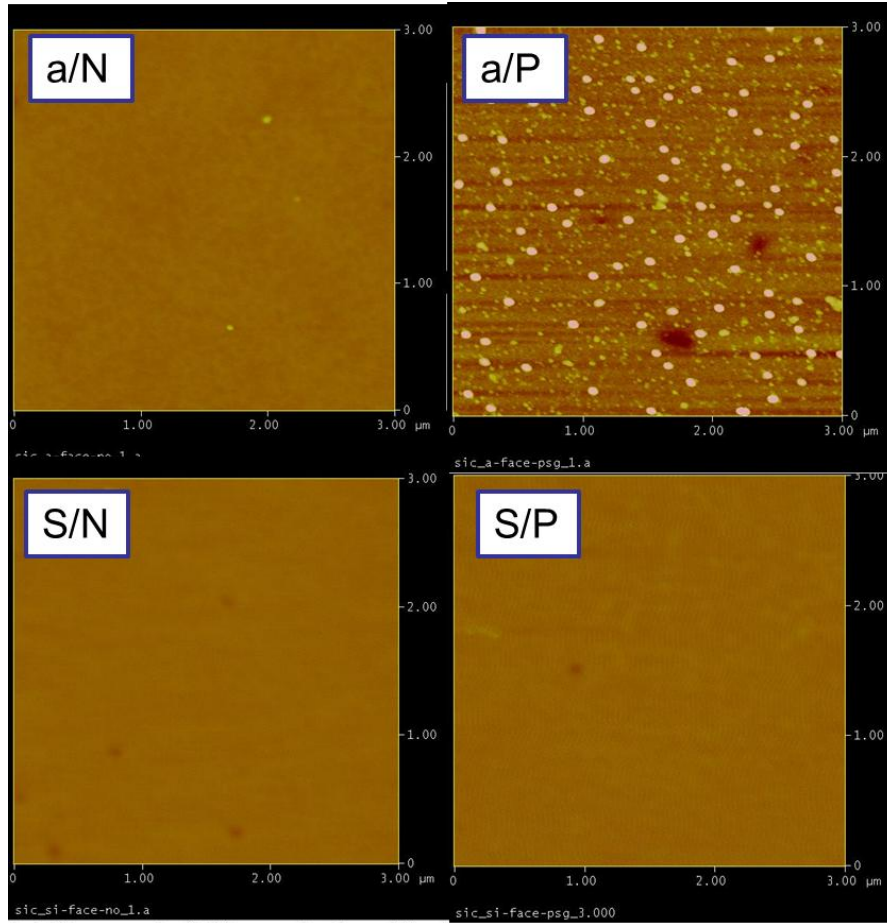
Figure 2.16 AFM results on 'a/N' a-face with NO anneal, RMS=0.25nm; 'a/P' a-face with PSG anneal, RMS=3.2 nm; 'S/N' Si-face with NO anneal, RMS=0.20nm; 'S/P' Si-face with PSG anneal, RMS=0.37 nm.

Assuming that scattering centers are all singular points without perimeters, the mean free path of electron λ_m can be correlated to mobility in the following way, $\lambda_m = 3.41 \times 10^{-2} * u[nm]$ (1.9), as derived in section 1.5. As a result, μ=85 cm²/V-s lead to mean free path λ_m =2.89 [nm], and μ=125 cm²/V-s to λ_m =4.26 [nm]. And in principle, only those roughness features that are close or shorter than λ_m are effective in scattering electrons.

The same set of samples is also studied by Transmission electron microscopy (TEM) that has higher resolution. As shown in Figure 2.17, there are indeed nano-scale roughness at the interfaces as well as a transition layer from SiC to SiO_2, which makes it hard to define the interface profile thus roughness values. This makes AFM a more attractive tool because HF etching will be self-terminated at SiC surface, exposing the true interface morphology in 2D. The nm lateral resolution is challenging for AFM, yet still achievable with special care on tip size and scanner step size etc. Chemical analysis of the transition layer will be discussed more in section 3.5.
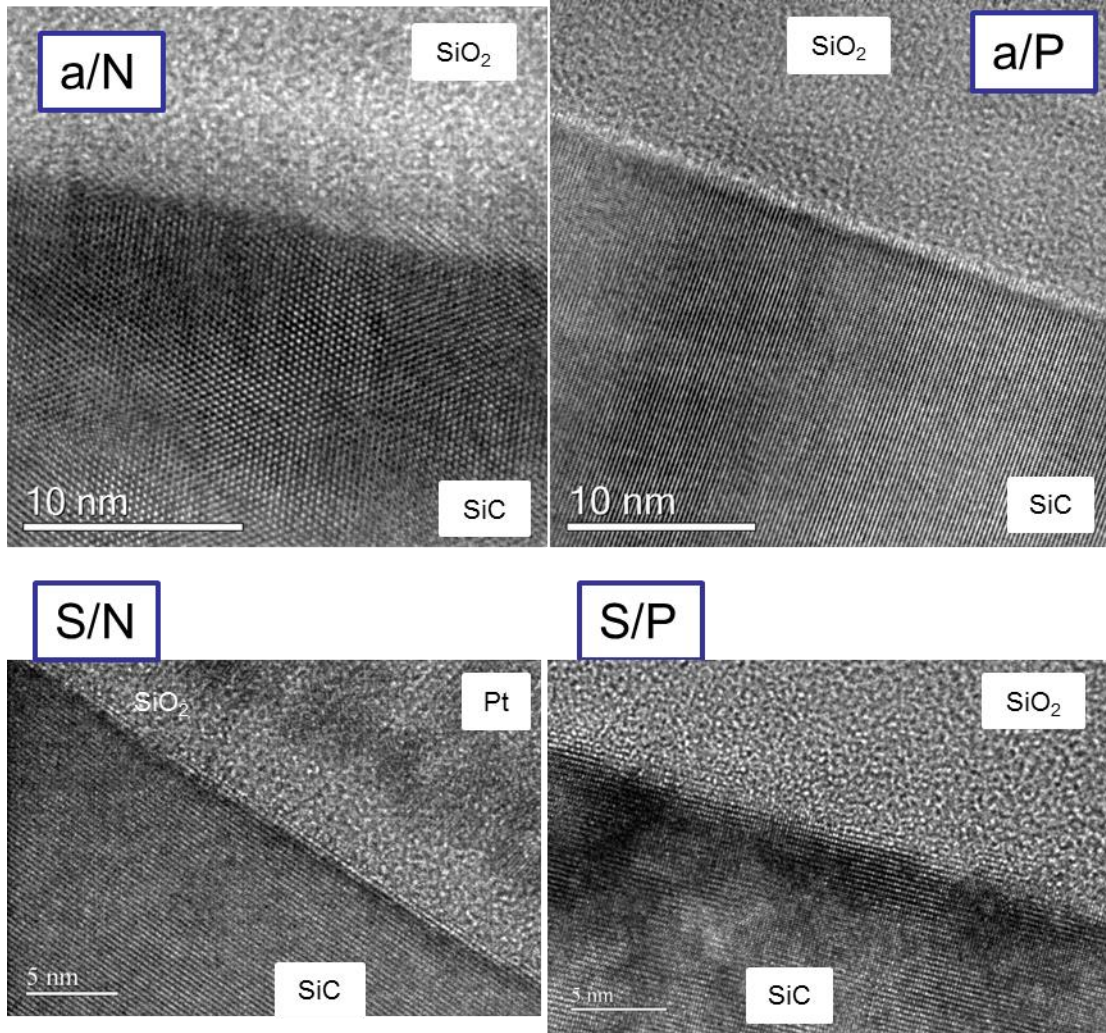
Figure 2.17 TEM results on 'a/N' a-face with NO anneal, in direction [0001]; 'a/P' a-face with PSG anneal, in direction [1$\bar{1}$00]; 'S/N' Si-face with NO anneal, in direction [1$\bar{1}$00]; 'S/P' Si-face with PSG anneal, in direction [1$\bar{1}$00].

2.8 *Summary*

PSG and NO anneals are applied to a-face, resulting in record high mobilities. The interfaces are studied and compared with Si-face by various electrical and physical

measurements. Based on these results, alternate mobility limiting mechanisms are discussed in Chapter 3 in further depth.

2.9 *References in Chapter 2*

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Chapter 3 Mobility Limiting Mechanisms

In this chapter we discuss the expected limits on the inversion layer mobility and their applicability to the results reported in Chapter 2.

Hi-low C-V results reported in section 2.2 show that both nitrogen and phosphorous reduce the SiC interface trap density substantially. Nevertheless the inversion layer mobility relative to the bulk mobility remains at a rather low value as compared to silicon devices. For example for the same doping ($N_A=10^{16}$ cm^{-3}) the ration of the inversion layer mobility to the bulk mobility is ~1/3 for Si devices and ~1/7 for SiC devices.

For the Si-face of SiC, D_{it} used to be considered the limiting factor for the channel mobility, at least at low gate voltages. For a NO anneal, the mobility enhancement scales with the interfacial N content until the reduction of D_{it} saturates, corresponding to the saturation of the interfacial N coverage at ~1/2 monolayer areal density, as shown in Figure 1.9 [1]. This μ_{FE} -D_{it} correlation continues for the Si-face-PSG, where the lower D_{it} produced by P passivation leads to still higher mobility compared to NO annealing, as in Figure 1.9 and Figure 1.10.

However, this is no longer the case when mobility is further improved on the a-face. In section 3.1, we first comprehensively compare the results from Chapter 2, and show that the coulomb scattering is no longer the limiting factor for the high mobility cases. Section 3.2 introduces the interfacial counter-doping model to account for the doping effect from N and P anneal, in addition to defects passivation. Section 3.3 and 3.4 present more supporting evidences to the counter-doping model, and address the questions of 'Why does the a-face yield consistently higher mobility than the Si-face?' and 'Why does P (at

apparently lower coverage) result in higher mobility than N?'. Section 3.5 discusses other possible limiting mechanisms after coulomb scattering.

3.1 *Post coulomb scattering limiting*

Table 3.1 compares μ_{FE} with N_{it} (E_c–E=0.2-0.6eV) by the hi-low and C-ψ_s methods, for a-face and Si-face with PSG and NO anneals. There is no longer a strong and monotonic correlation between N_{it} and μ_{FE}, although specific situations differ between hi-low and C-ψ_s methods. For example, compare the a-face PSG and a-face NO, where a larger interface defect density, N_{it} leads to better μ_{FE}.

Table 3.1 Summary of field effect mobility μ_{FE}, interface trap density N_{it} (E_c–E=0.2-0.6eV) by hi-low and C-ψ_s methods, and mobility temperature dependence for a-face and Si-face with PSG and NO anneals.

Face/Anneal	μ_{FE} [cm^2/V-s]	hi-low N_{it} [10^{11} cm^{-2}]	C-ψ_s N_{it} [10^{11} cm^{-2}]	Mobility temperature dependence
a-face PSG	125	1.02	2.33	n/a
a-face NO	85	0.79	2.10	Negative
Si-face PSG	85	0.25	2.25	Negative
Si-face NO	45	0.68	2.84	Positive

Defects at E_c–E <0.2eV can be detected by other low temperature method, e.g. constant capacitance deep-level-transient spectroscopy (CCDLTS) measurements, where D_{it} increases steadily towards E_c edge [2]. This may change the N_{it} comparison in different case.

Nevertheless the signature negative temperature dependence of mobility (section 2.6) confirms that N_{it} is no longer the limiting factor to mobility.

Note that at a medium doping level, the bulk mobility applicable to the a-face is either the same or ~10% higher than the Si-face bulk mobility, depending on direction [3], so the a-face/Si face difference is not due to the mobility anisotropy in 4H-SiC.

These results raise the following questions:

i) What is the mechanism by which nitrogen and phosphorus increase the mobility?

ii) Why does the a-face yield consistently higher mobility than the Si-face?

iii) Why does P (at apparently lower coverage) result in higher mobility than N?

iv) What is the limiting factor beyond D_{it}?

3.2 *Interfacial counter-doping into n-type*

The reduction of D_{it} suggests that both N and P play a defect passivation role. In addition, they are also n-type donors in SiC, in fig.4(c). Phosphorus resides on silicon lattice sites, and nitrogen on carbon sites, which both have layers of hexagonal (h) and cubic (k) lattice sites alternating within one unit cell, resulting in distinctly different ionization energies in eV, i.e. for P, they are 53meV at (h-site), 93 meV at (k-site), and for N, they are 42 meV at (h-site), 84 meV (k) (k-site) [4].
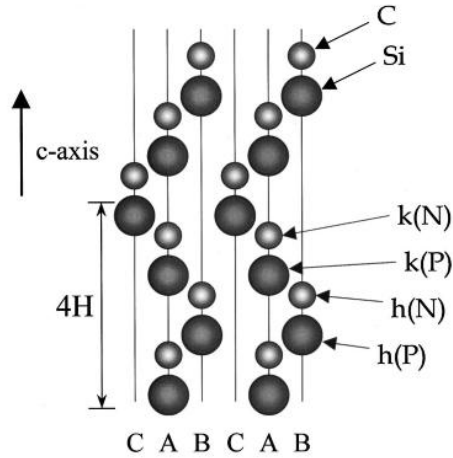
Figure 3.1 Substitutional sites for P and N in 4H-SiC.

It is possible that a small amount of each species become incorporated in a very thin layer of SiC [4] , [5], [6] at the interface, converting the doping type from p to n, which can still be easily depleted by the adjacent p-well without gate bias.

In Figure 3.2(a), in the inversion mode, the positive charge in the n-type depletion layer will cancel part of the negative electrical field built up by the negative charge in the p-well depletion region, reducing the slope of the potential drop towards the interface, effectively raising the surface potential.

In Figure 3.2(b), V_G further increases to produce strong inversion, and in addition to the conventional inversion channel, the thin n-type layer is also filled by electrons and becomes neutral, which in turn widens the bottom of the conducting channel.

As a result, for the same inversion electron density, the electric field is lower, relieving surface roughness scattering, and resulting in better mobility. And at any V_G, there are more electrons, leading to higher screening, which also improves mobility.
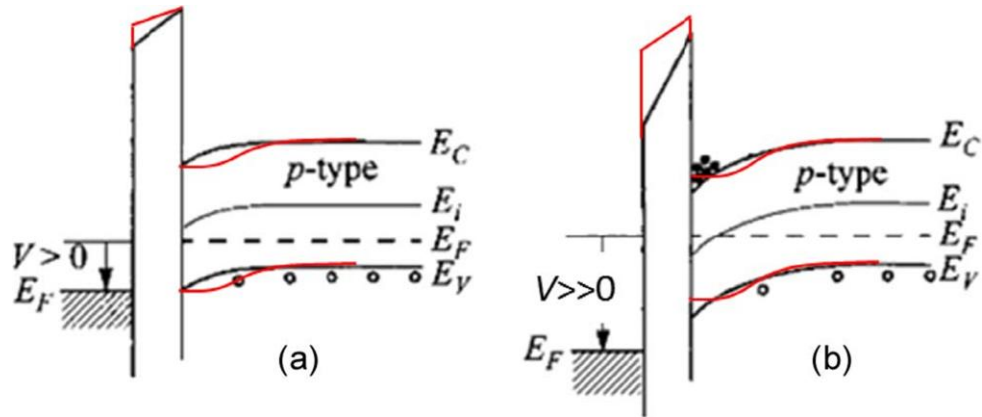
Figure 3.2 Energy-band diagrams of an n-channel MOSFET, in (a) depletion and (b) strong inversion, where standard enhancement mode structure is illustrated in black, and n-type counter-doping is highlighted in red.

Bulk counter-doping by N implantation has been reported [7], [8], [9], where normally-off devices are difficult to achieve, and the channel mobility attains a high value only at low gate voltage and drops sharply as the channel vertical electric field approaches that of normal MOSFETs, as shown in Figure 3.3 [9]. The *interfacial counter-doping* described above is distinctly different.
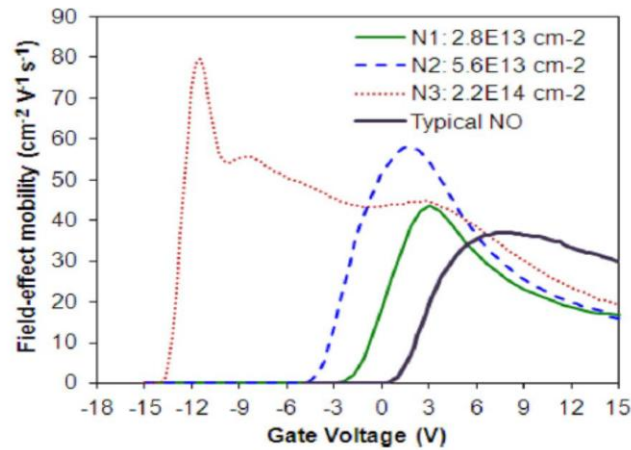
Fig. 5. Field-effect mobility of lateral MOSFETs with 10-μm channel length as a function of pre-oxidation N implant dose at room temperature.

Figure 3.3 Field-effect mobility of lateral MOSFETs with 10-μm channel length as a function of pre-oxidation N implant dose at room temperature [9].

3.3 *Why is the a-face mobility higher than Si-face?*

Numerous authors have reported results that show that inversion layer mobility measured on the a-face is higher than that of the Si-face. There are two important physical differences between these faces: (i) a-face is 50% C, 50% Si resulting in no polarization charge that exists on Si-face and C-face. Bare Si-face and C-face have ~1eV difference in electron affinity [10], however at SiO_2/SiC (unpassivated) interface, such difference between the two polar faces is not observed by internal photoemission of electrons (IPE) study [11] [12]. It is not clear if N and P passivations on polar and nonpolar faces will have different band structure. (ii) Si-face surfaces are miscut 4°off-axis towards ⟨11$\bar{2}$0⟩ to facilitate the epitaxial growth while a-faces are not miscut.

In addition the a-face has better lattice recovery and lower sheet resistance after implantation and activation than the Si-face, which implies that under similar conditions,

it may be easier for dopants to be electrically activated on the a-face than the Si-face,

leading to a higher n-type doping level and better mobility [13].
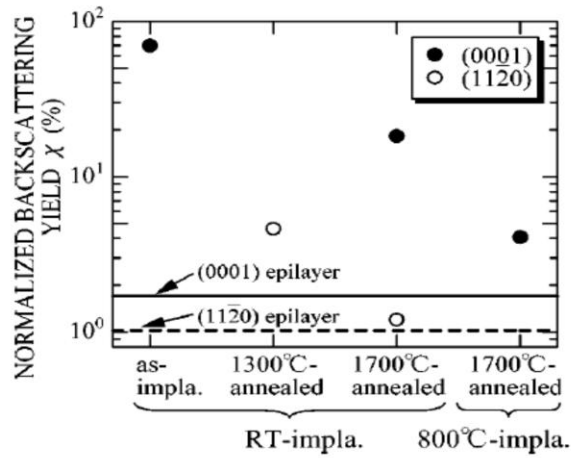
FIG. 3. Dependence of normalized backscattering yeild (χ) of 4H–SiC before and after annealing. P$^+$ implantation was done at RT or 800 °C.

Figure 3.4 Dependence of normalized backscattering yield (χ) of 4H–SiC before and

after annealing. P+ implantation was done at RT or 800 °C [13].

Conclusion:

A number of factors have been discussed related to the a-face/Si face mobility difference.

Each may play a role. Although, at this point, there is no definitive explanation.

3.4 *Why on both faces, does P passivation result in higher mobility than N passivation?*

Table 2.1 shows that on each face, P coverage is always substantially small than N but P on the a-face yields the highest mobility. This may be a counter doping effect as only a small fraction of activated donors can result in a high n type doping level, and activation ratio decreases with implant concentration per cm^3 [14]. In one extreme case, it was demonstrated that P can be activated even by an oxidation process [15], which is typically lower than 1200°C. This suggests the possibility of a higher n-type doping for PSG than for NO.

Roccaforte et al. published two important results, independently from our study that bear on this question, supporting counter doping at the interface, as proposed in section 3.2. The results also support the fact that P has stronger counter doping effect than N.

In the first study [5], on a p+ doped sample, with concentration $N_A=2\times10^{19}$ cm^{-3}, nitrous oxide (N_2O) and phosphorus oxychloride ($POCl_3$) ambient anneals are applied, on SiC patterned with field oxide, to selectively introduce N or P to the SiC surface. After oxide removal, Scanning Spreading Resistance Microscopy (SSRM) is used to measure the resistance difference on SiC surface with and without the N or P anneal. Surface resistivity is higher with N and lower with P than the original doping. A possible explanation is that N and P as donor convert the initial p+ SiC into n type, and depending on the final n doping level, results in higher or lower resistivity. Apparently P yields a higher n-type doping level than N.

This is further confirmed by a second study from the same group [6]. Scanning

Capacitance Microscopy (SCM) is applied on a cross section of n-type (0001) or Si-face

4H-SiC, with and without N and P anneal (1000–1150°C), as illustrated by Figure 3.5.

SCM uses an ultra-sharp conducting probe to form a metal-insulator-semiconductor

(MIS/MOS) capacitor with an ultrathin oxide (2-3 nm) and the 4H-SiC. When the probe

and surface are in contact, a 1V AC bias is applied at 100kHz frequency, generating

capacitance variations in the sample which can be detected using a GHz resonant

capacitance sensor. The tip is then scanned in 2D while the tip's height is controlled by

conventional contact force feedback. Carriers are alternately accumulated and depleted

within the semiconductor's surface layers by the alternating bias, changing the tip-sample

capacitance. The magnitude of dC/dV gives information about the concentration of

carriers and the difference in phase carries information about the sign of the charge

carriers [16][17].
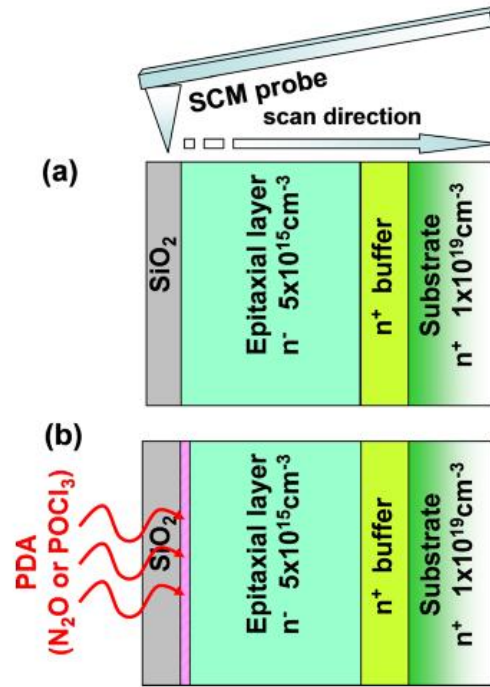
Figure 3.5 Schematic of the cross section of a MOS capacitor on 4H-SiC epitaxial samples, before (a) and after the PDA (b). The scan direction of the SCM probe during the measurement is also indicated. The electrically modified layer below the SiO$_2$ in the sample subjected to PDA is indicated by a dashed region [6].

The carrier concentration profile reveals that the peak donor concentration is $N_D=5\times10^{17}$ cm^{-3} for N sample, $N_D=4.5\times10^{18}$ cm^{-3} for P, compared to the initial n- doping of $N_D=5\times10^{15}$ cm^{-3}. The paper also estimate the N and P doped interfacial region thickness to be 5.1 and 1.7 nm, based on the Debye length (L) [6].

The product of those two values gives the areal density of activated N and P as donors, as $N_{D\_N}=2.5\times10^{11}$ cm^{-2} and $N_{D\_P}=7.6\times10^{11}$ cm^{-2}. If we assume their N and P coverages are comparable to our coverage in Table 2.1, then the activation ratio of N and P can be estimated on Si-face, i.e. 0.04% for N and 0.32% for P.

It has also been reported that on a-face, higher temperature NO anneal at 1250 °C yields higher mobility, i.e. 118 cm^2/V-s [18], compared to NO anneal in this study at 1175 °C and 85 cm^2/V-s. This is consistent with the counter doping model where higher temperature leads to higher activation ratios thus higher n-type counter doping, resulting in higher mobility.

3.5 *Other possible limiting mechanisms*

Additional limiting factor for the mobility beyond D_{it} or coulomb scattering include phonon scattering and surface roughness. Temperature dependence study in section 2.6 suggests that phonon scattering is playing a more important role, with other factors also contributing although not dominant, since fitting does not perfectly match the data. Surface roughness remains a possible candidate. As discussed in section 2.7, only short range roughness can be effective as a scattering center, and only very high resolution surface microscopy can reveal this. In the field of Si MOS devices, surface roughness scattering is widely used to account for the rapid decrease in the electron channel mobility at high vertical electric fields, yet efforts to increase the channel mobility by reducing the Si/SiO_2 interface roughness remain unsuccessful.

C. Hu et al. proposed an additional scattering mechanism [19], where a small amount of electron wavefunction penetrates into the amorphous SiO_2 region given its finite barrier height, as shown in Figure 3.6. The mobility in the oxide is practically negligible thus, by losing that fraction of carriers, the overall effective mobility is reduced.
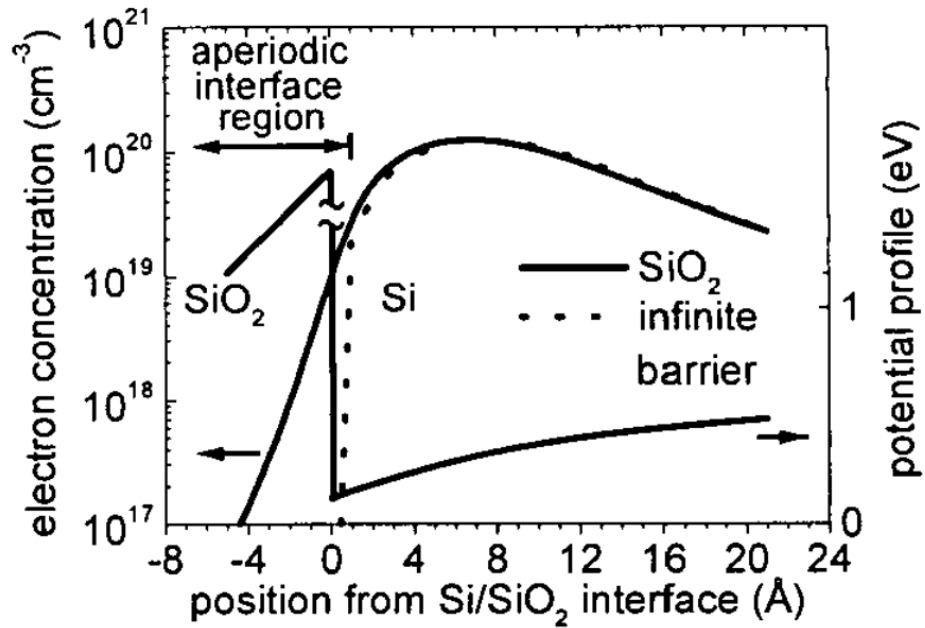
Figure 3.6 Electron wavefunction penetration into gate dielectric in Si MOS [19].

The fraction of electron wavefunction in the dielectric, f is a function of electron barrier height Φ_{Be} and the transverse electrical field E_{eff}, i.e. lower Φ_{Be} and higher E_{eff} both increase wavefunction penetration, as shown in Figure 3.7. Φ_{Be} of HfO_2, Si_3N_4 and SiO_2 on Si are 1.1eV, 2.1eV and 3.1 eV respectively.
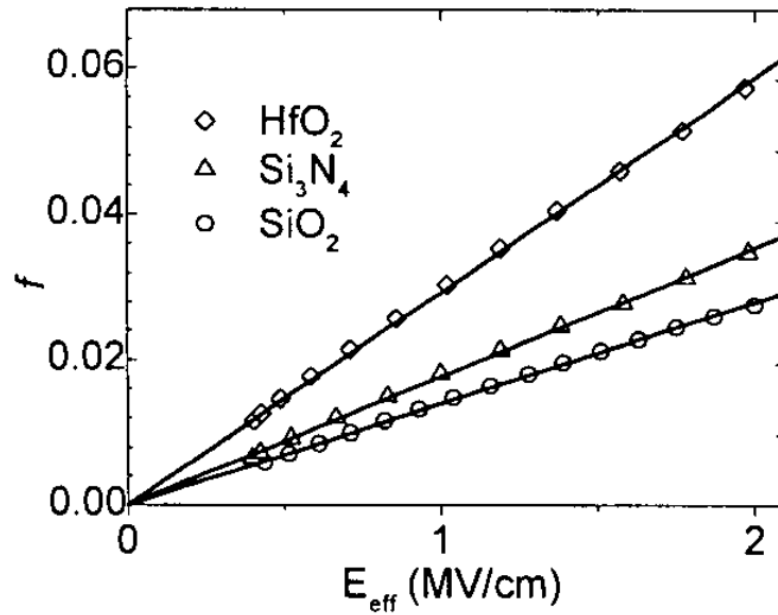
Figure 3.7 Fraction f of electron wavefunction in the dielectric is a linear function of E_{eff} [19].

Compared to Si, 4H-SiC not only has a wider bandgap E_g by 2.14eV, the electron Φ_{Be} is also reduced by 0.45 eV, assuming exactly the same oxide on both materials (Figure 3.8). Both the wider bandgap and less Φ_{Be} can increase f.
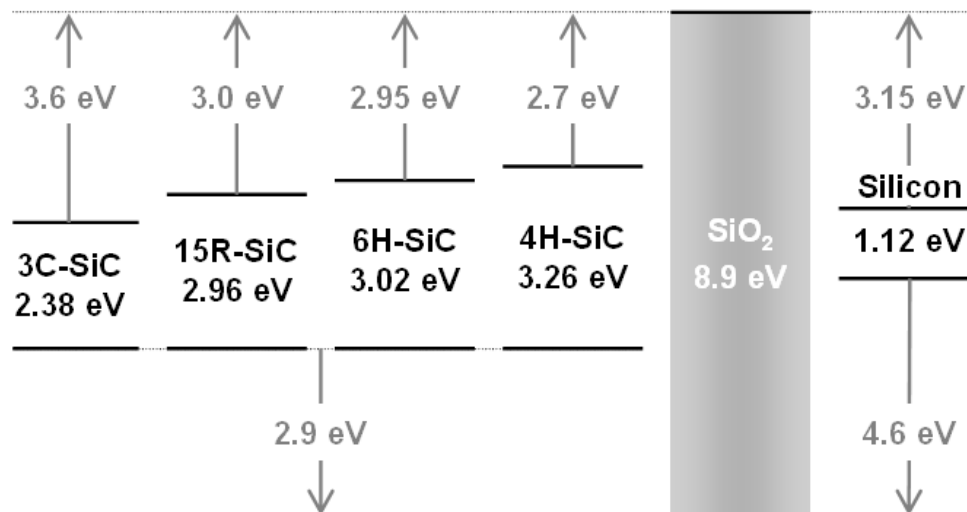
Figure 3.8 Bandgaps and relative band-offsets of Si, SiO₂, and common SiC polytypes [20]. Electron affinity of SiO₂ is 1 eV.

To estimate the former effect, we need to first translate the wider E_g effect into E_{eff}, i.e.

$E_{eff} = \frac{1}{\epsilon_s} * \left(\frac{qn_{inv}}{2} + \epsilon_s \mathcal{E}_M \right) = \frac{q * n_{inv}}{2\epsilon_s} + \mathcal{E}_M$. The semiconductor dielectric constants ϵ_s are

close for Si and SiC. The semiconductor depletion charge makes a larger difference. In

strong inversion the surface potential is given by $\Psi_s = 2\Psi_{BP} = \frac{2kT}{q} \ln \left(\frac{N_A}{n_i} \right)$, where the

intrinsic carrier density n_i is a strong function of E_g, i.e. $n_i = 9.65 \times 10^9$ cm^{-3} for Si and

5×10^{-9} cm^{-3} for SiC. So with the same p-doping, at strong inversion, the semiconductor

electric field E_M of SiC is much larger than that of Si, i.e. $\mathcal{E}_M = \sqrt{\frac{4kTN_A}{\epsilon_s}} \ln \left(\frac{N_A}{n_i} \right)$. Figure

3.9 compares Si and 4H-SiC MOS E_{eff} vs. inversion electron concentration, with p-well
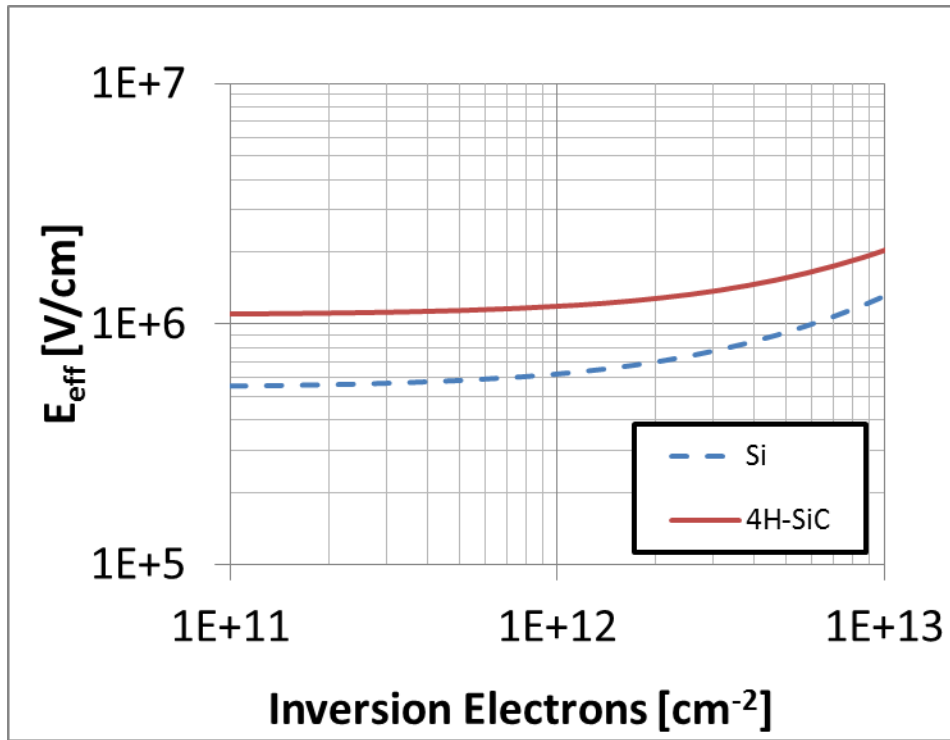
doping $N_A = 1 \times 10^{18}$ cm^{-3}.

Figure 3.9 Comparison of Si and 4H-SiC MOS E_{eff} vs. inversion electron concentration, with p-well doping $N_A = 1 \times 10^{18}$ cm^{-3}.

As a result, SiC may suffer from a greater fraction of electron wavefunction in the dielectric. More study is needed to find out the *f* more quantitatively for SiC. But this can only be a few percent.

In addition, it has been reported that a chemical transition layer exists at the SiO_2/SiC interface, which decreases with NO anneal time [21]. Given that this measurement was done in a cross-sectional TEM geometry, this decrease may represent a reduction of atomic scale roughness or a chemically modified layer. It's still under discussion whether such transition layer exists [22], or how would such transition layer effect Φ_{Be} or the ultimate mobility. In the chemically modified case it is possible that Φ_{Be} is substantially reduced, increasing *f*.

3.6 *Summary*

We have reported measurements of the mobility of the a-face of SiC with the two different passivating agents. These systems show some of the highest inversion mobilities ever reported in SiC. Nevertheless the mobility is still below expectation. In this chapter we discuss possible limiting mechanisms.

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Chapter 4 Nitrogen Incorporation on the a-face of 4H-SiC

Incorporation of nitrogen at the SiC/SiO2 interface has proven very effective for defect passivation and counter doping, both of which in turn improve the mobility. So it is of interest to systematically study the N uptake behavior on a-face. Section 4.1 describes the fabrication and test procedures used in this study, and section 4.2 shows the interface trap density (Dit) for different NO anneal time. Depth profiling is studied by Secondary Ion Mass Spectrometry (SIMS) as shown in section 4.3. Nitrogen coverage at the interface is extracted by XPS and the uptake curve of N vs. anneal time is presented in section 4.4. In the end, the correlation of interface trap density (N_{it}) and N incorporation as well as anneal time is summarized in section 4.5.

4.1 *Fabrication and test*

Five pieces of a-face n-type 4H-SiC samples with ~10 um epitaxial layers doped with nitrogen at ~ $1x10^{16}$ cm^{-3} are used for this study. Following a standard RCA cleaning process, samples underwent dry oxidation at 1150°C for 1 hr. All the samples are subjected to NO annealing at 1175 °C for different times to vary the N coverage at the interface, i.e. 0min, 7.5 min, 15 min, 30 min and 90 min. Then 600μm diameter gate metal circle caps are patterned by Aluminum liftoff. Back oxide is removed by HF, and silver paste is used to attach samples onto a larger carrier sample and form the back ohmic contact.

Interface trap density (D_{it}) measurements were first performed using the simultaneous high (100 kHz)-low frequency (quasi-static) CV technique at room temperature. Following the D_{it} measurements the front side gate and back size metals are removed,

retaining the oxide, and sent out for SIMS measurement. Finally the oxide is removed by HF, and XPS measurements are done on the exposed interface. In this way, we determine the interface N coverage density with anneal time on the a-face, and the correlation of N incorporation with electrical performance in terms of D_{it}.

4.2 *Interface trap density (D_{it}) vs. anneal time*

Figure 4.1 compares Dit with different NO anneal times at 1175°C. The first 7.5min passivates most of the traps and reduces D_{it} by 10×. Additional anneal times further reduce the defects only marginally. The values saturate at ~5×10^{11} cm^{-2}eV^{-1}.
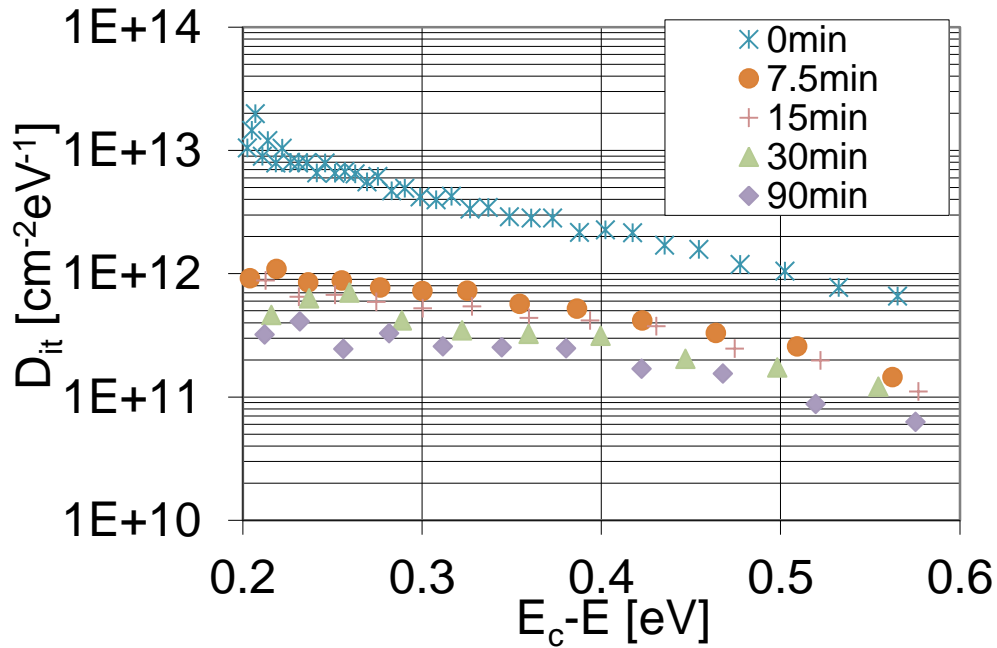
Figure 4.1 a-face D_{it} evolution with NO anneal time, 0, 7.5, 15, 30, 90, from 0.2 to 0.6 eV below the conduction band (E_C), extracted from 'hi-low' C-V measurements.

4.3 *Depth profiling by Secondary Ion Mass Spectrometry (SIMS)*

Secondary Ion Mass Spectrometry (SIMS) profiling is shown in Figure 4.2, for 4 samples

with NO anneal times from 7.5 min to 90 min. As the species of interest, only N

concentration is calibrated to atoms/cm^{-3}, and Si, O and C are used to mark the interface

position, shown in arbitrary units on the right side.

There are two major points from this plot, (1) N is piling right at SiO_2/SiC interface,

which is at ~600 Å depth on horizontal axis and not in the bulk oxide; and (2) the N

concentration starts high at 7.5min and increases with longer anneal time, yet beyond

30min there is no distinguishable difference with SIMS resolution.
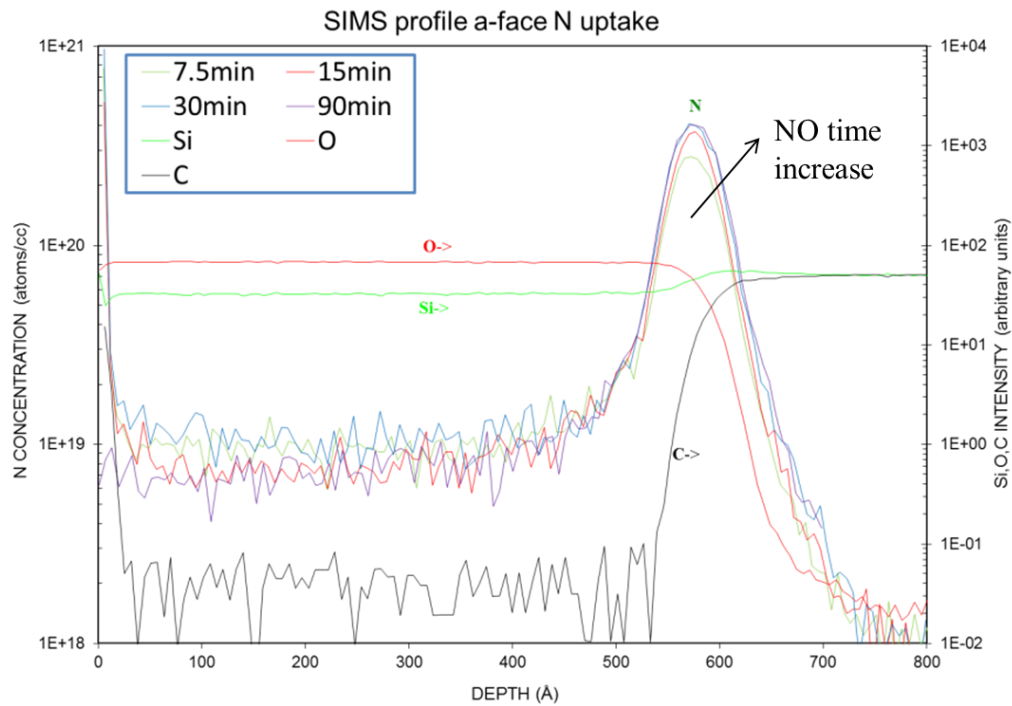
Figure 4.2 SIMS result profiling through the gate oxide, interface and bulk SiC, N concentration is calibrated to atoms/cm^{-3} to the left side vertical axis, and Si, O and C are in arbitrary units to the right side vertical axis.

It is interesting to compare these N profiles on a-face to that on Si-face, shown in Figure 4.3 that is reproduced from John Rozen's dissertation [1]. On both a-face and Si-face, N is piled up at the interface. As shown below the N binding energy is the same across different faces (Figure 2.11).
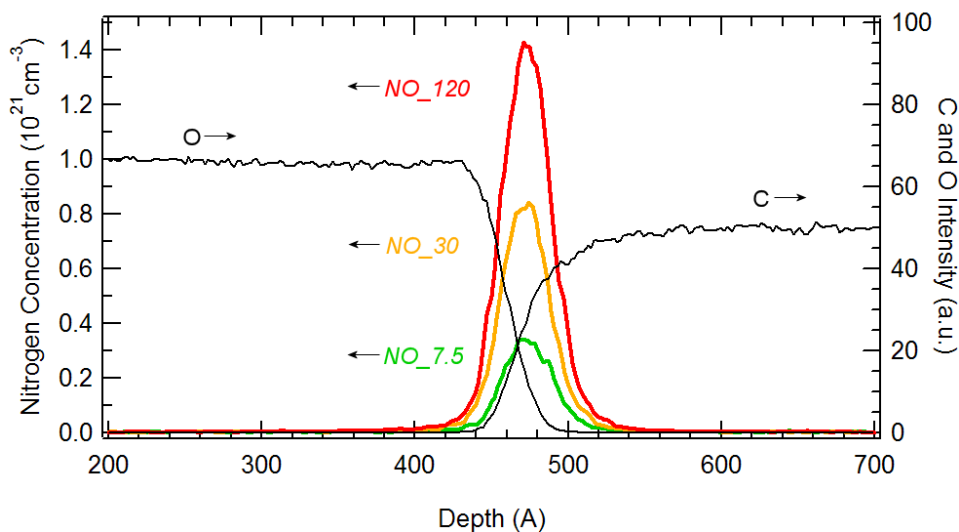
Figure 4.3 Si-face, SIMS profiles for the samples annealed in NO for 7.5 min, 30 min and 120 min [1].

4.4 *Nitrogen uptake curve*

The a-face N areal densities at different anneal times are studied systematically and quantitatively by XPS that is calibrated by MEIS results. The a-face N uptake is compared with that on Si-face and C-face, at the same anneal temperature, i.e. 1175°C, shown in Figure 4.4. The curves can be fitted by simple, first order Langmuir kinetics, i.e. $y = A \times \left(1 - e^{-t/t_o}\right)$, where A=6.9×10^{14} cm^{-2} and t_o=6.6min for a-face. N coverage

saturate at the highest rate and with the largest density on the a-face. Saturation N atomic coverage are 6.9×10^{14} cm^{-2} on a-face, 6.7×10^{14} cm^{-2} on C-face, 4.0×10^{14} cm^{-2} on Si-face.
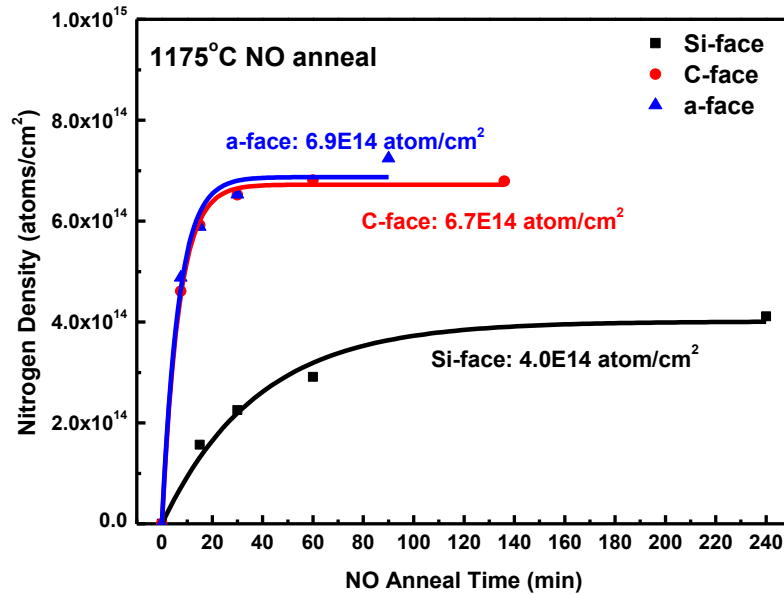
Figure 4.4 Comparison of a-face, Si-face and C-face N content dependence of anneal time. The points are XPS experimental measurements and solid lines are fitted curves using simple, first order Langmuir kinetics.

A similar trend also exists in the oxidation process across the different crystal faces. The mechanism of nitric oxide (NO) post-oxidation annealing is not yet completely understood. Comparison of the nitrogen uptake rates with oxidation rates (reproduced in Figure 4.5 from S. Dhar's dissertation [2]) demonstrates that nitrogen incorporation is closely related to the oxidation process [3].
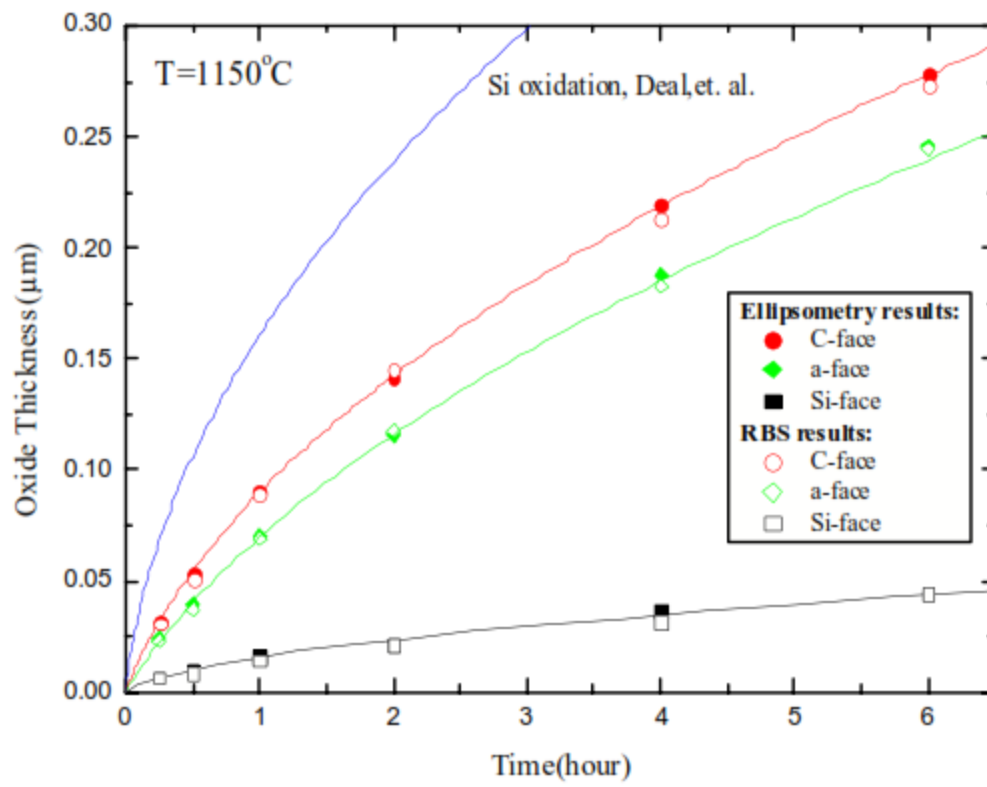
Figure 4.5 a-face, Si-face and C-face dry oxidation curves at 1150°C, the solid symbols are ellipsometer results and the opened symbols are RBS results [2].

4.5 *Correlation of Interface trap density (N_{it}) and N density*

For MOSFET that is limited by coulomb scattering, inversion layer mobility performances is strongly dependent on the total interface trap density (N_{it}). We define N_{it} as the energy integral of D_{it} over the interval of 0.2 to 0.6 eV, the best available range from this measurement technique. N_{it} for NO anneal times from 0min to 90min are 11.6, 1.9, 1.5, 1.0, 0.7×10^{11} cm^{-2}, and plotted as a function of N density and NO anneal time (Figure 4.6). Nitrogen effectively passivates most of the interface defects in 7.5min, and continues reducing N_{it} marginally with greater N coverage.
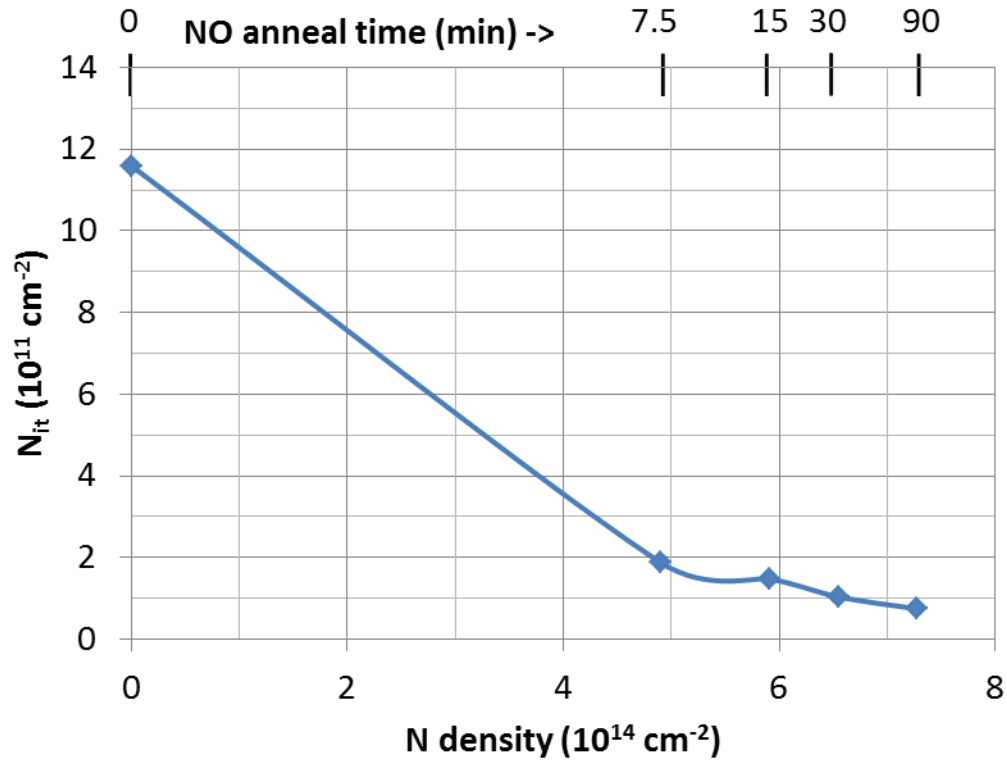
Figure 4.6 N_{it} (0.2~0.6eV below E_c) as a function of N density (bottom axis) and NO anneal time (top axis).

As mentioned in section 1.6.2, D_{it} and mobility across the three different crystal faces at saturated N coverage have been reported, and no monotonic relation was found (Figure 1.13).

4.6 *References in Chapter 4*

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Chapter 5 Reactive Ion Etching Effects on Mobility and its Recovery

5.1 *Introduction*

The need for high power, high temperature, and energy saving electronics has led to increased interest in wide band gap MOSFET type devices. Enhancement in the basic crystal quality of 4H-SiC and significant advances in interface passivation suggest that such a MOS based technology can be realized using this material. The trench MOSFET (or U MOSFET) is a desirable device configuration for this application given its higher current density compared to other common structures, particularly the double-diffused or D-MOSFET structure. Trench devices usually employ the Si-face or C-face of a SiC wafer, with trench side walls, typically formed by Reactive Ion Etching (RIE). The side walls may correspond to crystalline a-faces, including the $(11\bar{2}0)$ face. This particular crystal face yields higher mobility than the Si-face, given the same post oxidation anneal [1][2][3][4][5]. Ideally this is advantageous as the sidewall forms the majority of the channel. However early reports of a practical high voltage UMOSFET formed with RIE trench found very extensive roughness on the sidewall after RIE as measured by AFM, and even worse after an implant activation anneal. The crystal structure cannot be recovered even following two sacrificial oxidation cycles [6].

Other work reported high mobilities in short channel (typically a few μm) devices on various faces in UMOSFETs formed by RIE [7],[8],[9] followed by sacrificial oxidation [7],[8] or H_2 etch [9] to remove plasma damage.

It has been found that the most effective gases for SiC dry etching are usually based on fluorine chemistry, i.e. $Si + xF\text{->}SiF_x$ and $C + xF\text{->}CF_x$. And it is reported that a SF_6/Ar combination at 10:40sccm ratio yields a smoother uniform surface compared to the SF_6/O_2 recipe [10], thus was adopted in this study.
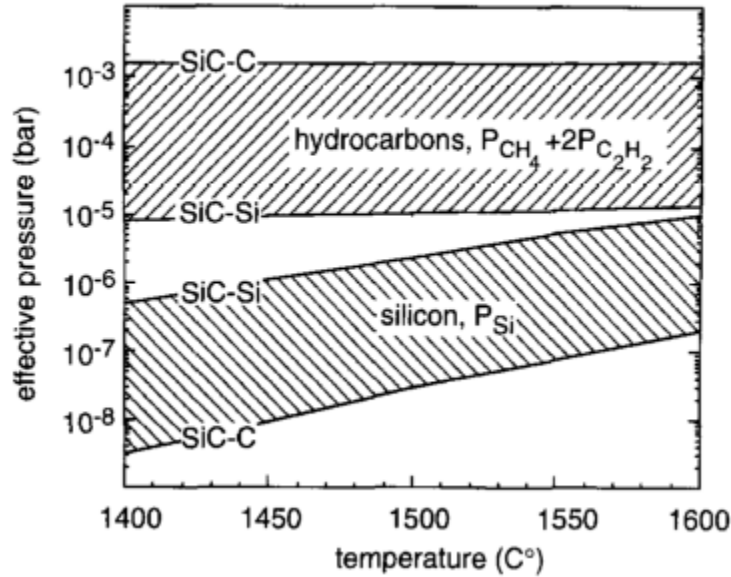
Figure 5.1 Temperature dependence of equilibrium pressures for SiC decomposition products under

1 atm hydrogen gas [12].

Etching in H_2 is effective in improving surface morphology to create atomically flat surfaces, on Si-face, C-face and other faces [12][13][14]. In such a high temperature etching process, the major reaction products are CH_4, C_2H_2 and Si [12].

For trench structures, H_2 etching has also been proven effective in recovering the surface on both side wall and bottom [14].
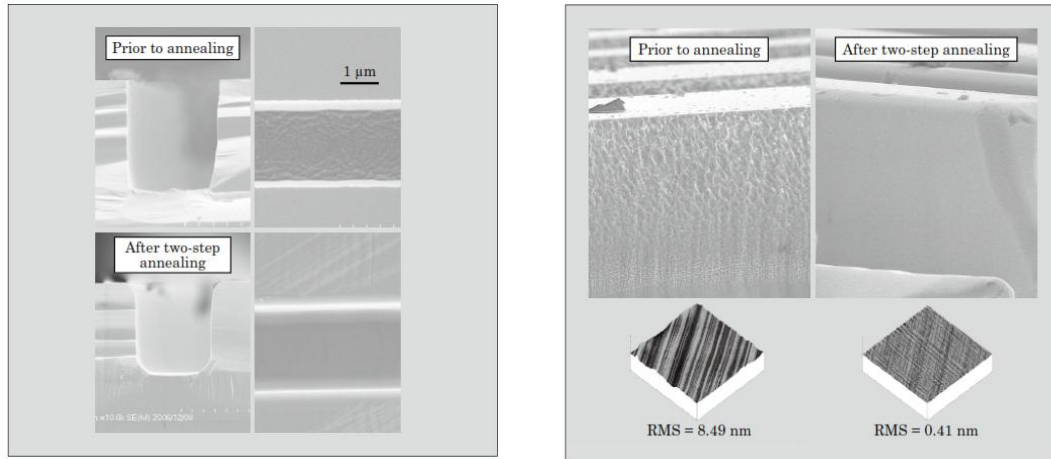
Figure 5.2 Improvement in trench shape, sidewall and bottom flatness after 'two-step' annealing, i.e. 10 minutes at 1,700 °C in SiH$_4$/Ar then 10 minutes at 1500 °C in H$_2$. The first step is effective for obtaining rounded trench corners, and the second step obtains a smooth surface without changing the trench shape[14].

In this dissertation the damage and annealing processes are studied in a model system consisting of a-face 4H-SiC material that is described in section 5.2. We report MOSFET channel mobilities from high quality epitaxially prepared surfaces, from surfaces having undergone a RIE process and surfaces subjected to a H$_2$ etch recovery in section 5.3. The mobility is measured on long-channel (150μm) device, with precise channel dimensions and CV extracted oxide thickness, to assure the precision of the mobility values. The mobility is correlated to the measured CV behavior (section 5.4) surface roughness (section 5.5), crystal structure (section 5.6) and chemical bonding (section 5.7) at each step. Hydrogen etching is proven to be effective in roughness and mobility recovery. The roughness induced mobility reduction mechanism is also discussed (section 5.8).

5.2 *Fabrication and test*

Using a well-cut, a-face, 4H SiC wafer with a p-type epitaxial layer (Al doping ~1 x

10^{16} cm^{-3}) , n+ source and drain areas were formed by nitrogen implantation at 700°C

with different energies and doses, to form a box profile into SiC (<400nm) with n-type

doping of 6 x 10^{19} cm^{-3}. The implanted nitrogen is then activated and the implantation

damage annealed thermally at 1550°C for 30 min in an Ar ambient, with the surface

protected by a graphite cap. After annealing, the cap is removed by an O_2 plasma etch. A

thick sacrificial oxide is then grown to recover the intrinsic surface from any affect

caused by the previous processes.

MOSFET-type device fabrication for channel mobility evaluation included the following

steps: , i) RCA cleaning, ii) thermal oxidation in pure O_2 at 1150°C for 1hr , iii) a 2hr

NO anneal at 1175°C, resulting in a total gate oxide thicknesses of ~ 55nm. Then the

source and drain areas are exposed by HF etching of the sacrificial oxide and Al is

deposited and patterned to form ohmic contacts. Finally the gate contact is formed by

patterned Al deposition.

 A complimentary MOS capacitor (MOSCAP) is fabricated on an n-type companion

sample fabricated at the same time through the oxidation and NO anneal steps for

interface defect evaluation, D_{it}. The MOSCAP's are formed by Al deposition and

patterned on the gate oxide. Silver paste forms an ohmic contact on the back the sample

after oxide removal by HF.

Electrical measurements are carried out to extract the field effect mobility on the

MOSFETs and D_{it} from the MOSCAPs.

After initial electrical testing, all electrode metals are removed by wet etch, and the gate oxide removed by HF, exposing the interface surface. AFM measurements are carried out in the channel regions and on companion samples.

The same samples are then exposed to an RIE process, with SF_6 10sccm, Ar 40sccm, RF150W, DC self- bias 250V, pressure 60mTorr, at room temperature and a plasma time of 1min. Approximately 70nm of SiC is removed by this process. After RIE, the oxidation/NO fab process is repeated on the "as-etched" surface" to produce MOSFETs and MOSCAPs for mobility and interface state density measurement. . Following this second round of electrical testing, the oxide is etched off to allow another AFM scan.

 The RIE roughened surfaces are then recovered by exposure to a 1400°C H_2 (2.9% hydrogen in argon, 1slm) etch process, for 5min at peak temperature. This is expected to remove at least tens of nm of SiC. After an AFM evaluation, we repeat the device fabrication and electrical testing procedure used above.

The complete processing flow is summarized in diagram 1.
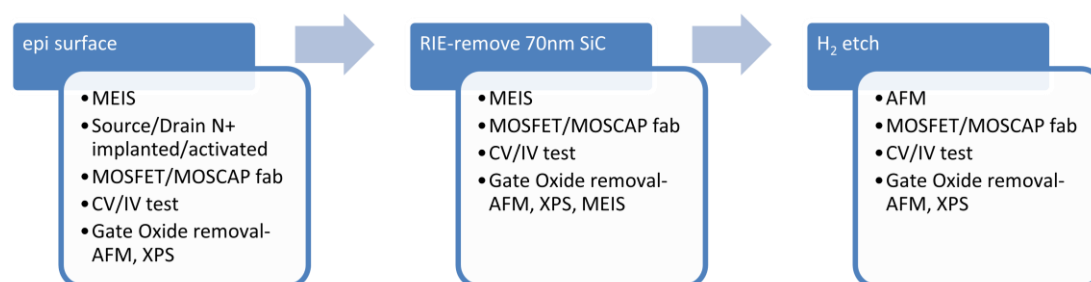
Figure 5.3 Diagram of Overall processing flow.

5.3 *Field effect mobility*

Figure 5.4 shows field effect mobilities comparing the epitaxial grown surface with surfaces that have undergone RIE and H_2 processing. Clearly the RIE process reduces the mobility extensively and the H_2 etch recovers mobility. In addition to lower mobility, the RIE devices show lower yield and early gate oxide breakdown. This sets a limit to the maximum gate voltage possible on the RIE sample as shown in Fig 1.

After the H_2 etch, the ohmic contact resistance is increased significantly. This is due to the multiple oxidations, RIE and H_2 etch processes on the same SiC consuming significant portions of the implanted n+ SiC regions that are essential for ohmic contact. As a result, the evaluated mobility is substantially under-estimated using this formula, $\mu_{FE} = \frac{L}{W C_O V_{DS}} \left(\frac{dI_D}{dV_G} \right) \Big|_{V_{DS} \to 0}$, since the real channel voltage is considerably smaller than V_{DS}. The correction to the mobility due to this effect using data from the Transmission Line Model (TLM) measurement is included as dash line in Figure 5.4.
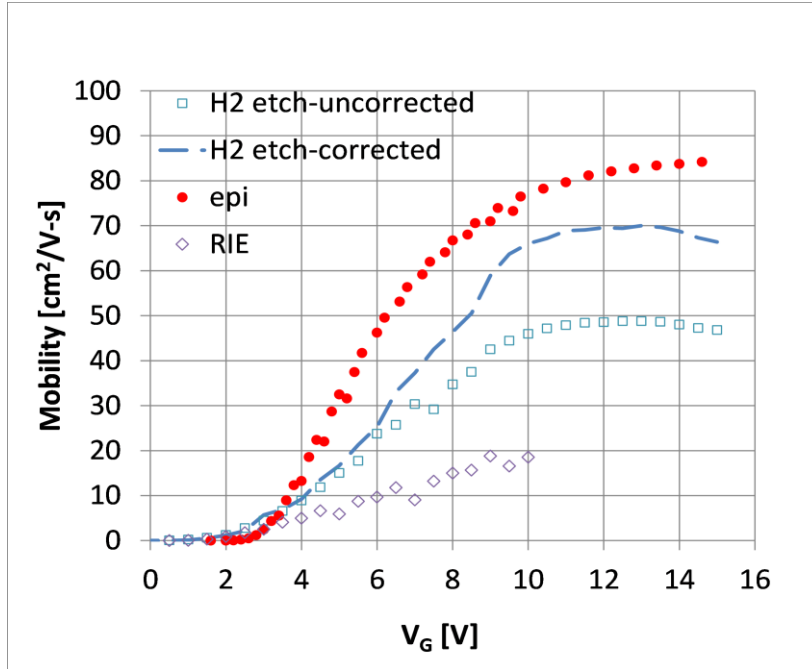
Figure 5.4 Field effect mobilities μ_{FE} with 2hr standard NO anneal, beginning with peak μ_{FE}=85 cm^2/V-s with epi condition, then reduced to μ_{FE} =20cm^2/V-s after RIE roughening and recovered to μ_{FE} =70cm^2/V-s after H$_2$ etch, both corrected and uncorrected results are included.

5.4 *Interface trap density (D_{it}) extracted by the 'hi-low' technique*

The 'hi-low' C-V measurements on companion n-type MOSCAP's and the extracted interface trap density (D_{it}) are shown in Figure 5.5 (a) and (b), for the cases of epi and RIE samples with an NO anneal (H$_2$ etch is the same as epi). Interface state density measurements on a structure without an NO anneal on epitaxial material is also included as a reference [5]. A significant flat band voltage shift is observed and discussed below. NO is effectively passivating the interface regardless of the surface roughness. Although the extraction of absolute D_{it} values via C-V have been questioned [16], and surface roughness in the RIE case may add some error to E_c-E position due to field crowding, the

straightforward comparisons of different processes clearly indicates the major effect of N

interface state passivation.
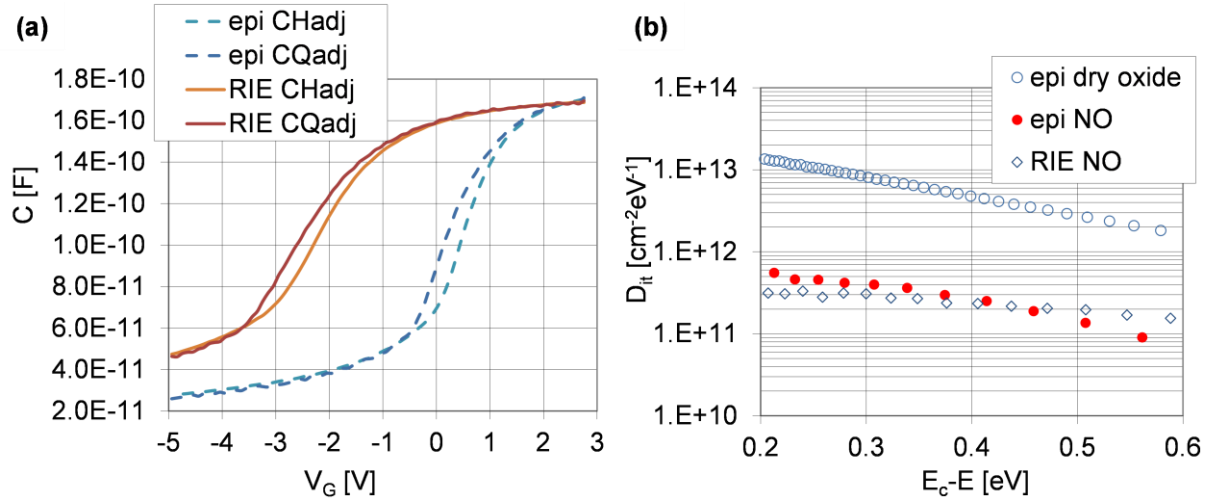
Figure 5.5 (a) 'hi-low' Capacitance-Voltage measurements on companion n-type MOSCAP's, comparing epi (dash lines) and RIE(solid lines) both with NO anneal at 1175°C 2hr. CQ and CH are quasi-static and high frequency capacitance curves. Flat band voltages are 0.85V for epi and -1.12V for RIE. Effective charges are -1.43×10^{+11} cm^{-2} for epi and +6.01×10^{+11} cm^{-2} for RIE. (b) Corresponding Interface Trap Density (D$_{it}$) vs energy 0.2 to 0.6 eV below conduction band. Without NO anneal epi case is also included as reference, shown in empty circles[5], stars and filled circles are epi and RIE with NO anneal at 1175°C 2hr, respectively.

5.5 *Surface morphology by Atomic Force Microscopy (AFM)*
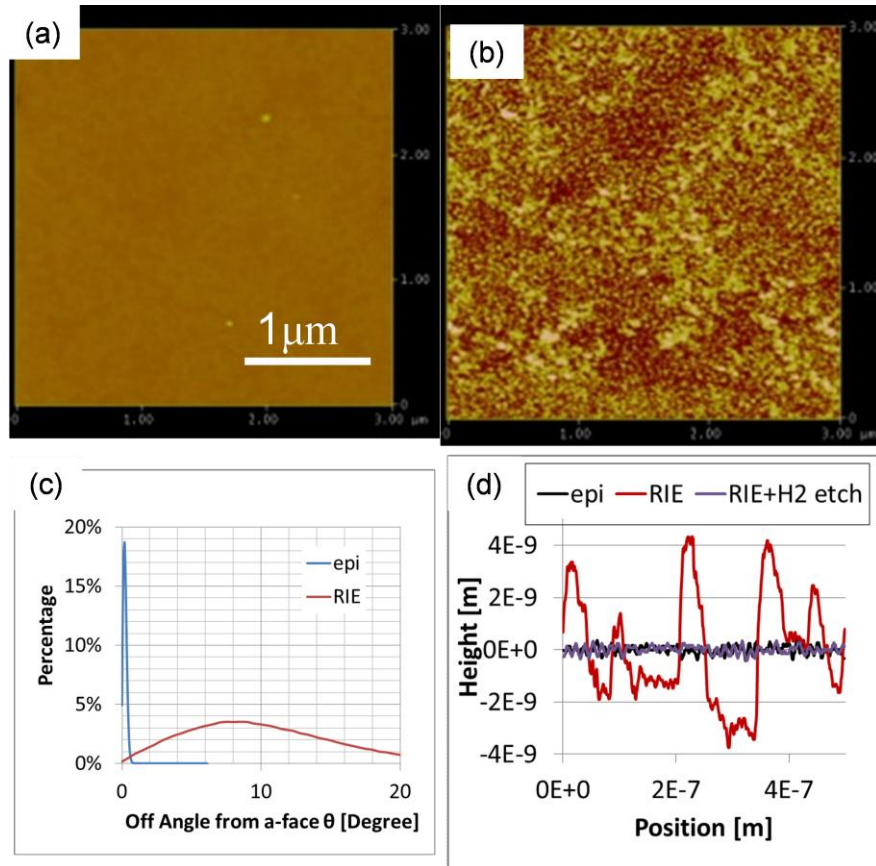
Figure 5.6 AFM surface images of (a) epi, (b) RIE (70nm SiC removed) after MOSFET mobility evaluation and gate oxide removal by HF. H_2 etch recovered surfaces looks identical to (a) epi. The corresponding RMS values are 0.25nm, 4.57nm and 0.28nm respectively. (c) is slope distribution of angle θ from (a) epi and (b) RIE. (d) is the profile of (a) epi, (b) RIE and RIE+ H_2 etch.

A series of accompanying atomic force microscopy (AFM) measurements are used to correlate roughness and mobility. Figure 5.6 shows that the initial atomically flat surface in (a) is seriously roughened by RIE, and thermal oxidation cannot recover the surface

(b). A H_2 etch is proven effective in recovering the RIE roughened surface to the epi-like condition (Figure 5.6d), consistent with earlier reports [14].

Slope distributions in Figure 5.6 (c) are calculated from (a) and (b) in terms of the inclination angles $\theta : \theta = \tanh^{-1}\left(\frac{dz}{dx}, \frac{dz}{dy}\right)$ [17]. This inclination angle θ essentially represent the angle by which the RIE surface locally deviates from a-face plane. For the epi case, the surface is approximately flat (a-face) within error. For RIE with oxidation, the surface might be thought of as facets deviating from the a-face with a distribution of angles, peaking at about 8 degree. Figure 5.6 (d) is the topological profile taken from (b) showing the amplitudes and distances of features on the surface.

5.6 *Crystal quality study by Medium Energy Ion Scattering (MEIS)*

Medium energy ion scattering is a surface characterization technique sensitive to structural imperfections of a surface [18]. Channeling is the steering of an ion beam through the open spaces between rows or planes of atoms in a crystal. The surface peak measured in channeling gives information of the first few monolayers and their crystal structure.
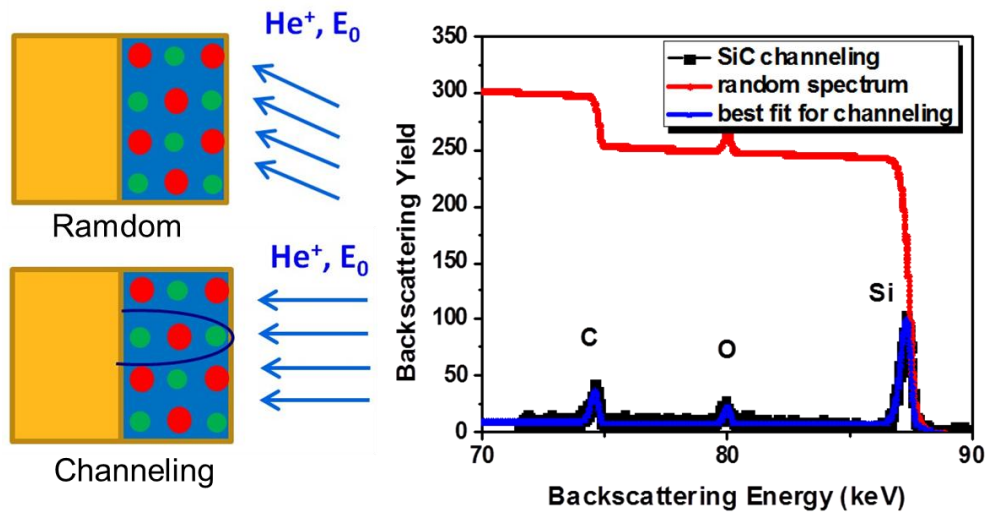
Figure 5.7 Random and channeling ion beam alignment and the corresponding typical spectrums on pristine Si-face 4H-SiC, using 100 keV H$^+$.

Figure 5.8 shows MEIS channeling results that help to better understand the crystal quality of the SiC affected by RIE. The virgin sample is used as a reference.
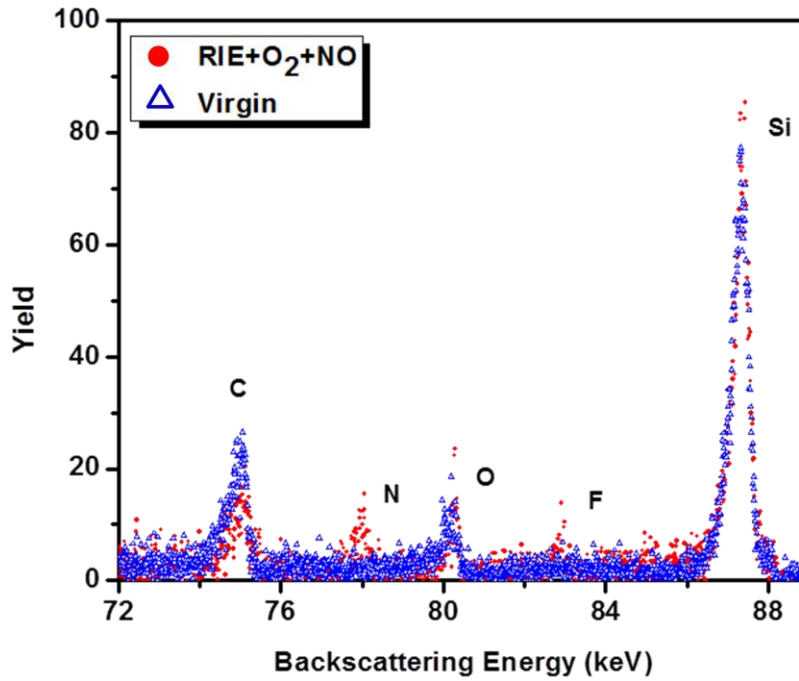
Figure 5.8 MEIS 100 keV H$^+$ channeling spectra on a-face virgin sample (blue triangles, Si : 2.22 x 10^{15} atoms/cm^2, C: 3.58 x 10^{15} atoms/cm^2, O : 7.5 x 10^{14} atoms/cm^2) and then is exposed to 1min RIE and followed by thermal oxidation (O$_2$) and NO anneal, oxide is removed by HF before channeling (red circles, C: 2.26 x 10^{15} atoms/cm^2, Si:2.22 x 10^{15} atoms/cm^2, N: 8.1 x 10^{14} atoms/cm^2, F: 3 x 10^{14} atoms/cm^2, O: 6.7 x 10^{14} atoms/cm^2).

It is known that RIE exposure damages the SiC crystal structure considerably and deposits a polymer film rich in fluorine and carbon, and the polymer can be removed by UV ozone, O$_2$ plasma or thermal oxidation, as summarized in Figure 5.9 from [19].

Sample/final surface treatment	Surface overlayer			SiO$_x$			Substrate SiC	
	C$_F$	F$_A$	C$_{C,O}$	O	Si$_O$	F$_B$	Si$_C$	C$_{Si}$
	287.7–292.5 eV	687.2 eV	283.7–284.6 eV	531.5–532.1 eV	101.7–102.7 eV	685.4 eV	100.4 eV	282.4 eV
Epitaxial 4H SiC wafer	—	—	9% (1.5)	8% (1.1)	—	—	44% (0.5)	39% (0.4)
1 CF$_4$ RIE + solvent	2% (2.9)	12% (0.8)	4% (2.4)	9% (0.6)	5% (0.3)	5% (0.3)	25% (0.3)	36% (0.2)
3 CF$_4$ RIE + UV ozone	—	—	5% (2.0)	24% (0.8)	8% (0.9)	2% (0.4)	27% (0.3)	34% (0.3)
4 CF$_4$ RIE + O$_2$ plasma	—	—	4% (2.7)	38% (0.6)	12% (0.8)	2% (0.5)	21% (0.2)	25% (0.3)
6 CF$_4$/O$_2$ RIE	—	3% (0.9)	—	5% (0.6)	—	7% (0.8)	40% (0.4)	44% (0.4)
8 CF$_4$ RIE + deposited oxide (densified)/ HF	—	—	16% (1.4)	11% (0.6)	—	—	32% (0.2)	40% (0.1)
9 CF$_4$ RIE + thermal oxide/HF	—	—	11% (1.0)	10% (0.9)	—	—	38% (0.5)	41% (0.3)

Figure 5.9 Summary of XPS results from RIE-treated samples after various surface treatments, giving the atomic percentage composition of all detected species (>1 atomic percentage) within the near-surface region sampled at 75° photoelectron take-off angle. Figures in brackets are the ratio of the 15°–75°XPS peak area counts. XPS binding energy ranges (eV) corresponding to each resolved species are also given [19].

In our MEIS measurements, we first confirm that the deposited polymer film is covering the damaged crystal surface, and that after oxygen plasma, the polymer is removed, but surface damage remains (not shown in Figure 5.8). And the 'RIE+O2+NO'(another sample) spectrum shows that thermal oxidation and the NO anneal removes the polymer layer, consumes the damaged SiC layer, forms SiO$_2$ (which was etched off prior to the MEIS measurement) and results in an interface SiC layer with near perfect (virgin) crystal quality. This also confirms that given its low RIE DC self- bias, crystal damage is limited to a shallow depth. Nevertheless this surface did not recover the initial mobility. The NO anneal introduces 8.1 x 10^{14} cm^{-2} N to the interface. The small fluorine intensity p in the 'RIE+O2+NO' spectrum is due to residual HF on the surface left during oxide

removal that isn't completely rinsed off. An H_2 etched surface yields an identical

spectrum to the epi surface that is not shown here.
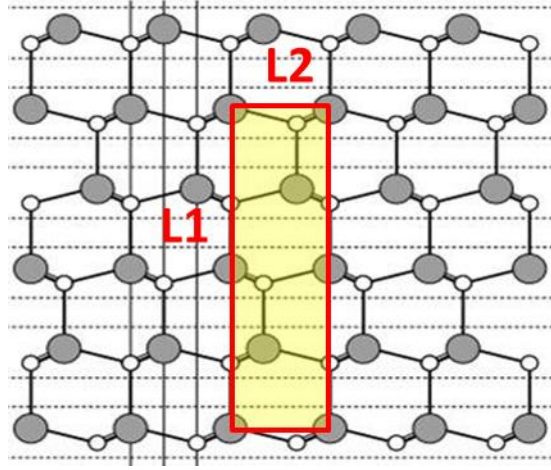
Figure 5.10 Top view of a face SiC, (the same view as the ion beam), the boxed region is the 2-D unit cell for area density calculation. Large filled circles are Si and small empty dots are C atoms. Lattice constant is 3.09 Å.

The Si and C surface peak intensity on the virgin sample can be calculated theoretically

in the following way. In one unit cell (Figure 5.10) there are 4 silicon atoms and 4 carbon

atoms. With $L_1 = \left(4 + 4 \times \frac{1}{3}\right) \times 1.89\text{Å} = 10.08\text{Å}$, $L_2 = 2.67\text{Å}$, area of the unit cell is

$10.08\text{Å} \times 2.67\text{Å} = 26.91\text{Å}^2 = 2.691 \times 10^{-15} cm^2$. So Si areal density is

$\frac{4}{2.691 \times 10^{-15} cm^2} = 1.49 \times 10^{15} atoms/cm^2$, the same as C density. Due to lattice thermal

vibration, ion beam also has chance to see atoms below the surface layer. The Si surface

peak taking the second layer into consideration will be $1.49 \times 10^{15} atoms/cm^2 \times$

$(1 + I_2) = 2.0 \times 10^{15} atoms/cm^2$, where $I_2 = e^{-\frac{R_c^2}{2\rho^2}}\left(1 + \frac{R_c^2}{2\rho^2}\right) = 0.33$ is the

probability second layer is exposed to the beam, $R_c = 2(\frac{Z_1 Z_2 e^2 d}{E})^{1/2}$ is the shadow cone

radius, for 100keV silicon, $R_c = 0.159\text{Å}$ and $\rho = \sqrt{\rho_{Si}^2 + \rho_{Si}^2} = 0.074\text{Å}$ is the relative thermal vibration amplitude [18]. MEIS result of Si peak size is $2.2 \pm 0.1 \times 10^{15} atoms/cm^2$, in very close agreement with theoretical prediction.

5.7 *Chemical bonding study by X-ray photoelectron spectroscopy (XPS)*

XPS is used to study and compare N bonding and coverage at the epi and RIE MOS interfaces. The N 1s photoelectron energy gives the same binding energy within the energy resolution of the spectrometer, indicating that the nitrogen binding site is the same in both cases. The total N coverage is $6.6 \times 10^{+14}$ cm^{-2} on the epi and $8.2 \times 10^{+14}$ cm^{-2} on the RIE surface. This coverage difference may be due to: (1) the RIE induced roughness which increases the initial surface area by ~27%, based on AFM results, close to the measured N increase or (2) a crystal face dependent N coverage saturation level.

5.8 *Discussion*

The MEIS analysis (Figure 5.8) makes it very clear that SiC crystal structure is recovered at the oxide/SiC interface for the RIE+O2+NO sample. CV measurements show that the RIE-NO sample has a similar near conduction band D_{it} with epi (Figure 5.5b), consistent with the similar effective N coverage. However, there is a huge difference in effective charges between the two cases, both in magnitude and polarity, i.e. $-1.43 \times 10^{+11}$ cm^{-2} for epi and $+6.01 \times 10^{+11}$ cm^{-2} for RIE. This large amount of positive charge (presumably in the near interface oxide) can either act as centers to scatter carrier electrons to reduce the mobility and/or trap electrons at the interface.

The source of such positive charge in the RIE sample is probably not due to massive crystal damage as MEIS reveals a well-ordered structure. However the sensitivity of MEIS to structural defects is only ~1%, and may not detect defects at levels which give rise to anomalous electrical behavior. The difference in charge may be related to the complicated morphology (Figure 5.6 (c)), compared to the case of epi with an "ideal on a-face" structure. The RIE sample consists of surfaces that deviate from the perfect a-face by various angles with a distribution peaked at ~8° off the normal. It is known that oxide growth mechanisms are different on the Si face and C-face, and a large oxidation rate anisotropy may possibly lead to a complex, non-planar surface. A H_2 etch can recover the mobility and sacrificial oxidation cannot, as the latter is generally conformal to surface morphology while the former can actually restore surface flatness to the correct crystal face.

Finally, the AFM (Figure 5.6d) shows dominant roughness features spaced by ~100nm, much greater than the mean free path extracted from the measured mobility, ~1nm. The AFM is currently resolution limited and cannot reveal features on this scale, which may be setting the ultimate mobility.

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Chapter 6 Conclusion

This dissertation concerns the 4H-SiC MOSFET interface structure, defect states and

inversion layer mobility on the $(11\bar{2}0)$ a-face using nitrogen and phosphorous passivation

methods. In addition the recovery of the surface properties following reactive ion etching,

an important step in device fabrication is explored. We correlate electrical measurements,

i.e. current-voltage (I-V) and capacitance-voltage (C-V) with physical characterizations

including X-ray photoelectron spectroscopy (XPS), Atomic Force Microscopy (AFM),

Transmission electron microscopy (TEM), Secondary Ion Mass Spectrometry (SIMS),

Helium Ion Microscope (HIM) and Medium Energy Ion Scattering (MEIS).

A significant phosphorus induced inversion layer mobility enhancement of ~125 cm^2/V-s

is achieved, and the revisited effect of NO on the a-face of 4H-SiC also yield an

impressive mobility of ~85 cm^2/V-s. These results indicate that N and P interface

incorporation improves the interface both by passivation and by interfacial counter

doping, with the latter mechanism more effective on the a-face than the Si-face. The

interface trap density (N_{it}) and mobility-temperature dependence both indicate coulomb

scattering is no longer the limiting factor for the N and P annealed a-face inversion layer

mobility. Other possible limiting mechanisms are discussed. Nitrogen incorporation on

the a-face is systematically studied, revealing that on a-face N saturates faster to a higher

level compared with other crystalline faces, and passivates interface traps.

We also report the use of hydrogen annealing to implement the successful recovery of the

a-face $(11\bar{2}0)$ crystal structure and the inversion layer mobility following degradation by

reactive ion etching (RIE). The results impact the processing of SiC trench MOSFETs

where the a-face sidewall forms a significant portion of the conducting semiconductor

channel.