ZINC OXIDE-BASED RESISTIVE SWITCHING DEVICES

by

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ABSTRACT OF THE DISSERTATION

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Recently, resistive switching (RS) memory devices have attracted increasing attentions due to their potential applications in the next-generation nonvolatile memory. Zinc Oxide (ZnO) - based RS devices possess promising features, such as well-controlled switching properties by in-situ doping and alloying, low-temperature fabrication processes, superior radiation hardness, and low cost. The goal of the research is to study the feasibility of using the transitional metal (TM) doped ZnO for making RS devices.

The Fe-doped ZnO (FeZnO) is used to make the bipolar and unipolar RS. The FeZnO is grown through MOCVD. Fe is a deep-level donor in ZnO, and Fe doping leads to better device thermal stability and larger value at the high resistance state (HRS) for switching. For the Ag/FeZnO/Pt bipolar RS structures, the ratio of the HRS over the low resistance state (LRS) of 3.8×10^2 is achieved. The dominant conduction mechanisms are attributed to the Poole-Frenkel emission at the HRS and Ohmic behavior at the LRS, respectively. A FeZnO/MgO bi-layer (BL) is used to replace the FeZnO single layer (SL) to form an Ag/FeZnO/MgO/Pt bipolar RS structure. This BL device demonstrates a higher R_{HRS}/R_{LRS} ratio ($\sim10^6$) than the SL counterpart. For the Au/FeZnO/MgO/Pt unipolar RS device, the R_{HRS}/R_{LRS} ratio of 2.4×10^6 at 1V is achieved.

In order to reduce the processing temperature, the Ni-doped ZnO/MgO BL structure is adapted to make the RS devices using the sputtering - MOCVD hybrid deposition. The Ni doping enhances the compensation of oxygen deficiency in ZnO, resulting in larger HRS values. By controlling the compliance current during the "SET" process, three different reversible RS modes, i.e. threshold switching, volatile switching, and memory switching are obtained. Compared with the memory switching, the volatile switching possesses lower power consumption and better HRS stability. Furthermore, the different compliance currents lead to the different LRS values, which could be used for the multi-level per storage cell applications. The electrical characteristics and microstructure analysis suggest that the compliance current setting affects the formation and rupture of the metallic filaments, leading to the conversion of different switching modes.

The FeZnO switching resistor (R) is vertically integrated with a ZnO diode (D) to form the 1D1R structure, which overcomes the cross-talk in the 1R-based crossbar switching matrix. The 1D1R exhibits high R_{HRS}/R_{LRS} ratio, excellent rectifying characteristics, and robust retention. The new ZnO RS technology presents great impact on the future classes of memory devices for applications such as switching matrix, multi-level storage, and 3D non-volatile memory architecture.

DEDICATIONS

To my Ph.D thesis advisor, Dr. Yicheng Lu

And my master degree advisor, Dr. Jinmin Li

To my father, Xuping Zhang

And my mother, Jing Sun

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Introduction

1.1. Motivation

In the last several decades, computer memory develops rapidly by reducing the size of the unit cell and increasing the intensity of the memories. However, conventional memory techniques are facing numerous scaling and reliability challenges when the characteristic dimension reaches to the physics limitation. To solve the problems, resistive random access memory (RRAM) is emerging as an important nonvolatile memory (NVM) technology [1]. The oxide-based resistive switching devices have inspired substantial scientific and commercial interests due to their simple structure, great scalability, fast operating speed, and low power consumption [2-4]. Among them, ZnO-based resistive switching devices possess promising features, such as well-controlled switching properties through *in-situ* doping and alloying, and low cost due to its abundant material source and relatively simple processing. Furthermore, the multifunctional properties such as semiconducting and resistive switching of ZnO can be achieved through the proper doping process, facilitating the device integration.

It has been proposed that resistive switching in oxides is attributed to the formation and rupture of the conductive filaments in the oxides, which are closely related to the oxygen vacancies and oxygen ions [2, 5], or metal ions [6]. However, the difficulty in control of the length and amount of the conductive filaments in the resistive memory fabricated using the single layer (SL) oxide structure prevents the device from achieving a high and stable R_{HRS}/R_{LRS} ratio, which could cause false programming and readout hazards. To overcome these problems, several oxide-based bilayer (BL) structures have

been reported. These BL structures have better control on the switching parameters and improve the performances of the resistive memory devices. Up to date, there has been no information on the BL structures used in ZnO-based resistive switching devices though ZnO has shown promising multifunctional properties for integrated RRAM applications. In this research, we fabricated Ag/FeZnO/Pt (SL) and Ag/FeZnO/MgO/Pt (BL) structures for resistive switching. Their current-voltage (*I*–*V*) characteristics are analyzed and compared. The transition metal (TM) Fe, is used to form the $Fe_xZn_{1-x}O$ (x~4%) films which serve as the switching layer. In the ternary $Fe_xZn_{1-x}O$, most Fe atoms tend to be in a Zn substitutional site with a small displacement due to the similar ionic radius as Zn. Fe has superior thermal stability over other TM ions in the ZnO lattice [7, 8]. These properties could result in higher structural quality of the material and better endurance performance for resistance switching. Fe is a deep level donor in ZnO [9, 10], and Fe doping could increase the resistivity of the HRS for resistive switching [11].

There are several issues related to the mechanism of the resistive switching that need to be clarified. For example, different polarities of the resistive switching have specific applications; therefore understanding of the reason for the unipolar and bipolar RS and the relationship between them are critical for further development of resistive switching. In addition, the cause for the switching between the HRS and LRS is worth studying in order to optimize the RS parameters, such as the ratio of R_{HRS}/R_{LRS}, the parameter dispersion, and the endurance performance. Compared to the memory RS, the threshold RS is a volatile memory, which could serve as a good switch device to control the random access to specific memory cells. Due to the difficulty of finding the reading voltage and the relative stable LRS in threshold switching, a medium mode, which is

called the volatile switching mode, becomes more important in the practical application. Free of another reset process, low operation current, and possible faster speed turn this kind of switching into a promising complement for regular memory switching. The conversion between these three RSs will be discussed in the electrical characteristics and TEM analysis.

The crossbar array provides for both high density and easy multi-bit operation; therefore, is preferred for the applications in nonvolatile memory and reconfigurable switching matrix. However, if the crossbar array only consists of a resistive switching device (1R) between the top and bottom electrodes, during reading process on one R cell in HRS, the parasitic current can easily flow through the nearby cells in LRS, leading to reading disturbance among the neighboring cells, thus causes fake readout signals. The 1D1R cell consisting of a diode (1D) and a switching resistor (1R) is ideal for avoiding such malfunction in the crossbar configuration because the diode's rectifying behavior under the reverse bias could eliminate the cross-talk. There are two types of resistive switching devices: the unipolar one in which the resistive switching between low-resistance state (LRS) and high-resistance state (HRS) is only dependent on the magnitude of applied voltage, but independent of the polarity; and the bipolar one in which the SET (switching from HRS to LRS) and RESET (switching from LRS to HRS) processes occur under the applied voltages with different polarities. There are unique advantages of using the unipolar switching device over the bipolar counterpart in the crossbar system. First, the unipolar resistive switching only depends on the magnitude but is independent of the polarity of the applied voltage, leading to easy operation with the unipolar voltage source. Second, the different absolute values of the SET and RESET

voltages can prevent reading/writing confusions under multiple-control signals. The vertical 1D1R structure is ideal for such crossbar configuration as it can significantly save the cell area to $4F^2$ (F is the minimum feature size), thus increase the memory density. Furthermore, the vertically integrated 1D1R is preferred for 3-dimensional (3-D) integration.

However, 1D1R crossbar structure applications also have their limitations. 1D1R array is a passive crossbar matrix, which just connect the word and bit lines at each node. For the simple digital circuits, there are only high voltage, which is recognized as the signal “1”; and low voltage, which is recognized as the signal “0”. There is no simple medium voltage which could RESET the node for unipolar RS. For further complicated application the crossbar system has to be controlled by the outside circuits. Alternatively, the RS device could be organized in an active array comprising of a transistor at the node which disable the RS cell if it is not addressed. Regular voltage could SET the node and the reversed voltage could RESET for the bipolar RS. ZnO-based thin film transistor is an emerging transistor for the active 1T1R memory integration for flexible memory application.

The aim of this interdisciplinary work is to enhance the performance of the resistive switching and stimulate integration based on the resistive switching devices. 1D1R and other integration structures can serve as the basic circuit building block for reconfigurable switching matrix and nonvolatile memory (NVM).

1.2. Objectives and Scope of Work

The objectives of this research are to design, fabricate and characterize the ZnO-based resistive switching devices and explore their integration with other ZnO devices. The scope of this study covers:

(1) Design and development of the ZnO-based resistive switching devices, including the unipolar and bipolar switching devices. Study its conduction mechanism through simulation and curve fitting of the current in the HRS and LRS. Adapt the ZnO/MgO bilayer structure as the active layer in the resistive switching device to enhance the resistive ratio and the stability of the operation parameters.

(2) Investigation on conversion of different resistive switching modes in similar structure. Through compliance current setting, we could achieve the conversion between the threshold switching, volatile switching and memory switching, but control the operation parameters. TEM characteristics are also used to prove the assumption with the electrical analysis.

(3) Integration of the TM-doped ZnO resistive switching device with other ZnO devices to explore its applications. The unipolar switching device is vertically integrated with a diode into the 1D1R structure for switching matrix. The bipolar switching device is integrated with thin film transistor into 1T1R for non-volatile memory on flexible substrate.

1.3. Organization of the Dissertation

After establishing the motivation and the specific objectives and scope of this research in Chapter 1, a review of the related work on ZnO-based resistive switching in Chapter 2. Chapter 2 also provides a background on the technical approach employed in

designing ZnO switching devices and related integration. In Chapter 2 the review for the mechanism discussion on the resistive switching is also presented. Chapter 3 includes a discussion of the characterization of the ZnO-based bipolar and unipolar resistive switching devices. A detailed description of the experimental results is also presented on the bilayer structure study for the switching parameter optimization. Chapter 4 deals with the conversion of different switching modes. The switching modes included the threshold switching mode, volatile switching mode, and memory resistive switching mode. Chapter 5 presents the integration of resistive switching devices with diode and other devices. The optimization for the vertical Schottky diode is also discussed. Finally, Chapter 6 summarizes the results of the dissertation research and presents further work.

Chapter 2

Technical Background

Resistive switching device is a new fundamental circuit element, whose resistance depends on the history of applied voltage (magnitude, polarity, and duration). Compared with other charge-storage memory, the oxide resistive switching memories (OXRRAM) are emerging as nonvolatile memory technology due to their ability of scaling, high storage density, fast write time, and low power operation. ZnO RRAM devices can be built on glass and SiO_2/Si substrates, offering full optical transparency, large ON/OFF ratio, fast programming speed, and long retention time. ZnO-based resistance switching device possess several advantages, including well-controlled switching properties through in-situ doping and alloying, a simple fabrication process, and radiation hardness. ZnO resistive switching device in an ultra-high-density configuration possess both the non-volatile characteristics of ROM and the high speed of DRAM and SRAM. In this chapter, the role of ZnO in the field of resistive switching research will be discussed. Various reported switching devices and related integration based on ZnO operating in different modes will also be discussed in this chapter.

2.1. Basic Memories and Technical Challenges

Semiconductor memory is a critical part of digital systems in computers for storing data and programs. As shown in Figure 2.1, there are two different types of computer memories: volatile memory and non-volatile memory. Volatile memory requires power to maintain the stored information, in other words it needs power to achieve the function of memory. Volatile memory retains the information as long as

power supply is on, but when power supply is off or interrupted, the stored memory is lost. Static Random Access Memory (SRAM) and Dynamic RAM (DRAM) are two main memory devices in the volatile memory. SRAM utilize static latches as the storage cells and DRAM storage the binary data on capacitors, which could reduce the feature size of the unit cell. The operation times for SRAM and DRAM are short (0.3 ns for SRAM and 10 ns for DRAM), but the density is very low because of the large size of the unit cell ($140F^2$ for SRAM and $6F^2$ for DRAM, F is the minimum feature size). In addition, SRAM and DRAM could only be used for the temporary data, because when the power is off, the memorized information will disappear.

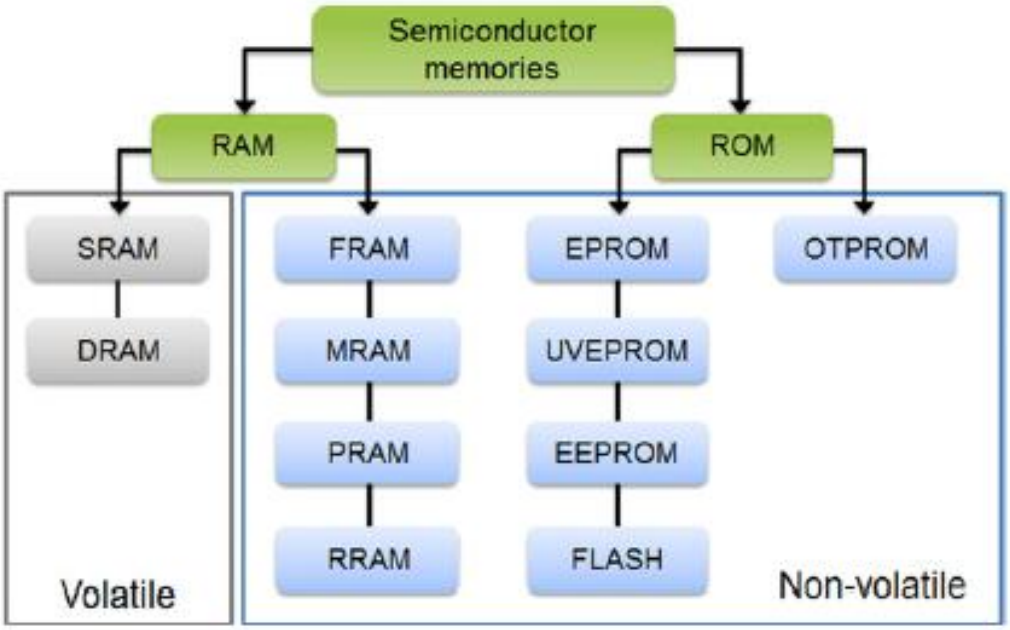


Figure 2.1 Categories of standard semiconductor memories and emerging memories [12].

Non-volatile memory is another type of computer memory that can retain stored information even when not powered. Examples of non-volatile memory include read-only memory, flash memory, ferroelectric RAM (F-RAM), most types of magnetic computer storage devices (e.g. hard disks, floppy disks, and magnetic tape) and optical discs. Normally these kinds of memories has longer operation time (larger than 10 ns), however because of relative small unit size and non-volatile characteristics, they are the important components in the computer memory.

In order to overcome the disadvantages in both types of the well-developed memories, there are several expectations and requirements for the next generation of memory technology.

Unit cell size: Memory density is a critical aspect in the performance. Currently the common memory has the minimum unit size of $6F^2$. The unit cell size for the next generation memory should be in the range of $4F^2$ to $6F^2$.

Writing and reading operation: The operation voltage of the memory should be less than 10 V to protect the active layer and the reading voltage cannot be less than one tenth of writing voltage.

Resistance ratio and stability: Normally the ratio for memory is larger than 10 to identify the signal "1" and "0", however higher resistive ratio and limited dispersion of the parameters could increase the yield of the devices.

Endurance performance and retention time: The endurance performance of the common memory should be larger than 10^5 testing cycles and the device should be robust for more than 5 years. [1]

Novel memory technology fulfilling with the requirements above could be a suitable candidate for the next generation of memory.

2.2. Resistive Switching

Recently, a new fundamental circuit element, memory resistive switching (RS) device, is emerging as a promising resistance random access memory (RRAM) device. In a RS device, the resistance value depends on the history or polarity of an applied voltage. It exhibits switching characteristics when the threshold voltage is reached. When the power is off, the device will keep the same resistance state, therefore it is categorized into the non-volatile memory. There are two different types of RS: unipolar and bipolar. The unipolar RS between low (LRS) and high resistance state (HRS) only depends on the magnitude but independent of the polarity of the applied voltage,[13,14] while the bipolar RS depends on not only the magnitude but also the polarity.

Various materials are used to achieve the resistance switching, including metal oxide, [6, 15] chalcogenide, [16, 17] and organic molecular system, [18, 19] etc. Compared with other memory devices, the oxide-based resistive switching devices are promising due to its simple structure and fabrication process, high storage density, fast writing and reading speed, and low power operation. There are plenty of oxide materials could be used for resistive switching device, such as NiO_x [15], TiO_x [20], AlO_x [21], CuO_x [22], HfO_x [23], ZnO [6] etc.

However, because the active layers of the structures listed above are only one layer, they are very difficult to control the parameters of the resistive switching. It is reported that using two-layer structure to optimize the performance. For example, a 5 nm

ZrO_x layer is added on the HfO_x layer to form a ZrO_x/HfO_x BL structure to improve the stability of switching performance, and the ratio of R_{HRS}/R_{LRS} is increased by ~100 times over the single HfO_x-based structure [24]. It is also reported that a BL switching structure, consisting of the AlO_x as a tunnel layer and TiO_x as a transport layer, reduces the dispersion of the switching parameters [25].

Generally speaking, there are two different kinds of RS effects: memory RS and threshold RS [26, 27], and the characteristic I-V curves are shown in Figs. 2.2 (a) and (b), respectively. The memory RS effect has an IV curve loop and two reversible transitions. As both LRS and HRS are stable when the power is off, they can be used in nonvolatile memory devices. However, as shown in Fig. 2.2 (b), the threshold RS effect has only one stable resistance state if no external bias applied, which could be categorized into volatile memory. There are several methods to make the conversion between the two switching. Chang *et al*. observed two types of reversible resistance switching (RS) effects by control thermal cycling in a NiO film: memory RS at low temperature and threshold RS at high temperature. [28] They used a dynamic percolation model to explain the transition phenomena and showed that the RS effects are controlled by the thermal stability of the conduction filaments, and the conversion from the two types of resistive switching result from the competition between Joule heating and thermal dissipation. Another method is using voltage pulse to change between bistable memory switching and monostable threshold switching in Pt/NiO/Pt structure.[29] Memory RS could be changed to threshold RS by applying a positive electrical pulse with height of 2 V and width between 10^{-2} and 10^{-4} s. The change is reversible by applying a negative electrical pulse with the same height and width. The polarity- and width-dependence of the switching transition

and compositional difference on electrical properties in NiO_x proved that the migration of oxygen ions is responsible for the switching transition in Pt/NiO/Pt structures.

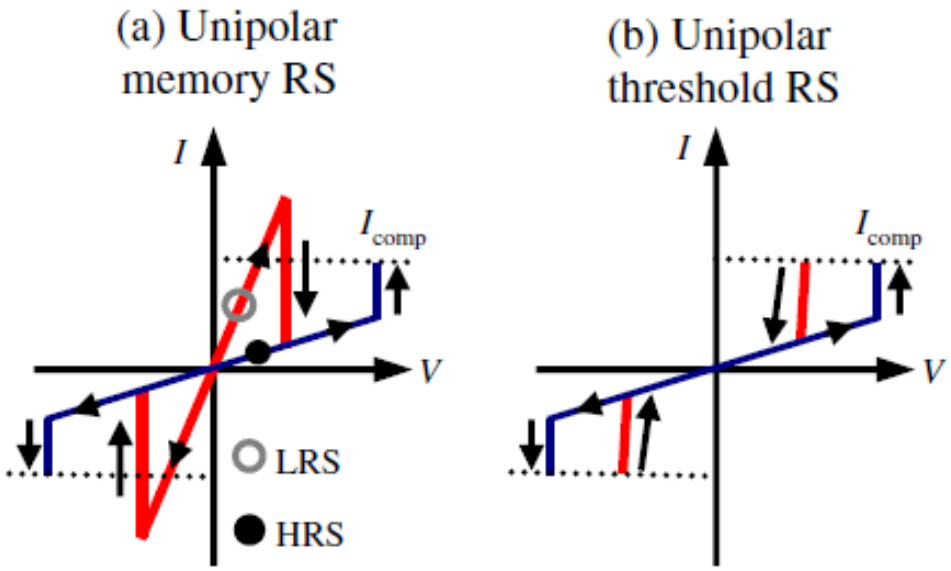


Figure 2.2 Schematic diagrams of current-voltage (I-V) curves for two resistance switching (RS) phenomena: (a) unipolar memory RS and (b) unipolar threshold RS. [28]

Figure 2.3 summarizes the main mechanisms of the memory resistive switching [1]. In the redox related resistive switching effect, there are two different types: chalcogenide and electrode dominated effect. Thermal Chemical Mechanism (TCM) [2] and Oxygen Ion Drifting Mechanism (ODM) [5] could explain the chalcogenide dominated effect, and the Electro-Chemical Metallization Mechanism (MCM) [6] need the interface redox between the electrode and active layer, therefore it could explain the electrode dominated effect, and mainly for the bipolar RS. However, both of the Thermo Chemical Mechanism and the Oxygen vacancies/ion involved drifting mechanism are

involved with the oxygen vacancies or ions. The main difference between these two mechanisms is that TCM used Joule heating to explain the rupture (unipolar RS) and ODM used drifting of the oxygen vacancies or ions under the reverse voltage to explain the rupture (bipolar RS). [5]

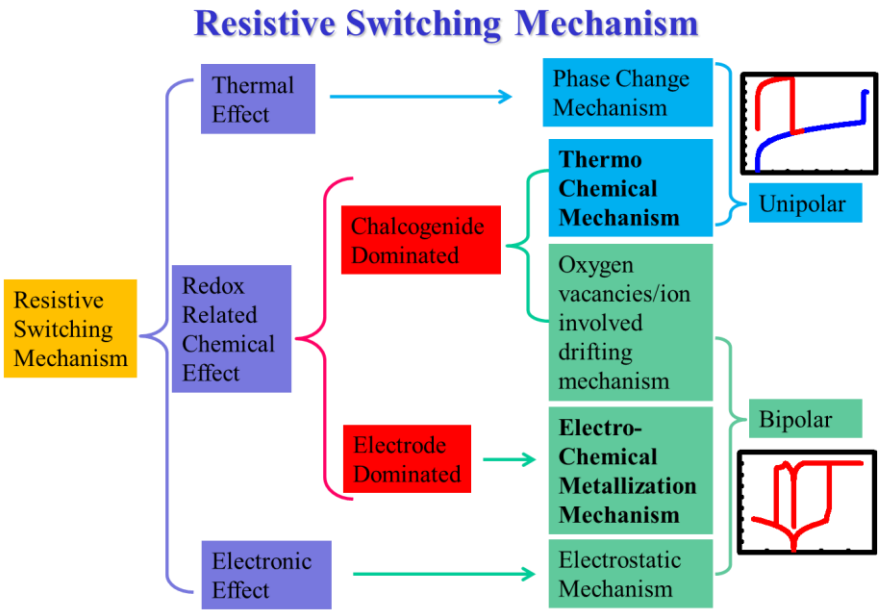


Figure 2.3 The category of the resistive switching mechanisms, according to [1].

The detailed study for the mechanism of resistive switching is complicated and still controversial. Some research group tried to study the compliance current (CC) effect to the resistive switching and get a preliminary knowledge for the mechanism.

During the set step of resistance switching, the limited current is confined on the memory to avoid excessive current and possible avalanche breakdown, which is also called compliance current (CC). Seo *et al* [30] first mentioned that the low resistance

values of the switching are dependent on the compliance current in polycrystalline NiO films by sputtering. Rohde [21] described that if the allowed maximum current was not limited to a certain low value, the sample completely broke down, maybe due to avalanche multiplication. By setting a proper current compliance value, stable switching from off- to on-state was repetitively observed. It was considered that the sudden increase in current at SET point was due to the formation of strong filaments that switch the film to the on-state. Therefore, it can be imagined that the maximum allowed current (current compliance) influences the formation of strong filaments. A higher current compliance for switching to the on-state, therefore, results in the formation of stronger and less resistive filaments, which in turn need more energy and power for their rupture. Tsunoda *et al* [31] also confirmed that the on-state resistance was controlled by the magnitude of the current compliance in Pt/TiO_2/Ag system. Kinoshita *et al* [32] pointed out that if compliance current in the Pt/NiO/Pt system is less than 1 mA, the response time for the current limiter in the semiconductor parameter analyzer may not catch up the rapid increase in the current during the set transition. Later Wan *et al*. proved the overshooting will exist under 1mA. [33]

Cao *et al*. [34] found out in the Pt/TiO_2/Pt structure there is a kind of threshold current. If the compliance current is more than the threshold current, there will be no reset switching, and the curve fitting shows that the reset current not only have the initial ohmic region, just as other switching-achieved curve; but also have the nonlinear region. From equation, they find that the conducting mechanism of the LRS changes from Ohmic to Poole-Frenkel emission when applying a large CC. Thus, the switching behaviors disappear after the conversion of the conducting mechanism. It is suggested that a proper

CC is essential to obtain a reversible resistive switching behavior. Kwon *et al* [35] use TEM image to indicate the bias voltage is largely reduced when the current level reaches the compliance limit, preventing further growth of other nanofilaments. Wang *et al*. showed that lower CCs produce conductive filaments (CFs) with simple connectivity and good controllability, resulting in a narrow distribution of switching voltages and a high ratio of high-to-low resistance states. In contrast, the stronger net-like CFs are formed at higher CCs, and their complete ruptures are difficult. Thus, the lower high-resistance states and a wide distribution of SVs appear in the reversible switching processes. [36] Lee *et al*. used random circuit breaker network model to simulate that if reduce the compliance current, the volume of the conducting filaments will decrease. [37] Nagashima *et al*. reported that varying the compliance current value resulted in the variation of LRS resistance, although the HRS resistance in each measurement was almost identical, even when the switching does not really happened. More importantly, there was a systematic relationship between the compliance current and the LRS resistance, indicating the "multistate memory effects".[38]

2.3. ZnO-based Resistive Switching Devices

Zinc oxide (ZnO) is a kind of wide band gap semiconductor material with a direct band gap of 3.34 eV at room temperature. [5] Compared with other wide band-gap semiconductors, ZnO has several advantages, such as a high free exciton binding energy of about 60 meV as compared to 25 meV for GaN, large UV photoresponse, superior radiation hardness, availability of large size single crystal substrates facilitating for homoeptaxial growth, and ease of wet chemical etching. ZnO nanostructures have

become one of the most promising and useful multifunctional nanostructures. It can be grown at low temperature on various substrates, giving ZnO a unique advantage over the other wide bandgap semiconductors, such as GaN and SiC nanowires. MOCVD growth can also provide atomically sharp interface control, and possible end-facet morphology control for various device applications. Catalyst-free growth of ZnO nanotips by MOCVD leads to superior optical properties.

Among oxide RS devices, ZnO-based RS devices possess advantages. First, through in-situ doping and alloying, ZnO-based devices could control the resistive switching properties. [5] Also, the ZnO device fabrication is a simple process, and it could grow without high temperature and use solution to do the wet etching for the patterning. The ZnO materials also have the character of radiation hardness.[39] Furthermore, the multifunctional properties of ZnO and its nanostructures make it feasible for integration. There are several publications on ZnO-based unipolar RS devices. Chang *et al* reported the Pt/ZnO/Pt devices, which exhibit the bistable resistance switching behaviors. [2] They attributed the low and high resistance states to the Ohmic behavior and Poole-Frenkel emission, respectively. The transparent RS device was made using ITO as an electrode and ZnO as an active layer.[40] Yang *et al* reported that the Mn-doping could enhance the ratio of R_{HRS}/R_{LRS} and the response time of the Ag/Mn-doped ZnO/Pt reached to 5 ns.[6] Peng *et al* fabricated the ZnO based RS device on different substrate and presented different switching performance.[41] A transparent switching device has also been demonstrated using GaZnO as the electrodes and ZnO as an active layer [42].

The Poole-Frenkel emission theory for oxygen vacancies related resistive switching is firstly mentioned in the reference [2] where it is believed that the conduction mechanism of HRS in high electric field is PF emission and the ZnO thin films contain non-negligible traps, i.e., oxygen vacancies most likely. This work used ZnO-based unipolar resistive switching device. However, Ag filament is also found in ZnO film by Yang *et al in* figure 2.4, and it is mentioned that the metal-involved filament forming and rupture may lead to the bipolar resistive switching.[6]

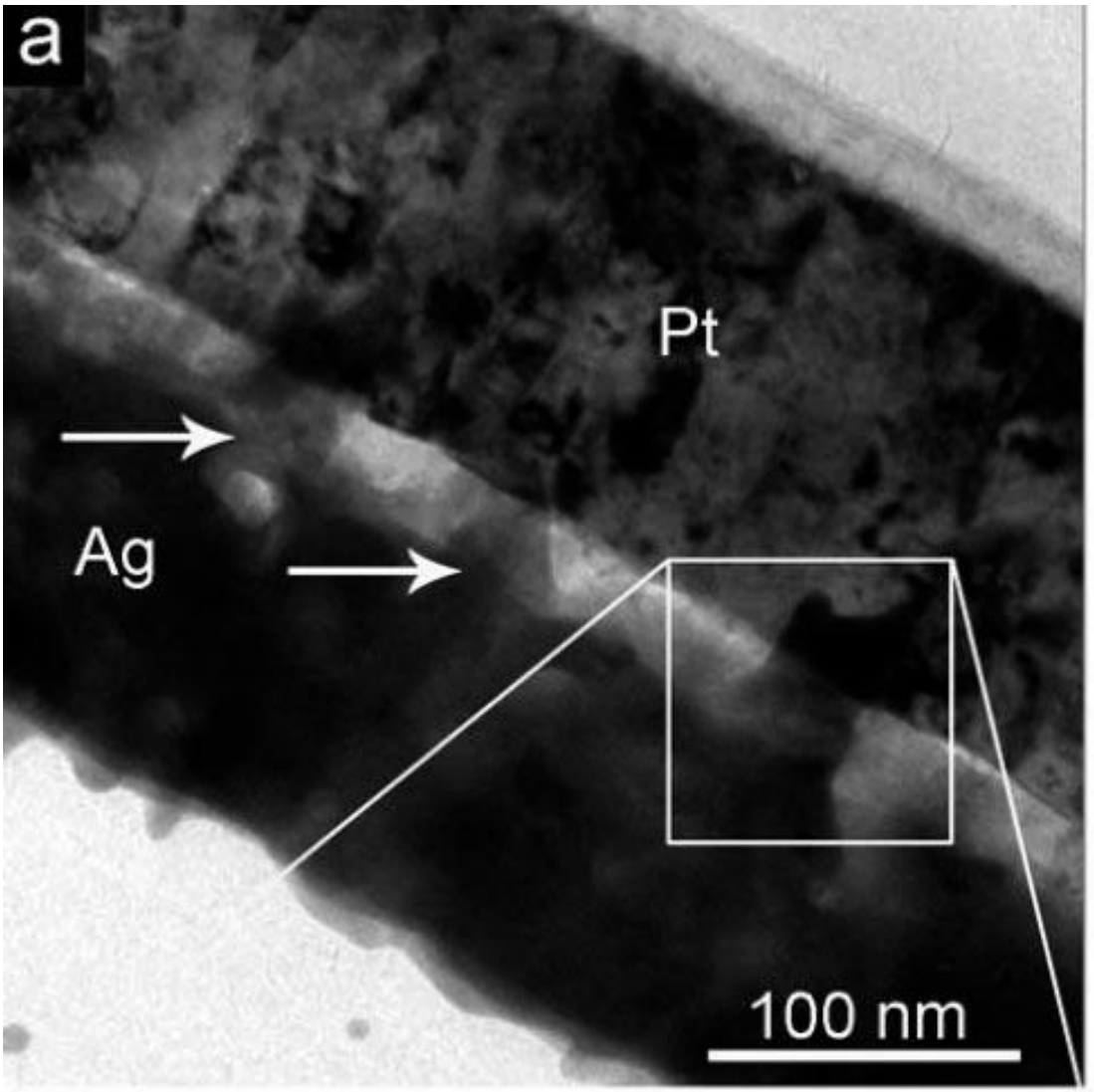


Figure 2.4 Conventional TEM observation for conductive filaments in the Ag/ZnO:Mn/Pt memory cell that has been switched to LRS.[6]

2.4. Integration of Resistive Switching Devices

Information technology is experiencing increased need for reconfigurable systems-on-demand that are capable of on-the-fly task and defect adaption, in real-time, and at a lower cost. High-performance electronic systems combining state-of-the-art processing logic, memories, and sensors on a single chip is desired. The challenge in implementing an advanced reconfigurable switching matrix network that can be integrated with various functional subsystems is substantial. Furthermore, the advanced crossbar architectures are becoming more critical in high density and high-performance systems. New embedded switching schemes should deliver high performance with large variations in device parameters when these devices approach nanometer scale. To date, even the design of such crossbar array are based on different material systems and complicated fabrication processes resulting in extremely low yield and are therefore, impossible for commercial application.

There are two different kinds of crossbar array using RRAM. One is called active array, which contained one transistor and one memory (1T1R) and the RRAM at the cross-point is actively controlled by the transistor. The other is passive array, with one diode and one memory (1D1R), and the cross-point is passively controlled by the outside circuit. Because the minimum area of the 1D1R vertical structure is $4F^2$ (F is the minimum feature size), the 1D1R integration crossbar array has good potential for scaling down.

The crossbar array structure is widely used for high-density storage and reconfigurable electronics. When the memory resistor (R) serves as the unit cell in the 1R-only crossbar array architecture, the malfunction would occur. In such a crossbar array, during reading process, the parasitic current can easily flow through the nearby R cells in LRS, thus causes the fake reading signals. For example, in a 2×2 crossbar structure shown in Fig. 2.5 (a), bit 1 is in HRS, while bit 2, 3 and 4 are all in LRS. To read bit 1, a voltage pulse is applied to world line 1 while bit line 1 is ground. In the ideal operation, no parasitic current can pass from world line 1 to reach bit line 1 and the readout signal of bit 1 is in HRS. However, a parasitic current path consisting of nearby bits in LRS exists, and current can pass through bit 2, 3 and 4 in LRS to reach bit line 1. A fake readout signal of LRS for bit 1 is therefore obtained.

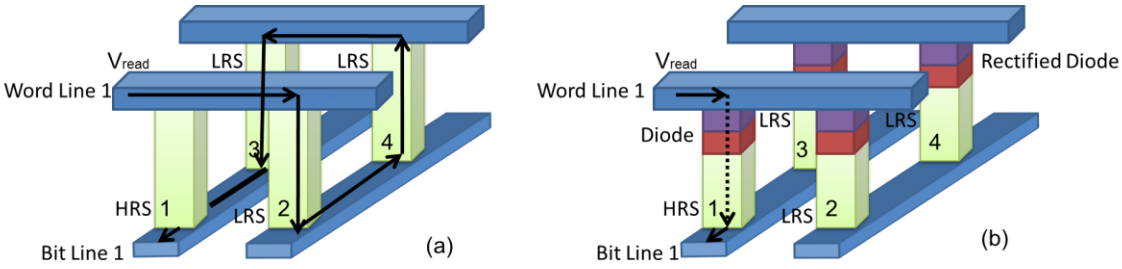


Figure 2.5 (a) Reading malfunction in an array consisting of 2×2 resistive switching cells without diodes. (b) Rectified reading operation in an array consisting of 2×2 cells with diodes.

To eliminate the parasitic path, a diode has to be added to form the 1D1R unit cell in this 2×2 crossbar structure, as shown in Fig. 2.5(b). When positive reading voltage is applied on the bit 1, the diode in bit 4 will be equivalently under the reverse bias, this

integrated diode will block the current flowing through the nearby bits in LRS to reach bit line 1 (except the extremely small leakage current flowing through the reversely-biased diode). Thus, the reading signals will be acquired correctly. Therefore, in a crossbar matrix, it is needed to integrate a diode (1D) with a memory resistor (1R) to form the 1D1R unit cell to achieve the resistive switching without the crosstalk.

Up to now, several different kinds of 1D1R switching structures have been reported. There are four different types of diode could be used in the 1D1R crossbar array. First is Si-based diode based 1D1R integration. Golubovic *et al* first fabricated vertical polycrystalline silicon p-n diodes fabricated up to the metal-1 level using basic processing steps of a CMOS front-end-of-line for 65nm node and beyond.[43] In 2010 Cho *et al* fabricated 1D1R based on the nonvolatile organic memory device.[44] They used back Al/p-Si/Al as diode and Al/PI:PCBM/Au as memory element. In the 1D1R structure the ratio of forward current over the reverse current is 10^3, and the R_{HRS}/R_{LRS} in the forward bias is 10^2. However there are two major problems in this 1D1R structure. First this structure is based on the Silicon diode, which is lack of the compatibility of RRAM fabrication and further CMOS integration. Secondly the organic memory showed the bipolar switching characteristics, which is not suitable for passive crossbar array structure.

Second is the p-n diode based 1D1R integration. Kang *et al* presented the $CuO_x/InZnO_x$ thin-film diodes for cross-point memory applications.[45] The vertical structure is Pt/p-CuO/n-IZO/Pt, as shown in Fig. 2.6. The forward and reverse current of the cross-point diode is 10^3. Lee *et al* used NiO as a memory and p-CuO/n-IZO as a diode to form the 1D1R structure with 0.5 um×0.5 um cells, where the ratio of HRS over LRS

was about 80 after 1,000 cycles.[46] In the paper they introduced 2-stack 1D1R cross-point structure to enlarge the memory cell density. They just shared the same bit line and used two different word lines to connect the memory and switching element. They also announced that their Pt/Ti-doped NiO/Pt storage node has the HRS/LRS ratio as large as 10^3. Cell and device properties of the cross-point structure 8×8 array are reported. Lee *et al* also mentioned to use Pt/NiO/Pt as oxide resistive memory cell and Pt/p-NiO_x/n-TiO_x/Pt as oxide diode. All films were deposited by using DC magnetron sputtering. For the integration the total ratio of HRS/LRS is 10^3, and the forward current over reverse current is 10^5. However from the Fig. 2.7 we could find out that because of the large threshold voltage (1V) of the p-n diode, if the voltage is less than the 1V, the forward on current is still low, the reading voltage of the 1D1R structure should be much larger than 1V, so that the reading voltage will easily reach to the reset voltage range resulting in fake reset signal. Also the high reading voltage will lead to unnecessary power consumption, which will become worse in the crossbar array.

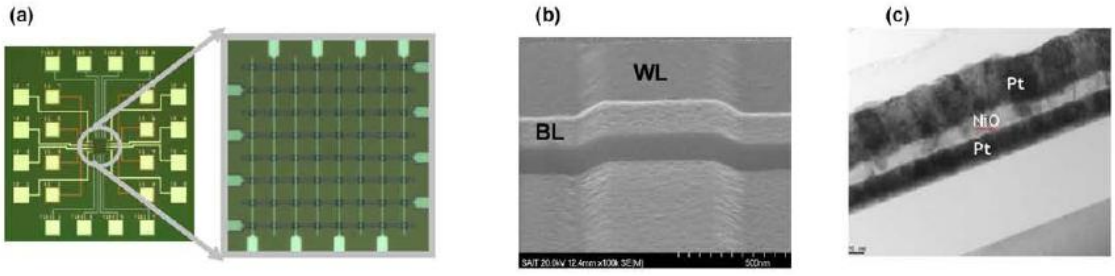


Figure 2.6 (a) Optical microscopic image including pads for our test array structures and image of the 8x8 cell array. (b) SEM image of Pt word and bit line. (c) TEM image of NiO storage element.[46]

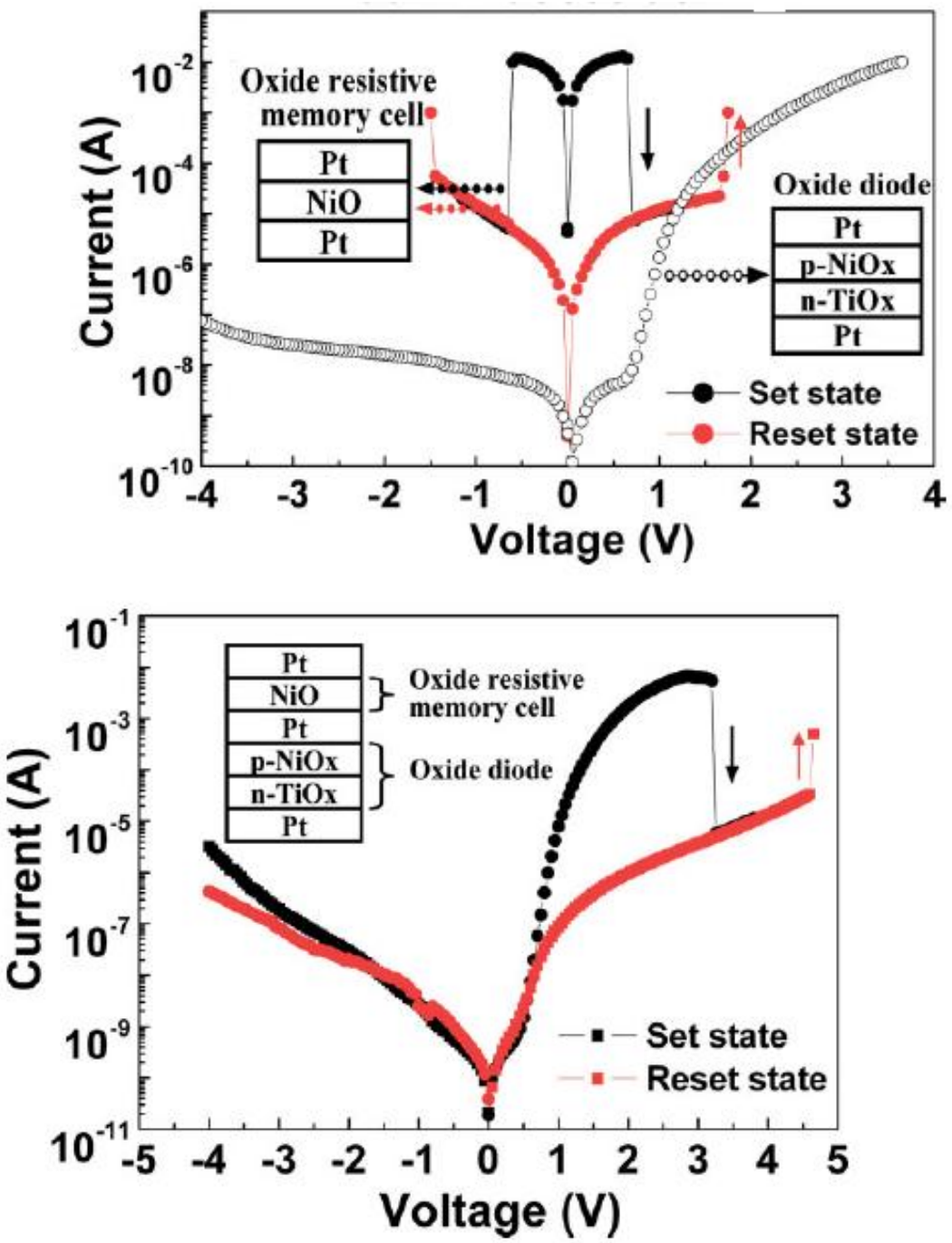


Figure 2.7 The IV characteristics of the single memory cell, diode cell and the integration 1D1R structure.[46]

Third is the Schottky diode based 1D1R integration. Allen *et al*. announced the highly rectifying Schottky contacts on the n-type hydrothermal ZnO using silver oxide.[47] A 40~80 nm thick silver oxide film was deposited by the reactive RF sputtering of a Ag target (99.99% purity) using an Ar/O_2 plasma, a RF power of 50 W, and a processing pressure of 4×10^{-3} mbar (about 3×10^{-3} torr). A Pt capping layer was then deposited onto the silver oxide film by e-beam evaporation. However their structure is lateral structure and the distance between Schottky diode and Ohmic diode is 25 μm. Shima *et al* used Pt/TiOx/Pt for a resistive memory and a Schottky diode.[48] The tri-layer with electrically asymmetrical interface is synthesized by means of the reactive sputtering technique followed by the oxygen annealing. The initial current-voltage characteristics in the $Pt/TiO_x/Pt$ tri-layer cell have rectifying behavior originated from the Schottky junction formed between TiO_x and Pt top electrode layer. In their device, the ratio of HRS over LRS was about 100 and it present 25 switching cycles and no decay is observed. Shin *et al* presented a Schottky-type diode switch consisting of a Pt/(In, $Sn)_2O_3/TiO_2/Pt$ stack for applications to the cross-bar type resistive –switching memory arrays.[49] Fig. 2.8 also showed the difference between p-n diode type and Schottky diode type of 1D1R resistance ratio. Just because of the confinement of the p-n diode in the low voltage, the resistance ratio cannot be larger than 10 below 1V. However the resistance ratio of the Schottky-type 1D1R structure could be as large as 10^2. Tallarida *et al* also announced 1D1R structure of Ag/ZnO/Ti as Schottky diode and Au/TiO2/Au as unipolar memory cell. Their ratio of HRS over LRS is 10^2 and forward current over reverse current is 10^5.[50] Recently, a ZnO-based 1D1R structure has been reported,

where the memory region and the diode region are separated and these two kinds of elements are interconnected horizontally using a common bottom electrode.[51]

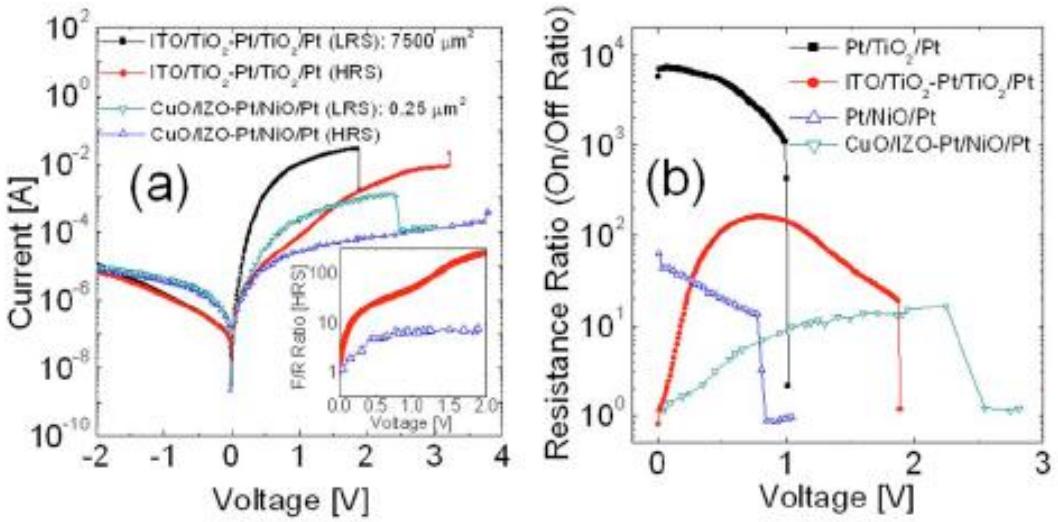


Figure 2.8 The IV characteristics of ITO/TiO_2-Pt/TiO2/Pt and CuO/IZO-Pt/NiO/Pt 1D1R structure.[49]

Recently some self-verifying diode is been used for 1D1R crossbar array. Kim *et al* presented the Ag/amorphous-Silicon/poly-Silicon can exhibit diode-like I-V characteristics at on-state with reverse bias current suppressed to below 10^{-13} A and rectifying ratio is larger than 10^6, just as the Fig. 2.9 shown.[52] However there might be some errors. In the ten consecutive switching IV curve it is shown that the device could be switched on at about 1.5V and with -1.5V it could be switched off. However in the response time testing the device need -3.5V to be turned off and -2V is not enough. So the two figures seem to be conflict with each other. Zuo *et al* also mentioned that n^+-Si/ZrO_2/Pt based memory cell also have the self-rectifying effect. The rectification ratio

is 10^4 and on/off ratio are 10^6. However its program voltage should be as high as -12V, but need positive reading voltage [53]. In the crossbar array it is inconvenient to use positive voltage to read and use negative to set/reset, so it is common to use unipolar instead of bipolar for the 1D1R crossbar array.

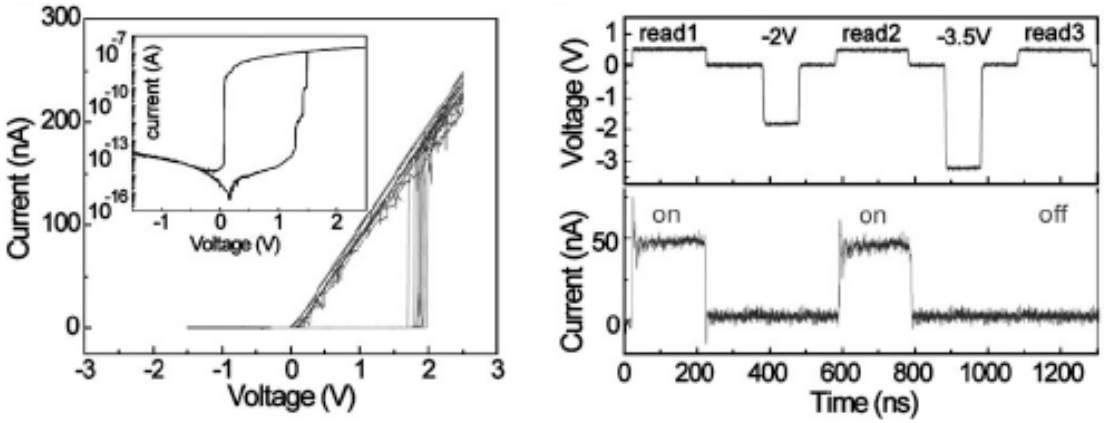


Figure 2.9 The IV characteristics curve of the self-rectifying structure and the response time of the device. [52]

In summary, Schottky diode based 1D1R crossbar array has the advantage of good fabrication compatibility of diode and memory, low reading voltage and avoidance of two polarities for operation voltage, and have encouraging potential for further 1D1R cross-point array integration.

However, 1D1R structure is still a passive array and need the outside control module. To avoid outside circuits, 1-transistor 1-RS device (1T1R) RRAM cell structure is fabricated. The 1T1R structure is similar to a DRAM cell, and the capacitor is replaced by the RS device for non-volatile memory use. The data is stored as the resistance state of the RS device and the transistor is served as the access switch for reading and writing

data. The 1T1R cell used as a basic building block for a memory array could avoid the sneak current and ensure reliable operation as the R should be used as bipolar resistive switching device. Hsu *et al.* first proposed the 1T1R resistive switching memory array structure on a semiconductor substrate comprises forming an array of transistors comprising a polycide/oxide/nitride gate stack with nitride sidewalls, and the transistors comprising a source and a drain region adjacent to the gate stack.[54] Kurotsuchi *et al* [55] first fabricated the 1T1R structure with a Phase Change Memory (PCM, using O-GST film) as the memory and the programming current is less than 100 μA. Later the HfO_x based RRAM is connected with an external, commercial-used MOSFET and form the 1T1R structure and limit the operative current to be 20 μA.[56] It is also calculated using a performance and energy model that the write access time is inversely proportional to minimum value of resistance and directly proportional to the square of oxide layer thickness. The read access time of the cell is only a function of the maximum value of resistance and does not change by the layer thickness. Read operation is one order of magnitude faster than write operation in the 1T1R cell. From energy perspective, the write operation is roughly three times more energy consuming than the read operation. The write energy increases quadratically for larger layer thicknesses while read energy dissipation depends only on the bit line capacitor and is not a function of the physical parameters of the device.[57] Another 1T1R structure is used to modulated the $Ti/ZrO_2/Pt$ resistive switching device to multilevel resistive switching state.[58] The dimension of HfOx-based RRAM has also been scaled down to 37 nm to meet the nanopillar transistor performance in the 1T1R structure, which also prove the prospect for

RRAM in the high-density applications. [59] To sum up, currently reducing power consumption and scaling down are two main tasks for 1T1R further memory applications.

2.5. Summary and Challenges of ZnO Resistive Switching Research

In summary, we have shown that resistive switching device based on the resistive random access memory is a promising candidate for the further memory development. So far the resistive switching device could be fabricated as the unipolar switching device, bipolar switching devices, and threshold switching devices. Because of the unique advantages, ZnO and its nanostructures is a highly suitable material for resistive switching design. The discussion paves the way for developing the explanation of resistive switching mechanism. Single resistive switching device could be integrated for 1D1R and other applications.

Challenges for future memory design are also indicated from the review analysis. First, the resistive ratio for the resistive switching devices that reported so far is relatively low. The low resistive ratio will reduce the operation error tolerance and increase the risk of wrong readout signal in the memory architecture. The stability of the current resistive switching devices also needs to be optimized. Second, the mechanism of resistive switching is still not clear. The confused relationship between different switching modes blocks the way for the development of the resistive switching device. Third, the integration of the resistive switching is still facing the fabrication difficulties. Large cell size in the 1D1R blocks the development for the resistive switching in the matrix and other applications. In the next three chapters of this thesis, the solutions to the three challenges above are discussed.

Chapter 3

ZnO-based Bipolar and Unipolar Resistive Switching Devices

In the previous chapter, it is presented that transition-metal-doped ZnO is emerging as a promising material for the resistive switching device. ZnO based resistive switching devices possess advantages due to the well-controlled switching properties through *in-situ* doping and alloying, multifunctional achievement, high quality nanostructures, and low cost due to its abundant material source and relatively simple process. The unipolar resistance switching only depends on the magnitude but is independent of the polarity of the applied voltage, leading to easy operation with a unipolar voltage source. In addition, unipolar device could be used for passive matrix to save the cell area ($4F^2$), and increase the density of the memory architecture. However, some digital electronics could only provide one supply voltages and one reference voltage (ground). In order to SET (forward bias) and RESET (reverse bias) the device, the resistive switching device should possess bipolar characteristics. In this chapter the different fabrication conditions has been introduced for both bipolar and unipolar resistive switching devices. Curve fitting method is presented for the conduction discussion. Parameter stability comparisons with different structures are also discussed. The thickness affects the polarity of the resistive switching, which could be used for different applications.

3.1. Device and Demonstration of Fe-doped ZnO Resistive Switching Devices

3.1.1 FeZnO Single Layer Structure

To make the RS device, metal-oxide-metal (MOM) structure is fabricated. Si wafers were used as substrates. A SiO_2 layer (300 nm thick) was formed on the Si substrate by thermal oxidization. A Pt/Ti (100 nm/5 nm) layer was deposited on SiO_2 by e-beam evaporation, in which Ti was used as an adhesion layer and Pt as the bottom electrode. In the SL structure, the $Fe_xZn_{1-x}O$ (x~4%) layer (~70 nm) was directly grown on the Pt surface by metal-organic chemical vapor deposition (MOCVD) technique. Diethylzinc (DEZn) was chosen as Zn precursor, and ultra-high purity (UHP, >99.999%) Ar and O_2 gases were used as the carrier and oxidizer, respectively. Substrate temperature of 450-500^oC and chamber pressure of ~50 torr was kept during the growth. The device patterns with a diameter of 80 μm were formed by photolithography and wet chemical etching using hydrochloric acid. Ag metal layer (~100 nm) was deposited by e-beam evaporation on the top of $Fe_{0.04}Zn_{0.96}O$ film to serve as the top electrode. X-ray diffraction (XRD) (θ-2θ scan) measurements were carried out on the SL and BL structures using a Siemens D500 X-ray diffractometer. Hitachi (S-800) field-emission scanning electron microscopy (FESEM) was used to inspect the surface morphology and layer structures. *I–V* measurements were conducted using Agilent 4156C Semiconductor Parameters Analyzer.

3.1.2 FeZnO/MgO Bilayer Structure

In the BL structure, a thin MgO layer (~5 nm) was grown on the Pt surface, then a $Fe_xZn_{1-x}O$ (x~4%) layer was subsequentially grown on top of the MgO layer, both by MOCVD. For the MgO growth, bis(methylcyclopentadienyl) magnesium (MCp_2Mg) and

UHP O_2 were used as the Mg precursor and oxidizer, respectively. MgO was grown at a substrate temperature of 300-350 ^{o}C and the as-grown MgO layer appears to be amorphous. The $Fe_{0.04}Zn_{0.96}O$ layer in the BL structure was grown under the same growth conditions as that in the SL structure.

Fig. 3.1(a) shows the schematics of the SL and BL bipolar RS structures and Fig. 3.1(b) is the SEM image of the Ag/FeZnO/MgO/Pt (BL) structure. Three obvious layers, consisting of bottom electrode, oxides and top electrode, are observed. Pt/Ti bottom electrode and Au/Ag top electrode appear to be single layers. The MgO layer is too thin to be observed in the SEM picture.

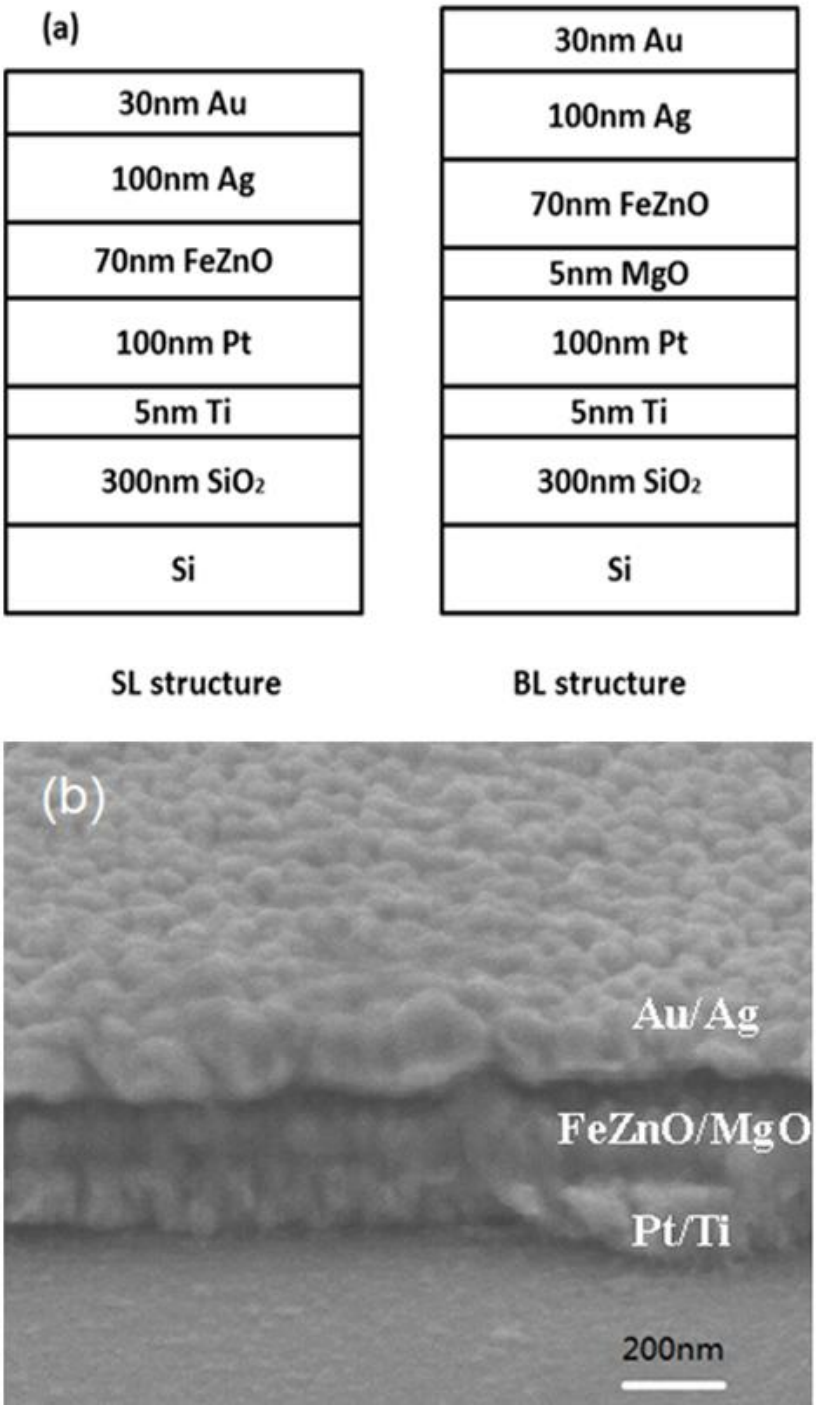


Figure 3.1 (a) The schematic diagrams of the bipolar resistive switching structures: the left diagram shows an Ag/FeZnO/Pt (SL) structure, and the right diagram shows an Ag/FeZnO/MgO/Pt (BL) structure; (b) an SEM image of the BL structure.

Figure 3.2 shows the XRD results of FeZnO SL and FeZnO/MgO BL structures grown on Pt/Ti/SiO_2/Si substrates. The intensity is plotted on a log scale. All peaks in both samples can be indexed into three different phases, which are ZnO, Pt, and Si. As an adhesion layer, Ti is very thin and thus goes undetected in these XRD patterns. The as-grown MgO layer is amorphous. However, it could be re-crystallized during the subsequent $Fe_xZn_{1-x}O$ growth at high temperature (~ 450^oC). Small thickness (~5 nm) makes it still undetectable in XRD. The XRD patterns of $Fe_xZn_{1-x}O$ (x~4%) are indexed by using diffraction data of ZnO (JCPDS ICDD PDF No. 89-0510). The FeZnO layers in both SL and BL structures show the wurtzite structure without a phase separation and they are highly textured along c-axis. However, additional peaks of (10-10) and (10-11) appear in the FeZnO layer of the BL structure (Fig. 3.2(b)) but not from the SL structure (Fig. 3.2(a)). This implies that the texturing of FeZnO layer grown on Pt is different from that grown on MgO surface. When a $Fe_xZn_{1-x}O$ (x~4%) layer is directly deposited on the Pt surface, due to a lack of epitaxial relationship, the adatoms (having high surface diffusion rate at substrate temperature) tend to arrange themselves toward the direction that has the lowest surface energy so that the FeZnO layer would grow predominantly along the c-axis direction, while growth of crystallites with other orientations is inhibited (Fig. 3.2(a)). However, when the FeZnO is grown on the MgO layer, MgO could be re-crystallized and its crystalline grains provide crystallographic alignment to the FeZnO film, thus inducing growth along the other orientations besides c-axis (Fig. 3.2(b)). The growth mode will finally switch to the c-axis direction due to large surface energy anisotropy of ZnO. These phenomena are also observed on wurtzite ZnO (0001) epitaxial films grown on MgO substrates [60].

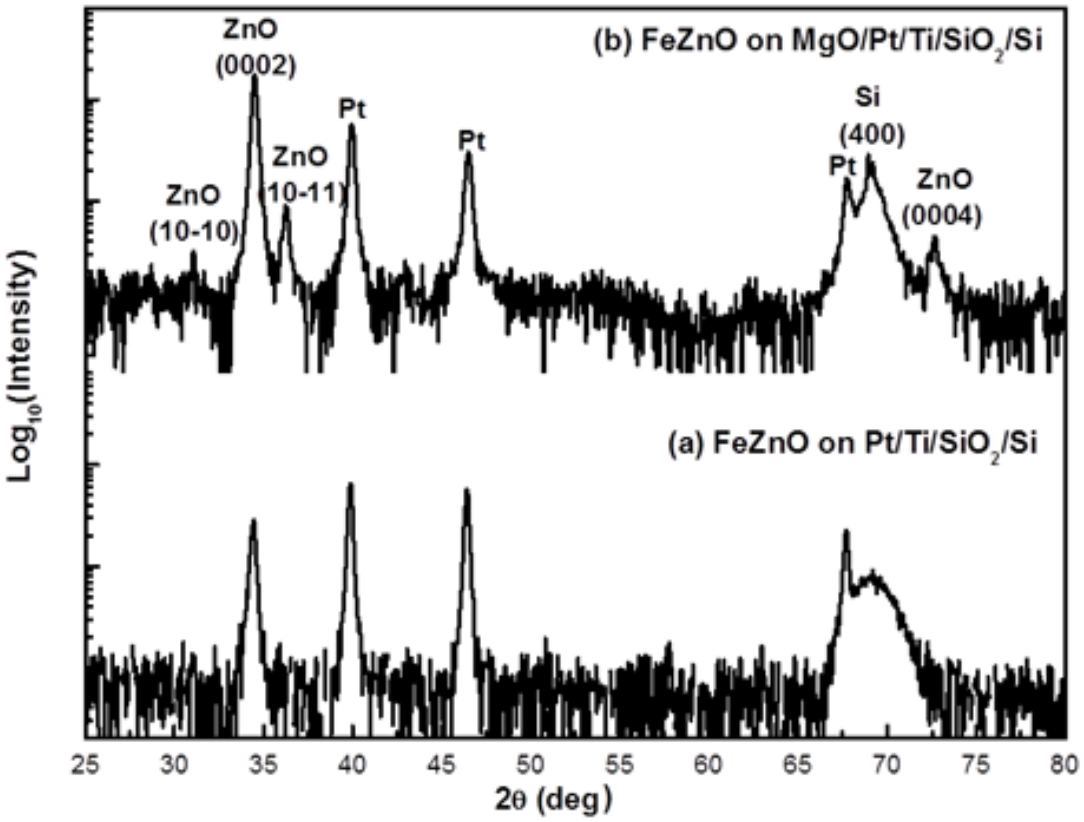


Figure 3.2 XRD spectra of the FeZnO deposited (a) on the Pt/Ti/SiO_2/Si, and (b) on the MgO/Pt/Ti/SiO_2/Si.

3.2. Polarity of FeZnO Resistive Switching Device

3.2.1 Bipolar Resistive Switching

Fig. 3.3 exhibits the bipolar resistive switching characteristics of the Ag/FeZnO/Pt (SL) structure and the Ag/FeZnO/MgO/Pt (BL) structure. During the measurements, the bottom electrode is grounded and the varied voltage is applied on the top electrode. When voltage is less than the threshold switching voltage, the current is relatively small and the device is in the HRS. When the voltage reaches V_{SET}, the current increases dramatically

and the device switches to LRS. The switching device remains in LRS, until the voltage reduces to V_{RESET}, then the current decreases sharply and the device switches from LRS back to HRS. The reversible I-V curve loop indicates the memory behavior. Under the reading voltage that is usually chosen between V_{SET} and V_{RESET}, HRS and corresponding small current could be recognized as the logic "0" (OFF) while the large current in LRS represents the logic "1" (ON) in the memory circuit. Under a reading voltage of 0.2 V, the currents flow through the HRS and LRS of the SL structure are 1.8×10^{-5} A and 6.8×10^{-3} A, corresponding to the R_{HRS} and R_{LRS} of 1.1×10^{4} Ω and 29 Ω, respectively. The ratio of R_{HRS}/R_{LRS} is 3.8×10^{2}. The V_{SET} is 0.70 V and the V_{RESET} is -0.77 V, which corresponds to an electrical field of around 10 kV/cm. The electrical field is smaller than other reports for ZnO resistive switching devices in literatures, which could benefit the retention performance. Both threshold voltages are far away from the reading voltage, which can prevent the reading voltage from triggering the switching process and leading to severe problems in controlling and reading the memory switching states.

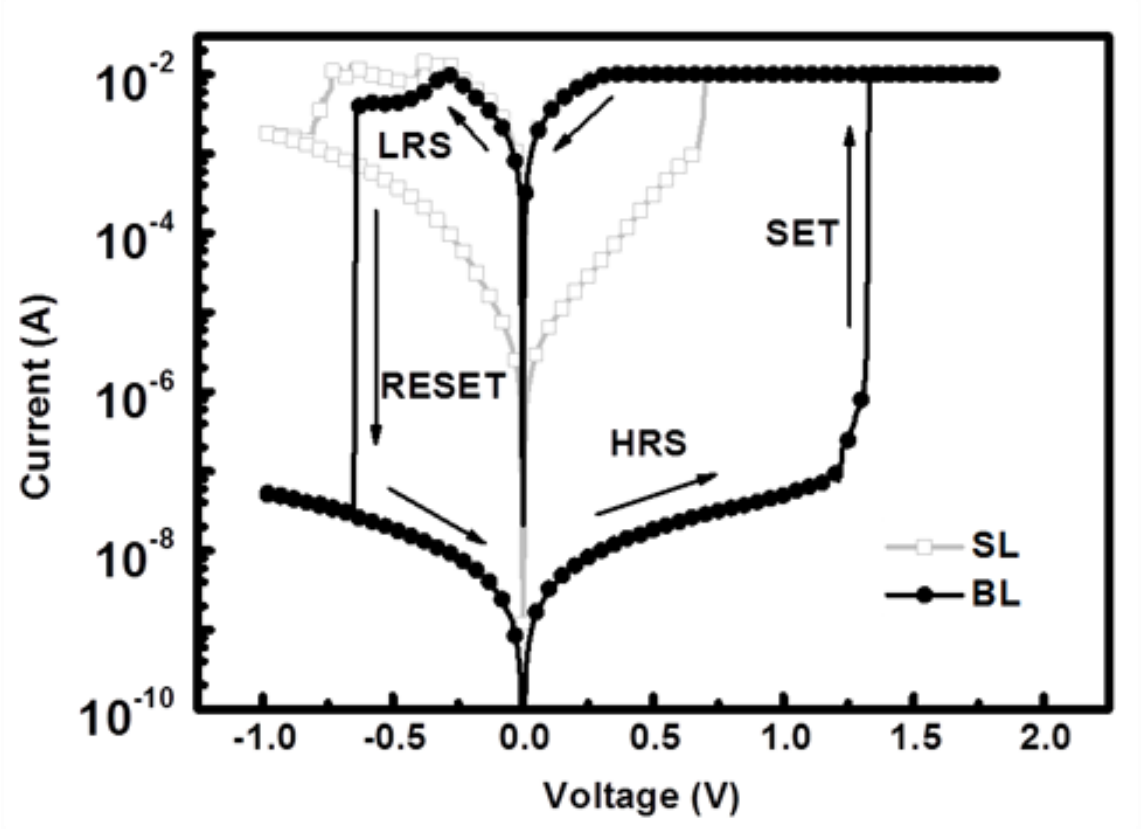


Figure 3.3 The I-V characteristics of the Ag/FeZnO/Pt (SL) structure and the Ag/FeZnO/MgO/Pt (BL) structure.

The I–V characteristics of the SL structure at HRS and LRS are also analyzed through curve fitting. The HRS curve from Fig. 3.4(a) is fitted well to the following equation:

$$\ln\left(\frac{I}{V}\right) = a_1 \times V^{\frac{1}{2}} + b \qquad (1)$$

It accounts for the Poole-Frenkel emission (PFE) model,[61] which is

$$\ln\left(\frac{J}{E}\right) \propto q^{\frac{3}{2}} \left(\pi\varepsilon_r\varepsilon_0\right)^{-\frac{1}{2}} \left(rkT\right)^{-1} E^{\frac{1}{2}} \qquad (2)$$

where J is the current density, E is the electric field, q is the electric charge, ε_r is the relative permittivity of the material, ε_0 is the permittivity of free space, k is the boltzmann's constant, and T is the temperature. In the fitting of the equation (1) the value of a_1 and b are found to be 9.3 and -14, respectively. The well-fitted result implies that the dominant conduction mechanism in HRS is the emission of trapped electrons in the FeZnO layer. It is speculated that the resistive switching is attributed to the formation and rupture of conductive filaments that are related to the oxygen ions or metal ions. In fact, we observed that after annealing the samples under oxygen ambient, the devices were no longer able to make the complete resistive switching. At the LRS of Fig. 3.4(b), the IV curve is fitted well to the linear straight line $I = a_2V$, where the fitting parameter value of a_2 is 3.4×10^{-2}. Thus, the conduction mechanism in LRS follows the Ohmic behavior.

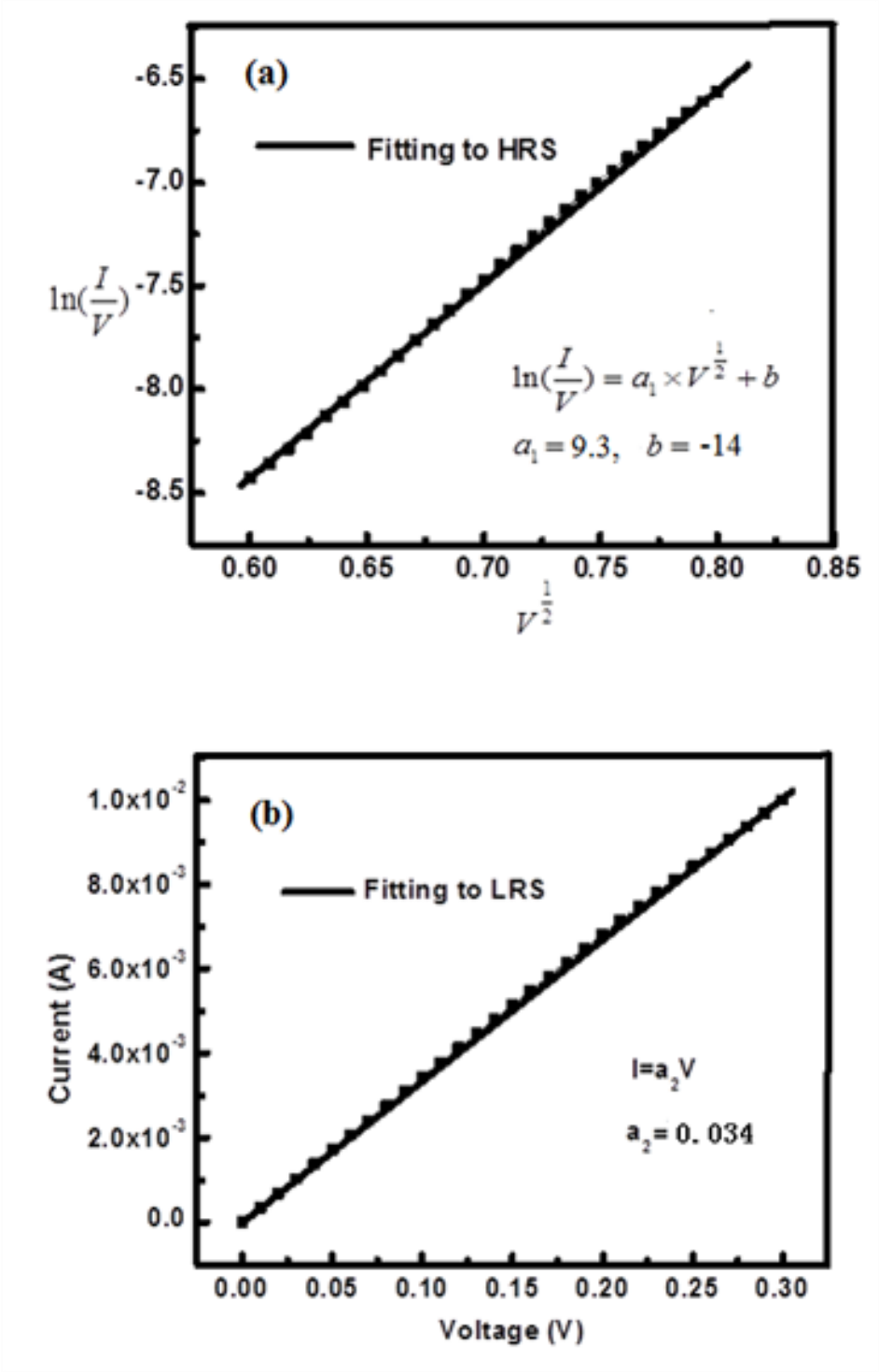


Figure 3.4 The curve fitting for measured I-V characteristics of the SL structure at (a) HRS and (b) LRS. The measured data are represented by square dots, and the fitting results are represented by straight lines.

Figure 3.3 also shows the *I–V* characteristics of the BL structure. Through comparison between these two structures, it can be seen that both structures have similar R_{LRS}; however, they have significantly different R_{HRS}/R_{LRS} ratios. In the BL structure, the currents in HRS and LRS are 6.5×10^{-9} A and 6.4×10^{-3} A at 0.2 V, corresponding to the resistance values of 3.1×10^{7} Ω and 31 Ω, in HRS and LRS, respectively. The R_{HRS} of the BL increases by 10^{3} over that of the SL structure. The ratio of R_{HRS}/R_{LRS} for the BL structure is 9.9×10^{5}, which is also more than three orders larger than that of the SL structure (3.8×10^{2}). The significantly enhanced R_{HRS}/R_{LRS} of the BL structure leads to a large difference in reading ON/OFF signal, which can minimize the confusion in reading signal of "0" and "1" when it is used for the nonvolatile memory applications.

Up to now, the measured retention times of both SL and BL structures are over 10^{7} s (Fig. 3.5), indicating robust performance of the resistive switching devices. The high thermal stability from Fe doping in ZnO could result in better endurance performance. In comparison of the current values in the HRS of the SL and BL structures, the peak-to-valley ratios for the SL and BL curves are $2.1\text{x}10^{2}$ and 17, respectively. A narrower switching current distribution and a higher R_{HRS}/R_{LRS} ratio ($>10^{5}$) are obtained simultaneously in the BL structure, which would lead to better and repeatable device performances. Since currents in the HRS and LRS are recognized as the OFF and ON signal in the reading step, the minimized dispersion of the currents is particularly desired for the reading process of the memory devices.

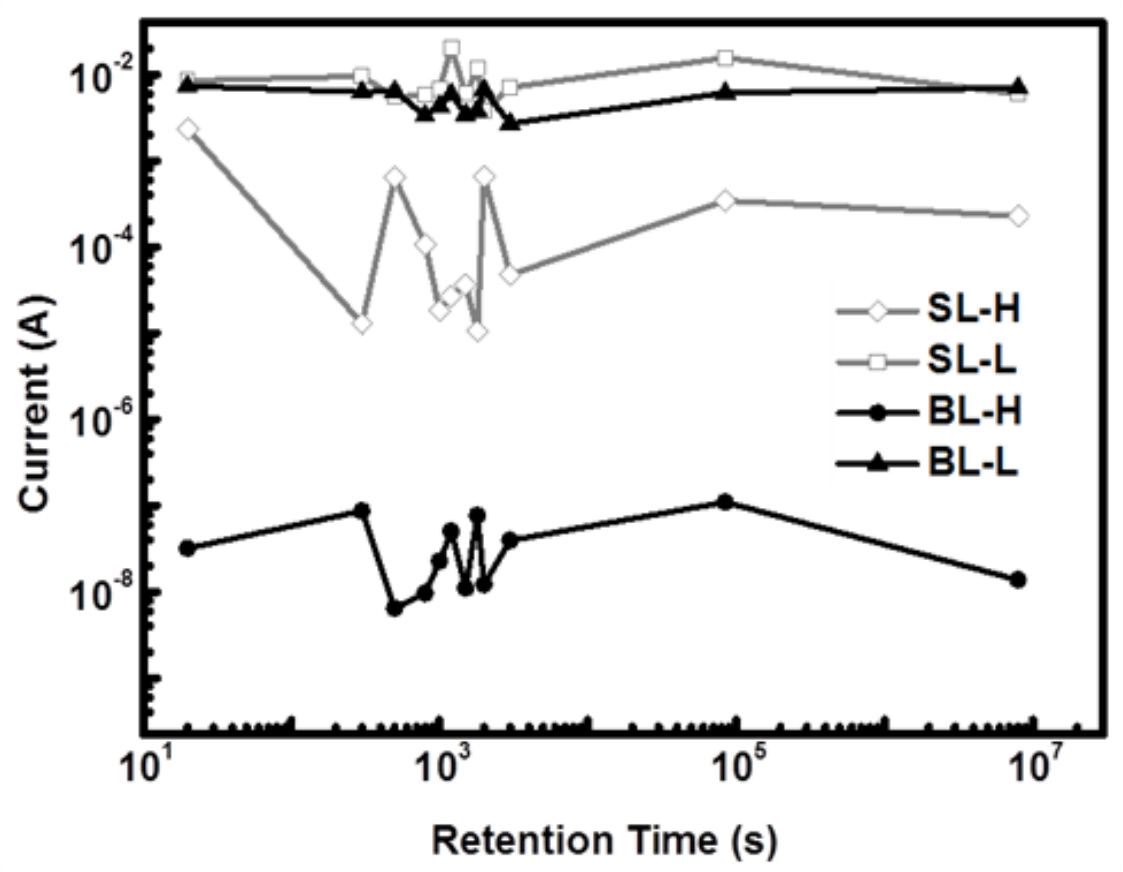


Figure 3.5 The retention time of the SL and BL structures.

Shown in Figure 3.6 are the switching voltage distributions of 20 cycles for the device with the SL and BL structure, respectively. In the SL structure, the reset voltages V_{RESET} are in the range of -0.91 V to -0.59 V, with the average voltage of -0.75 V, and a standard deviation of 0.097 V. In the BL structure, the V_{RESET} values are in the range of -0.97 V to -0.58 V, with the average voltage of -0.71 V and a standard deviation of 0.085 V. On the other hand, in the SL structure the set voltages V_{SET} are in the range of 0.46 V to 1.12 V, with the average voltage of 0.77 V, and a standard deviation of 0.21 V. In the BL structure the set voltages are in the range of 1.21 V to 1.45 V, with the average voltage of 1.31 V and a standard deviation of 0.075 V. Both SL and BL structures have

similar value range and distribution of V_{RESET}. But the V_{SET} of the BL is larger than that of the SL structure. By comparing the standard deviation values, it is shown that the V_{SET} dispersion of the BL structure is significantly reduced in comparison with that of the SL structure. Since the V_{SET} value is directly related to the writing process of the memory, thus the narrow distribution of the V_{SET} would improve the stability of the memory devices.

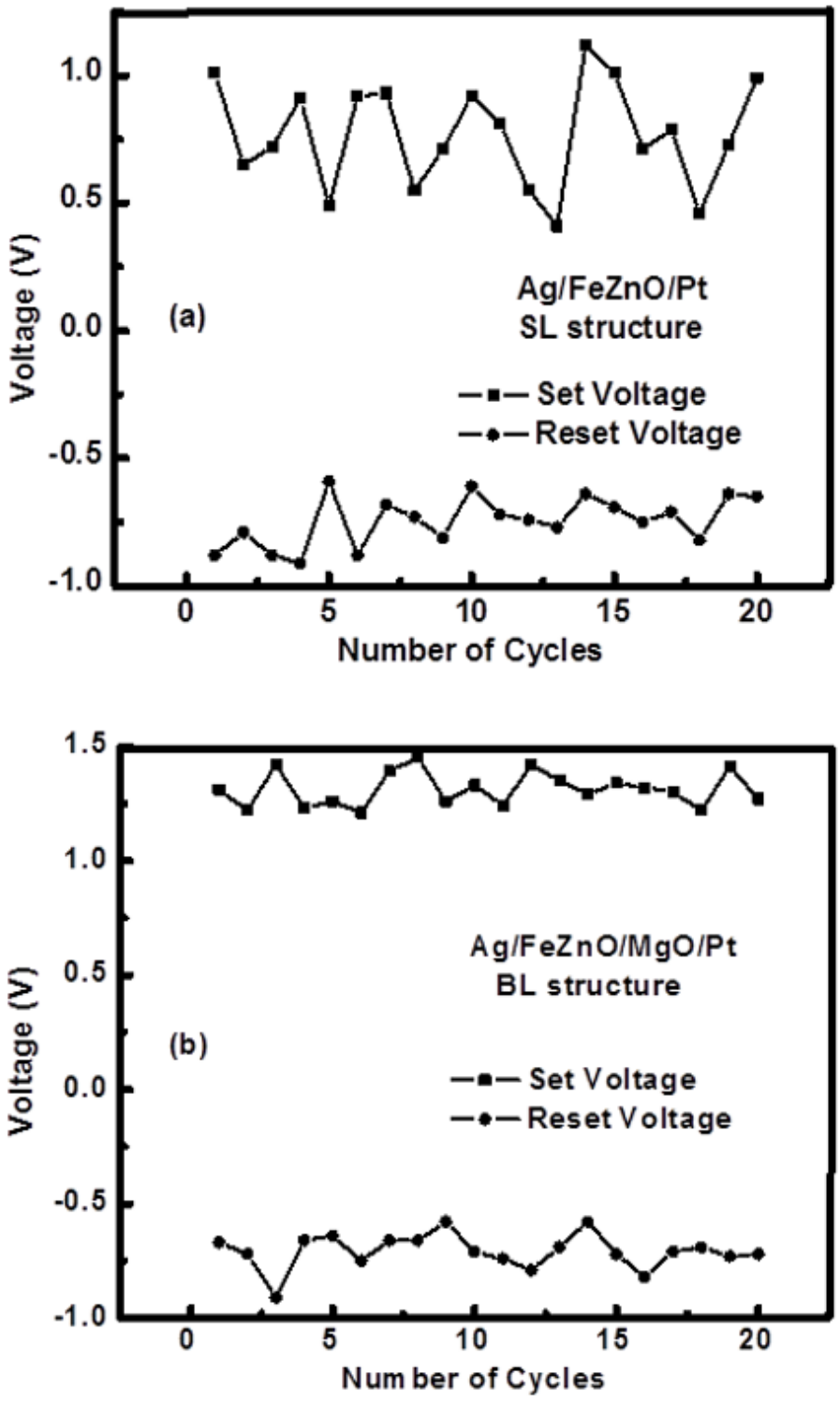


Figure 3.6 The distribution of the operation voltages of the (a) SL and (b) BL structures.

3.3. Unipolar Resistive Switching

Figure 3.7(a) shows the I-V characteristics of the Au/$Fe_{0.04}Zn_{0.96}O_x$/MgO/Pt unipolar resistive switching structure. The fabrication condition of unipolar RS structure is similar to that of bipolar RS device, the only difference is using Gold as the top electrode, At the beginning, the resistance state of the device is in HRS (step 1). When the applied voltage reaches the SET region, the device turns to LRS (step 2) and remains in LRS (step 3). When the voltage reaches the RESET voltage, the resistive state switches to HRS (step 4). When the measured voltage reaches 1V, the R_{HRS}/R_{LRS} ratio is 2.4×10^6. A retention time of 10^7 s has been obtained, and the results are shown in Figure 3.7(b). Higher fluctuations in HRS compared to LRS are due to the different conduction mechanisms between HRS and LRS. It is noteworthy to mention that after eight months (~2×10^7 s) and more than 200 testing cycles, the R_{HRS}/R_{LRS} ratio remained larger than 10^5.

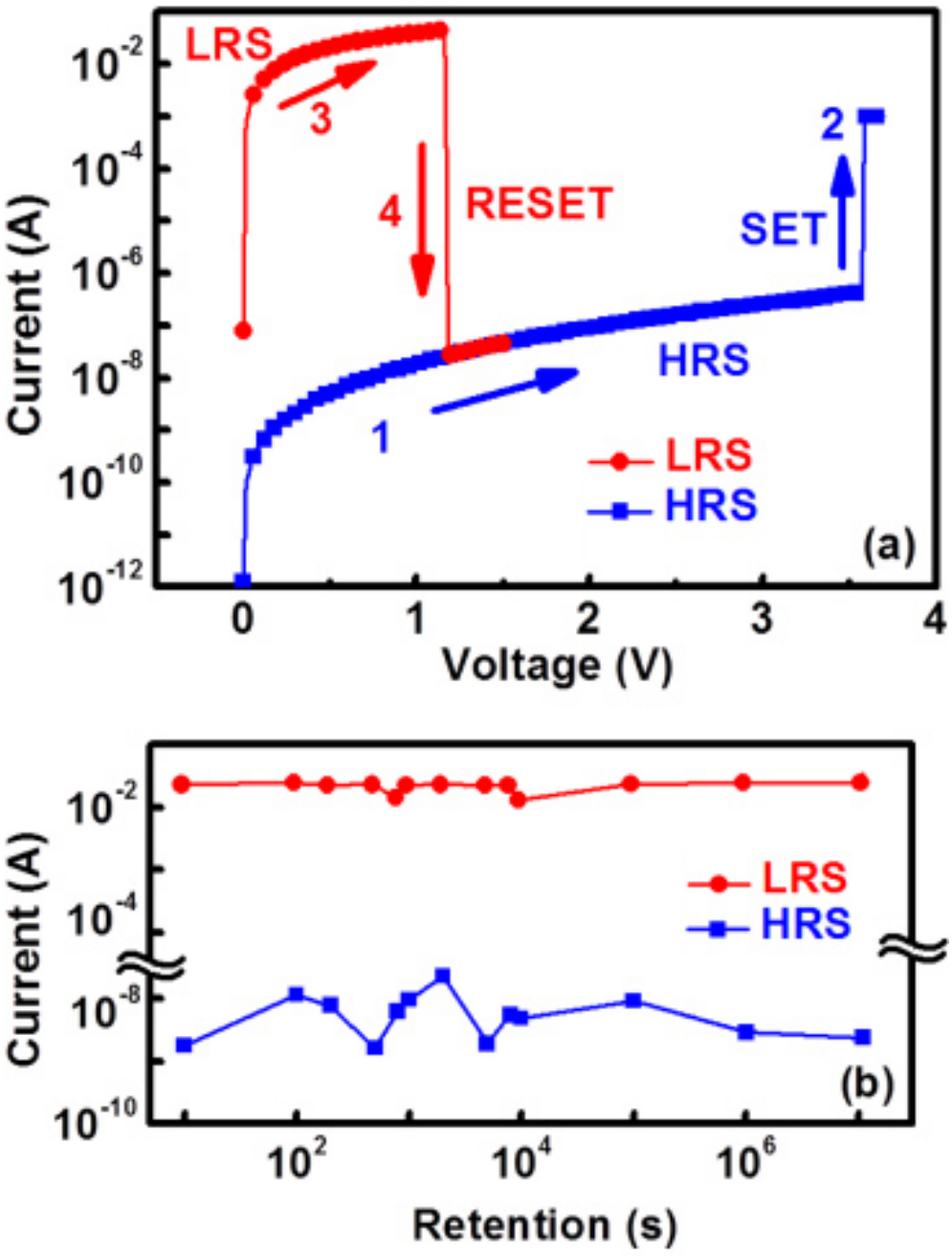


Figure 3.7 (a) The I-V characteristics and (b) retention time of the FeZnO/MgO switching resistor. The entire characterization was conducted at room temperature.

I-V characteristics of the unipolar switching device were also analyzed by curve-fitting to different current transportation models. In Figure 3.8 (a), the I-V characteristics

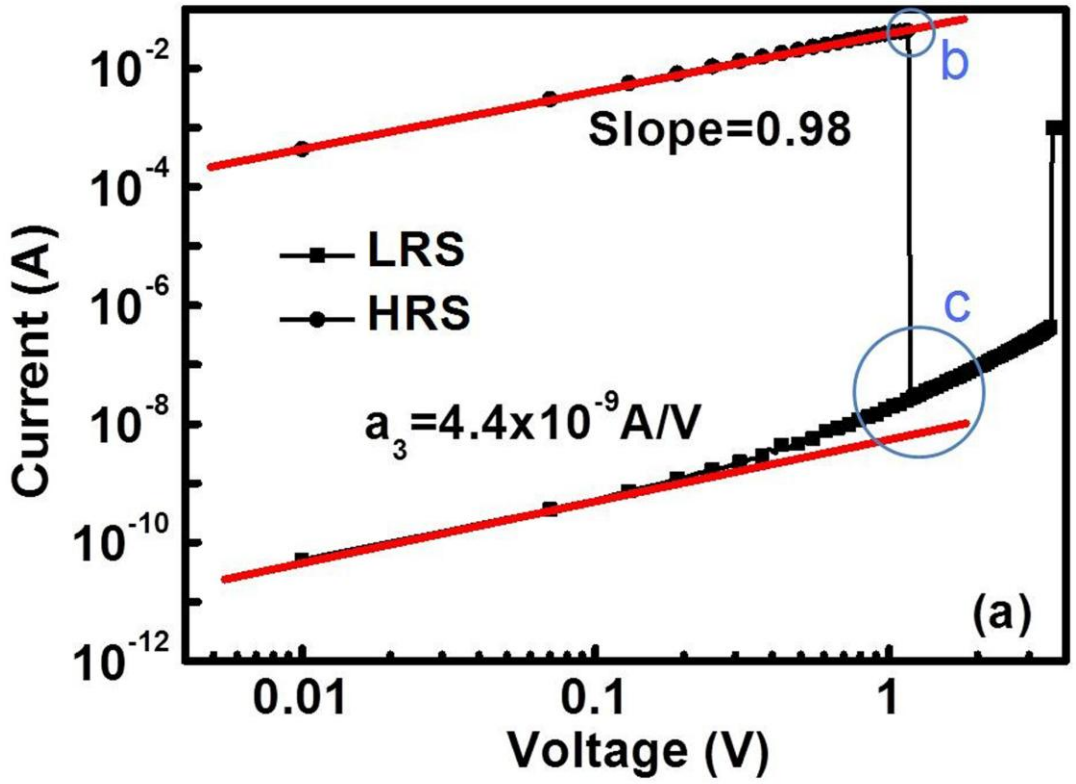
in LRS are fitted with a linear relation $I = a_1V$ in the log-log plot, where $a_1 = 0.042$ A/V, indicating good ohmic characteristics. However, at higher bias voltages (>1.1 V), the I-V curve shows a slight deviation from the initial linearity, as indicated in Figure 3.8 (b). This deviation at higher voltages is attributed to the Joule heating effect, which could increase resistance of conducting paths before the onset of the rupture process, leading to HRS.

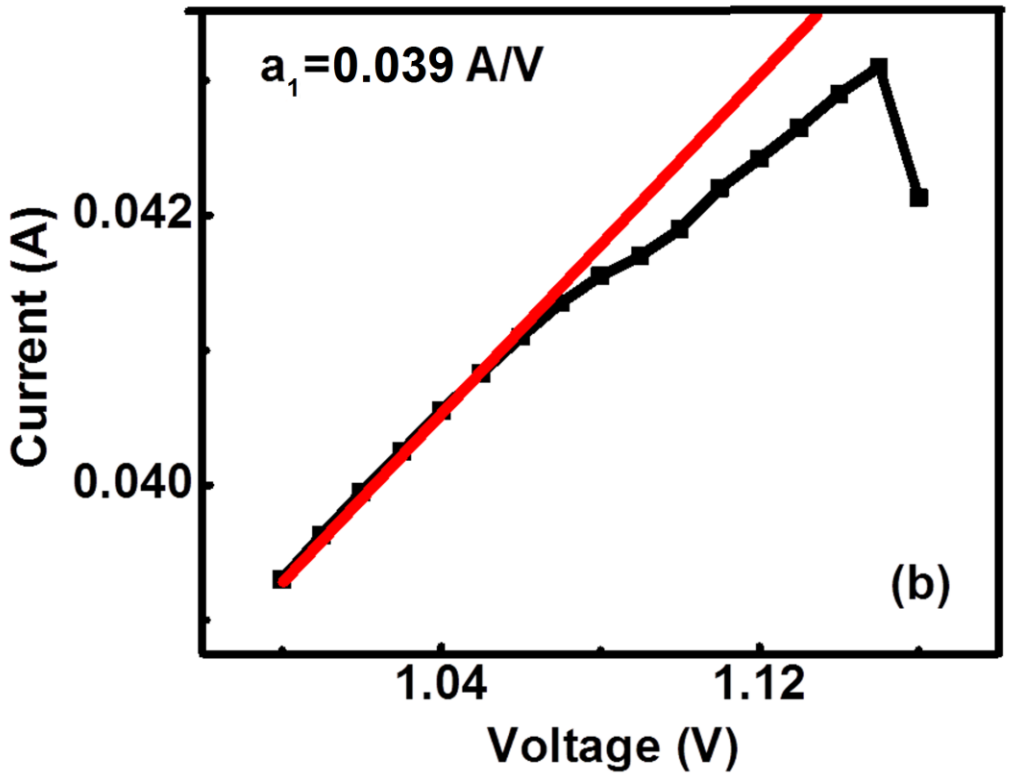
Fig. 3.8(c) illustrates the I-V characteristics of HRS and experimental results. The HRS curve is also fitted well to the following equation:

$$\ln\left(\frac{I}{V}\right) = a_2 \times V^{\frac{1}{2}} + b \qquad (1)$$

where $a_2 = 2.11$ and $b = -19.9$. It indicated the I-V characteristics of unipolar RS device at HRS also follow Poole-Frenkel emission (PFE) theory, as well as the bipolar RS device. At low voltages (<0.1V), it fits well with a linear relation of $I = a_3V$ as shown in Fig. 3.9(a), where $a_3 = 4.4\times10^{-9}$ A/V, which is $\sim10^7$ times less than a_1. This could result from the fact that the RESET process may not have totally ruptured all the conducting paths formed during the SET process, and thus there still exist a few conducting paths, which provide ohmic conduction with much higher resistance. From the curve fitting analysis, the resistive switching might result from the formation and rupture of the conducting paths composed by deep-level defects, such as oxygen vacancies (V_o), which serve as the positive charges according to the PFE model. In the FeZnO/MgO bilayer memory stack, the bonding energy of MgO is higher than that of ZnO, resulting in more difficulties in forming the Vo in the MgO layer than in the FeZnO layer. By adding a MgO layer to form the FeZnO/MgO bilayer switching structure, the Vo and related

conducting filaments are suppressed, resulting in higher HRS and more uniform performance of the resistive switching.




a1=0.039 A/V
Current (A)
0.042
0.040
(b)
1.04
1.12
Voltage (V)

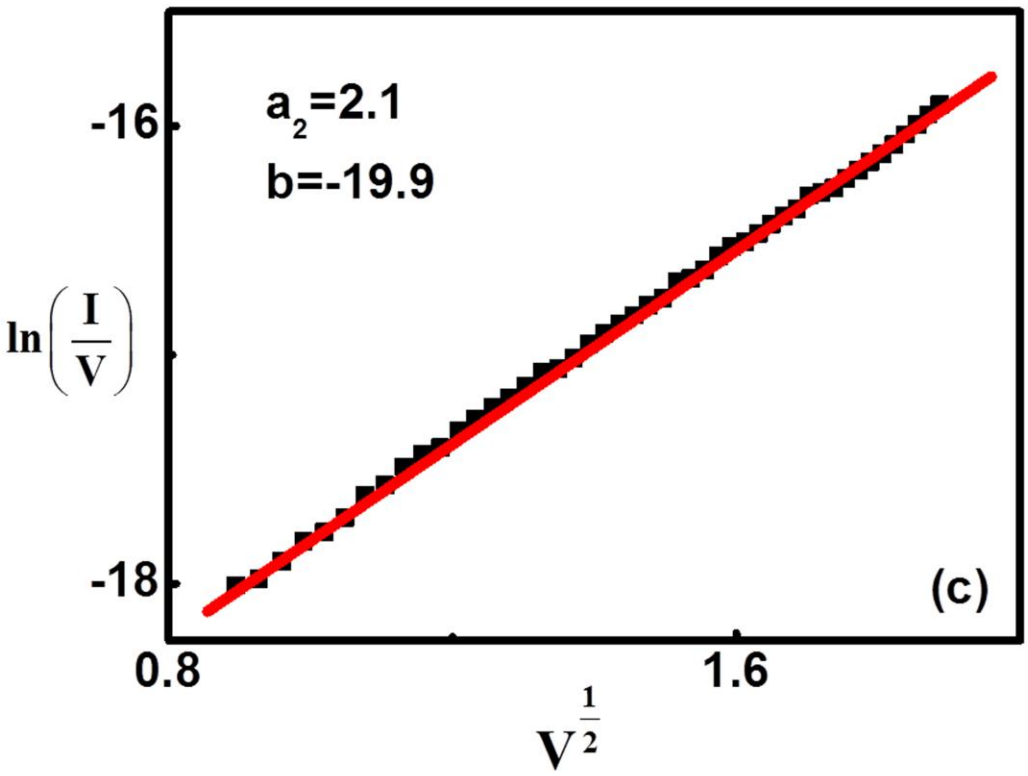

a2=2.1
b=-19.9
-16
-18
ln(I/V)
(c)
0.8
1.6
V^1/2

Figure 3.8 (a) A log-log plot of I-V characteristics of the FeZnO/MgO switching resistor. (b) The enlarged region b in figure (a), where a slight deviation from the initial linearity of LRS occurs when the voltage is larger than 1.1 V. (c) The enlarged region c in figure (a), where the experimental data of HRS are fitted by the Poole-Frenkel model when the voltage is larger than 1V.

3.2.3 Thickness Dependence of Switching Polarity

Different types of RS polarities have their own advantages and disadvantages. Unipolar RS (URS) could simplify the unit operation with the unipolar voltage source, which is used for the 1D1R-based crossbar system and increase the density. Bipolar RS (BRS) is used for the integration with TFT to avoid the outside control system. Hence it may expand the application scope in memories to develop devices that can achieve the BRS and URS with the similar structure. In addition, the comparison discussion between URS and BRS may pave a way for understanding the mechanism for the resistive switching. Goux *et al* reported the BRS and URS could exist in NiO-based memory cell with a thermal oxided Ni layers and the different oxidation duration change the resistive switching mechanism from electrochemical-based mechanism to thermal-based mechanism. [62] Yoo *et al* changed the Ta concentration in the TaO_x to converse the URS to BRS and explained this phenomenon using random circuit breaker network model.[63] Hu *et al* applied different compliance current to obtain the URS or BRS in the Al/DLC (Diamond-like carbon)/W structure.[64]

Thickness of the active layer is a critical parameter for the resistive switching. Common RS device has the thickness of 5~500 nm. For the further investigation of the

thickness dependent RS behavior, the experiment is conducted with the following four samples with different resistive switching performance.

Table 3.1. Effects of thickness and electrodes on resistive switching performances:

Sample Number	A1	B1	A2	B2
Structure (Top electrode /oxide thickness)	Ag/70 nm	Au/70 nm	Ag/200 nm	Au/200 nm
Average Set Voltage (V)	1.31	2.79	1.84	3.66
Polarity	Bipolar	Unipolar	Unipolar	Unipolar

From Table 3.1, we can figure out that with same type of top electrode, thicker device performs larger Vset. The thicker device needs more voltage to reach certain electric field to SET the conductive filament. With the same thickness, the device with Ag top electrode possesses smaller V_{set} than that with Au top electrode. During SET process, Ag cations drift from the top electrode and reduce into the Ag metal atoms in the oxide layer. Therefore, the effective layer thickness for SET is decreased, and the electric field is also reduced.

With Au as the top electrode, both the thick (B1) and thin (B2) device show the unipolar RS. It is proposed that the oxygen vacancies or oxygen ions are involved in the formation of filament in the Au/Oxide/Pt structure. As soon as the filament is connected

between the TE and BE, the resistive state of the device is switched from the HRS to LRS. The device is reset back to HRS when the filament is ruptured by the Joule heating effect. Therefore this type of device presents unipolar RS behavior.

However, using Ag as the top electrode of thin (A1) device, under positive voltage, Ag cations could penetrate through the whole Chalcogenide (oxide) layer and be reduced by electrons flowing from the cathode to form Ag filaments, as shown in Figure 3.9. When a positive voltage is applied on Ag TE, the oxidation occurs on this electrochemically active material. Therefore Ag^+ cations are generated, which could be described as $Ag = Ag^+ + e^-$. If the oxide layer is relatively thin, the mobile Ag^+ cations drift toward Pt BE through the thin ZnO layer and are reduced there by electrons flowing from the cathode, i.e., $Ag^+ + e^- = Ag$. The successive precipitations of Ag metal atoms at the cathode lead to a growth of the Ag protrusion, which finally reaches the TE and forms a highly conductive path in the ON state. The filament is strong and can only be ruptured by negative voltage. When the polarity of the applied voltage is reversed, an electrochemical dissolution takes place somewhere along the filament, which also could be described as $Ag = Ag^+ + e$-, and Ag^+ cations drift back to the Ag TE and are reduced there by electrons flowing from the TE, i.e., $Ag^+ + e^- = Ag$. The rupture of the Ag filament reset the system into the OFF state. In this condition, the device shows the bipolar resistive switching and can be explained by MCM.

For thick (A2) device with silver top electrode, under the similar electric field and applied time of A1, Ag cations cannot penetrate through the whole oxide layer. Oxygen vacancies or oxygen ions involved in the whole filament formation. If the oxide layer is relatively thick, the Ag^+ cations may not be able to travel to the Pt BE and they are

reduced by capturing incoming free electrons, as shown in Figure 3.9. Therefore the Ag filament is partly formed, oxygen vacancies or oxygen ions also involved in the whole filament formation. Rupture is easily occurred in the weak part (oxygen involved part) by Joule Heating. In this condition, the device shows the unipolar resistive switching and can be explained by TCM.

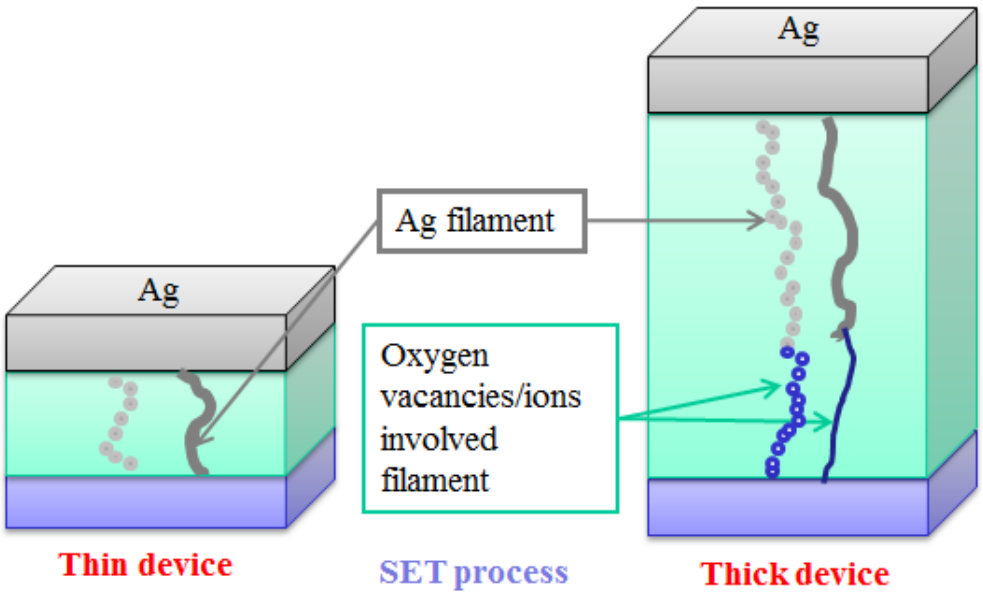


Figure 3.9 The proposed SET process and formed filament in the unipolar and bipolar resistive switching.

3.3. Ni-doped ZnO Resistive Switching Device Fabricated at Room Temperature

Recently, resistive switching (RS) memory devices have attracted increasing attentions due to their potential applications in the next-generation nonvolatile memory.

ZnO-based RS devices have inspired substantial scientific and commercial interests because of their high storage density, fast operating speed, low power operation, and well-controlled switching properties by *in-situ* doping and alloying. In addition, the feasibility of ZnO deposition at room temperature (RT) could reduce the processing cost of RS device, and increase the yield of multifunctional devices integration, as a result of no thermal budget. RT fabrication could also facilitate RS device process for flexible memory. The goal of the research is to demonstrate ZnO based RS devices using RT process on different substrates for novel memory applications.

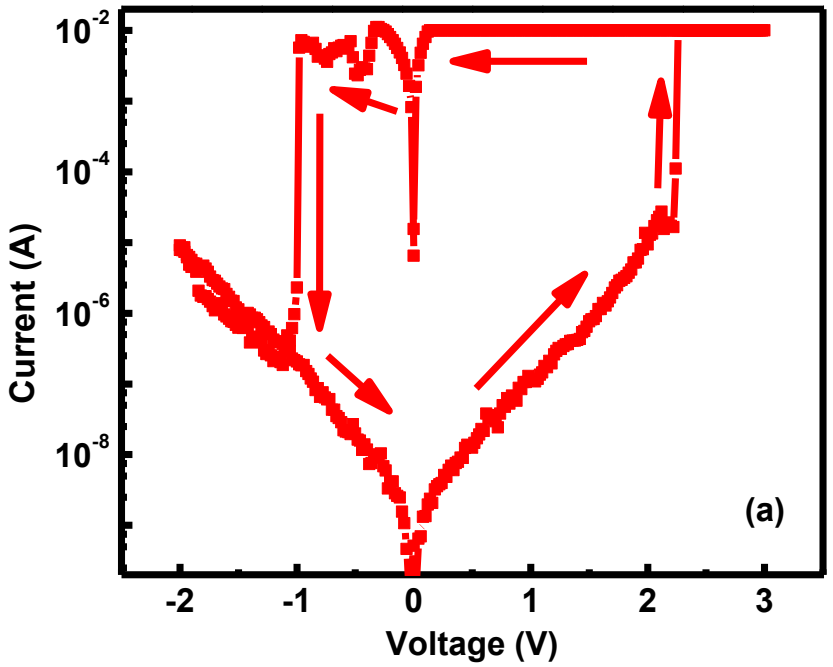
Flexible memory has been widely used in the novel display and wearable computer because it has advantages of excellent portability, low cost, light weight and user friendly interfaces over conventional bulk silicon technology. Kim et al. first reported using $Al/Al_xO_y/Al$ structure and glued the polymer substrate with the Si under 50 °C using oxygen plasma for the active layer. The ON/OFF ratio could be as large as 10^4, and they claimed that the switching can be explained by the formation and rupture of the conducting filament. [65] Gergel-Hackett et al. also mentioned to use TiO_2 as an active layer by sol gel deposition method. The operation voltage is larger than 2 V, and the ON/OFF ratio is larger than 10^4. [66] A flexible resistive switching memory device based on grapheme oxide (GO) is presented by Hong et al.. They used spin-coating methods with 100°C annealing for 1 hour. [67] Jeong et al. has been used TiO2-based device for flexible RRAM applications in the stacked crossbar system. However because it is fabricated by shadow mask and the dimension is relative large, the ON/OFF ratio is still less than 100. [68] Cheng et al. chose Ni/GeO/HfON/TaN structure for flexible memory and announced that it has the lowest recorded switching power(4.8 μW/1 nW) and

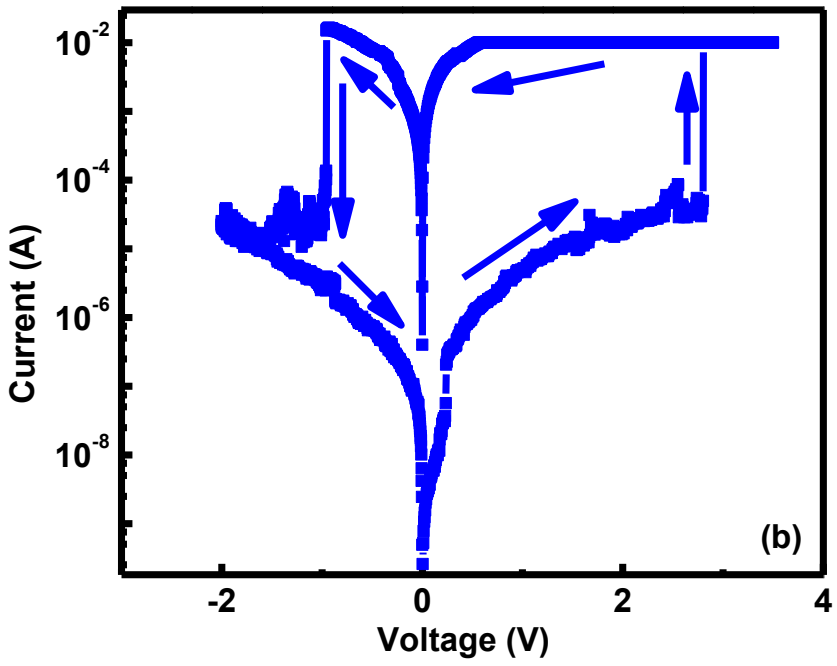
considered it is comparable to Nonvolatile memory on silicon. [69] Recently Mondal et al. used Sm_2O_3 and Lu_2O_3 thin films for low-power flexible memory application. Amorphous Sm_2O_3 and Lu_2O_3 thin films were deposited at room temperature by radio-frequency magnetron sputtering on flexible polyethylene terephthalate substrate. The filament conduction model was adopted to describe the RS behavior in the Sm_2O_3 and Lu_2O_3 ReRAM devices.[70]

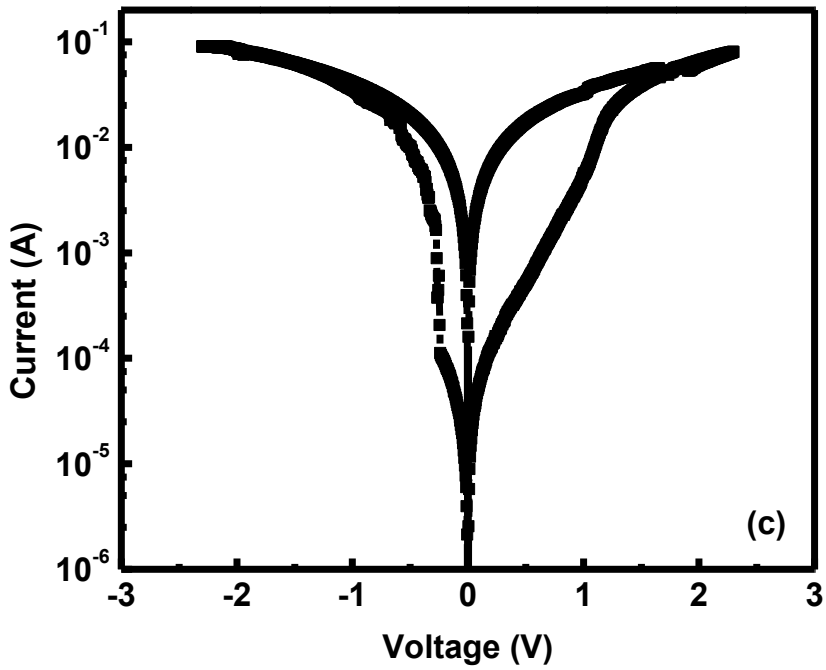
ZnO is a promising candidate for the flexible memory. First, ZnO is a kind of multifunctional material and using ZnO as the materials, many functional device could be achieved, such as resistive switching device, thin film transistor, and surface/body acoustic wave sensor. ZnO is a toxic-free material, and the ZnO based flexible memory could be used as the biosensor and wearable electronics. In addition, ZnO deposition is simple and could be done with room temperature, which is very important for most of the flexible polymer substrate. Last but not least, ZnO material is transparent and this character could broad the application field for the flexible memory devices. [71] Kim et al. used the sol gel method for ZnO as active layer and got fast programming speed. However the active layer needs annealing with the temperature above 100 °C, which is dangerous for the regular flexible substrate. [72] ITO/ZnO/ITO structure has also been studied by Seo et al. with the ON/OFF ratio of 100 and it shows the transparent performance. The problem is that the device needs Indium, which is expensive when compared with ZnO, and toxic for the human body. [73] Lee et al. used stainless steel as the substrate for ZnO-based flexible memory device and the ON/OFF ratio is about 100. All the fabrication was done under room temperature and no post-treatment was used. But the steel may limit the application for the flexible substrate. [74] Wang et al. used

InGaZnO as active layer by sputtering on a flexible plastic substrate and applied circular pads with a diameter of 0.5 mm for the shadow mask, and got good mechanical endurance, but the ON/OFF ratio is still about 100. [75] In order to solve the problems above and take the full advantage of the ZnO materials, ZnO based flexible memory has been studied in the thesis.

In the experiment, the Ni-doped ZnO is deposited as the active layer of the RS devices using sputtering technology. Ni doping enhances the compensation of oxygen deficiency in ZnO, resulting in larger high resistive state (HRS) values in RS. The Platinum bottom electrode and silver top electrode are formed by e-beam evaporation and photolithography. All of the fabrications are at room temperature. The IV characteristics are shown in Fig. 3.10. At the reading voltage of 0.1V, the resistance ratio of R_{HRS}/R_{LRS} for RS device on SiO_2/Si is 5.96×10^6. The dominant conduction mechanisms are attributed to the Poole-Frenkel emission at the HRS and Ohmic behavior at the LRS, respectively. For the application of flexible memory, the RS devices are also fabricated on the polymer substrate. The resistance ratio is 4.91×10^2, as shown in the Fig. 3.10 (b). Compared with the RS device on Si, the resistance ratio of RS device on flexible substrate is much smaller. Rough surface for the polymer substrate may introduce more leakage for the active NiZnO layer and even with RESET process it is difficult for the devices to totally switch back to the HRS. The feasibility of fabricating the RS devices on polymer substrates paves the way for flexible memory and display applications.


Current (A)
10^-2
10^-4
10^-6
10^-8
-2
-1
0
1
2
3
Voltage (V)
(a)


Current (A)
10^-2
10^-4
10^-6
10^-8
-2
0
2
4
Voltage (V)
(b)


Current (A)
Voltage (V)
(c)

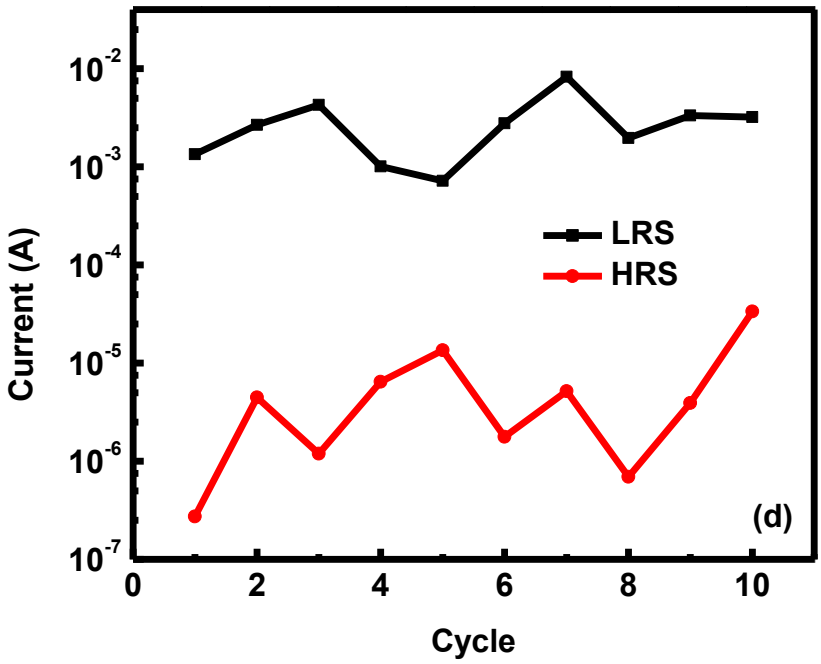

Current (A)
Cycle
LRS
HRS
(d)

Figure 3.10 The IV characteristics of ZnO based resistive switching device on SiO_2/Si (a) and polymer flexible substrate (b) at RT. (c) The flexible memory fabricated with shadow mask with the dimension of 400 um. (d) The stability of the flexible resistive switching.

In order to keep the processing condition at room temperature processing, single NiZnO layer was deposited as the active layer using sputtering method. The main difficulty was to protect the flexible substrate from being damaged through the deposition and fabrication process. To avoid complex process, shadow mask with common bottom electrode and active layer are applied for fabrication. Only the top electrode is deposited using electron beam evaporation with the shadow mask for pattern the metal. Because of the shadow mask preparing difficulties, the minimum dimension we used for the shadow hole was 400 um. According to the discussion for HRS curve fitting in this chapter before, because the area for the top electrode is relative large, there are a lot of tiny filament cannot be totally ruptured by RESET process and the current in HRS is relatively high. At the reading voltage of 0.05V, the current in the LRS and HRS are 1.75×10^{-3} A and 2.91×10^{-5} A, respectively. The ON/OFF ratio is 60.3, as shown in the figure 3.10 (c). Compared with the result of regular resistive switching device, the LRS is in the similar range, but the current in the HRS is too high, leading to lower ratio. Compared with the stability characteristics with the regular switching device, the resistive switching device on flexible substrate is much worse, as shown in figure 3.11 (d). The reason for this problem may be from the fabrication condition. The polymer surface is much rougher than the regular SiO_2/Si substrate and with the double-side adhesive tape

the surface condition may be worse. Rough surface may introduce more leakage for the active NiZnO layer and even with RESET process it is difficult for the device totally return back to the HRS.

3.4 Summary

The nanometer scale $Fe_xZn_{1-x}O$ films are used to make both of bipolar and unipolar memory resistors, and the polarity of the memory resistors is dependent on the electrode and the thickness of the oxide. The multifunctional ZnO and its ternary compounds are grown through MOCVD with in-situ doping. The Au/FexZn1-xO(70 nm)/MgO(5 nm)/Pt structure shows the unipolar resistive switching with the ratio of the high resistance state (HRS) over the low resistance state (LRS) over 10^6 at 1V, while the Ag /FexZn1-xO (70 nm) /MgO (5 nm) /Pt structure shows bipolar resistance switching with the ON/OFF ratio over 10^5 at 1V. It is found that the mechanism of HRS and LRS is Poole-Frenkel emission and resistive conduction, respectively. By using the FeZnO/MgO (BL) oxide structure, switching performances including R_{HRS}/R_{LRS} ratio and switching stability are significantly improved in comparison with that of the FeZnO only (SL) oxide structure. The BL structure has the similar R_{LRS}, however, its RHRS increases by 10^3 over the SL counterpart, and overall R_{HRS}/R_{LRS} ratio of 10^6 is achieved. These improvements are useful in RRAM application, where large R_{HRS}/R_{LRS} ratio would prevent false reading signals while narrow distribution of V_{SET} and R_{HRS} would confine writing voltage and reading signal range. These improvements are mainly attributed to the oxygen vacancy suppression in the MgO layer of the BL structure. The difference in thickness and electrode materials could lead to different polarities. In order to fulfill the

requirement of room temperature process, Ni-doped ZnO is also been used in the resistive switching devices.

Chapter 4

Resistive Switching Mode Conversion Controlled by Compliance Current

In the previous chapter, we discussed the single resistive switching device with unipolar and bipolar performance. Beginning in this chapter we will discuss various methods to explain the mechanism of the resistive switching. From Chapter 2 we learned that there are several theories based on the conversion modes for similar switching structures. We observed three types of reversible resistive switching modes for resistive random access memory using Ni-doped ZnO/MgO structure. By controlling the compliance current limitation during SET process, threshold switching, volatile switching and memory switching could be achieved and converted. Compared with the memory switching, the volatile switching processes the advantages of lower power consumption and better HRS stability. Different compliance currents lead to different LRS, which could be used for multi-level per storage cell applications. Combined the electrical characteristics with TEM analysis, it could be figured out that compliance current setting affect the formation and rupture for different shapes of metallic filaments, which also lead to the conversion of different switching modes. In addition, one kind of materials which could process two memory switching polarities is highly attractive because the specific advantages of the two modes broaden the application scope of the device and enable larger flexibility in terms of memory architecture.

4.1. Introduction

The resistive random access memory (RRAM) becomes a promising candidate for the next generation of memory technology due to its low-power-consumption, high-device density, and fast-speed.[1, 76] Based on the switching mode, there are mainly two different types of resistive switching devices reported so far: memory switching and threshold switching.[28] In the memory switching device, the resistance state keeps the previous state until the SET/RESET voltage is reached, no matter the power is on or off. On the other hand, in the threshold switching device, after SET process the resistive state cannot keep in the low resistance state (LRS) under a small voltage (less than threshold voltage), it would return into the high resistance state (HRS). In contrast to the memory switching, the threshold switching can avoid the RESET process and reduce the power consumption that could be a good supplement for the non-volatile memory.

Several groups have reported to achieve the conversion between the memory switching and threshold switching. Chang *et al*. observed two types of reversible resistance switching effects by controlling thermal cycling in a NiO film: the memory resistive switching at low temperature while the threshold resistive switching at high temperature. [29] They used a dynamic percolation model to explain the transition phenomena and showed that the resistive switching effects are controlled by the thermal stability of the conduction filaments, and the conversion from the two types of resistive switching results from the competition between Joule heating and thermal dissipation. Hwang *et al* use the voltage pulse to change between the bi-stable memory switching and the mono-stable threshold switching in Pt/NiO/Pt structure. [77] The memory switching was changed to the threshold resistive switching by applying a positive electrical pulse;

the change was reversible by applying a negative electrical pulse. The migration of oxygen ions is responsible for the switching transition in Pt/NiO/Pt structures. It is also demonstrated that via tuning the strong electron correlation the memory and threshold resistive switching could be converted. In the same manuscript, it is reported that annealing the NiO_x sample in vacuum at 300°C for 30 minutes could also change the threshold switching to the memory switching.

During the SET process, compliance current is commonly applied on the device between the top and bottom electrodes to protect the device from hard-breakdown. [33] It is discovered that the current limitation in the SET process will affect the parameters of the resistive switching, such as the resistance in the LRS. [13] Su *et al* used temperature dependent electrical characteristics to present different models for resistive switching with compliance current changing. [78] However, current reports are lack of direct evidences to explain the effect of compliance current. Recently, there is a report of nanoisland system to use the compliance current setting to get the threshold switching and memory switching. [35] However, in the threshold switching, there is only one stable resistive state and the resistive state will return back to HRS in the low voltage region, which is the region commonly used as the reading voltage for memory device. [76] Therefore, it is difficult for the threshold switching to use as a memory device and the applications are limited to the temporary switching, or in contrast experiment with memory switching mechanism study. In the manuscript, we reported another switching mode called volatile switching. In the volatile switching we avoid the additional RESET process, which is necessary for memory switching. On the other hand, LRS of volatile switching could keep in the small voltage, which is different from the threshold

switching. We also used the TEM and electrical characteristics to prove connection between compliance current, conductive filament formation and difference of the switching modes.

4.2. Device Structure and Design

The resistive switching devices were fabricated on the conventional Silicon wafer. 300 nm SiO_2 was thermally grown on the Si for insulating bulk substrate. Bottom electrode Pt (100 nm) was evaporated on the adhesive Ti layer (10 nm). The active layer of the resistive switching device consists of a Ni-doped ZnO (40 nm, deposited by sputtering) on the top of MgO (10 nm, deposited by MOCVD). Ni doping could compensate the oxygen deficiency in ZnO and decrease the carrier density.[10] Therefore, after RESET the HRS for resistive switching in the ZnO-based active layer is increased. The Ni-ZnO/MgO used as the two layer structure could increase the HRS value and enhance the stability of the switching device. [80] The top electrode is 100 nm silver layer with the 30 nm gold coating layer using e-beam evaporation. The structure for cross-section was shown by TEM in Figure 4.1. The diameter of the circle device tested for resistive switching is 120 um. The current-voltage characteristics were tested with an Agilent 4156C semiconductor parameters analyzer in the voltage sweeping mode. The TEM/EDS characterization was carried out by Hitachi HD 2700C.

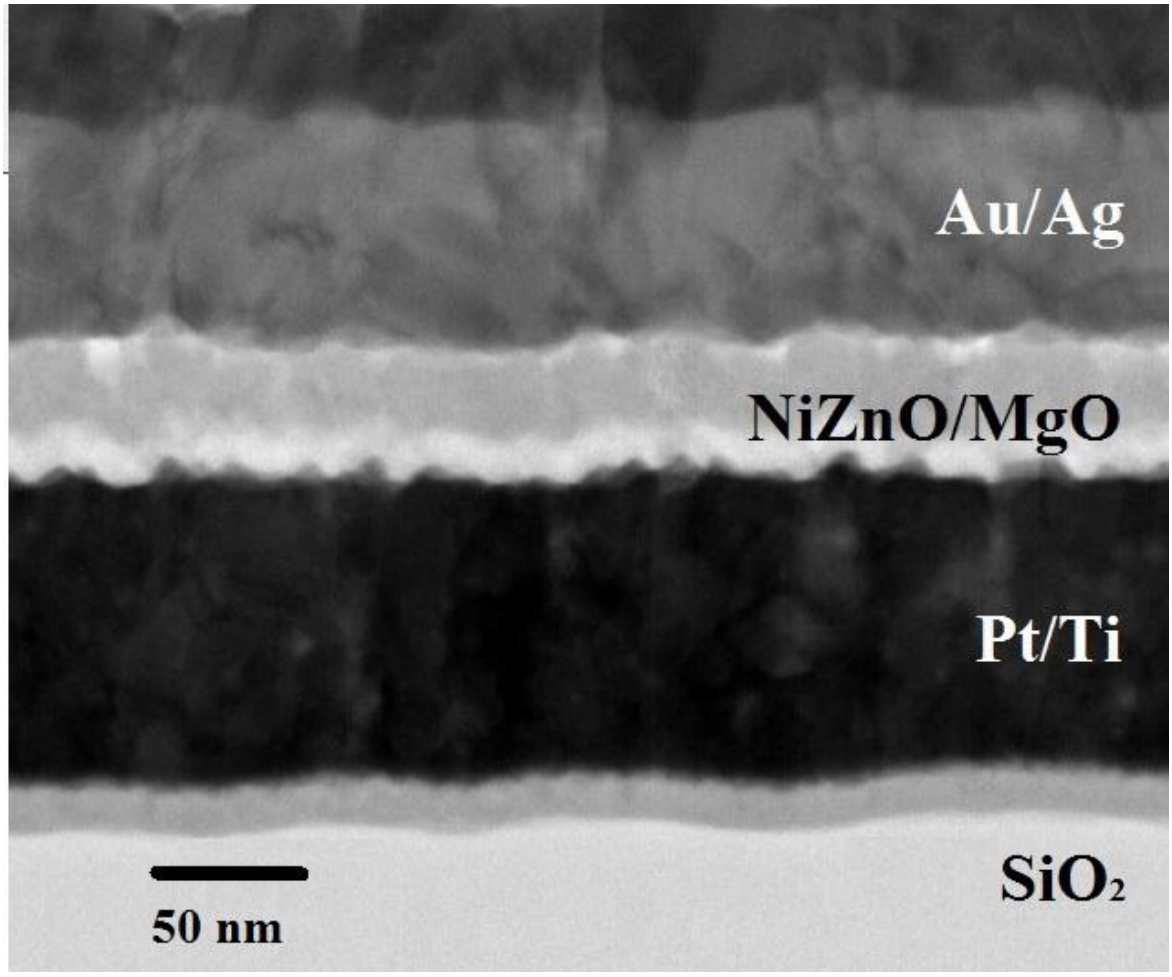


Figure 4.1. A cross-sectional TEM image of the resistive switching devices.

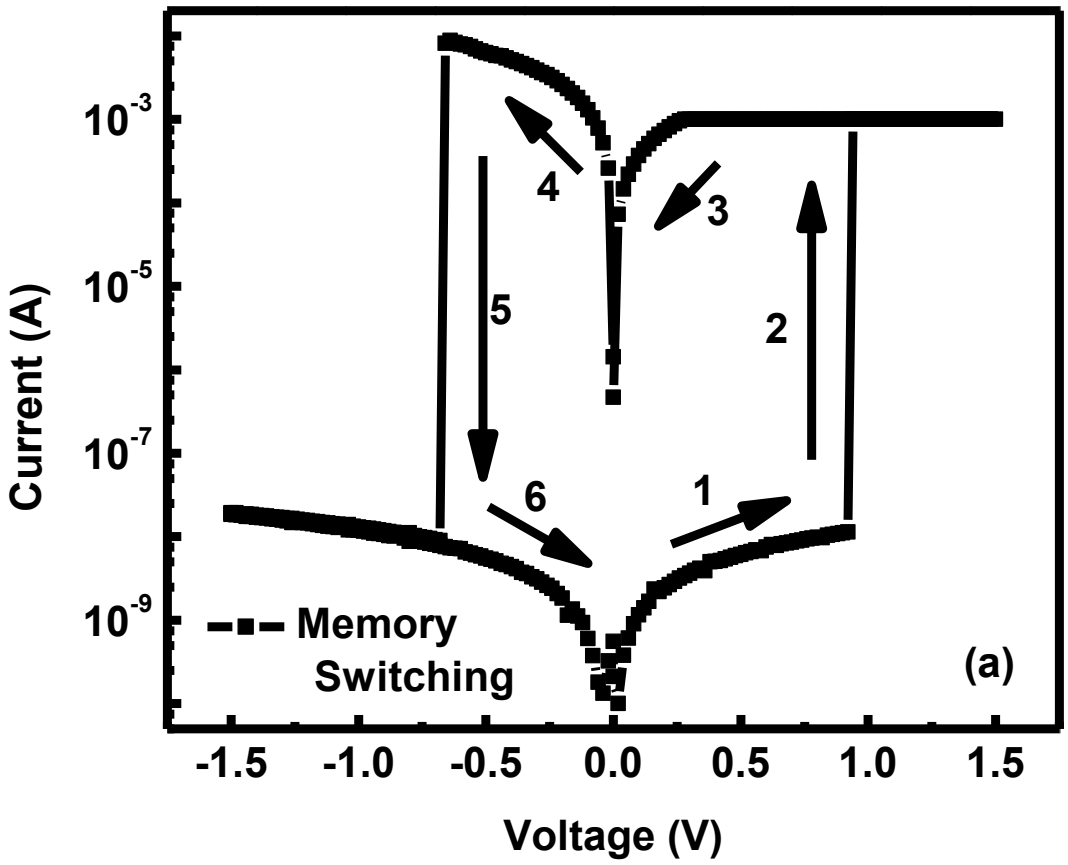
4.3 Electrical Characteristics for Modes Conversion

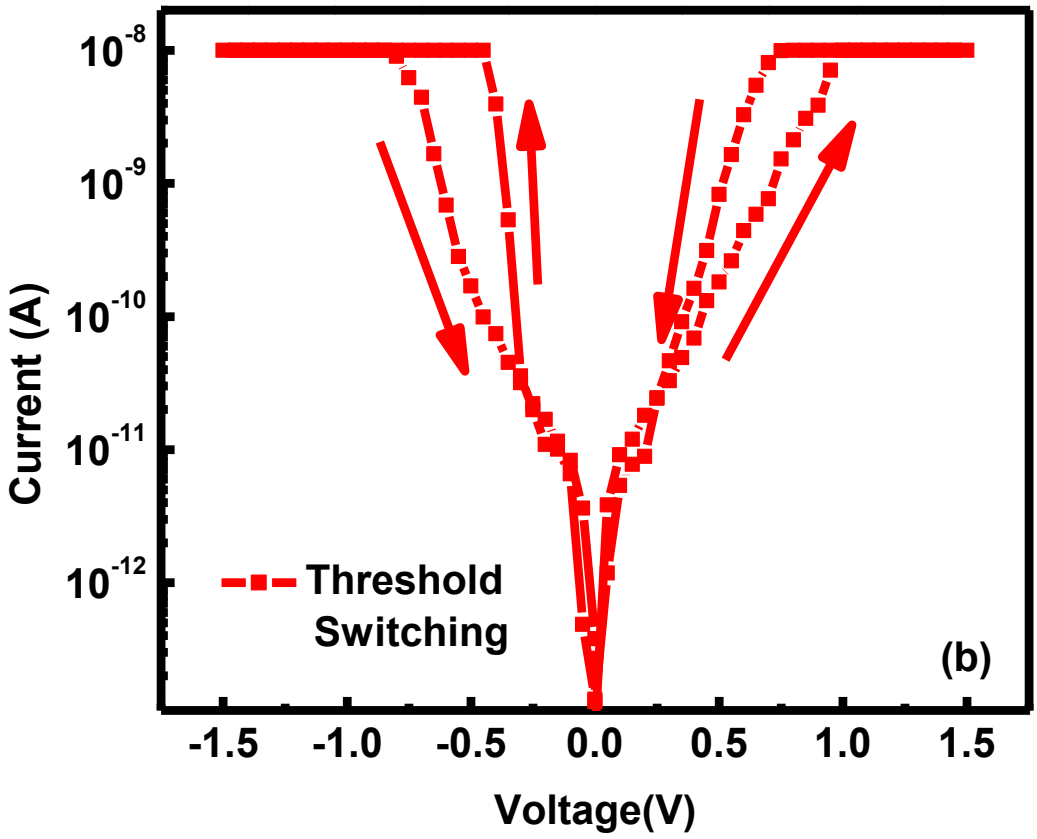
The IV characteristics of three switching modes are shown in Fig. 4.2. During the testing, the bottom electrode is connected to the ground and the varied voltage is applied to the top electrode. It is shown that the current go through the active oxide layer between the two electrodes and the current also represents the resistance state. At first, the device is in HRS, as shown the step 1 of the Fig. 4.2. When the threshold voltage is reached at step 2, the current increased dramatically and the SET process occurs. If the current

limitation is limited as 1 mA, no matter whether the power is on or off, the device keeps in LRS until it reached to RESET voltage. Therefore, in this condition, the device shows memory switching behavior. At the reading voltage of 0.05V, the resistance ratio of R_{HRS}/R_{LRS} is 2.47×10^5, as shown in Fig. 4.2(a). If the compliance current setting is changed to 10 nA for SET, the LRS cannot sustain in the low voltage and the resistance state will return back to the HRS, as shown in Fig. 4.2 (b). This behavior is called threshold switching because the device has the threshold voltage range for SET and RESET. The threshold switching can be free of RESET process, but it is difficult to find the reading voltage as the memory behavior measurement in the threshold switching device. Normally the reading voltage of the resistive switching should be less than one tenth of the write voltage, [76] therefore the interference between read and write process could be avoided for multi-cycles testing. However in the threshold switching, the LRS cannot sustain in the low voltage and the resistance state will return back to HRS. This performance of threshold switching increases the difficulties for memory characteristics.

If the compliance current is set at the middle range of 1 μA, another switching mode - volatile switching could be achieved, which is shown in the Fig. 4.2 (c). In this mode, the IV memory loop looks similar as the memory switching; however, if the power for the resistive switching device is off, the device would automatically return back to the HRS and save the RESET process. On the other hand, the memory behavior still could be read out because in the low voltage range of the volatile switching, LRS still could keep the resistance state unless the power is off. The resistance ratio of the volatile switching is about 1.49×10^3 at 0.05V. After 10^7 s of retention time and 10^4 testing cycles, the device still keeps the robust switching performance. In the same reading voltage, the threshold

switching could only be in HRS as shown in Fig. 4.2(b).




Current (A)
10-8
10-9
10-10
10-11
10-12
Threshold
Switching
(b)
-1.5
-1.0
-0.5
0.0
0.5
1.0
1.5
Voltage(V)

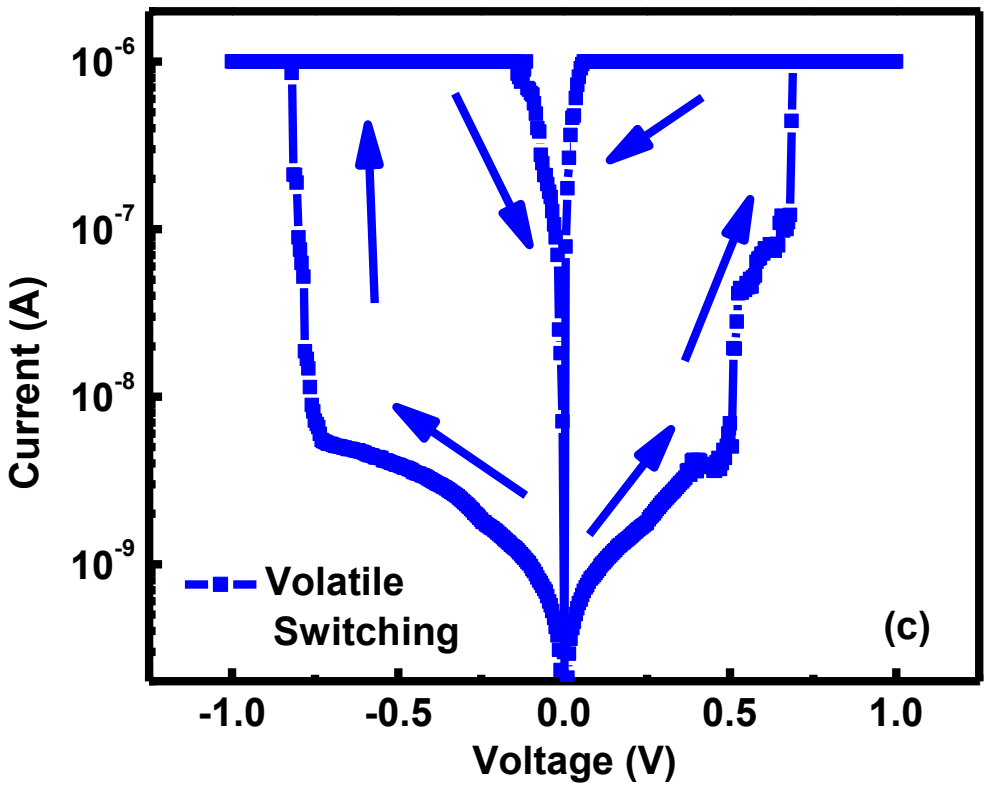
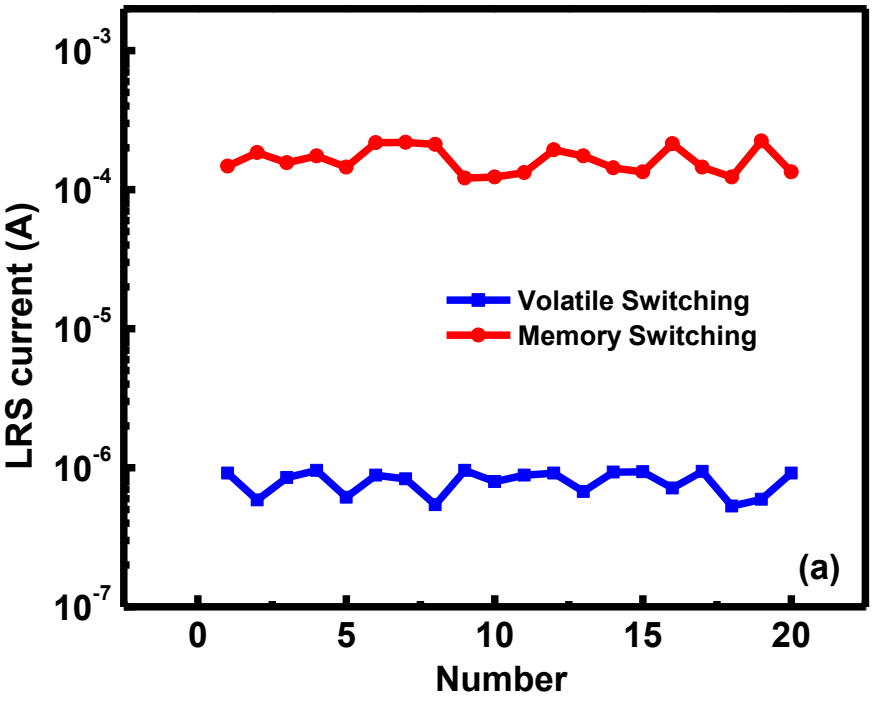
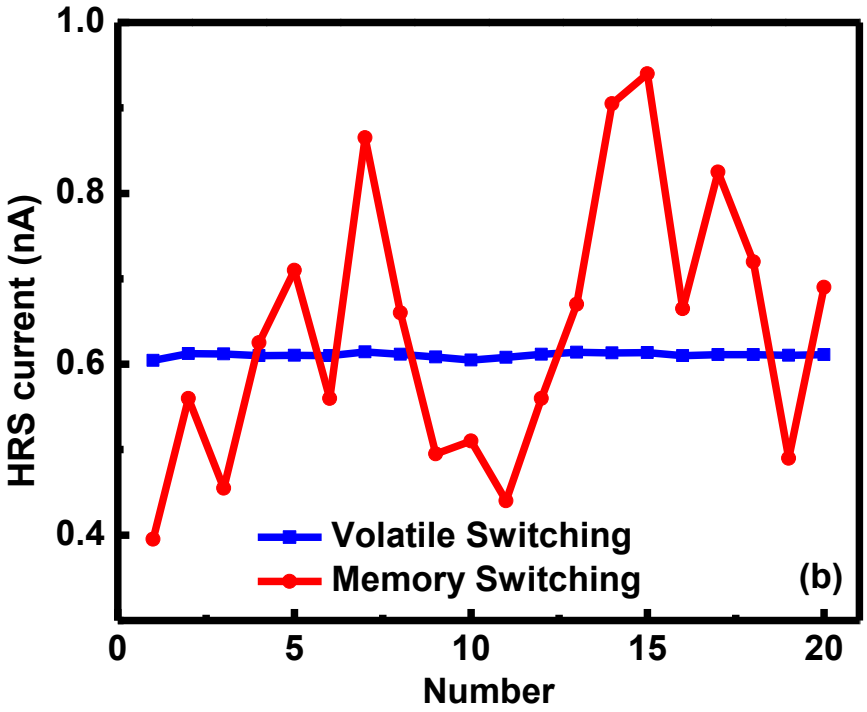


Figure 4.2. The IV characteristics of (a) memory switching, (b) threshold switching, and (c) volatile switching. The switching mode can be converted by changing the compliance currents.

Figure 4.3 shows the performance comparison between volatile switching and memory switching. Threshold resistive switching mode has not been discussed because of the difficulty for choosing the reading voltage in the small voltage range. From the curve fitting, the conductions for HRS of both switching modes are recognized as Poole-Frankel emission. From the Fig. 4.3(a) it could be figured out that the LRS in the memory switching (when the compliance current in the device is 1 mA) is much smaller than that

in volatile switching (when the compliance current is 1 μA). The difference between these two modes may lead to the value difference of LRS, which both fit well for the ohmic conduction. Fig. 4.3 (b) exhibits the HRS stability comparison. The HRS stability of volatile switching is much less than memory switching, which may result from the high power consumption of the memory switching device during the testing. Fig. 4.3(c) shows the operation current under the different compliance current. It should be mentioned that when the compliance current is set around 1 μA, the device show the threshold switching behavior and when the compliance current larger than 50 μA it is the memory switching. It indicates that with different compliance currents, the resistive switching device could get different LRS. When the compliance current limitation in the SET increases, the current in the LRS also increases, indicating the resistance decrease. On the other hand, the HRS does not change significantly with the compliance current varying. For the multi-level storage per cell (MLC) application, the single device could be applied with different compliance current and get different current in LRS at reading voltage, and the large gap difference could facilitate the MLC functionalization.


LRS current (A)
10-3
10-4
10-5
10-6
10-7
Volatile Switching
Memory Switching
(a)
0
5
10
15
20
Number


HRS current (nA)
1.0
0.8
0.6
0.4
Volatile Switching
Memory Switching
(b)
0
5
10
15
20
Number

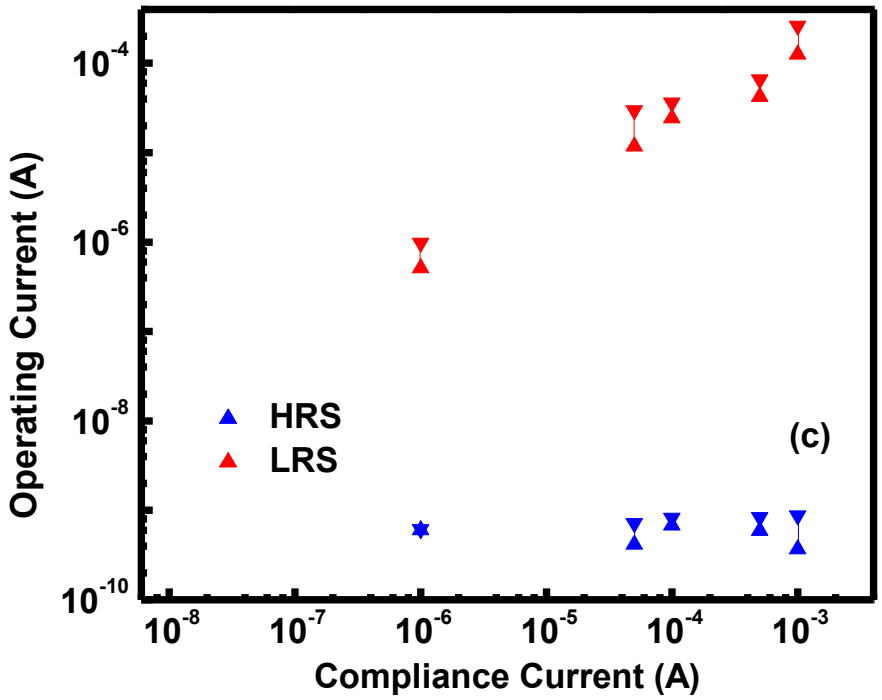
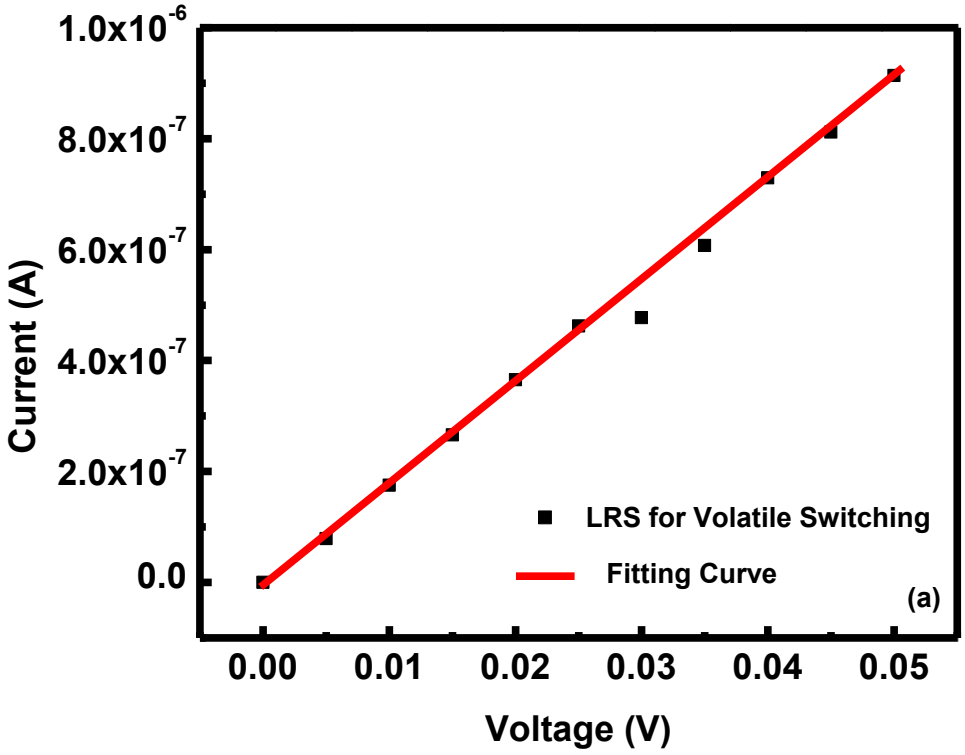


Figure 4.3. (a) LRS current, (b) HRS current comparison of the volatile switching and memory switching. (c) The different reading current at different compliance current. The reading voltage is set at 0.05 V.


1.0x10-6
8.0x10-7
6.0x10-7
4.0x10-7
2.0x10-7
0.0
Current (A)
0.00
0.01
0.02
0.03
0.04
0.05
Voltage (V)
LRS for Volatile Switching
Fitting Curve
(a)

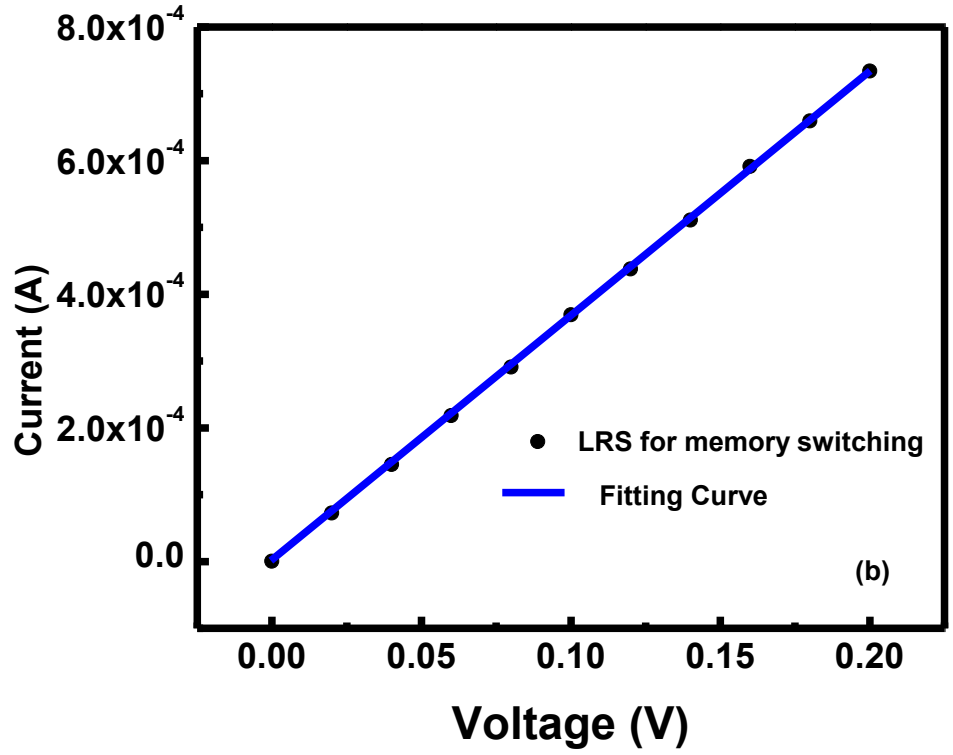

8.0x10-4
6.0x10-4
4.0x10-4
2.0x10-4
0.0
Current (A)
0.00
0.05
0.10
0.15
0.20
Voltage (V)
LRS for memory switching
Fitting Curve
(b)

Figure 4.4. The LRS curve fitting for volatile switching (a) and memory switching (b).

Figure 4.4 show the curve fitting for IV characteristics in LRS for the volatile switching and memory switching. Both of the curve were fitted well for the ohmic conduction. Form the analysis of Chapter 3 the LRS of resistive switching may involved with the formation of the metallic filament. It could be calculated that the resistance of LRS in the volatile switching and memory switching are 5.47×10^{4} Ω, and 2.73×10^{2} Ω, respectively. The different resistance ratio for volatile switching and memory switching is 2.0×10^{2}, which is result from the different compliance current setting.

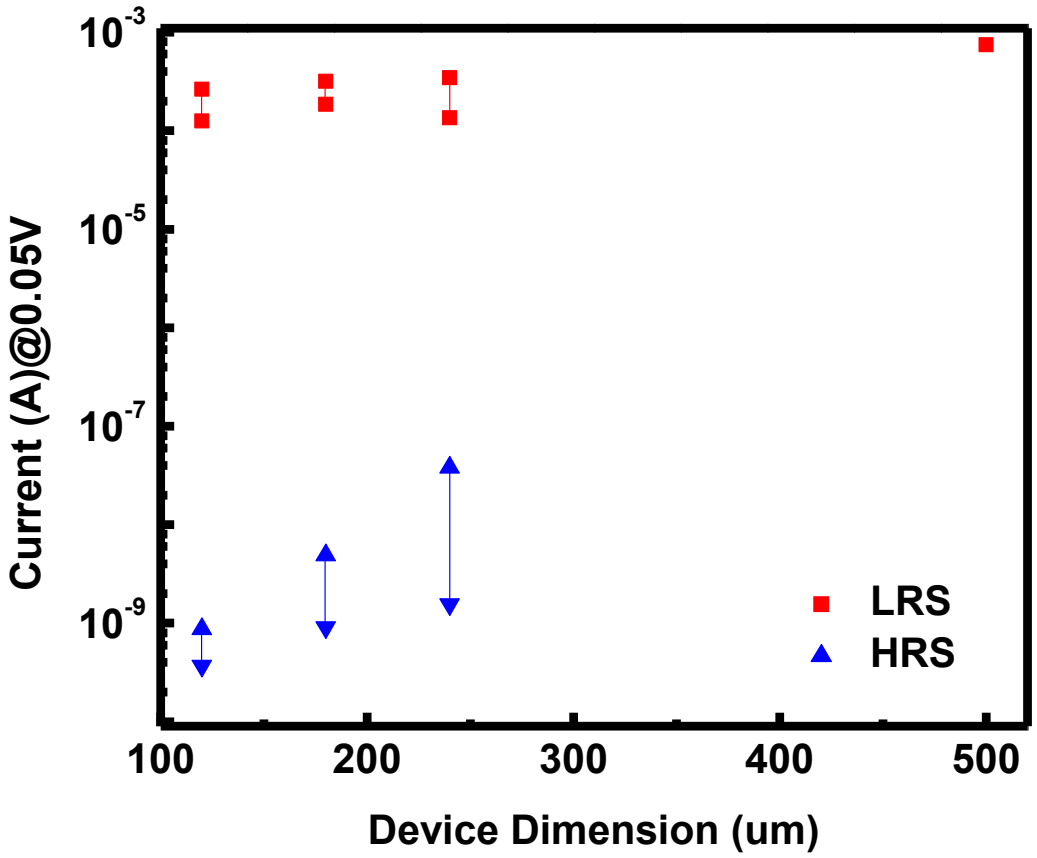


Figure 4.5. The IV characteristics for memory switching with different dimension

Figure 4.5 present the electrical characterization for memory switching with different dimensions. The diameters of the device are 120 μm, 180 μm 240 μm and 500 μm. As small as 6 μm for the diameter have been designed for the mask, however due to the probe size limitation, if the size of the top electrode is smaller than 120 μm, more steps need to be done for the testing. On the other side, if the diameter is larger than 400 μm, such as 500 μm, the device can only switch from HRS to LRS, and cannot RESET back to the HRS. It could also be figured out that compared with the LRS in different size, the current in LRS is not proportional to the area size of the device. However, when the size increase, the current in the LRS shows the increasement. For example, compared with the devices with the size of 240 μm and 120 μm, the area size ratio is 4:1, but the average current ratio is 0.98 mA/0.77 mA, which is only 1.27. Therefore , it is indicated that the switching device is not scalable for the current dimension.

Combined with the discussion in the previous curve fitting results for the LRS, it is indicated that the resistance in the LRS is mainly dependent on the dominate filament connected between the top and bottom electrode. There may a lot of filaments connected during the SET, however all the filaments are connected parallel. Therefore, the whole resistance in LRS is dependent on the filament with the smallest resistance. The LRS depenence on the device dimension also prove this assumption. It means that different from the uniform cause for the resistive switching, the formation and rupture of the dominated filament result in the SET and RESET of the switching device. Therefore, when the size of the device increase, the dominated filament will barely be affected, and

the current does not show the significant difference. On the other hand, because of the mechanism of the HRS is the Poole Frankel emission, the trap emission should be proportional to the area size, therfore the HRS is scalable with the dimension. Also it is shown in the figure that when the size increase, the parameter stability for the HRS become worse. It may because that there are some tiny filaments existing after RESET, and when the size increase, there will be more possibility for not totally rupture of the filaments, therefore the resistance ranges become larger.

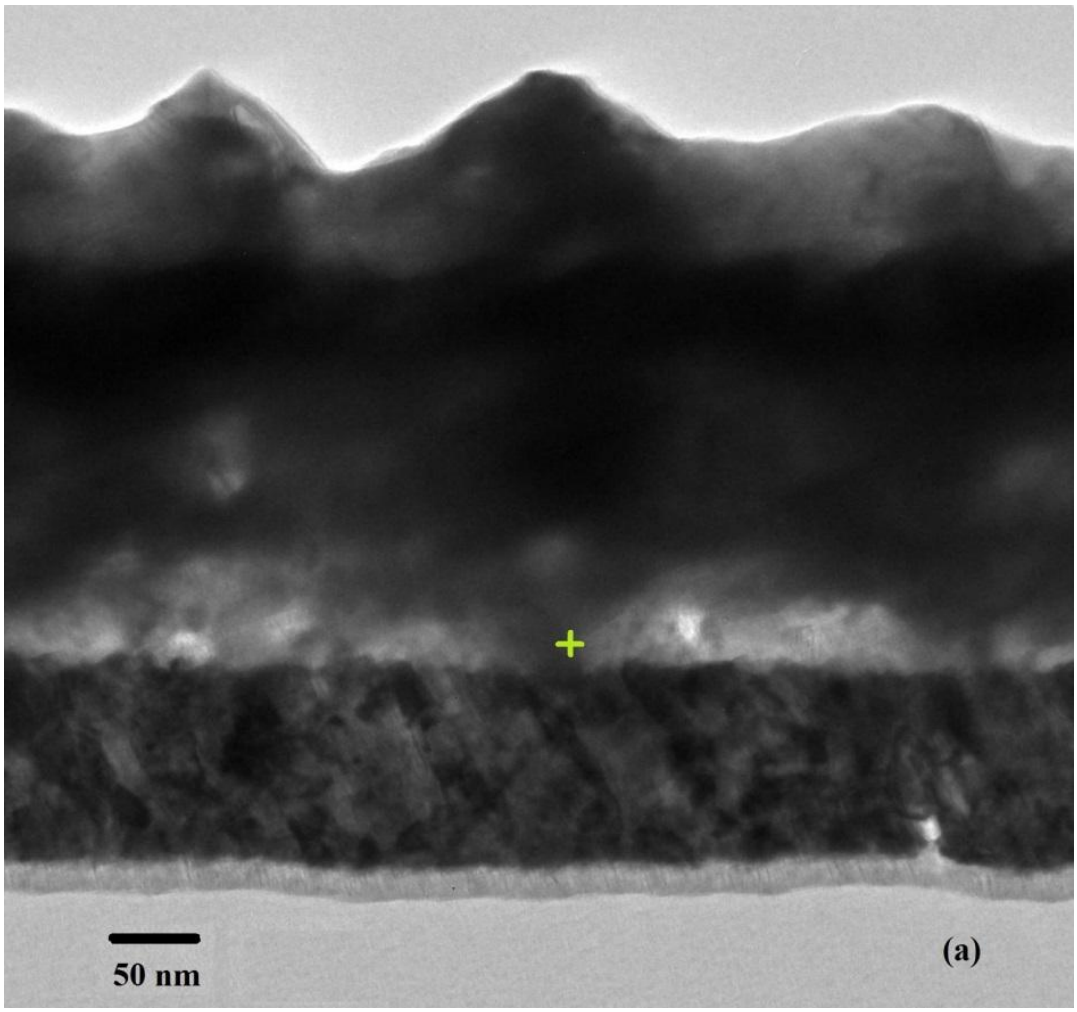
4.4. TEM Characteristics for Different Switching Modes

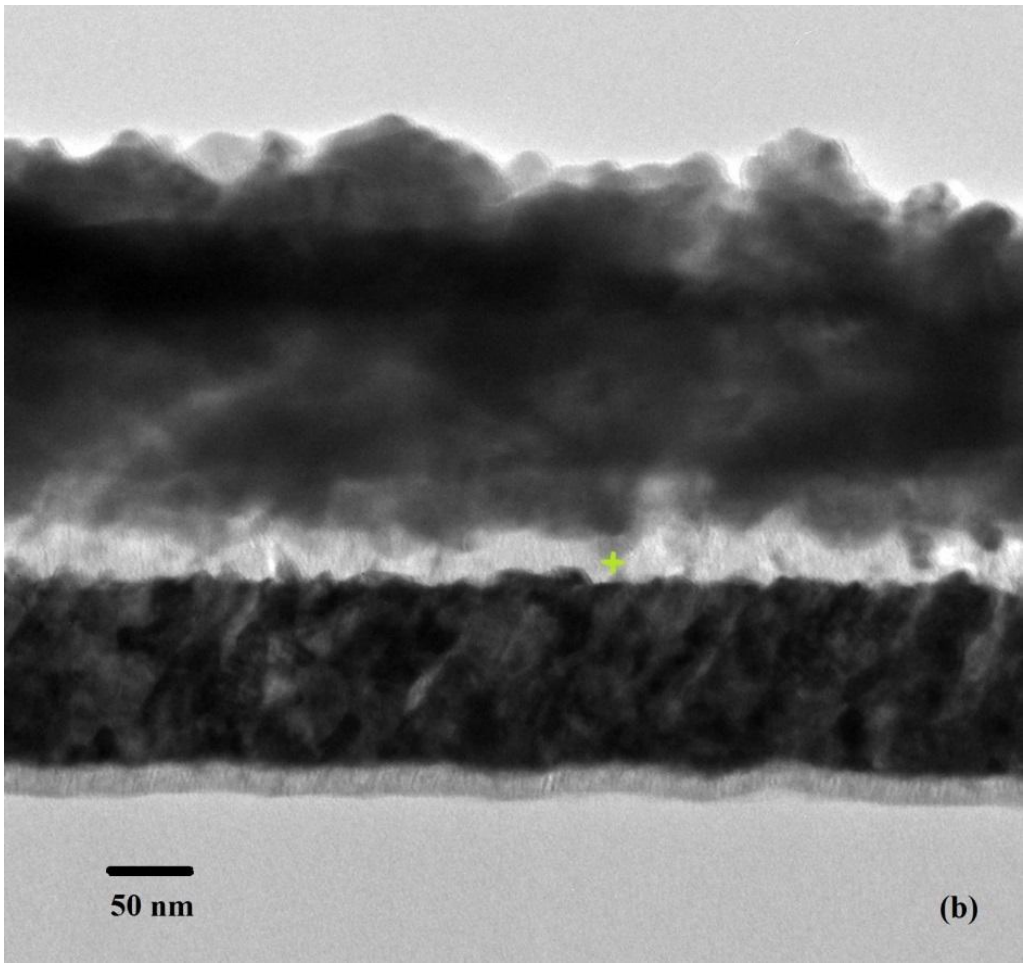
Shown in figure 4.6 are the TEM images of the volatile switching device and the memory switching device after SET process, then removing the external power. Fig. 4.6 (a) exhibits the sample after applying the compliance current of 1 mA. In the electrical testing, the device shows the memory switching behavior. As shown in the TEM, Ag penetrates through the NiZnO layer and into the MgO layer to form the filament. In comparison with the “fresh” sample without applying the compliance current in Fig. 4.1, it can be seen that the SET process from HRS to LRS in the resistive switching may result from the formation of the silver filaments connected between the top electrode and bottom electrode. As soon as the conductive path is formed, the current through the device could significantly increase, leading to the SET process, and the resistance state switching from the HRS to the LRS. [6] The resistive state could be switched back to HRS only when the RESET voltage is reached. Fig. 4.6 (b) shows the TEM image of the sample after applying the compliance current of 1 μA and behaves as the volatile switching. In compared with the memory switching device, Ag does migrate into NiZnO

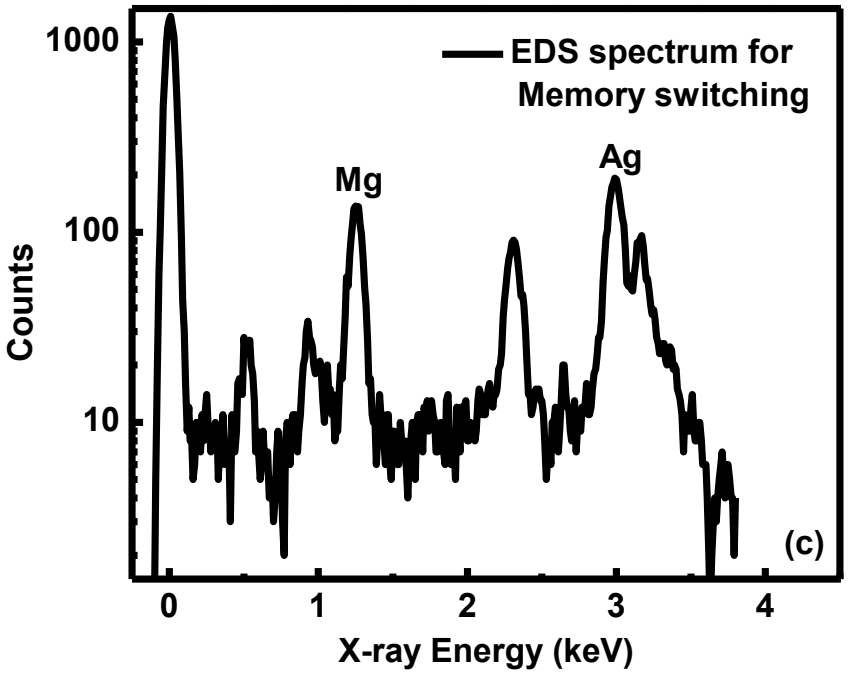
too; however, hardly into the MgO layer. In the TEM image, we could not observe the filament connected through the two electrodes. The low allowed current during SET increase the difficulty in migrating to the MgO layer. In this case, even if Ag could migrate to the MgO layer, it is difficult to keep the connected filaments when the power is off. This is in accord with the electrical testing results for volatile switching, in which the resistance state of the volatile device switches from LRS back to HRS when the power is off, and To analyze the composition of the filaments in these two switching modes, the simple EDS measurements are conducted on these samples. The comparison of the count ratios of silver to magnesium for different switching modes is presented in Fig. 4.6 (c) and 4.6 (d), respectively. In the MgO layer of the memory switching device, the Ag/Mg ratio is 1.29 while the ratio for volatile switching device is only 0.34. From the results of both TEM and EDS, one can clearly see the difference of the number and shape of the filaments between the two switching modes. It implies that after the SET process, Ag filament formed in the memory switching device is much stronger than that in the volatile switching devices.

Compliance current sets the maximum allowed current go through the device during SET process. When the large compliance current is set, there will be large current flows through the formed filament. Compared with the volatile switching, there are more and thicker filaments formed in the memory switching; therefore, the resistance of the filaments in the memory switching is small. When the power is off, the filament cannot be ruptured and it shows the non-volatile memory behavior. When the small compliance current is set, for the volatile switching, there will be small current flows through the Ag filament between the top and bottom electrode. From the IV characteristics, TEM and

EDS analysis, one can see that the filament in volatile switching is weak and the resistance of the filament is large. It is easily ruptured when the power is off. Thus, the compliance current affects the formations and ruptures of the conductive filaments, and finally determines the switching mode.




50 nm
(b)


1000
100
10
Counts
EDS spectrum for
Memory switching
Mg
Ag
(c)
0
1
2
3
4
X-ray Energy (keV)

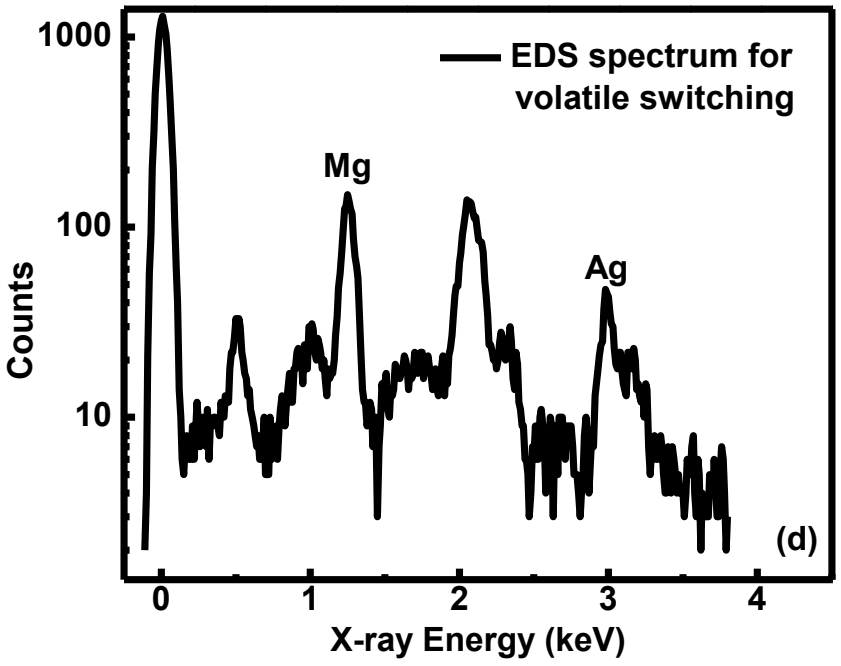

1000
100
10
Counts
EDS spectrum for
volatile switching
Mg
Ag
(d)
0
1
2
3
4
X-ray Energy (keV)

Figure 4.6 The TEM Characteristics of the memory switching (a) and volatile switching (b). The green marks indicated where the EDS data took for memory switching (c) and volatile switching (d).

4.5 Summary

In conclusion, three different types of switching modes have been investigated by different settings of the compliance currents. IV characteristics indicated that lower compliance current could lead to larger LRS and the conversion from the memory switching to volatile switching. TEM characteristics also proved that the compliance current could control the filament formation during the SET process, impact the filament status when the power is off, and finally affect the switching mode. The volatile switching mode paves the way for low power consumption and RESET-free memory application.

Chapter 5

Integration of ZnO-based Resistive Switching Devices

In the previous two chapters, we focused on single ZnO-based resistive switching device. From the previous discusion, it can be figured out that resistive random access memory (RRAM) is emerging as a promising nonvolatile memory (NVM) device. It has the potential advantages such as high density, fast speed and low power consumption. In order to fully use the advantage of high density, crossbar structure has been used for the memory architecture. However as mentioned in the Chapter 2, if the crossbar structures are totally made by the resistive switching devices, during the reading process there will be a parasitic current through the neighbor cells and the wrong readout signals are sent out. In this chapter we introduce a ZnO-based 1D1R structure, which is formed by a vertical integration of a FeZnO/MgO switching resistor (1R) and an Ag/MgZnO Schottky diode (1D). This 1D1R structure exhibits high R_{HRS}/R_{LRS} ratio, excellent rectifying characteristics, and robust retention. Flexible memory and 1T1R structure will also be discussed in this chapter.

5.1. 1D1R integration

5.1.1 ZnO-based Schottky diode:

In order to avoid the sneak current in the crossbar system, the diode is investigated for the integration of 1D1R structure. Based on the progress of the ZnO-based resistive switching devices, we investigated the ZnO-based Schottky diode for the 1D1R integration. The material of the diode and resistive switching device both are based

on ZnO, which could facilitate the fabrication process and optimize the integration process. [81]

With the consideration of barrier height and ideality factor in Fig. 5.1, it could be figured out that the Ag/ZnO could form the better Schottky diode. Ag oxidizes easily into AgO_x during the contact formation, producing a high barrier height. [82] It was also observed that that the thermal stability of Ag Schottky contacts was better than that of Au or other metal Schottky contacts. [83] It is well known that in the fabrication process of Schottky contacts, the surface states, contaminants and defects affect the barrier height and leakage current. Oxygen plasma was used to clean the surface before the metallization process in order to minimize such effects.[84] Coppa *et al* [85] also mentioned that plasma cleaning resulted in highly ordered, stoichiometric, and smooth surfaces of ZnO and significant improvement in the IV diode characteristics. The bonding energy of Mg-O (393.7 kJ/mole) is much higher than that of Zn-O (284.1 kJ/mol), therefore Mg-doped ZnO contains less oxygen vacancies than ZnO, resulting in the low leakage current in the Schottky diode; furthermore, MgZnO possesses better thermal stability than the pure ZnO [86]. It is also reported that the formation of zinc vacancies becomes lower after doping, which can compensate the donors and reduces the leakage in the zinc-rich growth condition [87].

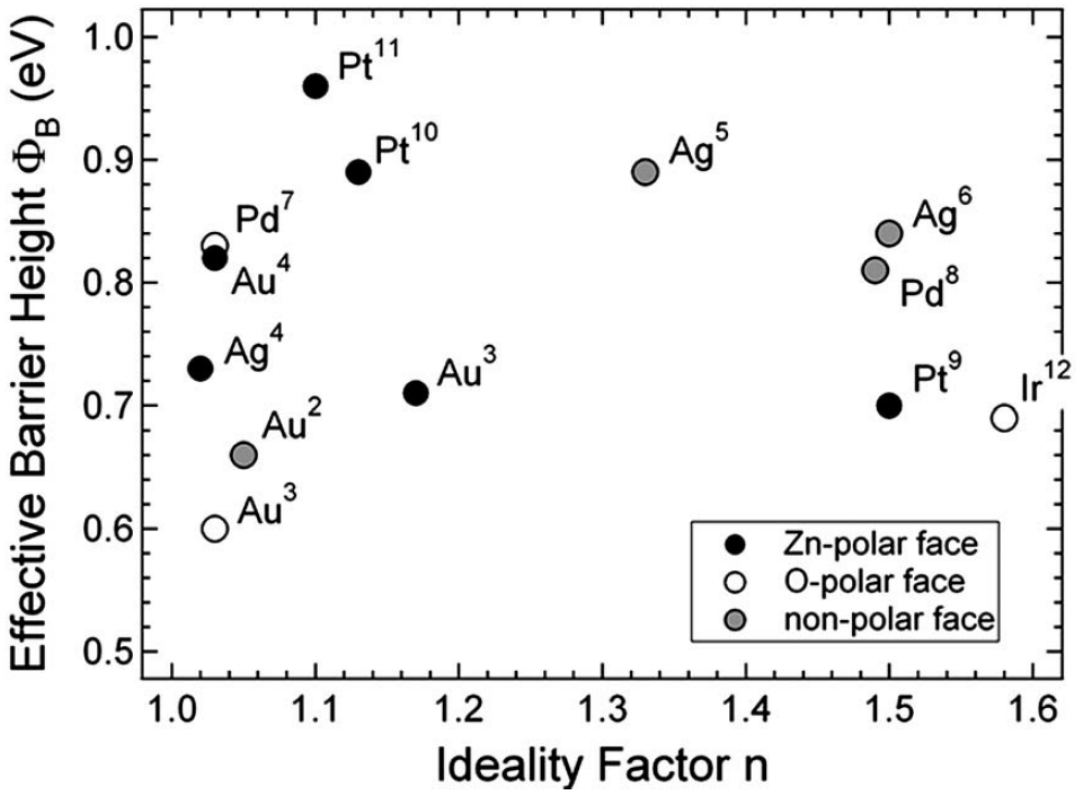


Figure 5.1 Effective barrier height vs ideality factor n for the best reported Schottky contacts on n-type ZnO with different metal. [47]

In the work, the Mg doping concentration in the ZnO is investigated and presented in figure 5.2. When the Mg concentration increases, forward and reverse current decrease. This may result from that the Mg doping could suppress the oxygen vacancies in the ZnO. The maximum ratio of forward current/reverse current exists when Mg = 6%. If the Mg doping increases from 6% to 10%, the forward current decreases to 10% of previous value. This may result from the alloying disorder and relatively bad crystal quality in the higher Mg concentration.

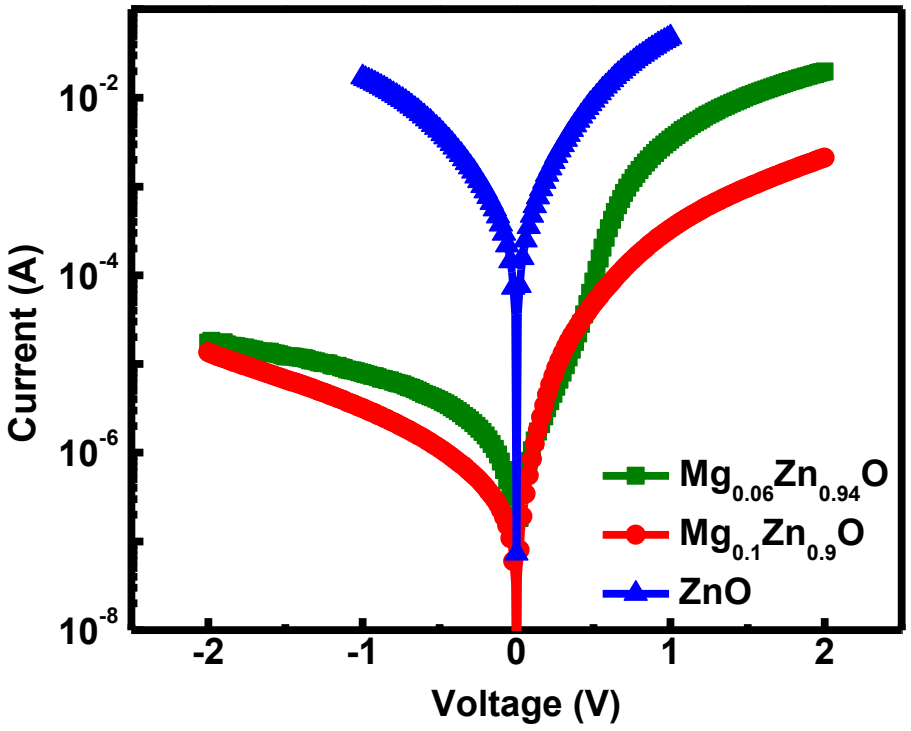


Figure 5.2 The IV characteristics of the ZnO-based Schottky diode with different Mg doping.

The Top Electrode of the unipolar resistive switching device is gold. To vertically integrate the diode with the memory devices, we need to use the Au TE of memory as the BE of the diode. In order to improve the ohmic contact performance of the Au/MgZnO, we compared the performance of the Au/Al/ZnO/MgZnO/Ag and Au/GaZnO/MgZnO/Ag structure. It is shown in figure 5.3 that these two structures have the similar ON/OFF ratio, however, when considering the performance of the memory (current in the LRS), we chose the Au/GaZnO/MgZnO/Ag structure for further integration.

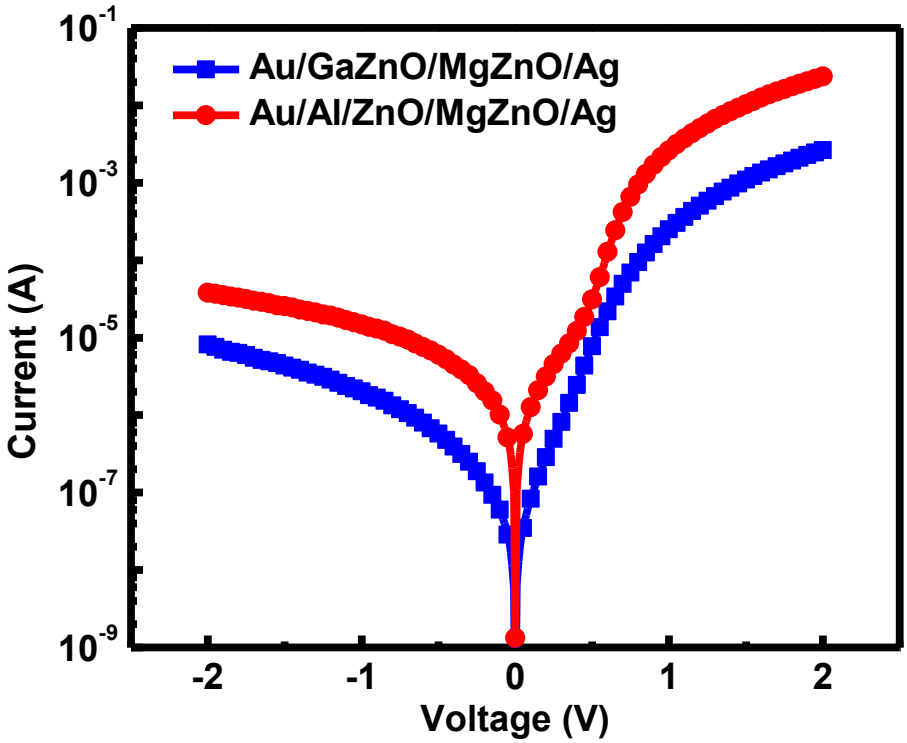


Figure 5.3 The IV characteristics of the ZnO-based Schottky diode with different ohmic contact.

However in this structure, the Ga doping may diffuse into the MgZnO layer and deteriorate the reverse performance of the diode. We tried different thickness of the MgZnO layer to minimize the effect of the Ga doping, and the result is shown in figure 5.4. It is indicated that the 350nm of MgZnO is better than the thickness of 230 nm, and the optimized Schottky diode (Ag/350nm $Mg_{0.06}Zn_{0.94}O_x$ /GaZnO/Au) has the best performance with the forward/reverse current ratio at ±1V is 2.4×10^7. In the future work, CV and IVT character methods should be conducted for the barrier height and ideal factor of the MgZnO based Schottky diode.

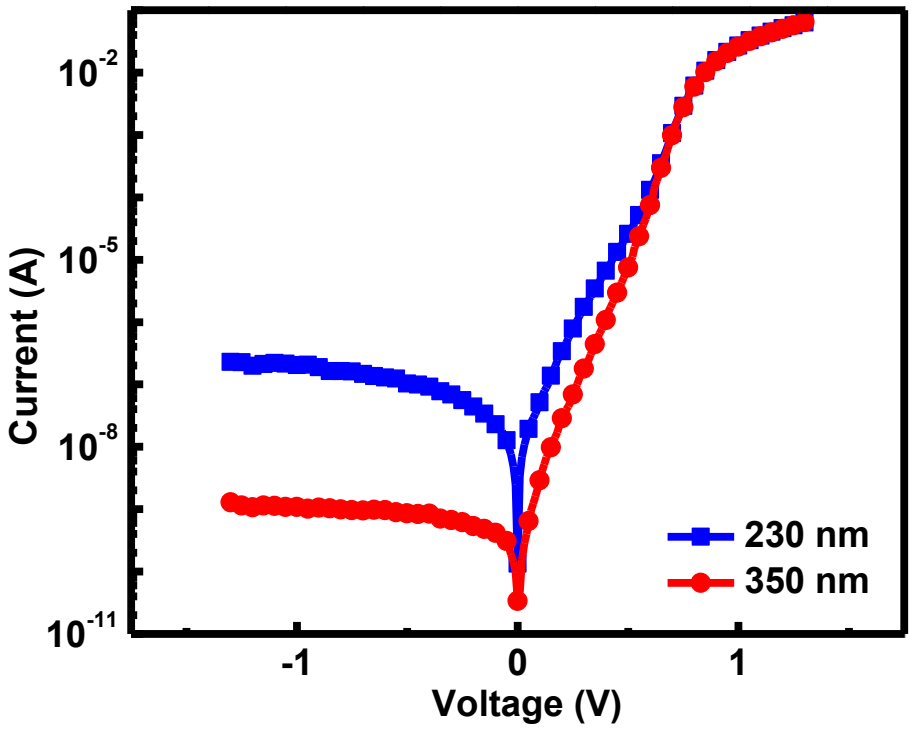


Figure 5.4 The IV characteristics of the ZnO-based Schottky diode with different MgZnO thickness.

5.1.2 Vertical integration

The ZnO-based 1D1R component, consisting of a Au/FeZnO/MgO/Pt structure as a unipolar switching resistor and a Ag/MgZnO/GaZnO/Au structure as a Schottky diode, is shown in figure 5.5. The vertical structure is chosen as it is preferred for 3-dimensional (3-D) integration. Pt was used as a bottom electrode for the resistor. To improve adhesion, 5 nm of Ti was deposited first on SiO_2, followed by a 100 nm of Pt deposited using e-beam evaporation. MgO (5 nm) and $Fe_{0.04}Zn_{0.96}O_x$ (70 nm) layers were deposited

on Pt by metal-organic chemical vapor deposition (MOCVD). Au was deposited and patterned as the top electrode of the switching resistor and also as the bottom electrode for the diode. A Ga-doped ZnO (GZO) thin layer (10-nm) was deposited on top of the Au layer to serve as the n^+ layer to achieve the ohmic contact. Then $Mg_{0.06}Zn_{0.94}O_x$ (350 nm) was deposited by MOCVD, and a Au/Ag layer formed the Schottky contact onto it. The diameters of the top and bottom electrodes of the diode are 40 and 60 μm, respectively. A Zeiss Leo Field Emission scanning electron microscopy (FESEM) was used to inspect the surface morphology and layer structures. The I-V characterization was conducted with an Agilent 4156C semiconductor parameters analyzer in the voltage sweeping mode.

We consider ZnO for "1R" in the 1D1R structure mainly due to its advantages: (i) multi-functionality, (ii) easy to grow nanostructures, and (iii) active devices like diodes and transistors are available for integration for real applications. However, in comparison with other metal oxides (including Ta-, Hf- oxides, etc) - based RRAM, ZnO has a smaller energy band gap. Actually, ZnO is a wide band gap semiconductor and it usually shows n-type semiconducting behavior due to existence of various point defects and impurities during the synthesis, while the other oxides listed above belong to insulators. So far, the ZnO-based RRAM results show relatively high current density comparing with these oxides. In fact, TiO_2 has the similar band gap to ZnO, and it is interesting to see that many TiO_x-based RRAMs also show relatively high current density. Reducing the n-type conductivity in ZnO needs heavy compensation doping using Li, Ni, or Cu, etc. In our case, the $Fe_{0.04}Zn_{0.96}O_x$ has higher resistivity than ZnO because Fe is the deep level dopant; however, its resistivity is still much lower than the other metal oxides mentioned above. Ta- and Hf- oxides have been used for high-K dielectrics. The material

properties of these ultra-thin films have been well studied and controlled. In comparison, the various growth technologies of ZnO-based materials are still less mature. It will be the key to further understand and control the doping and defects in order to fully develop the ZnO - based RRAM technology. This will be particularly important for RRAM, in which the devices are in the nano-scale, and defects will play the critical role for the resistive switching, as briefly discussed in the work.

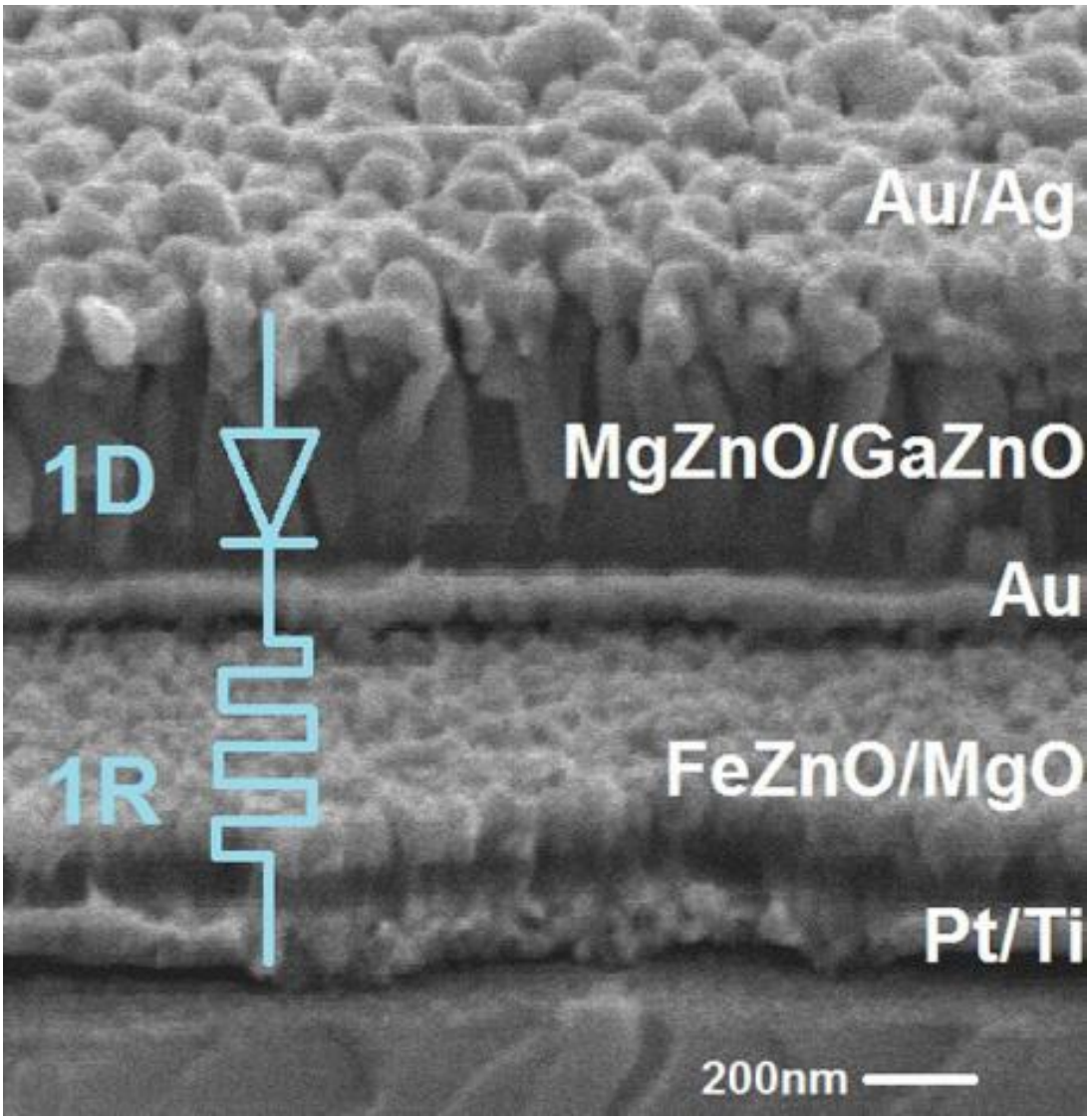


Figure 5.5 A SEM image of a vertically integrated ZnO-based 1D1R structure.

The layer structure of the vertical Schottky diode is Ag/MgZnO/GaZnO/Au. It contains two different types of M-S contacts.

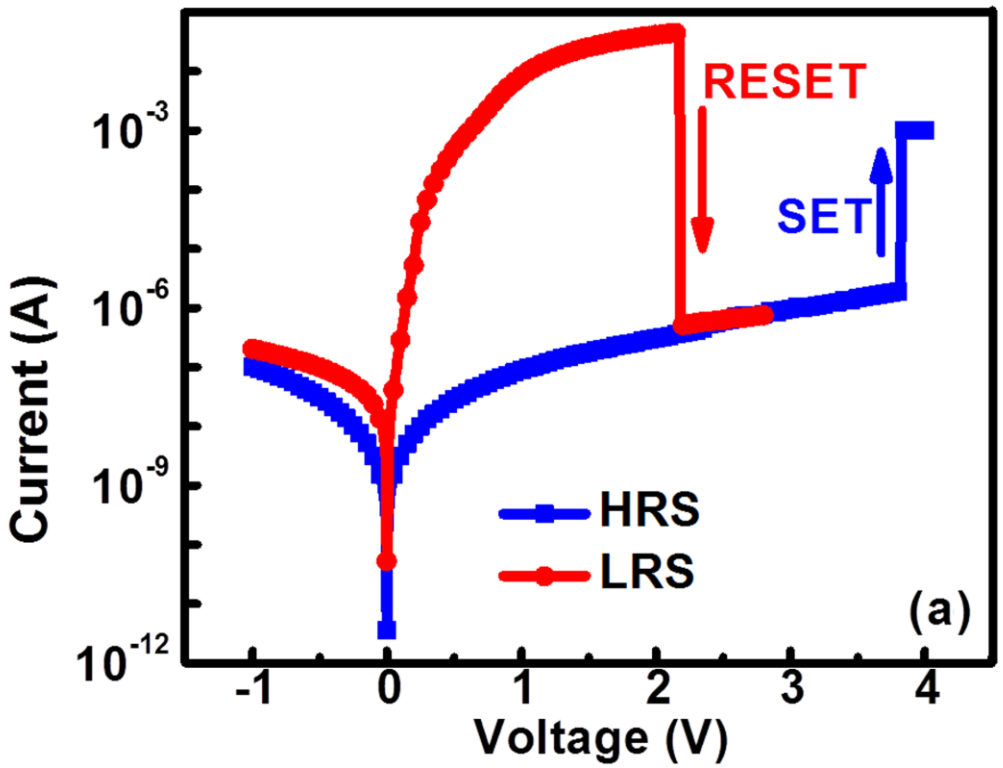
In the integrated 1D1R structure, Au is the common electrode which serves as the top electrode for the switching resistor (R) and also as the bottom electrode to form the ohmic contact for the Scottky diode (D). Generally Au is not a good choice for the ohmic contact in the discrete ZnO diode due to its high work function value. In order to form the ohmic contact between Au and ZnO, the field emission (FE), i.e. tunneling mechanism should dominate the current transportation. In this work, a highly Ga-doped ZnO (GZO) thin layer is deposited on the Au to serve as the n^+ GaZnO layer to realize the ohmic contact in the n^- MgZnO/n^+ GaZnO/Au structure.

It is well known in the ZnO research society that Ag forms good Schottky contact to ZnO. The low work function metals, such as In, Al and Ti, yield low Φ_{SB}'s with the exception of Ag. Ag oxidizes easily, producing high barrier heights that depend on the degree of oxidation. In the current work, we also have found that Ag forms better Schottky contacts with MgZnO in comparison to Pt, Au and other metal schemes. We chose the MgZnO instead of ZnO as the semiconductor material to form the Schottky diode. We have found that the Mg-doped ZnO (MgZnO) contains less oxygen vacancies, leading to the low leakage current in the Schottky diode. Furthermore, $Mg_xZn_{1-x}O$ (x~ 6%) possesses better thermal stability than the pure ZnO.

5.1.3 1D1R Testing Results

Figure 5.6 (a) presents the 1D1R characteristics from -1 V to 4 V, in which bistable resistive switching is observed under the forward bias; at the same time the current is suppressed under the reverse bias. The R_{HRS}/R_{LRS} ratio at 1V is 9.4×10^4, and the RESET and SET voltage regions of the 1D1R are 1.53 V to 2.98 V and 3.64 V to 7.21 V, respectively. The forward/reverse current ratio of LRS in the 1D1R structure at ±1 V is 4.1×10^4, which clearly shows the rectifying behavior of the 1D1R structure under reverse bias. The retention time of the 1D1R structure is also more than 10^7 s. In comparison with the single 1R device, both the SET and RESET voltages in the 1D1R device increase slightly due to the contribution of the resistance of the diode. The large ratios of the R_{HRS}/R_{LRS} and forward/reverse current with high endurance performance shown in the figure 5.6 (b) demonstrate that the vertically integrated ZnO 1D1R structure is promising for memory control without the fake switching and crosstalk that commonly occur in the 1R-only crossbar array.

We attribute the current differences between the single diode and the integrated diode to the morphology change of the bottom electrode of the diodes: the diode directly grown on the Au/glass has smoother bottom and top electrodes than the vertically integrated diode (the later one built on the memory resistor which has nanostructure and relatively rough surface). It is known that the M-S interface properties (including the roughness which relates the effective junction area) would significantly impact on the Schottky diode characteristics.


RESET
SET
HRS
LRS
(a)
Current (A)
Voltage (V)
10^-3
10^-6
10^-9
10^-12
-1
0
1
2
3
4

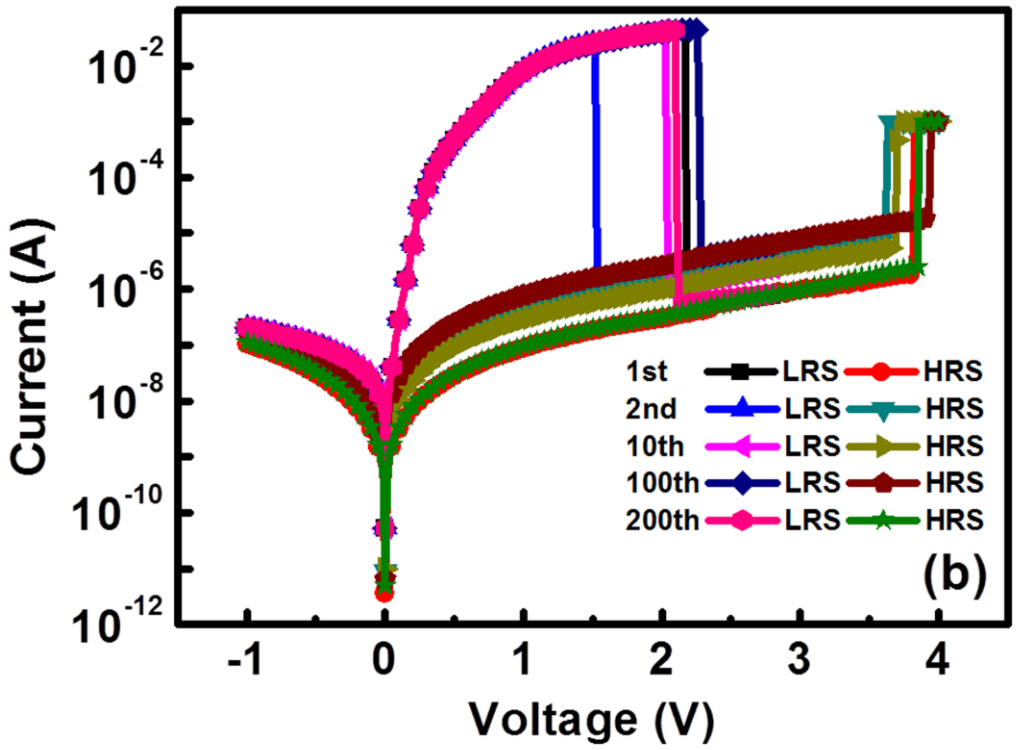

1st LRS HRS
2nd LRS HRS
10th LRS HRS
100th LRS HRS
200th LRS HRS
(b)
Current (A)
Voltage (V)
10^-2
10^-4
10^-6
10^-8
10^-10
10^-12
-1
0
1
2
3
4

Figure 5.6. I-V characteristics of (a) the vertically integrated ZnO-based 1D1R, and (b) the endurance performance of the 1D1R structure within 200 cycles.

To show the details of diode behavior in the 1D1R structure, both I-V characteristics of 1D1R and 1R-only in LRS are redrawn in the linear scale, as shown in figure 5.7. The insert image presents the schematic circuit model of the 1D1R structure, where the MgZnO Schottky diode under the forward biasing is represented by the Piece-Wise Linear (PWL) Diode model (it is also called "battery-plus-resistance" model), containing three components in series: an ideal diode, a "battery" (cut-in voltage: V_{D0}), and a dynamic resistor (r_D). When the switching resistor in the 1D1R is in LRS, the diode is in the series connection with a small resistance Rl of the switching resistor; however, when the switching resistor in the 1D1R is in HRS, the diode is in series with a large resistance Rh. Compared with the 1R-only device, the I-V characteristics of 1D1R shift ΔV (~0.7 V) which is equal to V_{D0}, the cut-in voltage of the diode. There is a slope difference of the linear region between the two I-V curves: for 1R-only device, the slope is equal to R^{-1}, while for 1D1R the slope is equal to $(r_D + R_l)$-1. This resistance difference (~9 Ω) is primarily due to the contribution of the diode. When "1R" is in HRS, the small diode resistance r_D (~ 9Ω) is in series with a large memory resistance R_h (~ $1.6\times10^7\Omega$), the current flowing through the 1D1R structure is predominantly controlled by the "1R". Therefore, the diode behavior looks "disappeared". Actually after RESET, the switching resistor operates in the HRS, then the diode in series with "1R" with large resistance looks "disappear". The resistive state stays in the HRS until the bias reaches to the SET

voltage, then the device switches to the LRS again and the diode behavior of the 1D1R structure can be seen again. It should also pointed out that in the 1D1R cell based crossbar array, the reading voltage will be arranged at 1V, which is far away from the RESET/SET voltage of 2.2V and 3.9V.

To further clarify the issue, we are compiling the I-V characteristics of 1D1R structures reported by other groups to support our results and analysis. From these figures and comparisons, one can make the conclusions:

(1) The I-V characteristics for all of the four 1D1R structures have similar HRS and LRS characteristics. In the ITO/TiO_2/Pt structure, the resistive ratio at 0.6 V is about 100. The SET and RESET voltage is about 2V and 4V, respectively. [49] In the Pt/TiO_x/Pt structure, the resistive ratio at 1V is around 100. The SET and RESET voltage is also about 2V and 4V, respectively. [48] In CuO/InZnO structure, the resistive ratio at 0.6 V is about 10^3. The SET and RESET voltage is about 3V and 5V, respectively. [46] In our device of the work, the HRS/LRS ratio at the reading voltage of 1V is 9.4×10^4 at 1V and the SET and reset is 2.2V and 3.9V, respectively.

(2) All of the four I-V characteristics for LRS exhibit the similar diode behaviors. In *Ref. 49*, the forward/reverse current ratio was as high as 1.6×10^4 at ±1V. In *Ref. 48*, the forward/reverse current ratio was 10^3 at ±1V. In *Ref. 46*, the forward/reverse current ratio was as high as 10^4 at ±2V. In our device of the work, the forward/reverse current ratio is 4.1×10^4 at ±1V.

(3) Through comparison of above 1D1R structures, it can be found out that our structure not only is the first fully ZnO-based 1D1R structure with a bi-layer to control the electrical parameter of the switching resistor and diode, but also has the highest

HRS/LRS ratio, the highest forward/reverse current ratio, and relatively low operation voltage.

In summary, we have clarified the diode behaviors in the 1D1R structure by providing both experimental results and modeling analysis. The characteristics of the 1D1R structures reported by other groups also support our analysis here. Furthermore, by comparing with these recent publications, it is clear that our work has presented the uniquely integrated ZnO-based1D1R structure with the excellent performances.

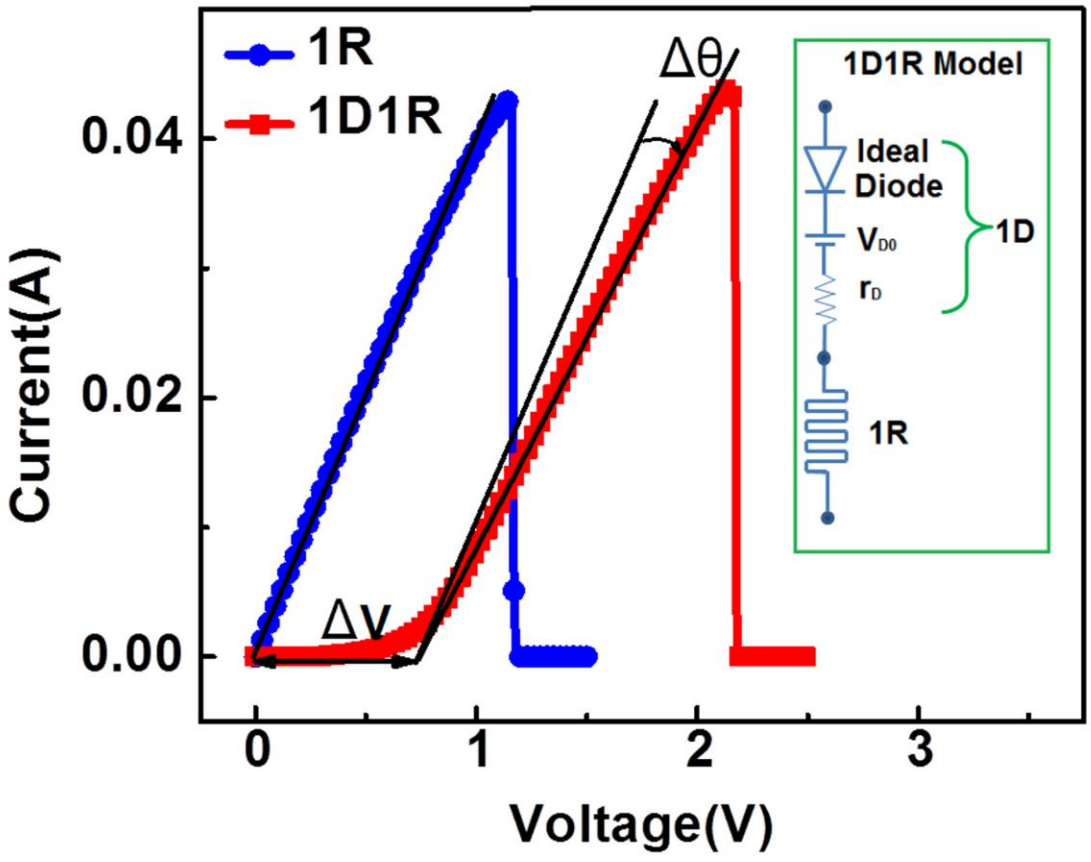


Figure 5.7 I-V characteristics of the 1R-only and the 1D1R under LRS are presented in the linear scale. Their I-V curves show two major differences: voltage shift of ΔV and slope change of Δθ. The insert image shows the schematic circuit

model of the 1D1R where a switching resistor is in series with the diode presented by the PWL model.

5.2 Control compliance current for 1T1R integration

In order to avoid the passive array in the crossbar memory system, bipolar resistive switching device is integrated with ZnO-based Thin Film Transistor, and the TFT is fabricated by colleagues in our group. [70] Figure 5.8 shows the I_{DS}-V_{GS} characteristics in saturation regions for ZnO TFT. The extracted threshold voltage (V_{th}) is 2.1V, respectively. It shows high on-off ratios (>10^9) with the on-current for I_{DS} to be as large as 10^{-3} A, which is close to the requirement for our ZnO-based RS device for further integration.

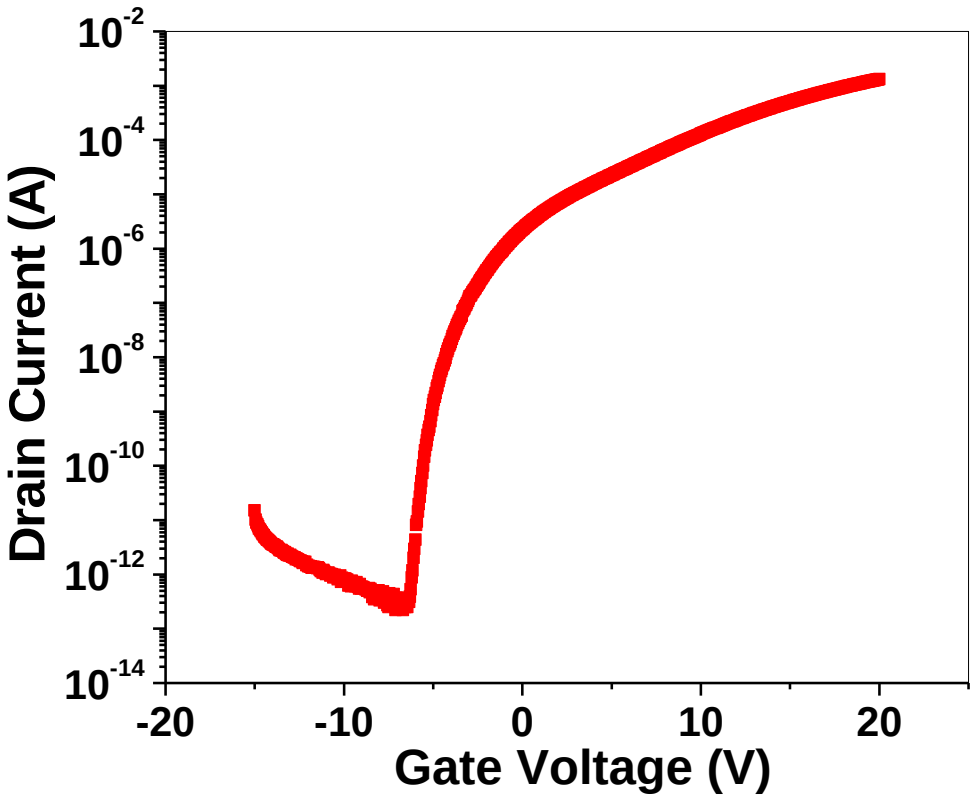


Figure 5.8 I_{DS}-V_{GS} transfer characteristics of ZnO TFT in the saturation region.

To meet the requirement of the 1T1R integration, compliance current is applied to reduce the current in LRS. For example, in the FeZnO-based bipolar switching resistor described above, if the compliance current limitation for the SET step is changed from 10 mA to 150 μA, the current in LRS is reduced by almost 2 orders (from 1.1×10^{-2} A to 1.6×10^{-4} A), which is suitable for the further integration with TFT; however the R_{HRS}/R_{LRS} ratio would be simultaneously reduced from 9.9×10^{5} to 1.2×10^{2}. In our case, the variation of the compliance current for the SET process controls the formation of the conductive filaments through the FeZnO/MgO layer. When the compliance current is

reduced, a smaller SET current could only introduce the filaments which are weaker and less conductive than that formed under large compliance current setting. The lower compliance current increases the resistance of the LRS and decreases the maximum allowed current density of the device. Therefore, different settings of the compliance current limitations for this type of resistive switching devices could satisfy different memory preferences, such as high R_{HRS}/R_{LRS} ratio for high yield ratio, or low current in LRS for the integration.

5.4. Summary

In summary, a vertically integrated ZnO-based 1D1R switching device consisting of a FeZnO/MgO unipolar switching resistor and a MgZnO Schottky diode is demonstrated. Different structures for the vertical ZnO Schottky diode have been studied. The overall R_{HRS}/R_{LRS} ratio of the 1D1R structure at 1 V is ~10^5, the forward/reverse current ratio at ±1 V is 4.1×10^4, and the retention time is over 10^7 s. The conduction mechanisms of the HRS and LRS are Poole–Frenkel emission and resistive conduction, respectively. This device is promising as the basic circuit building block of the crossbar arrays for applications in reconfigurable electronics and nonvolatile memory.

Chapter 6

Conclusions and Suggestions for Future Work

6.1. Conclusions

ZnO-based resistive switching devices including both bipolar and unipolar RS devices are demonstrated. By using the FeZnO/MgO bilayer (BL) oxide structure, switching performances including the R_{HRS}/R_{LRS} ratio and the switching stability are significantly improved in comparison with that of the FeZnO single layer (SL) oxide structure. The BL structure has the similar R_{LRS}; however, its R_{HRS} increases by 10^3 over the SL counterpart, and the overall R_{HRS}/R_{LRS} ratio of 10^6 is achieved. These improvements are desired to the RRAM application, where a large R_{HRS}/R_{LRS} ratio could prevent false reading signals while the narrow distribution of V_{SET} and R_{HRS} would confine the writing voltage and reading signal range. Curve fitting revealed that the conduction mechanisms in HRS and LRS are Poole-Frenkel emission and Ohmic behavior, respectively. The resistive switching is attributed to the formation and rupture of the filament, which involves by oxygen vacancies, oxygen ions, or metal ions. Room temperature process could be used for Ni-doped ZnO RS device on flexible substrate.

Preliminary comparisons between the unipolar and bipolar resistive switching have been analyzed and discussed. Applied with different thickness, electrode and compliance current, the varied IV characteristics support the basic hypothesis for the mechanism of the resistive switching. We designed and controlled the RS polarities using appropriate electrodes and critical thickness of the oxide layers. The switching modes (memory/volatile/threshold) are successfully converted by controlling the compliance

current level. IV characteristics indicated that lower compliance current could lead larger LRS and the conversion from the memory switching to volatile switching. TEM characteristics also prove that the compliance current could control the filament formation during the SET process, impact the filament status when the power is off, and finally affect the switching mode.

The 1D1R integration is studied based on the performance of unipolar and bipolar RS devices. The MgZnO-based Schottky diode is optimized with an ON/OFF ratio of 2.4×10^7. A vertically integrated ZnO-based 1D1R unit cell consisting of a FeZnO/MgO unipolar switching resistor and an Ag/MgZnO Schottky diode has been demonstrated. The MgZnO-based Schottky diode is optimized with an ON/OFF ratio of 2.4×10^7. For the 1D1R, its overall R_{HRS}/R_{LRS} ratio at 1V is $\sim10^5$, the forward/reverse current ratio at $\pm$1V is 4.1×10^4, and the retention time is over 10^7 s. This novel 1D1R component is promising as the basic circuit building block of the crossbar arrays for applications in reconfigurable electronics and nonvolatile memory. Compliance current will be applied to control the current in LRS for the requirement of the ZnO-based 1T1R integrations.

6.2. Suggestions for Future Work

Even with the extensive research that has been done in ZnO-based resistive switching, the field is still in its early stages. To be in the mature stage of development, the parameter of switching device could be optimized. Moreover, more studies have to be made for the fully integration application. The following new generation of ZnO resistive switching devices and platforms should be studied:

- **Integration for the resistive switching devices:** The single resistive switching could only be part of the memory switching. The unipolar passive of the resistive switching could integrate with diode for switching matrix and the active bipolar resistive switching device could be combined with the ZnO thin film transistor for further nonvolatile memory application. With the basic of the Schottky diode, the Schottky contact based MESFET could also been studied for application. In the further work, the n×n basic 1D1R array should be fabricated to fully demonstrate the advantage of the 1D1R integration. Compared the n×n 1D1R array to n×n 1R-only array, the avoided sneak current in the 1D1R array could prove the accurate readout signals for crossbar structures.
- **Mechanism study for the resistive switching:** In this dissertation, we have used modes conversion to clarify the reason for the resistive switching. In order to totally understand the mechanism, in-situ characteristics need to be used for checking the switching devices. Universal model study for resistive switching is also necessary for further device performance improvement.
- **Further study for flexible memory:** In this dissertation, we demonstrated the fundamental resistive switching results for flexible memory. According to the requirement of the wearable device and novel display, the flexible memory with bio sensor would be a new application for future human life.

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