Magnesium Zinc Oxide High Voltage Thin Film Transistors

By

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ABSTRACT OF THE DISSERTATION

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Dissertation Director:
Prof. Yicheng Lu

Energy is one of the most important topics in the 21st century, and solar energy has been a leading technology in the search to replace fossil-fuel energy as a sustainable and clean energy source. In order to provide an energy-efficient, less expensive, and reliable energy source, the PV system on glass (PV SOG) is emerging as an attractive concept. It integrates solar cells, solar inverters, and controller circuits on a single glass substrate.

This dissertation focuses on development of the novel oxide-based high voltage thin film transistor (HVTFT) on glass technology, which is one of the core devices for solar inverter of the PV-SOG. Currently, the inverter counts for more than 10% of the total cost of an entire PV system. The solar inverter will be the major challenge of PV-SOG because the conventional solar inverters are bulky and could not be directly built on glass substrates. In particular, its key device, high voltage transistor, is not only pricy but also requires high process temperature which is incompatible with glass substrates.

In comparison of several semiconductor materials, such as polycrystalline silicon, amorphous silicon, SiC and GaN, ZnO based materials have several

promising features suitable for HVTFT on glass technology, including wide bandgap, high thermal conductivity, high mobility, and low deposition temperature. However, the thin film transistor (TFT) made up of the pure ZnO generally suffers from poor stability and reliability due to high defect density in the material. Because energy source is a basic unit of the infrastructure, it's critical for a solar energy system to have a long lifespan. The first important issue of this dissertation research was to improve the TFT stability by adding a small amount of Mg into ZnO to form the ternary oxide, $Mg_XZn_{1-X}O$ (MZO, X<0.03) as the TFT channel. The density of oxygen vacancies in MZO was reduced so that after negative bias stress (NBS) the threshold voltage shift of MZO TFT was 30% smaller in comparison with the shift of ZnO TFT counterpart.

Based on the solid foundation of stable MZO TFTs, MZO high voltage TFT (MZO HVTFT) on glass technology was designed and developed. To eliminate the electrical field crowding around the corners of the conventional TFT with a rectangular channel, a symmetric circular-shape transistor was adapted. From the simulation result, the peak electrical field is reduced by 50% in the symmetric circular structure than in the conventional rectangular structure. However, the MZO HVTFT with the circular configuration only showed a blocking voltage of 92V. To further enhance the device performances, especially the blocking voltage, we developed a modified MZO (m-MZO) HVTFT, which had an ultrathin MZO transition layer (MZO-TL) using the in-situ modulation doping in the channel-dielectric interface. The comprehensive characterizations using X-ray photoelectron spectroscopy (XPS) and energy-dispersive X-ray spectroscopy

(EDS) were conducted to study depth profiles of elements across the channel-gate dielectric interface. It was proved that this interface engineering effectively suppressed the interdiffusion of Zn and Si between the channel and dielectric layers, resulted in the reduction of the interface states and the oxide trapped charges. The combination of the interface engineering with the symmetric device design significantly increased the blocking voltage of the m-MZO HVTFT on glass. As a result, the regular m-MZO HVTFT (channel length=10μm) has on/off ratio of 3.5×10^{10} and blocking voltage of 305V, which is suitable for the regular AC 110V power system. The m-MZO HVTFT with a channel length=25μm has on/off ratio of 3.3×10^{9} and blocking voltage of 609V which is suitable for the regular AC 220V power system.

Finally, in order to expand the HVTFT technology from glass to the flexible substrate, the ZnO-based HVTFTs on plastic substrate were explored. By adopting low temperature even room temperature process, such as sputtering and atomic layer deposition, the flexible HVTFT consisting of the ZnO based channel with Al_2O_3 dielectric layer showed an on/off current ratio of 10^{9} and blocking voltage of 92V.

The MZO HVTFT technology opens opportunities for cost-effective and highly efficient power management systems for many applications. The HVTFTs on glass will serve for the inverter in novel Building-integrated photovoltaics (BIPV) and smart glass while the flexible HVTFT is promising for the emerging self-powered wearable systems.

Dedication

To my family and mentor

Chien-Yu Lin, who always loves me unconditionally, takes care of me and gives me strength.

Professor Yicheng Lu, who teaches me the true importance of life and research.

Chin-Kuo Hong and Hsiu-Chen Chen, who raised me and support the pursuit of my dream.

Yi-Ting Wu and Shih-Kuei Lin, who give my family unreserved support and love.

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I also would like to thank my dissertation committee members, Prof. Jaeseok Jeon, Prof. Mehdi Javanmard, and Prof. Ming Lu for spending their valuable time to review my dissertation. Their profound questions and suggestions improved my understanding of the topics and helped to promote the improvement of my dissertation.

It's my honor to have had the chance to work with colleagues in Prof. Lu's research group, who have provided indispensable help to further my work. Dr. Chieh-Jen Ku gave me comprehensive training in device fabrication and set a solid foundation for my dissertation. Dr. Pavel Reyes guided me through writing papers, making proposals, and reviewing scientific articles. Dr. Rui Li gave professional and limitless support of material growth and analysis. My thanks also go to all other members: Dr. Ziqing Duan, Dr. Yang Zhang, Mr. Tengfei Xu, Mr. Tanvir Mohsin, Mr. Keyang Yang, Ms. Szu-Ying Wang, Ms. Ke Tang, Mr. Guangyuan Li, Mr. Yuxuan Li, Mr. Hongfei Ye, Ms. Navila Alim, and other visiting scholars and students. Their great assistance in the research as well as their friendship gave

me the momentum and courage to solve difficulties in both scientific work and daily life. A special thank has to be given to Mr. Robert Lorber, our guardian of the cleanroom. Your talented mechanical skills keep our tools running. It has been an unforgettable experience to work with you and Dr. Pavel Reyes to manage the laboratory.

My friends have given me great backing in my life. Ms. Carol Blumenthal, Dr. Jeremy Sykes, and Mrs. Tari Lee Sykes have always been there for my family and me. Your support helped us to stand on our own feet in the United States, and your wise advice guided us through the seemingly hopeless days. I really appreciate your great care and generous support.

Above all, I would like to thank my family. My wife, Chien-Yu Lin, always supports me unconditionally, encourages me consistently, and loves me unreservedly. My parents, Chin-Kuo Hong and Hsiu-Chen Chen, always give me great freedom and support in my path to explore my passion. My parents-in-law, Yi-Ting Wu and Shih-Kuei Lin, always gives my wife, my children, and me the greatest love and care.

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Chapter 1   Introduction

1.1. Motivation

For decades, solar energy has been a leading technology in searching to replace fossil-fuel energy as a sustainable and clean energy source. However, cost and efficiency remain as major concerns.[1] As the price of photovoltaics (PV) modules has been dropping, the inverters for energy converters now count for more than 10% of the total cost of an entire PV system[2]. Additionally, in a conventional PV system all PV modules link to a central inverter; therefore, the overall system performance can be brought down by an underperforming module in the array or individual solar cells blocked from sunlight.

To solve these problems, and to optimize each individual solar module, the micro inverter technology[3] has been proposed to embed inverters into each photovoltaic module. However, at the present time, the cost of micro inverters is still higher than that of centralized inverters in small systems (≤10 kW)[4]. Another major factor hindering the wide adoption of solar energy is a conflict between aesthetics and energy saving. Many consumers find the placement of solar arrays on buildings to be unsightly. Consequently, the technologies of integrating photovoltaics into buildings, i.e. Building Integrated Photovoltaics (BIPV) have been proposed[5,6]. BIPVs serve as building elements so that the appearance of houses won't be compromised due to the post-installation of solar panels.

To address these three major issues, i.e. efficiency, cost and appearance, we have explored a new type of solar inverter which can be integrated with PV

modules to form a solar PV system on glass (PV-SOG). PV-SOG has three major advantages: suitable for mass production of an integrated system, occupying a small unit size, and enabling optimization of a single PV module; therefore, PV-SOG will be promising for many applications, including BIPV and self-powered smart glasses.

For solar inverters, high voltage transistors are essential to multiple functions, including DC/DC converters and DC/AC inverters. Currently, state-of-the-art high voltage and high power devices for the solar inverters use the popular SiC and GaN transistors. However, both of those wide bandgap semiconductors require epitaxial growth at high temperature on the strictly selected single-crystal substrates, which excludes their adoption in SOG. In contrast, TFT technology, which offer the low temperature process, and low material and fabrication cost is particularly beneficial to SOGs. As a result this dissertation research focuses on studies and development of oxide-based high voltage TFT (HVTFT) on glass substrate. The novel $Mg_xZn_{1-x}O$ (MZO) is used with the interface engineering to serve as the core HVTFT material. The device adopts the unique symmetric design to enable the high blocking voltage. The comprehensive characteristics with computer simulation provide the insight of electrical characteristics.

In addition to HVTFT on glass technology, we have also conducted the feasibility study to expand HVTFT on flexible substrates. As one of the central technologies of Internet of Things (IoT), wearable electronics have attracted increasing interests and broaden applications. It is critical to have more efficient and convenient wearable power components for the wearable electronic systems.

Up to date, in contrast to the well-studied energy harvest technologies, the related power management systems haven't been well established. The research on flexible HVTFT aims to explore its applications in the self-powered wearable electronics.

1.2. Objectives and Scope of Work

The objectives of this work are to design, fabricate and analyze the prototypes of ZnO-based thin film transistors for high voltage applications. The scope of this dissertation includes:

- Understand and improve the stability, especially Negative Bias Stress(NBS) Stability of ZnO based TFT through development of a ternary $Mg_xZn_{1-x}O$ (MZO) to replace the pure ZnO as the channel layer

- Develop the prototype of MZO HVTFT on glass through unique design of the symmetric structure to resolve electric field crowding therefore increase the high voltage operation.

- Develop Interface engineering to resolve the Zn-diffusion introduced degradation of the TFT devices, thus enhance the IV characteristics and blocking voltage of the MZO HVTFT on glass.

- Conduct comprehensive characterizations with the computer simulation to understand the device physics, especially the interface phenomena to improve the design of the MZO HVTFT.

- Explore the flexible HVTFT by development of low temperature fabrication process of HVTFT on the plastic substrate.

1.3.   Organization of the Dissertation

After presenting the motivation, scope, and organization of the dissertation in Chapter 1, the basic knowledge and technical information are covered in Chapter 2. The introduction includes background of PV-SOG, current HVTFTs technologies, and materials advantages of ZnO for HVTFT. In Chapter 3, the development of a stable MZO TFTs through material engineering is addressed. After the development of a reliable channel material, the design, fabrication, and characterization of a MZO based HVTFTs on glass through the design of device structures and interface engineering are discussed in Chapter 4. To have better ideas of the critical interface engineering and its related benefits for certain applications, Chapter 5 analyzes the MZO transition layer as a diffusion barrier in detail by utilizing different characterization methods, including XPS, FIB/TEM/EDS, electrical measurement, and oxide electrical breakdown test. To broaden the application of ZnO based high voltage TFT, the HVTFT on flexible substrate using low temperature process is covered in Chapter 6. In Chapter 7, a summary and suggested future work are given.

Chapter 2 Technical Background

Energy is one of the most important topics in the 21st century, and solar energy has been a leading technology in the search to replace fossil-fuel energy as a sustainable and clean energy source. However, the adoption rate of solar energy is not as high as expected. The cost and efficiency remain as major concerns, and the aesthetic is another important factor affecting popularity of the solar energy technology. In order to provide an energy-efficient, less expensive, and reliable energy source, we present a new concept of photovoltaics on glass (PV-SOG) technology. In this chapter, the introduction of PV-SOG, especially in the solar inverter, is introduced. The advantages and design of PV-SOG are discussed, so are the comparison among potential high voltage device technologies for solar inverter. At the end of the chapter, the advantages and issues of ZnO for high voltage applications are described.

2.1. Photovoltaics System on Glass (PV-SOG)

PV-SOG integrates solar cells, solar inverters, and controller circuits on a single glass substrate. This system not only provides optimization of single solar module for high energy efficiency but also enables the easy-integration for implementing building integrated photovoltaics (BIPV). BIPV provides better appearance by integrating photovoltaics technologies with the building, and it even makes photovoltaics become parts of the building fabrics, such as ceiling tile, windows. Moreover, the cost can be significantly reduced through a single fabrication process of system-on-glass. Overall, it addresses three major topics of

solar technology: efficiency, cost, and aesthetical appearance. Because the high voltage devices are only required in the inverter circuits, following introduction focuses on the components in solar inverters.

2.1.1. Components in solar inverters

There are two major tasks of solar inverter circuits: generation of largest power output and provide proper current form into grid and/or energy storage equipment, such as batteries, capacitors. The important components in the solar inverters include maximum power point tracking (MPPT), DC/DC converter, DC/AC inverter, and controller circuits.

- Maximum Power Point Tracking (MPPT): MPPT is responsible for tuning the load to maximize the power output of solar modules. The power of a PV module varies due to many reasons, such as the degradation of solar cells, the intensity of sunlight. Through the feedback signal from the PV module like the open circuit voltage, MPPT can vary the operating point of the PV module by adjusting the load to reach the maximum power output. While the PV modules are connected to the batteries in the off-grid system, it is integrated in the DC/DC converter to adjust the output of PV power, so the batteries can be charged efficiently. To improve the efficiency of PV module, MPPT can also be used in conjunction with a mechanical tracking system. By optimizing the face angle the operating point of PV module, the output power of PV system can be maximized.

- DC/DC converter: DC/DC converter can be used to increase or decrease the voltage from the PV modules. Generally, the voltage from PV modules varies from 12 VDC to 70 VDC, and it should be boosted up to the system DC Bus voltage of around 200 VDC or 400 VDC for the grid application of 110VAC or 230VAC[7]. The DC/DC converter also plays an important role to make the PV system robust. While the PV module underperforms, the DC/DC converter can boost up the voltage output, so the following DC/AC inverter can function correctly. For the direct connection between appliances and solar energy, DC/DC converters transform solar energy to applicable DC voltage which can be used directly to drive the appliance, including charging the batteries.

- DC/AC inverter: In order to be connected to the grid, DC/AC inverters are essential to invert DC power from solar cells to AC power for the grid. DC/AC inverter can also be used to amplify the voltage output. There are three popular types of DC/AC inverter circuits: a) With 50/60 Hz transformer(Low Frequency with Transformer, LF-T), b) With HF-transformer (High Frequency with Transformer, HF-T), and c) Transformer-Less (TL).[8] In comparison with the inverters with transformers, TL inverters have following advantages:

  1. Fewer components, small size, and light weight
  2. Cost effective and reliable.
  3. The efficiency is higher (96~98%).

The minimum input voltage of TL inverter has to be larger than 350 VDC. The addition of DC/DC converter (boost-convert) increases the input range; however, the original advantages are slightly sacrificed, such as slightly lower 94% efficiency, slightly heavier weight.[8]

2.1.2. System design (Inverter Topology)

The configuration of PV system affects the overall efficiency and cost tremendously, and the performance varies depending on the circumstance. There are three main categories of inverter topologies: the central inverter, the string inverter, and the micro inverter.

- Central Inverter: The central Inverter as shown in the Figure 2.1(a) is the conventional technology that one inverters connects to multiple parallel PV strings. Each string of PV modules generates a sufficient high voltage, so there is no need to use DC/DC converter. It is commonly used in the large systems, such as utility-scale PV power plants, which produce large power (>30kW, up to 1MW). The configuration is simple and provides a great efficiency when every module function correctly. However, the output power may degrade seriously due to the failure or underperformance of one or several PV modules, and it may result from many reasons, such as partial shading, module degradation, dust, bird droppings. The efficiency of whole system will drag down due to the mismatch between PV modules. Moreover, energy loss is introduced by the centralized MPPT which is not optimized for each PV module, extra energy consumption from the addition of string diodes, etc.[9] The requirement of high voltage DC cables is also a

safety concern. Furthermore, the system is bulky, so it lacks of the flexibility to be mounted on different subjects. Furthermore, the large size of PV system can dramatically change the appearance of the mounted subjects, such as houses, and lots of people don't consider that bulky solar panels are aesthetic. The individual design for each installation make the benefits of mass-production cannot be reached. It could be a great bottleneck for the popularization of solar technology.

- String Inverters: A modified topology of inverters aims at improving energy efficiency by introducing separate MPPT for each string, eliminate the loss from string diode. The topology as shown in the Figure 2.1 (b) is that one inverter only connects to a string of PV modules. Since only a string of PV modules share one inverter, the whole system is more robust against the underperformance of individual PV module. However, the inverter still is connected to several PV modules, so the output condition cannot be optimized specifically for each PV module.

- Micro Inverters: This topology addresses the low efficiency issues in central and string inverters. A micro Inverter connects to only one PV module as shown in the Figure 2.1 (c), so a MPPT can be dedicated to each PV. Also, the solar tracker can be more effective because it only need to consider a single PV module. Overall, the topology of micro inverters can help each PV module to generate maximum power output. Moreover, this topology can make the unit size of PV system smaller, so it provides the flexibility to be utilized on many different applications, such portable devices[10–12], self-

power smart window[13]. Although the customized MPPT for each module produce maximum power output, micro inverter may still suffer from high cost per watt. Because a single PV module cannot provide high output voltage for grid connection, the micro inverters are needed for the high voltage amplification. The high voltage amplification usually is a low efficiency conversion[7]. As a result, the cost of micro inverters is still higher than the cost of centralized inverters in small systems (≤10 kW)[4].
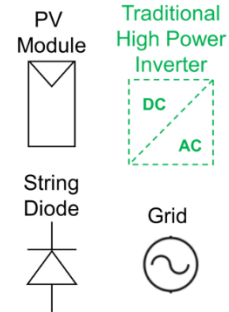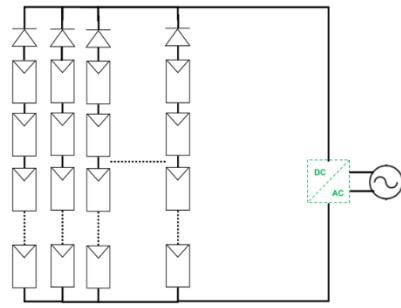
Figure 2.1. The topologies of current inverters: (a) Central Inverter, (b) String Inverter, and (c) Micro Inverter.

2.1.3. Advantages of PV-SOG

In respect of manufacture cost, the configuration of SOG can help to reduce the overall cost. In addition to inverters, all other components including solar cells and controller circuits are designed using the same process, so the mass production of all components on the same product line can be achieved. This integration process also makes unit size of PV-SOG smaller, and it gives the installation of PV system more flexibility. As a result, it has better opportunities to conquer the limitation of space for absorbing solar energy. In respect of energy efficiency, the MPPT is dedicated to one PV module In a PV-SOG, so the output power can be maximum. The reduction of the external connection can cut down the energy loss from the power dissipation of power lines. Overall, PV-SOG can absorb more solar energy and deliver more electric energy than traditional topologies of inverters.

In terms of maintenance and lifetime, since every PV module is integrated with an individual inverter, it is easier to monitor and maintain every PV-SOG. Although the lifetime of individual PV module is the same, the lifetime of overall PV system can extended because of the easiness of repair or replacement of the individual broken PV-SOG.

Last but not least, the glass substrate makes PV-SOG more transparent than conventional system with bulky inverters. Because of the transparency and the small unit size, PV-SOG makes minor changes the effect on the appearance of mounting substrate minimized. Therefore, it is suitable for the application to BIPVs.

2.1.4. Design of PV-SOG

The design of PV-SOG is shown in the Figure 2.2(a), and the development will be divided into two phases. At the first stage as shown in the Figure 2.2 (a), we will would like to use HVTFT in the DC/DC converters. By integrate DC/DC converters directly with PV modules, each system on glass can provides high and stable voltage output for the following centralized DC/AC inverters. Through this integration, the output efficiency of each solar pane can be optimized. Later, we can further apply HVTFT in the DC/AC inverters to form a real PV-SOG as shown in the Figure 2.2 (b). It requires a high frequency operation to produce a better pseudo-sinusoidal output; therefore, the deeper understanding and improvement the AC performance of HVTFT are necessary. By integrating all components of solar inverters, the benefits of PV-SOG mentioned in previous section can be fulfilled. For different applications, such as different amount of sunlight exposure, the configuration of PV-SOG can be modified. If the system is for charging batteries, it only requires an integrated DC/DC converter. If the PV module can provide high DC output, the system only requires a DC/AC inverter for the connection to the grid. On the other hand, if the PV module can only provide low DC output, both a DC/DC converter and a DC/AC inverter are necessary for PV-SOG.

(a) 1ˢᵗ stage
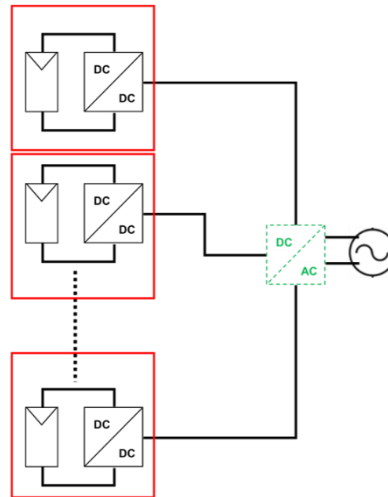
(b) PV-SOG
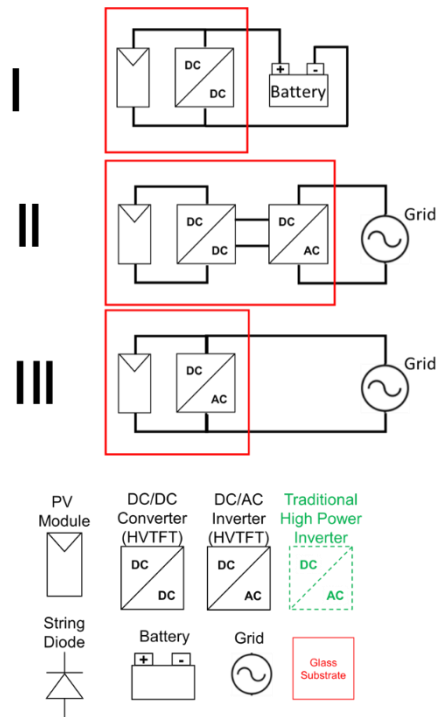
Figure 2.2 Topology and design of (a) first stage of integration, and (b) PV-SOG

As shown in the Figure 2.3(a), the output voltages of DC/DC converters are 200 VDC and 400 VDC for the grids of 110 VAC and 230 VAC, respectively[7]. In order to be utilized in the inverters, our target of blocking voltage of 300V and 600V for the system of 110V and 230V AC system, respectively. One of the major goal of this proposal is to apply PV system on glass to the mobile applications. For these application, low stand-by power consumption is critical; therefore, we seek to lower the off leakage current. On the other hand, in order to be operated at higher frequency, a better on-state performance is also important. Therefore, a large ON/OFF current ratio is the main goal.

For the design of DC/DC converter, in order to be integrated on a substrate glass substrate, a bulky transformer is unwanted. Therefore, we would like to adopt transformer-less boost-up circuit as shown in the Figure 2.3(b) for the PV-SOG where HVTFTs are used as the switch. The transformer-less converter use inductors and/or conductors without using bulky transformer to generate voltage gain, and the gain only depends on the duty cycle in continuous boost-up circuit. The ideal gain of boost-up circuit is based on the equation (2.1):

$$Gain = \frac{V_O}{V_i} = \frac{1}{1-D} \tag{2.1}$$

By changing the input signal to the HVTFT, the gain changes. However, when the amount of energy stored in the inductor cannot provide continuous current during the OFF period, the circuit operates in the discontinuous mode. Unlike in the continuous mode, the gain in the discontinuous mode is lower and affected by the inductor value, the input voltage, the commutation period, and the output current.

For the design of the DC/AC inverter, a circuit of the full bridge (H bridge) inverter as shown in the Figure 2.3(c). By using pulse width modulation, it can transform the DC signal into AC sinusoidal signal. While the frequency is 1 kHz, the output signal is still choppy. If the frequency reaches 16 kHz, the wave form will be very close to sinusoidal wave[8]. HVTFTs will be used as the 4 switches indicated in the figure. As a result, the DC/AC inverter requires the switches have great performance at higher frequency.

(a)PV inverter
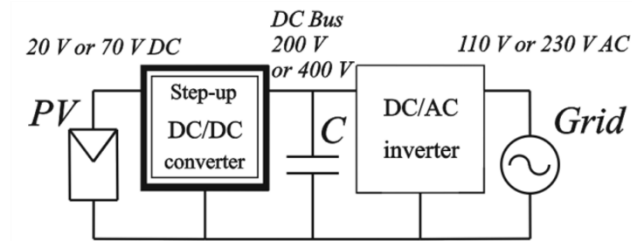
Fig. 3. The example of PV inverter with integrated DC/DC step-up converter

(b)DC/DC Step-up Converter   (c)Full Bridge Inverter
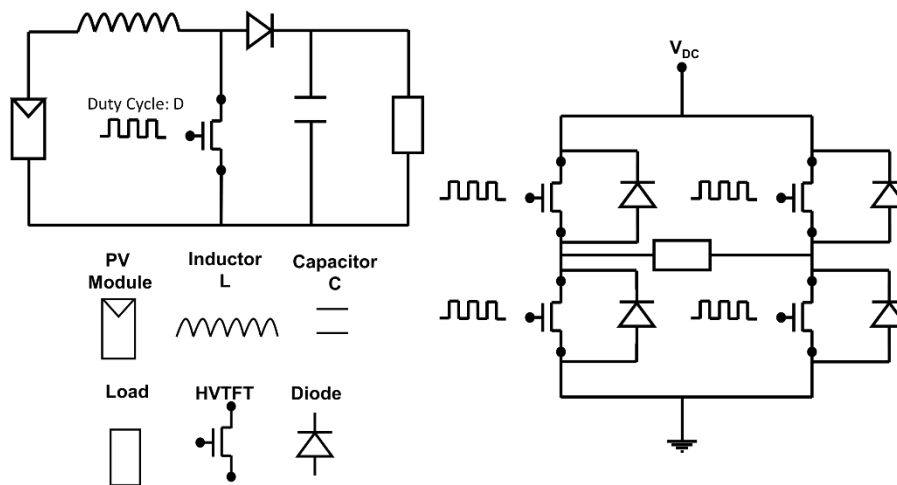
Figure 2.3 (a) A schematic of a PV system, including a PV cell, a converter, an inverter, and a grid[7] (b) A circuit of a transformer-less DC/DC converter. (c) A circuit of a full bridge inverter.

2.2. High Voltage Thin Film Transistors (HVTFTs)

For the solar inverters, high voltage transistors are essential to several applications, including DC/DC converters, DC/AC inverters. As mentioned in previous chapter, state-of-the-art high voltage and high power devices, such as SiC, GaN transistors for the solar inverters are not compatible with PV-SOG because these devices require epitaxial growth at high temperature on strictly selected single-crystal substrates. As a result, TFT technology, which has low process temperature and fabrication cost, is compatible and beneficial for SOGs. As a result, here we only focus on the high voltage TFTs.

2.2.1. Channel Materials for HVTFTs

Several semiconductor materials have been tried out to make HVTFT devices. Amorphous Si[14] and poly-Si[15] HVTFTs have been studied since the 1980s[16–18]. For the part of amorphous Si HVTFT, in early period (1993), Martin et al.[19] already demonstrated an amorphous Si TFT as shown in Figure 2.4(a) can sustain operating voltage of 400 V with drain offset structure. However, the on/off ratio was only around 5 orders. In 1999, Nahm et al.[20] demonstrated a α-Si: H HVTFT with thick double layer gate insulator for reflective active-matrix cholesteric liquid crystal displays. The on/off ratio reached 6 orders and ON-current reaches 10 μA at V_{DS}=100V as shown in Figure 2.4(b); however, the operating voltage only reached 100V. Chow et al. demonstrated an amorphous Si TFT could provide high blocking voltage up to 800 V[21] using input voltage 0~20V, and it was integrated with MEMS-- a cantilever bridge in Figure 2.4(c). Although the fabrication of amorphous Si TFTs could be at low temperature (<400°C), its poor performance

(on/off ration~10^4) limited its application. For the part of Poly-Si HVTFTs, in 1988 Unagami[22] demonstrated High-voltage poly-Si TFTs with multichannel structure in Figure 2.5(a). The devices had high on/off ratio of 7 orders. However, the blocking voltage was only around 130V, and the fabrication temperature of 670°C could be risky for some regular glass substrates, not to mention flexible substrates. In 1990, Huang et al.[23] designed poly-Si HVTFTs with metal field plate in Figure 2.5(b), and the current-pinching effects result from offset region was alleviated, but the blocking voltage was still around 100V. In 2002, Krishnan et al.[16] demonstrated a dual gate HVTFT with variable doping slot in Figure 2.6(a) which has a blocking voltage in excess of 300V. However, the on/off ratio was limited around 4~5 orders, and the fabrication process could be complicated due to control of doping profile. Furthermore, the process temperature reached 600°C which could be a concern for regular glass substrate. In 2004, Cheng et al.[24] utilized excimer laser crystallization (ELC) to fabricate poly-Si lateral double diffused metal oxide semi-conductor (LDMOS). As shown in Figure 2.6(b), the blocking voltage reached 240V, and on/off ratio was 1.23×10^6. However, the process temperature kept as high as 600°C, and the expansive laser annealing made TFTs have poor uniformity especially in the large area applications. Overall, poly-Si HVTFTs show better driving capability, but their low blocking voltage and non-uniformity from grain boundaries make them inadequate to meet the requirements of PV-SOG. In addition, all Si-based TFT technology suffers from the absorption of visible light, restricting its application for transparent electronics.

Figure 2.4 (a) The transfer characteristics of an α-Si HVTFT in early period[19]. (b) The transfer and output characteristics of α-Si:H HVTFT with a thick double layer gate insulator[20]. (c) The top-view pictures, transfer and output characteristics of α-Si:H HVTFT which was integrated with MEMS [21].

(a)
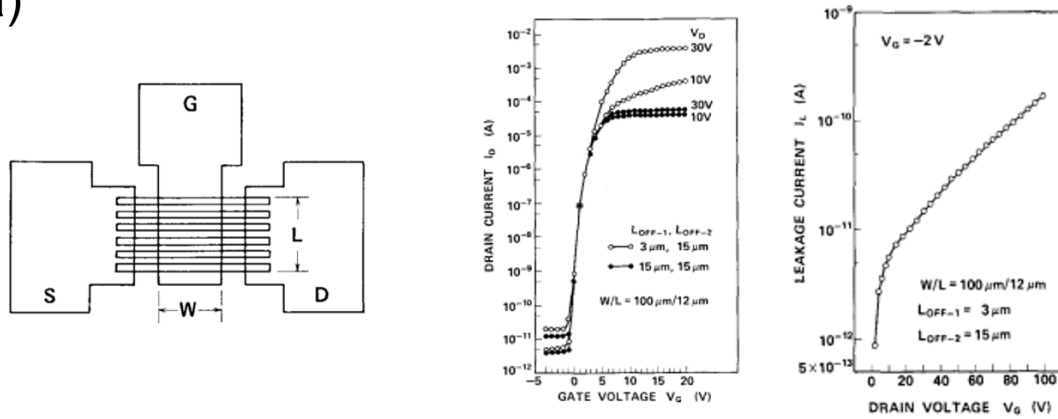
(b)
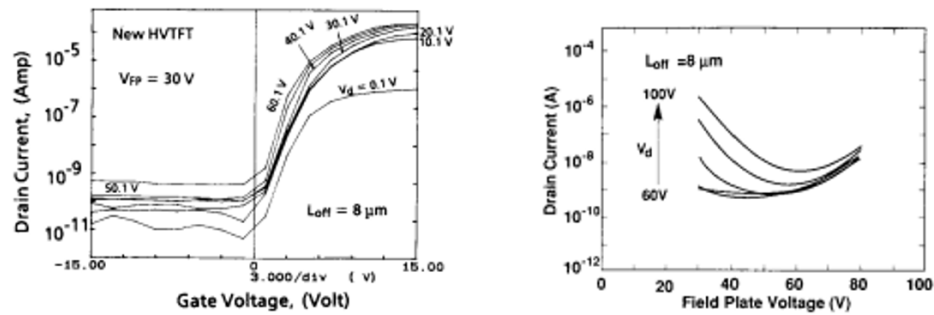
Figure 2.5 Electrical Performance of poly-Si HVTFTs. (a) The top-view, transfer

characteristics and leakage current of High-voltage poly-Si TFTs with multichannel

structure[22]. (b) The transfer characteristics and effect of field plate bias on the drain

current of poly-Si HVTFTs with metal field plate[23].
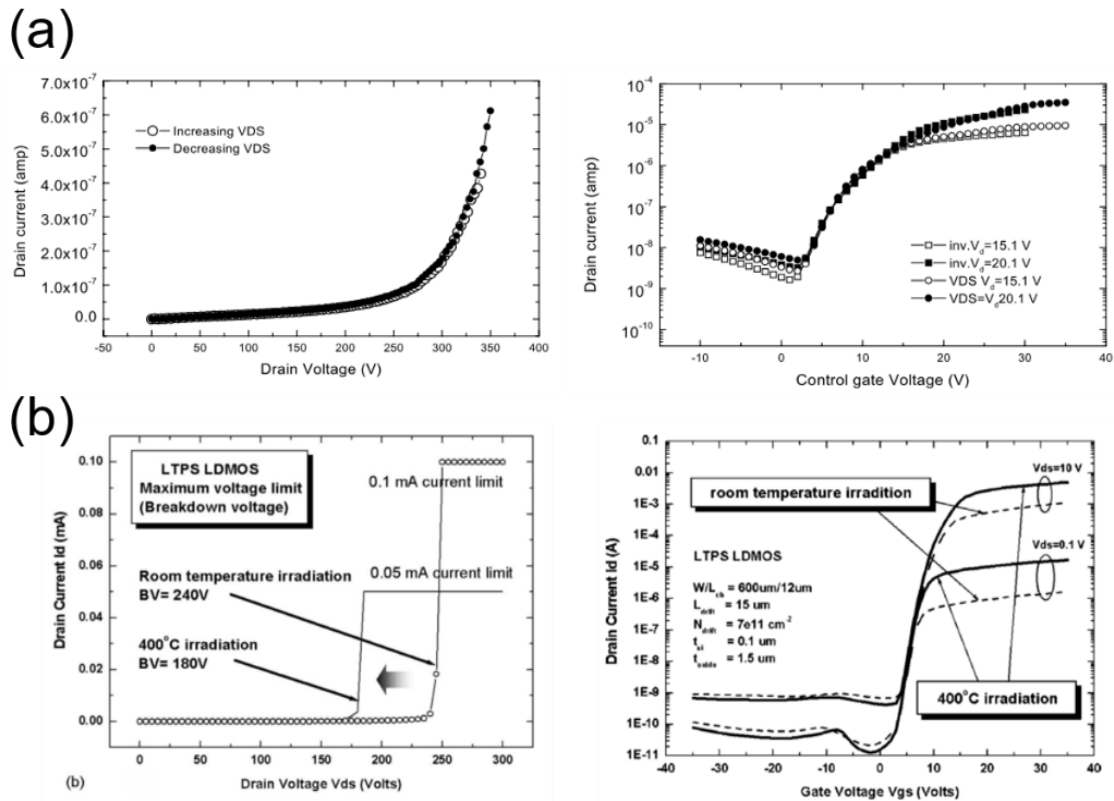
Figure 2.6 Electrical Performance of poly-Si HVTFTs. (a) The transfer and output characteristics of a dual gate HVTFT with variable doping slot[16]. (b) The transfer and output characteristics of a poly-Si lateral double diffused metal oxide semi-conductor (LDMOS) which is fabricated by excimer laser crystallization (ELC)[24].

Due to the restriction of Si-based TFT, people started working on new semiconductor materials for high voltage TFT. Organic materials and oxide semiconductor are the most popular candidates. Organic TFTs which offer low cost and low process temperature have been used in display and RFID technologies. Recently, Smith et al.[25] reported a high-voltage organic thin-film transistor (HVOTFT), which showed switch drain-to-source voltages higher than 300 V with a controlling voltage range from 0 to 20 V in Figure 2.7. However, its low mobility, poor long-term stability basically excluded its application in PV-SOGs, which operate under sunlight radiation, and its lifetime, like the regular residential solar cells, is expected   to be more than 25 years[5].

Since Nomura et al[26] demonstrated Indium Gallium Zinc Oxide (IGZO) TFTs with high electrical performance at low process temperature, oxide semiconductor TFTs have emerged in many applications, especially in displays, and transparent electronics. In the area of HVTFT, Jeong et al.[27] reported an IGZO HVTFT in Figure 2.8 which operated at above 100 V with an ON/OFF current ratio of 10^7. Although this is beyond the regular operating voltage in regular TFTs, it is still not sufficient to be used in inverters for a solar PV system. Furthermore, it is desired to use indium-free materials due to the high cost of indium, especially in the case of large-area electronic systems such as solar cells. In addition, the toxicity of IGZO due to its high indium concentration is of considerable environmental concern.

(a)
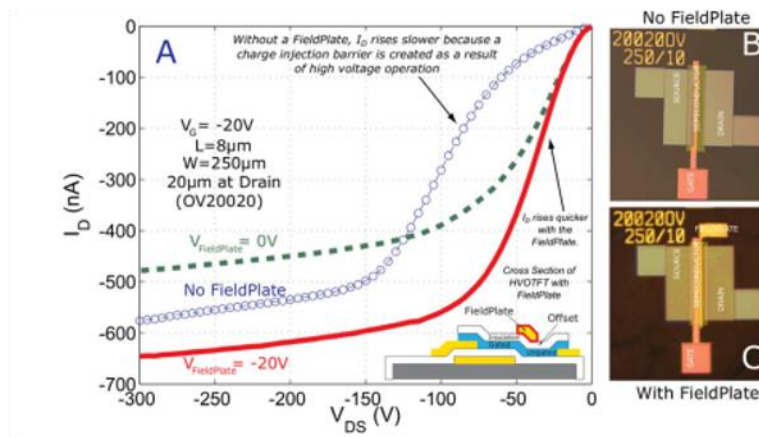
(b)
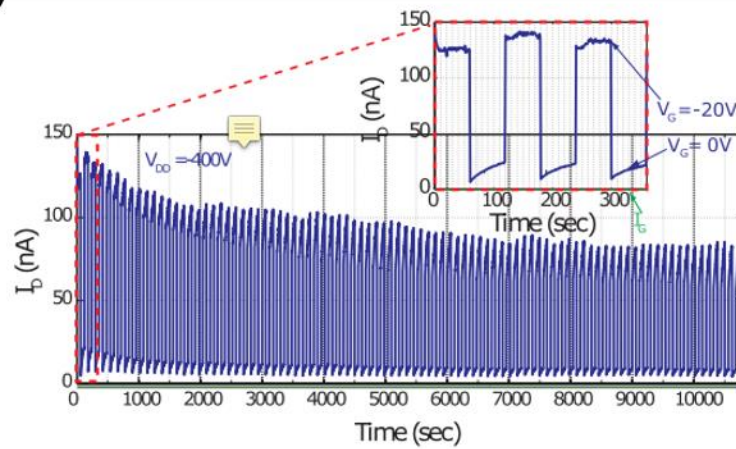
Figure 2.7 (a) The output characteristics of a single HVOTFT. (b) Output current

of a inverter circuit built by HVOTFT.[25]
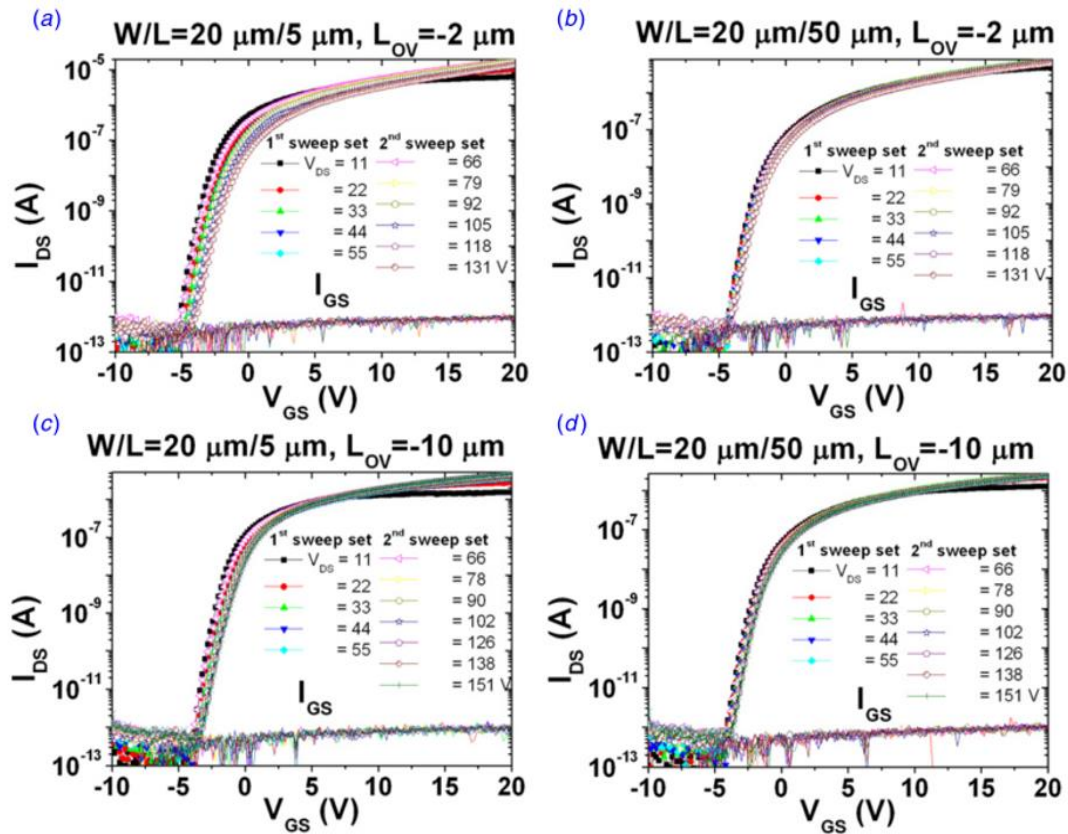
Figure 2.8 The transfer characteristics of an IGZO HVTFT of different dimensions[27].

2.2.2. Device Structures for HVTFTs

In 1982, Unagami et al.[15] demonstrated the symmetric offset region as shown in Figure 2.9(a) to prevent large potential (drain bias) across the gate dielectric and gate-induced junction breakdown. These offset regions could smooth the distribution of electrical field, so the peak of electrical field would be reduced. As a result, the devices could operate in the condition of the higher bias. As shown in Figure 2.9(b), devices with a longer offset showed higher blocking voltage, no matter what the methods of fabricating the offset structure were used. However, these offset regions were high-resistive regions, so the driving capability of device was impaired as shown in Figure 2.9(c). Also, the high resistive offset area resulted in current crowding.

In 1988, Tanaka et al.[28] used lightly doped drain (LDD) ion implantation to increase the conductivity of offset regions as shown in Figure 2.10(a). By adjusting the dopant concentration, the on/off ratio improved more than an order. However, this LDD also weakened the blocking capability of HVTFT, and the control of low doping profile was hard due to the "dopant segregation" effect[17]. Also, the devices with LDD suffered a severe current pinching phenomenon and reproducibility problems. The relationship between blocking capability and performance of ON state was still a trade-off.

To break this trade-off between blocking capability and ON-current, Martin et al.[29] and Huang et al.[23,30] added an independently biased metal field plate (MFP) overlapping partially or entirely the offset area as shown in Figure 2.11(a). When HVTFT was in the ON-state, the MFP bias (V_{FP}) could increase the conductivity of

the offset area, so the effect of increases of offset length on the ON-current was minimized as shown in Figure 2.11(b). Under OFF-state (blocking voltage), MFP bias (V_{FP}) could suppress the leakage current as shown in Figure 2.11(c). Therefore, the on/off ratio improved. Moreover, MFP technology also lowered the dependence of ON-current and leakage current on the offset length, so it made devices more immune to misalignment error. Although MFP made a better balance between blocking capability and ON-current, it required an extra electrode and two-steps dielectric deposition. Moreover, the operating points of MFP bias required optimization based different drain bias. As a result, it increases not only the cost but also the complexity of the circuit design, and it is not compatible with regular device processing.

In 1996, Chen et al.[31–33] invented a Semi-Insulating (SI) field plated High Voltage TFT as shown in Figure 2.12(a). The SI field plate connected from the gate to the drain reduced the effective offset in the ON-state, and in the OFF-state it still kept the function of offset region as shown in the Figure 2.12(b). Therefore, the SI HVTFT had better performance in both blocking capability and on-state performance of HVTFT as shown in the Figure 2.12 (c) and (d) respectively. Although higher conductivity of SI field plate could improve the switching speed in the ON-state, it was limited to restrict the leakage from SI field plate at low level in the OFF state.

In 2002, Xu et al.[17] proposed a new method: variable doping slots (VDS) as shown in the Figure 2.13(a) in the offset region to improve the performance. As shown in Figure 2.13(b) and(c), VDS devices showed better transfer

characteristics and blocking voltage than LDD device and offset-drain device. However, VDS still required precise control of doping profile to avoid electrical field crowding, and the extra implantation was costly.

(a)
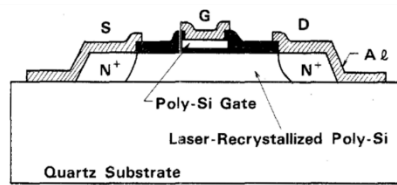
(b)
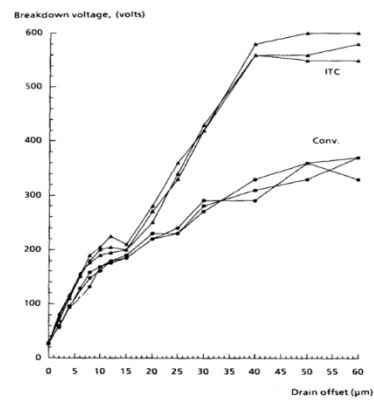
(c)
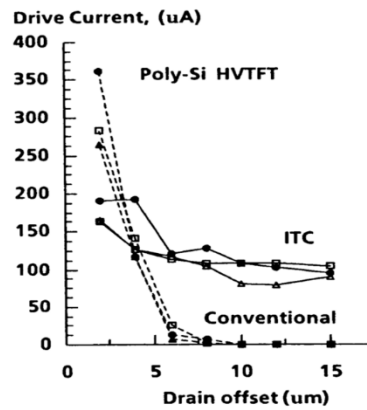
Figure 2.9 (a) Cross-section of symmetric offset gate HVTFT[15], (b) The relationship between the blocking voltage and offset length in the conventional and implant-through-contact (ITC) offset gate HVTFT[34], and (c) The relationship between the ON-current and offset length in the conventional and ITC offset gate HVTFT. [35]
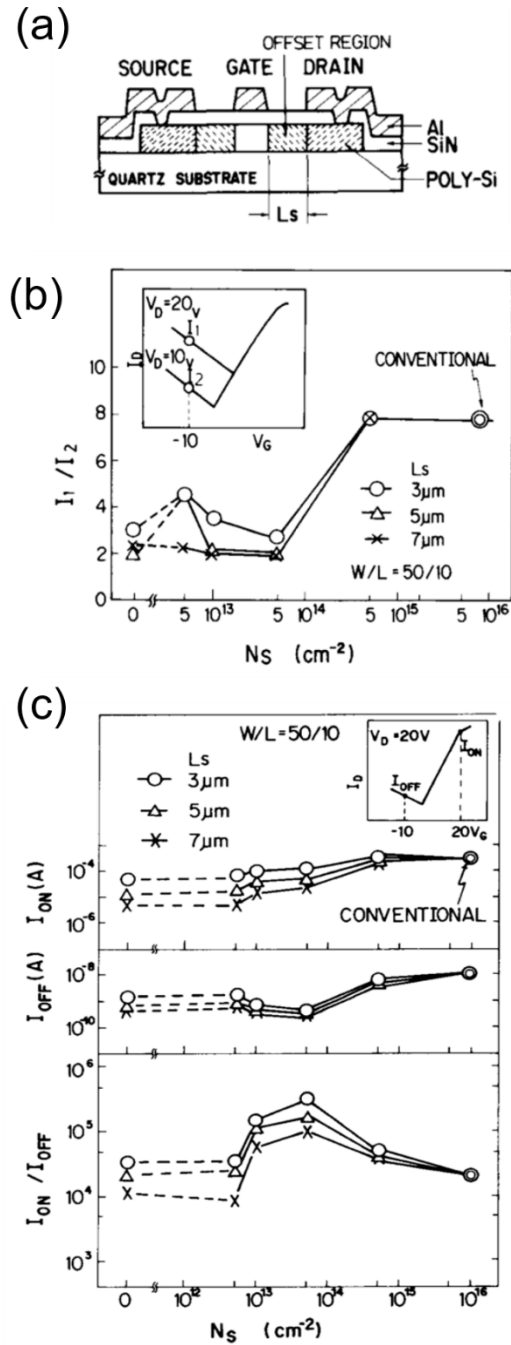
Figure 2.10 (a) cross-section of LDD dopant offset TFT, (b) the effect of doping concentration on the leakage current increasing rate with drain bias, and (c) the effect of doping concentration on on/off ratio [28]

(a)
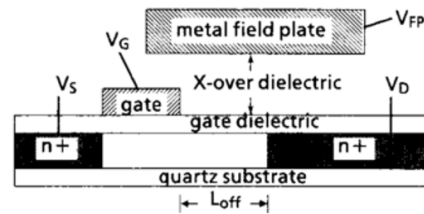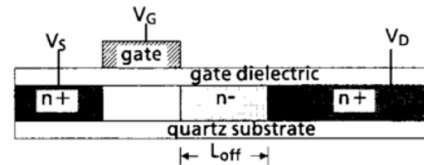
(b)

conventional (dashed line)
FP-HVTFT's (solid lines).

Log (Drain current), (µA)

cross: $V_D = 60.1$ V
Triangle: $V_D = 40.1$ V
square: $V_D = 20.1$ V
circle: $V_D = 0.1$ V

All Curves @ $V_G = 10$V

Offset Length (µm)

(c)

conventional (dashed line)
FP-HVTFT's (solid lines).

Log (Drain current), (pA)

All Curves @ $V_G = 0$V

$V_D = 100$V

$V_D = 60$V

$V_D = 20$V
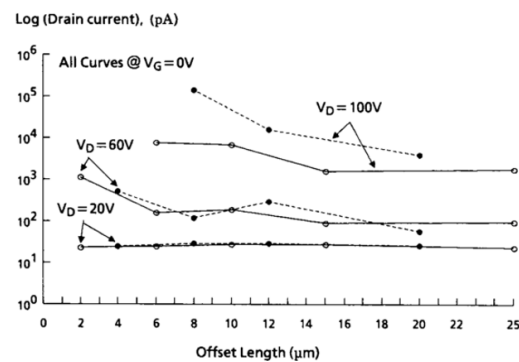
Offset Length (µm)

Figure 2.11 (a) Cross section of FMP HVTFT in comparison with the regular gate offset HVTFT, the effect of the bias of metal field plate on the (b) ON-current, and (c) the OFF-current with different offset lengthes. [30]

(a)

(b)

(c)

(d)
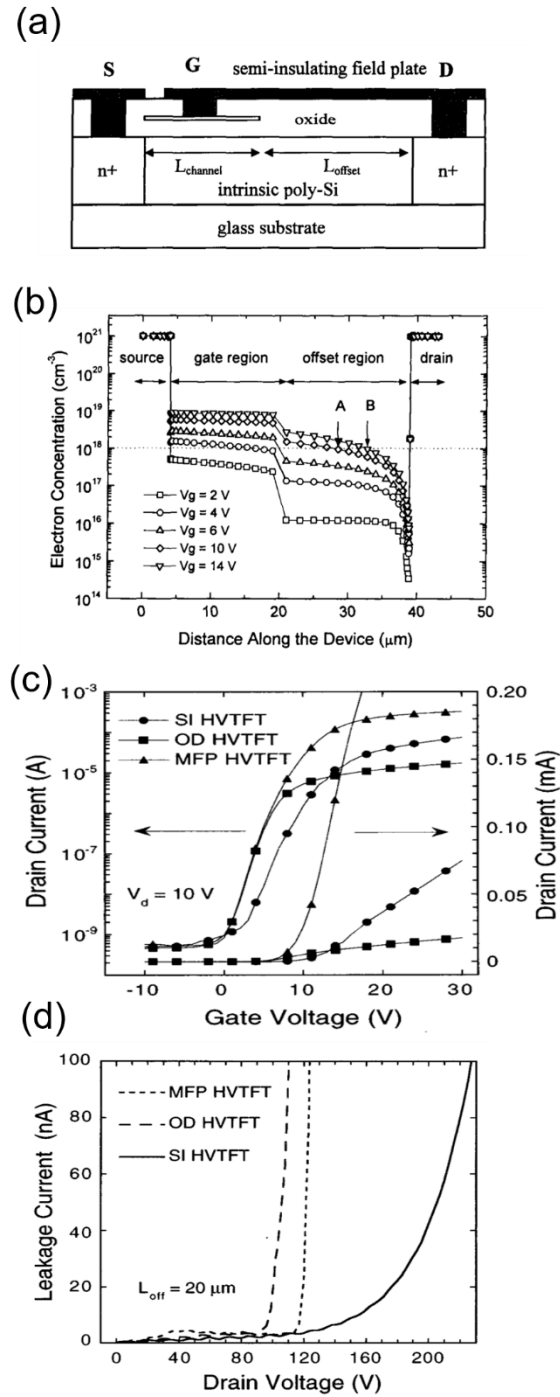
Figure 2.12 (a) Cross section of SI HVTFT in comparison, (b) the effect of the gate bias on the effective offset lengthes, the comparison of (c) On-state performance , and (d) the blocking voltage between SI, OD, and MFP HVTFTs. [31]
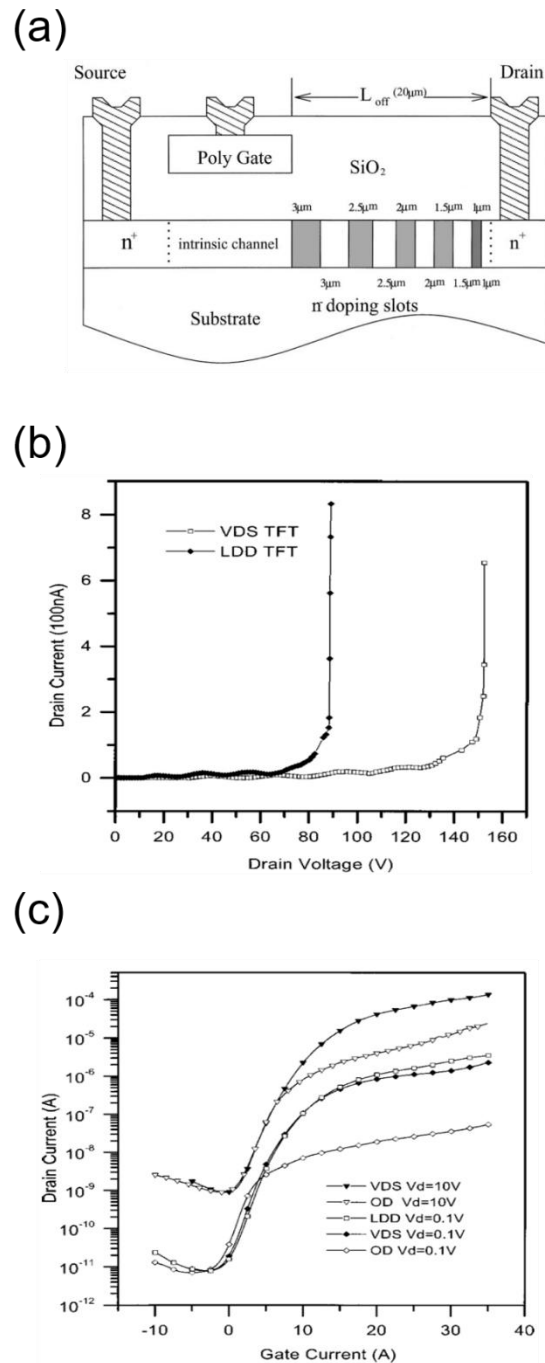
Figure 2.13 (a) Cross section of VDS HVTFT in comparison, (b) the comparison of blocking voltage ce between VDS and LDD HVTFTs, and (c) the comparison of On-state performance between VDS and LDD HVTFTs.[17]

2.3. Advantages of ZnO for HVTFTs

In last decades, ZnO has been widely studied as an electrical, optoelectric, piezoelectric materials, and people has applied it to different kinds of devices, such as varistors, thin film transistors, memory. Therefore, the fabrication process of ZnO based devices are developed and optimized well, and some technologies, such as IGZO TFTs are even commercialized to mass production. These well-developed technologies can speed up the development of ZnO based HVTFT. Moreover, ZnO material possesses following important features which are critical to the application of high voltage active devices.

2.3.1. Wide Bandgap Materials

Although the maximum breakdown field measured in the experiment is affected by the defects, composition mismatch and measurement erros[36], the theoretical breakdown field of a material is strongly related to the intrinsic energy bandgap. ZnO, a wide energy bandgap materials, has high electrical breakdown field. For the junction breakdown, several literatures indicated the direct relationship between energy bandgap and blocking voltage.[36,37] Ideally, ZnO has breakdown electrical field of 2×10^6 V/m which is almost ten times larger than Si $(0.3 \times 10^6$ V/m) [38]. For transverse electric field, ZnO materials can sustain high electric filed, so it is the major materials used in the varistors for surge protection. For longitudinal electric field, Zhang et al. reported that the single crystalline ZnO nanowires can sustain electrical field of level of 10^6 V/m[38].

2.3.2. High Thermal Conductivity

For a high voltage or high power device, it's very critical to dissipate heat from the devices. Using materials of high thermal conductivity can prevent the accumulation of heat, so the related failure, such as joule heating can be alleviate. The thermal conductivity of ZnO is 1~1.4 (W/cm-K) which is as high as Si (1.5 W/cm-K)[39]. Although it cannot compared with the supreme thermal conductivity of SiC (5 W/cm-K), it is at the same level as GaN (1.3 W/cm-K)[40].

2.3.3. Transparency

As a wide bandgap material, ZnO is a transparent materials which does not affect the appearance of the substrate. By building ZnO on transparent substrates, it is easier to develop the transparent electronic devices. As mentioned in the previous paragraph, the aesthetic appearance plays an important role on the adoption rate of solar technology. If the PV system can be transparent, it won't affect the appearance of mounting surface. As a result, transparent PV system will be very suitable for the application of BIPV.

2.3.4. High Quality Channel Layer at Low Process Temperature

Currently, the state-of-the-art high voltage and high power devices use the popular SiC and GaN transistors. However, both of these wide bandgap semiconductors require epitaxial growth at high temperature on strictly selected single-crystal substrates, which excludes their application in SOGs. In contrast, TFT technology made at low temperature is a more suitable candidate for PV-SOGs. In order to fabricate devices on large area substrate, the fabrication process has to be compatible with large and low-cost substrates, such as regular glass

which cannot sustain higher temperature. Si based materials are most popular in the TFT technologies. Poly-Si TFTs show its advantages over α-Si: H TFTs in mobility (~100 cm^2/V-s) because of large crystal size in poly crystalline film. However, the unpredictable distribution of grain boundaries of poly crystalline form result in poor uniformity of device performance. Therefore, in the case of covalent semiconductors, such as Si, the uniformity and performance are the trade-offs.

To solve issues in Si based TFT, many alternative materials for the channel in TFT are studied, and it can be divided into two major directions: low cost and higher performance. In the area of pursuing low cost TFTs, the organic TFTs (OTFTs) are proposed to replace α-Si: H TFTs because of the low cost growth methods such as spin-coated, printed, or casted on the substrate at room temperature without using vacuum equipment. However, the stability will be the major concern for OTFT.[41] In the area of the high performance TFT, ionic oxide TFTs attract lots of attention in recent years. In the conventional Si-based semiconductor materials, the carrier transport paths by "sp3"orbital are strongly directive, so the disorder in the crystalline structure will degrade the mobility seriously. However, in the ionic oxide semiconductors, such as ZnO have the carrier transport paths through less-directive "s" orbital contributed by post-transition metal cations, so the disorder effect on the carrier transportation is minimized. As a result, ionic oxide semiconductors have higher carrier mobility in less-crystalline structure than covalent semiconductors do.[26] Since ionic oxide semiconductors have the mobility (10~100 cm^2/V-s) in less-crystalline structure, it can have the high mobility without sacrificing the uniformity in the amorphous form

or nano-crystalline form. As a result, oxide TFT make a good balance between better uniformity (amorphous Si TFT) and higher mobility (poly-Si TFT).

Meanwhile, the low order crystalline of the film can be achieved at a lower growth temperature, so the high performance oxide semiconductor transistors can be built at a lower process temperature. This opens the possibility of building the high performance transistors on the low-temperature substrates, such as normal glasses, polymer substrates, and flexible substrates. It is very critical to the novel TFTs applications, such as portable electronics, flexible electronics, and wearable electronics.

In application of PV-SOG, the HVTFTs is built on a glass substrates, and the deformation of regular glasses is around 650°C. If the high temperature process is used, the expensive quartz substrates are required. As mentioned in previous sections, we are targeting the reduction of cost for the large application. As a result, the process temperature should be controlled below 600°C.[42] In fact, in this study, our highest process temperature was only 400°C.

2.4. Reliability issues of ZnO TFTs

The stability of TFTs plays an important role in the practical application. As an infrastructure, solar technology has a strict standard of 25-year life time. As core components in solar energy system, solar inverters also have a high request on the devices.

The reliability issues in ZnO TFTs are more complicated than Si-based TFTs because ZnO consists of more types of defects from two elements: Zn and O. The most abundant native defects to be Zn or O vacancies depends on the growth

condition, and different growth conditions result in differences in chemical stoichiometry.[43] In the study of ZnO based TFTs, it is believed that the native defects in the ZnO based channel layer have a great impact on the device characteristics, including field effect mobility, on-off ratio, subthreshold swing, and bias stress stability[44]. Based on the first principles calculation, the oxygen vacancy in ZnO has the lowest formation energy[45] among the donor like defects. Because oxygen vacancy is a deep state in the n-type ZnO, it is generally in the neutral state. (V_O). However, in the several circumstances, it still strongly affect the conductivity of the channel.

First, under negative gate voltage, a depletion region is created in the TFT channel. In the depletion region, the fermi level approaches toward valence band minimum, the electrons in the deep state (V_O) can be excited and released into the conduction band. Because V_o^+ is thermodynamically unstable, V_o^{2+} is the preferable state. These electrons released from oxygen vacancies would increase the conductivity of channel and affect the stability of ZnO TFTs. Second, this instability will be worse at a higher temperature while the thermally excited oxygen atoms release from original sites and create vacancies. [46]

The inverters block the voltage at OFF status, and it requires negative gate bias to deplete the ZnO channel. Therefore, the HVTFT will majorly operate under negative gate bias. Meanwhile, due to the heat induced by long time exposure to sun light, the operating temperature of solar technology is usually higher. This high temperature will be a great challenge to ZnO HVTFT.

2.5. Summary

In the chapter, we presented the technical background of the high voltage transistors for solar inverters. The basic introduction of solar energy system is described, including the importance of solar inverters, topologies, and components in the solar inverters. To promote the popularity of solar technologies, several solar applications have emerged, such as BIPV, smart glass. We proposed a concept of PV-SOG suitable for these applications and defined the requirement of HVTFT for PV-SOG.

The previous works of HVTFTs were reviewed. Up to date, most studies have focused on devices using Si materials, including amorphous Si and polycrystalline Si. In order to optimize the trade-off between the ON-current and blocking capability, several device structures and process methods were developed, including symmetric offset gate, LDD dopant offset, FMP, SI, and VDS. However, existing Si based HVTFT technologies are not suitable for PV-SOG due to the intrinsic limitation of Si, such as small bandgap, and poor electrical performance at low crystalline form.

To solve these issues, we studied a wide bandgap oxide semiconductor ZnO as the candidate for HVTFTs in PV-SOG. ZnO has intrinsic advantages, such as large bandgap and good thermal conductivity, promising for high voltage operation. In particular, ZnO keeps relatively high electrical performance even at low crystalline form. Moreover, the Indium-free feature makes ZnO price competitive in comparison with other oxide materials, such as In-Ga-Zn-O (IGZO). However,

ZnO has some intrinsic issues of negative bias and thermal stability. The majorly related defects- oxygen vacancies introduce instability of threshold voltage in ZnO TFT. Therefore, in the dissertation we would add a small amount of Mg into ZnO to form a ternary oxide, $Mg_xZn_{1-x}O$ (MZO, X<0.03) as the TFT channel. This was an effective and cost efficient way to improve the stability which made MZO a great candidate for HVTFTs in PV-SOG.

The development of MZO HVTFTs will open the opportunity to incorporate high voltage transistors in the system integration; therefore, it will build the foundation of PV-SOG which can provide people less expensive, more aesthetics, and more efficient solar energy system. In addition to solar inverters for PV-SOG, HVTFTs may be utilized in other integrated system, such as self-powered smart glasses, flat-panel x-ray imaging systems for medical radiology, and space engineering.

Chapter 3 Improvement of Stability of ZnO TFTs

3.1. Background

Currently, majorities of manufacturers offer the 25-year standard solar panel warranty, which means that power output should not be less than 80% of rated power after 25 years. Inverters in PV system should have similar long life span, so it is critical for high voltage devices in solar inverters to have robust and stable electrical performance. Pure ZnO TFTs have a critical concern of the stability issues that turn-on voltage of ZnO TFTs shifts. This instability of turn-on voltage is more serious at higher temperature and at high negative gate bias. Unfortunately, solar panel often operates at higher temperature due to the long exposure to the sunlight. Moreover, the HVTFT works at negative gate bias to block the high voltage. These high temperature and negative gate bias are big challenges to pure ZnO devices.

Several reports indicated that donor like defects associated with oxygen vacancies could result in electrical instability in ZnO based TFTs[43,47]. To overcome shortcomings of ZnO TFTs, the IGZO TFTs emerged as a promising enabling technology which is now quickly commercialized to mass production. However, as mentioned in the previous chapter, with an increase in the cost of Indium metal and environmental concerns, it is also desired to develop an Indium-free TFT technology, especially for low cost applications.

To address this issue, we developed a ternary MZO film as the channel layer. A small amount of Mg is introduced into ZnO to form the $Mg_xZn_{1-x}O$ (x=0.03) channel layer, where the Mg-O has a stronger bonding energy (393.7 kJ/mole)

than that of Zn-O (284.1 kJ/mol). Thus, it requires more energy to form an oxygen vacancy in the ternary $Mg_xZn_{1-x}O$ alloy[48]. The amount of Mg incorporation in $Mg_xZn_{1-x}O$ is kept low to avoid the degradation of TFT electrical characteristics from the alloying induced scattering and disorder. Our previous work already demonstrated that a small amount of Mg doping into ZnO improved in the thermal stability[49]. This chapter would focus on the stability at negative gate bias.

3.2. Fabrication Process and Setup of Electrical Test of Regular TFTs

To simplify the problems and speed up the process, in this study of the negative bias stress we utilized the regular common bottom gate TFT, instead of high voltage structure. The fabrication process is illustrated in Figure 3.1. Bottom gate $Mg_xZn_{1-x}O$ (x=0, 0.03) TFTs were fabricated on heavily-doped p-type Si wafers with a 50 nm thermally grown SiO_2 as a gate dielectric. Two types of 50 nm channel layers: ZnO and $Mg_{0.03}Zn_{0.97}O$ (MZO) were grown by MOCVD at 400°C. DEZn (diethyl zinc) and MCp2Mg (bis (methylcyclopentadienyl) magnesium) were the precursors for Zn and Mg, respectively. The concentration of Mg in MZO film was characterized by using the optical bandgap in the transmission spectrum. The channel layers were patterned by the wet etch process, and two-steps procedure was used to prevent the undercut profile. The first step was done by diluted hydrochloric acid (1:2000) 5 seconds, and the diluted acetic acid (1:2000) 35 seconds was the second step. The source and drain metallization were formed with 100 nm Ti/ 50 nm Au by a lift-off process. The channel layer dimension is fixed at a width/length (W/L) ratio of 150 μm / 5 μm. An AZ-5214 photoresist layer was

coated on top of the TFT channel, serving as a passivation layer to prevent ambient absorption/desorption during the electrical testing. All the electrical/NBS stability tests were conducted in a light-tight probe station using an HP-4156C electrical testing system.

(a) Thermal Oxidation SiO$_2$ 55nm

Gate Oxide SiO$_2$

p^{++} Si substrate as Bottom Gate

(b) MOCVD ZnO-related deposition

ZnO Related

Gate Oxide SiO$_2$

p^{++} Si substrate as Bottom Gate

(c). Photolithography Pattern & Wet Etch

ZnO Related Channel

Gate Oxide SiO$_2$

p^{++} Si substrate as Bottom Gate
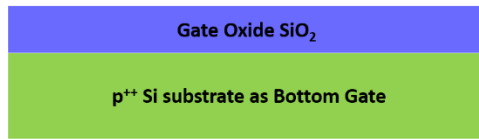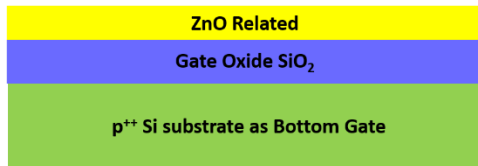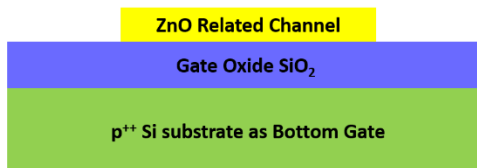
(d)*Photolithography Pattern (Source/Drain)
    Image Reversal for lift-off process
  *E-beam Evaporator
    Titanium 100nm/ Gold 50nm
  *Immerse in Acetone for metal lift-off

Ti/Au
Drain

Ti/Au
Drain

ZnO Related Channel

Gate Oxide SiO$_2$

p^{++} Si substrate as Bottom Gate
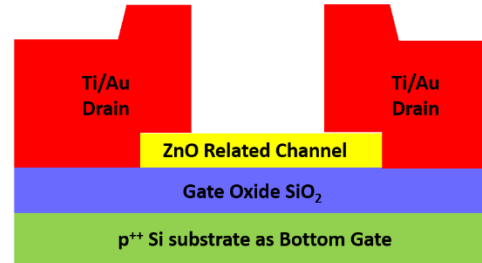
(e) *Photolithography Pattern (Contact)
    Photoresist works as a passivation layer
  *SiO$_2$ wet etch for the gate contact pad

AZ 5214 (Photoresist)

Ti/Au
Drain

Ti/Au
Drain

ZnO Related Channel

Gate Oxide SiO$_2$

p^{++} Si substrate as Bottom Gate
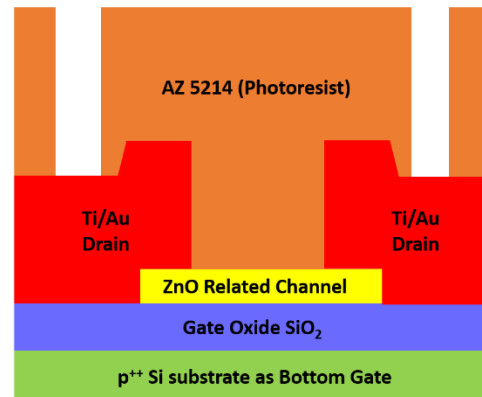
Figure 3.1 (a) ~ (e) The schematic diagram of fabrication process and (e) cross-sectional view of the regular TFT

3.3. The Effect of Mg-doping on the Electrical and Material Characteristics

The transfer characteristics of ZnO and MZO TFTs with V_{DS}=10Vand V_{DS}=0.1V are shown in Figure 3.2 (a) and (b) respectively. The threshold voltage (V_{TH}) is defined as the gate voltage value when a drain current (I_{DS}) reaches 10^{-8} A. The field effect mobility (μ_{FE}) is extracted from the linear region (V_{DS}=0.1V). The subthreshold swing (S.S.) is extracted from a 3-decades range in the subthreshold region of the log10 (I_{DS}) vs V_G curve with V_{DS}=10V as in the equation (3-1)

$$S.S. = \left[\frac{\partial \log_{10} I_{DS}}{\partial V_G} \right]^{-1}$$

(3-1)

Both ZnO and MZO TFTs have the same threshold voltage of 3.5 V. The MZO TFT exhibits higher μ_{FE} of 30 cm^2/V-s and smaller S.S. value of 0.57 V/decade while the ZnO TFT shows μ_{FE} of 25 cm^2/V-s and S.S. of 0.79 V/decade. Since all TFTs were built on the same common Si bottom gate and dielectric layers, it could be assumed that the differences of μ_{FE} and S.S. values between the two different TFT mainly resulted from the different bulk trap densities. If we assume bulk defects is much more than interface defects, the maximum bulk trap density (N_{BS}) of the channel can be extracted from the S.S [50] as in the equation (3-2):

$$S.S. = \ln 10 \times \frac{kT}{q} \left[1 + q \frac{tN_{BS}}{C_{ins}} \right]$$

(3-2)

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, t is the thickness of the channel, and C_{ins} is the capacitance of the insulator. N_{BS} of ZnO TFT is 4.81 x 10^{17} cm^{-3} which is higher than 3.36 x 10^{17} cm^{-3} MZO TFT.

Several material characterizations were conducted to analysis the impact of a small amount of Mg in the ZnO. First, the XPS was utilized to analyze the concentration of oxygen vacancies in the films. In Figure 3.3 (a), it shows that O_{1s} peaks in XPS spectra of ZnO and MZO thin films. Gaussian fitting is used in the deconvolution of these O_{1s} peaks. The peak at the lower binding energy ~530 eV (O_I) is attributed to O^{2-} ions located in a stoichiometric wurtzite ZnO structure. The other peak at the higher binding energy ~532 eV (O_{II}) is related to O^{2-} ions in "oxygen deficient" ZnO which could be the oxygen vacancies. The ratio of two areas (O_{II}/O_{tot}) indicates the relative quantity of this oxygen-related defect. By alloying 3% Mg into the ZnO thin film, MZO showed smaller quantity of oxygen-related defects (15.6%) in comparison with ZnO (19.3%).

We also used the FIB to prepare the samples for TEM characterization, so the impact of the addition of a small amount of Mg into ZnO on the variation of grain size can be evaluated. AFM experiments were also conducted to evaluate the impact on the surface roughness. The results are presented in the Figure 3.3 (b) and (c). In the TEM images, the ZnO and MZO films have the similar grain size around 30nm. The density of grain boundary of the two materials is essentially the same. The AFM results also show that the ZnO and MZO films have very similar surface roughness. From the XPS analysis and the TEM/AFM imaging, we can conclude that the addition of a small percentage Mg into ZnO film doesn't change the film structure significantly but does suppress the oxygen vacancies significantly.
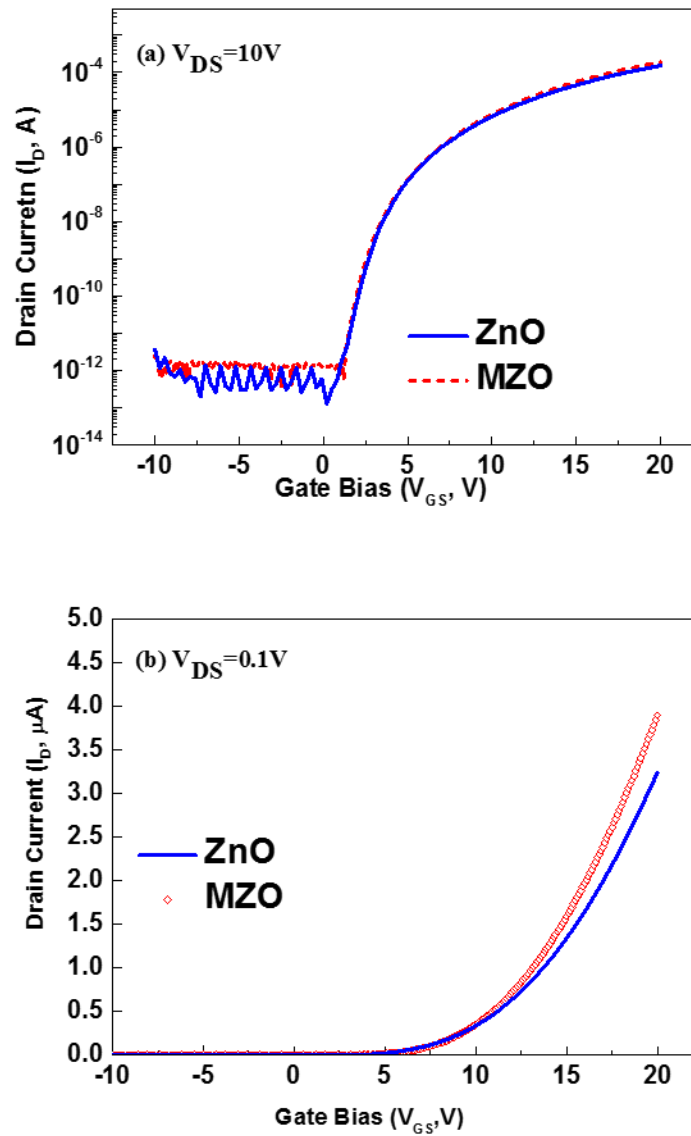
Figure 3.2 I_{DS}-V_{GS} transfer characteristics of ZnO and MZO TFTs (a) at high drain

bias condition (V_{DS} =10V), (b) at low drain bias (V_{DS} =0.1V).

(a) XPS Result

ZnO

O_{II} 19.3% O_I 80.7%

Intensity [a.u.]

MZO

O_I 84.4%

O_{II} 15.6%

534   532   530   528   526

Binding Energy [eV]

(b) TEM

SiO₂

ZnO

Pt

10 nm

SiO₂

MZO

Pt

5 nm

(c) AFM

ZnO

rms=2.70 nm

MZO
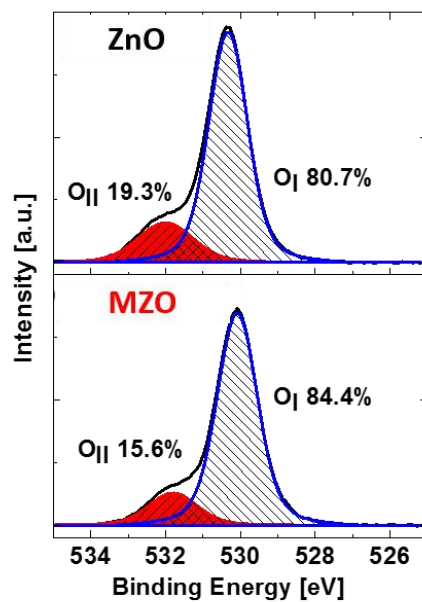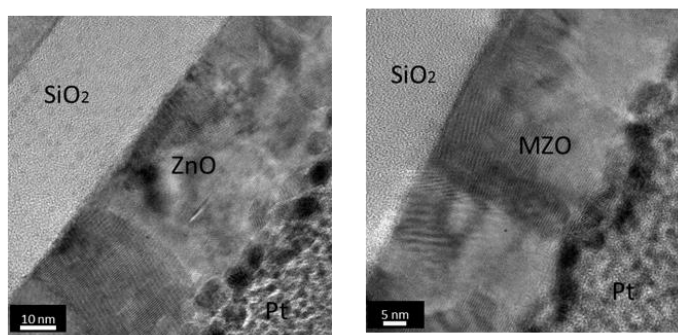
rms=2.90 nm
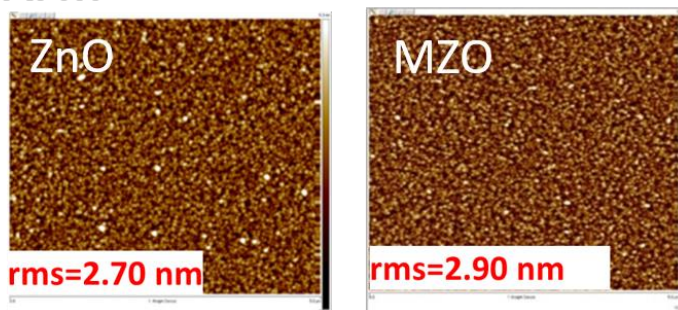
Figure 3.3 (a) XPS spectra[49] (b) TEM pictures, and (c) AFM pictures of pure ZnO and MZO channel layers.

3.4. Negative Bias Stress (NBS) Stability Result

As mentioned in the 3.1, the blocking voltage testing of HVTFT operates in the OFF state, so a good negative bias stress (NBS) stability is essential to HVTFTs for solar invertor. During NBS testing, a constant voltage of -20V was applied to the gate electrode to ensure a uniform electrical field (4 MV/cm) distribution along the channel layer while source/drain contacts were grounded ($V_D= V_S =0V$). The total amount time of NBS testing was 7,200 sec. Figure 3.4 (a) and (b) present transfer characteristics for MZO and ZnO TFTs with $V_{DS}=10V$ under NBS testing, respectively. Negative shifts of threshold voltage are observed with different bias stress times (t_{NBS}) for MZO and ZnO TFTs. NBS instability is defined as the change of threshold voltage (ΔV_{TH}) after NBS testing. After $t_{NBS}=7,200$ sec, MZO TFT had -1.21 V shift in threshold voltage which is only 30% of the shift in ZnO TFT ($\Delta V_{TH} =-3.56$ V). In the meantime, the *S.S.* value of MZO TFT changed from 0.57 V/decade to 0.82 V/decade, and the *S.S.* value of ZnO TFT degraded from 0.79 V/decade to 0.96 V/decade. Moreover, ZnO TFT shows anomalous hump after NBS, and the hump became more serious in longer stress time. On the contrary, there was no hump shown in MZO TFT after $t_{NBS}=7,200$ sec. The NBS result showed that MZO TFT had a better NBS stability than ZnO TFT did, so MZO channel material is more preferred to be used for the HVTFT.
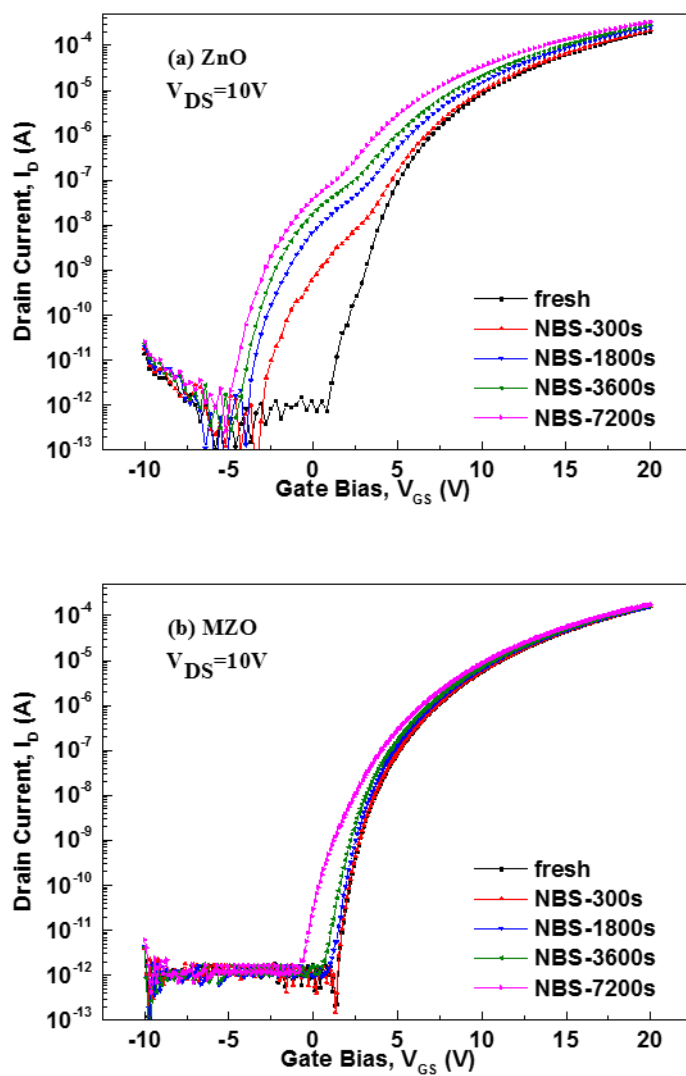
Figure 3.4. I_{DS}-V_{GS} transfer characteristics of ZnO and MZO TFTs (a) in the saturation region (V_{DS} =10V), (b) in the linear region (V_{DS} =0.1V). [51]

To have a further understanding in NBS result, the stretched-exponential model [52] is used to fit the shifts of threshold voltages (ΔV_{TH}) with respect to t_{NBS} as shown in Figure 3.5. The stretched-exponential equation is defined as in the equation (3-3)

$$\left|\Delta V_{TH}\left(t\right)\right| = \Delta V_0\left[1 - \exp\left(-\frac{t_{NBS}}{\tau}\right)^{\beta}\right]$$

(3-3)

where ΔV_{TH} (t) represents the threshold voltage shift induced by bias stress, ΔV_0 is effective voltage drop across the gate dielectric layer, and β is the stretched exponential exponent. The τ is the characteristic trapping time for carriers, and it's related to the average effective energy barrier that carriers in conducting channel needed to overcome before they can enter the insulator or near interface region.

The extracted β values of the two devices are: β~1 for the MZO TFT and β =0.53 for the ZnO TFT. The β value represents the distribution of time constants of the trapping process, so it indicates the width of involved trap distribution. A larger β value in the MZO TFT means that its trap distribution is more uniform than that of ZnO TFT [53]. In comparison with 7.49 x 10^4 second of ZnO TFT, the larger τ of MZO TFT (1.19 x 10^5 second) suggests that MZO has fewer charges trapping during NBS than ZnO TFT does.
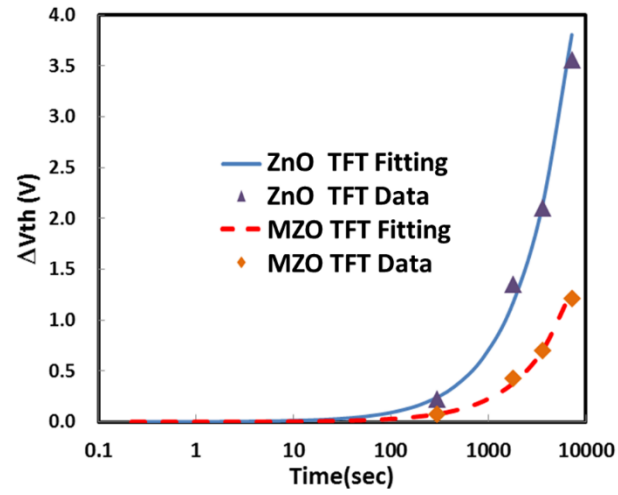
Figure 3.5. The threshold voltage shift ΔV_{TH} versus the stress time. The testing results are fitted based on the stretched exponential equation. [51]

3.5. Discussion

Figure 3.6 (a)-(d) depict the energy band diagrams of ZnO and MZO TFTs in "fresh" and "under NBS" states. In the "fresh" state, the fermi level of the channel is close to conduction band minimum (CBM). Since most oxygen vacancies are neutral and located near valance band maximum (VBM)[54,55], they have little effect on the electrical performance. As indicated in the 3.3, MZO TFT has fewer oxygen vacancies than ZnO TFT does because of higher Mg-O bonding energy. Therefore, as shown in the schematic Figure 3.6 (a) and (b), the ZnO TFT has more neutral oxygen vacancies.

During NBS, the gate negative bias depletes the channel. Because the upright band bending in the depletion region, the fermi level moves close to VBM. This results in the reduction of the formation energy of ionized oxygen vacancies (V_o^{2+}). Furthermore, the ionization from V_o to V_o^{2+} causes outward relaxation of neighboring Zn atoms which increases the energy barrier for returning the initial position [56], leading to the stabilization of V_o^{2+}. As shown in the Figure 3.6 (c) and (d), ionized oxygen vacancies are generated in both MZO and ZnO TFT. Because the intrinsic difference in neutral oxygen vacancies, there are more ionized oxygen vacancies created in ZnO TFT than in MZO TFT during NBS.

These positively ionized oxygen vacancies are attracted to the negative bias. Therefore, some ionized oxygen vacancies in the bulk of channel layer migrate toward the channel/gate dielectric interface during NBS. The migration of oxygen vacancies involves in that a nearest-neighbor oxygen atom in the oxygen lattice jumps into the original vacant site leaving a vacancy behind. The calculated

migration energy barrier for V_o^{2+} is 1.7 eV and for V_o is 2.4 eV, making V_o^{2+} more mobile under an electric field [57]. The migrated ionized oxygen vacancies can be trapped near channel/dielectric interface. The trapped ionized oxygen vacancies can attract extra free carriers in the channel. As a result, the threshold voltage shifts negatively after NBS.

Moreover, these defects related ionized oxygen vacancies (V_o^{2+}) are donor-like type and located above midgap and near the conduction band minimum[54,55], so the electrons trap/de-trap from these defects affect the subthreshold swing of TFT. Therefore, ZnO TFT with more defects has more serious degradation in S.S. than MZO does after NBS. Also, The hump in the subthreshol region is only observed in ZnO TFT. This hump is analyzed as donor-like defects at intermediate energy levels from the conduction band[50], can it can be also linked to the ionized oxygen vacancies.

The "loosely bound oxygen" in ZnO TFT indicates lower energy requires for the ionization and migration of oxygen vacancies. As shown in the Figure 3.3 (a), XPS results indicated that a small Mg composition introduced into the ZnO channel layer would strengthen the atomic bonding [49] of oxygen, so the oxygen vacancy related defects (loosely bound oxygen) are reduced. In consequence, in comparison with ZnO TFT, a smaller negative shift of threshold voltage and hump-free transfer characteristics are observed in MZO TFT.
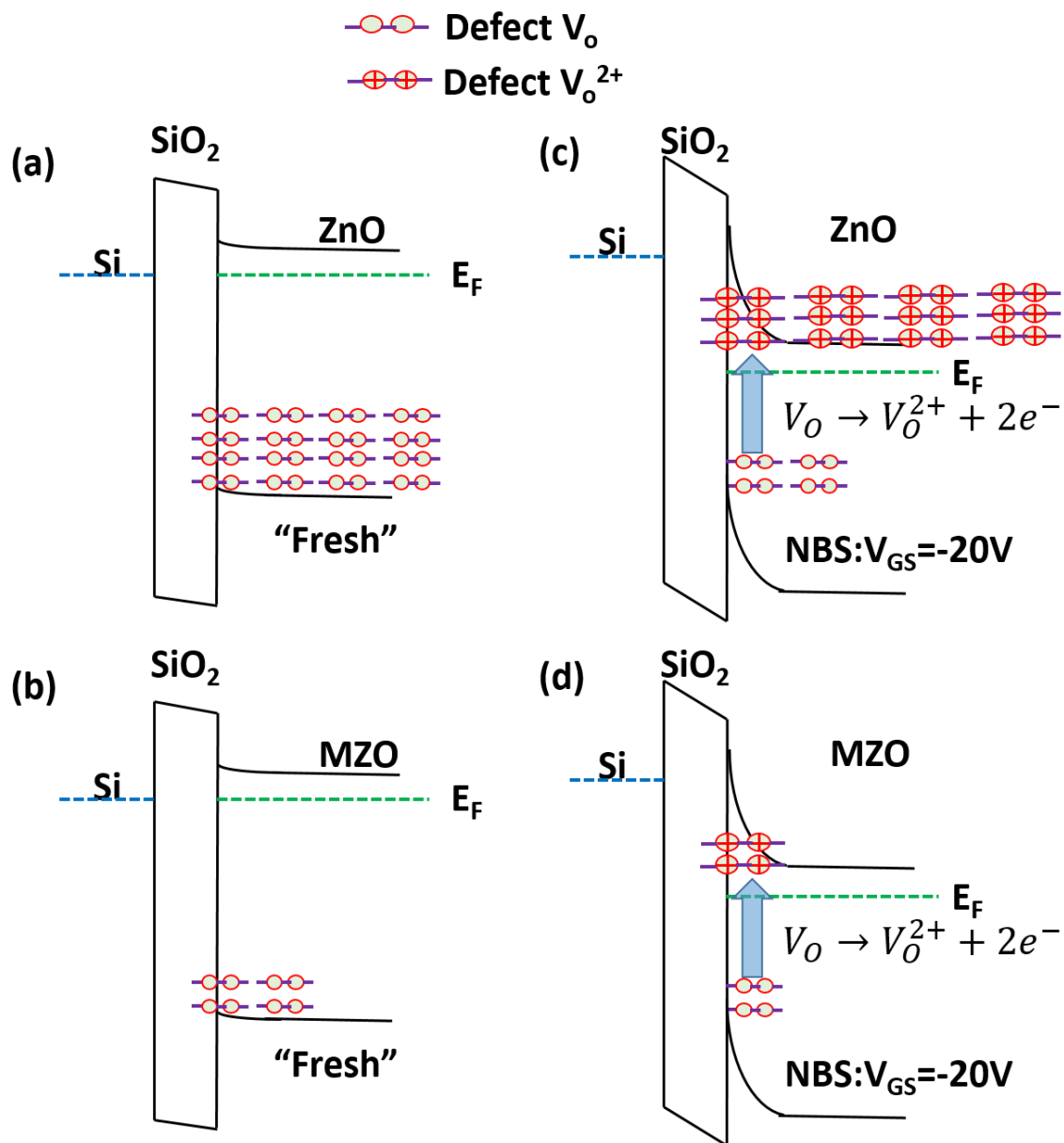
Figure 3.6. The schematic energy band diagrams of a ZnO TFT (a) at fresh state, (b) under NBS; and of an MZO TFT (c) at fresh state, and (d) under NBS. The neutral oxygen vacancies are ionized and migrate to the channel/dielectric interface during NBS.

3.6. Summary

In this chapter, we justified the importance of stability of TFTs for the applications of solar inverters and elucidated that the high density of oxygen vacancies could be the root cause of instability of ZnO TFTs. The addition of a small amount of Mg into ZnO layer was studied to suppress the formation of oxygen vacancies. The material analysis showed that MZO films kept similar surface morphology and grain size with ZnO film; however, the density of oxygen vacancies was reduced. The electrical analysis showed that MZO TFTs have slightly better electrical characteristics, such as on-current, subthreshold swing than ZnO TFTs do. In term of NBS stability, MZO TFTs had significant advantages over ZnO TFTs. A 30% less in shift of threshold voltage, hump-free and smaller degradation of subthreshold swing were obtained for the MZO TFT than that of the ZnO TFT. MZO TFTs provided a superior and more stable electrical characteristics than ZnO TFTs do. As a result, MZO TFT technology established a solid foundation for the development of high voltage applications.

Chapter 4 MZO HVTFTs on Glass

4.1. Background

Because of the transition temperature of regular glass is around 666°C, the low process temperature of the TFT technology is more suitable than that of the Si-based metal–oxide–semiconductor field-effect transistor (MOSFET) and SiC/GaN high power transistors technologies. Also, the lower fabrication cost of the TFT technology is preferred to provide low cost energy (dollar/Watt) which critically affects the popularity of energy technology. Compared to popular Si-based TFTs, ZnO TFTs have several advantages for PV-SOG, such as a transparent channel material, better balance between electrical performance and uniformity, and wide bandgap materials. To solve the intrinsic issue of electrical stability in ZnO TFTs, in Chapter 3 we demonstrated using MZO film to replace pure ZnO film as channel layer to suppress the formation of oxygen vacancies. Therefore, MZO TFTs showed better electrical stability than ZnO TFTs. As an Indium-free oxide semiconductor TFT technology, MZO TFTs technology showed great potential to be applied in PV-SOG at low fabrication cost.

4.2. Design of HVTFTs on Glass

4.2.1. Overall design of HVTFTs on glass

To develop HVTFTs on glass, there were several critical adjustments which were different from regular TFTs used in Chapter 3. First of all, the device structure requires an extra region to sustain high voltage bias. Among the HVTFT structures mentioned in Chapter 2, the simple structure of drain and source offsets was

chosen. It can provide an un-gated region for high voltage operation without adding extra masks or process steps. Secondly, in order to eliminate electric field crowding in conventional rectangular channel, the symmetric channel was designed. Thirdly, in order to replace the high temperature thermal oxidation, PECVD was used to deposit SiO_2 dielectric layer.

4.2.2. Symmetric Structure

For major applications of TFT technologies, such as display technologies, the TFTs have the rectangular channels which is similar to the CMOS. However, the rectangular design would introduce non-uniform electrical field distribution with the highest field located at the corners of the channel, which limits the blocking voltage of the devices. To solve this problem, a symmetric structure was designed as shown in Figure 4.1. The circular structures included the bottom gate, channel layer, and source/drain electrode. By removing the corners in the rectangular shape, the electrical field crowding at the corner area in the channel was eliminated.

In order to further understand the benefits of adoption of circular structures, SILVACO 3D Victory software was used to simulate the electrical field distribution in the channel of TFT devices with and rectangular in Figure 4.2a and circular in Figure 4.2b configurations, respectively. For fair comparison, both configurations have the equivalent channel length (L=10 μm), gate-to-drain offset (L$_{GD}$=5 μm) and gate-to-source offset (L$_{GS}$=3 μm). The fabrication processes are exactly the same, such as the dielectric thickness, channel thickness, materials. The bias conditions are identical. (V$_{GS}$=-20V, V$_{DS}$=90V) As shown in Figure 4.2d, at OFF state of high voltage operation, the electrical field crowding occurs on the drain side around the

corner of the rectangle where the maximum field reaches over 2,800 kV/cm. This becomes the weak point where the breakdown of TFT happens. On the contrary, the field distribution in the circular structure as shown in Figure 4.2c is uniform from drain to source, and the highest field is only 1,420 kV/cm, which is approximately 50% less than in the rectangular counterpart. It shows that the symmetric design of a circular structure removes the severe electrical field crowding around the corners of a rectangular channel. Therefore, the HVTFT with the circular structure is able to work at a higher bias voltage and offers a higher blocking voltage over the regular rectangular configuration.
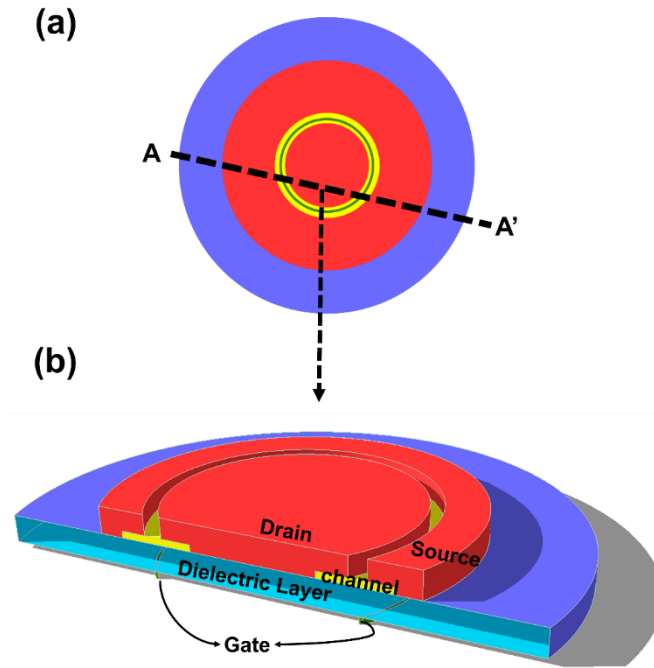
Figure 4.1. Schematic diagrams of an MZO HVTFT with a circular structure are shown: (a) the top view and (b) the three-dimensional cross-sectional structure along A-A' in (a).
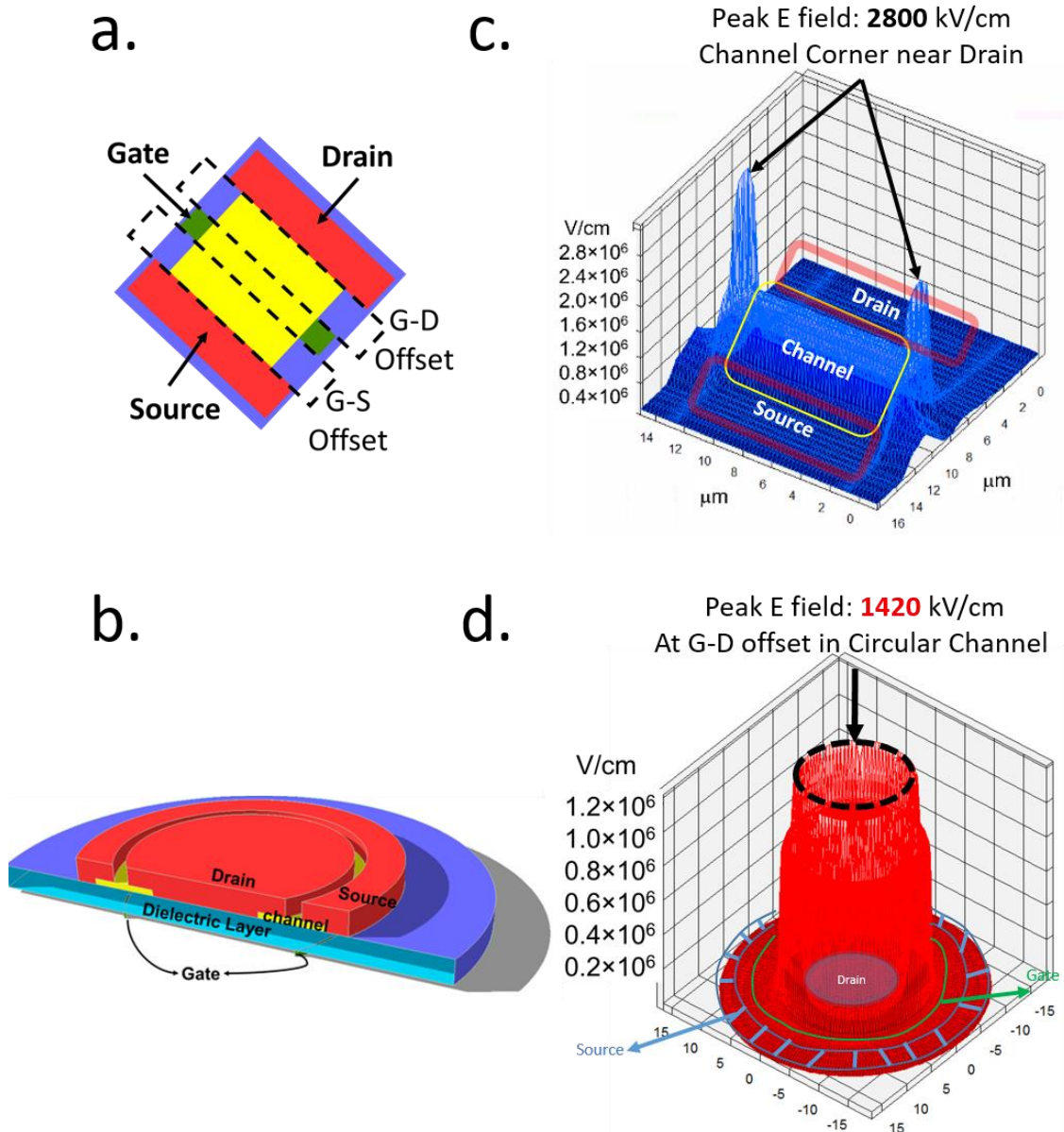
Figure 4.2 Top view of (a) an HVTFT with a rectangular structure and (b) an HVTFT with a circular structure. Simulation results of the electrical field distribution in the TFT channel (c) with a rectangular structure and (d) with a circular structure.

4.2.3. Fabrication Process of HVTFTs

The HVTFTs were fabricated on 0.4mm thick commercial glass substrates as shown in Figure 4.3a, and the pictures of the circular structure were shown in Figure 4.3b and c. As shown in the inserted table, the channel lengths/ gate-to-drain offset lengths are 10/5 µm, 15/10 µm, and 25/20 µm for nominal, longer, and longest HVTFT, respectively. The gate-to-source offset is kept the same of 3 µm. The detailed process steps are illustrated in Figure 4.4. A 50 nm chromium (Cr) layer was deposited by DC sputtering (Ar gas, P=5 mTorr, 300W, room temperature, deposition rate~2.3 Å/second). The Cr layer was patterned by using a dry etching process (Oxford C, ICP power 600W, RF power 10W, Cl_2=47 SCCM + O_2=3 SCCM, P=10 mTorr, T=50°C) to serve as the bottom gate electrode. Then, a 200 nm SiO_2 layer was deposited by PECVD (Trion PECVD, ICP power 60W, N_2O=100 SCCM + N_2=100 SCCM+ SiH_4=86 SCCM, P=900 mTorr, T=400°C, Deposition rate~2nm/second) as the gate dielectric layer. Following the SiO_2 deposition, the channel was deposited using metal organic chemical vapor deposition (MOCVD) at 400°C. DeZn (diethyl zinc) and MCp2Mg (bis (methylcyclopentadienyl) magnesium) were used as the precursors for Zn and Mg, respectively. Three types of 40 nm channel layers were deposited on SiO_2: pure ZnO, $Mg_{0.03}Zn_{0.97}O$ (MZO) and $Mg_{0.03}Zn_{0.97}O$ plus a modulation-doped thin layer (m-MZO). In the m-MZO HVTFT, a modulation-doped 10 nm $Mg_yZn_{1-y}O$ transition layer (MZO-TL) was inserted between the MZO channel layer and the SiO_2 dielectric layer, and the Mg composition (y) in the $Mg_yZn_{1-y}O$ TL decreased from the side adjacent to SiO_2 (y=1) to the other side adjacent to the channel (y=0.03).

The channel layers were patterned by the wet etch process, and two-steps procedure was used to prevent the undercut profile. The first step was done by diluted hydrochloric acid (1:2000) 5 seconds, and the diluted acetic acid (1:2000) 35 seconds was the second step. The source and drain metallization (100 nm titanium / 50 nm gold) was deposited using electron beam evaporation, followed by a normal lift-off process. A 1.5 μm photoresist film (AZ-5214) was coated on top of the TFT channel, serving as a passivation layer to prevent ambient absorption/desorption during electrical testing. The VIA opening for contact pad was done by wet etching. (BOE 1:10 120 seconds)
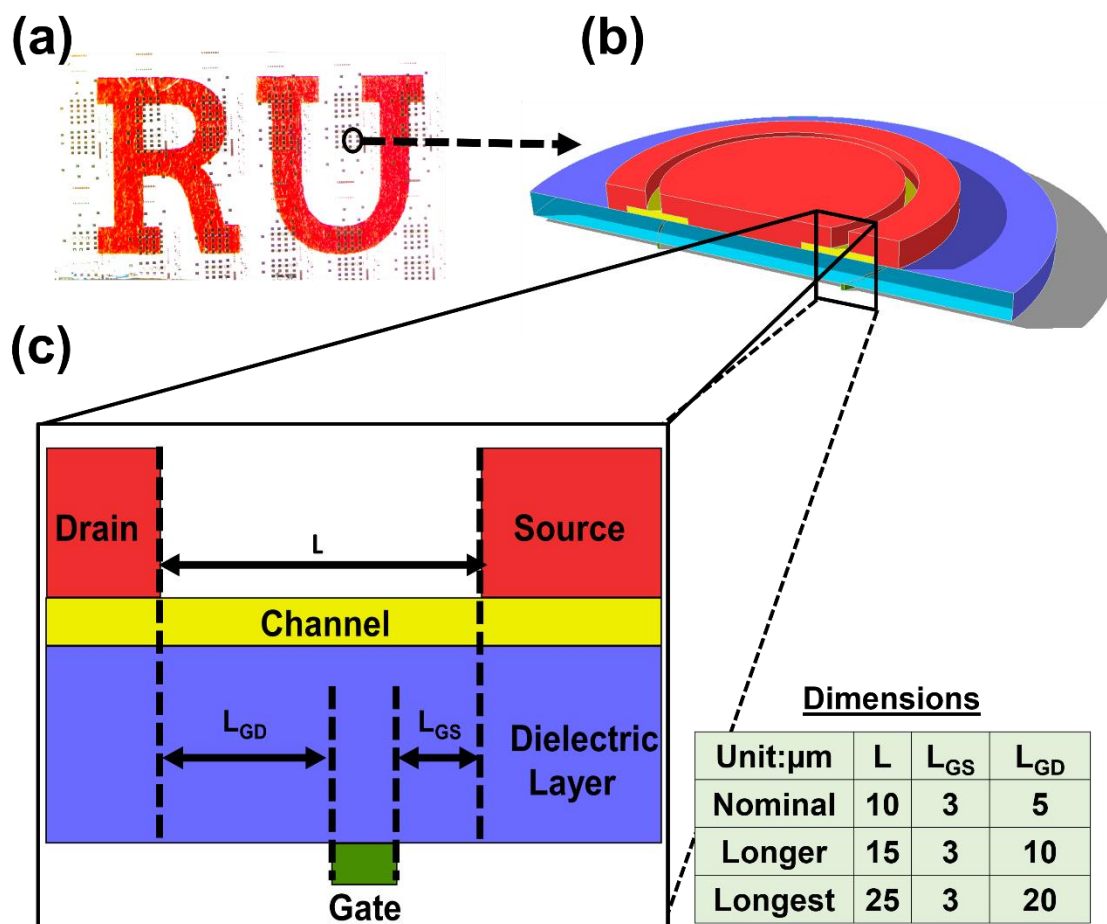
Figure 4.3 (a) A photograph displays the transparent HVTFTs on glass. (b) The cross sectional view, (c) schematic of the layer structure with a table of dimensions, and (d) materials of a ZnO based HVTFT built on glass.

1. Sputtering Chromium 50nm

Cr metal

Glass substrate
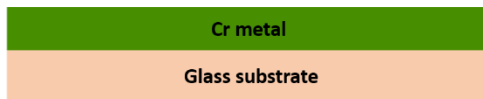
2. Photolithography Pattern (Gate)
& ICP Dry Etch
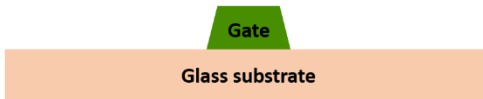
Gate

Glass substrate

3. PECVD SiO$_2$ deposition

PECVD SiO$_2$

Gate

Glass substrate

4. MOCVD ZnO-related deposition

ZnO Related

PECVD SiO$_2$

Gate

Glass substrate

5. Photolithography Pattern & Wet Etch

ZnO Related Channel

Gate

Glass substrate
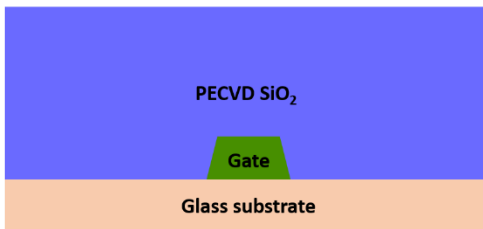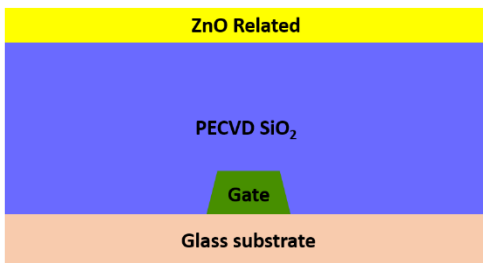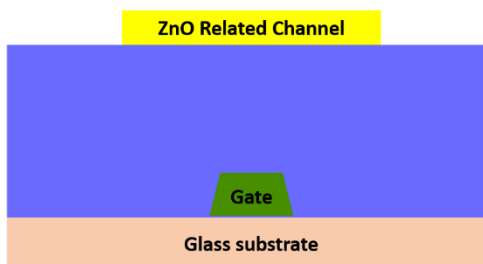
6. Photolithography Pattern (Source/Drain)
Image Reversal for lift-off process

7. E-beam Evaporator
Titanium 100nm/ Gold 50nm

8. Immerse in Acetone for metal lift-off

Ti/Au
Drain

Ti/Au
Drain

ZnO Related Channel

PECVD SiO$_2$

Gate

Glass substrate
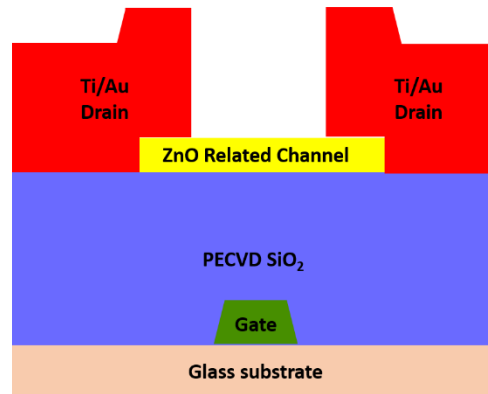
9. Photolithography Pattern (Contact)
Photoresist works as a passivation layer

10. SiO$_2$ wet etch for the gate contact pad

AZ 5214 (Photoresist)

Ti/Au
Drain

Ti/Au
Drain

ZnO Related Channel

PECVD SiO$_2$

Gate

Glass substrate
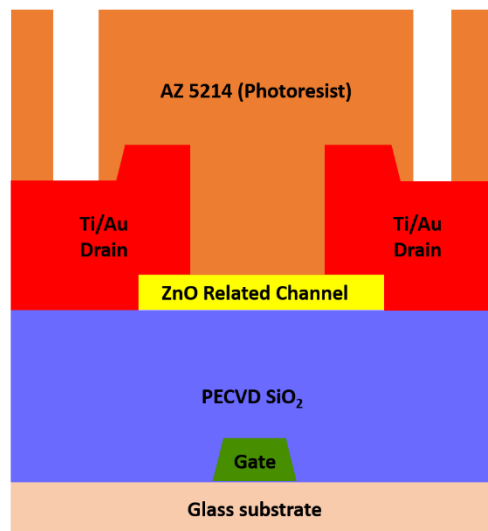
Figure 4.4 The schematics of the HVTFTs process steps.

4.3. Testing of HVTFTs

4.3.1. Testing Setup

The electrical measurements under the low bias were conducted using an HP-4156C with an HP-41501B Pulse Generator. With the boost from the connection of a pulse generator, the maximum voltage of the HP-4156C electrical testing system was limited to be 200V. The system which had a current resolution of 1×10^{-15} A was used for all transfer characteristics. For electrical measurements under high bias (over 200V), a high voltage testing system was built based on a Tektronix 370 with the probe station. As the current resolution of Tektronix 370 only reached 1×10^{-6} A, it was only used for the testing of blocking voltages. In order to avoid problems with arcing and tracking due to environmental conditions, the devices were immersed in Fluorinert FC-40 during the high voltage measurements. The devices showed the same electrical characteristics in air and FC-40 environment. The electrical measurements at different temperatures were conducted using an Agilent 1500B. All measurements were conducted in a light-tight probe station.

4.3.2. Definitions of Electrical Parameters

The threshold voltage (V_{TH}) of HVTFT is defined as the gate voltage value when a drain current (I_{DS}) reaches 10^{-9} A with $V_{DS}=0.1$V. The turn-off voltage (V_{OFF}) is defined as the gate voltage value when a drain current (I_{DS}) reaches 10^{-13} A with $V_{DS}=10$V. The subthreshold slope (S.S.) is extracted from a 3-decades range in the sub-threshold region ($I_{DS}=10^{-13}\sim10^{-10}$ A) of the $\log_{10}$ (I_{DS}) *vs* V_G curve with $V_{DS}=10$V:

$$S.S. = \left[\frac{\partial log_{10}(I_{DS})}{\partial V_G}\right]^{-1} \tag{4-1}$$

The ON-current (Ion) is the drain current while a TFT operates at V_{GS}=10V and V_{DS}=10V. The ON/OFF ratio is obtained by comparing between the ON-current and the lowest current within the gate bias range of -25V to 10V. The blocking voltage is defined as the highest drain bias that a TFT can sustain without a breakdown in the OFF state.

The shifts of threshold voltage in the thermal stability measurement

$$\Delta V_{TH}(ZnO, T) = V_{TH}(ZnO, T) - V_{TH}(ZnO, 300K) \tag{4-2}$$

$$\Delta V_{TH}(MZO, T) = V_{TH}(MZO, T) - V_{TH}(MZO, 300K) \tag{4-3}$$

$$\Delta V_{TH}(mMZO, T) = V_{TH}(mMZO, T) - V_{TH}(m - MZO, 300K) \tag{4–4}$$

4.4. Experimental Results

4.4.1. Transfer Characteristics and Thermal Stability

The transfer characteristics of HVTFTs with three different channel materials and structures are shown in Figure 4.5a, and the data are summarized in Table 4-1. Compared with ZnO HVTFT, MZO HVTFT shows a better subthreshold slope (S.S.) and on-current. The most significant improvement of the MZO over the pure ZnO channel layer is in its thermal stability, which is one of the critical requirements for high voltage devices being integrated into PV-SOGs. By measuring the transfer characteristics of HVTFTs at different temperatures, the shifts of threshold voltage (ΔV_{TH}) are compared in Figure 4.5b. As temperature increases from 294 K (room temperature) to 367 K, MZO HVTFT only shows a threshold voltage shift ΔV_{TH} of

-6 V in comparison to ΔV_{TH} of -10.5 V in the pure ZnO counterpart. This negative shift of threshold voltage at higher temperatures results from the thermally activated electrons from the trap states located in the channel and in the interface between the channel and gate dielectric SiO_2.

In Figure 4.5c, the activation energy of drain currents at different gate biases is extracted from the Arrhenius plot (*ln I_D vs. T^{-1}*) in equation (4-5):

$$I_D = I_{D0}e^{-E_a/k_B T}$$ (4-5)

where *I_{D0}* is the drain current constant, k_B the Boltzmann constant, *T* the temperature in Kelvin, and *E_a* the activation energy of drain current.

If the trap density in TFT is high, the moving rate of the Fermi level with respect to the gate bias from the deep level to the conduction band is roughly inversely proportional to the total trap density. The steeper falling rate (0.177 eV/V) of the MZO HVTFT, as opposed to that of the ZnO HVTFT (0.107 eV/V), indicates that the MZO TFT has a lower trap density. Because both MZO and ZnO HVTFTs are fabricated on the same SiO_2 gate dielectric layer, the interface trap densities of the two devices are similar. Therefore, the improvement of thermal stability in MZO HVTFT over ZnO HVTFT is mainly attributed to the reduction of traps in the bulk channel. In fact, the Mg-O has a stronger bonding than Zn-O[49], resulting in the lower density of oxygen vacancy in the MZO channel than that of the pure ZnO channel.

In the comparison between MZO HVTFT and m-MZO HVTFT, it is found that the later shows an order higher on-current and a steeper S.S. than the MZO counterpart. The steepest falling rate (0.246 eV/V) of the activation energy of the

drain current suggests a nearly 40% lower total trap density in m-MZO HVTFT than in MZO HVTFT. Since both of MZO and m-MZO HVTFTs are made up of the same MZO channel and SiO_2 gate dielectric layer, these differences in characteristics between the two HVTFTs are mainly caused by the different interface properties between the channel and gate dielectric layer. Specifically, the unique interface design and engineering using modulation doping of Mg in m-MZO HVTFT reduces the interface trap density. Therefore, the total trap density in m-MZO HVTFT is lower than in the MZO HVTFT.
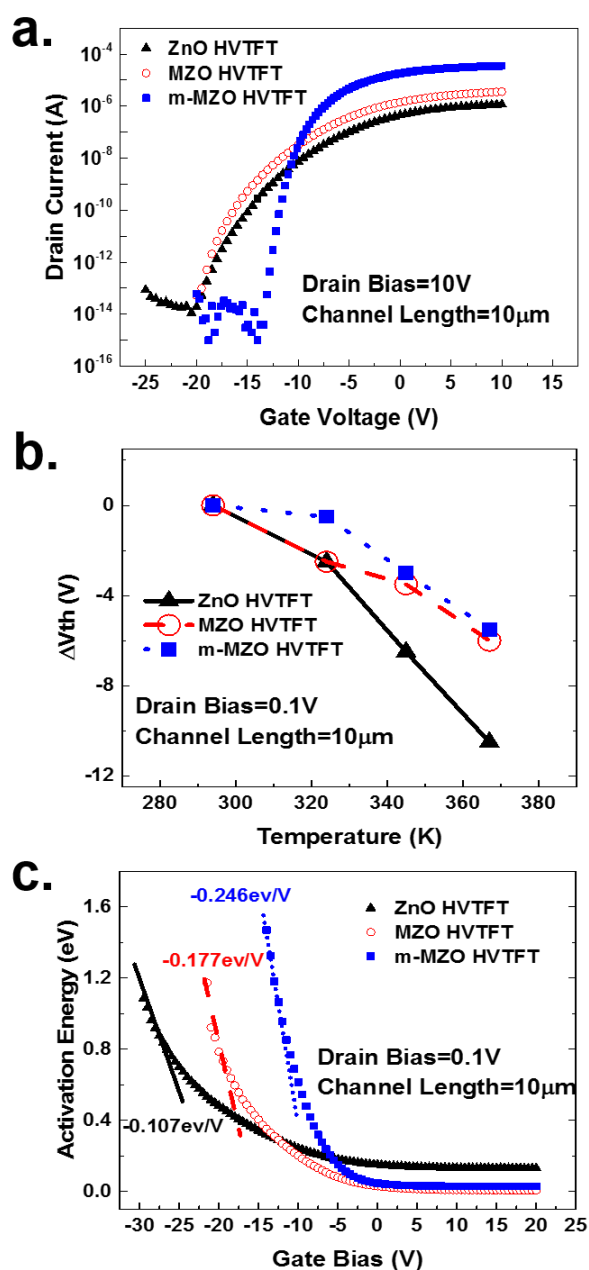
Figure 4.5. The electrical performances of HVTFTs. (a) Transfer characteristics of ZnO, MZO and m-MZO HVTFTs with V_{DS}=10V. (b) The shift of threshold voltage of HVTFTs at different temperatures. (c) The extracted activation energy of drain current as a function of gate bias in HVTFTs.

Channels	On/Off Ratio	V_{OFF} (V)	S.S. (V/Decade)
ZnO	6.1×10^7	-19.0	1.37
MZO	6.7×10^7	-19.0	1.24
m-MZO	3.5×10^{10}	-13.0	0.53

Table 4-1 Electrical characteristics of ZnO, MZO, and m-MZO HVTFTs with the equivalent channel length L=10μm.

4.4.2. High voltage blocking capability

Having the capability of blocking high voltages and operating at high bias conditions reliably are the essential characteristics for the application of high voltage transistors in PV inverters. Since ZnO HVTFT fails to show thermal stability, we here only compare MZO and m-MZO HVTFTs. The results of blocking voltages of MZO and m-MZO HVTFTs with the same channel length (L=10 μm) are shown in Figure 4.6a. The drain leakage current of MZO HVTFT increases abruptly, and the device burns down at V_{DS}=90 V. In contrast, the drain leakage current of m-MZO HVTFT keeps as low as 10^{-12} A even at much higher V_{DS}=200 V (here 200 V is the limitation of HP-4156C used for testing).

A comparison of the transfer characteristics at normal bias (drain bias=10 V) among three m-MZO HVTFTs with different channel lengths is presented in Figure 4.6b. There is a trade-off between blocking capability and driving capability in m-MZO HVTFT. As the channel length increases, the blocking voltage increases; however, the on-current drops. As shown in Figure 4.6c, the values of the blocking voltage/on-current for the nominal (L=10 μm), longer (L=15 μm), and longest (L=25 μm) m-MZO HVTFT are 300 V/3.5×10^{-5} A, 427 V/6.61×10^{-6} A, and 609 V/4.57×10^{-6} A, respectively. The statisical data can be found in section 4.4.3 . The output characteristics of m-MZO HVTFT of L=10 μm are presented in Figure 4.6d. It shows better saturation behavior at low gate bias. At high gate bias, the drain current increases as the drain bias increases. This kink effect was also observed in the IGZO HVTFT[27]. It might be related to the channel length modulation induced self-heating effect[27,58].

For the high voltage circuit, the ideal case is that high drain bias only happens at OFF state. However, it is possible that the devices turn on accidentally before the decrease of drain bias. Therefore, the immunity toward high drain bias at ON state is also a important factor of a robust system. The m-MZO HVTFTs with channel length of 10, 15, and 25 μm have the highest operating drain bias of 70, 110, and 200 V as shown in Figure 4.7a, b, and c, respectively. The maximum drain voltage without degrading the on-current defines the highest operating drain bias of each HVTFT, except for the case of 25 μm which only shows 200 V due to the limitation of the testing equipment. Under these high drain bias conditions, all m-MZO HVTFTs show a high on/off ratio of more than 10^7, and the V_{OFF} and off-current almost constant at any drain bias condition. Theses features indicate that m-MZO HVTFTs are stable even under high bias conditions.The m-MZO HVTFT of 25 μm can operate at drain bias of 200V with a blocking capability over 600 V, suitable to be used as an inverter of PV-SOG. The comparison of m-MZO HVTFTs with different channel lengths are summarized in Table 4-2.
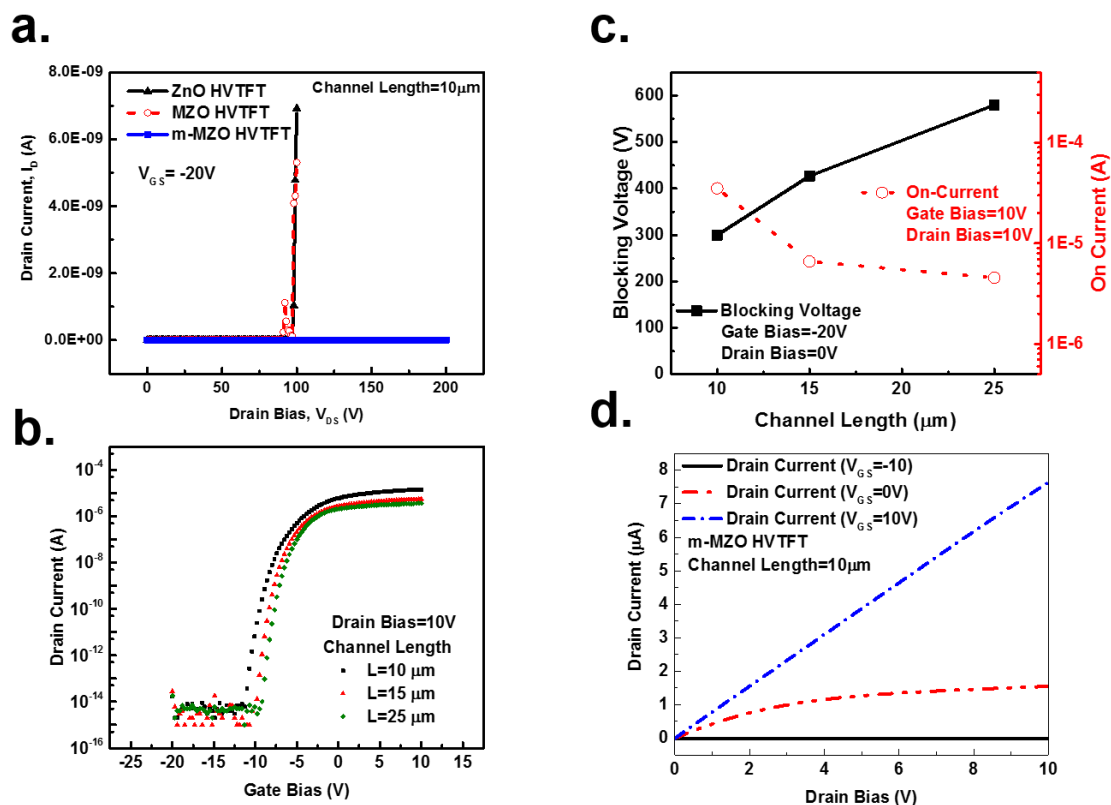
Figure 4.6. The electrical performances at high bias conditions and the blocking capabilities of HVTFTs: (a) drain leakage current of off state in ZnO, MZO and m-MZO HVTFTs; (b) transfer characteristics of m-MZO HVTFTs with different channel lengths, (c) the channel length dependence of blocking voltage and On current, and (d) the output characteristics of m-MZO HVTFT with a channel length L= 10 μm.
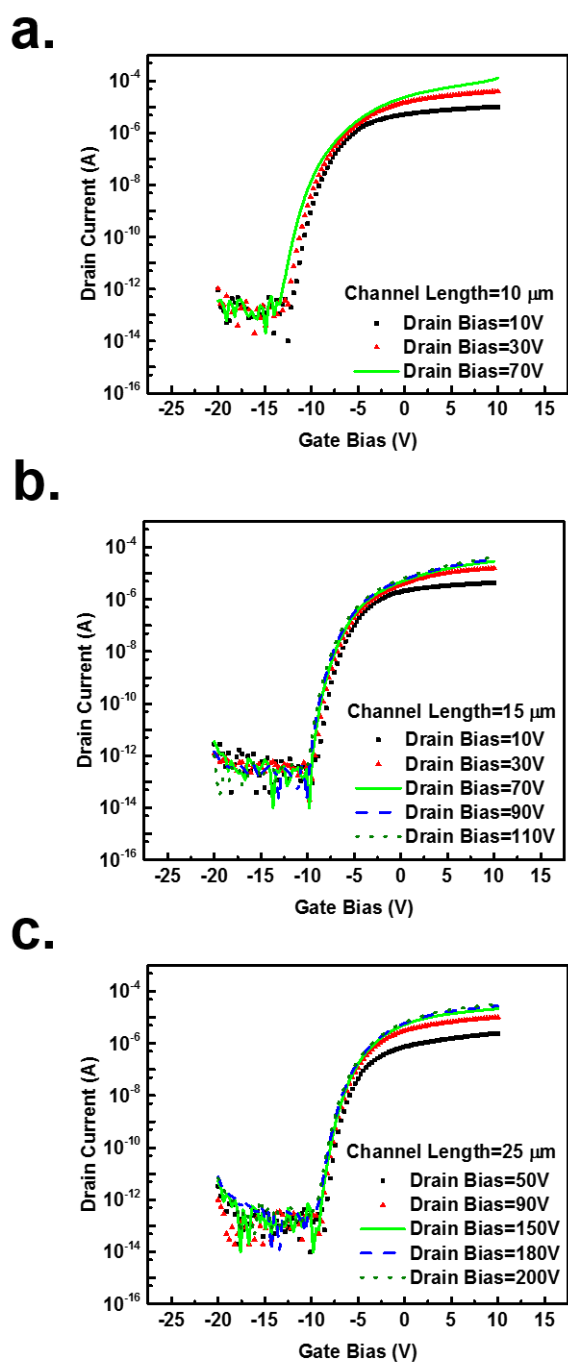
Figure 4.7. The transfer characteristics at high bias conditions of m-MZO HVTFTs with a channel length (a) L=10, (b) 15, and (c) 25 μm, respectively.

L(μm)	Ion (A)	Blocking Voltage(V)	Maximum Drain Current (A)
25	3.3×10^{-6}	609	3.2×10^{-5} (at V_{DS}=200 V*)
15	5.8×10^{-6}	447	3.0×10^{-5} (at V_{DS}=110 V)
10	3.5×10^{-5}	305	1.3×10^{-4} (at V_{DS}=70 V)

*instrument limit

Table 4-2 Voltage-blocking capabilities and output characteristics of m-MZO

HVTFTs with three different channel lengths (L=10μm, 15μm, 25μm)

4.4.3. Statistical Data of Electrical Performance

The statistics of electrical performances of m-MZO HVTFTs are presented in Figure 2.1, including (a) on-current, (b) off-current, and (c) blocking voltage. The data show the trade-off between blocking voltage and on-current; furthermore, such trade-off is directly affected by the offset length. The dominate factor of the variation in data is attributed to the device processing issues, especially the mask misalignment in the photolithorgraphy process of the ring-structures. Such variation could be suppressed by refining the photo-mask design and using a better alignment tool. It is noticed that the variation of the off-current (Figure 2.1b) is larger than that of on-current (Figure 2.1a). This is due to much smaller values of the off-current which are close to the measurment limit of the instrument system.
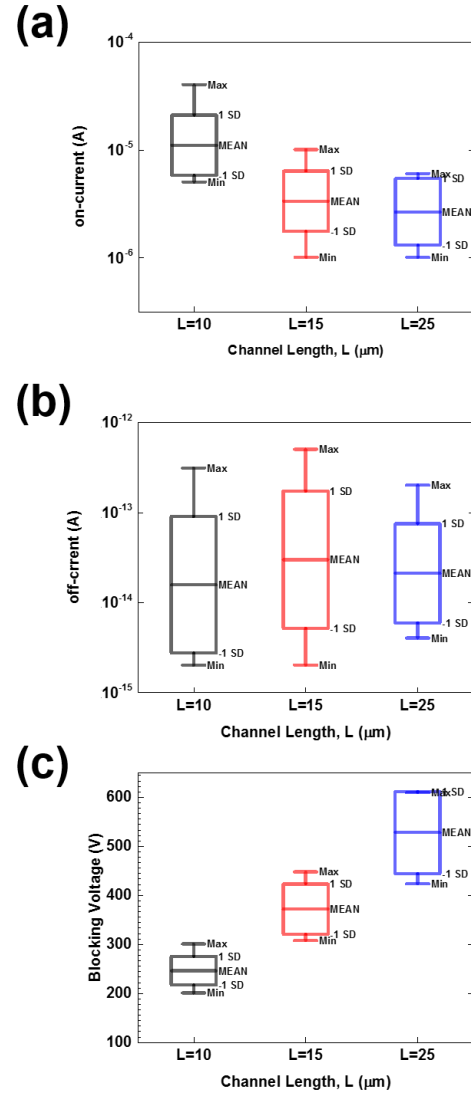
Figure 4.8. The statistic data of (a) on-current, (b) off-current , and (c) blocking voltage of the m-MZO HVTFTs with three different channel lengths (L = 10, 15, and 25 μm). The error bar provides mean , maximum (Max), minimum (Min), plus one standard deviation (1SD) and minus one standard deviation (-1SD) values. The numbers of data points are taken from 25 , 25, and 15 devices with the channel length of 10, 15, and 25 μm.

4.5. Discussion

4.5.1. The effect of interface engineering on electrical performance

The interface engineering using a modulation-doped thin MZO transition layer (MZO-TL) in the m-MZO HVTFT improves transfer characteristics, thus enables high voltage blocking capability. Such improvements are mainly attributed to the prevention of Zn diffusion into the SiO_2 dielectric layer. Zn could diffuse as ions, such as Zn^{2+} into the dielectric layer and then become the fixed charges in SiO_2. Because the positive Zn^{2+} trapped inside SiO_2 would attract electrons, it requires an extra negative gate bias voltage to deplete the channel. As a result, MZO HVTFT, which has extra diffusion of Zn^{2+} into SiO_2, has more negative V_{OFF} than m-MZO HVTFT does. Moreover, the out-diffusion of Zn from the MZO channel layer would generate Zn-related defects, such as Zn vacancies and Zn interstitials in the MZO channel layer, especially near the MZO/SiO_2 interface, thus degrading the electrical performance of transistors. The total trap density from the subthreshold slope (S.S.) can be estimated in the equation (4-6)[59]:

$$S.S = \log_e 10 \times \frac{k_B T}{q} \left(1 + q \frac{t N_{bulk} + D_{it}}{C_G}\right) \qquad (4\text{-}6)$$

where q is the elementary electric charge, k_B the Boltzmann constant, T the temperature in Kelvin, t the channel thickness, N_{bulk} the bulk trap density, D_{it} the interface trap density, and C_G the capacitance per area of the gate dielectric layer (C_G is 1.73×10^{-4} F/m^2 and 1.69×10^{-4} F/m^2 for MZO and m-MZO HVTFT, respectively. The theoretical values of SiO_2=3.9 and MgO=9.90[60] are used in estimation). The S.S. of MZO and m-MZO HVTFT are 1.24 V/decade and 0.53

V/decade respectively. The total trap density includes the bulk trap (tN_{bulk}) and the interface trap (D_{it}), which are calculated to be 2.14×10^{12} cm^{-2} and 8.36×10^{11} cm^{-2} for MZO and m-MZO HVTFT, respectively. Since the channel material is the same, the difference in the total charge density between HVTFT and m-HVTFT is approximately equal to the reduction of the interface trap density, which is 1.3×10^{12} cm^{-2}. By adding a modulation doped transition layer into the m-MZO HVTFT, Zn diffusion into the SiO_2 dielectric layer is significantly suppressed. (The detailed analysis of MZO-TL is covered in the Chapter 5.) The interface engineering successfully adjusts the threshold voltage V_{TH} close to 0 V and makes the S.S. steeper than that of MZO HVTFT.

4.5.2. Effect of interface engineering on blocking voltage

The addition of the MZO-TL also enables the higher blocking voltage. The ideal breakdown field of a pure MgO is 12 MV/cm[61]. Although the effective thickness of the dielectric layer increases by adding the MZO-TL, a 10 nm MZO transition layer can not provide more than 12 V of the blocking voltage. Furthermore, the gate leakage current keeps at a similar level in both HVTFTs after the breakdown at high drain bias. Therefore, the significant enhancement of the blocking voltage in m-MZO HVTFT cannot be attributed to the extra voltage drop on the MZO-TL. In order to understand the fundamental cause of the improvement in blocking voltage, SILVACO Atlas software was used to simulate the electric field distributions in the two different devices. As drawn in the Figure 4.9a and b, MZO HVTFT possesses extra positive oxide charges in comparison to m-MZO HVTFT.

The amount of the extra equivalent oxide charges per unit area (Q_{OX}) is estimated based on the equation (4-7):

$$Q_{OX} = -\Delta V_{OFF} \times C_G \tag{4-7}$$

where C_G is the capacitance per area of the gate dielectric layer. The difference in V_{OFF} between MZO and m-MZO HVTFT is around -6V, so the extra 6.47×10^{11} cm^{-2} of positive charges are placed in the MZO HVTFT. Figure 4.9a shows the case of MZO HVTFT of 9.6×10^{11} cm^{-2}, and Figure 4.9b represents the case of m-MZO HVTFT of 3.13×10^{11} cm^{-2}. Except the different charge density of charge sheet in the dielectric layer, two devices are identical. The bias conditions are also the same of gate bias=-20V and drain bias=90V. The low drain bias is to keep both MZO and m-MZO HVTFTs still functional.

To focus on the most critical area where the peak electrical field locates, we draw a cutline across the simulation figure as indicated in Figure 4.9c. By comparing the electrical field distribution along the cutlines, the impact of oxide charges near the interface on electrical field distribution in the device can be displayed as shown in Figure 4.9d. The maximum values of the electrical field near the interface are 1,520 kV/cm and 1,410 kV/cm for MZO and m-MZO HVTFT, respectively. The reduction of the maximum electrical field allows m-MZO HVTFT to operate at higher drain bias, enabling higher blocking voltage. Overall, the MZO-TL in m-MZO HVTFT acts as a barrier against Zn diffusion so that the interface states and trapped charges are reduced. This improvement leads to the decrease of the maximum electrical field near the channel-gate dielectric interface, resulting in the increase of the blocking voltage.
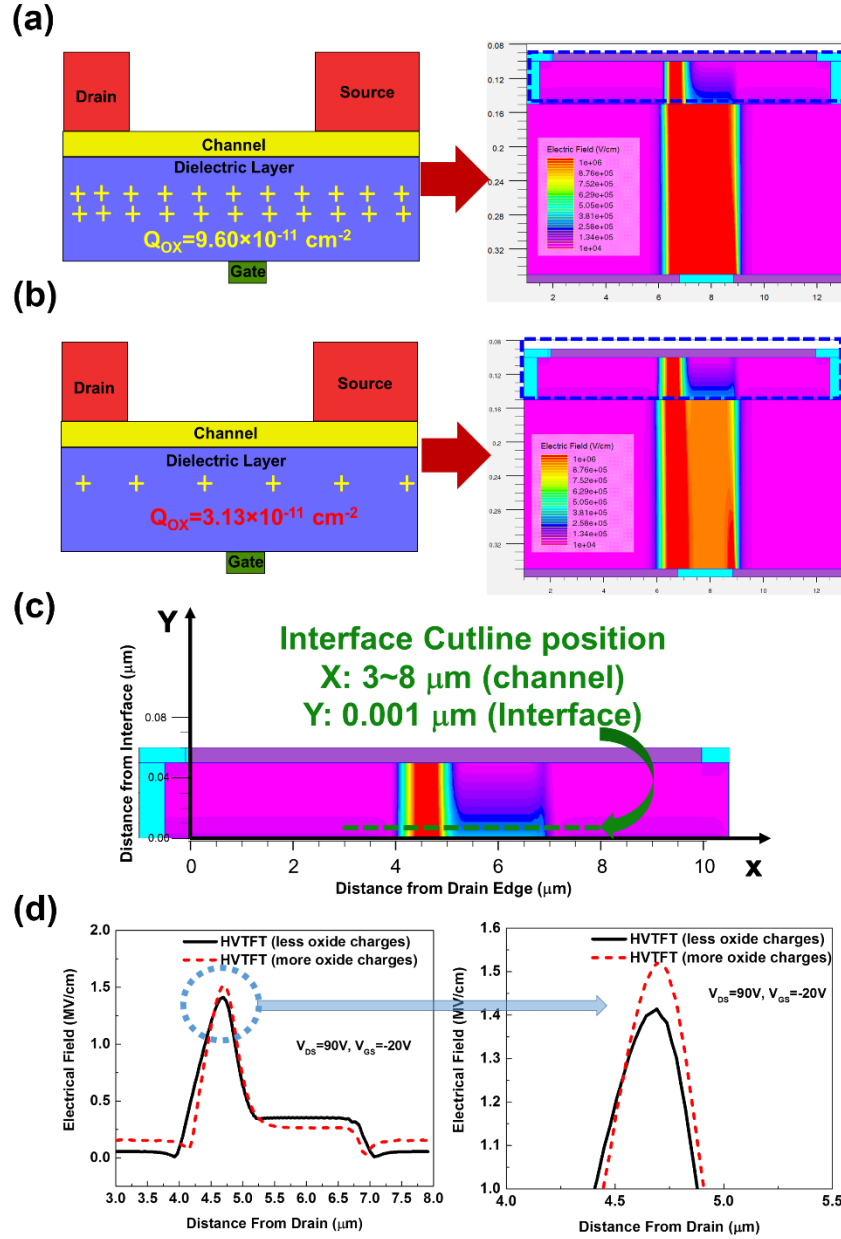
Figure 4.9. Schematic diagrams of different interface designs and layer structures of (a) MZO and (b) m-MZO HVTFT, respectively. (c) The location of cutlines is near the interface of channel/gate dielectric and above the gate edge where the maximum electrical field locates. (d) A comparison of the electrical field of MZO HVTFT and m-MZO HVTFT along the cutlines.

4.5.3. Analysis of localized electrical field in gate connection area

In the ring configuration, a contact pad is needed to connect the gate as shown in Figure 4.10(a). The electrical field in the gate connection area is different from the other area in the ring. In order to analyze the influence of the gate connection, the simulation was also conducted for the area with the gate connection. As shown in the Figure 4.10(b), the "Path 1" is the majority of areas without the gate connection, and the "Path 2" is the area with the gate connection. The cross-section view of structures of the "Path 1" and "Path 2" are shown in Figure 4.10(c). The electrical field distributions in "Path 1" and "Path 2" in MZO HVTFT and m-MZO HVTFT are simulated and the results are presented in Figure 4.11. In both "Path 1" (Figure 4.11 (a)) and "Path 2" (Figure 4.11(b)) regions, m-MZO HVTFTs show the lower maximum electric field than that of MZO HVTFTs. It indicates that the transition layer enables to reduce the peak electrical field in the devices with the gate connection.

The effects of the gate connection on the electrical field of HVTFTs along the cutlines are shown in the Figure 4.12. For both of m-MZO and MZO HVTFTs, the distribution and maximum value of electrical fields in the path 1 and 2 are almost the same. The major difference is the electrical field in the gate-source offset region. In the path 1, the electrical field drops quickly; on the contrary, in the path 2 the electrical field is constant in whole gate-source offset region.
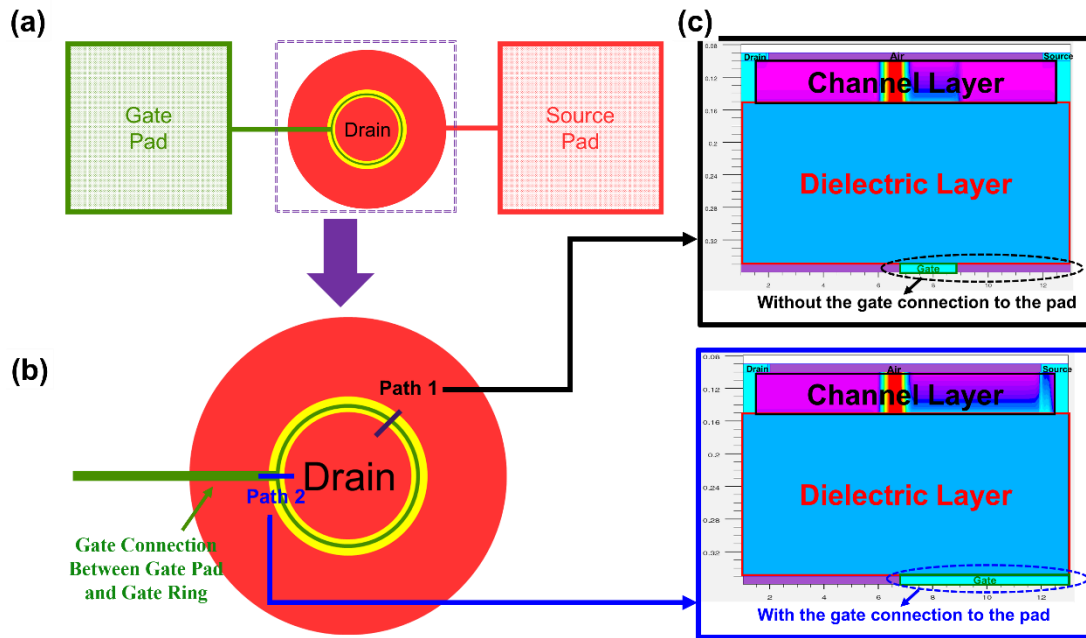
Figure 4.10 The schematics of 2D simulation areas of a HVTFT with and without

the gate connection: (a) top-view of the whole device, (b) two simulation paths,

and (c) cross-sectional view of structures along two paths
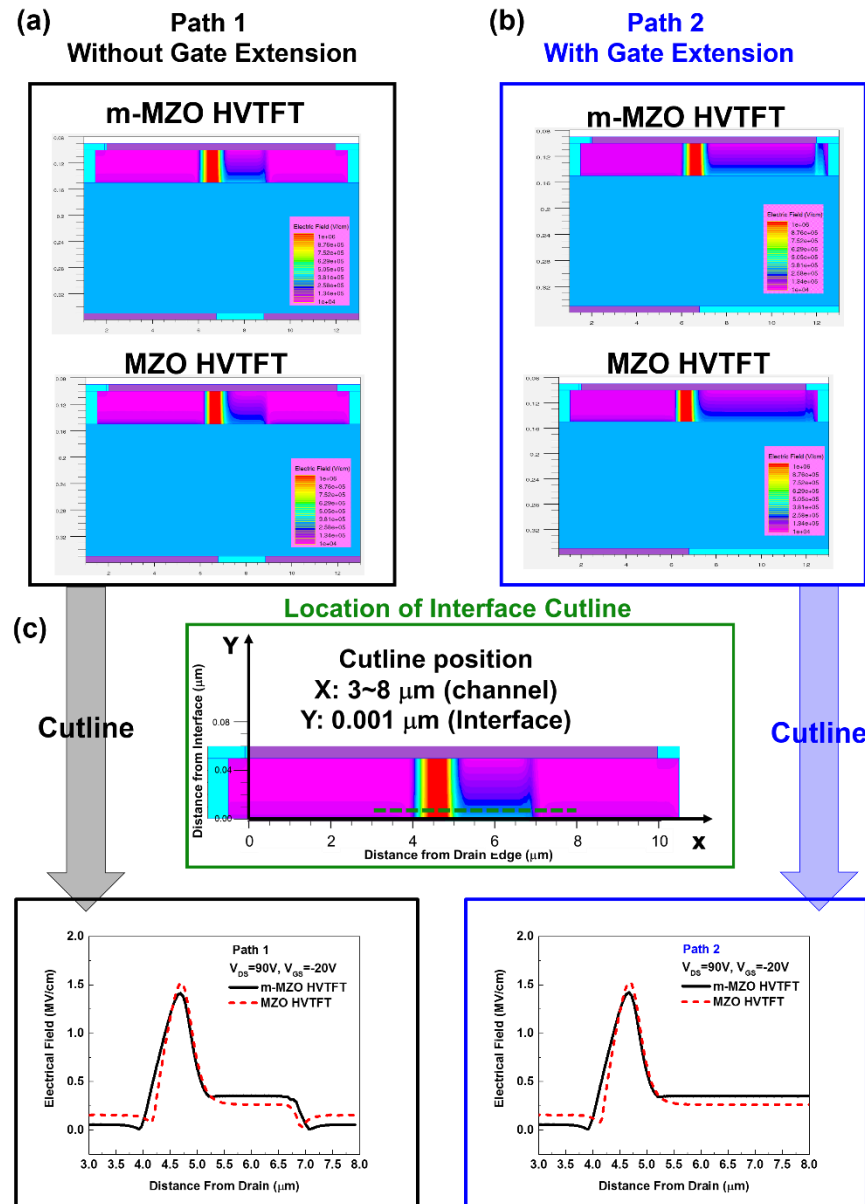
Figure 4.11. The simulation results of the electrical field distributions in the channel layers. The comparisons of electrical field distribution between MZO and m-MZO HVTFTs are presented for the configuration: (a) without the gate connection and (b) with the gate connection. (c) The location of 1D cutline. The comparison between m-MZO and MZO HVTFT along Path 1 and Path 2 are shown.

m-MZO HVTFT
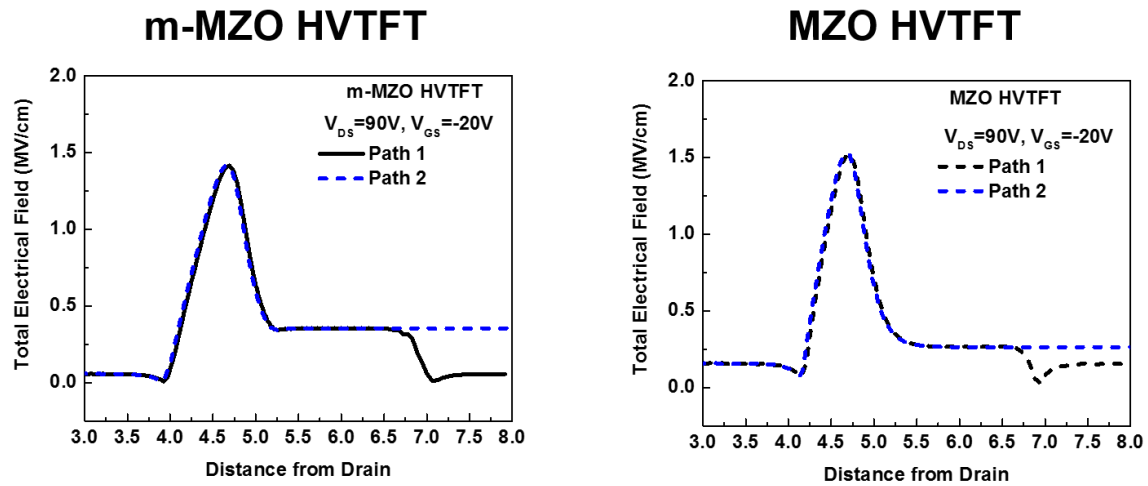
MZO HVTFT

Figure 4.12 The influence of the gate connection (Path 1: without the gate connection; Path 2: with the gate connection) to the electrical field distribution at the interface cutlines of m-MZO and MZO HVTFTs.

4.6. Summary

In this chapter, we demonstrated the MZO high voltage thin film transistors on a transparent glass substrate. The ring structure design reduced the electric field crowding effect in the devices. The thermal stability was enhanced by doping ZnO with a small amount of Mg to form the MZO channel layer. The interface design and engineering were conducted by inserting a modulation-doped ultra-thin MZO transition layer between the SiO_2 gate dielectric layer and the MZO channel, and they significantly improved the subthreshold slope and on-current values. More importantly, it enabled high blocking voltage of 609 V with an on/off ratio of $3.3{\times}10^8$, and operating voltage over 200 V. The comprehensive characterizations confirmed that the enhancement in the HVTFT performance was mainly attributed to the reduction in interface trap density and trapped charges, which leads to the reduction of the maximum electric field in the channel. This MZO-based HVTFT on glass technology is promising to serve as the solar inverter in PV-SOG technology to implement the emerging BIPV and self-powered smart glass.

Chapter 5 Interface Engineering in MZO TFTs

5.1. Background

In a TFT device, the interface between the channel and the dielectric layer is extremely critical to the electrical performance because it affects the carrier transportation significantly. A poor interface results in many negative impacts, such as poor subthreshold slope, a low mobility, an increase of leakage current.

In HVTFTs, the dielectric layer is deposited by PECVD, instead of thermal oxidation in MOSFET. The quality of PECVD is not as good as thermal oxide. Moreover, in the bottom gate structure, the channel layer is deposited after the dielectric layer, so the elements of the channel layer have a chance to diffuse into the dielectric layer. This diffusion not only creates traps in the bulk of the dielectric layer but also degrades the channel/dielectric interface. As described in Chapter 4, the inter-diffusion of Zn and Si elements created serious issues, such as generating extra interface defects and oxide trapped charges. In order to suppress the inter-diffusion between the channel and dielectric layer, we designed and added a transition layer MZO-TL as a diffusion barrier. The detailed analysis through comprehensive characterizations is presented in this chapter.

5.2. Interface Design and Engineering

There are several reports about diffusion barriers for ZnO based TFT, including Silicon Nitride[62] and Aluminum oxide[63]. However, the extra elements might introduce unknown impacts on the electrical performance and stability. Furthermore, it would be preferred to make the ultrathin and high quality diffusion

barrier layer without breaking vacuum during the channel growth to assure the interface quality. As a result, we adapted the Magnesium Oxide (MgO) which offered multiple advantages in designing of the interface. MgO has been widely used as a buffer layer for ZnO epitaxial growth. Using the MgO layer wouldn't add any new elements in the MZO HVTFT structure. The barrier layer was grown on SiO_2, immediately followed by the subsequent growth of the MZO channel without breaking vacuum. The actual barrier is the $Mg_yZn_{1-y}O$ (0.03$\leq$y$\leq$1) transition layer (MZO-TL) grown using the *in-situ* modulation doping by tailoring the Mg composition in order to reduce the lattice mismatch induced defects. The detailed analysis is described in the following Section 5.4.2. As MgO is a high-k material (k~9.9) the increase of effective oxide thickness would be minimized. Therefore, the improvement of the blocking voltage won't result in a huge sacrifice of on-current. Moreover, the bandgap of MgO is around 7.8 eV. It is a good insulator which prevent the increase of the gate leakage current.

The device structure and fabrication process for this study are essentially the same presented in Chapter 3 except inserting an MOCVD grown diffusion barrier between the SiO_2 (gate dielectric) and MZO (channel). The right side of Figure 5.1(a) and (b) presents the schematic layer structure of the regular MZO HVTFT and the m-MZO HVTFT which has the diffusion barrier, respectively.

5.3. Materials Characterization

To make a fair comparison, the samples for the material analysis were fabricated at the same conditions of regular TFT, except the patterning process. The structural and interfacial properties were analyzed using JEOL 2100F Field

Emission Lorentz Transmission Electron Microscopy (TEM), Energy-dispersive X-ray spectroscopy (EDS), and X-ray photoelectron spectroscopy (XPS). The TEM samples were prepared by using a FEI HELIOS 600 Dual Beam Focus Ion Beam (FIB).

5.3.1. XPS Characterization

X-ray photoelectron spectroscopy (XPS) was used to estimate the atomic percentages of different elements in the interface regions. The depth profiles were obtained by using the in-situ sputtering process. Figure 5.1(a) and (b) show depth profiles of atomic percentages of Si, Zn, and Mg in the MZO and the m-MZO HVTFT, respectively. A small amount (3%) of Mg doping is barely shown inside the MZO channels in both of MZO and m-MZO samples due to the detection limit of XPS. However, a narrow peak of Mg does appear in the m-MZO sample, produced from the $Mg_yZn_{1-y}O$ transition layer (MZO-TL). In the MZO sample, Zn diffuses extensively into the SiO_2 layer as indicated by the length of overlapped XPS profiles of SiO_2 and MZO. In contrast, there is an abrupt interface with negligible overlapped profiles of Si and Zn in the m-MZO sample.

5.3.2. TEM/EDS characterization

To understand the effect of the MZO-TL on improving the properties of the interface between the channel and gate dielectric layer, the cross sections of MZO and m-MZO samples prepared by a Focus Ion Beam(FIB) were studied using a transmission electron microscopy (TEM). Figure 5.2(a) and (b) show the images of the interface regions in MZO and m-MZO HVTFT samples, respectively. As shown in the inset of Figure 5.2(a), the gray dots are observed only in the SiO_2

dielectric layer of the MZO HVTFT sample. To identify these dots, energy-dispersive X-ray spectroscopy (EDS) was used to analyze the elemental composition of the films at different positions (point "A" to "F") across the interface. As shown in the dashed box of Figure 5.2c, the Zn peak in MZO HVTFT appears not only in the MZO channel area (point A) but also near the interface (point B) and even inside the gate dielectric SiO_2 layer (point C). The EDS results further confirm that the observed gray dots are related to the Zn element. Moreover, in the EDS spectrum, there is a Si peak marked by the "circle" in the MZO area (point A), The results indicate that the interdiffusions occur across the interface (point B): Zn diffuses from the MZO layer into SiO_2 while Si diffuses from the SiO_2 layer into the MZO layer. In contrast, for m-MZO HVTFT, as shown in the dashed box of Figure 5.2(d), the Zn peak appears in the MZO area (point D), only a tiny peak appears near the interface (point E), but no Zn peak is observed inside the SiO_2 layer (point F). On the other hand, as shown in the circle, there is no Si peak detected in the MZO area (point D).

Therefore, the modulation-doped thin transition layer inserted between the MZO and SiO_2 acted as a diffusion barrier, which hindered Zn and Si diffusion across the interface between the channel and gate dielectric layer. TEM/EDS and XPS characterizations provided consistent results that the phenomenal interdiffusion between the SiO_2 gate dielectric layer and the MZO channel layer was only detected in the MZO HVTFT. The MZO-TL in m-MZO HVTFT acted as a diffusion barrier, which effectively blocked the interdiffusion of Zn from the MZO to SiO_2, as well as Si from SiO_2 to the MZO channel.
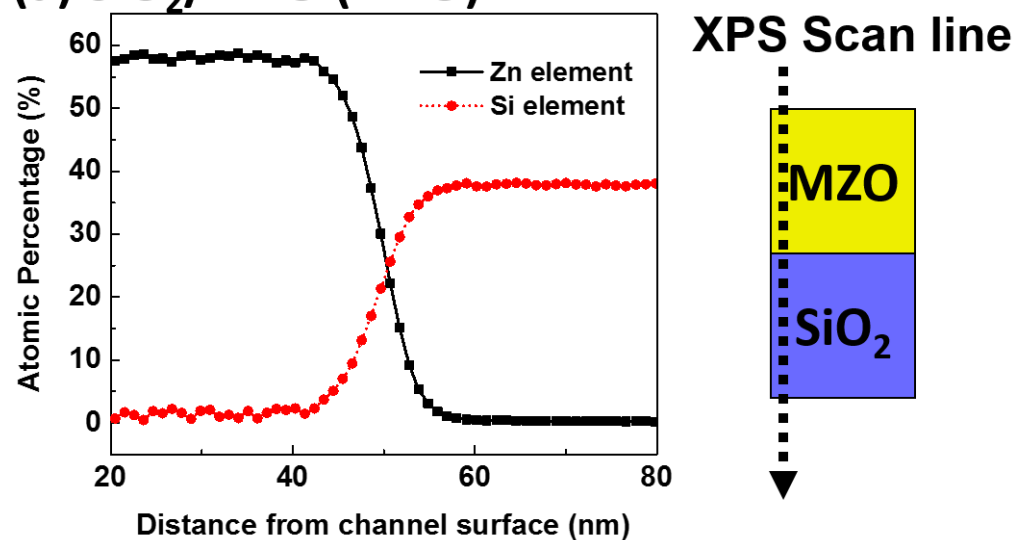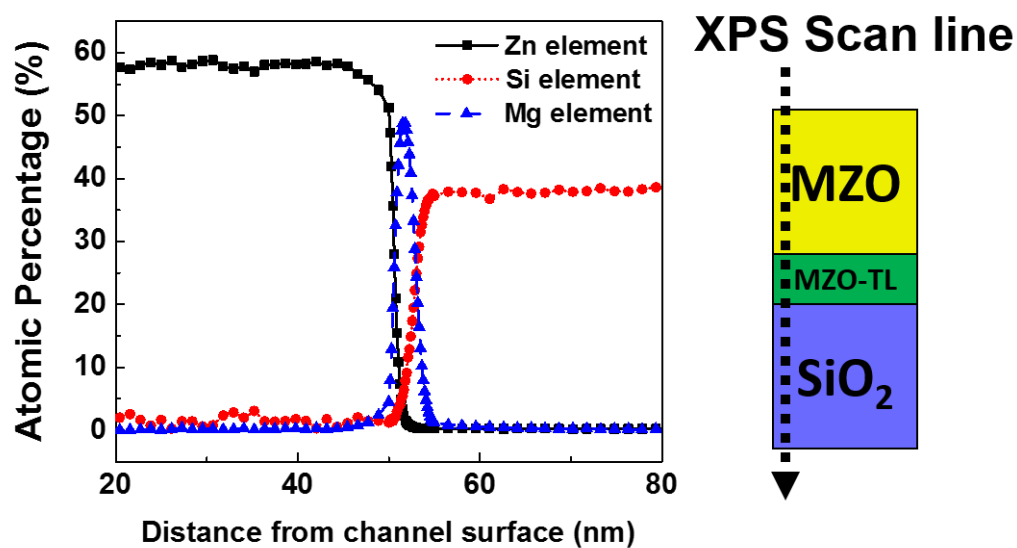
Figure 5.1. Depth profiles of atomic percentage of Si, Zn, and Mg from XPS measurements of (a) MZO and (b) m-MZO samples along the scan lines shown in the TEM pictures. The oxygen profile is not included.
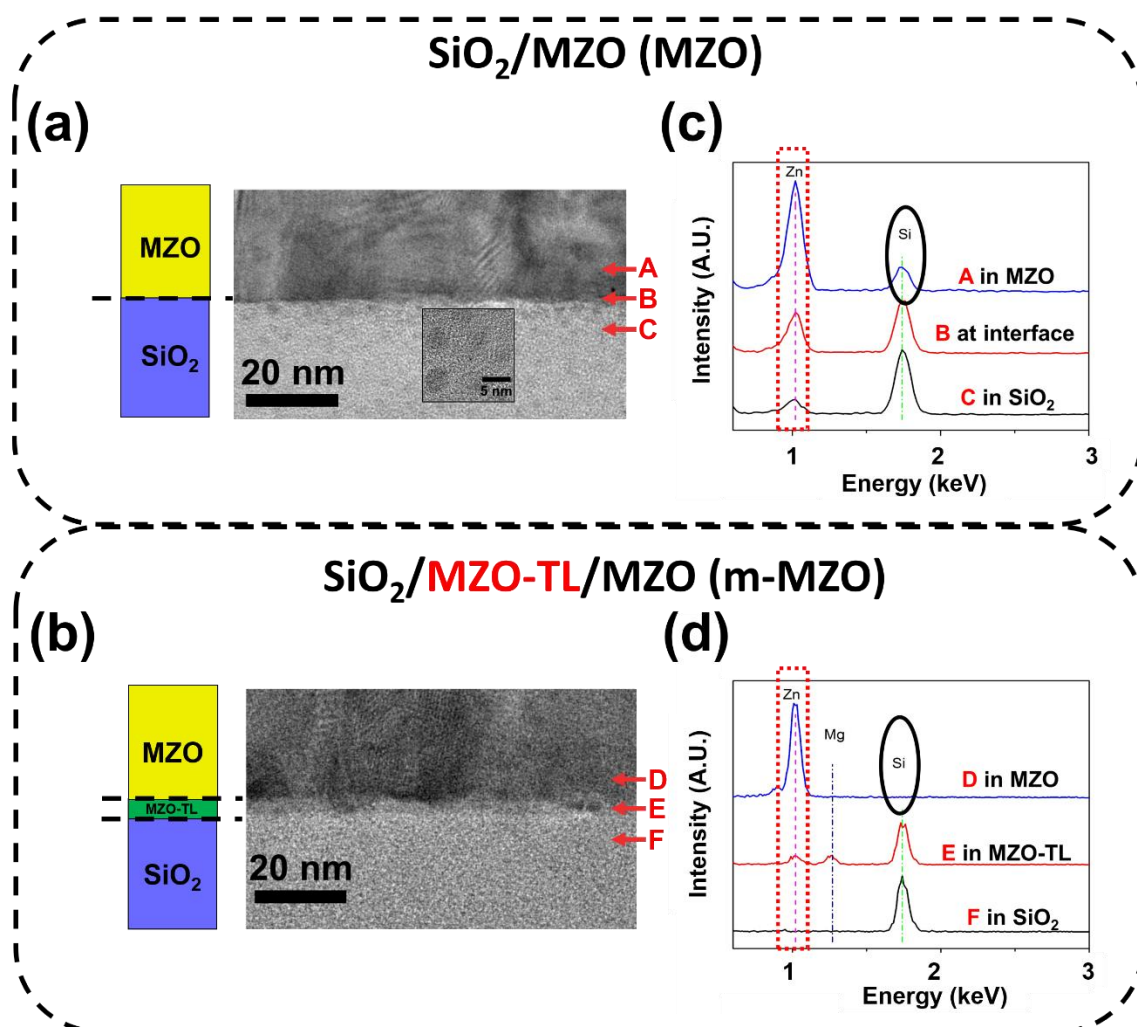
Figure 5.2 TEM images of the interfaces between the channel layer and the SiO_2 dielectric layer (a) without a transition layer (for MZO HVTFT) and (b) with a modulation doped transition layer (for m-MZO HVTFT). The inset of Figure 5.3(a) features the gray dots found in the SiO_2 layer in the MZO sample. EDS spectra of Zn, Mg and Si elements at the different locations (marked in the TEM images) across the channel – gate dielectric interface for (c) MZO and (d) m-MZO samples.

5.4. Electrical Characterization

The I-V characteristics of ZnO and MZO TFTs with V_{DS} = 10V and V_{DS} = 0.1V are shown in Figure 5.3(a) and (b), respectively. As described in Chapter 3, the threshold voltage (V_{TH}) is defined as the gate voltage value when a drain current (I_{DS}) reaches 10^{-8} A with V_{DS}=10V. The turn-off voltage (V_{OFF}) is defined as the gate voltage value when a drain current (I_{DS}) reaches 10^{-13} A with V_{DS}=10V. The field effect mobility (μ_{FE}) is extracted from the linear region. The subthreshold swing (S.S.) is extracted from a 3-decades range in the subthreshold region of the $\log_{10}$ (I_{DS}) vs V_G curve with V_{DS}=10V as in (5-1)

$$S.S. = \left[\frac{\partial \log_{10} I_{DS}}{\partial V_G} \right]^{-1} \qquad (5-1)$$

The MZO TFT exhibits V_{OFF} of -2.5V, V_{TH} of 2.6V and S.S. value of 1.3 V/decade while the m-MZO TFT shows more positive V_{OFF} of 2.5V, V_{TH} of 5.0V and steeper S.S. of 0.3 V/decade. Since all TFTs are built on the same substrate (common gate) and dielectric layers, it can be assumed that the differences of V_{TH} and S values between the two different TFT channels and interface mainly result from the different trap densities measured during electrical tests The total trap density from the subthreshold slope (S.S.) can be estimated in the equation (5-2)[33]:

$$S.S = \log_e 10 \times \frac{k_B T}{q} \left(1 + q \frac{t N_{bulk} + D_{it}}{C_G} \right) \qquad (5-2)$$

where q is the elementary electric charge, k_B the Boltzmann constant, T the temperature in Kelvin, t the channel thickness, N_{bulk} the bulk trap density, D_{it} the interface trap density, and C_G the capacitance per area of the gate dielectric layer

(C_G is 1.73×10^{-4} F/m^2 and 1.69×10^{-4} F/m^2 for MZO and m-MZO HVTFT, respectively. The theoretical values of SiO$_2$=3.9 and MgO=9.90[34] are used in estimation). The total trap density includes the bulk trap (tN_{bulk}+ D_{it}) and the interface trap (D_{it}), which are calculated to be 8.17×10^{13} cm^{-2} and 1.48×10^{12} cm^{-2} for MZO and m-MZO HVTFT, respectively.

As indicated in Chapter 4, the Zn diffusion caused both the negative threshold voltage shift and subthreshold slope degradation. The threshold voltage shift is mainly attributed to the Zn^{2+} ions trapping in the bulk of the dielectric layer, and these positive charges can attract extra electrons and move the turn-on voltage of the device to the more negative value. The subthreshold slope degradation also could be related to the defects generated by the Zn diffusion, The Zn diffusion induced defects could exist in channel layer, and even penetrate through the SiO$_2$/Si interface and then may break the Si-O bonds. Overall, the interface defect density increases by the Zn diffusion from the channel to the dielectric layer.

a.

b.
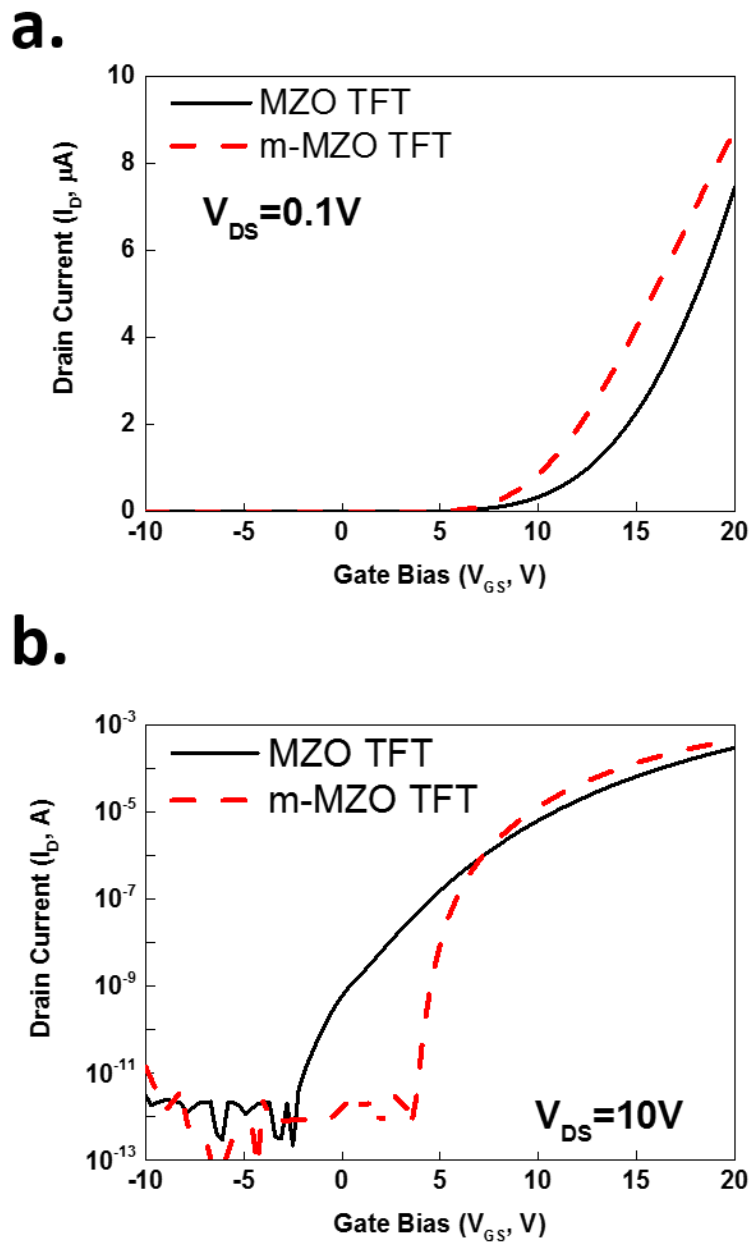
Figure 5.3 Comparisons between the regular MZO TFT and the m-MZO TFT with interface modification: (a) TFT I-V characteristics; (b) the effect of MgO thickness on electrical performance; (c) depth profiles of elements near the MZO TFT interface; (d) depth profile of elements in m-MZO TFT interface.

5.4.1. The effect of continuous growth of (MZO-TL) and MZO channel

To make a good interface between the channel and the dielectric layer, there is a strict Q-time control of the time gap between the depositions of two layers. In our design, the transition layer (MZO-TL) and MZO channel were both deposited by MOCVD, so it allowed us to continuously deposit the channel layer after the deposition of the transition layer without breaking the vacuum. Therefore, the exposure of the interface to outside ambient was limited. The comparison of continuous growth and with vacuum break in MOCVD is shown in Figure 5.4. The TFT with vacuum break has more negative threshold voltage of 2.3V, and poorer subthreshold slope of 1 V/decade. The total trap density, including the bulk trap (tN_{bulk}+ D_{it}) and the interface trap (D_{it}) is 6.19×10^{13} cm^{-2} which is one order higher than the TFT without vacuum break. Because two TFTs have the exactly the same film stack, the difference in trap density should attributed to the increase of interface states caused by the vacuum break. This comparison confirmed that the current MgO/MZO interface design with the transition layer plus the interface engineering using in-situ modulation doping without breaking vacuum in MOCVD significantly reduced the interface defects, resulted in improvement of the IV characteristics in m-MZO HVTFT.
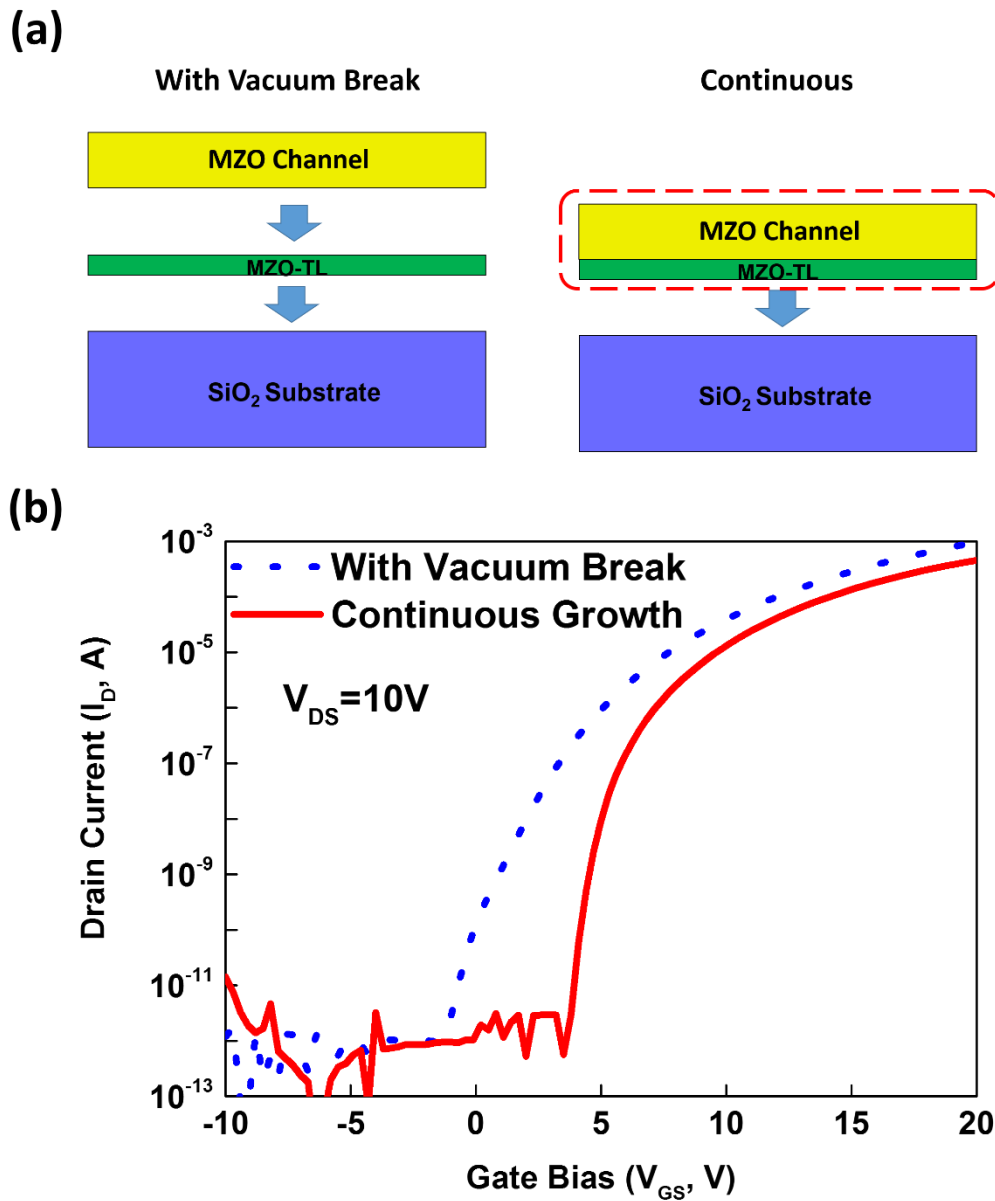
Figure 5.4 (a) The schematics of MOCVD growth of with vacuum break and continuous of the transition layer (MZO-TL) and the channel layer (MZO). (b) The comparison of transfer characteristics of TFTs which have two different MOCVD growth conditions.

5.4.2. Modulation doping of transition layer

Even with the MgO-based transition layer, the Mg- profile near the interface of the channel and dielectric layer is critical to TFT performance, especially in terms of subthreshold slope. If the Mg profile near the interface changes abruptly in a small distance as shown in Figure 5.5(b), the stress will not be release properly. In order to reduce the stress caused by lattice mismatch between the MgO TL layer (y=1) and MZO channel (y=0.03), we used the modulation doping technique to tailor the Mg composition in the transition layer. As shown in Figure 5.5(c), the Mg concentration gradually changed from 100% near SiO_2 interface to less than 3% (just like the doping level in the channel) near MZO channel. The comparison of transfer characteristics of these two different profiles is shown in Figure 5.5(d). The MZO TFT with steeply varied doping has threshold voltage of 6.8V and *S.S.* of 0.9 V/decade, and the MZO TFT with gradually varied doping has threshold voltage of 5.3V, and *S.S.* of 0.3 V/decade. The total trap density including the bulk trap (tN_{bulk}+ D_{it}) and the interface trap (D_{it}) are calculated to be 5.17×10^{12} cm^{-2} and 1.48×10^{12} cm^{-2} for MZO TFT with abrupt Mg profile and with gradually varied Mg doping profile, respectively.

Without gradient doping, the subthreshold slope degrades dramatically. As mentioned in previous paragraph, the dislocation between two layers can generate many interface defects. The other possible reason is related to the Mg concentration in the channel near the interface. In the case of the abrupt varied profile of MOCVD growth, Mg can pile up near the channel at the interface with the MZO-TL layer. This can increases the Mg concentration of the surface channel.

As indicated in Ku's article[49], high doping concentration ($\geq 10\%$) can deteriorate the TFT performance due to the alloying disorder and increased effective mass of electrons. However, since the on-current shows little degradation, the major factor of the TFT degradation should be still the extra interface states generated by lattice mismatch.
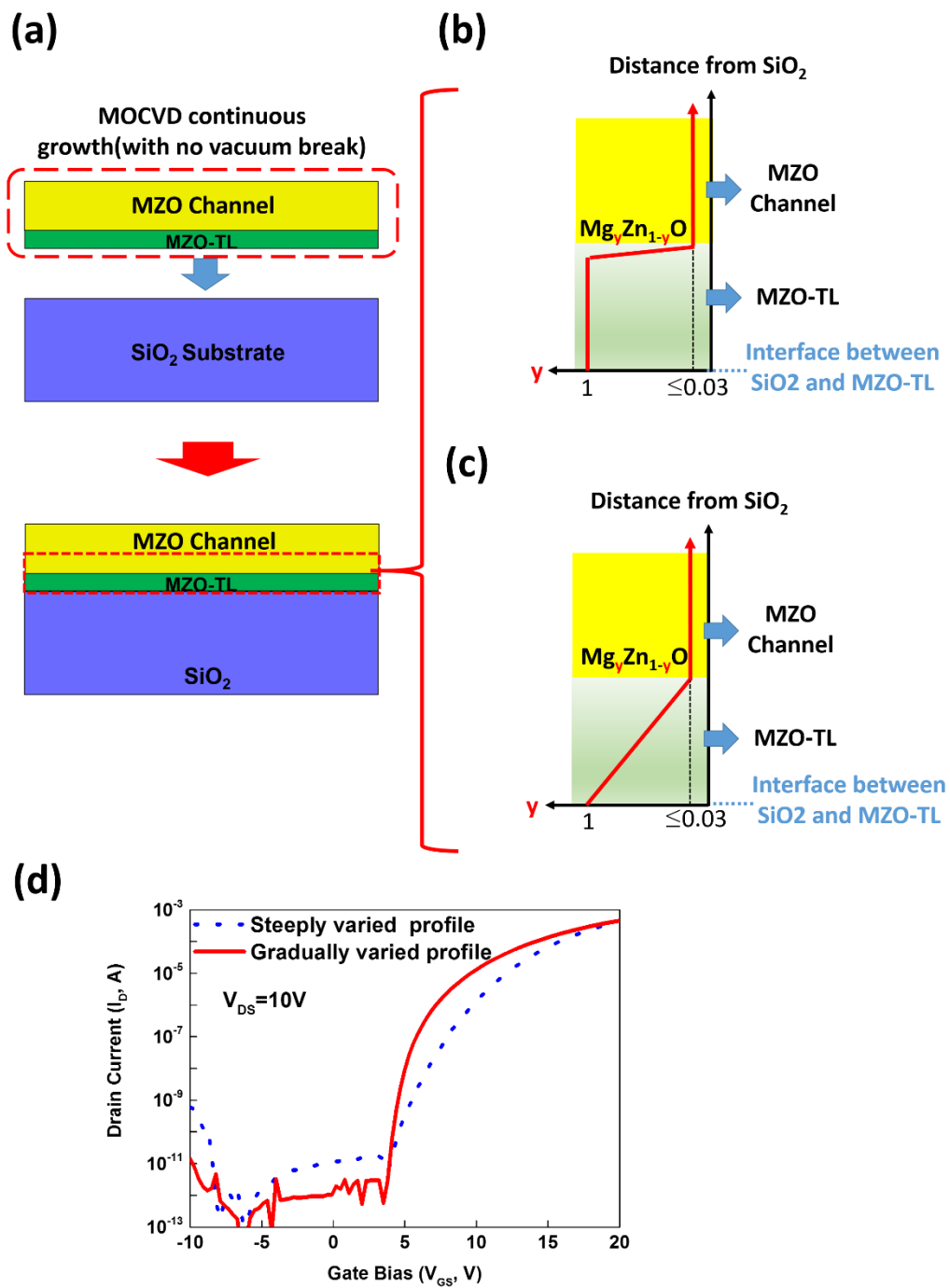
Figure 5.5 (a) The schematics of adding a transition layer. The schematics of (b) with abrupt Mg profile and (c) with gradually varied Mg doping profile. (e)The transfer characteristics of MZO with two different doping profiles.

5.4.3. Effect of MZO-TL Thickness

The effect of MZO-TL thickness on TFT electrical performance was also studied and the results are shown in Figure 5.6. In comparison with the m-MZO TFTs with MZO-TL=5nm, the m-MZO TFTs with a thicker MZO-TL layer (MZO-TL=15nm) show more positive (+1.8V) V_{TH} and 20% superior S.S. However, on-current I_{on} shows one order degradation, which may result from a thicker effective dielectric layer.

The positive moving of V_{TH} could be related to the suppression of positive Zn ions (Zn^{2+}) trapped in the SiO_2, while the improvement of S.S. could be attributed to the reduction of the interface states. The out-diffusion of Zn from the MZO channel layer could generate Zn related defects located in the channel and near the channel-gate dielectric interface. Thicker the transition layer, fewer Zn could diffuse into the dielectric layer. While the growth temperature and time of MZO channel increases, more and deeper diffusion of Zn ions will happen. It requires a thicker diffusion barrier to prevent Zn ions diffusion into the dielectric layer. However, a thicker diffusion barrier increases the effective thickness of dielectric layer which leads to degradation of electrical performance. As a result, the optimization of thickness of diffusion barrier is required for specific MZO channel growth condition. In our case of MOCVD MZO layer, we chose 5nm transition layer as the optimized thickness.
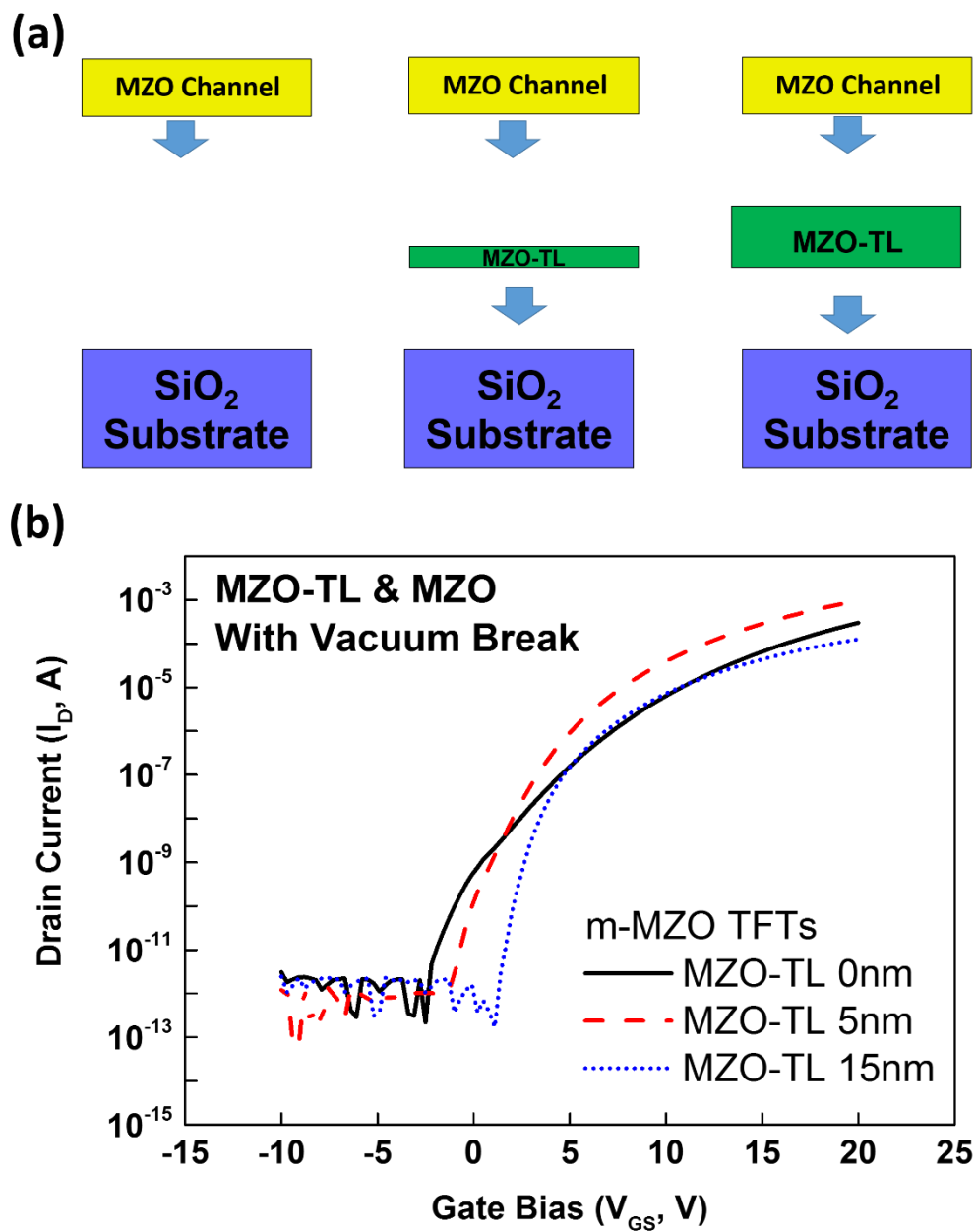
Figure 5.6 (a) The schematics of MOCVD growth of different MgO thickness for transition layer. (b) The transfer characteristics of m-MZO TFTs of different transition layers thickness (MZO-TL).

5.4.4. Gate Leakage Current

The inter-diffusion of Zn and Si elements can make damage to the dielectric layer. The diffusion could break the Si-O bonding and create defects. Also the trapped charges from diffused ions, such as Zn^{2+} also become defects inside the dielectric layer. By adding the thin transition layer as the diffusion barrier, the dielectric layer is protected from the damage caused by diffused elements during the subsequent channel deposition.

Figure 5.7(a) shows the comparison of the gate leakage current between MZO and m-MZO TFT under different negative gate bias. Since the dielectric layer is an insulator, this gate leakage should be from the electrons tunneling through the gate dielectric insulator. The gate leakage current in MZO TFT increases an order when the gate bias increases to around -25V, whereas, m-MZO TFT still keeps the low leakage level. Moreover, the hard breakdown happened in MZO TFT at the gate bias of ~-80V while m-MZO just shows a soft increase.

Such difference should be related to the defect density in the bulk of the dielectric layer. In comparison with m-MZO TFT, MZO TFT has more defects in the bulk dielectric layer due to Zn Ions diffusion into the gate dielectric layer in MZO TFT as shown in Figure 5.7(b). Based on the percolation theory[64], while the devices are under a large bias, some energetic carriers cause defects randomly in the bulk of the dielectric layer. When the defects are enough to form a path for carriers to conduct as shown in Figure 5.7(c), a catastrophic breakdown occurs. If the defect density of the gate dielectric layer is reduced, it will require higher bias and longer time to create enough defects for the formation of the conduction path.

As a result, compared to MZO TFT, m-MZO TFT showed lower gate leakage current under high negative gate bias and larger breakdown voltage
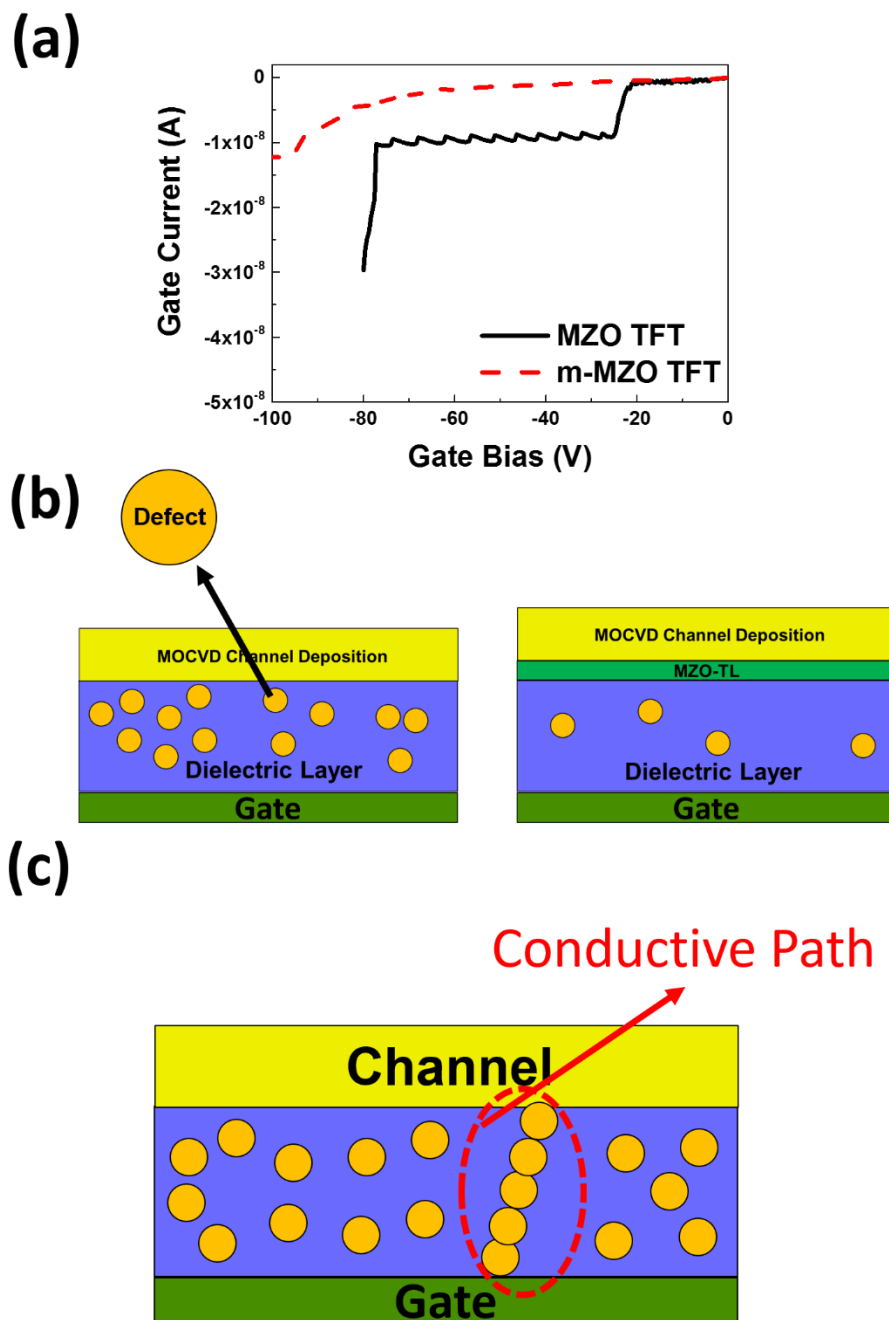
Figure 5.7 (a)The comparison of the gate leakage current of MZO and m-MZO TFTs. (b) The schematics of defects distribution in MZO and m-MZO TFTs. (c) The schematics of the dielectric breakdown mechanism

5.5. Summary

In this chapter, we conducted comprehensive characterizations to analyze the transition layer in different aspects, including materials and electrical performance. In the XPS analysis, the profiles of Zn and Si elements from channel to dielectric layer clearly indicate the effect of the addition of the transition layer which stopped the inter-diffusion of Zn and Si. The TEM/EDS characterization was consistent with the XPS results and further supported that the MZO-TL served as an effective diffusion barrier.

The structural characterization were correlated with the electrical performances. It is demonstrated that the interface engineered m-MZO TFTs possesses better electrical characteristics with a normally-off feature (V_{OFF} of 2.5V, which is preferable for lower power consumption applications. Moreover, almost two-order reduction of overall defect density was achieved in the modulation-doped m-MZO TFTs, resulted in much steeper subthreshold slope. To have deeper understanding and better control of the transition layer, we studied several important factors of the growth of MZO-TL. The continuous growth between channel and dielectric layer lowered the interface defect density by an order. The modulation doping of Mg with the gradual profile near the channel-dielectric interface lowered the interface defect density by 50%. Transition-layer thickness affected the amount of Zn diffusion. Although a thicker MZO-TL could further reduce Zn diffusion; however, it could also decrease the dielectric capacitance as well as the on-current. Furthermore, the diffusion barrier protected the dielectric layer from the damage caused by Zn diffusion; therefore, reduced the

gate leakage current at high negative gate bias and improved the oxide breakdown voltage. Overall, the interface engineering with addition of MZO-TL significantly improved the channel/dielectric interface and the quality of the dielectric layer, concomitantly, enhanced the electrical performance of the HVTFT.

Chapter 6 ZnO Based HVTFTs on Flexible Substrate

6.1. Introduction

Recently the "Internet of Things" (IoT) has been one of the most popular research topics in both academia and industries. IoT addresses the network of physical objects which can be controlled and interacted wirelessly supported by current computer technologies, such as Bluetooth, Wi-Fi, smart phone, cloud computing. Its technologies aim for improving users' experiences, improving the efficiency, and reducing power consumption in many applications, such as medical monitoring and treat, food supply. Among many IoT technologies, the wearable systems have attracted increasing research interests due to its broad applications and profound impact on people's daily life. In wearable systems, electronic devices such as receivers and sensors are required to be mounted on flexible and bendable surfaces. To improve the user experience, the physical connection, such as wired charging and wired communication should be minimized[65]. As a result, a mobile device of a long battery life and span is preferred.

Traditionally, wearable electronics systems are powered by Li-ion batteries or other external power sources; however, pollution of Li-ion batteries and external wirings diminish the attraction of wearable electronics[66]. This issue has stimulated the studies on self-powered portable electronics to build a sustainable system. Many studies focus on developing high efficiency wearable power generators. Just like the solar inverters in solar energy technologies, the power management system also plays a key role in the self-powered system; thus, the high voltage device is still the fundamental component in power control circuit. In this chapter,

we present the feasibility studies on flexible high voltage devices-flexible HVTFT, which can be integrated with wearable power generators to form a wearable energy system. It can be used to charge wearable batteries and/or directly drive other wearable components, such as sensors, actuators, and communication platforms.

6.2. Background

6.2.1. Self-powered wearable electronics

To make a self-powered wearable electronics, the energy sources have to be accessible from users or environment easily. Scientists and engineers have investigated different nano-generators from three major energy sources: biomechanical energy from the movement of human body, solar energy, and thermal energy from the temperature difference between human body and environment. However, in the past most technologies of nano-generators, such as piezoelectric nano-generator could only provide low power due to low efficiency; therefore, they were unable to provide sufficient energy to power wearable electronics[66].

Recently, a triboelectric nano-generators (TENGs) was introduced by Fan et al.[67]. TENG provides larger power, enabling to drive many electronics, such as Magnetic Sensor[68], Liquid Crystal Display (LCD), and Light-Emitting Diode (LED) Display[69]. Seung et al.[69] demonstrated a nano-patterned ZnO/PDMS/Ag based triboelectric energy harvester which generated over milliwatt from 120V and 65 μA on the textile substrate. The typical output characteristics of TENGs are high voltage but low current. In order to utilize the nano-generators to power regular

electronics, converting high voltage to regular voltage is necessary. Another critical issue is that generally the energy harvesting from environmental sources is not stable; however, it's important to provide constant voltage and current to power the regular electronics in the wearable systems.

To implement TENGs as an energy source for portable or wearable electronics, a power management system which is also built on a flexible substrate is essential.[70] However, the conventional power controller is bulky and not compatible with wearable electronics. It is built on a rigid substrate, separated from the nano-generators; thus requires extra wirings to make connection. To make a flexible power control device feasible to wearable systems, it is desired to integrate nano-generators with the power controller on a single flexible substrate, like a plastic or fabric textile. Such an integrated system not only provides small size and necessary flexibility but also improves the efficiency by removing external wirings between nano-generators and the power controller; therefore can be used to charge wearable batteries and/or directly drive electronic devices under vastly different environmental conditions.

6.2.2. Analysis on Flexible Transistors for High Voltage Applications

To develop an integrated power management system for wearable electronics, a high voltage transistor fabricated on a flexible substrate at low process temperature is needed. A thin film transistor is more suitable than MOSFET as a flexible high voltage device. Several materials, such as amorphous Si, polycrystalline Si, and Indium-Gallium-Zinc-Oxide (IGZO) have been utilized on the application of high voltage TFTs; however, none of them has been built on a

flexible substrate for high voltage applications. On the other hand, organic materials can be used to fabricate transistors at low process temperature. Recently, Smith et al.[25] reported a high-voltage organic thin-film transistor (HVOTFT) which operated at 400V. However, its low on-current of 0.3 μA (~6×10^{-3} A/cm^2 at V_{DS}=100V) due to low mobility makes the HVOTFT unable to directly connect to the nano-generators which have high output current. As described in the previous chapter, ZnO has several advantages in high voltage applications, such as wider bandgap, high mobility even in low crystallinity, low process temperature. Moreover, many energy harvesters are based on ZnO materials[69,71–73]. The integration will be much easier if the nano-generator and power management circuits are made up on the same materials.

6.3. Fabrication Process of HVTFTs on Flexible Substrates

To implement HVTFT to wearable electronics, using a flexible substrate is necessary. The flexible substrate, such as Polyethylene naphthalate (PEN), aromatic fluorine-containing polyarylates (PAR) and Polyimide (PI), can only withstand lower fabrication process temperature due to its low transition temperature and large coefficient of thermal expansion (CTE). The TFT process developed for the glass substrates cannot be directly implemented on flexible substrates without necessary modification. As feasibility studies on flexible HVTFTs, we deposited the channel using the RF sputtering technology at room temperature instead of MOCVD at 400°C for HVTFT on glass. Furthermore, we changed the gate dielectric layer by using Aluminum oxide (Al$_2$O$_3$) deposited by

atomic layer deposition (ALD) at low temperature (~100°C) to replace the PECVD

SiO_2 dielectric layer deposited at 400°C.

6.3.1. Selection of Flexible Substrate

We prefer to use Polyethylene Naphthalate (PEN) as the substrate for following reasons[74]: (i)PEN has a lower CTE of 13 ppm/K than PI (17 ppm/K) and PAR (53 ppm/K). (ii)PEN has high transparency (>85%) which is much better than PI (30~60%). For wearable electronics, it's important to have the attractive exterior. Transparent substrates make the least interference to the appearance of products.

Although PEN has smaller thermal expansion than other popular flexible substrates, the thermal expansion during the process would affect the mask alignment, resulting in low yield. In order to solve the problem, PEN substrates were degassed at 110°C for 12 hours before the device fabrication. Because the degassing temperature (110°C) is slightly higher than the highest process temperature, it prevents extra thermal expansion for the subsequent fabrication process. After degassing, PEN substrate was encapsulated with a 50nm ALD-Al_2O_3. This encapsulation process not only protected the plastic substrate from gas adsorption but also improved the adhesion of the gate metal. In the subsequent process, as long as no process temperature is higher than the encapsulation temperature, the thermal expansion of the PEN substrate can be minimized.

6.3.2. Development of Channel Materials

In the development of the channel material for flexible HVTFT, we used the regular TFTs shown in Figure 6.1(a) to evaluate the quality of the film first. The

process was very similar to the process steps mentioned in the section 3.2, except for the sputtering ZnO channel. The sputtering process was conducted at room temperature (25°C) and the total thickness of ZnO channel layer was ~45nm. The comparison between MOCVD ZnO and RF sputtering ZnO TFT is shown in Figure 6.1 (b). The RF sputtering ZnO TFT showed more negative turn-off voltage of -5V, 30% less ON-current, slightly worse subthreshold slop and comparable OFF-current. Overall, the quality of sputtering ZnO was just slightly worse than MOCVD ZnO. Considering lack of the thermal treatment in sputtering process, the channel quality of sputtering ZnO deposited at room temperature should be good enough for the application of flexible HVTFT. Meanwhile, the gate leakage current of RF sputtering ZnO TFT is lower than the case of MOCVD ZnO TFT. The possible reason might be related to the deposition temperature. The Zn and Si inter-diffusion in the interface of channel-gate dielectric layer is high sensitive to the temperature. The RF sputtering at room temperature had smaller thermal budget than MOCVD at 400°C, so less defects were generated in the bulk of the dielectric layer, resulted in smaller gate leakage current in the sputtering ZnO TFT.

(a)
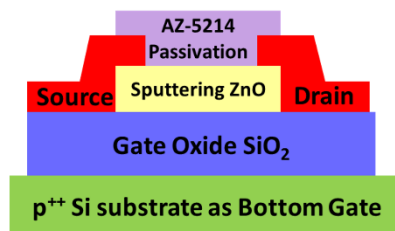
(b)
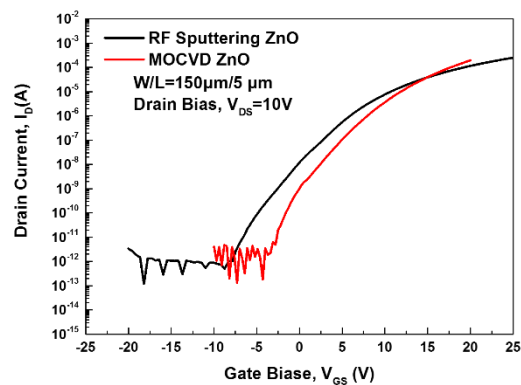
(c)
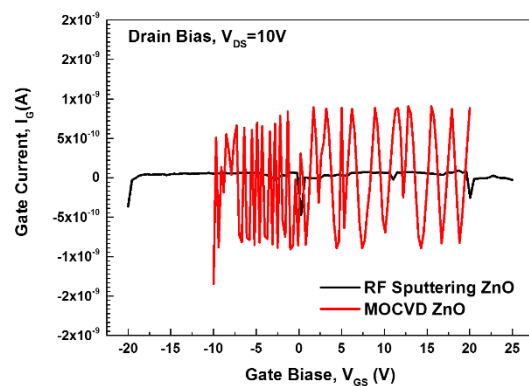
Figure 6.1 (a) The cross-sectional of regular sputtering ZnO TFT. (b)Transfer characteristics of RF sputtering ZnO and MOCVD ZnO TFTs. (c) Gate leakage current of RF sputtering ZnO and MOCVD ZnO TFTs.

6.3.3. Evaluation of Dielectric Layer

After development of the sputtering channel material, we studied the ALD Al_2O_3 film as the dielectric layer. As a gate dielectric, Al_2O_3 has attracted a great attention because of its strong adhesion to dissimilar materials, and thermal and chemical stabilities[75]. Also, Al_2O_3 has the wide bandgap (~9eV), a high electrical breakdown field (5~10 MV/cm), and a high permittivity (k=8.6~10) which make it a great candidates for being used as the gate insulator in high voltage transistors. For flexible applications, Al_2O_3 can be deposited using ALD at lower than 200°C which is compatible with the flexible substrates of lower glass transition temperature. Cheong et al. demonstrated a flexible and high performance (16.93$cm^2V^{-1}sec^{-1}$, low leakage current of ~0.1nA and SS of 0.39) Zinc–Indium–Tin Oxide TFTs which had ALD Al_2O_3 deposited at 150°C [76]. The low leakage current demonstrate its high insulating quality, and the good subthreshold slope indicated a good interface between ALD Al_2O_3 and oxide semiconductor channel.

The HVTFTs on the glass substrate was used to evaluate the new combination of Al_2O_3 dielectric layer and RF sputtering channel layer. The film stack of the testing device is shown in Figure 6.2 (a). The process steps are similar to that described in Section 3.2, except for the deposition of dielectric layer and channel layer. The channel layer recipe was described in Section 6.3.2. An Al_2O_3 (100nm) was deposited using ALD at 100 ℃ with trimethylaluminum (TMA) and ozone (O_3) as aluminum and oxygen precursors, respectively. The comparison of electrical characteristics between RF sputtering ZnO HVTFT (with 100nm ALD Al_2O_3 dielectric layer) and MOCVD ZnO HVTFT (with 200nm PECVD SiO_2

dielectric layer as shown in Chapter 4) is shown in Figure 6.2(b) and (c). In comparison with HVTFT of MOCVD ZnO with SiO_2 200nm, the HVTFT of RF sputtering ZnO with Al_2O_3 100nm shows the same turn-off voltage, an order higher ON-current, similar subthreshold slop and comparable OFF-current. The capacitance of SiO_2 200nm is only five times larger than Al_2O_3 100nm ($3.9 \times \varepsilon_0$ for SiO_2 and $9.3 \times \varepsilon_0$ for Al_2O_3). Based on the basic current-voltage equation

(6-1), the on-current is proportional to capacitance and mobility if the device dimensions and bias conditions are the same.

$$I_D = \frac{W}{L} C_d \mu [(V_{GS} - V_{TH})V_{DS} - 0.5 V_{DS}{}^2] \tag{6-1}$$

, where C_d is the dielectric capacitance and μ field-effect mobility. Therefore, besides of larger capacitance, the HVTFT of RF sputtering ZnO with Al_2O_3 100nm should have higher mobility than HVTFT of MOCVD ZnO with SiO_2 200nm does. However, from the comparison in Section 6.3.2 based on the same SiO_2 dielectric layer, MOCVD ZnO channel had higher intrinsic mobility than sputtering ZnO did. Therefore, the key factor of higher mobility in the HVTFT of RF sputtering ZnO with Al_2O_3 100nm should be related to better channel-dielectric layer between sputtering ZnO and Al_2O_3 in comparison with the interface of MOCVD ZnO and SiO_2. The enhanced channel-dielectric interface improved the field-effect mobility by reducing the surface scattering. Also, as shown in Figure 6.2(c), the leakage current of RF sputtering ZnO HVTFT is comparable to the case of MOCVD ZnO HVTFT. Overall, ALD Al_2O_3 showed a great potential to be used as the dielectric layer in flexible HVTFTs.
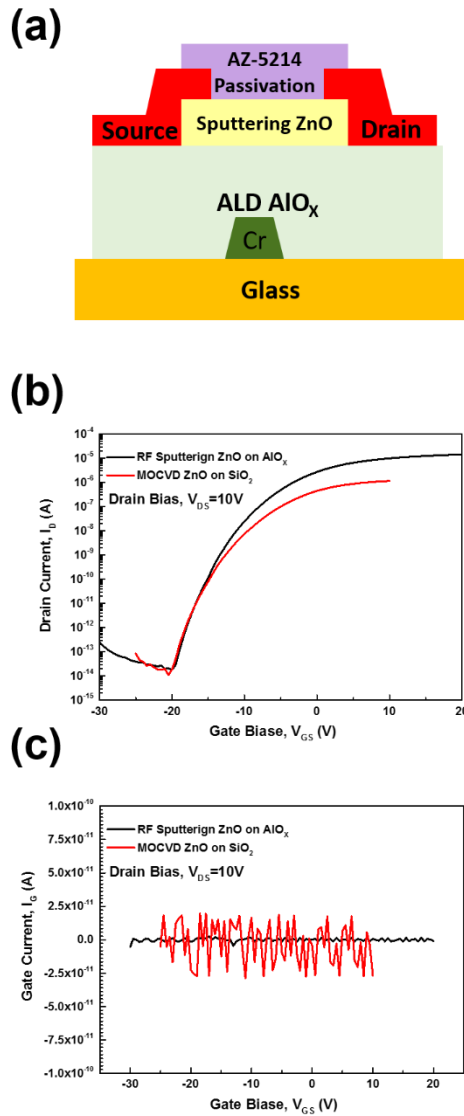
Figure 6.2 (a) a film stack of sputtering ZnO on ALD Al₂O₃ HVTFT. (b) The transfer characteristics and (c) gate leakage current of MOCVD ZnO/ PECVD SiO₂ and RF sputtering ZnO/ALD Al₂O₃ HVTFTs.

6.4. Experimental Results

6.4.1. Fabrication of flexible HVTFT

The structure of the flexible HVTFT is similar to the HVTFT on a glass substrate as described in Section 4.2.3. The flexible HVTFTs were fabricated on

125μm thick capsulated Polyethylene naphthalate (PEN) substrates. A 50 nm chromium (Cr) layer was deposited by DC sputtering at room temperature, with a deposition rate of ~2.3 Å/second), then patterned using a dry etching process (Oxford C, ICP power 600W, RF power 10W, Cl_2=47 SCCM + O_2=3 SCCM, P=10 mTorr, T=50°C) to serve as the bottom gate electrode. Then, a 100 nm Al_2O_3 layer as the gate dielectric layer was deposited by Atomic Layer Deposition (ALD) at 100 ℃ with trimethylaluminum (TMA) and ozone (O_3) as aluminum and oxygen precursors. Following the Al_2O_3 deposition, a 45nm ZnO channel was deposited by RF sputtering at room temperature with a deposition rate of 4 nm/min. The channel layer was patterned by the wet etch process. The source and drain metallization (100 nm titanium / 50 nm gold) was deposited using electron beam evaporation, followed by a normal lift-off process. A 1.5 μm photoresist film (AZ-5214) was coated on top of the TFT channel, serving as a passivation layer to prevent ambient absorption/desorption during electrical testing. Before VIA opening, the hard bake at 140°C was conducted to densify photoresist to resist the acid etching. For the VIA opening, wet etching was conducted using the diluted BOE (1:7).

6.4.2. Electrical Performance and Blocking Voltage

The electrical measurements were conducted using an HP-4156C with an HP-41501B Pulse Generator. With the boost from the connection of a pulse generator, the maximum voltage of the HP-4156C electrical testing system was limited to be 200V. The system which had a current resolution of $1x10^{-15}$ A was

used for all transfer characteristics. All electrical measurements were conducted in a light-tight probe station. Definitions of electrical parameters were described in 4.3.2.

The photo of the flexible and semi-transparent HVTFT is shown in Figure 6.3(a). The transfer characteristics of sputtering ZnO HVTFT on a flexible PEN substrate is shown in Figure 6.3(b). The measured electrical parameters are threshold voltage of -2.4V, subthreshold slope of 0.9 V/decade, on-current of 28 μA and ON/OFF current ratio of 10^9. The areal ON-currents density reaches 0.4 A/cm^2 which is two orders higher than HVOTFT[25]. The electrical performance is slightly better than the HVTFT on glass, consisting of the MOCVD ZnO and PECVD SiO_2 structure. This is mainly attributed to the larger gate capacitor possessed by high dielectric constant material Al_2O_3, as well as the good interface between ALD Al_2O_3 and sputtering ZnO channel layer. The gate leakage current is at negligible level ($<10^{-12}$A) as shown in Figure 6.3(b).

The total trap density from the subthreshold slope (S.S.) can be estimated in the equation (6-2)[59]:

$$S.S = \log_e 10 \times \frac{k_B T}{q}\left(1 + q\frac{tN_{bulk} + D_{it}}{C_G}\right) \tag{6-2}$$

where q is the elementary electric charge, k_B the Boltzmann constant, T the temperature in Kelvin, t the channel thickness, N_{bulk} the bulk trap density, D_{it} the interface trap density, and C_G the capacitance per area of the gate dielectric layer (C_G is 8.23×10^{-4} F/m^2. The theoretical values of SiO_2=3.9 and Al_2O_3=9.30 are used

in this simulation). The total trap density includes the bulk trap (tN_{bulk}) and the interface trap (D_{it}), which are calculated to be 7.26×10^{12} cm^{-2}.

The blocking voltage test is shown in Figure 6.4, where the blocking voltage is around 92V. While gate bias increases, both gate current and drain current increase simultaneously, and the source current keeps similar. After the breakdown, the current flowing from drain to gate indicates that the major breakdown mechanism is related to the dielectric oxide breakdown. The slow increase of the gate current could result from the increase of defect in the bulk of dielectric layer. After the defects in the bulk of dielectric layer formed a conduction path, the oxide breakdown happened. Keneko et al.[77] reported IGZO channel/ SiN dielectric transistors for BEOL applications, and the breakdown voltage was linearly proportional to the thickness of SiN dielectric layer. Because of ZnO based materials have wider bandgap which have intrinsic high breakdown field, the dielectric breakdown determined the device breakdown.[78] However, to improve the quality of the dielectric layer, a high temperature growth or annealing process is critical. Lefevre et al.[79] demonstrated both the higher process temperature and post thermal treatment could improve the blocking voltage of Al$_2$O$_3$ layer. In our flexible HVTFT, the process temperature is limited below 120°C, so the critical field of breakdown must be lower than ideal value.

(a)

(b)
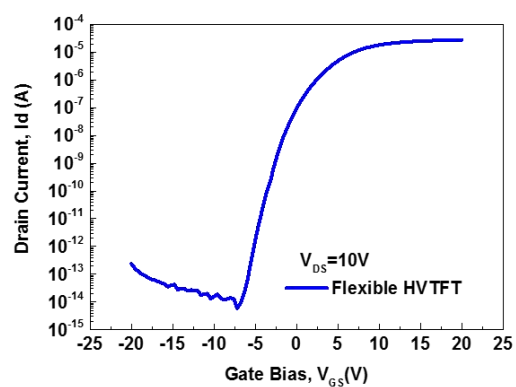
(c)
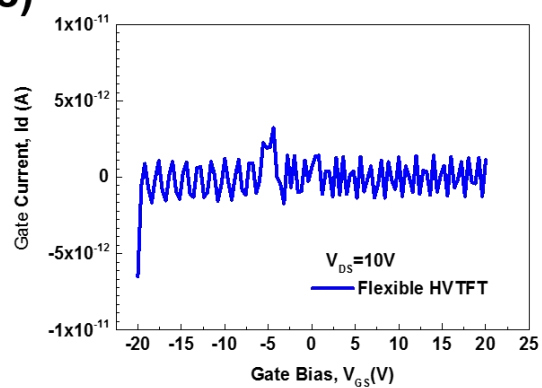
Figure 6.3 (a) The photo of (b) The transfer characteristics of, and (c) the gate leakage current of the flexible HVTFT on PEN substrate
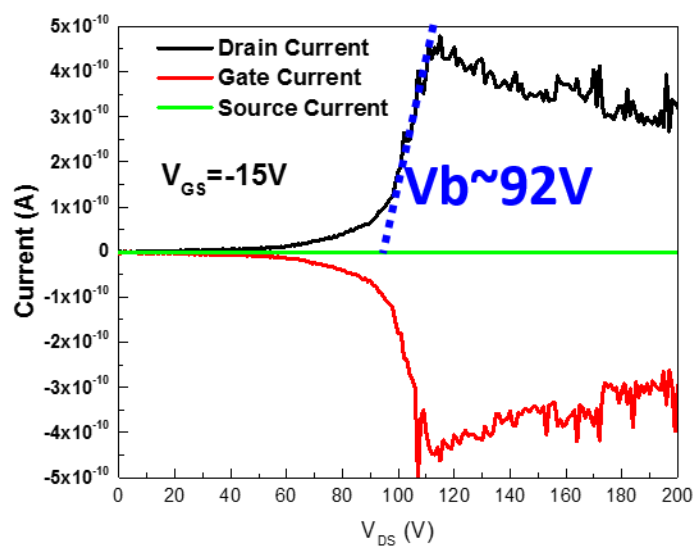
Figure 6.4 The blocking voltage measurement. The drain, gate, and source current are shown at the conditions of drain bias from 0 to 200V and gate bias of -15V.

6.4.3. Bending Effects on Electrical Performance

Several rods were used to bend flexible substrates to different radiuses of 3.35 cm, 3.06 cm, 2.9 cm, 2.75 cm, 2.50 cm, 2.35 cm, 2.13 cm, and 1.97 cm. There were U-shape metal stands to stabilize the rods. The PEN substrates were bended to the surface of rods and fixed by Kapton tapes. The bending platform is shown in Figure 6.5. The strain is parallel to the channel, and the direction is downward.

There were two types of bending tests. The first one was the dynamic measurement that the electrical measurement was done while the devices was under bending. The second one was the statistic measurement that electrical measurement was executed while the devices was flatten after bending.

Due to the lack of accurate measurement of Al_2O_3 mechanical properties, we adopted a simplified strain model without considering Young's modules of films. The strain values mentioned in this articles are calculated based on following equation (6-3) [80–82]. The corresponding strains are summarized in Table 6-1.

$$Strain\ (\%) = 100 \times \frac{Thickness\ of\ PEN + Thickness\ of\ TFT}{2 \times R_C} \qquad (6\text{-}3)$$
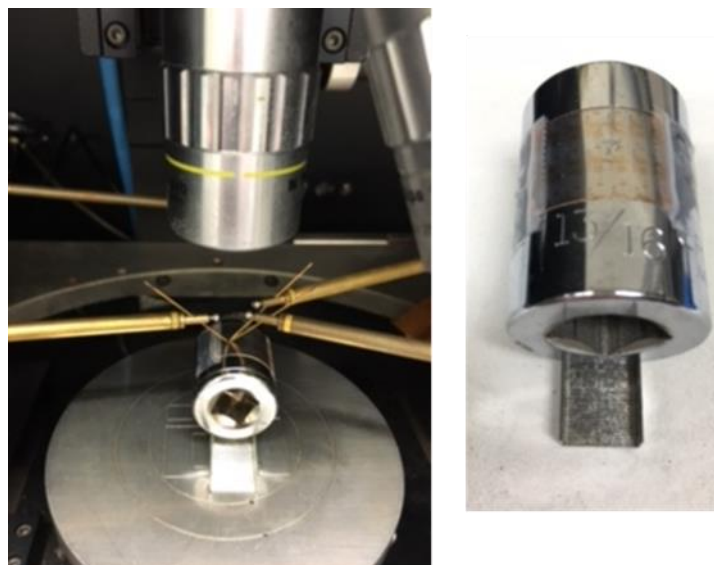
Figure 6.5 The setup of bending test of flexible HVTFT.

Radius (cm)	3.35	3.06	2.9	2.75	2.5	2.35	2.13	1.97
Strain (%)	0.19	0.20	0.22	0.23	0.25	0.27	0.29	0.32

Table 6-1 Corresponding Strain to different radius of the rods.

6.4.4. Dynamic Stress Testing on Electrical Characteristics

The electrical characteristics were simultaneously measured while the devices were bended. While HVTFT was under bending strain of 0.27%, the electrical characteristics still had a normal transistor-like behavior as shown in Figure 6.6 (a) but with a degradation of subthreshold slope, reduction of on-current and positively shift of threshold voltage. The off-current also increased. The degradation of on-current could be related to the reduction of the mobility which was affected by the strain field. Deflection of ZnO, as a piezoelectric material, creates a piezoelectric potential field. For the downward bending, the dielectric-channel interface was stretched, so the tensile strain was applied to the interface. He et al.[83] showed that tensile strain created positive potential, so the surface potential raised. Therefore, threshold voltage shifted positively, and mobility degraded.[80]

Larger the bending radius was, more serious the degradation of electrical characteristics was. When the bending strain increased to 0.32%, the HVTFT showed abnormal electrical characteristics that the on/off current ratio dropped from 10^8 to only 10^2. It was not only because of the strain field but also related some defects generated by the bending. The impact of the defects were still existed in ZnO HVTFT after being flatten which would be discussed in the following section.

(a)
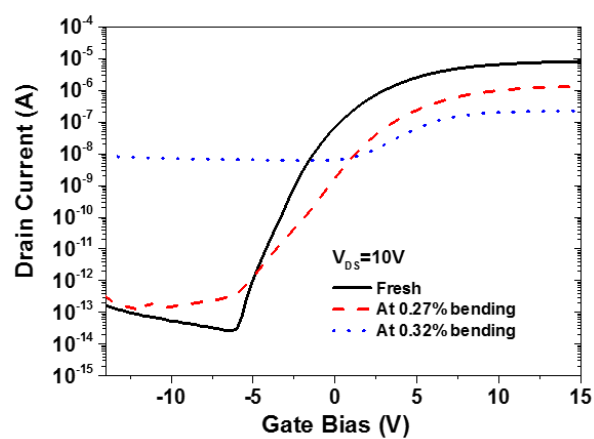
(b)
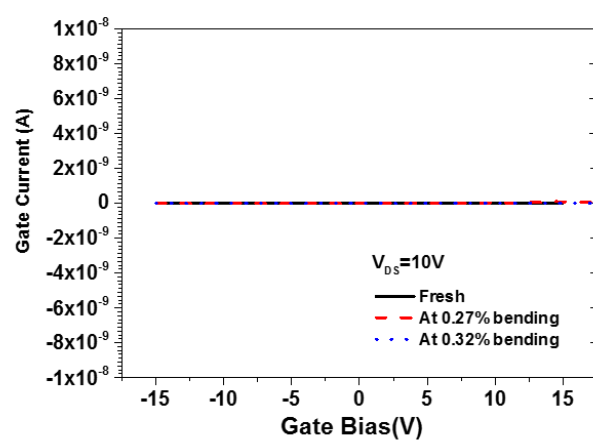
Figure 6.6 (a) Transfer characteristics and (b) gate leakage current of flexible HVTFT at different bending status.

6.4.5. Static Stress Testing on Electrical Characteristics

The transfer characteristics and the gate leakage current of flexible HVTFTs after bending of 0.27% strain were measured as shown in Figure 6.7 (a) and (b). It showed that the bending below 0.27% didn't affect the electrical characteristics of flexible HVTFT as long as the devices returned to flat status. Figure 6.7 (c) and (d) showed the electrical characteristics of flexible HVTFT after bending of 0.32%. After 1st strain of 0.32%, the electrical characteristic of ZnO flexible HVTFT measured at flat state didn't show a significant difference but a slightly negative shift in threshold voltage. However, the gate leakage current shown in Figure 6.7(d) indicated that the gate leakage actually increased at high gate bias. This increases in leakage current wasn't observed while the ZnO flexible HVTFT still at bending state. We suspected that the numbers of cracks in the bulk of the dielectric layer increased during the bending process, even in the unbending process. These cracks could form a leakage path for electrons to penetrate the dielectric layer, so the gate leakage current increased after several bending test.

As more bending operations were applied on the HVTFT, the gate leakage current increased further. The large bending would induce a permanent defects in the dielectric layer which were not recoverable even returning to the flat status.
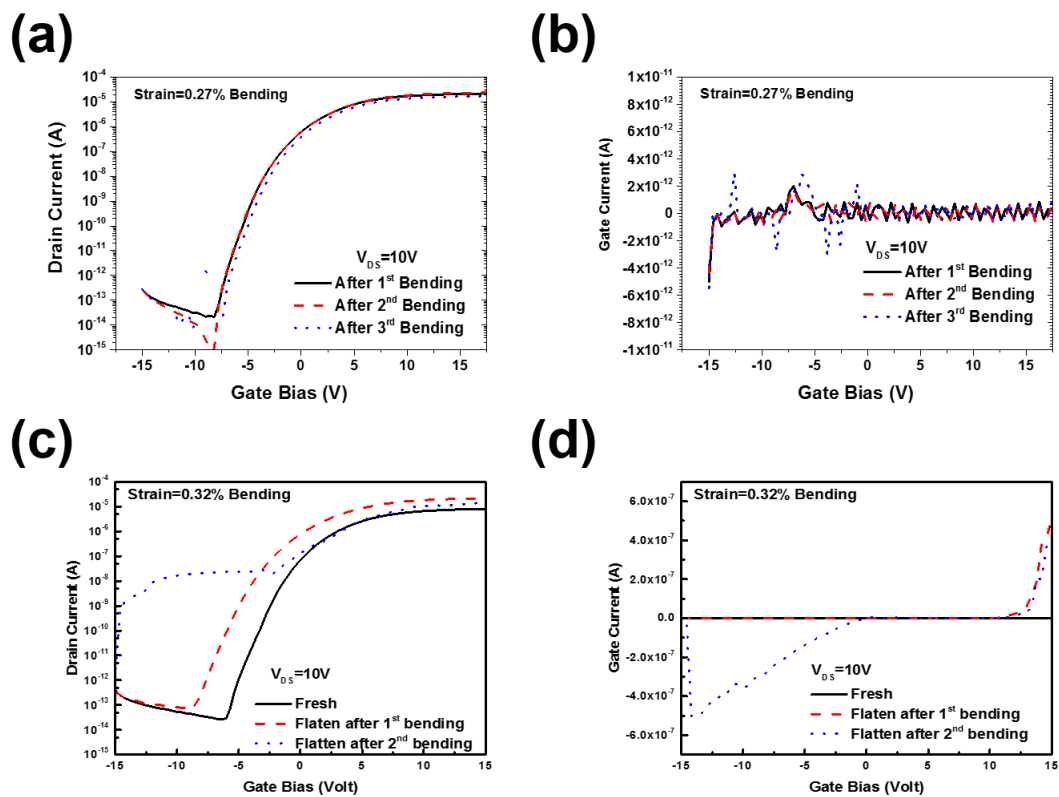
Figure 6.7 (a) The transfer characteristics and (b) gate leakage current of ZnO flexible HVTFT at flat status after bending strain of 0.27%. (c) The transfer characteristics and (d) gate leakage current of ZnO flexible HVTFT at flat status after bending strain of 0.32%

In the bending test, the major breakdown mechanism of flexible HVTFT was related to dielectric breakdown in both static and dynamic bending test, and it could also result from the mechanical strain which resulted in the cracks of the dielectric layer after large bending. There are several possible reasons for the formation of cracks. The first reason could be related to the lack of supporting substrate. Because of the thick substrate, we processed the flexible HVTFT without attaching flexible substrate on a fixed substrate. The free-standing plastics substrate not only made the wafer handling difficult but also potentially increased the risk of unintentional bending of the devices during the fabrication process. These extra wafer bending contributed to the additional degradation of the Al_2O_3 dielectric layer. The second main reason is the intrinsic property of Al_2O_3 film: high young's modulus. The Al_2O_3 young's modulus is 168 GPa[84], in comparison with HfO_2 of, SiO_2 of 70 GPa[74], and SiN of 210 GPa [74]. To prevent cracking, the total thickness is limited to minimum the strain. In the meantime, the dielectric thickness couldn't be too thin, or the blocking voltage decreases due to the reduced critical voltage of dielectric breakdown. As mentioned in previous paragraph, a higher deposition temperature is critical for improving the quality of Al_2O_3. However, a high temperature process also introduce higher strain. As a result, the optimization of the ALD Al_2O_3 growth conditions for the dielectric layer, such as temperature, film thickness are very critical. The other solution is to replace Al_2O_3 with more resilient dielectric film, such as SiO_2, polymer, hybrid film of hybrid of SiO_2 and silicone polymer[85].

6.5. Summary

In this chapter, we studied a compact and flexible ZnO HVTFT fabricated at low temperature ($\leq$100°C) on a plastic substrate (PEN). To be compatible with the low permitted process temperature of PEN substrate, we developed a RF sputtering ZnO channel at room temperature to replace MOCVD ZnO growth at 400°C. Although sputtering ZnO TFT showed 30% less ON-current and slightly worse subthreshold slop, it still showed a good performance for being used in the flexible HVTFT. Meanwhile, the ALD Al_2O_3 deposited at 105°C was studied to alter the PECVD SiO_2 deposited at 400°C. The good electrical performance indicated that ALD Al_2O_3 provided an enhanced channel-dielectric interface which improved the field-effect mobility by reducing the surface scattering.

Finally, the sputtering ZnO with ALD Al_2O_3 HVTFT were demonstrate, and it processed a sufficient on-current (~0.4 A/cm^2) and a high blocking voltage of 92V which matched well with the output characteristics of the nano-generators for power management requirement to the wearable systems. From the dynamic and static bending test, the flexible ZnO HVTFT showed degraded electrical performance while it was under bending. However, as long as the bending is less than 0.27%, flexible ZnO HVTFT recovered to its original electrical performance after being flatten. Overall, these preliminary results demonstrated the feasibility of flexible ZnO HVTFT.

Chapter 7 Conclusion and Suggestions for Future Work

7.1. Conclusion

The PV system on glass (PV SOG) technology is emerging to enhance the popularity of solar energy technology and stimulate its adaption. . The PV-SOG combines the advantages of micro-inverters, system-on-glass (SOG) and Building Integrated Photovoltaics (BIPV); therefore, it offers the promising features of high efficiency, low cost, and aesthetic appearance. However, the conventional high voltage transistors used in solar inverters couldn't meet the requirement of PV-SOG. The goal of this dissertation research is to study and develop a new high voltage transistor - MZO HVTFT which is suitable for the inverters in the PV-SOG.

In this dissertation, there were three phases to develop a stable and highly efficient ZnO-based HVTFT technology. The first phase was to solve the instability of TFT using the pure ZnO as the channel material. It was demonstrated that the thermal and biasing (especially NBS) instability issues were caused by   high concentration of oxygen vacancies in ZnO. A small amount of Mg was added into ZnO to form MZO channel layer. This Mg doping not only kept the superior electrical performance but also significantly improved the NBS stability. Unlike the traditional approach to use thermal annealing to improve the TFT stability, the new MZO channel doesn't require additional thermal treatment; therefore, reduces the overall thermal budget, which is particularly beneficial to SOG technology. In comparison with ZnO TFT, MZO TFT shows 30% less bulk defect density, and the threshold voltage shift after two hours NBS stress was only 30% of the shift in the

pure ZnO counterpart. The MZO TFT established a solid foundation for further development of high voltage devices.

The second phase was to design a circular structure dedicated for high voltage applications. A circular structure resolved the electrical field crowding in the conventional TFTs with a rectangular configuration. From the SILVACO simulation, the electrical field was more uniform in the circular structure than in the rectangular structure, and the peak electrical field was reduce by 50% in the circular structure in comparison with the rectangular structure. Lower peak electrical field allowed circular structure sustains higher bias conditions, so the blocking voltage increases.

The third phase was to conduct the design and engineering of the gate dielectric/channel interface in HVTFT. Although the circular MZO HVTFT showed on/off ratio of 6.1×10^7 and blocking voltage of 90V, the voltage was still below the high-voltage requirement of solar inverter. From the SILVACO simulation, the low blocking voltage was suspected to be related to the positive charges in SiO_2 dielectric layer. The positive charges in dielectric layer increased the peak electrical field in the channel, so the blocking voltages dropped. To improve the blocking voltage, we inserted an ultra-thin MZO transition layer (MZO-TL) through *in-situ* modulation doping between MZO channel and SiO_2 gate dielectric layer to form a new channel layer called m-MZO. This MZO-TL suppressed the Zn diffusion, so the amount of trapped Zn positive ions in the SiO_2 dielectric layer were reduced. The transfer characteristics showed that this modification improved the subthreshold slope and positively shifted threshold voltage close to 0V. As a result,

the regular m-MZO HVTFT (channel length=10μm) has on/off ratio of 3.5×10^{10} and blocking voltage of 305V which is suitable for the regular AC 110V power system. The longest m-MZO HVTFT (channel length=25μm) has on/off ratio of 3.3×10^{9} and blocking voltage of 609V which is suitable for the regular AC 220V power system.

To understand the roles of the MZO transition layer, a comprehensive characterizations was executed, including electrical and material analysis. By using XPS and TEM/EDS to analyze the depth profiles of elements, the interdiffusion of Zn and Si was observed clearly. The effect of MZO transition layer on suppressing the interface diffusion was also clearly demonstrated. Several optimization of MZO transition layer, including thickness, growth condition, doping profile, were studied. They showed that addition of MZO transition layer not only improved the blocking voltage but also modified dielectric/channel interface. Moreover, the damage of Zn diffusion to the SiO$_2$ layer was reduced by the transition layer, so the quality of the dielectric layer was improved.

To apply the concept of embedded power management to more applications, we further extended the HVTFT technology from on-glass to on-flexible substrates. The materials deposited at low temperature, RF sputtering ZnO and ALD Al$_2$O$_3$, were used to fabricate the ZnO-based flexible HVTFT on plastic substrate. The ZnO flexible HVTFT showed high on/off ratio of 10^9. Although blocking voltage of 92V was slightly lower than the requirement of 120V from triboelectric nano-generators, ZnO flexible HVTFT still showed a great potential of being utilized in the emerging self-powered wearable systems.

In summary, the work demonstrated that MZO based HVTFT on glass is feasible for the distributed micro inverters in an integrated PV-SOG. Our preliminary results also show that the HVTFT can be fabricated on the flexible substrate, which would significantly expand applications into flexible electrons and wearable electronics. Overall, this novel MZO HVTFT technology may lead to a broad impact on embedding high voltage power management systems used in both personal and home facility scales.

7.2. Suggestions for Future Work

Although lots of work have been done in the area of silicon based HVTFT, the development of oxide semiconductor based HVTFT is actually just starting. Most works in thesis dissertation just demonstrated the novelty, feasibility, and great opportunities of MZO HVTFT technology. To realize the full potential of the MZO HVTFT in power management applications, there are still many issues which need to be thorough investigated? The following topics are suggested for further study to develop the HVTFTs the on glass, flexible HVTFTs, and the transparent HVTFT for the integrated power management system.

7.2.1. Optimization of HVTFTs on glass

In order to improve the efficiency of the solar inverters, the on-current MZO based HVTFT has to increase. The simplest way is to increase the channel conductivity. However, the on-current and blocking voltage are trade-off, so increasing channel conductivity may also lead to the decrease of the blocking voltage. To have a better balance, the modification can focus on the dielectric layer. As shown in the experimental result, the breakdown mechanism of m-MZO HVTFT

was channel breakdown, instead of oxide breakdown. By replacing SiO_2 with some high k materials for the dielectric layer, the on-current can be enhanced because of the increase of gate capacitance. In the meantime, the physical thickness of dielectric layer can still be kept, so the blocking voltage remains at the similar level.

Another efficient way to improve the on-current is to shrink the offset region. By increasing the gate controlled channel area, the channel resistance decreases at on state and the current crowding effect can be mitigated. As shown in the simulation, the gate-to-drain offset area was responsible for sustaining high voltage bias. If the gate-to-drain offset decreases, the blocking voltage will drop seriously. On the other hand, the gate-to-source offset had little voltage drop in the simulation. By eliminating the gate-to-source offset, the blocking voltage should not be affected. In the meantime, the on-current is enhanced.

7.2.2. Improvement of flexible HVTFTs

For the huge potential market (projected global market of US$30.6 billion by 2020), lots of resources have been invested in the wearable electronics. While many issues have been addressed, the power supply is the main topic. To improve the user experience and practicability, self-powered system was proposed. While many energy harvesting and battery technologies for self-powered system are developed, an integrated power management is rarely studied. For the power management, a flexible high voltage transistor is needed, and the flexible ZnO HVTFT in this dissertation showed a great potential to provide a high efficient and low-cost solution to this need. In order to realize its full potential, more works are needed.

From the blocking voltage test and bending test, the quality of the dielectric layer dominates the performance of flexible HVTFTs. To prevent the early oxide breakdown, the thickness of dielectric layer should increase, but it's easier to form cracks in a thicker dielectric layer. The optimization of the thickness and growth condition of the dielectric layer is necessary for the improvement of flexible HVTFT. Studying other more ductile high-k materials is another possible solution to this issues. Moreover, to prevent the degradation from the bending, we should develop a bonding process to attach plastic substrates on fixed substrates during the fabrication process. It can prevent some unintentional bending and extend the life time of flexible HVTFT. By improving the dielectric layer, the overall performance of flexible HVTFT will be enhanced, especially in blocking voltage.

Although the criteria of standard life span of wearable electronics is not as high as basic facilities, such as solar cells, are. It is still very important to develop a stable and flexible devices. As we did in the HVTFTs on glass, a small amount of Mg should also be added into ZnO sputtering ZnO. Two possible ways should be studied: directly sputtering of MZO target and co-sputtering of MgO and ZnO targets. Directly sputtering of MZO target can skip the optimization of ratio of MgO and ZnO sputtering; it is harder for the sputtering of single target to adjust Mg composition easily which is essential to create a gradual profile as HVTFT on glass.

Another important topic is to understand the bending effect. Although the basic analysis of the bending effect on the electrical performance of flexible ZnO HVTFT had been done, the simple setup of bending test platform restricted us to gather more date, such upward bending, more different bending angles. In order

to make a comprehensive study of bendability, an automation testing platform is necessary. A practical way to create more bending conditions is to utilize 3D printing for making more rods of different radius and bending surface, including both upward or downward directions. In the meantime, the simulation software should also be used to analyze the bending effect on the carrier transportation and the breakdown mechanism. It can provide us better ideals to explain bending effect on the electrical performance. This understanding will be important for future studies and improvement to the flexible HVTFTs.

7.2.3. Development of fully transparent HVTFT

To be used in Building-integrated photovoltaics (BIPV), aesthetical appearance plays an essential role, so Tesla developed a BIPV solar roof which mimics French slate and Tuscan clay tiles. However, this application is limited to the roof tile. For the general solution for BIPV, a transparent appearance can be applied to much more building fabrics. Meanwhile, for the smart glass application, a transparent appearance is a must. On the other hand, wearable electronics as part of fashion, have even more request on the exterior appearance. As a result, transparent devices are strongly demanded by BIPV, smart glass, and wearable electronics.

Even though both m-MZO HVTFT on glass and flexible HVTFT on plastic substrates already showed good transparency, devices were still semi-transparent instead of fully transparent. The problem came from the electrodes which were formed by opaque metal materials. Because the electrodes can easily occupy more than 30% area of the whole devices, this issue seriously affects the overall

transparency. To solve to problem, gallium doped ZnO (GZO) or aluminum doped ZnO (AZO) are great candidates to form transparent electrode. GZO and AZO both have good conductivity and transparency, and they can be deposited by RF sputtering at low temperature and lower cost. The low process temperature is very critical for MZO HVTFT to be used in the PV-SOG and wearable electronics. By introducing transparent conducting oxide, we can develop a fully transparent MZO based HVTFT technology.

7.2.4. Integration of HVTFT towards PV-SOG

Depletion of fossil-fuel energy and global warming forced humanity to focus on renewable energy, and solar energy is dominant in sustainable and clean energy source. PV-SOG was proposed to further improve the adoption rate of solar power, and it possessed the features of micro-inverters, BIPV, and system-on-glass. The development of PV-SOG can provide a low cost, high efficient, and aesthetic solar energy technology.

Building a high efficient, low fabrication cost, and transparent HVTFT technology is a critical step toward solar inverters in PV-SOG. However, to demonstrate the feasibility of PV-SOG, a system level integration of solar cells, control circuit, and solar inverters is necessary. The process of control circuit can be based on MZO regular TFT which is identical to MZO HVTFT, so the bottlenecks of PV-SOG should be the integration of energy source and the power management system. Although the MZO HVTFT technology is compatible with regular low temperature process, there are still many issues of building PV-SOG, such as devices isolation, inter-connection, control of thermal budget.

In the beginning stage, the integration of the fabrication process can be separate. For example, after building the MZO based circuits for solar inverters and control circuits, the solar cells can be added through external connections. Through the system-level test of solar power output, the design of solar inverters and control circuits can be optimized. This study will help the development of full integration of the solar cell and MZO based circuits on a same glass substrate for PV-SOG. As a result, it becomes a real system-on-glass, and the fabrication cost can be reduced through the integrated fabrication process.

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Major Publications and Patent Applications

Journal Articles:
[1] H.Liang, Z.Mei, D.Ye, J.Li, **W.-C.Hong**, Q.Zhang, Y.Liu, L.Gu, R.Yu, Y.Lu, and X.Du, "Dual-functional crystalline BeO layer in enhancement-mode ZnO/Si thin film transistors," *Phys. status solidi - Rapid Res. Lett.*, vol. 1600443, p. 1600443, 2017.

[2] **W.-C.Hong**, C.-J.Ku, R.Li, S.Abbaslou, P.Reyes, S.-Y.Wang, G.Li, M.Lu, K.Sheng, and Y.Lu, "MgZnO High Voltage Thin Film Transistors on Glass for Inverters in Building Integrated Photovoltaics," *Sci. Rep.*, vol. 6, no. October, p. 34169, Oct.2016.

[3] C.-J.Ku, **W.-C.Hong**, T.Mohsin, R.Li, Z.Duan, and Y.Lu, "Improvement of Negative Bias Stress Stability in $Mg_{0.03}Zn_{0.97}O$ Thin-Film Transistors," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 914–916, Sep.2015. *(C.-J. Ku and W.-C. Hong contributed equally to this work.)*

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