ORGANIC MICROELECTROMECHANICAL RELAY TECHNOLOGY FOR ULTRALOW-POWER FLEXIBLE TRANSPARENT LARGE-AREA ELECTRONICS

by

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A dissertation submitted to the

Graduate School-New Brunswick

Rutgers, The State University of New Jersey

In partial fulfillment of the requirements

For the degree of

Doctor of Philosophy

Graduate Program in Electrical and Computer Engineering

Written under the direction of

Professor Jaeseok Jeon

And approved by

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New Brunswick, New Jersey

May 2017

ABSTRACT OF THE DISSERTATION

Organic Microelectromechanical Relay Technology for Ultralow-Power Flexible Transparent Large-Area Electronics

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Much research to date has focused on synthesizing new polymers or improving existing polymers, in order to overcome the limits of the conventional organic thin-film transistor (OTFT): (1) A rather low channel carrier mobility (< 20 $cm^2V^{-1}s^{-1}$ typically) requires a power supply voltage well above 2 V for a reasonable on-/off-current ratio (> 10^5); (2) The formation of a relatively poor-quality interface between the polymeric channel and gate insulator induces large off-state leakage current well above 10^{-13} A; (3) Asymmetric pairs of *n*- and *p*-type OTFTs result in noncomplementary switching. All these would affect the overall power consumption at the transistor, circuit, and system levels. This doctoral dissertation proposes and demonstrates radically-different, organic microelectromechanical (MEM) relays, in order to overcome such limits and hence enable efficient implementation of portable and/or wearable large-area electronics for the internet of things requiring ultralow-power operation, structural flexibility, visual

transparency, and low-cost/-temperature processing. Firstly, a polymer-based low-thermal-budget surface-micromachining process is developed to implement organic relay prototypes (comprising multiple or single input/output terminals). Fabricated relays exhibit unique *I*-*V* characteristics including immeasurably-low off-state leakage current, abrupt transitions to the on-/off-state with an input voltage swing less than 60 mV for a decade change in output current, a relatively high on/off current ratio well above 10^5, and complementary switching behavior and can endure a finite number of hot- and cold-switching cycles. Secondly, the effects of humidity, temperature, and low-surface-energy contacting electrodes materials on switching characteristics (such as hysteresis voltages and on-state resistance) are investigated. Thirdly, basic Boolean operations including AND, OR, and XOR and logic functions (*e.g.*, carry bit generation for four inputs) are demonstrated using a multi-input/-output relay.

ACKNOWLEDGEMENT

First, I would like to express my sincere, cordial, and deepest appreciation to my Ph.D. advisor Prof. Jaeseok Jeon for his unbounded enthusiasm, encouragement, patience, support, and guidance in my research towards completing my Ph.D. study at Rutgers. This is an enjoyable, inspiring and unforgettable memory in my life. My special thanks go to my dissertation committee members, Prof. Leonard Feldman, Prof. Yicheng Lu and Prof. Zhixiong (James) Guo for their enthusiastic serving on my dissertation committee and their evaluations and suggestions on my research work.

It is my pleasure to work with selfless and professional people in this project. I would like to thank Fangzhou Yu and Sourav Sagar for helping me with design and fabrication. Their insightful visions and suggestions make this project come true. I would like to thank Zhengyu Yang and Nabeela Khan for their assistance in simulation. I would also like to thank Wen-Chiang Hong and Siamak Abaslou for their suggestions in device testing.

The fabrication experiments were done in both Microelectronics Research Laboratory (MERL) of Rutgers University and Center for Functional Nanomaterials (CFN) of Brookhaven National Laboratory. I would like to thank all the staffs and co-workers in these two places, special thanks to Dr. Ming Lu, Dr. Aaron Stein, Dr. Chang-Yong Nam, Dr. Fernando Camino, Dr. Pavel Reyes, Dr. Yi Xu, Dr. Luozhou Li, Dr. Spencer Porter, Robert Lorber, Rui Li, Jiabao Zheng, Gwen Wright for their training and valuable advice on my project.

Last but not least, I am tremendously grateful to my parents and my wife for their support and encouragement. There are many difficult times during the Ph.D. study that make me start to double my abilities and decision. However, their enormous support helps me to strive for and fight through. I am truly blessed to be accompanied with my families.

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1. Introduction

The key idea of Internet of Things (IoT) is that electronic signal-acquisition and -processing systems (including sensors, actuators, and computers) we use today can be connected together wirelessly to incorporate the physical world into the internet network for more efficient collection, processing, and distribution of information [1]. New dimensions will be added to the world of information and communication technologies, and as a result, such IoT-based developments are expected to transform our daily lives significantly.

The IoT entails very broad vision. Many smart enviroments can be involved within the infrastructures of IoT (Figure 1.1), for example, wearable systems, smart buildings and vehicles, more broadly, smart industries and cities [2]. There are billions of applications

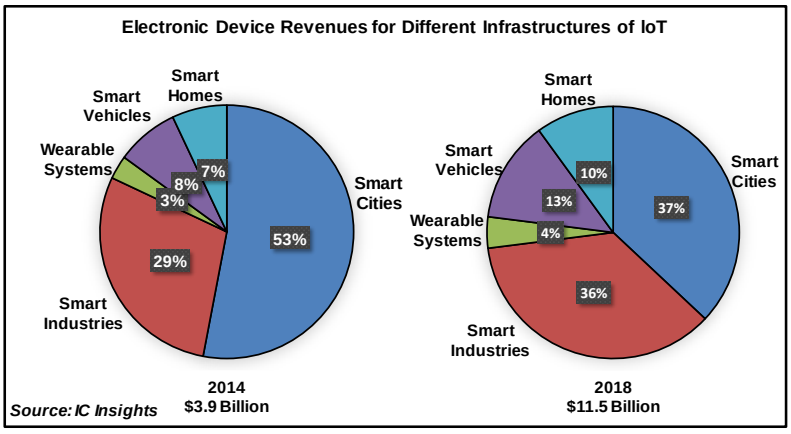

Figure 1.1 Adapted from [2]: The worldwide revenues of electronic devices used in different infrastructures of The Internet of Things (IoT). Smart cities, smart industries, smart vehicles, smart homes, and wearable systems are the main infrastructures of IoT. The revenue of electronic devices required in these infrastructures is 3.9 billion in the year of 2014. It is estimated to increase 195 % and reach 11.5 billion in the year of 2018.

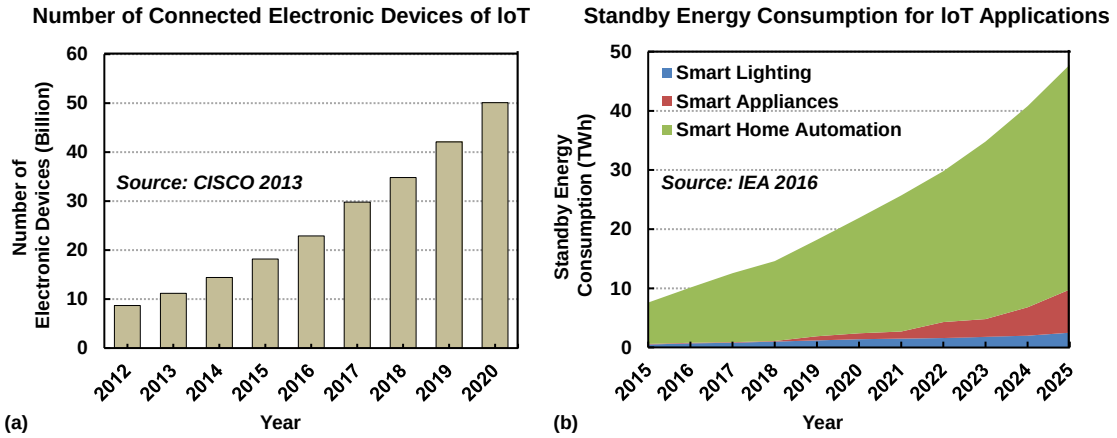

Figure 1.2 (a) Adapted from [3]: The growth forecast of connected electronic devices of IoT. The number of connected electronic devices is 23 billion in the year of 2016, but it is estimated to reach 50 billion by 2020. (b) Adapted from [4]: The standby energy consumption of electronic devices used in different main IoT applications. It is predicted that the standby power consumption of main IoT electronic devices reach 46 TWh in 2025, which equals to the annual electricity usage of Portugal in the year of 2012.

that could lead to these kinds of IoT enviroments, and many of these applications require one or several semiconductor devices including radio frequency identification tags (RFID), sensors and actuators, memory, display systemsm, *etc*. Mass-manufactured large-area electronics implemented on very thin and flexible plastic substrates, for example, can be one of the enabling technologies in that, any electronics, in principle, could be attached to the surface of any physical platforms. According to Figure 1.1, IoT industry is expected to see a very strong growth in the coming years from 3.9 billion in the year of 2014 to 11.5 billion in the year of 2018.

As the revenue of electronic devices required for IoT grows, an increasing number of electronic devices will be manufactured and used in our daily lives. As predicted in

Figure 1.2(a), while there are approximately 23 billion IoT electronic devices connected in the year of 2016, this number is forecasted to increase to more than 50 billion by 2020. Achieving high energy-efficiency would be of importance when such a large number of devices are connected and used for IoT applications. To assess the potential impact of IoT applications on energy consumption worldwide, research data on the standby power consumption of selected IoT devices is indicated in Figure 1.2(b). It is expected that the standby energy consumption of such IoT electronics would increase with annual growth rate of 20 % and surpass 46 TWh in 2025, which equals to the annual electricity consumption of Portugal in the year of 2012. More than 50 billion electric devices will be connected by 2020, and they would consume $120 billion energy.

To integrate that large number of electronic devices, IoT drives a huge demand for low-power/-cost devices that can save manufacturing costs and reduce global energy consumption. In this regard, various technologies that can achieve low manufacturing costs and low power consumption are already established or emerging for the realization IoT applications. One of these promising technologies is the organic thin-film transistor (OTFT). OTFT has been extensively researched over the past decades as an alternative or complement to conventional inorganic TFT in order to realize applications where large area coverage, low temperature processing, low cost, and structural flexibility are required. Recent advances in polymer synthesis and processing [5], together with advancements in polymer microfabrication technology, have recently enabled the implementation of OTFT in several IoT electronics recently including RFIDs [6], organic

light emitting diodes (OLEDs) [7], organic nonvolatile memory [8], radio frequency (RF) sensor [9], *etc*.

1.1. Status Quo: Organic Thin-Film Transistor Technology

In 1986, Tsumura *et al*. [10] introduced the first OTFT, which used organic semiconductor material as the active layer for the channel. Since then, the performance of OTFT has undergone significant improvements, and OTFT has now been considered as one of the promising semiconductor devices for the realization of low cost, low temperature, large area, and flexible electronic systems used for IoT [11-15]. The low temperature process (typically less than 200 °C) of organic materials makes OTFT suitable for implementation on various flexible substrates (*e.g.*, papers and plastics), which is otherwise not easy to be realized with conventional inorganic materials [12, 16].

Depending on the sequence in which different layers are deposited, there are mainly four different OTFT architectures as shown in Figure 1.3. The OTFT can be implemented on

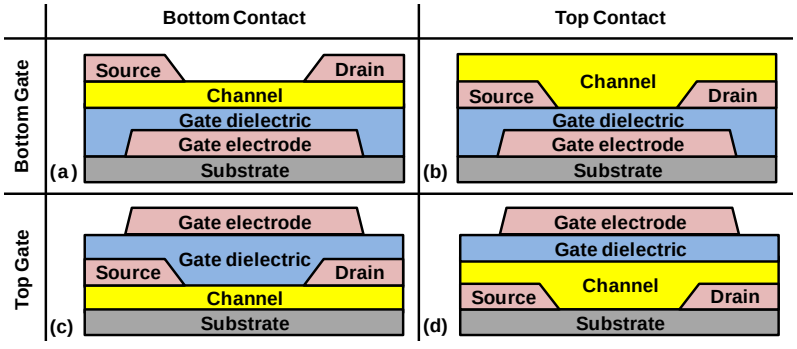

Figure 1.3 Schematic cross-section views of (a) Bottom gate bottom contact (BGBC) (b) Bottom gate top contact (BGTC) (c) Top gate bottom contact (TGBC) and (d) Top gate top contact (TGTC) OTFT.

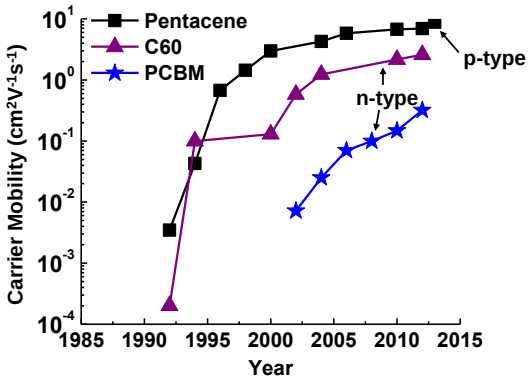

Figure 1.4 The development of the field-effect carrier mobility (μ) in some common *p*- and *n*-type semiconductors over the past decades [14].

an insulating substrate (*e.g.*, glass or plastic substrate), while an organic semiconductor material is used as a channel layer (which is also called the active layer), and inorganic and/or organic conducting materials are used for the gate and source/drain electrodes. Different OTFT structures as shown in Figure 1.3 have pros and cons [17]. The majority of OTFTs follows the bottom gate structure (Figures 1.3(a) and (b)) for the following reasons: (1) The deposition of organic semiconductor layer after the gate dielectric provides a wider process window for the growth of the high quality dielectric layer (that requires high temperature deposition or thermal treatment) without degrading the sensitive active layer [14]; (2) The deposition and patterning of the metal gate (that could involve high temperature treatments and require organic solvents) might contaminate the organic active layer underneath when the gate electrode is formed in the last step [12].

Figure 1.4 demonstrates the increase in field-effect carrier mobility (μ) of both *p*- and *n*-type semiconductors over the past decades. In fact, much research has been performed in order to improve such a relatively low mobility (< 20 $cm^2V^{-1}s^{-1}$ typically) of organic

semiconductors and thus to improve the performance of OTFT [12-15]. This is because the drain current-gate voltage (I_d-V_g) characteristics and intrinsic delay (f_t) of OTFT depend on the μ of the semiconductor layer:

$$I_d = \frac{W}{L} C_{dep} \mu \left(V_g - V_t - \frac{V_t}{2} \right) V_d \qquad \text{(When } V_d \le V_g - V_t \text{)} \tag{1-1}$$

$$\text{or } I_{d,sat} = \frac{W}{2L} C_{dep} \mu (V_g - V_t)^2 \qquad \text{(When } V_d > V_g - V_t \text{)} \tag{1-2}$$

$$f_t \propto \frac{W}{2L} \mu (V_g - V_t) \tag{1-3}$$

where C_{dep} is the capacitance of the depletion layer, V_d is the applied drain voltage, V_g is the applied gate voltage, V_t is the threshold voltage, and W and L are channel length and width, respectively. High μ is strongly desirable in order to manufacture OTFT with high on-state current $I_{d,sat}$ [5, 18] and low signal propagation delay [12, 14, 19].

Another challenge that hinders the wide adoption of OTFT technology is related to the gate dielectric layer [20]. Gate dielectric layer is of importance because: (1) The gate dielectric prevents the leakage current between the gate and semiconductor layers [21]; (2) The gate dielectric serves as a passivation layer, which can protect the semiconductor layer in the case of the top gate structure, *i.e.* TGBC and TGTC OTFTs shown in Figure 1.3 [22]; (3) The charge carrier accumulation at the interface of semiconductor layer/dielectric is significantly affected by the properties of gate dielectric, *i.e.* morphology, surface condition, the constant, and the thickness of the dielectric layer [23].

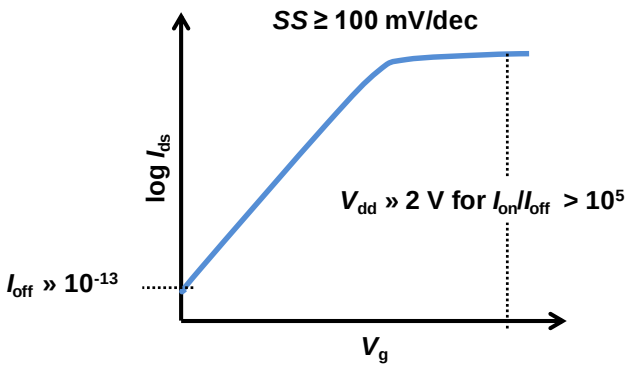

Figure 1.5 The conceptual I_{ds}-V_g characteristic of OTFT device showing the limited performances.

Generally speaking, large gate oxide capacitance (C_{ox}) is desirable to achieve a steep subthreshold swing (SS) [24-26]:

$$SS = \ln 10 \times \frac{k_B T}{q}\left(1 + \frac{C_{dep}}{C_{ox}}\right) \tag{1-4}$$

where k_B is the bolzman constant, T is the temperature, q is the elementary charge, C_{dep} is the capacitance of the depletion layer, and C_{ox} is the capacitance of dielectric layer. SS is fundamentally limited to be ln10 × k_BT/q = 60 mV/dec at room temperature and is typically greater 100 mV/dec for state-of-the-art OTFTs [27, 28].

To achieve a flexible OTFT, a suitable conducting polymer should be used as the electrode layer. So far, Poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) [29] and PANI (polyaniline blends) [30] are the most widely used conducting polymers for the formation of electrodes in OTFTs. However, the relatively low conductivity (~1 Ω·cm), air instability, and processing complexity make the use of conducting polymers for the realization of fully rollable OTFTs challenging.

There are several critical challenges for the application of OTFTs in organic electronics as shown in the typical I_{ds}-V_g curve of OTFT in Figure 1.5: (1) Organic semiconductors have a relatively low field-effect carrier mobility μ (well below 20 $cm^2V^{-1}s^{-1}$) [12-15]. Therefore, OTFTs tend to exhibit rather limited performance, *e.g.* V_{dd} well above 2 V (typically much above 10 V) is required to achieve reasonable on/off current ratio (> 10^5) [5, 18] and switching frequency (> 1 MHz) [12, 14, 19]. The large V_{dd} can lead to large amounts of dynamic power consumption; (2) Due to poor semiconductor/dielectric interface quality [24-28, 31], OTFTs show relatively large off-state leakage current (I_{off} is typically well above 10^{-13}), which would be exacerbated for small device dimensions in more intensive integrated circuits, particularly if a thin gate insulator is used to achieve a steep *SS*, which is well above 100 mV/dec [27, 28]. The large I_{off} can lead to large amounts of static power dissipation; (3) The large power consumption issue becomes aggravated at the circuit level as *p*-type OTFTs usually far outperform *n*-type OTFTs due to the fact that the μ of most *p*-type organic semiconductor is better than that of the *n*-type organic semiconductor and the air stability of most *n*-type OTFTs remain unsolved, all these factors makes it difficult to achieve complementary operations [14, 20]. While much work has been done to provide improved or new polymers and polymeric composites for active layers or gate dielectric layer or electrode layer in order to improve the performance of OTFTs [5, 18, 32-36], little work has yet been done (particularly at the transistor level) to reduce the overall power consumption in order to realize low power consumption of IoT electronics.

1.2. New Insight: Organic Microelectromechanical Relay Technology

Mechanical relays for computing was conceptualized by George Stibitz in 1930 [37]. With the advance of modern planar processing technology and micro-electro-mechanical systems (MEMS) technology over the past decades, it has become possible to fabricate miniaturized relays and integrate them on a single chip. The first micro-electro-mechanical (MEM) relay that turns on/off abruptly by making or breaking physical contact of two electrodes was demonstrated by Petersen in 1979 [38]. Such an abrupt switching behavior leads to high I_{on}/I_{off} ratio for a small given gate-voltage swing, and the existence of the air gap between contacting electrodes allows zero I_{off}. Recently, various MEM relay designs (such as laterally- [39-44] or vertically-driven relay structures [45, 46]) for logic application has been proposed to overcome the energy crisis of CMOS technology.

Figure 1.6 shows the structure of a simplified 3-terminal (3-T) MEM relay and the corresponding conceptual I_{ds}-V_g characteristic. The movable source of the MEM relay stands on the substrate and it forms a parallel plate capacitor with a fixed gate electrode underneath (Figure 1.6(a)). When $V_g < V_{rl}$, the relay is in the off-state, where there is an air gap between the source and drain electrodes preventing the current flow I_{ds}. As a result, the MEM relay has zero I_{off} as shown in Figure 1.6(b). When $V_g > V_{pi}$, the F_e between the source and gate electrodes attracts the movable source electrode towards the fixed gate electrode. The source then meets with the drain underneath abruptly. Therefore, the electrical contact is made and I_{ds} flows. The *SS* of the relay can be very close to zero, which enables the possibility of small applied voltage swing.

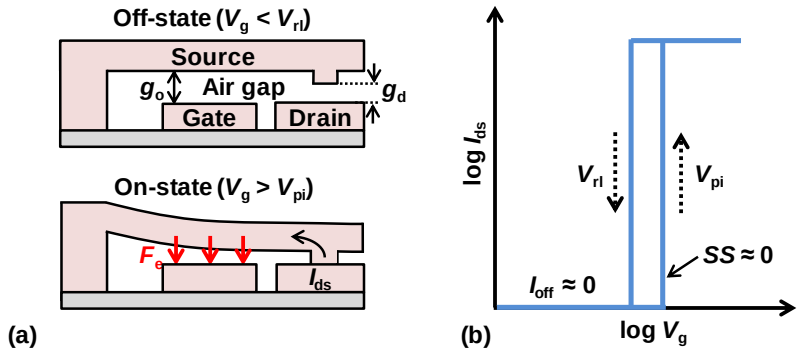

Figure 1.6 (a) Schematic illustration of a simplified 3-terminal (3-T) MEM relay. In the off-state ($V_g < V_{rl}$), V_{rl} is called the release voltage of the relay. The presence of air gap between source and drain electrodes prevents current flow I_{ds}, which results in zero off-state leakage. Actuation gap (g_o) is the air gap thickness between the source and gate. Dimple gap (g_d) is the air gap thickness between source to drain. In the on-state ($V_g > V_{pi}$), V_{pi} is called the pull-in voltage of the relay. The electrostatic actuation force (F_e) induced by the gate and source electrodes attracts the source to move downward so that the electrical contact between the source and drain is made, current flow I_{ds} is therefore formed, which leads to abrupt on-state transition. (b) The conceptual I_{ds}-V_g characteristic of MEM relay showing the relay has zero off-state leakage, it can turn on and off abruptly by a small gate-voltage swing with $SS \approx 0$. The hysteretic switching behavior (V_{pi}–V_{rl}) is due to pull-in mode operation and surface adhesion force (F_a) [39].

MEM relay could be considered as a promising switching device since it can provide zero static power consumption, potentially ultralow dynamic power consumption, and complementary switching operations. Specifically, a relay shows abrupt on/off transition behavior. *i.e.* when $V_g \geq V_{pi}$ is applied, the movable structure will be abruptly actuated to bring the source contact with drain electrode due to the induced electrostatic actuation force, and current can flow thereby, and when $V_g \leq V_{rl}$, the spring restoring force (F_{sp})

will bring the source out of contact with the drain electrode abruptly. As a result, relay can be made to operate with very low V_{dd} than OTFT in principle since the *SS* of relay is less than 0.1 mV/dec [47], while that of OTFT is typically well above 100 mV/dec [27, 28]. Relay has immeasurable low I_{off} and high on/off current ratio because the actuation air gap separates the source and drain when the device is in off-state, but the OTFT has relatively large leakage current due to poor semiconductor/dielectric interface quality and it consumes large static power consequently [31]. Due to the ambipolar nature of the electrostatic actuation force, it is always an attractive force between the movable electrode and fixed electrode regardless of the polarity of the applied voltage. Therefore, the advantage of electrostatic actuation switching behaviors of relay enables the symmetric pairs of *n*- and *p*-type relays for complementary operation. But complementary switching is still difficult to be realized by OTFTs simply due to the outperformance of *p*-type OTFTs to *n*-type OTFTs and the air instability of most *n*-type OTFTs [14, 20].

On top of the above intrinsic benefits of the MEM relay, an organic MEM relay could be compelling for the implementation of organic electronics with low power consumption and low manufacturing costs. Relay is operated by the electrostatic actuation of a movable electrode structure rather than by modulating the conductivity of a fixed semiconducting channel. Therefore, the performance of organic MEM relays will not be restricted by the limit of the relatively low μ of organic semiconductors. It is desirable to create relay with low effective spring constant (k_{eff}) to lower the switching energy needed to turn on the device [39]. The k_{eff} of the structural beam is proportional to Young's

modulus (*E)* of materials, and the threshold voltage (and hence operating voltage) of relays are proportional to $E^{0.5}$. Note that the *E* values of most organic materials are approximately two orders of magnitude lower than those of inorganic materials [48]. Along with zero leakage current, potentially very low operation voltage of organic MEM relays could make them appealing for ultralower-power applications. In addition, various polymers and/or light sensitive photoresists are commonly used in MEMS for mechanical structures/support or sacrificial layers [48]. They can be deposited via simple low-cost/-temperature methods (e.g., spin coating), unlike inorganic materials requiring relatively complicated film deposition- or etching-steps [49].

Organic MEM relay that could incorporate the advantages of mechanical relay structures, the salient properties of organic materials, and the low-temperature/-cost material processing, would be a promising candidate as the building block for ultralow power flexible, transparent, and large area electronics used in IoT.

1.3. Organization of the Dissertation

This Ph.D. dissertation aims to address challenges for achieving organic MEM relay technology that could be a promising alternative to OTFT for ultralow-power, flexible, transparent and large-area electronics.

Chapter 2 begins with the working principle of MEM relay. Then the prototype organic relay design is presented. Lastly, versatile multiple-input/-output relays including single-gate dual-body relay and dual-gate dual-body relay are introduced.

Chapter 3 discusses the fabrication process and materials to realize the implementation of organic MEM relays. The requirement, selection, and evaluation of the materials used for this work as well as fabrication challenges encountered and solution are presented.

Chapter 4 presents the characterizations of fabricated organic MEM relays. Static switching characteristics including I_{ds}-V_{gb}, I_{ds}-V_{ds}, body biasing effect, complementary switching, and hysteretic switching behavior, and dynamic performance including turn-on and turn-off switching delays are completely investigated. Endurance testing results show that organic MEM relays can endure a finite number of hot- and cold-switching cycles. The effects of temperature and humidity on switching characteristics (such as I_{ds}-V_{gb}, hysteresis voltages and on-state resistance) are studied. A dual-gate dual-body organic MEM relay that can perform basic logic functions and can generate a carry for four input bits is also is demonstrated.

Chapter 5 summarizes the key results and contributions of this dissertation.

2. Organical Relay Design and Simulation

MEM relay can be used to implement low-power organic electronics for IoT applications due to its unique behaviors such as abrupt on/off switching behavior that allows V_{dd} to be close to 0 V for low dynamic power consumption and zero off-state leakage current for zero static power consumption. Section 2.1 begins with a description of the structure and operation principle of a typical 4-Terminal (4-T) relay; this design has been proved to serve as a basic building block for various digital logic circuits including logic gates, clocking, memory circuits, adder and multipliers [43, 47, 50-54]. Based on this, the development of the organic MEM relay is discussed in Section 2.2, followed by the improvements made to the prototype (in Section 2.3).

2.1. Microelectromechanical Relay Structures and Operation Principle

The design of electromechanical relays is based on the mechanical motion of the movable structure that makes or breaks the physical contact between two electrodes in order to turn on or off [37, 55]. Two types of movable structures typically used in MEM relays are based on cantilever [56, 57] or clamped-clamped beam structures [44, 58, 59]. The cantilever beam has a fixed base (called “anchor”) on either side, and the buckled clamped-clamped structure has fix bases (anchors) at both sides. These two types of movable structures have advantages and disadvantages. Cantilever beam is relatively easier to fabricate than clamped-clamped beams but might not have sufficient spring restoring force (F_{sp}) that ensures the reliable turning-off of the relay. Clamped-clamped beam could be more complicated to manufacture, but provides more reliable F_{sp} to turn

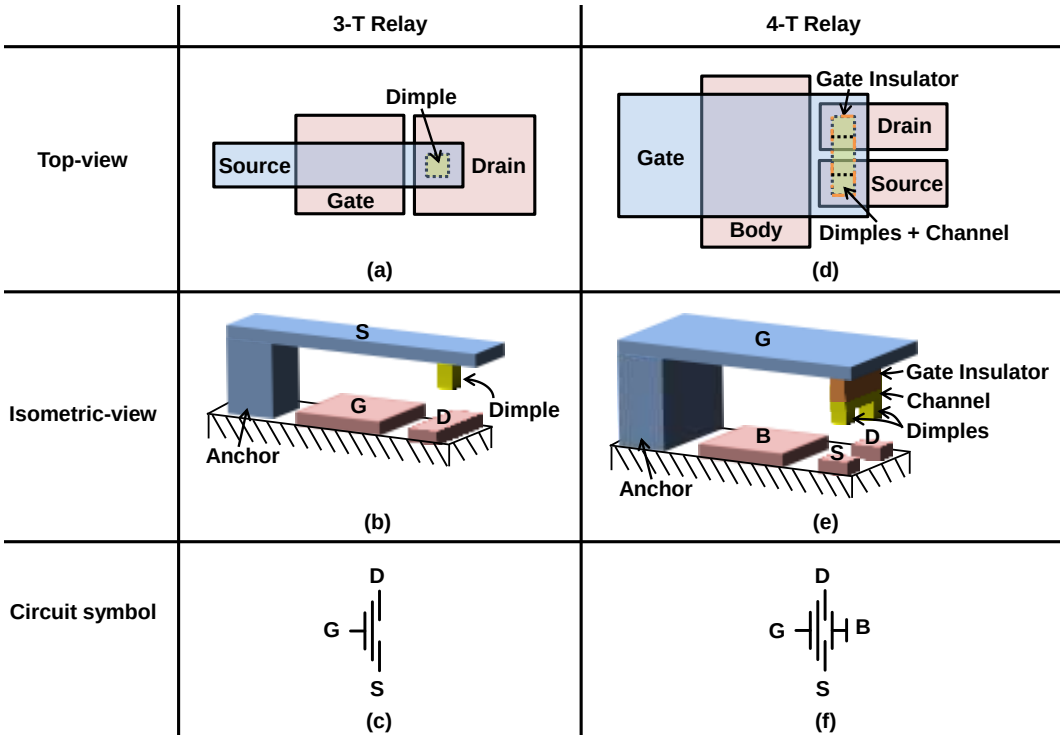

Figure 2.1 (a) Top-view, (b) Isometric-view, and (c) Circuit symbol of a 3-Terminal (3-T) relay. The 3-T relay comprises three terminals: a movable source, a gate, and a drain. The source electrode has one protruding region, referred to as dimple. The dimple restricts the motion of the movable source when it contacts the drain. (d) Top-view, (e) Isometric-view, and (f) Circuit symbol of a 4-Terminal (4-T) relay. The 4-T relay comprises four terminals: a movable gate, a body, a source, and a drain. The channel beneath the gate insulator has two protruding regions, referred to as dimples. The dimples restrict the motion of the movable gate when they contact the corresponding source and drain.

off the relay. Depending on the number of terminals of a MEM relay, relay can be defined as 3-terminal (3-T) or 4-terminal (4-T) as summarized in Figure 2.1. Note that MEM relays mimic the field-effect transistors (FETs) in that they also have the gate, body, and source/drain electrodes. The conductive contact dimple defines physical contacting regions. The anchor that stands on the substrate is the fixed base of the

cantilever beam.

The 3-T relay comprises three terminals: a movable source, a gate, and a drain (Figures 2.1(a), (b), and (c)). The dimple restricts the motion of the movable source when it contacts the fixed drain underneath. The electrostatic actuation force (F_e) that turns on or off the relay is controlled by the voltage difference between gate and source (V_{gs}), and the on-state current (I_{on}) that equals to I_{ds} is determined by the voltage between source and drain (V_{ds}). Nevertheless, the main disadvantage of 3-T relay occurs when several 3-T relays are used in a series circuit, in which the source of the first relay is connected to GND, and the drain goes to the source of the second relay. In this case, only the first relay can be operated reliably once certain gate voltage is applied to it since the electrostatic actuation is induced by V_{gs} and the source voltage (V_s) of the first relay equals 0 V. However, the source of the second relay is connected to the drain of the first relay. As a result, the V_{gs} of the second relay is not a stable input which leads to unreliable circuit operation.

An additional terminal (body electrode) can be added to the 4-T relay (Figures 2.1(d), (e), and (f)) to address the aforementioned issues of the 3-T relay. The 4-T relay comprises four terminals: a movable gate, a gate, a source, and a drain. The channel and the gate insulator are attached under the gate electrode, and they move together with the gate electrode during electrostatic actuation. The dimples restrict the motion of the movable gate when they contact the corresponding source and drain. F_e is now induced by the voltage applied between gate and body (V_{gb}) instead of V_{gs}. Once the relay is actuated, the

movable gate structure will bring the two dimples with channel and gate insulator into contact with the corresponding source and drain electrodes underneath. The channel behaves like a bridge connecting the source and drain when the relay turns on (dimples meet the corresponding source and drain electrodes). The function of the gate insulator is to block the conductive channel from the gate electrode. Therefore, current only flows within the channel, between source to drain electrodes, not to the gate electrode once the relay is in the on-state. In a word, vertically, the turn-on voltage is reliably controlled by V_{gb} independently regardless of the applied source or drain voltage, horizontally, the I_{ds} is determined by V_{ds}. Apart from that, the 4-T relay allows operation with reduced gate-voltage swing by applying a body bias [53], which will be discussed in-depth in Chapter 4 of the relay characterizations.

Figure 2.2 shows the spring model of a 4-T MEM relay to illustrate the operation principle. As for the 4-T MEM relay design, a movable gate electrode forms a parallel plate capacitor with a fixed gate electrode underneath. When the relay is in the off-state, there is an air gap between the dimples and source/drain electrodes underneath, which prevents the current flow I_{ds}. Once a voltage is applied to the capacitor, *i.e.* $V_{gb} > V_{pi}$ (pull-in voltage of the MEM relay), the F_e introduced between the gate and body electrodes moves the suspended movable gate stack downward. The movable gate brings the channel into contact with the source and drain to conduct current. F_e is given as a function of the displacement (x) of the movable structure [60]:

$$F_e(x) = \frac{\varepsilon_o W_a L_a V^2}{2(g_o - x)^2} \tag{2-1}$$

where ε_o is the permittivity of free space, g_o is the actuation gap, and W_a and L_a are the width and the length of the actuation area, respectively.

The spring restoring force (F_{sp}) begins to increase once the movable gate is actuated downward. F_{sp} is the balancing force of F_e and it is proportional to x of the movable beam [60]:

$$F_{sp}(x) = k_{eff}\, x \tag{2-2}$$

where k_{eff} is the effective spring constant.

At equilibrium state, F_e is equal to F_{sp} [60]:

$$\frac{\varepsilon_o W_a L_a V^2}{2(g_o - x)^2} = k_{eff}\, x \tag{2-3}$$

Note that F_e increases parabolically with x while F_{sp} increases linearly with x. The fact that F_e is bigger than F_{sp} keeps moving the suspended beam downward. As the beam continues to travel, there exist a critical point beyond which F_e is always greater than F_{sp}, and the beam is snapped down abruptly. This phenomenon is referred to as the "pull-in" effect [39, 60]. By analyzing Equation (2-3), one can solve that $x = \frac{1}{3} g_o$ is the critical point where the movable beam has travelled by $\frac{1}{3} g_o$. The voltage at this critical point,

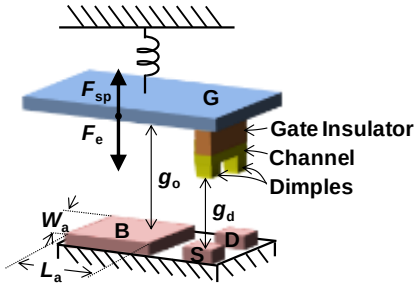

Figure 2.2 Spring model of the electrostatically actuated 4-T MEM relay. The air gap thickness between gate and body is called the actuation gap (g_o). The air gap thickness between the dimples and corresponding source and drain is referred to as the dimple gap thickness (g_d). The width and length of the body electrode are W_a and L_a, respectively. When V_{gb} is applied, the electrostatic actuation force (F_e) induced by the body and gate electrodes moves the suspended gate electrode together with the channel and gate insulator downward. The balancing force is the spring restoring force (F_{sp}) of the movable gate. If $F_e > F_{sp}$, the movable gate brings the channel into contact with the source and drain to conduct current, which leads to abrupt on-state transition. The channel beneath the gate insulator has two protruding regions, referred to as dimples. The dimples restrict the motion of the movable gate when they contact the corresponding source and drain.

which triggers the on-state of the relay, is referred to as V_{pi} [39, 60]:

$$V_{pi} = \sqrt{\frac{8k_{eff}\, g_o^{\,3}}{27\varepsilon_o W_a L_a}} \tag{2-4}$$

As shown in Figure 2.2, the relay employs dimples to make physical contact with the source and drain electrodes. As discussed above, the "pull-in" effect exists when $x = \frac{1}{3}g_o$. If $g_d \geq \frac{1}{3}g_o$, the relay operates in pull-in mode. If $g_d < \frac{1}{3}g_o$, the relay operates in non-

pull-in mode [39, 60]. One can choose the operation mode of the MEM relay by adjusting the ratio of g_o and g_d, respectively.

The V_{pi} of a relay operating in pull-in mode can be expressed as [39, 60]:

$$V_{pi} = \sqrt{\frac{8k_{eff}\, g_o^{\,3}}{27\varepsilon_o A_o}} \quad \text{where } g_d \geq \tfrac{1}{3} g_o \tag{2-5}$$

where k_{eff} is the effective spring constant of the movable structure, A_o is the overlap area between the movable structure and the fixed electrode, which is the effective actuation area. Note that the effective actuation area equals to the size of body electrode ($W_a \times L_a$) as shown in Figure 2.2.

For a relay operating in non-pull-in mode, the on-state occurs when $x = g_d$, and the non-pull-in voltage (V_{npi}) can be given by [39, 60]:

$$V_{npi} = \sqrt{\frac{2k_{eff}\,(g_o - g_d)^3}{\varepsilon_o A_o}} \quad \text{where } g_d < \tfrac{1}{3} g_o, \tag{2-6}$$

When the contact is made, the force balance equation is given by [39, 60]:

$$F_e + F_a = F_{sp} \tag{2-7}$$

where F_a is the surface adhesion force when two contact surfaces meet [39, 61].

Substituting Equations (2-1) and (2-2) into (2-7), the force balance equation becomes [39, 60]:

$$\frac{\varepsilon_o A_o V^2}{2(g_o - x)^2} + F_a = k_{eff}\, x \tag{2-8}$$

To turn off the relay, F_{sp} needs to be large enough to overcome F_e and surface adhesion force $F_{a.}$ A smaller voltage than V_{pi} (or V_{npi}) needs to be applied. By replacing $x = g_d$ into Equations (2-8), the release voltage (V_{rl}) is solved as [39, 60]:

$$V_{rl} = \sqrt{\frac{2(k_{eff}\, g_d - F_a)(g_o - g_d)^2}{\varepsilon_o A_o}} \tag{2-9}$$

Note that V_{rl} sets the lower limit for the relay supply voltage scaling [39].

2.2. Prototype Organic Relay

Figure 2.3 presents an isometric schematic, the circuit symbol, cross-section view, scanning electron micrographs (SEM), and the design parameters and values of the prototype fully-polymeric MEM relay. This MEM relay comprises six terminals: a movable gate stack, a body, and two pairs of source/drain on both sides. The operation of the organic MEM relay is similar to that of 4-T relay as introduced in Section 2.1, in which the current flow between the source and drain (I_{ds}) on either side is controlled by V_{gb}. The relay comprises a fully polymer-based movable structure suspended by serpentine springs above source, drain, and body electrodes. Along with vias, the conductive polymer, Poly(3,4-Ethylenedioxythiophene):Polystyrene-Sulfonate (PEDOT:PSS) (attached above an insulating polymer that serves as the gate dielectric) connects the gate electrodes to the movable structure. Note that the etch holes (4 μm^2) are

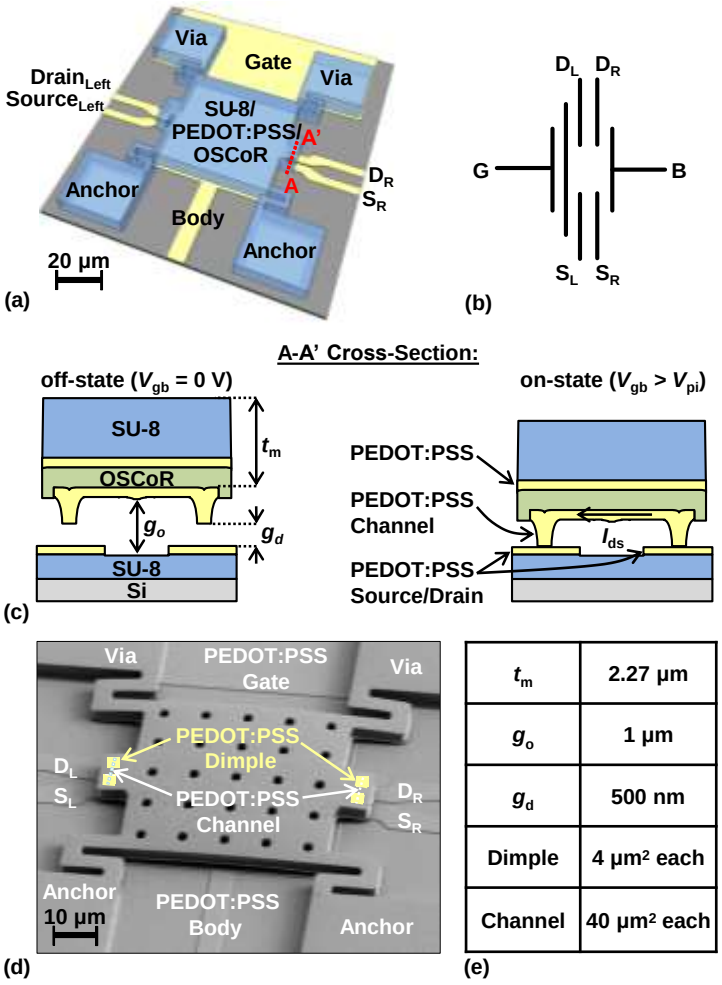

Figure 2.3 (a) Schematic view of the prototype organic MEM relay. The movable stack comprises different dielectric (SU-8 and OSCoR) and conductive (PEDOT:PSS) polymer materials, the stack is electrically connected to the gate electrode through the vias. (b) Circuit symbol of the relay. (c) A-A' cross-section view of the relay. Off-state: an air gap prevents current to flow between the source and drain on either side. On-state: electrostatic actuation force between the gate and body brings both channels into contact with the pairs of source and drain. (d) SEM of the relay. (e) Design parameters. Note that 4 µm^2 etch holes are patterned onto the gate stack in order to ensure release of the relay by vapor HF and to reduce residual stress of the gate stack [62].

patterned on the gate stack in order to ensure release of the relay by vapor-phase hydrogen fluoride (HF) and to reduce residual stress of the gate stack [62]. In order to provide sufficient charge for the actuation of the structure, V_{gb} is applied to induce F_e on the movable structure and actuates the gate stack downward toward the body (shown in Figure 2.3). As V_{gb} across the actuation gap (g_o) increases, F_e between the gate and body increases parabolically, while the spring restoring force (F_{sp}) of the folded-flexures increases linearly. When the magnitude of F_e exceeds that of F_{sp}, the movable gate snaps down abruptly, and the conductive polymer channel (underneath a polymer gate dielectric) is brought into contact with the pair of source and drain on either side to conduct current. Because the prototype relay is designed to operate in pull-in mode, V_{pi} at which the movable stack pulls can be expressed as Equation (2-5). When V_{gb} is lowered below V_{rl} (Equation (2-9)), F_{sp} becomes large enough to overcome F_e and $F_{a.}$ Thus, the contacts of the dimples to source and drain electrodes on both sides are broken, and the relay turns off. Note that the fringing capacitance, actuation area reduction due to the release holes and the bending of the actuation plate are assumed to be negligible.

Based on the design as shown in Figure 2.3, several key design parameters are summarized as follow: (1) The relay is designed to work in pull-in mode with g_o = 1 μm, g_d = 500 nm, and g_d/g_o = 0.5 because pull-in operation is found to be preferred for optimal energy efficiency [59]. V_{pi} of the relay is therefore determined by g_o according to Equation (2-5); (2) The relay has a clamped-clamped structure with four bases (anchors) on both side of the movable beam. As mentioned in section 2.1, unlike the cantilever design that suffers from insufficient spring restoring force, the buckled clamped-clamed

beam should produce reliable restoring force to turn off the relay once the electrostatic actuation is revoked; (3) There are four symmetric folded-flexures as serpentine springs to suspend the movable beam while there are only two strain springs to suspend the beam in the conventional clamped-clamped structure. The main benefit of adding extra springs to the overhanging beam is for minimizing the possibility of rotating the beam torsionally during electrostatic actuation; (4) k_{eff} of the relay depends on the design parameters of the folded-flexures attached to the movable beam [59]; (5) The A_o between the suspended gate electrode and the fixed body electrode is defined by the size of gate electrode. By changing the dimensions of the gate electrode, the A_o can be changed, which in turn affects F_e; (6) Gate leakage current to the body could happen if the bottom of the gate stack is not protected by gate dielectric. Once high gate voltage is applied, the relay is catastrophically pulled in (*i.e.*, the whole gate stack collapses onto the substrate). As a result, huge current could flow from the gate to body, which leads to device failure [39, 60]. To address this issue, the entire bottom of the gate stack of the prototype organic MEM relay is covered with thick (~200 nm) organic gate dielectric to prevent any possible short circuit; (7) The gate dielectric can be patterned together with the whole gate stack and it is a self-aligned process; (8) Two dimples along with a channel underneath both sides of the suspended plate have two main functions. Firstly, one pair of dimples and the channel provide the electrical path once dimples meet with the source and drain electrodes on both sides. Secondly, the dimples reduce the possibility of "catastrophic" pull-in, this "foot" issue is especially common on relay without dimple [39, 60].

2.2.1. Electrode Engineering

Overall, the organic relay structure consists of three parts: bottom electrodes, a movable gate stack, and an air gap between the bottom electrodes and the stack. Figure 2.4(a) shows the layout of the prototype organic MEM relay, it has one gate, one body, and two pair of source and drain electrodes. The total footprint is 412 × 400 μm^2 for the prototype relay. Conservatively, large electrode pads area of 100 × 100 μm^2 and large minimal space of 38 μm between adjacent pads are used in the layout. These areas consume relatively large footprint but provide enough space to locate probe tips during device characterizations. In fact, the large pads (100 × 100 μm^2 each) make up 40 % of the total device area in the prototype relay design.

Figure 2.4(b) shows the zoom-in view of the channel and dimple region. The width of the wire routing is decreased from 6 μm to 5 μm. The minimal distance of 2 μm between source and drain electrodes is set in order to prevent undesirable surface leakage, which is conservative larger than the minimum feature size (1 μm) of the photolithography tools (Karl Suss MA6 Mask Aligner and Karl Suss MJB3 Mask Aligner) used for this work.

The relay is anchored to the electrode layer by four vias and two of the vias form electrical connection from the gate electrode to the conductive PEDOT:PSS layer in the gate stack as shown in Figure 2.4(c). The size of anchor is 40 × 40 μm^2. The size of via is 38 × 38 μm^2. Because the conductive organic material PEDOT:PSS has a finite conductivity, relatively large-area vias are used to lower the resistance of each via.

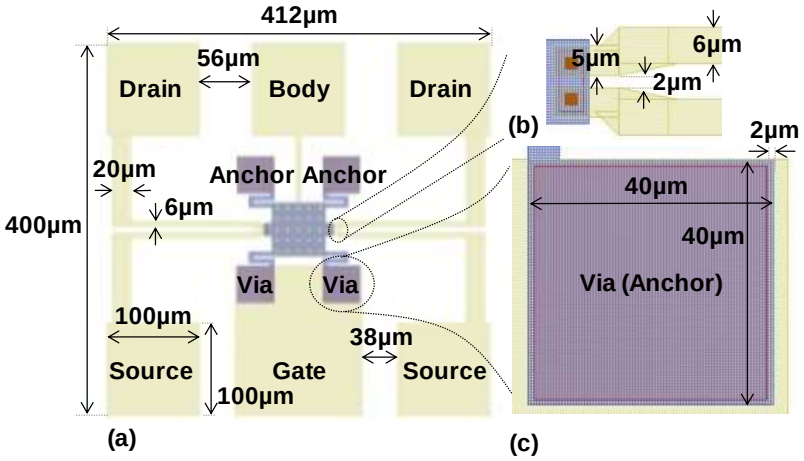

Figure 2.4 (a) Layout of the prototype relay. The minimum size of electrode pad is 100 × 100 μm^2, that is conservative large to place probe tip for relay electrical characterizations. The minimum space between electrode pads is 38 μm, that is set in order to conservatively place separate probe tips on two adjacent electrode pads. The relay is anchored by four anchors on PEDOT:PSS substrate. Two vias enable connection from the conductive layer (PEDOT:PSS) in the gate stack to the gate electrode. (b) Zoomed-in view showing channel and dimple region, the spacing between the source and drain electrodes is set to 2 μm to prevent surface leakage. (c) Zoomed-in view showing relay is anchored on PEDOT:PSS substrate. The size of the anchor is 40 × 40 μm^2, that is conservative large to provide enough reliability. The size of via is 38 × 38 μm^2. The gate electrode is connected to the conductive layer in the gate stack through two vias.

Note that V_{pi} can be reduced effectively by adjusting the body bias in order to allow for operation with a lower gate-voltage swing [53, 63]. Ideally, a change in the V_b results in commensurate change to the gate switching voltages V_{pi} and V_{rl}. *i.e.*, a 1 V voltage change in V_b should result in a 1 V change in V_{pi}. To validate the prototype organic relay design, Finite-Element-Analysis (FEA) was performed using simulation software (CoventorWare). Figure 2.5(a) shows the simulated V_{pi} of the organic relay that operates

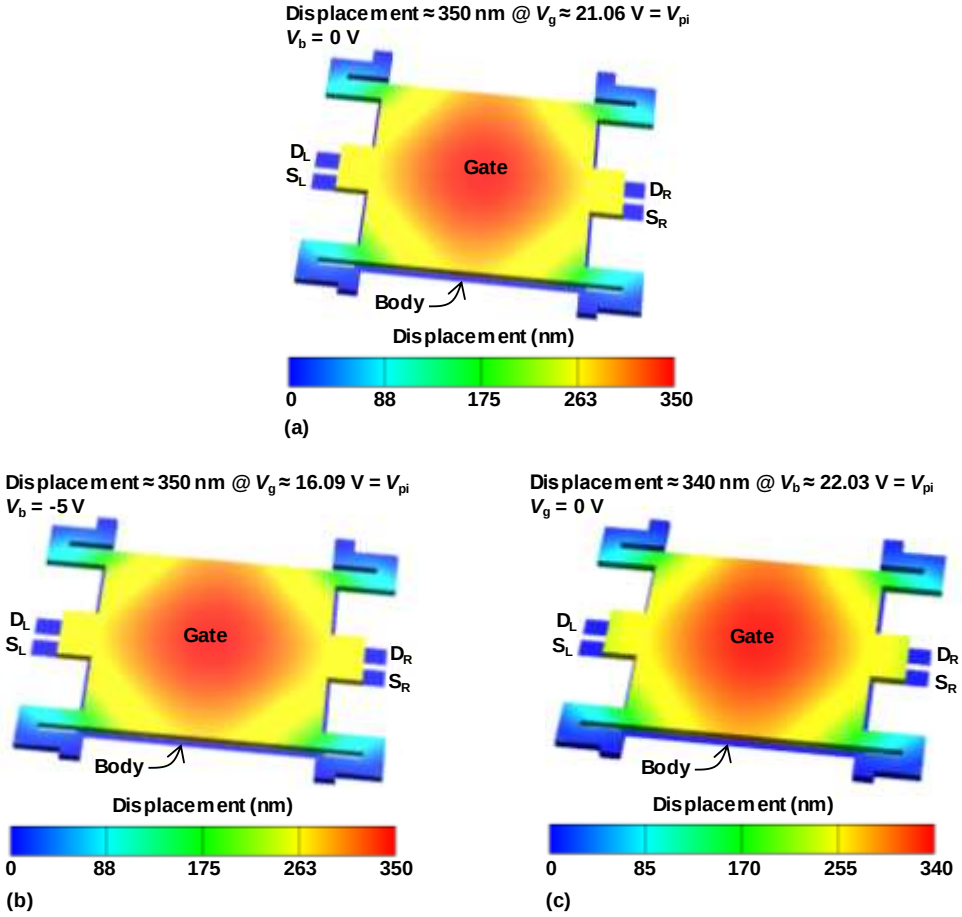

Figure 2.5 The relay used in the FEA simulation has W = 3 μm, L = 7 μm, W_a = L_a = 57 μm, g_o = 1 μm, g_d = 500 nm and t_m = 2.27 μm. V_d and V_s were set to 0 V in the simulation. (a) When V_b = 0 V, the relay is actuated downward by ~350 nm (≈ 1/3g_o) at V_g ≈ 21.06 V = V_{pi}, then it turns on abruptly. (b) When body bias V_b = -5 V, the relay turns on at V_g ≈ 16.21 V = V_{pi}. (c) The relay turns on at V_b ≈ 22.03 V = V_{pi} and V_g = 0 V. The number of volume element mesh created of the simulation was 25162 and displacement tolerance was set to be 0.001 μm.

in pull-in mode (g_o = 1 μm, g_d = 500 nm, and g_d/g_o = 0.5) without body bias. When V_g = 21.06 V is applied, F_e brings the movable beam downward. The maximum displacement of the suspension beam reaches 350 nm (≈ 1/3g_o) before the relay turns on abruptly. This

result confirms that once the movable beam passes the critical point ($g_o/3$), the movable beam suddenly snaps down, and relay turns on. Figure 2.4(b) presents that the simulated V_{pi} is 16.61V with V_b = -5 V. Compared with the V_{pi} without body bias in Figure 2.4(a), this result verifies the effective adjustment of V_{pi} for the relay with body bias, *i.e.* a commensurate change to V_{pi} with a change in body bias.

Due to the nature of the electrostatic actuation force, it is always an attractive force between the movable gate electrode and fixed body electrode regardless of the polarity of the applied V_{gb}. As demonstrated in Figure 2.3(c), the simulated V_{pi} value of the relay that is actuated by the body-to-gate voltage is 22.03 V, which is consistent with the V_{pi} of the relay that is actuated by the gate-to-body voltage.

2.2.2. Air Gap Engineering

The air gap of the relay is important because: (1) The air gap physically separates the movable gate from the underneath body electrode and the channel from the underlying source and drain electrodes in the off-state; (2) The strength of the induced electrostatic force between the gate and body electrodes is affected by the thickness of the air gap, *i.e.* $F_e \propto 1/g_o^2$ [39]; (3) The ratio of g_o and g_d defines the operation mode of the relay.

Figure 2.6 shows the change of F_e and F_{sp} during the mechanical motion of the movable gate and the cross-section view of the prototype relay to illustrate the transition from the off-state to the on-state. The vertical dimension of the prototype relay is designed as g_o = 1 μm, g_d = 500 nm, and g_d/g_o = 0.5 > 1/3. From the prospect of most energy-efficient operation, the dimple gap should be one-half of the actuation gap [39]. F_{sp} is provided by

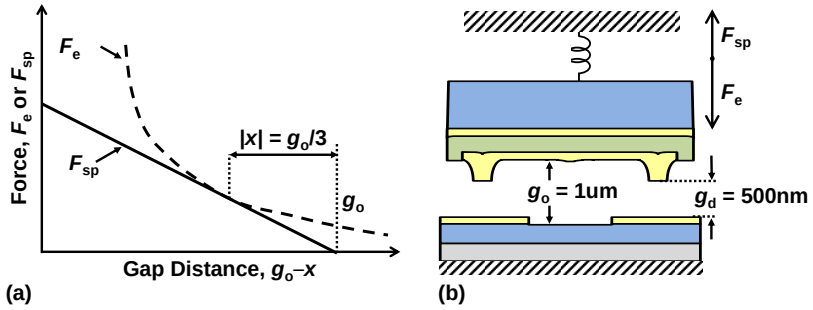

Figure 2.6 (a) Change of F_e, F_{sp} *vs.* gap distance of the prototype relay. (b) The cross-section view of the prototype relay. The ratio of g_d and g_o is 0.5, that is greater than 1/3. The relay operates in pull-in mode. The movable gate snaps down abruptly after it travels to $x = g_o/3$, F_e is always greater than F_{sp} after the movable gate moves beyond $g_o/3$.

the folded-flexures of the relay which behave like a serpentine spring. F_e is induced by V_{gb}. Initially, $x = 0$, neither F_{sp} nor F_e exists. Once V_{gb} is applied to the relay, F_e is induced. According to Equation (2-1), F_e increases parabolically with x as indicated by the dash-line in Figure 2.6(a). Because the movable stack moves downward, F_{sp} starts to exist and it increases linearly with x according to Equation (2-2). F_{sp} is shown as the solid line in Figure 2.6(a). As long as V_{pi} is applied that enables $F_e > F_{sp}$, the gate stack continues to move downward till the critical point $x = g_o/3$, where $F_e = F_{sp}$. Because $g_d > g_o/3$, the dimples do not contact the source and drain electrodes underneath at this moment, relay keeps moving downward. However, once the relay passes the critical point ($g_o/3$), $F_e >> F_{sp}$, the movable stack suddenly snaps down, the dimples meet with the source and drain electrodes underneath, and therefore the relay turns on.

2.2.3. Gate Stack Engineering

The details of the gate structure design are shown in Figure 2.7. One of the advantages of the 4-T relay design is that the flexure structures and the actuation area are decoupled, *i.e.*, the k_{eff} is only determined by the folded-flexures dimensions (the movable beam is considered as a rigid plate) and the actuation area is defined by the area of the suspended gate stack. As indicated in Equation (2-5) and (2-9), both V_{pi} and V_{rl} are proportional to $\sqrt{k_{\text{eff}}}$. k_{eff} is determined by the dimensions of the folded-flexures, the intuitive expression of k_{eff} is given by [39, 60]:

$$\frac{1}{k_{\text{eff}}} \cong \left(\gamma_{\text{f}} \frac{E_{eq} W t_m^{\,3}}{L^3} \right)^{-1} + \left(\gamma_{\text{t}} \frac{G_{eq} W t_m^{\,3}}{L} \right)^{-1} \tag{2-10}$$

where t_{m} is the thickness of the movable gate stack, W and L are the width and length of the folded-flexure springs, respectively. γ_{f} and γ_{t} are the flexural inertia and torsional inertia, respectively. γ_{f} and γ_{t} were extracted to be 3.36 and 1.59×10^{10} by using nonlinear fitting method to fit the FEA simulated results. A total of 36 simulated V_{pi} values for relays with various W and L (as shown in Table 2.1) were used in the nonlinear fitting. $E_{\text{SU-8}}$ and $G_{\text{SU-8}}$ (Table 2.1) are the Young's modulus and shear modulus of SU-8. Note that the gate stack comprises 200 nm gate insulator (OSCoR), 70 nm gate conductor (PEDOT:PSS) and 2 μm (SU-8) as shown in Figure 2.3(c). The thickness of SU-8 layer dominates that of the gate stack. To simplify the calculation, the Young's modulus and shear modulus of SU-8 polymer are referred to as the equivalent values hereby, that $E_{\text{eq}} = \sum(E_{\text{i}} \cdot t_{\text{i}})/\sum t_{\text{i}} \approx E_{\text{SU-8}}$ and $G_{\text{eq}} = \sum(G_{\text{i}} \cdot t_{\text{i}})/\sum t_{\text{i}} \approx G_{\text{SU-8}}$ [60].

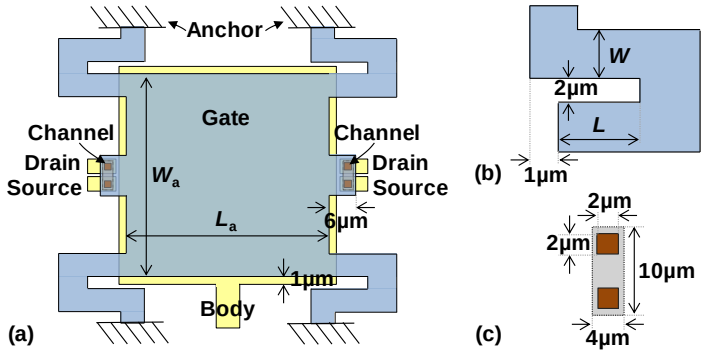

Figure 2.7 (a) Top-down view of the prototype relay layout. Note that release etch holes on gate stack are not shown. The minimum feature size of the photolithography tools (Karl Suss MA6 Mask Aligner and Karl Suss MJB3 Mask Aligner) used for this work is 1 μm and the maximum photolithographic alignment tolerance is conservatively set to 1 μm. The spacing between the source and drain electrodes is set to 2 μm, the spacing between body and either drain or source is set to 2 μm to prevent surface leakage. The gate stack to body cut-out is set to 1 μm to allow for sufficient photolithographic alignment tolerance, the overlap actuation area is determined by the gate stack area ($W_a \times L_a$). The channel is enclosed by the gate stack by 1 μm. The channel to drain/source overlap is minimized to prevent unwanted electrostatic actuation force between the channel and drain/source. (b) Dimensions of the folded-flexures that supports the gate stack. The effective spring constant of the flexure-beams can be estimated from Equation (2-10). (c) Dimensions of the channel. Each contact is enclosed by the channel with boundary of 1 μm. The contact dimple dimensions are limited to 2×2 μm^2 to prevent the in-used stiction and F_a [39].

Various W, L and gate actuation area ($W_a \times L_a$) values (Table 2.1) are designed in the layout to investigate their impacts on the prototype MEM Relay.

Firstly, gate actuation area ($W_a \times L_a$) is fixed to investigate the effects of W and L of the folded-flexures. Figure 2.8(a) shows the FEA simulated V_{pi} values of the prototype organic MEM relay with various W and L values using simulation software (CoventorWare). Gate actuation area were restricted as $W_a = L_a = 57$ μm. For the

Table 2.1 Design parameters and values of the prototype relay.

Parameter	Value
Young's Modulus (E_{SU-8})	2 GPa [64]
Shear Modulus (G_{SU-8})	1.2 GPa [65]
Actuation Plate Width and Length ($W_a = L_a$)	(37, 57, 77, 97) μm
Folded-Flexure Length (L)	(5, 7, 10, 12, 15, 17, 20, 25, 30) μm
Folded-Flexure Width (W)	(3, 5, 7, 9) μm
Movable Gate Stack Thickness (t_m)	2.27 μm
Designed Actuation Gap Thickness (g_o)	1 μm
Designed Dimple Gap Thickness ($g_d = 0.5g_o$)	500 nm
Dimple Area (A_d)	2×2 μm^2 each
Channel Area (A_c)	4×10 μm^2 each

prototype design, the target V_{pi} value is below 30 V. Therefore, from the FEA simulated V_{pi}, we can expect the required W and L of the folded-flexures. To ensure that the relay can be turned off, *i.e.* $V_{rl} > 0$ V, F_{sp} must be sufficient to overcome F_a:

$$F_{sp}(x) = k_{eff}\, x > F_a \tag{2-11}$$

F_a is mainly caused by van der Waals interactions between two contacting surfaces [39, 61]. The 4-T relay with tungsten (W) contacting electrodes is reported to have the F_a ~ 0.45 μN with the dimple area of 2 × 10 μm^2 [39, 66]. While there is no reported F_a value of PEDOT:PSS contacting electrodes, we conservatively assume the arbitrary F_a to be ~ 1 μN for our organic relay with 4 × 4 μm^2 PEDOT:PSS contact electrodes. In order to estimate a proper k_{eff} for the relay to turn off, F_a = 1 μN was assumed. $x = g_d$ = 500 nm and F_a = 1 μN were substituted in Equation (2-11). $k_{eff} > 10$ N/m was therefore estimated. From the simulated k_{eff} plotted in Fig 2.8(b), one can estimate the necessary W and L

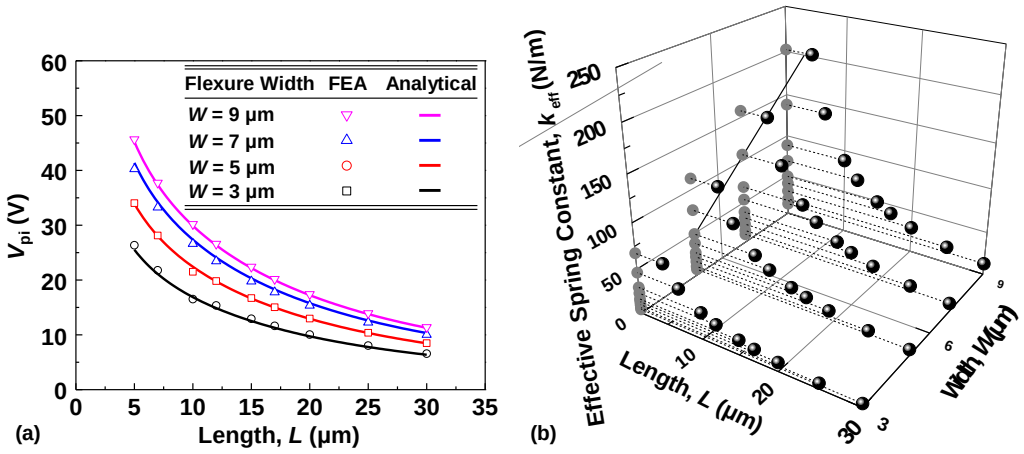

Figure 2.8 (a) FEA simulated and theoretical calculated V_{pi} *vs. L* of the prototype relays. The analytical model is within 90% of FEA simulation. The relays have various *W* and *L* values with t_m = 2.27 μm, g_o = 1 μm, g_d = 500 nm, W_a = L_a = 57 μm. V_b, V_d, and V_s were set to 0 V in the simulation. (b) Simulated k_{eff} of the prototype relay with various *W* and *L* values. When *W* is fixed, k_{eff} decreases with the increasing *L*. When *L* is fixed, k_{eff} increases with the increasing *W*.

combinations of the folded-flexures to produce a k_{eff} greater than 10 N/m. Note that among all the designed *W* and *L* values as shown in Table 2.1, only a few *W* and *L* combinations (*W*, *L*) including (3 μm, 25 μm), (3 μm, 30 μm), (5 μm, 30 μm), and (7 μm, 30 μm) are outliers.

When designing the *W* and *L* of the folded-flexures, there are several conservative designs with wider *W* and shorter *L* to assure a sufficient k_{eff} of the movable structure. Note that these conservative designs unnecessarily lead to large V_{pi} value of the relay because the area of the actuation plate can also be increased to reduce V_{pi}.

The actuation area (A_o) is another important factor in the gate stack design since the A_o affects the magnitude of V_{pi} according to Equation (2-5). As indicated in Figure 2.7(a),

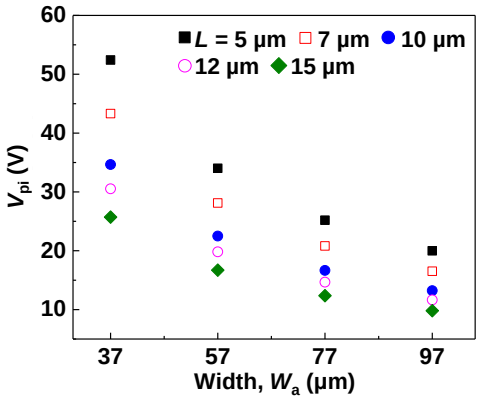

Figure 2.9 FEA simulated V_{pi} *vs.* W_a of the prototype relays. The relays have t_m = 2.27 μm, g_o = 1 μm, g_d = 500 nm, W = 5 μm, and $L \leq 15$ μm. V_b, V_d, and V_s were set to 0 V in the simulation. As W_a increases ($W_a = L_a$), the actuation area ($W_a \times L_a$) increases, therefore V_{pi} decreases according to Equation (2-5).

the A_o of the prototype organic MEM relay equals the area of the gate stack area ($W_a \times L_a$). Figure 2.9 shows the FEA simulated V_{pi} values of the prototype organic MEM relay with different W_a. As ($W_a \times L_a$) increases with W_a ($W_a = L_a$), the simulated V_{pi} decreases. Note that the simulations were based on prototype relays with parameters W = 5 μm and $L \leq 15$ μm (Table 2.1) as the restricted factors to ensure relatively large k_{eff}. These conservative folded-flexure parameters could lead to $k_{eff} > 15$ N/m as shown in Figure 2.8(b). As a result, these conservative folded-flexure parameters should assure sufficient stiffness for the relays to turn off.

2.3. Multiple-Input/-Output Relays

2.3.1. Single-Gate Dual-Body Relay

Figure 2.10 presents an isometric schematic, cross-sectional views, layout and scanning electron micrographs (SEMs) of the single-gate dual-body organic MEM relay. The

design parameters and values are given in Table 2.2. The single-gate dual-body relay comprises a fully polymer-based movable structure suspended by serpentine springs above two body electrodes and two pairs of source/drain on both sides. Along with vias, the conductive polymer (attached above an insulating polymer that serves as the gate dielectric) connects the gate electrode to the movable gate stack. Note that in the single-gate dual-body relay, the fixed body electrode is divided into two bodies with the same body length ($2L_b$).

The key improvements in the single-gate dual-body relay design over the prototype relay are summarized as follow: (1) The ratio of $g_d/g_o = 1/3.5 < 1/3$ is set in order to enable the single-gate dual-body relay operate in non-pull-in mode. The turn-on voltage of the relay operates in non-pull-in voltage is referred to as non-pull-in voltage (V_{npi}); (2) Vertically, both g_o and g_d are scaled down in order to reduce V_{npi} of the relay for lower V_{dd} application; (3) Horizontally, body is divided into two body electrodes in order to present the versatility of the relay; (4) The overlap area between the conductive polymer in the movable structure to the source/drain on both sides of the relay is removed; (5) The size of a contact dimple is reduced to $1.5 \times 1.5\ \mu m^2$.

The single-gate dual-body relay is now designed to operate in non-pull-in mode. In order to understand the transition from the off-state to the on-state of this refined relay, the change of F_e, F_{sp} during the mechanical motion and the cross-section view of the movable structure are shown in Figure 2.11. To provide charge for the actuation of the structure, V_{gb} is applied to induce F_e on the movable gate structure and it actuates the gate

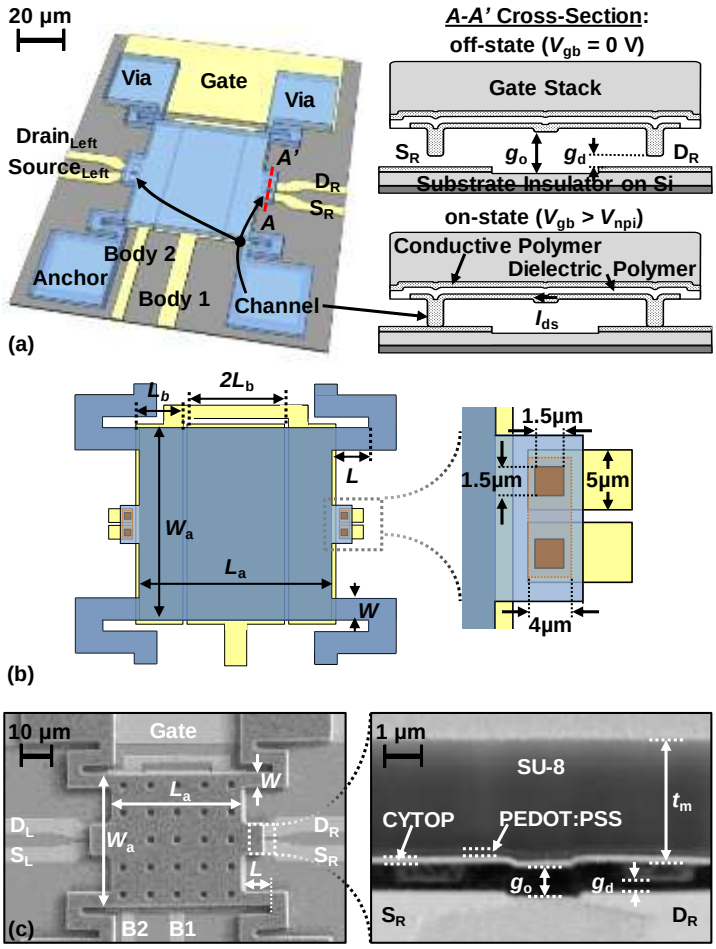

Figure 2.10 (a) Isometric schematic and cross-sectional views of the single-gate dual-body relay. (b) The layout view of the relay. (c) SEMs of the relay.

Table 2.2 Design parameters and values of the single-gate dual-body relay.

Parameter	Value
W	3, 5, 7 μm
L	10, 12, 15, 17 μm
$W_a = L_a = 4L_b+3$	47, 52, 57 μm
$t_m = t_{SU\text{-}8} + t_{PEDOT:PSS} + t_{CYTOP}$	2.46 μm = 2.3 μm + 70 nm + 90 nm
$g_o = 3.5g_d$	0.7 μm
$E_{CYTOP} = 0.7E_{SU\text{-}8} = 0.7E_{PEDOT:PSS}$	1.4 GPa [67, 68]
Channel	10 × 4 μm^2 each
Dimple	1.5 × 1.5 μm^2 each

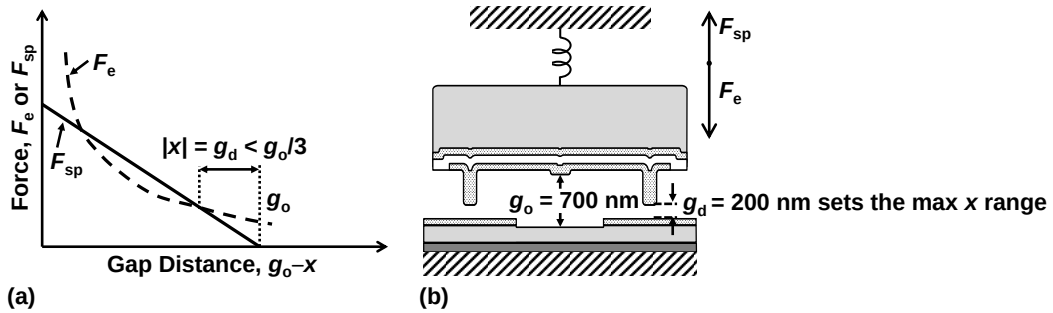

Figure 2.11 (a) Change of F_e, F_{sp} *vs.* gap distance of the single-gate dual-body relay. (b) The cross-section view of the single-gate dual-body relay. The ratio of g_d and g_o is 1/3.5, that is smaller than 1/3. The relay operates in non-pull-in mode, in which g_d determines the maximum displacement the relay. The relay turns on when the movable gate travel till $x = g_d$, F_e becomes equal to F_{sp}.

stack downward toward the body electrodes. F_e (represented by dash line in Figure 2.11(a)) increases parabolically with x according to Equation (2-1) and F_{sp} (represented by solid line in Figure 2.11(a)) increases linearly with x according to Equation (2-2). As long as the magnitude of F_e is greater than that of F_{sp}, the movable structure continues to be actuated downward. Recall from the pull-in mode operation in the prototype relay, the movable structure will pass the critical point ($g_o/3$), then suddenly snaps down. However, in non-pull-in mode operation, g_d defines the maximum displacement of the movable structure because the dimples restrict the motion of the movable gate stack when they contact the corresponding source and drain electrodes. This maximum displacement is the point of intersection of the solid line and dash line in Figure 2.11(a). V_{npi} of the single-gate dual-body relay is given by Equation (2-6) The V_{rl} of the single-gate dual-body relay is expressed by Equation (2-9).

Figure 2.12(a) shows the analytical calculated V_{npi} and V_{rl} of the refined single-gate dual-body relay that operates in non-pull-in mode and Figure 2.12(b) shows the analytical calculated V_{pi} and V_{rl} of a relay that operates in pull-in mode. As L increases, the k_{eff} decreases according to Equation (2-10). As a result, both V_{npi} and V_{pi} of the relays decline as indicated in Figures 2.12(a) and (b). In Figure 2.12(a), one can see that the difference between the calculated V_{npi} and calculated V_{rl} is relatively small. On the contrary, the relay that operates in pull-in mode as shown in Figure 2.12(b) has large difference between the calculated V_{npi} and calculated V_{rl}. The difference between V_{npi} (or V_{pi}) and V_{rl} is referred to as hystersis voltage.

There are two main causes of the hysteresis voltage. One reason is non-zero F_a, which depends on various factors such as the the contact materials, area and surface properties [39, 61]. The second cause is the relay operation mode. As indicated in Figure 2.6, if the relay is designed in pull-in operation mode, the magnitude of F_e exceeds that of F_{sp} once the device turns on after passing the critical point ($g_o/3$). Therefore, V_{gb} must be lowered further in order to turn off the device even without the presence of F_a. However, in the case that the relay operates in non-pull-in mode as presented in Figure 2.12, F_e is equal to F_{sp} at the moment the device turns on. As a result, V_{gb} only needs to be lowered just a little bit to trigger the relay to turn off assuming the value of F_a is zero. The single-gate dual-body relay is designed to operate in non-pull-in mode in order to minimize the hysteric switching behavior.

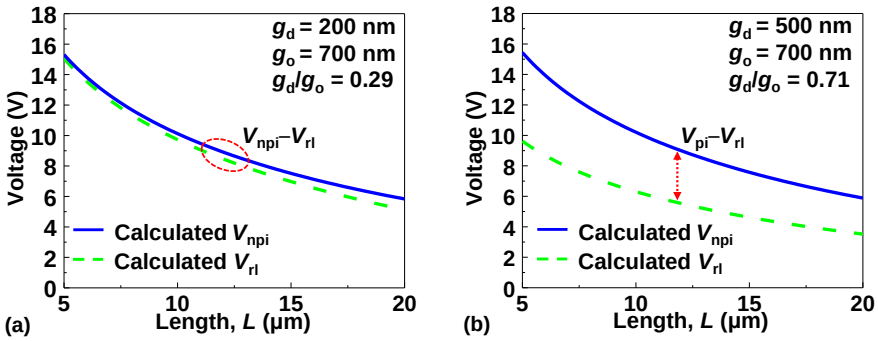

Figure 2.12 (a) The theoretically calculated V_{npi} and V_{rl} of the refined single-gate dual-body relay that operates in non-pull-in mode with g_o = 700 nm, g_d = 200 nm, g_d/g_o = 0.29 < 1/3. (b) The theoretically calculated V_{pi} and V_{rl} of an arbitrary relay that operates in pull-in mode with g_o = 700 nm, g_d = 500 nm, g_d/g_o = 0.71 > 1/3. The other parameters of the relays are the same: $W_a = L_a$ = 57 μm, W = 3 μm, t_m = 2.46 μm. F_a = 0.45 μN was assumed [39, 66].

Table 2.3 compares the single-gate dual-body relay design with the prototype relay design in terms of overlap area and capacitance between gate and body(s). In the single-gate dual-body relay, the movable structure is referred to as gate electrode and the body is divided into two separate body electrodes that can be biased independently. Note that the strength of F_e is proportional to A_o. Since the fixed body electrode is divided into two bodies with the same body length ($2L_b$), the overlap area between gate to each body electrode ($A_b = W_a \times 2L_b$) is the same. Therefore, body 1 and body 2 electrodes have the equal influence. Table 2.3 lists the overlap area and parallel-plate capacitance of the single-gate dual-body and the prototype relay. The single-gate dual-body relay now has smaller gate to body 1 & body 2 overlap area (3078 μm^2) compared with gate to body overlap area (3249 μm^2) of the prototype. That is because the inter-digitization of body electrodes in single-gate dual-body relay has a minimal space of 1.5 μm between body 1

Table 2.3 The overlap area and parallel-plate capacitance of the single-gate dual-body and the prototype relay.

	Single-Gate Dual-Body Relay			**Prototype Relay**	
	Gate to Body1&2	Gate to Body1 = Gate to Body2	Gate to Sources/Drains	Gate to Body	Gate to Sources/Drains
Overlap Area (μm^2)	3078	1539	0	3249	80
Off-State Capacitance (fF)	37.72	18.86	0	27.4	0.67
On-State Capacitance (fF)	122.49	61.24	0	52.30	1.29

Note: The calculations are based on relays with $W_a = L_a = 57$ µm.

and body 2 electrodes in the layout, which wastes some of the overlap area. In the single-gate dual-body design, the overlap area between the gate to source/drain electrodes on both sides is removed by adding one mask to pattern the conductive layer in the movable gate stack. However, there is a small overlap area between the gate to source/drain electrodes on both sides in the prototype relay, which could result in small drain-bias effect [69]. Note that the ratios of the on-state capacitance to the off-state capacitance ratio are 3.25 and 1.89 for the single-gate dual-body relay and the prototype relay, respectively.

Fig, 2.13 presents the FEA simulation results of the relay with the relay parameters in Table 2.2. Specifically, this work is based on the relay with $W = 5$ µm, $L = 10$ µm, $W_a = L_a = 57$ µm, $L_g = 27$ µm, $g_o = 700$ nm, $g_d = 200$ nm, $t_m = 2.46$ µm. Both body 1 and body 2 were applied to actuate the relay in the simulation as shown in Figure 2.9(a). Since the relay operates in non-pull-in mode, the relay turns on when the suspension beam travels

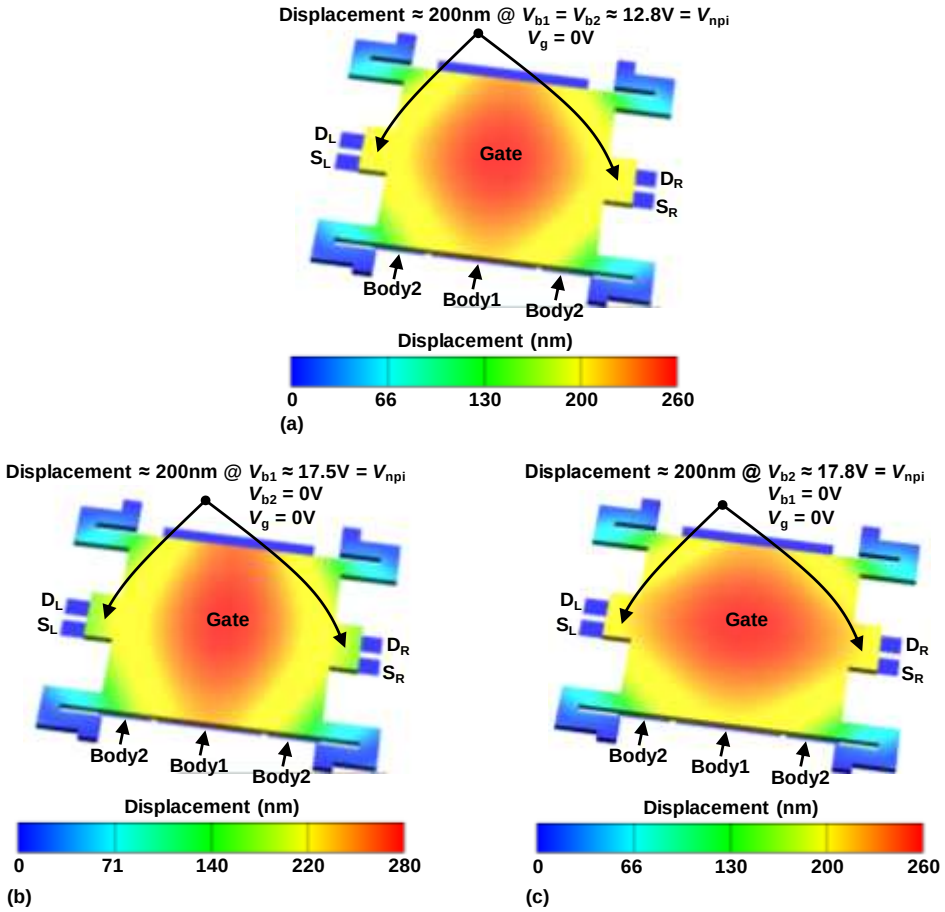

Figure 2.13 The FEA simulation result of the single-gate dual-body relay. The parameters of the relay are W = 5 μm, L = 10 μm, $W_a = L_a$ = 57 μm, L_b = 13.5 μm, g_o = 700 nm, g_d = 200 nm, t_m = 2.46 μm. (a) The relay turns on when $V_{b1} = V_{b2} \approx$ 12.8 V, V_g = 0 V. The maximum downward displacement of ~260 nm occurs at the center of the movable body with the displacement of ~200 nm along the channel regions. (b) The relay turns on at $V_{b1} \approx$ 17.5 V, $V_{b2} = V_g$ = 0 V. (c) The relay turns on at $V_{b2} \approx$ 17.8 V, $V_{b1} = V_g$ = 0 V. The number of volume element mesh created of the simulation was 28417 and displacement tolerance was set to be 0.001 μm.

the distance equal to g_d. The V_{npi} is 12.8 V in this case. Figure 2.9(b) shows only body 1 was applied to actuate the relay with $V_{b2} = V_g$ = 0 V. As indicated in Equation (2-6), $V_{npi} \propto 1/\sqrt{A_0}$, the gate to body 1 overlap area (A_b) is half of the gate to bodies overlap area

(A_o). Therefore, the V_{npi} in the case when body 1 was applied should be $\sqrt{2}$ of the V_{npi} when both body 1 and body 2 are applied to actuate the relay. The simulation verifies that the V_{npi} (17.5 V) of the case when body 1 was applied is approximately $\sqrt{2}$ of the V_{npi} (12.8 V) of the case when body 1 and body 2 were used. Figure 2.9(c) confirms that body 1 and body 2 has equal influence on the actuation of the relay and either of these two bodies can be applied independently to turn on the relay. As the V_{npi} (17.8 V) of the case when body 2 was applied is approximately the same as the V_{npi} (17.5 V) of the case when body 1 was applied.

2.3.2. Dual-Gate Dual-Body Relay

Figure 2.14 shows a three-dimensional schematic, cross-section views, and scanning electron micrographs (SEMs) of dual-gate dual-body organic MEM relay comprising two gates, two bodies, and two pairs of source/drain electrodes. Design parameters and values are summarized in Table 2.4. The dual-gate dual-body relay is also designed to operate in non-pull-in mode with g_o = 600 nm, g_d = 150 nm, and g_d/g_o = 1/4. Briefly, the relay turns on when V_{gb} is greater than V_{npi}, and it turns off when V_{gb} is lowered below V_{rl}.

The key improvement of the dual-gate dual-body relay can be seen from the B-B' cross-section view of the dual-gate dual-body relay in Figure 2.14(b). The gate electrode in the suspension gate stack is subdivided into two equally-sized gate electrodes and the fixed body electrode is subdivided into two equally-sized body electrodes. The overlap area between gate 1 to body 1 is the same as that between gate 2 to body 2. Meanwhile, there is zero overlap area between gate 1 and body 2 or between gate 2 and body 1. Depending

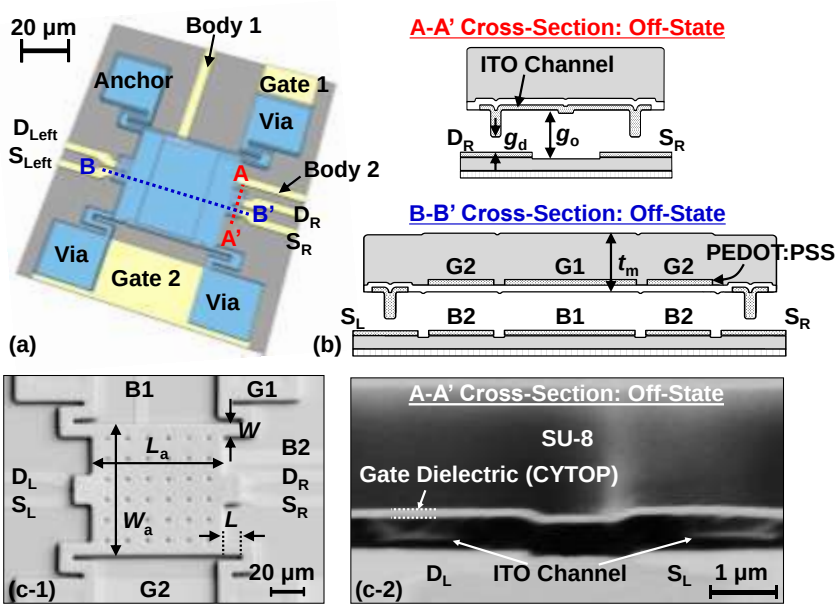

Figure 2.14 (a) Isometric schematic of the dual-gate dual-body organic MEM relay. (b) Cross-section views across A-A' and B-B' in the off-state of the relay. (c-1) Plan-view and (c-2) cross-section view SEMs of the relay.

Table 2.4 Design parameters and values of the dual-gate dual-body relay

Parameter	Value
W	6, 8, 10 μm
L	10, 13, 16, 19 μm
$W_a = L_a$	64 μm
$t_m = t_{SU\text{-}8} + t_{PEDOT:PSS} + t_{CYTOP}$	1.96 μm = 1.8 μm + 70 nm + 90 nm
$g_o = 4 \cdot g_d$	0.6 μm
Channel (Total: 2)	10 × 4 μm^2 each
Dimple (Total: 4)	1.5 × 1.5 μm^2 each
$E_{CYTOP} = 0.7 \cdot E_{SU\text{-}8} = 0.7 \cdot E_{PEDOT:PSS}$	1.4 GPa [56, 57]

on the input combinations, the A_o will be different. Because V_{npi} is proportional to $1/\sqrt{A_o}$ (Equation (2-6)), the V_{npi} value of the relay will be different depending on the input combinations.

3. Organic Relay Fabrication Process

In this chapter, a polymer-based surface-micromachining process is developed to implement the relay designs described in the previous chapter. Solution-processable organic materials, which are beneficial in building large-area circuits at relatively low temperature and low cost [22, 70], are employed to build the organic relays.

In this chapter, process development efforts to achieve well-functioning organic MEM relays for ultralow power, flexible transparent large-area electronics are presented. Also, improved fabrication flow for advanced organic MEM relay design is discussed.

Figure 3.1 shows a five-mask low-thermal-budget process used to fabricate the prototype organic MEM relay. The details of each step are described as follows.

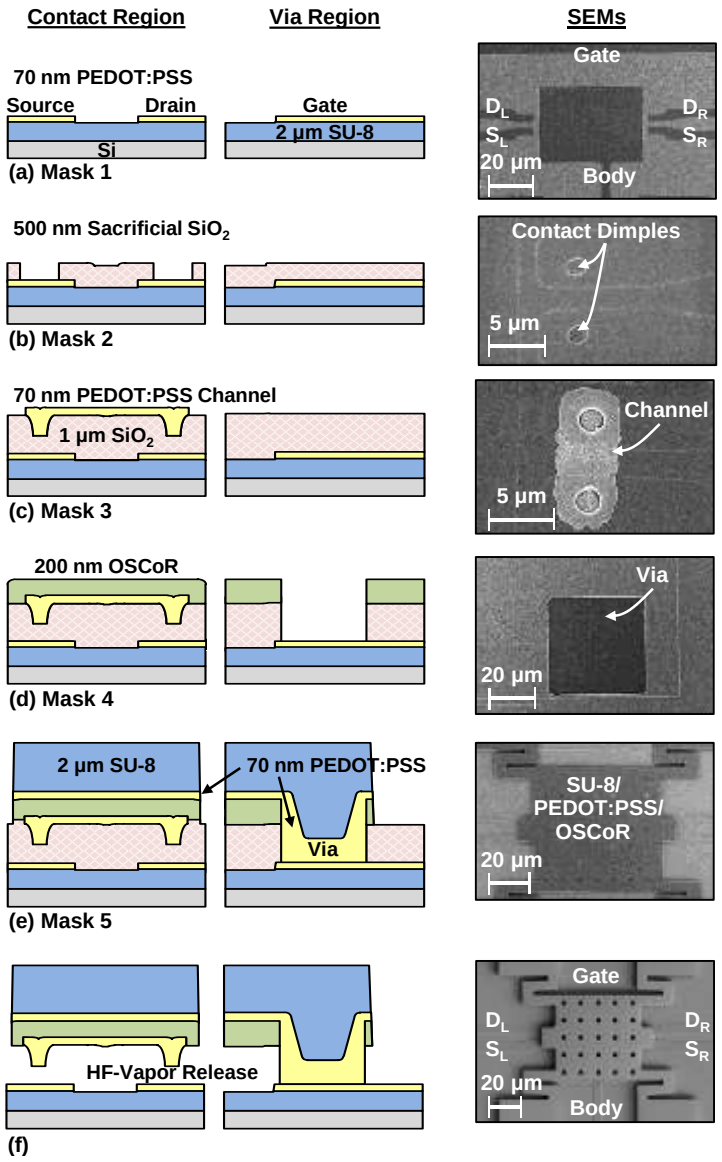

Figure 3.1 Low-thermal-budget (≤ 150 °C) process flow:

(a) Mask 1: Formation of the gate, body, and source/ drain (PEDOT:PSS) on the cross-linked SU-8.

(b) Mask 2: Plasma enhanced chemical vapor deposition (PECVD) and patterning of the 1st sacrificial SiO_2 (500 nm) to form contact dimples.

(c) Mask 3: PECVD of the 2nd sacrificial SiO_2 (500 nm) and the formation of PEDOT:PSS channel.

(d) Mask 4: Formation of gate dielectric (OSCoR 4000 polymer) and vias.

(e) Mask 5: Spin-coating and patterning of the gate stack comprising SU-8, PEDOT:PSS, and OSCoR.

(f) Movable stack released in vapor-phase hydrogen fluoride (HF) at 50 °C.

3.1. Substrate Preparation

The fabrication of the MEM relay starts with the substrate preparation as shown in Figure 3.1(a). Table 3.1 summarizes the process recipe of using SU-8 (MicroChem Corp., SU-8 2002) as the polymer substrate for the relay. SU-8 has robust chemical and thermal stability. It cannot be attacked by most organic solvents used in fabrication such as acetone, Isopropyl Alcohol (IPA), 1-methyl-2-pyrrolidinone (NMP)-based solvents stripper after proper treatment [71, 72]. SU-8 has good resistance to vapor-phase HF, which was used to release the organic MEM relay eventually [73]. SU-8 sustains up to 250 °C and adheres well to Si surface. All these properties make SU-8 a suitable candidate for the organic substrate layer.

SU-8 was spin-coated at 3000 rpm on top of Si wafer, and then, the standard SU-8 process recipe, which includes pre-bake, UV flood exposure, hard-bake, developing, and long-time post-bake, was used to fabricated the substrate (Figure 3.1(a)).

Note that even though the SU-8 is used as substrate without any geometric pattern, it should be rinsed for longer than suggested developing time using propylene glycol

Table 3.1 Fabrication process of SU-8 substrate.

Step	Procedure	Remark
1	Soft-bake SU-8	Baking at 95 °C for 2 minutes
2	UV Exposure	Cross-linking SU-8
3	Hard-bake SU-8	Baking 95 °C for 2 minutes
4	Developing	Rinsing away uncross-linked SU-8
5	Post-bake	Curing SU-8 at 150 °C for 30 minutes

monomethyl ether acetate (PGMEA) to get rid of any uncross-linked SU-8 after UV flood exposure and hard-bake. Also, SU-8 needs to be cured at 150 °C for 30 minutes to become fully cross-linked. SU-8 becomes a chemical robust and optical transparent permanent substrate after these treatments. Otherwise, SU-8 could form bubbles during the subsequent fabrication steps due to any uncross-linked residue.

To promote the adhesion between the next layer to the hydrophobic SU-8 surface, SU-8 substrate was first activated with O_2 plasma for 20 seconds with 50 sccm O_2, 200 mT, and 50 W, and then an adhesion promoter (Silquest A-187) was applied prior to the electrode forming step.

3.2. Mask 1: Electrode Definition

A conductive polymer, Poly(3,4-Ethylenedioxythiophene):Polystyrene-Sulfonate [PEDOT:PSS (Clevios PH1000)], was deposited and patterned to form the first electrode layer as shown in Figure 3.1(a). PEDOT:PSS has been explored for use in solar cells [74] and thin-film transistors [75] as a candidate to replace indium tin oxide (ITO) due to its optical-transparency (> 90 % in the visible spectrum [29]) and relatively high conductivity (~10^3 $S \cdot cm^{-1}$ [76]); and stretchable electrodes [77] and strain gauges [78] due to its plasticity and piezoresistive behavior. However, because of its hygroscopic behavior [79], which causes swelling and shrinking of the film upon absorption of moisture, and chemical incompatibility with acid-sensitive photoresists and alkaline developers and strippers used in conventional photolithography [80], fabrication of most PEDOT: PSS-based devices has had to resort to nonconventional lithographic techniques

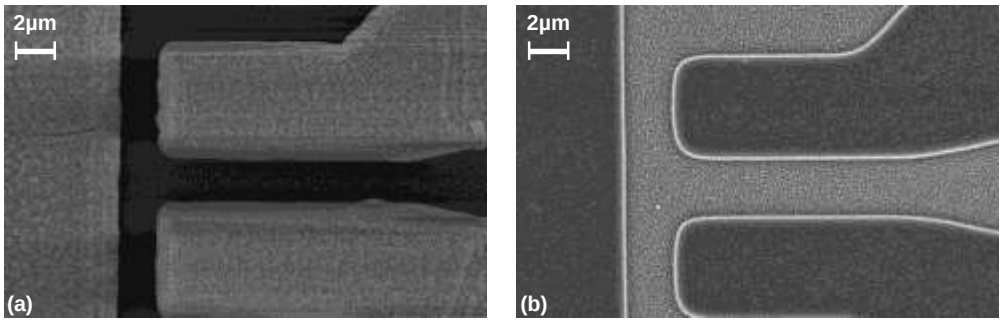

Figure 3.2 The SEMs of the patterned PEDOT:PSS electrode layers using (a) conventional photoresist showing damaged PEDOT:PSS surface and (b) fluorinated photoresist showing intact PEDOT:PSS surface.

such as roll-to-roll and inkjet printing or indirect patterning methods such as lift-off [81]. Most, if not all, PEDOT:PSS-based devices reported to date are fabricated using a single mask layer with poor photolithography resolution, thus limiting their potential applications [73, 80, 82].

PEDOT:PSS reacts with acid-sensitive photoresists and conventional alkaline developers and strippers. Therefore, fluorinated photoresist (Orthogonal, Inc., OSCoR 4000) and fluoroether-based developer and stripper, which are benign to PEDOT:PSS were used to pattern the PEDOT:PSS electrodes on top of SU-8 substrate [80]. Figure 3.2(a) shows the SEM of PEDOT:PSS layer patterned by conventional photoresist (AZ 5214E). Once AZ 5214E is spin coated on PEDOT:PSS, the photoactive compound reacts with PEDOT:PSS due to the acidity of PEDOT:PSS. After the development process using Tetra Methyl Ammonium Hydroxide (TMAH)-based developer, the surface of PEDOT:PSS is damaged [82]. In order to address this issue, organic materials compatible fluorinated photoresist systems were applied to develop the PEDOT:PSS electrode layer.

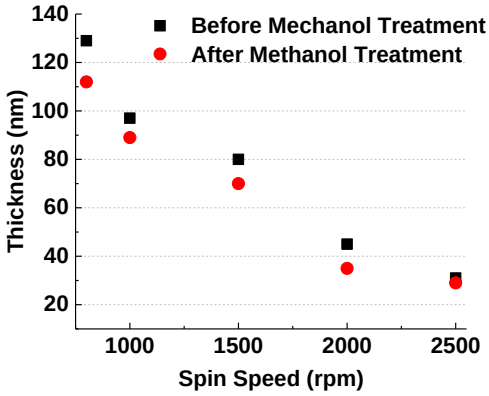

Figure 3.3 The thickness of spin-coated PEDOT:PSS layer *vs.* spin speed. The black square presents the layer thickness of PEDOT:PSS before methanol treatment, and the red dot indicates the layer thickness of PEDOT:PSS after methanol treatment.

As indicated in Figure 3.2(b), the PEDOT:PSS surface remains intact. The conductivity of this patterned PEDOT:PSS layer is unaffected by using four point probe to confirm. The measured resistivity of the film was ~3 Ω·cm *vs.* ~3.2 Ω·cm before *vs.* after the photolithography.

The second challenge in forming PEDOT:PSS electrode is owing to the relatively high (~1 Ω·cm [29]) resistivity of pristine PEDOT:PSS. Post-deposition treatment on the film with acidic solutions [76] or organic compounds such as methanol [76], Ethylene Glycol, and Dimethyl Sulfoxide [29] is the typical method to reduce its resistivity. After the deposition of PEDOT:PSS (Figure 3.1(a)), the substrate was dipped into methanol for a minute. The measured resistivity of the film was ~3 Ω·cm *vs.* ~$2 \cdot 10^{-3}$ Ω·cm before *vs.* after the treatment. The thickness of the spin-coated PEDOT:PSS (Figure 3.3) shows that the treatment of methanol reduces the thickness of PEDOT:PSS due to the removal of the

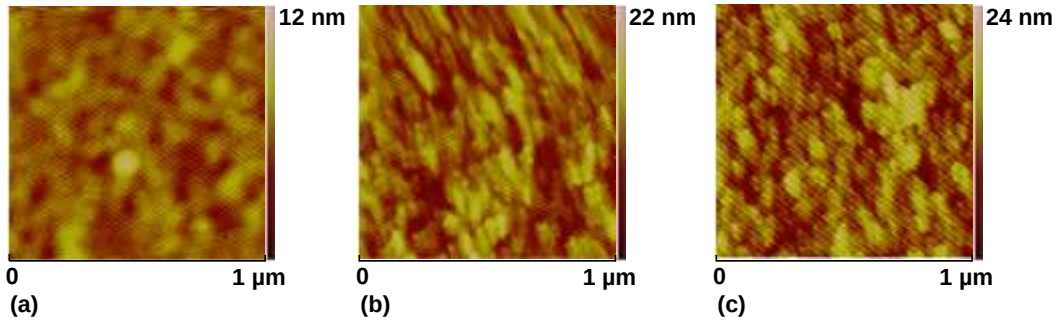

Figure 3.4 AFM images of (a) fresh PEDOT:PSS surface, (b) PEDOT:PSS surface after staying in water for 2 minutes and (c) PEDOT:PSS surface after staying in water for 10 minutes. All the PEDOT:PSS films were spin coated at 1500 rpm on Si wafer and baked at 90 °C for 1 hour.

insulator PSS from the film [76]. By spin coating PEDOT:PSS solution at 1500 rpm, 70 nm PEDOT:PSS film can be formed for the electrode layer.

The third challenge of using PEDOT:PSS is due to its hygroscopic property, *i.e.*, it swells or shrinks when exposed to a water mixture during subsequent fabrication steps. As indicated in Figure 3.4, the PEDOT:PSS surface becomes rougher and wavier when it meets with water molecules because of the volume expansion of the PEDOT:PSS film, which could lead to cracking or delaminating of the film. Note that the optimized baking condition of the PEDOT:PSS is 90 °C for 1 hour. Adhesion promoter (Silquest A-187) was applied after spin-coating and baking of PEDOT:PSS to ensure the better adhesion between PEDOT:PSS and the next layer.

70 nm PEDOT:PSS was spin-coated on the SU-8 substrate at 1500 rpm, baked at 90 °C for 1 hour, and then patterned into the electrodes by photolithography and O_2 plasma

reactive ion etching (RIE, Trion Phantom III reactive ion etcher) at rate of 35 nm/minute with 50 sccm O_2, 30 mT, and 50 W.

3.3. Mask 2: Contact Opening

As shown in Figures 3.1(b) and (c), SiO_2 was deposited via PECVD at rate of 48 nm/minute with 555 sccm SiH_4, 500 sccm N_2O, 900 mT, 25 W, and 100 °C as a sacrificial layer.

In order to select the materials for the sacrificial layer, chemical and thermal compatibility as well as film quality have to be considered thoroughly: (1) The deposition of the sacrificial layer does not chemically damage the organic layers (PEDOT:PSS and SU-8) underneath; (2) The sacrificial layer etching process either by wet etching or dry etching has to be benign to the organic layers (PEDOT:PSS and SU-8) underneath; (3) The sacrificial layer can be selectively etched away eventually in the relay releasing step; (4) The deposition of the sacrificial layer has to perform at low temperature (≤ 150 °C); (5) The deposition of the sacrificial layer requires uniformity and thickness controllability.

Organic materials for sacrificial layer are preferred for low-thermal-budget manufacturing due to their low-temperature deposition process. However, most of the organics are suffering from the possible dissolution upon confronting organic solvent [83], which would be inevitably used in the later process. Thus, they cannot provide reliable sacrificial layer before the final releasing step. On the other side, organic such as CYTOP (Bellex Corp., CTL-809M) has strong chemical resistance to most organic

solvents, acid, and based [84], so that it is too difficult to be etched away completely by any solvent in the releasing step. In addition, it is relatively difficult to control the uniformity and the thickness of the spin-coated organic sacrificial layer.

Inorganic materials would be preferred for sacrificial layer considering the factors such as uniformity and controllability of film thickness. Metal or metal oxide layer such as Al or Al_2O_3 could also be a candidate for the sacrificial layer because their etchants are usually compatible with organic materials [48]. However, wet chemical etching process are prone to stiction due to capillary forces at the interface [83]. The capillary forces caused by the liquid etchant will make the released relay stuck down permanently if the spring resting force (F_{sp}) of the movable beam is insufficient [48, 83]. Therefore, sacrificial layer that can be deposited and selectively dry etched at a relatively low temperature (≤ 150 °C) without affecting other layers is desirable to avoid the stiction issue.

After short-loop experiments and considering all requirements mentioned above, low-temperature PECVD SiO_2 is chosen as a sacrificial layer, which could be selectively etched by vapor HF. The SiO_2 deposition process does not affect the organic layers (PEDOT:PSS and SU-8) underneath. The low-temperature deposition (≤ 150 °C) maintains the low-temperature budget of the whole process flow.

To open the sacrificial layer for the formation of contact dimples, two 2 × 2 μm^2 holes need to be etched away in the first sacrificial layer. As shown in Figure 3.1(b), the SiO_2 layer was patterned by photolithography and removed by a combined dry-wet etching to define contacting regions. Specifically, 400 nm SiO_2 was etched first by RIE (50 sccm

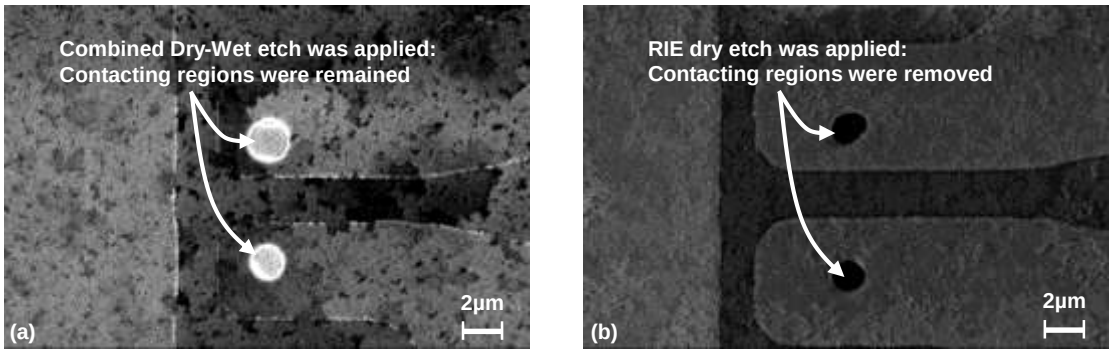

Figure 3.5 The SEMs of (a) sample that the contacting regions were etched by combined dry-wet etching, showing that the bottom electrode (PEDOT:PSS) is intact and (b) sample that the contacting regions were etched by only RIE dry etching, showing the bottom electrode (PEDOT:PSS) is completely removed.

CHF_3 and 50 sccm Ar at 30 mT, and 150 W) at etch rate of 20 nm/minute, leaving approximately 100 nm SiO_2 in the contacting regions to protect the underlying PEDOT:PSS from the dry etching process. The remaining ~100 nm SiO_2 was removed in HF/H_2O vapor (49 % HF) at 50 °C for 15 seconds, to expose PEDOT:PSS surfaces. The application of a combined dry-wet etching is because the etching gases used to etch SiO_2 also etch the PEDOT:PSS film very quickly. If only RIE is applied to open the contact dimples, one cannot ensure the SiO_2 to be completely etched without damaging the PEDOT:PSS underneath. This becomes even severe because over-etching is required to fully open the contacting regions.

Figure 3.5 shows the SEMs of samples using combined dry-wet etching and only dry etching to open the contacting regions. By applying combined dry-wet etching, a reliable contact opening process could be achieved without affecting the PEDOT:PSS underneath.

On the contrary, if only dry etching was applied to open the contacting regions, bottom PEDOT:PSS could be completely removed after the etching process.

3.4. Mask 3: Channel Formation

After the second 500 nm sacrificial layer was deposited, ~70 nm PEDOT:PSS was spin-coated at 1500 rpm on top of SiO_2 to form the conductive channel layer (Figure 3.1(c)).

Because the dimple region is relatively large (2×2 μm^2) and shallow (500 nm), the PEDOT:PSS solution can easily cover every corner of the opened contacting regions to form a continuous layer. After ~70 nm PEDOT:PSS layer was spin-coated at 1500 rpm and baked at 90 °C for 1 hour, OSCoR 4000 and fluoroether-based developer, which are benign to PEDOT:PSS were used to pattern the PEDOT:PSS. Then RIE (50 sccm O_2, 30 mT, and 50 W) was used to the etch the PEDOT:PSS channel layer at etch rate of 35 nm/minute. Note that 20 % O_2 plasma over-etching was applied to assure the complete etch of PEDOT:PSS. Eventually, fluoroether-based stripper was used to strip away the OSCoR 4000 photoresist on top.

3.5. Mask 4: Via Formation

PEDOT:PSS compatible photoresist, the OSCoR 4000, was used as a mask to open vias (Figure 3.1(d)). The via has two functions: Firstly, via forms electrical connection from the gate electrode underneath to the conductive layer in the gate stack; Secondly, the movable beam can be anchored on the substrate by using the vias. Conventional photoresist cannot be used in this step because the photoresist needs to be spin-coated on top of the defined channel layer. The acid-base reaction between the channel

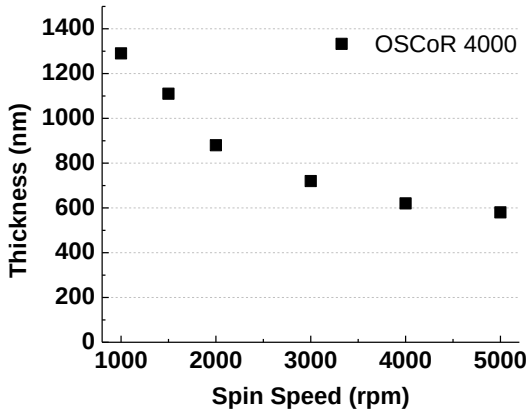

Figure 3.6 The thickness of spin-coated OSCoR 4000 photoresist *vs*. spin speed.

PEDOT:PSS and conventional photoresist can degrade the conductivity of PEDOT:PSS layer or delaminate the PEDOT:PSS layer.

Relatively deep vias (1 μm) are required to be opened through the SiO_2 sacrificial layer and the gases used to etch SiO_2 also etch the OSCoR 4000 very quickly. Note that the SiO_2 dry etching process (50 sccm CHF_3 and 50 sccm Ar at 30 mT, and 150 W) can etch SiO_2 at the rate of ~20 nm/minute and OSCoR 4000 at the rate of ~18 nm/minute. Therefore, a sufficiently thick OSCoR 4000 layer is required to transfer patterns. Figure 3.6 shows the thickness of the OSCoR 4000 at different spin speed. Approximately 1100 nm thick of OSCoR 4000 was achieved at 1500 rpm to form the photoresist mask for vias etching.

A combined dry-wet etching was applied to etch vias and leave the PEDOT:PSS underneath intact. Specifically, 900 nm SiO_2 was first etched via RIE (50 sccm CHF_3 and 50 sccm Ar at 30 mT, and 150 W), leaving approximately 100 nm SiO_2. After that, the

remaining ~100 nm SiO_2 was completely removed in HF/H_2O vapor (49 % HF) at 50 °C for 15 seconds, to expose clean PEDOT:PSS surfaces, and ~200 nm OSCoR 4000 was remained after the vias opening step.

3.6. Mask 5: Movable Structure Formation

The remaining ~200 nm OSCoR 4000 was used as a gate dielectric layer (Figure 3.1(d)) to insulate the PEDOT:PSS channels on both sides to the conductive layer in the movable stack. The purpose of gate dielectric layer is to provide good electrical insulation. Moreover, the following criteria must be considered for gate dielectric layer: (1) Low-temperature (≤ 150 °C) deposition to maintain the low-thermal budget of the process; (2) Uniformity and thickness controllability; (3) Good chemical resistance to vapor HF; (4) Optical transparency; (5) Good etching selectivity between gate dielectric layer and SiO_2 sacrificial layer. (6) Low residual thermal stress to enable low vertical strain gradient within the gate stack [39].

Two candidates were selected as dielectric candidates via short-loop experiments because they satisfy most of the requirements of the gate dielectric mentioned above. The SEMs of the released gate stack samples with 10 nm atomic layer deposition (ALD) deposited Al_2O_3 and 200 nm spin-coated OSCoR as gate dielectric layers are shown in Figure 3.7. Figure 3.8 illustrates two kinds out-of-plane deflections of the structure beams. It appears that the released gate stack with SU-8 beam (1 μm) and Al_2O_3 (10 nm) has a concave upward shape due to a positive strain gradient. During the SU-8 layer formation, the sample has to be heated up to 95 °C in order to conduct photolithography. Because the

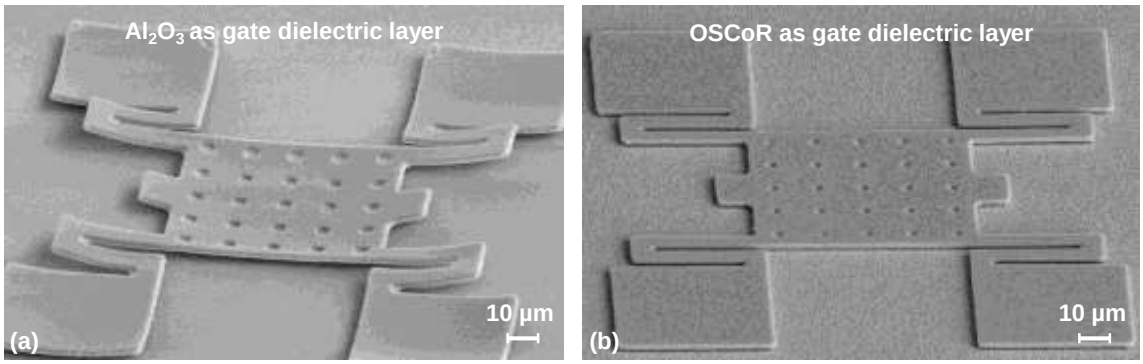

Figure 3.7 SEMs of the movable gate stacks (a) with 10 nm Al_2O_3 as dielectric underneath 1 μm SU-8 and (b) with 200 nm OSCoR as dielectric underneath 1 μm SU-8.

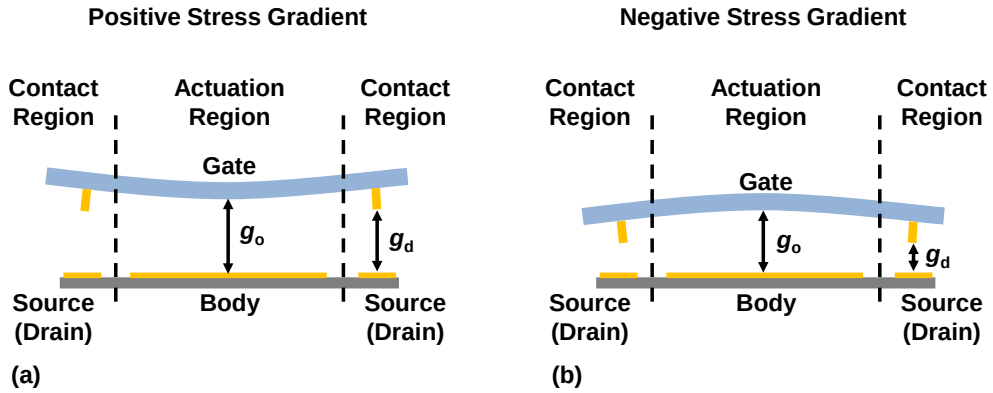

Figure 3.8 Simplified cross-section schematics of MEM relays with non-zero stress gradient. (a) Positive stress gradient results in a concave upward beam structure. (b) Negative stress gradient results in a concave downward beam structure. The out-of-plane deformation results the actual g_o and g_d to be different from the as-fabricated g_o and g_d.

thermal expansion coefficient of SU-8 ($52 \cdot 10^{-6}$ K^{-1} [85]) is larger than that of Al_2O_3 ($7.5 \cdot 10^{-6}$ K^{-1} [86]), Al_2O_3 film is under compressive stress. Due to the positive stress gradient created within these two layers, Al_2O_3 tends to expand more than SU-8, which results in severe concave downward shape after the suspended gate stack is released. The bending up of the beam leads to vertical deflection in both g_o and g_d. The actual g_o and g_d

are therefore larger than the designed values. It is measured from SEMs of gate stack samples with different dimensions (Table 2.1) that the deflections range from 300 nm to 1 μm. However, the released gate stack with SU-8 (1 μm) and OSCoR (200 nm) shows small strain gradient within the layers and the gate stack exhibits unmeasured concave downward shape. That is because most of organic materials have the thermal expansion coefficients in the same order [87]. It is measured from SEMs of gate stack samples with different dimensions (Table 2.1) that the deflections are all within 40 nm. Ideally, zero strain gradient within different layers in gate stack is desirable to ensure zero out-of-plane deflection of the movable beam, so that the as-fabricated g_o and g_d are identical to the actual g_o and g_d. The low strain gradient within the gate stack with OSCoR as the gate dielectric material is therefore make it more suitable than Al_2O_3 to form the gate insulator.

OSCoR has good chemical resistance to vapor HF. OSCoR film can be easily etched by O_2 plasma, but O_2 plasma will not etch SiO_2 sacrificial layer. Therefore, using OSCoR as gate insulator ensures a good etching selectivity between gate dielectric layer and SiO_2 sacrificial layer. The deposition of OSCoR layer is a low temperature process because the maximum temperature of applying OSCoR is 95 °C (baking temperature).

The disadvantage of using organic material as gate insulator is that the uniformity and thickness is not easy to control compared with using inorganic material [88]. Because inorganic material is commonly deposited by Physical Vapor Deposition (PVD) or Chemical Vapor Deposition (CVD), the uniformity and thickness controllability are

therefore better. According to the step profiler measurements (Dektak stylus profiler), the spin-coated OSCoR gate dielectric layer has ~13 % un-uniformity along the wafer, the film is thicker at the center of the wafer and thinner at the edge.

On top of the gate dielectric layer, ~ 70 nm PEDOT:PSS film was spin-coated and baked at 90 °C for 1 hour to form the conductive layer in the gate stack. The PEDOT:PSS is the gate electrode layer that provides electrical path through the vias (Figure 3.1(e)) to gate electrode on the first electrode layer.

After the formation of conductive layer in the gate stack, a thick mechanical layer is required to form the movable beam. A soft actuation structure is desirable to minimize the switching energy (E_s) because $E_s \propto V_{dd}^2$ and $V_{dd} \propto 1/\sqrt{k_{eff}}$ [39]. The k_{eff} of the structural beam is proportional to Young's modulus (E) of the beam material. Therefore, materials with small Young's modulus are preferred to manufacture the relay for low power application.

The Young's modulus values of some common inorganic and organic materials used in micro-electro-mechanical systems (MEMS) are summarized in Table 3.2. Since the Young's modulus values of organic materials are typically smaller than those of inorganic materials [48], organic materials are therefore chosen to build a soft actuation beam for low energy application.

Table 3.2 Young's modulus of common materials used in MEMS [48, 67, 68, 89, 90].

Material	Value (GPa)
Platinum	168
Poly-Si	158
SiGe	140
Gold	79
PS	3
PMMA	2.4
SU-8	2
Polyethylene	2
PEDOT:PSS	2
CYTOP	1.4

2.0 μm SU-8 (MicroChem Corp., SU-8 2002) was applied on top of PEDOT:PSS as the thick mechanical layer (Figure 3.1(e)). SU-8 was selected to form the actuation plate because: (1) SU-8 is one of the common thick polymers used in organic MEMS devices [90]; (2) SU-8 has good chemical resistance to organic solvents, acid, and vapor HF; (3) SU-8 can be spin-coated on top of acid PEDOT:PSS surface without degradation [91]; (4) SU-8 is a negative photoresist. The geometric shape of the actuation beam and the etch holes (2×2 μm^2) of the beam can be patterned by UV exposure without metal mask [73, 90].

After the SU-8 was patterned, the residual ~70 nm PEDOT:PSS and ~200 nm OSCoR in the gate stack were etched by O_2 plasma RIE (50 sccm O_2, 30 mT, and 100 W). Because the O_2 plasma etches SU-8, PEDOT:PSS, and OSCoR 4000, the etch rate of each layer needs to be carefully considered. The etch rates for different organic materials under different conditions are summarized in Table 3.3. According to this table, 37 seconds

Table 3.3 RIE O_2 plasma etch rates for organic materials used in the MEM relay process.

Etch Rate (nm/minute)					Pressure (mT)	RF Power (W)	O_2 Flow (sccm)
CYTOP	PEDOT:PSS	AZ 5214	SU-8	OSCoR 4000			
48	14	11	21	60	30	30	50
60	35	14	43.2	96	30	50	50
274	161	62	102	216	30	80	50
630	267	161	159	588	30	100	50
1014	363	241	168	912	30	150	50
504	240	132	120	468	15	100	50
612	276	173	196	534	30	100	50
817.2	367	232	212	786	50	100	50

were required to completely etch ~70 nm PEDOT:PSS and ~200 nm OSCoR. As a result, ~100 nm SU-8 was etched. 20 % O_2 plasma RIE over-etching was conducted to fully pattern the movable gate stack (Figure 3.1(e)).

Lastly, all the fabricated relays were released in HF/H_2O vapor (49 % HF) at 50 °C for 18 minutes (Figure 3.1(f)).

3.7. Process Improvements

Improvements to the process are required due to the several limitations in the prototype organic MEM relay. Because of the limited conductivity of PEDOT:PSS, inorganic materials are used for contacting electrodes to reduce the on-state resistance. New organic materials and fabrication steps are also employed to realize thinner gate dielectric layer formation and more reliable fabrication. The improved six-mask process is illustrated in Figure 3.9. The key improvements are described as below: (1) In the electrode definition step (Figure 3.9(a)), PEDOT:PSS was pre-mixed with 5 % ethylene

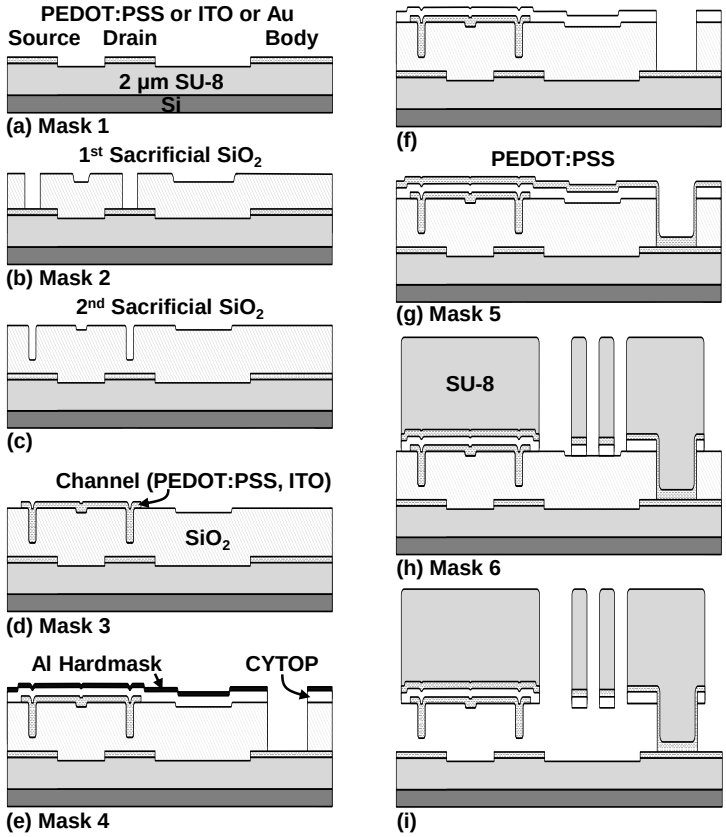

Figure 3.9 Refined Low-temperature (≤ 150 °C) five-mask fabrication process flow.

(a) Mask 1: Formation of the gate, body, and source/drain using PEDOT:PSS, ITO or Au.

(b) Mask 2: PECVD and patterning of the 1st sacrificial SiO_2 to form contact dimples.

(c) PECVD of the 2nd sacrificial SiO_2.

(d) Mask 3: Formation of channel using PEDOT:PSS or ITO.

(e) Mask 4: Spin-coating CYTOP as gate dielectric and deposits Al on top of CYTOP to treat the surface of CYTOP and form hardmask.

(f) CYTOP becomes hydrophilic and ready for PEDOT:PSS coating in next step after stripping Al.

(g) Mask 5: Formation of PEDOT:PSS gate layer.

(h) Mask 6: Spin-coating and patterning of the structural SU-8, then etching PEDOT:PSS and CYTOP to form the gate stack.

(i) Movable stack released in vapor HF at 50 °C

glycol (EG) to lower its resistivity [92]. Inorganic materials ITO and gold (Au) were used due to the low resistivity and good chemical resistance to vapor HF. The measured resistivity of deposited ITO and Au were $2 \cdot 10^{-4}$ Ω·cm and $4 \cdot 10^{-8}$ Ω·cm, respectively; (2) In the channel formation step (Figure 3.9(d)), ITO film was used in order to reduce the on-state resistance; (3) CYTOP was used to replace the OSCoR 4000 to achieve thinner gate insulator layer (Figure 3.9(e)); (4) A new mask was added in the fabrication process as shown in Figure 3.9(g) to remove the overlap area between the conductive polymer PEDOT:PSS in the movable structure to the underneath source and drain electrodes on both sides of the relay.

As shown in Figure 3.9(a), PEDOT:PSS, ITO (comprising 90 % In_2O_3 and 10 % SnO_2) and Au were used as the electrode material for the fully- and partially-polymeric relays, respectively. All these three materials have good resistance to HF vapor release etching. As transparent conductive materials, PEDOT:PSS and ITO also have good optical transparency (> 85 % [93] and ~ 90 % [94], respectively) and relatively low resistivity (~1 Ω·cm [93] and ~10^{-4} Ω·cm [94], respectively).

For fully-polymeric relay, prior to deposition, PEDOT:PSS was mixed with 5 % EG to lower its resistivity [92] and filtered once through a nylon-membrane syringe filter (that has a pore size of 0.45 μm) to remove large agglomerates [95]. Measured resistivity of 70 nm PEDOT:PSS was 3 Ω·cm *vs.* $5 \cdot 10^{-3}$ Ω·cm before *vs.* after mixing with EG. Fluorinated photoresist (Orthogonal, Inc., OSCoR 4001) and fluoroether-based developer

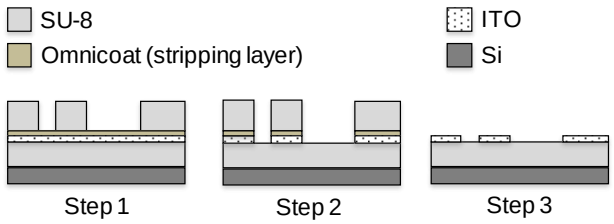

Figure 3.10 The fabrication steps of forming ITO electrodes. Step 1: Patterning of SU-8 on top of Omnicoat stripping layer (~5 nm). Step 2: Etching Omnicoat and ITO layers. Step 3: Stripping the SU-8 layer by removing the Omnicoat with NMP-based solvent.

and stripper [80] were used to pattern PEDOT:PSS (Figures 3.5(a) and (d)) and the sacrificial layer in Figure 3.5(b) where PEDOT:PSS surfaces were exposed.

For partially-polymeric relay, either ITO or Au was used as the electrode layer. ITO was deposited via DC magnetron sputtering for the electrode layer in Figures 3.9(a) and (d). A deposition rate of 6.8 nm/minute was achieved with 85 sccm Ar, 3.5 mT, and 150 W. The ITO layer was patterned into the gate, source, drain, and body (Figure 3.9(a)) and channel (Figure 3.9(d)) with photolithography and inductively coupled plasma reactive ion etching (ICP-RIE). The ITO etching recipe was: 90 sccm HBr, 10 sccm Cl_2, 20 sccm Ar, 30 mT, 800 W ICP power, and 100 W RIE power, and the etch rate was ~21 nm/minute.

The photolithography and etching of ITO are not straightforward because normal positive photoresist cannot stand the high-power plasm used in the ICP-RIE etching. However, if robust negative photoresist such as SU-8 is used, it becomes difficult to be removed after UV exposure. High temperature O_2 ash or long-time wet photoresist stripping is not practical since it would damage the SU-8 substrate. Therefore, a lift-off process involving

SU-8 as photoresist and Omnicoat [96] as stripping layer was applied (Figure 3.10). Specifically, on top of sputtering deposited ITO surfaces, ~5 nm Omnicoat stripping layer was spin-coated at 2000 rpm and baked at 150 °C for 2 minutes. SU-8 was then spin-coated and patterned via UV exposure to form the electrode mask. Short O_2 plasma RIE (50 sccm O_2, 30 mT, and 50 W) was applied first to etch Omnicoat layer at etch rate of ~40 nm/minute, then ICP-RIE (90 sccm HBr, 10 sccm Cl_2, 20 sccm Ar, 30 mT, 800 W ICP power, and 100 W RIE power) was conducted to etch ITO layer at etch rate of ~21 nm/minute. After the ITO layer was defined, SU-8 mask was removed easily with Omnicoat in NMP-based solvent stripper with ultrasonic agitation for 2 minutes, leaving the clean ITO surface and intact SU-8 substrate. Omnicoat is a good stripping layer as it does not affect the UV exposure of SU-8, and it can be etched in O_2 plasma. Most importantly, it can be easily removed using NMP based solvent stripper.

Cr/Au was deposited via electron-beam (E-Beam) evaporation to form the electrode layer on top of the SU-8 substrate (Figure 3.9(a)). Conventional lift-off process using positive photoresist AZ 5214E was applied for the formation of the Au electrodes.

CYTOP is used for the gate dielectric in the improved process due to several reasons: (1) The thickness of CYTOP can be controlled easily than OSCoR polymer by diluting the CYTOP solution with fluorinated solvents [97]; (2) CYTOP is compatible with PEDOT:PSS film; (3) CYTOP has good insulating property and low pinhole defect density [84]; (4) CYTOP has good resistance to HF vapor release etching and optical transparency (> 95 %) [84, 98].

The process involving via formation as shown in Figures 3.9 (e) and (f) is updated due to the replacement of the gate dielectric material. CYTOP was diluted with a fluorinated solvent (Bellex Corp., CT-SOLV 180) in the ratio of 1:3, and the diluted CYTOP was spin-coated at 2000 rpm and cured at 95 °C for 30 minutes to form a 90 nm thick body dielectric layer. This was followed by electron-beam evaporation, patterning, and etching of 40 nm Al. Using the Al layer as a hardmask, CYTOP was etched in O_2 plasma at etch rate of ~60 nm/minute with 50 sccm O_2, 30 mT, and 50 W (Table 3.3), and the sacrificial layer was etched by combined dry-wet etching as in Figures 3.9(b) and (e)). The substrate was immersed in a phosphoric-acid-based etchant (Transene Inc., Al etchant Type A) at 30 °C for 2 minutes to strip the Al hardmask and produce via holes (Figure 3.9(f)). It should be noted that the Al layer was employed not only for serving as a hardmask, but also for modifying the surface property of CYTOP. Due to interactions at the Al/CYTOP interface (between Al atoms and the carbonyl functional groups of CYTOP), the end-groups of CYTOP are oriented toward the interface [97], and the surface of CYTOP becomes hydrophilic. This wettability is critical to ensure adhesion of the subsequent PEDOT:PSS layer to CYTOP.

Afterward, ~70 nm PEDOT:PSS was deposited by spin-coating at 1500 rpm and baking at 90 °C for 1 hour (Figure 3.9(g)). This PEDOT:PSS layer, which was positioned between CYTOP and the following structural SU-8, overlays the via-holes to provide electrical connection between the movable structure and gate electrode (Figure 3.9(h)).

Prior to the deposition of SU-8 (that serves as the structural material and as a hardmask for the following PEDOT:PSS and CYTOP etching), the substrate was immersed in 1 mol. % NaCl for 60 seconds, which was an important step that ensures proper patterning of SU-8 later. The surface treatment promotes ion exchange between monovalent cations Na+ and mobile counter-ions of the anionic sulfonate functional groups of PSS and hence prevents the as-deposited SU-8 from being cross-linked (even before exposure to UV light) by the underlying (acidic) PEDOT:PSS [91]. After the treatment, 4.3 μm SU-8 (MicroChem Corp., SU-8 2005) was spin-coated at 3000 rpm, pre-baked at 95 °C for 2 minutes, cross-linked by UV light for 2 seconds, post-exposure baked at 95 °C for 25 seconds, and developed in PGMEA for 130 seconds. Using SU-8 as a mask, PEDOT:PSS and CYTOP were completely removed (Figure 3.9(h)) by RIE at etch rate of 35 nm/minute with 50 sccm O_2, 30 mT, and 200 W (Unaxis 770 Etcher). The thickness of SU-8 was reduced to 2.3 μm after the plasma etching. Lastly, all the fabricated relays were released in HF/H_2O vapor (49 % HF) at 50 °C for 18 minutes (Figure 3.9(i)).

4. Relay Characterizations

Organic MEM relay would be a promising candidate as alternative or complement to OTFT for ultra-low-power electronics due to its ideal characteristics of zero off-state leakage and abrupt switching property. In this chapter, static switching characteristics such as I_{ds}-V_{gb}, I_{ds}-V_{ds}, body bias effect, and complementary switching, and dynamic switching characteristics including turn-on and turn-off switching delays are investigated. Switching endurance and the influences of temperature and humidity on current-voltage characteristics are also investigated. Using a single relay that incorporates multiple input and output electrodes, various basic logic and carry-generate functions are demonstrated.

4.1. Current-Voltage (*I*-*V*) Characteristics

4.1.1. I_{ds}-V_{gb} Curves

Figure 4.1 shows measured I_{ds}-V_{gb} characteristics of the fabricated prototype relay (g_o = 1 μm, g_d = 500 nm). The measurement was conducted using semiconductor device analyzer (Agilent B1500A). Relay switching characteristics: zero off-state leakage current due to an air gap between the channel and source/drain on either side (on the order of fA, which is the noise level of the semiconductor parameter analyzer used for testing), abrupt on/off switching behavior (< 1 mV/dec), and relatively high on/off current ratio (I_{on}/I_{off}) of ~10^5 were observed. The measured pull-in voltage (V_{pi}) value (V_{pi} = 24.2 V at V_g = 0 V) is larger than the theoretical value (V_{pi} = 22.0 V at V_b = 0 V) obtained from Equation (2-5) due to a small negative strain gradient within the gate stack, which makes the actual g_o approximately 100 nm larger than the as-fabricated g_o of 1 μm. Increasing the drain bias

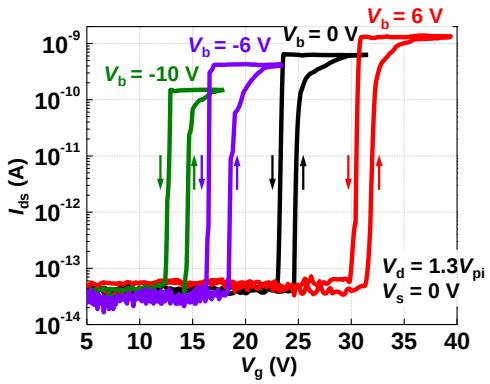

Figure 4.1 Measured I_{ds}-V_{gb} characteristics of the prototype relay for various body biases at 25 °C in air at 1 atm. Immeasurably-low off-state leakage current and abrupt switching behavior were observed. Dimensions of the relay: actuation gap thickness g_o = 1 μm, dimple gap thickness g_d = 500 nm, folded-flexure width W = 5 μm, folded-flexure length L = 10 μm, actuation plate width and length W_a = L_a = 57 μm, and movable gate stack thickness t_m = 2.27 μm.

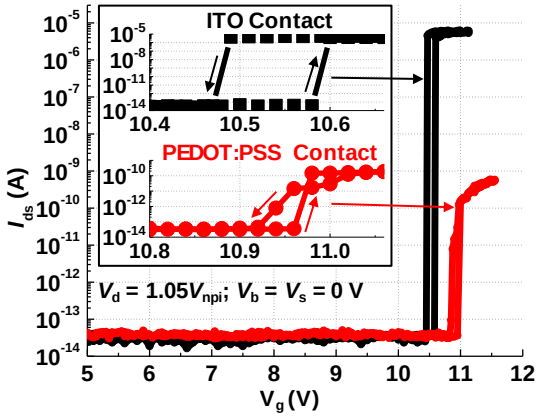

Figure 4.2 Measured I_{ds}-V_{gb} curves of the fully- and partially-polymeric single-gate dual-body relays at 25 °C in air at 1 atm. Maximum V_g = 1.05V_{npi} = V_{dd}. Body 1 and Body 2 were tied together to form a body terminal. Dimensions of the relays: g_o = 700 nm, g_d = 200 nm, W = 7 μm, L = 15 μm, W_a = L_a = 57 μm, and t_m = 2.46 μm.

voltage ($V_d = 1.3 \cdot V_{pi}$) decreases the on-state resistance (R_{on}): 57.7 GΩ, 50.4 GΩ, and 30.4 GΩ for V_b of -6 V, 0 V, and 6 V, respectively. These are larger than those expected for hard contact materials (< ~10 KΩ for tungsten [99]) because of the finite conductivity of Poly(3,4-Ethylenedioxythiophene):Polystyrene-Sulfonate (PEDOT:PSS) (~10^2 S·cm^{-1} for the film treated with methanol). The conductivity of PEDOT:PSS can be further increased by mixing it with highly-conductive metallic particles such as graphene [100] and/or treating it with formic acids [76]. The drain electrode was biased at a value 30 % larger than V_{pi} for each body bias to achieve a stable contact after the relay is pulled-in; I_{ds} still increases for V_g values above V_{pi} because the number of asperities in contact increases with increasing gate overdrive (V_g–V_{pi}). Hysteresis behavior (V_{pi}–V_{rl} > 0 V) is caused by non-zero surface adhesion force (F_a) in the contact regions and pull-in mode operation, which can be remedied by using proper surface-coating materials [101] and operating the relay in non-pull-in mode with $g_d/g_o < 1/3$ [59].

The Measured I_{ds}-V_{gb} characteristics of the fully- and partially-polymeric single-gate dual-body relays (g_o = 700 nm, g_d = 200 nm) are shown in Figure 4.2. Fully polymeric relay has PEDOT:PSS as contact and partially-polymeric relay has indium tin oxide (ITO) as the contact. In the off-state, both relays exhibit a near-zero leakage current I_{off} of ~10 fA due to the air gap of (as-fabricated) thickness g_d (200 nm) between the channel and pair of source/drain on either side. The relays turn on abruptly at non-pull-in voltage (V_{npi}) when the voltage between the gate and body (V_{gb}) is increased from 0 V to supply voltage (V_{dd}), which is set at 1.05V_{npi}. Measured V_{npi} values (10.6 V and 11 V) are slightly different from each other due to process-induced variations; they are smaller than the V_{npi}

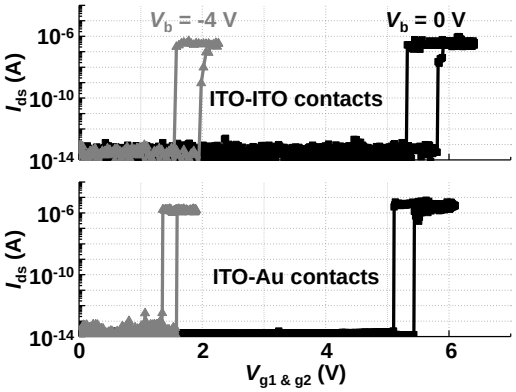

Figure 4.3 Measured I_{ds}-V_{gb} curves of the partially-polymeric dual-gate dual-body relays—one with ITO source and drain (S/D) and the other with Au S/D—for different body biases at 25 °C in air at 1 atm. Body 1 and Body 2 were tied together and biased to 0 V (black ink above) or -4 V (gray) for each relay. Gate 1 and Gate 2 were also tied together. Maximum $V_{g1} = V_{g2} = 1.1 \cdot V_{npi} = V_{dd}$, V_s = 0 V, and $V_d = V_{dd}$. Dimensions of the relays: g_o = 600 nm, g_d = 150 nm, W = 6 μm, L = 16 μm, $W_a = L_a$ = 64 μm, and t_m = 1.96 μm.

value (11.5 V) obtained from Finite-Element-Analysis (FEA) since a slight positive strain gradient within the movable structure (SU-8/PEDOT:PSS/CYTOP) makes the actual g_o ~30 nm narrower than the as-fabricated g_o (700 nm). The partially-polymeric relay, which employs ITO as the contact material, shows a larger on-state current I_{on} of 5.3 μA at V_{dd} (or equivalently, lower on-state resistance R_{on} of 2.1 MΩ) and higher I_{on}/I_{off} ratio of 10^8, compared with the fully-polymeric relay ($I_{on} \cong$ 0.6 nA, $R_{on} \cong$ 2.3 GΩ, and $I_{on}/I_{off} \cong 10^5$). I_{on} of the partially-polymeric relay remains relatively constant for $V_{gb} \geq V_{npi}$, *i.e.*, stable ohmic contacts are formed between the ITO channel and source/drain. Conversely, I_{on} of the fully-polymeric relay increases gradually for $V_{gb} \geq V_{npi}$. The observed discrepancies in the on-state characteristics result from the differences in electrical and

mechanical properties of PEDOT:PSS and ITO. Firstly, measured resistivity of the as-deposited ITO layer ($2 \cdot 10^{-4}$ Ω·cm) is an order of magnitude smaller than that of the as-deposited PEDOT:PSS layer ($5 \cdot 10^{-3}$ Ω·cm). While the resistivity of ITO remains rather unaffected by changes in humidity, the resistivity of PEDOT:PSS increases steadily over time by about 40 % when the relay is left under ambient relative humidity (60 % RH) [97]. This increase in resistivity is because PEDOT:PSS tends to absorb moisture from ambient air until it reaches an equilibrium moisture content [29], as expected for typical polymers. Secondly, elastic modulus (E) and hardness of PEDOT:PSS (2 GPa and 150 MPa, respectively [68, 102]) are approximately two orders of magnitude smaller than those of ITO (190 GPa and 16 GPa, respectively [103, 104]). Because PEDOT:PSS is relatively soft (easily deformable and malleable), the number of elastically- and/or plastically-deformed asperities and hence total contact area between the PEDOT:PSS surfaces increases for $V_{gb} \geq V_{npi}$, *i.e.*, an increasing number of current paths is formed at the interface as the compressive load between the channel and source/drain increases, thus causing a larger I_{on} at $V_{gb} = V_{dd}$ than at V_{npi}.

Figure 4.3 shows measured I_{ds}-V_{gb} curves for two types dual-gate dual-body relays (g_o = 700 nm, g_d = 200 nm)—one with ITO S/D and the other with gold (Au) S/D with different body biases. Both relays show off-state leakage current below 100 fA, abrupt switching behavior, and I_{on}/I_{off} above 10^7. V_{npi} is reduced commensurately from 5.81 V to 1.95 V for the relay with ITO S/D and from 5.43 V to 1.56 V for the relay with Au S/D when the body bias (V_b) is adjusted to -4 V. The R_{on} is measured to be smaller for the relay with Au S/D (≅ 0.9 MΩ) than that for the relay with ITO S/D (≅ 5.6 MΩ) because

the ‘contact’ resistance at the interface between the ITO channel and Au S/D: $R_c \cong 0.9$ MΩ—which is dominant over the resistances associated with the channel and S/D themselves: $R_{ch} \cong 0.2$ kΩ and $R_{s/d} \cong 60$ Ω—is estimated to be smaller than that between ITO and ITO ($R_c \cong 6$ MΩ, $R_{ch} \cong 0.2$ kΩ, and $R_{s/d} \cong 4.2$ kΩ). Each of the relays shows a hysteresis voltage, *i.e.*, each requires an input voltage swing to be at least 480 mV or 310 mV, respectively, to switch on/off, due to adhesive forces between the (dis)similar surfaces.

4.1.2. I_{ds}-V_{ds} Curves

Figure 4.4 shows measured I_{ds}-V_{ds} characteristics of the prototype relay (g_o = 1 μm, g_d = 500 nm). A diode behavior is observed due to a potential energy barrier to electron flow (Φ_B = ~0.8 eV) between the PEDOT:PSS (Φ_P = ~5.3 eV [105]) and the tungsten probe tip (Φ_M = ~4.5 eV) used for testing. I_{ds} increases (or R_{on} decreases) with larger gate overdrives (V_g–V_{pi}) for a given V_{ds} because the contact force between the channel and source/drain contacting surfaces increases and thus the number of contacting asperities on the surfaces increases.

Measured I_{ds}-V_{ds} characteristics of the single-gate dual-body relays (g_o = 700 nm, g_d = 200 nm) are shown in Figure 4.5. The partially-polymeric relay (with ITO contacts) shows a linear (Ohmic) behavior as expected, while the fully-polymeric relay shows a diode-like behavior at low V_{ds} due to the potential energy barrier to electron flow (Φ_B = 0.8 eV) between PEDOT:PSS (Φ_P = 5.3 eV [105]) and the tungsten probe tip (Φ_W = 4.5 eV) used for testing. For a given V_{ds}, I_{ds} increases (or R_{on} decreases) with increasing gate

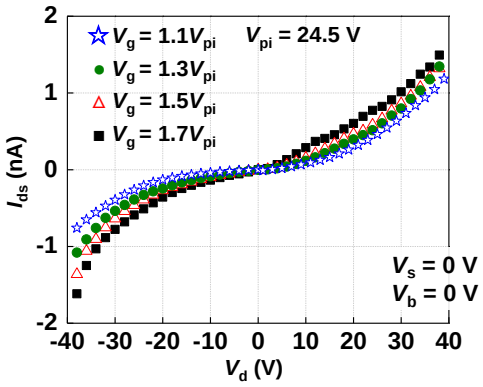

Figure 4.4 Measured I_{ds} as a function of V_d of the prototype relay (in Figure 4.1) at 25 °C in air at 1 atm. A diode behavior is seen due to a potential energy barrier between the PEDOT:PSS and the tungsten probe tip used for testing. A stronger gate-overdrive (V_g–V_{pi}) for a given V_d results in a larger on-state current, I_{ds}. Dimensions of the relay: g_o = 1 µm, g_d = 500 nm, W = 5 µm, L = 10 µm, W_a = L_a = 57 µm, and t_m = 2.27 µm.

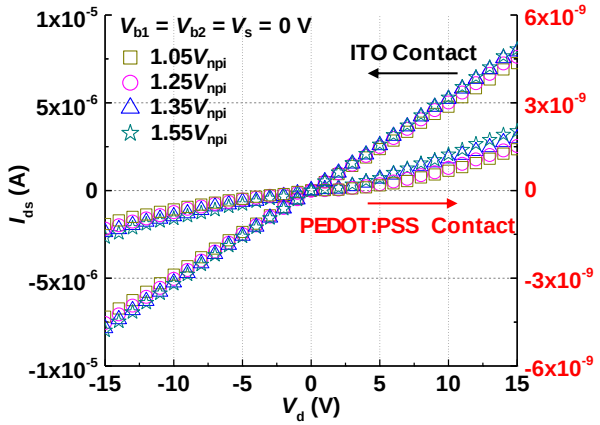

Figure 4.5 Measured I_{ds}-V_{ds} characteristics of the fully- and partially-polymeric single-gate dual-body relays (in Figure 4.2) at 25 °C in air at 1 atm for various gate overdrive voltages. Maximum $V_g = n \cdot V_{npi}$, where n is as shown in the inset. Dimensions of the relays: g_o = 700 nm, g_d = 200 nm, W = 7 µm, L = 15 µm, W_a = L_a = 57 µm, and t_m = 2.46 µm.

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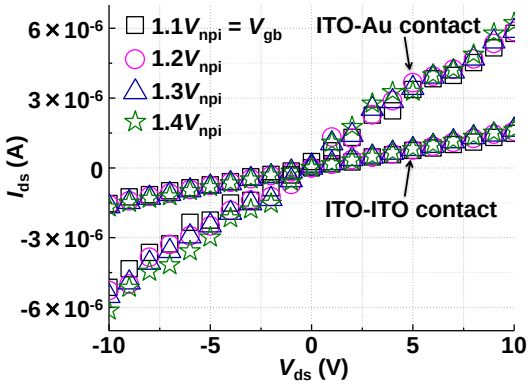


Figure 4.6 Measured I_{ds}-V_{ds} characteristics of the partially-polymeric dual-gate dual-body relays (in Figure 4.3) for various gate overdrive voltages at 25 °C in air at 1 atm. $V_{g1} = V_{g2}$ and $V_b = V_s = 0$ V. V_{gb} was set to 110 % of V_{npi} or larger, as indicated in the figure. Dimensions of the relays: g_o = 600 nm, g_d = 150 nm, W = 6 μm, L = 16 μm, $W_a = L_a$ = 64 μm, and t_m = 1.96 μm.

overdrive voltage (V_{gb}–V_{npi}) for both relays because the number of contacting asperities between the channel and source/drain increases with V_{gb}–V_{npi}. The contact resistance (R_c) at the interfaces between the channel and source/drain can be calculated:

$$R_c = R_{on} - R_{s/d} - R_{ch} \tag{4-1}$$

where $R_{s/d}$ and R_{ch} are the resistances associated with the source/drain and channel, respectively. $R_{s/d}$ and R_{ch} are calculated to be 1.8 KΩ and 72.3 Ω, respectively, for the partially-polymeric relay, and 42.2 KΩ and 1.8 KΩ, respectively, for the fully-polymeric relay. Since R_{on} are 2.1 MΩ and 2.3 GΩ for the ITO and PEDOT:PSS contacts, respectively, which are dominant over $R_{s/d}$ and R_{ch}, R_c can be considered equal to R_{on}.

Both of the partially-polymeric dual-gate dual-body relays (g_o = 600 nm, g_d = 150 nm), exhibit a linear I_{ds}-V_{ds} behavior (Figure 4.6) as expected due to the Ohmic metallic contacts. R_{on} decreases with increasing (V_{gb}–V_{npi}) because the number of current-conducting paths formed by contacting asperities increases. Note that the diode-like behavior (typically observed for contacts comprising different metallic materials) is barely seen at low V_{ds} for the relay with ITO-Au contacts since the work function of the ITO (4.1~5.5 eV depending on deposition methods/conditions [100]) would be comparable to that of Au (5.1~5.5 eV).

4.1.3. Body Biasing Effect

Figure 4.7 shows that the body bias of the prototype relay (g_o = 1 μm, g_d = 500 nm) can be used to tune the threshold V_{pi}. A change in V_b causes commensurate changes to V_{pi} and V_{rl} because the relay is actuated electrostatically, *i.e.*, driven by the absolute voltage between V_g and V_b. The hysteresis for different V_b values is approximately 1.3 V; V_{pi}–V_{rl} = 1.30 V, 1.28 V, and 1.17 V for V_b = -6 V, 0 V, and 6 V, respectively. The right pair of source and drain were biased at 0 V and 1.3·V_{pi}, respectively, and the left pair of source and drain were left floating.

Figure 4.8 shows that the body bias effect of the single-gate dual-body relays with ITO contact (a) or PEDOT:PSS contact (b), body bias can be used to tune the threshold V_{npi}. A change in V_b causes commensurate changes to V_{npi} and V_{rl} because the on- and off-states of the relay are controlled by the electrostatic actuation force, which is induced from the

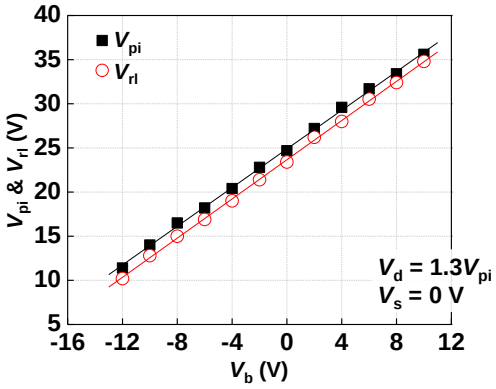


Figure 4.7 Measured V_{pi} and V_{rl} *vs.* V_b of the prototype relay (in Figure 4.1). A change in V_b results in commensurate changes to V_{pi} and V_{rl}. V_{pi}–V_{rl} = 1.30 V, 1.28 V, and 1.17 V for V_b = -6 V, 0 V, and 6 V, respectively. Hysteresis behavior ($V_{pi} \neq V_{rl}$) is due to finite F_a and pull-in mode operation. Dimensions of the relay: g_o = 1 µm, g_d = 500 nm, W = 5 µm, L = 10 µm, $W_a = L_a$ = 57 µm, and t_m = 2.27 µm.

absolute voltage between V_g and V_b. Therefore, by adjusting the body bias, the V_{npi} can be effectively reduced in order to allow for operation with smaller gate-voltage swing. Measured V_{npi} values at different V_b of PEDOT:PSS and ITO contact samples are slightly different from each other due to process-induced variations, and the measured V_{npi} values are smaller than the V_{npi} values obtained from FEA due to the slight positive strain gradient within the movable structure (SU-8/PEDOT:PSS/CYTOP) as described above. The hysteresis voltage (V_{npi}–V_{rl}) of PEDOT:PSS channel sample and ITO channel sample for different V_b values are approximately 50 mV and 100 mV, respectively. The right pair of source and drain were biased at 0 V and 1.1·V_{npi}, respectively, and the left pair of source and drain were left floating.

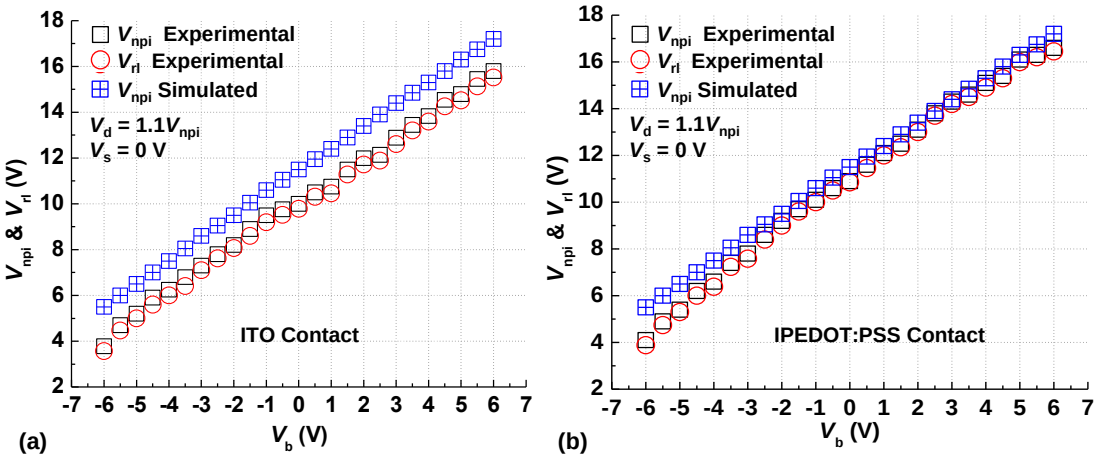


Figure 4.8 Measured V_{npi}, V_{rl} and simulated V_{npi} *vs.* V_b for the fully- and partially-polymeric single-gate dual-body relays (in Figure 4.2) with ITO contact (a) and PEDOT:PSS contact (b), respectively. Body 1 and Body 2 were tied together to form a body terminal. A change in V_b results in commensurate changes to V_{npi} and V_{rl}. Hysteresis behavior ($V_{npi} \neq V_{rl}$) is due to finite F_a. Dimensions of the relays: g_o = 700 nm, g_d = 200 nm, W = 7 μm, L = 15 μm, $W_a = L_a$ = 57 μm, and t_m = 2.46 μm.

Measured *I-V* characteristics of two dual-gate dual-body relays—one with indium tin oxide (ITO) S/D and the other with gold (Au) S/D—are shown in Figure 4.9. Zero I_{off}, abrupt transitions to the on-/off-state with an effective input swing well below 60 mV per decade change in I_{ds}, and I_{on}/I_{off} ratio above 10^7 are seen. The R_{on} and hysteresis voltage (V_{npi}–V_{rl}) are measured to be smaller (by ~84 and 35 %, respectively) for the relay with Au S/D than those for the relay with ITO S/D since the R_c and the F_a between the ITO and Au surfaces are smaller than those between the ITO and ITO surfaces (by ~85 and 47 %, respectively). The value of V_{npi} for the case where input voltages are applied to both gates (for a 'double-gate' operation) is smaller than that for the other two cases where inputs are applied to either gate (for a 'single-gate' operation) since electrostatic actuation

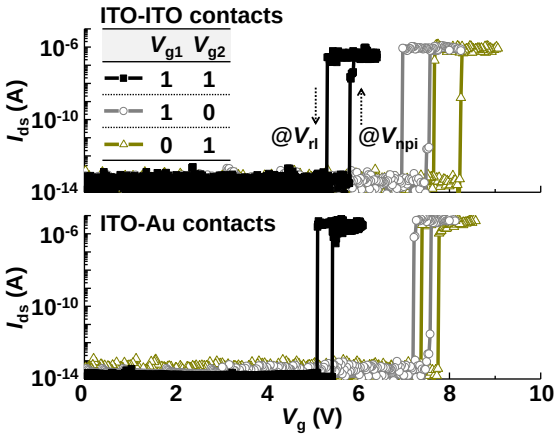


Figure 4.9 Measured I_{ds}-V_{gb} of the dual-gate dual-body relays (in Figure 4.3) for different input voltage combinations at 25 °C in air at 1 atm. '1' = V_{dd} = 1.1·V_{npi} = V_d and V_s = V_b = 0 V. V_{npi} ≅ 5.81 V and 5.43 V for the relays with ITO and Au S/D, respectively. Body 1 and Body 2 were tied together and biased to 0 V. Only one pair of S/D was used. Dimensions of the relays: g_o = 600 nm, g_d = 150 nm, W = 6 μm, L = 16 μm, W_a = L_a = 64 μm, and t_m = 1.96 μm.

depends on the overlap area (A_o) between the gate(s) and body(s) [60]. The values of V_{npi} for the single-gate operations (with input combination either [1 0] or [0 1]) are different from each other because of positive strain gradient within the movable structure, *i.e.*, g_o is narrower at the center than that at the edge by ~40 nm and ~20 nm for the relays with ITO and Au S/D, respectively.

4.1.4. Complementary Switching Behavior

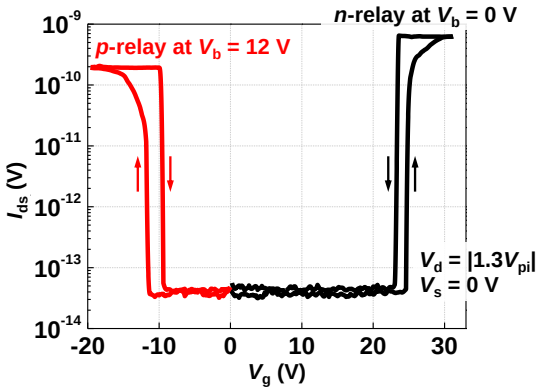


Figure 4.10 Measured I_{ds}-V_g for *p*- and *n*-type operations based on the prototype relay (in Figure 4.1) at 25 °C in air at 1 atm. Since electrostatic actuation is ambipolar, the operation of the prototype relay mimics that of an *n*-channel or a *p*-channel MOSFET. Both *n*-relay and *p*-relay are achieved by biasing the body terminal at 0 V or V_{dd}, respectively. The left pair of source/drain was left floating. Dimensions of the relay: g_o = 1 μm, g_d = 500 nm, W = 5 μm, L = 10 μm, W_a = L_a = 57 μm, and t_m = 2.27 μm.

The operation of the relay mimics that of MOS transistors due to the ambipolar nature of electrostatic actuation. Figure 4.10 shows that complementary switching behavior can be achieved by adjusting the body bias of the prototype relay. By applying 0 V or 12 V onto the body terminal, the relay can be operated like an *n*-channel or a *p*-channel MOSFET, respectively.

Figure 4.11 shows that complementary and symmetric *p*- and *n*-type operations based on the dual-gate dual-body relay can be implemented for digital logic, simply by adjusting the bias applied to the body electrodes of a relay: V_b = 3 V and 0 V for the *p*- and *n*-type

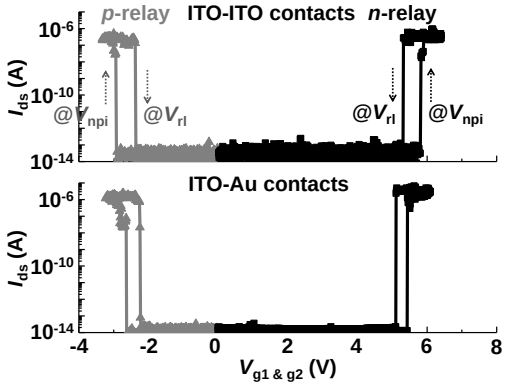


Figure 4.11 Measured I_{ds}-V_g for *p*- and *n*-type operations based on the dual-gate dual-body relays (in Figure 4.3) at 25 °C in air at 1 atm, showing symmetric operations for digital logic circuits. Gate 1 and Gate 2 were tied together to form a single node. One pair of S/D was left floating. Max $V_{g1} = V_{g2} = V_d = 1.1 \cdot V_{npi} = V_{dd}$ and $V_s = 0$ V. $V_b = 3$ V and 0 V for *p*- and *n*-relay, respectively. Dimensions of the relays: $g_o = 600$ nm, $g_d = 150$ nm, $W = 6$ μm, $L = 16$ μm, $W_a = L_a = 64$ μm, and $t_m = 1.96$ μm.

operations, respectively.

4.1.5. Hysteric Switching Behavior

Two different kinds of contact materials (PEDOT:PSS contacts and ITO contacts) were used to fabricate the single-gate dual-body relays. Both kinds of relays were designed to operate in non-pull-in mode with $g_d/g_o = 1/3.5$ because non-pull-in mode operation is better than pull-in mode operation in reducing hysteresis voltages [106]. The PEDOT:PSS-based relay exhibits a smaller hysteresis voltage (V_{npi}–$V_{rl} = 40$ mV) than the ITO-based relay (100 mV) from Figure 4.2 because of a smaller F_a. F_a is caused mainly by van der Waals interactions between two similar or dissimilar contacting surfaces. Analytically, the van der Waals force (F_v) is modeled by [61]:

Table 4.1 Hamaker constants of various materials in vacuum [107-109].

Material	Hamaker Constant ($\times 10^{-20}$ J)	Density (g/cm^3)
Au	48	19.3
W	40	19.25
ITO	15.1	7.1
PMMA	7.1	1.18
Polystyrene	6.6	1.05
PDMS	4.5	0.97

$$F_v = \frac{HA_c}{6\pi d^3} = \frac{\pi\rho_1\rho_2 C \cdot A_c}{6d^3} \tag{4-2}$$

where H is the Hamaker constant: $H = \pi^2\rho_1\rho_2 C$ [61, 107], A_c is the area between two flat contacting surfaces, d is the distance between the surfaces, ρ_1 and ρ_2 are the density of the interacting materials, and C is the particle-particle interaction coefficient. In general, polymers are less dense than inorganic materials [61]. For this reason, polymers tend to possess a lower H (particularly for polymer-polymer contacts) than metals and oxides [110-112]. Whereas H of ITO is well known (Table 4.1), H of PEDOT:PSS is not yet known; however, it can be easily inferred from H of other kinds of polymers that have a similar ρ, as $H \propto \rho_1\rho_2 C$ as shown in Equation (4-2). Assuming that C is comparable, H of PEDOT:PSS most likely lies between H of PDMS and polystyrene as ρ of PEDOT:PSS (1 g/cm^3) is between ρ of PDMS and polystyrene (Table 4.1). By extrapolation, H was extracted to be $5.3\cdot10^{-20}$ J. Because PEDOT:PSS has a smaller H than ITO, for given A_c and d, F_v (and hence F_a) between PEDOT:PSS surfaces should be smaller than that between ITO surfaces. Thus, the hysteresis voltage is smaller for the PEDOT: PSS-based relay than for the ITO-based relay. Note that the hysteresis voltage sets the lower limit for relay operating voltage (and hence operating voltage scaling) since relays require an input

voltage swing (at least) equal to the hysteresis voltage to turn on and off. The effective swing of a relay can then be defined as the hysteresis voltage needed to change I_{ds} by an order of magnitude: 12.5 and 8 mV/decade for the partially- and fully-polymeric relays (in Figure 4.2), respectively.

Figure 4.12(a) presents measured, simulated, and calculated V_{npi} values of polymeric relays as a function of L. V_{npi} decrease with increasing L as expected from Equations (2-5) and (2-10). The measured values are consistently smaller than the predicted values due to the positive strain gradient as described above. Inaccuracy in the measurements of device parameters, process-induced variations, and approximations in material properties also contribute to the difference between the measured and predicted values.

To determine F_a, measured V_{rl}^2 are plotted against V_{npi}^2 as shown in Figure 4.12(b). F_a was extracted from the y-intercept of the following Equation, which can be derived from Equations (2-6) and (2-9):

$$V_{rl}^2 = V_{npi}^2 - \frac{2F_a(g_o - g_d)^2}{\varepsilon_o A_{ov}} \tag{4-3}$$

The extracted F_a is smaller for the PEDOT:PSS contact (52 nN) than for the ITO contact (84 nN). This experimental finding is consistent with previous research [39, 106], in that F_a (caused predominantly by F_v) and hence hysteresis voltage can be made smaller when a low-surface-energy material with a lower H is employed for contacts.

Figure 4.13 plots measured hysteresis voltages of the relays as a function of V_{dd}. With

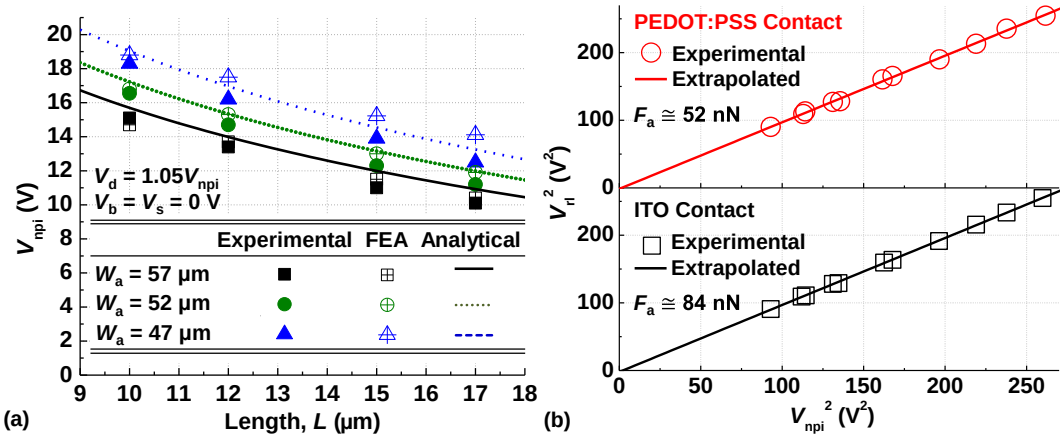


Figure 4.12 (a) Measured, simulated, and calculated V_{npi} *vs.* L of the fully- and partially-polymeric single-gate dual-body relays (in Figure 4.2). Maximum $V_g = 1.05V_{npi} = V_{dd}$. The measurement was performed at 25 °C in air at 1 atm. W = 7 μm and $W_a = L_a$. (b) V_{rl}^2 *vs.* V_{npi}^2. Each relay has four dimples: two on either side. The area of each dimple is 2.25 μm^2.

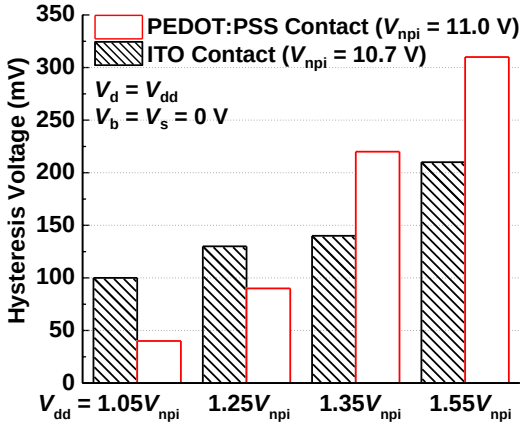


Figure 4.13 Measured hysteresis voltages of the fully- and partially-polymeric single-gate dual-body relays (in Figure 4.2) for different gate overdrive voltages at 25 °C in air at 1 atm. Max $V_g = V_{dd}$.

increasing V_{gb}–V_{npi}, the hysteresis voltage increases faster for the fully-polymeric relay than for the partially-polymeric relay. This behavior can be explained qualitatively as

follows: Since E and hardness of PEDOT:PSS are much lower than those of ITO (*i.e.*, more deformable and malleable), the total asperity contact area between the PEDOT:PSS surfaces increases faster as the load between the surfaces increases with $V_{gb}–V_{npi}$. Thus, the rate at which F_a increases at the PEDOT:PSS interface is greater than that at the ITO interface, and eventually, at $V_{dd} \geq 1.35V_{npi}$, the hysteresis voltage of the fully-polymeric relay exceeds that of the partially-polymeric relay.

The hysteresis results can be confirmed by measuring the topography and morphology of the PEDOT:PSS and ITO surfaces of polymeric relays using an atomic force microscope (AFM). Measured AFM images in Figure 4.14 show that the PEDOT:PSS surface is wavier and rougher than the ITO surface; Root-mean-square (RMS) values of surface roughness were extracted to be 2.12 nm and 0.74 nm (and peak-to-valley (PV) values < 16 nm and < 6 nm) for the PEDOT:PSS and ITO surfaces, respectively. It can be seen that, initially, PEDOT:PSS surfaces would touch at a small number of asperity points (Figure 4.14(a)), and that those asperities coming into contact would be deformed minimally when the applied load is relatively low. This corresponds with the relatively small F_a and $V_{npi}–V_{rl}$ of the fully-polymeric relay operated at $V_{dd} < 1.35V_{npi}$. It is worth noting here that the PEDOT:PSS-based relay needs ~100 mV to be turned off completely (Figure 4.2). The relatively less abrupt change in I_{ds} can be explained by Figure 4.14(a). For Figure 4.2, V_g were swept slowly with a long integration time for high-accuracy and -resolution measurement. During such a slow transition (to the off-state), some of elastically-deformed asperities (on the rough PEDOT:PSS surfaces) might be still remaining in contact with each other, thereby forming parasitic current paths and

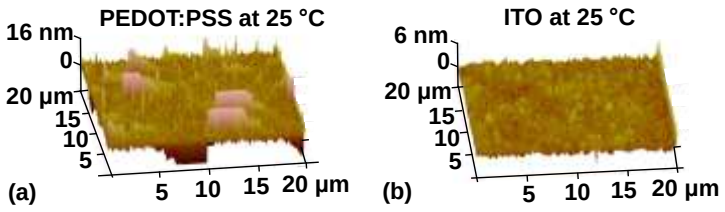


Figure 4.14 AFM images of (a) PEDOT:PSS and (b) ITO surfaces of polymeric relays measured at 25 °C in air at 1 atm. W = 7 μm, L = 15 μm, and $W_a = L_a$ = 57 μm. RMS values of surface roughness were extracted to be 2.12 nm and 0.74 nm for the PEDOT:PSS and ITO surfaces, respectively.

smoothening the abrupt change in I_{ds} as shown in Figure 4.5. Also note that F_a as well as V_{npi}–V_{rl} could be reduced further if appropriate surface coating materials and methods were employed; *e.g.*, a single or multiple anti-adhesive monolayer(s) coated by self-assembled monolayer (SAM) or atomic layer deposition (ALD) [113].

Two different kinds of contact materials (ITO-ITO and ITO-Au contacts) were used to fabricate two dual-gate dual-body relays. The F_a between the surfaces are mostly because of van der Waals interactions at the interfaces [106] and can be determined emprically by plotting V_{rl}^2 as a function of V_{npi}^2 and extrapolating the plot (Figure 4.15) to find the y-intercept (that contains F_a) [106, 114] acording to Equation (4-3), F_a are extracted to be 21 and 11 nN/μm^2 for the relays with ITO-ITO and ITO-Au contacts, respectively. The relay with ITO-Au contacts shows a smaller F_a mainly due to a lower compatibility index: $C_m \cong 0.36$ for dissimilar metallic pairs [60] that causes a lower work of adhesion, W_{ad} [115]:

$$W_{ad} = C_m \cdot (\gamma_1 + \gamma_2) \tag{4-4}$$

where $0 \le C_m \le 1$—'1' for identical materials, and γ_1 and γ_2 are the surface energies of

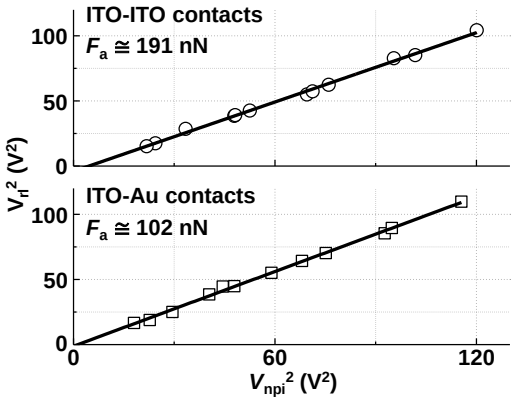


Figure 4.15 Measured and calculated V_{rl}^2 *vs.* V_{npi}^2 of the dual-gate dual-body relays (in Figure 4.3) at 25 °C in air at 1 atm in order to extract F_a for ITO-ITO and ITO-Au contacts.

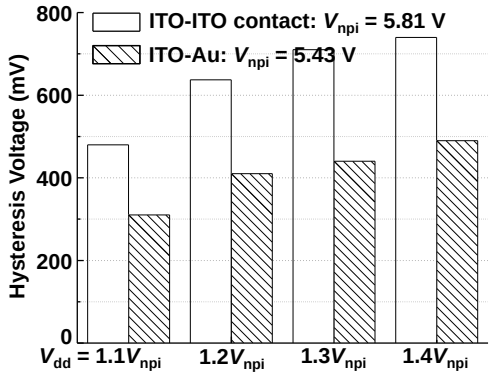


Figure 4.16 Measured hysteresis voltages of the dual-gate dual-body relays (in Figure 4.3) for various V_g–V_{npi}. Maximum $V_{g1} = V_{g2} = V_{dd}$, $V_b = V_s = 0$ V, and $V_d = V_{dd}$.

contacting materials. When two surfaces touch each other more strongly, *i.e.*, the electrostatic actuation force that brings the channel into contact with S/D is increased with increasing gate overdrive, van der Waals forces and thus hysteresis voltages (as well as F_a) of the relays increase (Figure 4.16).

4.2. Switching Delay

The measurement setup, as shown in Figure 4.17, was used to test the switching delay of single body, single gate relays with Au S/D and ITO channels. The dimensions of the relays used in the measurement are g_o = 600 nm, g_d = 150 nm, g_d/g_o = 0.26 < 1/3, W = 8 μm, and $W_a = L_a$ = 57 μm with L = 13 μm (V_{npi} = 5 V) or L = 10 μm (V_{npi} = 6.6 V). The t_{on} and t_{off} are estimated by measuring the time difference between the change in the Channel 1 of the Oscilloscope (Tektronix DPO2024B), which monitors the input signal (from a function generator, Tektronix 3252C, 2-channel 240 MHz) and the Channel 2 of the Oscilloscope, which records the voltage at the source electrode of the relay (Figure 4.17). The measured t_{on} is observed to decrease with increasing V_g due to the increasing V_g–V_{npi} and to saturate at approximately 10 μs eventually. At the same V_g, t_{on} is smaller with V_b = -2 V since the applied body bias pre actuates the suspended beam of the relay downward, which reduces the actual g_o and g_d of the relay [63]. As a result, the dimples attached to the suspended beam need to travel less distance to make contact with S/D electrodes underneath to conduct current flow I_{ds}.

To invistigate the effect of body biasing on t_{on}, a fresh relay with a shorter L (V_{npi} = 6.6 V) was tested at a constant V_g = 7 V with different body biases. Due to the effect of body biasing on pre-actuation of the relay [63], the t_{off} is observed to reduce with increasing $|V_b|$ (Fig. 4.19). The minimum t_{on} ~5.1 μs is achieved when V_b = -6 V and V_g = 7 V.

The measured t_{off} of the relay is much quicker than the t_{on} as shown in Figure 4.20. It should be noted that the measured t_{off} remains similar at various V_g and V_b. The measured

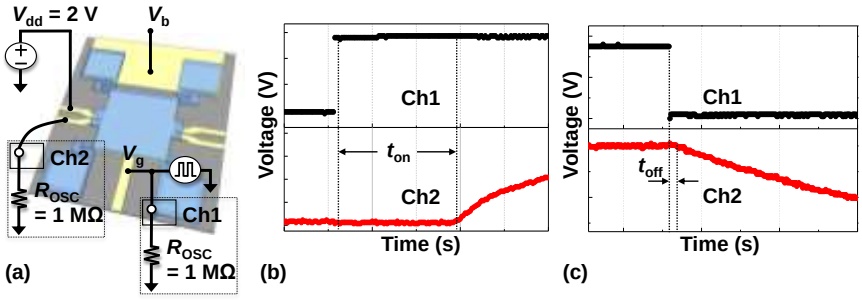


Figure 4.17 (a) Delay measurement setup of organic MEM relay. (b) The turn-on delay (t_{on}) can be extracted from the difference between the input and output signals. (c) The turn-off delay (t_{off}) can be extracted from the difference between the input and output signals. A function generator (Tektronix AFG3252C) was used to supply the input signals; a DC power supply (GW Instek GPS-4303) to set the DC biases; and an oscilloscope (Tektronix DPO2024B) to monitor and record the output signals.

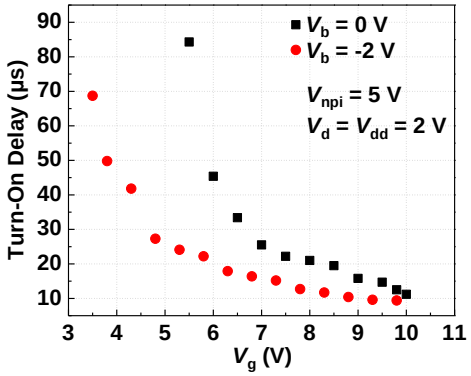


Figure 4.18 Measured t_{on} for different V_g with 0 V and -2 V body biases at 25 °C in air at 1 atm. Relay has V_{npi} = 5 V, W = 8 µm, L = 13 µm, and W_a = L_a = 57 µm. The t_{on} decreases with increasing V_g and saturates at ~9.4 µs.

t_{off} values of the polymeric relay are within the range of 1 to 10 µs. It is expected that the t_{off} is much quicker due to the fact that the suspended beam of the relay needs to travel a long distance between the dimples and respectively S/D electrodes to make a contact in order to turn on. However, the beam only needs to travel a very short distance (~2 nm) to trigger the off-state of the relay [63].

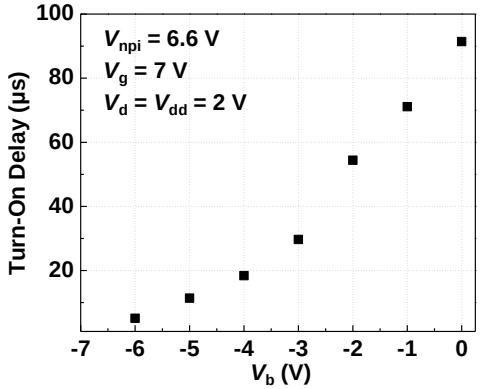


Figure 4.19 Measured t_{on} with different V_b at 25 °C in air at 1 atm. Relay has V_{npi} = 6.6 V, W = 8 μm, L = 10 μm, and W_a = L_a = 57 μm. The increasing $|V_b|$ decreases the t_{on}. The minimum t_{on} of ~5.1 μs is achieved at V_b = -6 V and V_g = 7 V.

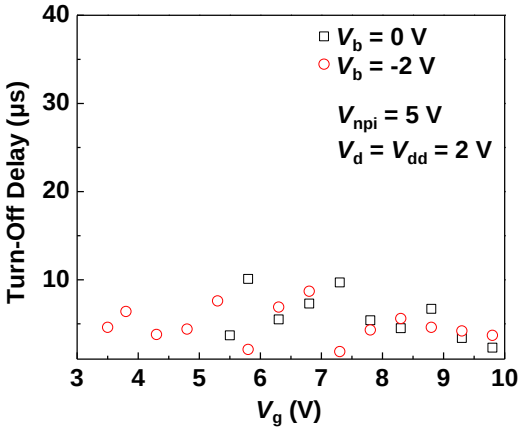


Figure 4.20 Measured t_{off} for different V_g with 0 V and -2 V body biases at 25 °C in air at 1 atm. Relay has V_{npi} = 5V, W = 8 μm, L = 13 μm, and W_a = L_a = 57 μm. The t_{off} values are within the range of 1 to 10 μs.

Note that the R_{on} (≅ 0.9 MΩ) for the polymeric relay with ITO-Au contacts is relatively high and the RC delay is estimated to be 90 ns for typical load capacitances (10~100 fF) [54]. RC delay is negligible compared with the measured t_{on} or t_{off} (~μs). Therefore, it can

be concluded that the mechanical switching delay dominates the t_{on} or t_{off} of the polymeric relays.

4.3. Switching Endurance

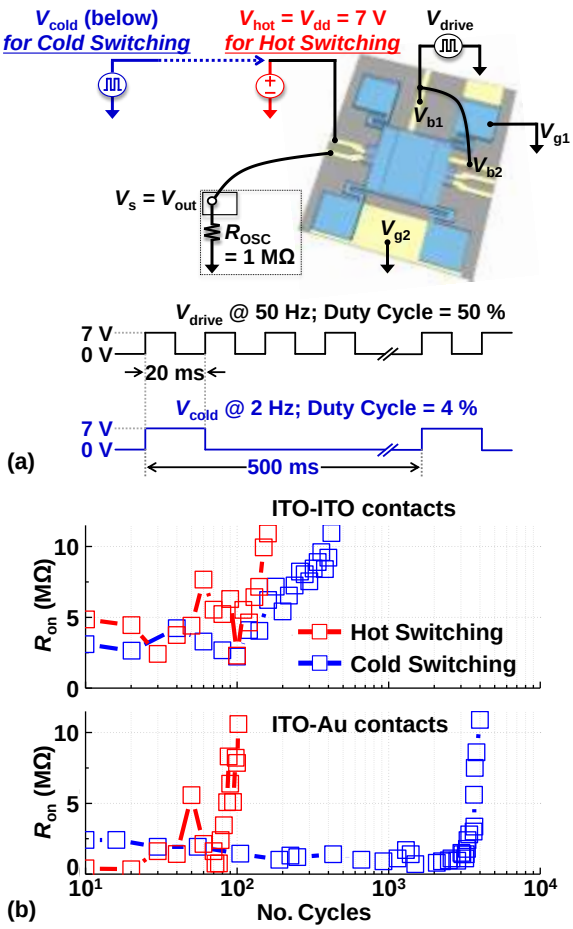


Figure 4.21 (a) Testing setup. Either DC V_{hot} or square-wave V_{cold} was applied to the drain electrode for hot or cold switching, respectively. (b) Measured R_{on} of the relays *vs.* number of hot- and cold-switching cycles. A function generator (Tektronix AFG3252C) was used to supply the input signals; a DC power supply (GW Instek GPS-4303) to set the DC biases; and an oscilloscope (Tektronix DPO2024B) to monitor and record the output signals.

Endurance of the relays with ITO-ITO contacts and ITO-Au contacts was measured

(Figure 4.21(b)) using the testing setup in Figure 4.21(a). Both relays endure a relatively small number of hot switching cycles. I_{ds} flowing between the S/D through the contacts induces local Joule heating. Contact asperities then start to deform plastically, *i.e.*, being softened and partly liquefied due to increase in temperature. This would in turn cause such damages to contact areas as pitting, hardening, or material transfer, or the deposition of organic contaminants around contact areas upon cycling, thereby causing such a sudden increase in R_{on} [60]. The relay with ITO-Au contacts endures a larger number of cold-switching cycles than that with ITO-ITO contacts, because the dissimilar contact materials result in smaller F_a and thus are less likely to induce in-use (fatigue) failures.

4.4. Effects of Temperature and Humidity on *I-V* Characteristics

Figure 4.22 shows measured V_{npi} and V_{rl} values of the fully- and partially-polymeric relays as a function of temperature. Interesting phenomena are seen: Firstly, when the relays are heated from 25 °C to 140 °C, both V_{npi} and V_{rl} are decreased by > 20 %; secondly, the hysteresis voltage of the fully-polymeric relay is increased by > 8× with increasing temperature, while that of the partially-polymeric relay remains relatively constant regardless of temperature.

The large decrease in V_{npi} and V_{rl} is mainly due to the temperature-dependent elastic modulus (E) of the polymers composing the moveable structure. It has been shown that E of SU-8 is reduced by > 5× when temperature increases to 150 °C [64]. The temperature dependence of E of PEDOT:PSS and CYTOP has not been reported; however, it is well known that E of polymers usually decrease with increasing temperature because the

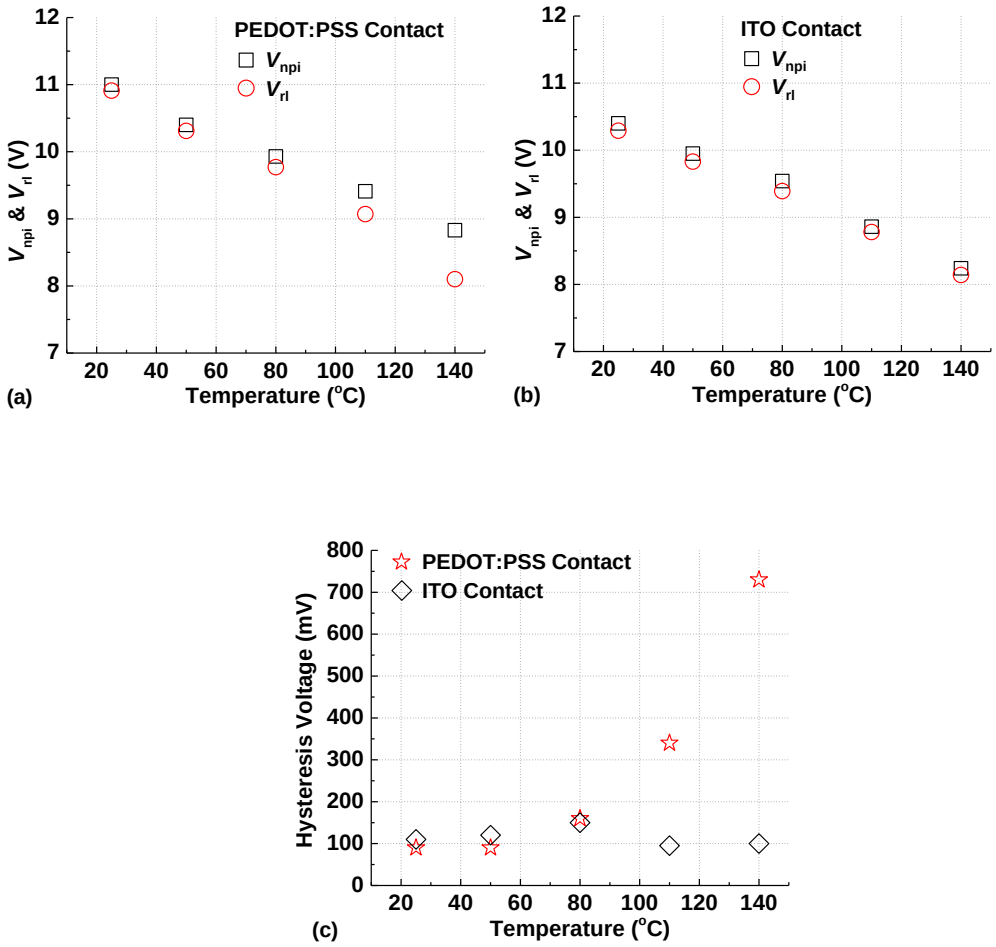


Figure 4.22 Measured V_{npi} and V_{rl} values as a function of temperature for (a) fully-polymeric (b) partially-polymeric relays (in Figure 4.2) in air at 1 atm. Bias conditions are: $V_d = 1.05V_{npi} = V_{dd}$; $V_b = V_s = 0$ V; maximum $V_g = V_{dd}$. (c) Hysteresis voltages of the relays in (a) and (b). Dimensions of the relays: g_o = 700 nm, g_d = 200 nm, W = 7 μm, L = 15 μm, $W_a = L_a$ = 57 μm, and t_m = 2.46 μm.

interatomic force that holds atoms together decreases as the bond length increases during thermal expansion [116]. Therefore, V_{npi} and V_{rl}, which are proportional to $E_{eq}^{0.5}$ as shown in Equations (2-6) and (2-9), decrease as the temperature increases (to 140 °C).

The decrease in V_{npi} and V_{rl} is partly due to different coefficients of thermal expansion

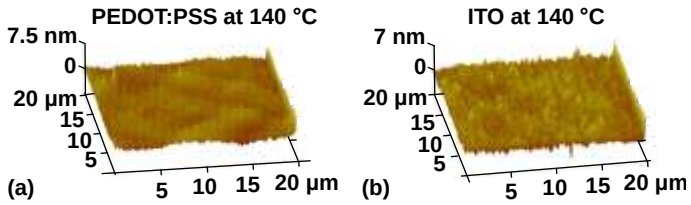


Figure 4.23 AFM images of (a) PEDOT:PSS and (b) ITO surfaces of the polymeric relays (in Figure 4.2) measured at 140 °C in air at 1 atm. RMS values of surface roughness were extracted to be 0.71 nm and 0.76 nm for the PEDOT:PSS and ITO surfaces, respectively.

(CTEs) of the polymers. Given the same thermal stress, CYTOP expands more than SU-8 since a CTE value is larger for CYTOP than for SU-8: 74 ppm/°C *vs.* 52 ppm/°C. Due to the thermally-created strain gradient, the movable structure is deflected downward for V_{gb} = 0 V. As a result, the actual g_o becomes narrower than the as-fabricated g_o, and both V_{npi} and V_{rl}, which are proportional to $g_o^{1.5}$ as shown in Equations (2-6) and (2-9), are reduced.

In order to investigate the influence of temperature on the hysteresis voltage, the topography and morphology of the PEDOT:PSS and ITO surfaces of the relays were examined using AFM at different temperatures. At 25 °C, it appears that PEDOT:PSS has a quite irregular and wrinkled surface with a RMS roughness > 2 nm and PV roughness of > 10 nm (as shown in Figure 4.14(a)). In contrast, at 140 °C, PEDOT:PSS shows an apparently much smoother and flatter surface with a RMS roughness of < 1 nm and PV roughness of well below 5 nm (Figure 4.23(a)). The substantial changes in topography and morphology of the PEDOT:PSS surface is because of the chains of covalently-bonded monomers within PEDOT:PSS, which are reoriented as the temperature

approaches the glass transition temperature (~150 °C) [92]. The large changes observed for the PEDOT:PSS contact—together with the soft, deformable and malleable nature of PEDOT:PSS, which becomes more pronounced after heating—lead to a significant increase in total asperity contact area and F_a, thereby bringing about the exponential-like increase in hysteresis voltage shown in Figure 4.22(c). It should be noted that the hysteresis voltage of the relay (with PEDOT:PSS contacts) remains relatively high (near 700 mV) once the surface of PEDOT:PSS becomes flattened out after the annealing treatment (Figure 4.22(a)). Regarding the ITO surface, no apparent changes in morphology and topography were observed before and after heating (Figures 4.14(b) and 4.23(b)). This is simply because the highest temperature used for testing (140 °C) is much less than the melting point (> 1500 °C) and typical annealing temperatures (> 200 °C) of ITO. The hysteresis voltage (as well as F_a) thus remains relatively unchanged for the temperature range shown in Figure 4.22(c).

The potential use of the all-polymer prototype relay as a biochemical sensor is demonstrated using the prototype relay. The water-absorption behavior of PEDOT:PSS was exploited to use the relay as a humidity sensor. Figure 4.24 shows measured I_{ds} of the relay over time. When the as-fabricated relay was left under ambient relative humidity (RH = 60 %), I_{ds} was decreased gradually and stabilized after six days. This is because PEDOT:PSS absorbs moisture from the ambient air until it reaches an equilibrium moisture content, as expected for typical polymers that absorb and are permeable to moisture [29], [117]. The relay was then placed in a beaker containing water (RH = 95 %) for 24 hours, to expose the hygroscopic PEDOT:PSS (that absorbs moisture very easily)

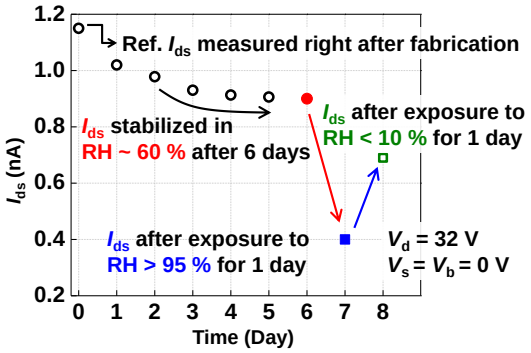


Figure 4.24 Measured I_{ds} of the prototype relay (in Figure 4.1) as a function of time at 25 °C in air at 1 atm. When the relay was placed in RH = 60 %, I_{ds} were decreased gradually and stabilized eventually; in RH = 95 %, I_{ds} was dropped dramatically; and in RH < 10 %, I_{ds} was recovered partially.

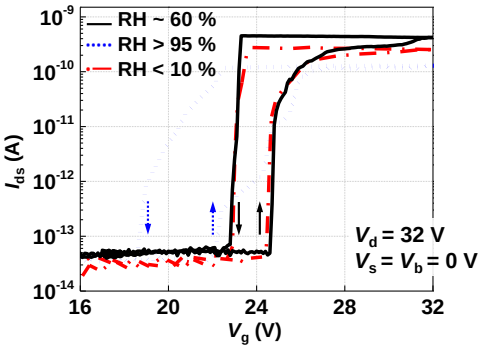


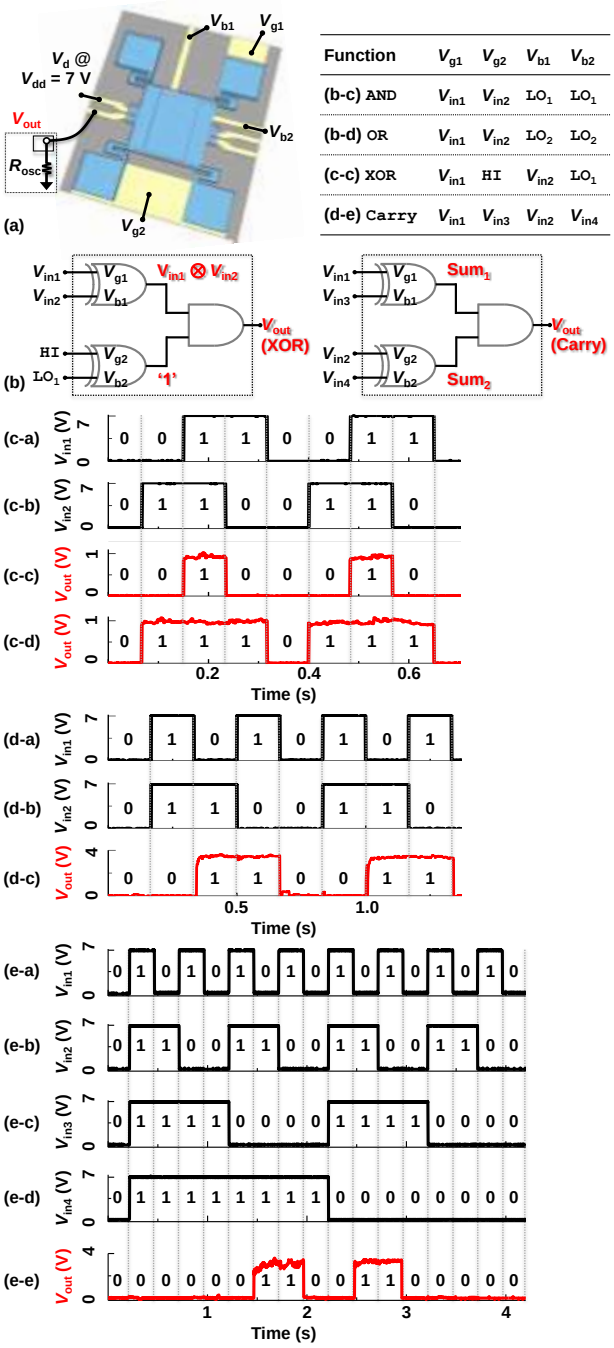
Figure 4.25 Measured I_{ds} *vs.* V_g of the prototype MEM relay (in Figure 4.1) in various RH conditions at 23 °C and 1 atm. After the relay was exposed to RH = 95 % for a day, I_{ds} and V_{pi} were lowered. These I_{ds} and V_{pi} were recovered partially and fully, respectively, after the relay was stored in RH < 10 % for a day.

to moisture-rich environments. The I_{ds} of the relay was decreased significantly (by ~55.6 %), due to phase separation between the PEDOT chains and the PSS component in the polymer mixture [117]. When the relay was placed in a desiccator (RH < 10 %) for the next 24 hours, I_{ds} was recovered to ~76.7 % of its original value (measured in Day 6 in Figure 4.20).

Figure 4.25 shows measured I_{ds} *vs.* V_g characteristics of the relay under different RH conditions. When the relay was exposed to RH = 95 % for one day (after being stored in RH = 60 % for six days), the threshold V_{pi} of the relay was dropped by ~10.6 % because the folded-flexures of the movable stack absorb moisture and become mechanically more compliant (lower effective spring constant). After the relay was stored in a desiccator (RH < 10 %) for another day, V_{pi} was recovered to ~99 % of the previous value (measured in RH = 60 %). These changes in I_{ds} and V_{pi} shown in Figure 4.25 indicate changes in humidity levels. The relay sensor can be post-fabricated using the low-thermal-budget process on top of CMOS readout circuits or integrated with relay-based readout circuits.

4.5. Relay for Logic-Gate and Carry-Generate Functions

A single dual-gate dual-body relay can easily achieve basic logic and carry generate functions. For the measurements, a function generator (Tektronix AFG3252C) was used to supply the input signals; a DC power supply (GW Instek GPS-4303) to set the DC biases; and an oscilloscope (Tektronix DPO2024B) to monitor and record the output signals. Measured logic waveforms (Figure 4.26(c)) using the bias configuration (Figure 4.26(a)) confirm that a relay can perform either two-input AND or OR operations when the bias applied to its body electrodes (tied together to form a single node) is adjusted properly—to 0 V and -2 V for AND and OR, respectively. The maximum value of the output voltage ($V_{out} \cong 1$ V) measured at the source electrode is lower than the V_{dd} applied



Function	V_{g1}	V_{g2}	V_{b1}	V_{b2}
(b-c) AND	V_{in1}	V_{in2}	LO_1	LO_1
(b-d) OR	V_{in1}	V_{in2}	LO_2	LO_2
(c-c) XOR	V_{in1}	HI	V_{in2}	LO_1
(d-e) Carry	V_{in1}	V_{in3}	V_{in2}	V_{in4}

Figure 4.26 (a) Bias configuration. LO_1 = 0 V, LO_2 = -2 V, and HI = V_{dd} = 7 V. (b) Symbolic representation for XOR and carry generate functions. (c) Measured logic waveforms: (c-a) input 1 signal; (c-b) input 2 signal; (c-c) AND output signal; and (c-d) OR output signal. (d) Measured logic waveforms: (d-a) input 1 signal; (d-b) input 2 signal; and (d-c) XOR output signal. (e) Measured timing diagrams: (e-a) input 1 signal; (e-b) input 2 signal; (e-c) input 3 signal; (e-d) input 4 signal; and (e-e) carry bit output signal.

to its drain electrode ($V_d = V_{dd} = 1.1 \cdot V_{npi} \cong 7$ V), due to the voltage divider formed by the contact resistance between the ITO channel and ITO S/D (≅ 5.6 MΩ) and the input impedance (1 MΩ) of the oscilloscope (Tektronix DPO2024). The output voltages are observed to be somewhat unstable since the number of deformable nanometer-scale asperities on the channel and S/D surfaces (that come in contact with each other to form conductive paths) would change slightly over time. Measured timing diagrams in Figure 4.26(d) using the biasing scheme in Figures 4.26(a) and (b) demonstrates an XOR function. For this experiment, a fabricated relay with ITO channels and Au S/D was used instead. Since the resistance of the ITO-Au contacts (≅ 0.9 MΩ) is smaller, the maximum output voltage ($V_{out} \cong 4$ V) is measured to be greater than that for the relay with pure ITO contacts (Figure 4.26(c)).

5. Conclusions

In order to enable efficient implementation of portable and/or wearable large-area electronics for the internet of things requiring ultralow-power operation, structural flexibility, visual transparency, and low-cost/-temperature processing, organic microelectromechanical (MEM) relays technology that can provide for zero static power consumption, very low dynamic power consumption, and complementary switching operations is investigated.

In this dissertation, prototype and multiple-input/-output organic MEM relay design, the development of reliable polymer-based low-thermal-budget surface-micromachining process, which led to the successful characterizations of organic MEM relay were discussed. The energy-efficient operation of the organic MEM relay as a switching device, body biasing and complementary switching, the hysteresis voltages improvement by contact materials engineering, the switching delay, the hot- and cold-switching endurance are characterized, the effect of temperature and humidity on the behaviors of the organic MEM relay are investigated. In addition, relay-based logic gates and carry-generate functions are demonstrated.

In Chapter 2, the designing of the prototype organic relay is demonstrated, the refined single-gate dual-body relay that is designed in non-pull-mode operation mode is discussed with inter-digitized body electrode that enables the independently control of each body electrodes to adjust the actuation. A versatile relay design, dual-gate dual-body relay with inter-digitization of the gate and body is presented to enable logic-gates and

carry-generate functions.

In Chapter 3, it was shown that a low-thermal-budget (≤ 150°C) surface-micromachining process based on conductive polymer and nonconductive polymers is developed to implement organic relays on flexible substrates. The challenges, requirements, selections, solutions of each material layers are presented.

In Chapter 4, it was shown that the fabricated organic MEM relays exhibit unique *I-V* characteristics including immeasurably-low off-state leakage current, abrupt on-/off-state transition with an input voltage swing less than 60 mV for a decade change in output current, a relatively high on/off current ratio well above 10^5, and complementary switching behavior. The fabricated organic MEM relays endure a finite number of hot- and cold-switching cycles. In addition, the effects of temperature, humidity and low-surface-energy contacting electrode materials on switching characteristics (such as hysteresis voltages and on-state resistance) are demonstrated. A versatile dual-gate, dual body organic MEM relay that can generate a carry for four input bits and perform basic Boolean operations for two input bits is demonstrated.

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