WIRELESS ELECTRICAL STIMULATORS FOR NANOFIBERS WITH APPLICATION IN NEXT GENERATION MUSCLE PROSTHESIS

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ABSTRACT OF THE DISSERTATION

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Dissertation Director: Professor Laleh Najafizadeh

Functional loss and impairment of skeletal muscle could occur as a result of a diverse range of causes including trauma, aging, and diseases such as amyotrophic lateral sclerosis, negatively impacting the lives of more than 2 million people in the United States. Existing solutions for the repair and regeneration of skeletal muscle display contractility only "after" new muscle has been regenerated, which is typically a lengthy process. Such limitations highlight the need for the development of new technologies that can provide function and regeneration of lost tissue in a timely manner. A possible solution to enable patients with immediate function as new tissue regenerates is the development of new classes of subcutaneous muscle prosthesis, which are envisioned to be made by combining biomaterials such as ionic electroactive polymers (iEAPs) with their implantable controllable electrical stimulators. Towards this goal, the work presented here proposes novel circuit-level and system-level solutions for the design and realization of wirelessly tunable electrical stimulators for iEAPs.

The first part of this dissertation focuses on the problem of implementing precise reference circuits that will be required in stimulators. Three novel design solutions are presented. First, a BiCMOS-based curvature compensation technique, which can be realized in any BiCMOS/CMOS technology, is proposed to completely cancel the nonlinear temperature dependent terms of the base-emitter junction voltage in bandgap reference voltage circuits. Second, a

new design solution based on the bandgap voltage difference of Si and SiGe $p-n$ junctions is proposed to significantly improve the accuracy of SiGe-based reference circuits. For both proposed solutions, theoretical derivations are presented, and circuits are designed, fabricated, and experimentally characterized. Finally, a multi-piecewise solution is presented which results in references with maximum stability.

The second part of the dissertation focuses on the design of the tunable stimulators and their integration with iEAPs. The unique characteristics of iEAPs impose several design challenges for the stimulator. These challenges are identified, and solutions are proposed. The electrical stimulation is proposed to be provided using a tunable external capacitor-less low dropout regulator (LDO). To enable remote tuning, the frequency at the primary side is utilized to wirelessly adjust the magnitude of the voltage from the LDO, and hence, the electric field generated at the secondary side (implant). Furthermore, a system-level solution is presented to remotely control the polarity of the electric field as well as its magnitude, enabling iEAPs with a wide range of movement possibilities. The performance of the proposed stimulator in generating reliable output is extensively evaluated experimentally under various conditions, including coil misalignment. The stimulator is integrated with iEAP samples, and the functionality of the end-to-end module is examined based on the response and the movement characteristics of iEAPs in a series of *in vitro* experiments. Results demonstrate the feasibility of using the proposed system as a reliable tunable electrical stimulator for iEAPs.

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Chapter 1

Introduction

The skeletal muscle is responsible for the maintenance of posture and voluntary body movements [1]. When the skeletal muscle suffers from the minor injury, it can regenerate rapidly to avoid the loss of muscle mass [2]. However, regarding the large volume injuries, aging or the illness (such as amyotrophic lateral sclerosis, vascular disease or cancer), the skeletal muscle is incapable of fully restoring function via its regeneration process [3, 4]. In the healing process of the large volume injuries, the injury site is occupied by the scar tissue, and thus the satellite cells are not capable of filling the voids around the damaged area [5, 6]. As a result, the function of the muscle is degraded and the patients' quality of life is negatively impacted due to the occurrence of functional loss and impairment of skeletal muscle.

Nowadays, the standard treatment for large volume deficiencies in skeletal muscle is the tissue's autologous transplantation from the donor [7]. Although this approach is effective on the reanimation of the elbow and forearm [8, 9], its limited success for larger defects in muscles cannot be denied [10]. In addition, by using autologous transplantation, the donor site morbidity can also increase the risk of infection during the surgery [11]. Therefore, a better treatment is highly demanded to bypass the issues brought from the autologous transplantation.

In the field of tissue engineering [12], several approaches have been investigated for the repair and regeneration of skeletal muscle. A general tissue engineering paradigm includes taking the muscle progenitor cell, seeding them on the 3-D scaffold, applying stimulation to achieve the cell differentiation and eventually constructing the tissue to implant into the patients [13]. A constructed tissue is considered as a functional skeletal muscle replacement only if it is capable of reproducing the contractile stress of native skeletal muscle. In the past few years, several approaches, such as intramuscular injections of skeletal myoblasts [10], have been sought to aid in the regeneration of deteriorated tissue [14–17]. However, there still exist

problems with producing artificial muscles that contract and relax similar to real muscles and also display immediate contractility upon being implanted. One possible solution to the problems of flexibility and immediate movement restoration is the development of new classes of subcutaneous muscle prosthesis, which combine ionic electroactive polymers (iEAPs) [18, 19] with integrated circuits as their simulators. In addition to creating movement, such a prosthesis will also speed up the tissue regeneration process by enhancing cellular proliferation alignment via stimulation upon implantation.

The successful implementation and operation of such a system will strongly rely on the implantable microelectronic devices, which have been receiving increased attention in recent years because of their great potential in offering solutions to problems in various clinical applications [20, 21]. To develop this iEAP-based subcutaneous muscle prosthesis, several design challenges need to be overcome. The essential requirements for the implantable electronic devices are the compact size and low power consumption. In addition, ideally, all the devices in the implant unit need to be powered-up wirelessly instead of relying on a local battery. Furthermore, reliable function in biological medium needs to be provided by this system.

1.1 Motivation

To provide the electrical stimulation to iEAPs for the new classes of muscle prosthesis, novel solutions for the development of responsible integrated circuits and wireless control technique are required. The work presented here is motivated by this demand, and proposes innovative solutions at the circuit and system levels.

The first part of the dissertation focuses on the development of novel high-performance reference circuits, following a "device-circuit interaction" design approach. High precision reference circuits are needed in implantable stimulators and virtually all electronic systems. A key requirement of reference circuits is to generate a robust voltage that is invariant against variations in environmental and operating conditions. Any variations in the reference voltage will directly affect the performance of the overall system. The most commonly used topology for the realization of reference circuits is the bandgap reference (BGR) [22]. A BGR is designed to generate an output voltage that is referred to the bandgap energy of the background

semiconductor material. In Si-based BGR circuits, the relation to the bandgap energy can be established through the base-emitter voltage (V_{BE}). However, V_{BE} also depends to the temperature (T) linearly ($\propto T$) and nonlinearly ($\propto [T\ln(T)]$) . Traditionally, a proportional to the absolute temperature (PTAT) component is created to cancel the linear-dependent term of V_{BE}, known as the complementary to the absolute temperature (CTAT) term [22]. The major problem with this approach is that the output of BGRs will still be dependent on the temperature (due to the existence of $\propto [T\ln(T)]$ terms), limiting their level of precision. In Chapter 3, three novel BGR topologies with new curvature compensation techniques are proposed, which advance the state-of-the-art BGRs.

The second part of the dissertation concentrates on the system level solutions for the realization of implantable stimulators. The work in Chapter 4, proposes to provide the electrical stimulation to iEAPs via a wirelessly tunable voltage regulator. This system is capable of remotely controlling the degree and the direction of their movement. Without using digital modulation schemes, the proposed stimulator uses frequency at the primary side, to wirelessly tune the magnitude and the polarity of the electric field generated at the secondary side, enabling iEAPs with a wide range of movement possibilities.

1.2 Contribution of this Research

Driven by the demand for the next generation muscle prosthesis, this dissertation presents innovative circuit and system level solutions for the realization of implantable stimulators for iEAPs.

1.2.1 Circuit-level Contributions

The electrical stimulation to the iEAPs needs to be provided by a voltage regulator, such as the low drop-out regulator (LDO). Ideally, a wireless tunable LDO with a stable voltage reference is required.

In Chapter 3, three different curvature compensation techniques are proposed to improve the accuracy of the BGR circuits. Section 3.4 presents a BiCMOS compensation approach combining the temperature properties of SiGe heterojunction bipolar transistors (HBTs) and CMOS

transistors. This proposed compensation approach has been experimentally demonstrated to outperform the temperature performance of the state-of-the-art SiGe reference circuits. This work is published in [23] and [24].

Section 3.5 presents a novel curvature-compensation technique for bandgap reference circuits implemented in the SiGe BiCMOS technology. The technique utilizes the designers' access to both Si-based and SiGe-based $p-n$ junctions. Curvature compensation is achieved in two steps: first, by weighted subtraction of two currents, one proportional to the base-emitter junction of a Si BJT, and the other proportional to that of SiGe HBTs, the non-linear temperature dependent terms are compensated; and second, by adding a PTAT current, the remaining linear temperature dependent terms are canceled. As a result, an almost complete temperature compensation is achieved. This work is published in [25] and [26].

In Section 3.6, a systematic design methodology utilizing a piecewise curvature correction technique to improve the temperature coefficient (TC) of BGRs is presented. It is shown that the temperature dependency of the drain current of a MOSFET transistor depends on the transistor's operating region. Using this property, a multi-piecewise compensation technique over a wide temperature range is achieved by controlling the operating region of MOSFETs through their gate-source voltages. This work is published in [27].

In Section 4.4, an LDO for the electrical stimulation of iEAPs is presented. The challenges brought from the special requirement of the application and the characteristics of iEAPs are discussed, and the circuit level solutions are provided. The proposed LDO uses the external-capacitor-less architecture to enable a fully on-chip solution for providing stable stimulation across a wide load range, as required by the properties of iEAPs. The LDO also offers precise line and load regulations, as well as improved power supply rejection (PSR) to suppress the supply noise when the LDO is powered up through wireless power transfer (WPT) links. This work is published in [28].

In Section 4.5, a design technique to implement wirelessly tunable LDO is introduced. The proposed technique, built upon the concept of frequency-based telemetry, converts the frequency of the sinusoidal signal at the primary side into an electrical current at the secondary side that will be proportional to the input frequency. This current is then used to change the reference level of the LDO and therefore, its output voltage. The proposed technique provides the

capability to tune the output of LDO remotely, and thus LDO can be used as a reliable stimulator for iEAPs to allow different degrees of movement for the subcutaneous muscle prosthesis. This work is published in [29].

1.2.2 System-level Contributions

In Section 4.3, the functionality of electrically stimulated iEAPs is evaluated under steady-state and transient conditions. An LDO is used to provide the electrical stimulation to the iEAPs, and *in vitro* characterization results are presented and discussed. Electrical characteristics of iEAPs in terms of conductance, and movement characteristics of iEAPs in terms of changes in the bending angle during xed and transient stimulation are evaluated. Measured results suggest that iEAPs in combination with LDO-based stimulator have great potentials for the realization of the next generation muscle prosthesis. This work is published in [30].

In Section 4.6, the proposed stimulator is implemented using custom-off-the-shelf components. This section presents a new system-level solution for the realization of a tunable electrical stimulator for iEAPs, capable of remotely controlling the degree and the direction of their movement using one control coil. The performance of the stimulator in generating reliable output is extensively evaluated under various conditions, including coil misalignment. In addition, the functionality of the end-to-end module is examined based on the response and the movement characteristics of iEAPs in a series of *in vitro* experiments. Movement characteristics of iEAPs in terms of changes in the bending angle during fixed and transient stimulation are evaluated. Measured results demonstrate the feasibility of using the proposed system as a reliable tunable electrical stimulator for iEAPs. Moreover, the combination of iEAPs and the proposed stimulator has great potentials for the realization of the next generation muscle prosthesis that is flexible, and can enable immediate movement restoration, upon implantation. This work is published in [31, 32].

1.3 Thesis Outline

The dissertation is organized as followings. In Chapter 2, a review of the previous works on implantable stimulators is presented. The design criteria, challenges, various applications and the

state-of-the-art works on implantable stimulators are surveyed. In Chapter 3, we propose three novel curvature compensated techniques in designing the BGR circuits. In Chapter 4, the system design requirements and challenges in the development of this iEAP-based subcutaneous muscle prosthesis are analyzed. Without using digital modulation schemes, a frequency-based design technique is proposed to wirelessly tune the magnitude and the polarity of the electric field generated at the secondary side, enabling iEAPs with a wide range of movement possibilities. Finally, Chapter 5 contains conclusions and potential research directions.

Chapter 2

Implantable Stimulators

As discussed in Chapter 1, an implantable stimulator can be implemented for the iEAP-based subcutaneous muscle prosthesis. In order to implement an effective system for the subcutaneous muscle prosthesis, we will review prior works on implantable stimulators that are realized in modern electronic technology platforms. In this chapter, the background information on implantable devices will be reviewed first. Next, the system specifications, design requirements and challenges of implantable stimulators will be studied. Finally, the design techniques and considerations are reviewed to meet the design challenges, along with a review of the system level implementation of the state-of-the-art implantable stimulators.

2.1 Background

Implantable devices are artificial medical instruments that can be inserted subcutaneously into a patient's body and either act as the replacement for the missing biologic structure or augment the patients' body parts [33]. In 1958, the first implantable device was reported when a cardiac pacemaker was successfully implanted in an animal [34]. After which, implantable devices have been extended to various clinic domains, such as the cochlear implants [35], vagus nerve stimulator [36], drug delivery systems [37] and defibrillator [38]. In the past few decades, the development of microelectronics-based medical implants has gone through revolutionary progress due to the advances in modern electronic devices and integrated circuits.

Electrical stimulators are examples of implantable devices, which are designed to provide low-level voltage/currents to excite nerve cells or muscle fibers via electrodes. As shown in Fig. 2.1, examples for application of implantable stimulators are categorized into four areas from the perspective of the dysfunctional body organs that need replacement or augmentation. Figs. 2.1-a, 2.1-b and 2.1-c illustrate the applications of visual neural stimulators (retinal prosthesis)

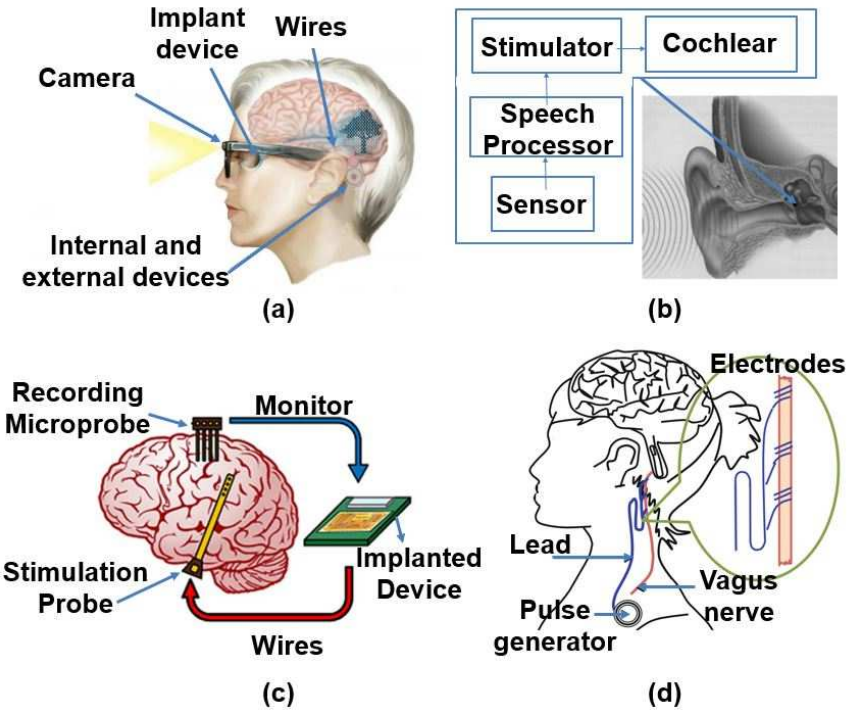


Figure 2.1: Examples for application of implantable stimulators: a) retinal prosthesis (after [45]), b) cochlear implant (after [48]), c) deep brain stimulator (after [52]), and d) vagus nerve stimulator (after [70])

[39–45], auditory neural stimulators (cochlear implants) [46–48], and deep brains stimulator [49–53], respectively. In addition to these three categories, various neuro stimulators have also been designed for epidural spinal cord [54], the vagus nerve [36, 55, 56], neuromuscular unit [57–59], diaphragmatic/phrenic nerve [60] and sacral nerve [61]. In Fig. 2.1-d, a vagus nerve stimulator is shown as the example of these neuro stimulators.

Due to the similarity between the electrical stimuli and natural biological stimuli, the cells' transmembrane potential [62] can be changed under electrical stimulation. Electrical stimulators can bring various benefits to the patients, depending on the applications. For instance, the stimulation provided from the retinal prosthesis can partially recover the lost perception of vision [63–68], while a vagus nerve stimulator can reduce the frequency of seizures in the patients with refractory epilepsy [69]. To maximize the benefit from these electrical stimulators, they must be designed carefully based on a thorough understanding of the design requirement and challenges.

2.2 Design Requirements and Challenges

The architecture of typical implantable stimulators can be separated into two units: the external unit and the implant [33]. The external unit usually includes the power transfer unit, and/or user interface to send the control command or the real-time monitoring telemetry. The implant usually includes the power unit (such as the secondary power coil in a wireless power transfer system, or the battery) and the signal conditioning circuits to generate the stimulation pattern. To understand the system architecture of implantable stimulators, it is important to study the design requirements and challenges. The analysis of these metrics will provide further insight into the system design.

2.2.1 System Design Requirements

The main system design requirements for implantable stimulators are related to the safety constrains, such as the size and the power consumption and power density of the implant unit.

2.2.1.1 Size

One essential requirement for the implantable devices is its overall size. The implantable stimulators' size must be compact to be implanted into the human body. For the applications with multiple electrodes (such as retinal prothesis), the size of implantable stimulators is further constrained to allow for integration with the implanted electrode arrays [71]. For typical implantable stimulators, the off-chip components can be the inductive coils [59] or off-chip antenna [72], the capacitors to tune coils to resonance [59], the capacitors in the charge mode stimulation circuits [73], the blocking capacitors for charge balancing purpose [74], and the energy storage capacitors to aid in power supply regulation [59]. Due to the space limitation in the implant, these discrete components are highly restricted [75] and must be carefully considered in the design iterations.

2.2.1.2 Power Source and Power Dissipation

Optimizing the technique for delivering enough power to implantable devices has been investigated in several works [76, 77]. The conventional implementation of the implantable devices

Table 2.1: Comparison of three types of wireless power transfer techniques (after [70])

	Inductive coupling	Resonance coupling	Radio charging
Mechanism for power transfer process	Magnetic induction	Resonance-enhanced magnetic induction	Received radio waves
Coupling components & circuits	Inductive coil	Resonant LC tuned circuit	Resonant LC tuned circuit
Frequency range	Sub RF or lower frequencies in the RF band	Sub RF or lower frequencies in the RF band	RF band
Efficiency	Medium	Highest	Least
Near/Far field transmission	Near-filed	Near-filed	Far-filed
Typical power transfer distance	5 to 7 mm	7 to 40 mm	2 to 10m
Spatial freedom	Less	More	Largest
Target location of the implants	Shallow	Shallow/deeper	Shallow/deeper
Create electromagnetic pollution?	No	No	Yes

relies on a battery in the implant unit or the power source provided percutaneously from the external unit via the tethering cable [78]. Although using battery or the power source from the external unit features several advantages (such as efficient power transmission), both the battery replacement (due to the size, limited storage capacity and the number of recharge cycles [79]) and the power sourcing via the tethering wire increase the likelihood of different kinds of injuries, hemorrhage, and infection [33]. Thereafter, the WPT approach is more favorable in most of the modern implantable devices. In a WPT system, the power is transferred from the external unit to the implant in a contactless manner, which offers an attractive power delivery solution for implantable devices by limiting the need for battery replacement or percutaneous leads.

In general, WPT technique can be categorized into near field, mid filed and far filed power transfer, based on the distance of the power transfer [76]. For biomedical applications, there are mainly three types of the wireless transfer techniques: the inductive coupling, the resonance coupling and the radio charging [70]. The first two approaches belong to near field power transfer category with a similar operation: the inductive coupling is based on magnetic induction, while the resonance coupling relies on resonance-enhanced magnetic coupling [80]. The radio charging method is one of the far field techniques, which employs the received radio-frequency (RF) waves via the antenna to serve as the power source. These RF waves usually locate at a much higher band than the frequency spectrum used in the inductive coupling and the resonance coupling. A brief comparison of these three power transfer techniques is shown in Table 2.1 [70].

The choice of the wireless power transfer techniques is based on the requirements of the

application. However, when using any of the wireless power transfer systems, the main challenge for the designers is the power transfer efficiency (PTE) [81], which is influenced by the distance of the coils, the energy transfer rate and the coupling coefficients between the coils. In addition, the power dissipation of the implantable devices is also of concern due to the heat density requirements of the human body. When allocating the power budget of the implantable system, it is important to investigate the amount of heat it will dissipate to the surrounding tissue to avoid the possibility of destroying the cells [33].

The PTE and power dissipation concerns become more important when the frequency locates in RF band. The RF waves can cause the thermal losses when it heats the tissues, which degrades the PTE and raised the possibility of the cell death [70].

2.2.2 Stimulation Requirements

Many implantable stimulators are required to provide precise, reproducible voltage or current stimulation for the target sites. The font-end circuits in the stimulator provide the selection command in activating the target channels, while a unique shape and firing pattern are created for each electrode [62]. Here we will review the stimulation requirements and the design challenges.

2.2.2.1 Stimulation Channels and Sites

Conventional implants include the single-channel type and multi-channel type. Single-channel implants produce the stimulation at a single site using a single electrode, while the multi-channel implants provide the electrical stimulation at different sites using an array of electrodes [82]. For general applications, the number of the channels is related to the control and coverage of the neural tissue when the tissue interfaces with the electrodes [69]. For some specific cases, such as retinal prosthesis, hundreds of the electrodes are unavoidable to bring the useful pixelated image to the patients [83–85]. This requirement hence raises the challenges for the size of the implant unit and calls for novel techniques in reducing the overall size brought from the multi-channel designs. One solution is the multiplexed CMOS stimulating probe [86, 87], in which one channel is associated with one multi-site probe. The probe itself includes the power, clock, command recovery and data control units, while each electrode in the probe is

connected to one stimulation site. For these sites, each of them must own the capability to be enabled/disabled, as well as be programmed with different stimulation parameters. To achieve this, several local building block circuits are designed in each site, such as the local finite state machine, recovery circuit, amplitude and timing registers, counters and the current driver [62]. The number of the stimulation sites depend on the application. For example, in [87], a 64-site system is designed for stimulating the central nervous system. Likewise, in [88], the multisite system is designed for cortical stimulation.

2.2.2.2 Stimulation Patterns

Conventionally, three types of stimulation modes have been used to generate the target stimulation signal, including the current mode stimulation (or current-controlled stimulation, CCS) [40–42, 89–91], the voltage mode stimulation (or voltage-controlled stimulation (VCS)) [92–96], and charge mode stimulation (or charge-controlled stimulation (ChCS)) [73,97,98]. In Fig. 2.2, the typical block diagram of all these three modes are depicted [70]. In each of them, the voltage signal generated from the microprocessor is passed to the digital to analog converter (DAC) [99]. Then for CCS, the output of the DAC feeds into a voltage to current converter (VIC) to produce the current stimulation signal to the tissue. The implementation of the VCS and ChCS are different from that of CCS. For VCS, an amplifier is connected in the signal path to generate the stimulation voltage signal, while an amplifier, a DC-DC converter, the charging circuit and the capacitor bank constitute the charge mode stimulation circuits.

The selection of the proper charging mode among the three candidates in Fig. 2.2 depends on the application requirements and the available size of the stimulator. For example, ChCS will be preferred when multiple off-chip capacitors are allowed in the design, due to its simple implementation and excellent safety performance [100].

By using any of the charging modes mentioned above, the designed stimulation waveforms can be either monophasic or biphasic [101]. The monophasic wave only consists of one kind of pulses in a unidirectional manner. In biphasic waveforms, a sequence of pulses shows up, while the adjoining pulses have opposite directions. The choice of the stimulation waveform is related to the charge balancing requirements inside the human body. When the electrical stimulation takes place, electrical charges are transferred to the tissue. The long period of

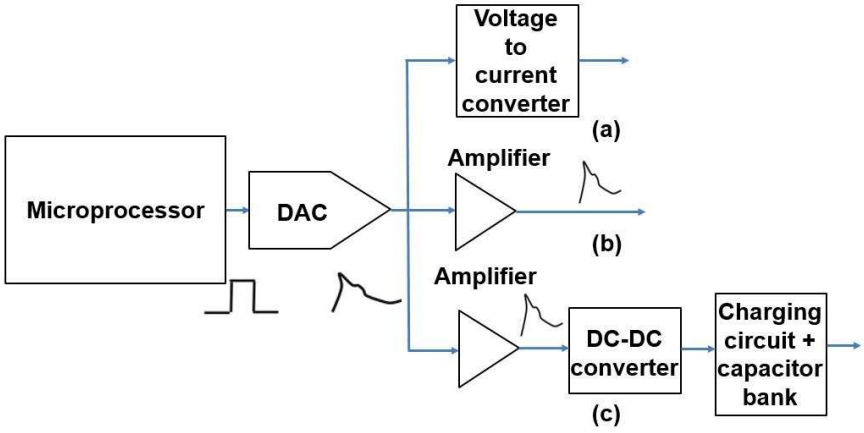


Figure 2.2: Three types of stimulation modes: a) current mode, b) voltage mode, and c) charge mode (after [70])

charge exchange will likely initiate the electrochemical processes inside the human body, such as the electrolysis. These processes are destructive to the tissues and cells, and thus need to be avoided. To prevent the onset of these issues, the net charge must be nulled in each stimulation cycle [102]. In the clinic, the suggested stimulation pattern is the biphasic current, in which the theoretical full charge balance can be ensured [103]. However, in practice both monophasic and biphasic waveforms can cause charge unbalance due to the device mismatches during the IC fabrication. Therefore, the charge balance requirements also impose the challenges of the stimulator design.

In addition to the charging mode and stimulation waveform, the precise control of the pattern specifications is also critical for an effective stimulation. For example, for a stimulation current, the pattern specifications include the current amplitude, the pulse width range, the fine gradients of the stimulation strength, and the repetition rates of the pulses [62, 104]. First, the pulse amplitude matters in most of the applications. For instance, in the cochlear device, the auditory percept can only be elicited with a minimum 1 mA pulse amplitude [47]. Moreover, a large amplitude resolution offers the adjustment flexibility in the stimulation driver, such as the creation of different brightness levels for the patients using retinal prosthesis [105]. Last but not least, the stimulation frequency is directly related to the outcome of the stimulation, such as the frame rate of the retinal prosthesis [43]. To achieve such a stimulation pattern, the stimulation driver must be capable of providing robust wireless programmability with high flexibility.

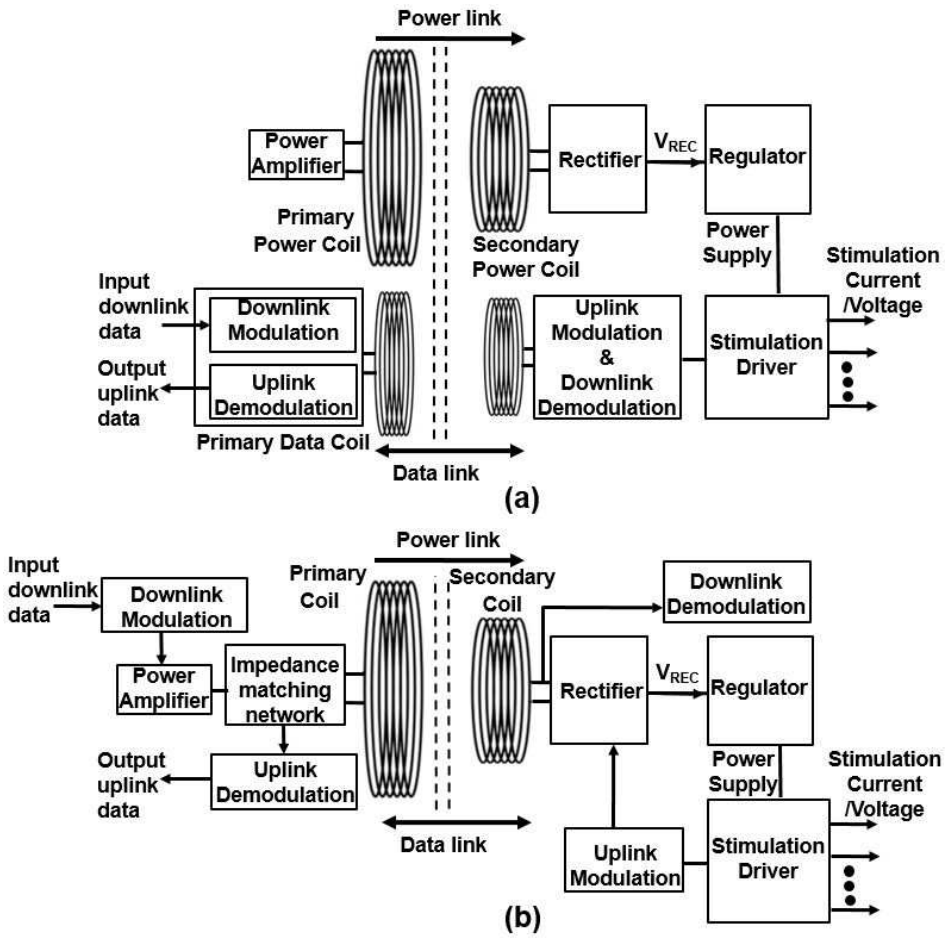


Figure 2.3: Block diagrams of two paradigms of implantable stimulators with bidirectional biotelemetry schemes: a) dual band system (after [104]), b) single band system (after [70]).

2.2.3 Wireless Telemetry

In the discussion of the stimulation pattern, it is acknowledged that it must be programmed wirelessly. Generally, for most of the implant applications, the bidirectional or unidirectional exchange of data needs to be maintained for the remote control and real-time monitoring purpose. The data communication can be achieved by a dedicated pair of data/control coils or via power coils in some circumstances. In Fig. 2.3, two paradigms of implantable stimulators with bidirectional biotelemetry schemes are illustrated.

In Fig. 2.3-a, an example of the dual band implantable stimulator with bidirectional biotelemetry system is shown [106, 107]. In the dual band wireless power and data telemetry systems, the power link and data link are separated to achieve both high data rate and good PTE. As

shown in Fig. 2.3-a, the modulation and demodulation building blocks are designed on both the external unit and the internal unit. In Fig. 2.3-b, a single band system [58,70,108] is shown, in which both power link and data link share the same coils. The information-carrying signals are transmitted bidirectionally between the external unit and the implant unit. The data telemetry uplink transmits the monitored/detected signal in the implant to the external unit, while the downlink sends the control command in the opposite direction. The single band system is an attractive solution for the applications that require compact size. However, it sometimes suffers from the interference issue due to the oppositely directed requirements from the power- and information-carrying signals [70].

The digital modulation schemes are commonly employed in the biomedical implanted devices [109]. The existing methods include amplitude shift keying (ASK) [110, 111], On-off keying (OOK) [112], phase-shift keying (PSK) [113–115], frequency-shift keying (FSK) [116], and load-shift-keying (LSK) [117, 118]. In addition, the telemetry can be performed as active telemetry [119] or passive telemetry [120]. The determination of the modulation scheme and the implementation of the telemetry requires a good understanding of the applications' requirements, such as the data rate.

2.3 Review of State-of-the-Art Works

To meet the design requirements and challenges, several design techniques have been proposed. In this section, we will first review the techniques in addressing specific challenges discussed in Section 2.2. After that, the state-of-the-art works in the system level implementation will be categorized according to the applications and reviewed.

2.3.1 Design Techniques in Addressing Size, Power Challenges

Due to the intrinsic size limitation of the implantable electronics, the design techniques to minimize the usage of the external components are attractive to the circuit designers. One example is the external capacitor-less configuration [121, 122] for the low drop-out regulator. As will be discussed in Chapter 4, this technique can be introduced for the iEAP-based muscle prosthesis to remove bulky LDO output capacitor and maintain the loop stability over wide

load ranges. Likewise, the design techniques to reduce the size of the multi-channel multi-site stimulators are important to overcome the size constrains for many applications. In [123], two approaches (1:4 demultiplexer and chip clustering) were presented in extending the 256-channel stimulator to a 1024-channel counterpart for the retinal prosthesis.

The power related challenges include the power budget, the PTE and the power consumption of the implant unit. First, since the power consumption of the implant unit is directly related to the heating effects, the prescribed global standards and regulations for electromagnetic protection (such as the specic absorption rate (SAR) [124, 125]) must be obeyed to guide the power budget allocation. Similarly, the upper limit of allowable exposure (MPE) for current and elds in [126] needs to be carefully studied in the system power planning. To avoid overheat effects to the tissues caused by the WPT system, the power budget for most of the implant unit is limited to a few milliwatts [127–129].

Second, within the allowable power budget for an application, the PTE needs to be optimized for an effective wireless power transfer. Several novel configurations for the wireless power transfer system have been presented, aiming at boosting the PTE. For example, in [81], an adaptive solution based on the closed-loop operation was proposed. The supply voltage of the class E power amplifier was dynamically adjusted to fulfill the load variations in the implant. Furthermore, the novel configurations have also been proposed to optimize the PTE. The invention of the 3-coil and 4-coil inductive link configurations [76, 130] have been proven to be effective for PTE boost. For a 3-coil wireless power transfer structure, the third link was inserted into the implant between the conventional primary and secondary coil, to transform the variable load impedance to an optimal impedance needed for an improved power transfer efficiency.

In the third place, the reduction of the implant unit's power consumption is also important. Currently, the low power circuit design techniques [131] have been extensively used for the building blocks in the implant unit. For instance, a low power current sensing circuit was proposed in [132] for monitoring implantable brain chemistry. Another attempt in reducing the power loss (and thus avoid overheat effects) is the employment of the full wave rectifier in processing the received sinusoidal power at the secondary power coil [81, 133].

2.3.2 Design Techniques in Addressing Stimulation Challenges

As discussed in Section 2.2.2, the application-specific stimulation patterns are needed in designing the stimulation drivers. To achieve the optimized solution, the circuit designers need to understand the metrics of three stimulation modes introduced in Section 2.2.2 (CCS, VCS and ChCS) and the associated issues.

We start from the CCS. According to the relationship among the charge, current, and stimulation duration, the amount of charge supplied in each stimulus is easily controlled by programming the current amplitude and the stimulation time. Therefore, the safety of tissue is under control when CCS is applied. However, CCS is usually complex in the circuit implementation and not competitive in the power efficiency [70]. In addition, it also suffers from two extra issues in practice. One is the high output impedance requirements. Due to the highly variable impedance of the tissue, the stimulation driver must provide high output impedance with the generated current source in all conditions [134]. The second one is the large compliance voltage associated with the current source. Under a large stimulation current and high output impedance conditions, high compliance voltage is necessary to preserve the accuracy of the output current and prevent it from saturation [43]. As a result, the high voltage requirement brought from the CCS will bring the safety challenges to a human body. Moreover, CCS also requires the high voltage CMOS technology to implement the circuits, which in turn increase the solution cost.

In terms of VCS, it features the simplest implementation (shown in Fig. 2.2-b) and thus the highest power efficiency among these three modes. Besides that, no high compliance voltage is required in using VCS. However, the charge delivered to the tissue using VCS can vary over a wide range, due to the tissue's load impedance. This variation can cause the safety concern for many applications [70].

The ChCS mode [98] offers a good balance between the design complexity and safety related issues. In virtue of the capacitor bank, the (well controlled) quantized amounts of charge are delivered to the tissue. Nevertheless, the capacitor bank needs to be implemented by the off-chip capacitors, which constrains its use in some applications.

A summary of the comparison of these three stimulation modes are provided in Table 2.2

Table 2.2: Comparison of three stimulation modes (after [70])

	CCS	VCS	ChCS
Design complexity	High	Lowest	Low
Charge controllability (Safety)	Good	Poor	Good
Power efficiency	Low	High	Medium

Table 2.3: Comparison of active and passive charge balancing techniques (after [70])

	Active charge balancing	Passive charge balancing
Design complexity	High	Low
Solution size	Low	Large (mainly due to the blocking capacitor)
Adaptivity	High (can be used for different stimulation parameter)	Lower (due to the larger time constant from the blocking capacitor)

[70]. Being aware of the safety requirements and the size budget from the application will aid the system designers in choosing the right stimulation modes.

In addition to the stimulation mode, the residual charge from either the monophasic or biphasic current stimulation is also a challenging issue. The residual charge during the stimulation cycles can increase the electrode voltage above the safe limit and thus jeopardize the human safety. Therefore, it is important to maintain the balanced charge in the stimulation cycles with the aid of dedicated circuits or components [135]. Currently, both active balancing techniques [42, 136, 137] and passive techniques [97, 138–140] are being used to tackle the charge unbalance issues. For the active charge balancing techniques, the charge in the stimulation is either being surveillanced in the real time [136] or corrected by a inserted discharging pulse [42] to achieve the balance. On the other hand, the counterpart passive solution can be implemented by a blocking capacitor [97,138,139] or the electrode discharge resistors [140]. A comparison between these two charge balance solutions is listed in Table 2.3 [70], from which we can see the active charge balancing technique is more versatile, while the passive one owns the lower design complexity. By choosing the proper charge balancing techniques to remove the residual charge, the electrode corrosion and the death of the cells can be well prevented.

2.3.3 Design Considerations for Wireless Telemetry

To provide the wireless programability of the stimulation pattern, the command signal needs to be modulated onto a carrier in the inductive link. As discussed in Section 2.2.3, the choice of the

Table 2.4: Comparison of active telemetry and passive telemetry (after [70])

	Active telemetry	Passive telemetry
Produce RF waves?	Yes	No
Power attenuation	Low	High
Size of required antenna	Small	Large
Target implant size	Smaller	Larger
Typical location of the target implant	Deeper inside the body	Underneath the skin
Power consumption	High	Low
Favored data rate	High	Low

Table 2.5: Comparison of three basic digital modulation schemes (after [70])

	ASK	FSK	PSK
Modulation parameter	Amplitude	Frequency	Phase
Complexity of implementation	Simple	Medium	High
Noise rejection	Poor	Moderate	Good
Bandwidth and its utilization	Low	Twice of ASK spectrum	Can achieve higher bandwidth utilization than FSK
Interference sensitivity	High	Less than ASK	Less than ASK

modulation schemes introduced in Section 2.2.3 is based on the requirements of the application. In Table 2.4, a comparison was made between active telemetry and passive telemetry [70], which shows the active telemetry is more appropriate for the applications with high data rate, such as the retinal prosthesis. In contrast, the passive telemetry will be of favor when only a small quantity of data needs to be transmitted.

The comparison study of the three basic binary digital modulation schemes is shown in Table 2.5 [70]. For these schemes, a tradeoff exists among the implementation complexity, the data-rate and the rejection of the noise and interference. Among these metrics, the data-rate requirement of the applications plays an important role in the selection of the modulation schemes. Typically, the carrier frequency must be limited to a certain range to avoid the increased heat and power dissipation in the tissue [141]. Therefore, data-rate-to-carrier-frequency (DRCF) ratio [142] is introduced as a figure of merit in justifying the modulated data amount on a certain carrier frequency. Usually, a higher DRCF can be obtained from the binary FSK than from the ASK. This fact can be taken into account in the modulation choice decision. For the other applications requiring high data rate, PSK should be considered first due to its advantages in the bandwidth utilization.

One such an example is the retinal stimulator, in which a relatively high data rate is desired. In the forward data telemetry, 1000 pixels are needed to restore important visual function using

[63]. To achieve the pixels requirements in the retinal prosthesis, each stimulator must be independently controlled to provide a customized stimulation pattern [123]. In [123, 143], PSK schemes are employed with novel techniques to overcome the data rate bottleneck caused by the budget of the acceptable power consumption. In [123], a data bandwidth reduction is achieved, and the data discard rate is reduced when the stimulation parameters are sent only by demand. Similarly, in [143], an on-chip address generator is introduced to take the initial address, while all other addresses are obtained following a programming rule.

In addition to the three basic schemes in Table 2.5, some other modulation schemes also exist. For instance, OOK and LSK are the special forms of the ASK. A notable feature of the LSK schemes is that the simultaneous power and data transfer is allowed at the same inductive link [144]. However, using the same link for both power and data raises a risk of power supply discontinuation when the secondary coil undergoes the short-circuiting condition for a certain period [70]. The pros and cons of LSK can also be considered in evaluating the proper schemes for the applications.

2.3.4 System Level Implementations

The discussion above demonstrates the design techniques and considerations to improve one or more metrics of implantable stimulators. Here, the system level state-of-the-art works are reviewed based on the four application category mentioned in Section 2.1.

In Table 2.6, the state-of-the-art works of the retinal prosthesis are presented. Due to the demand of the large volume data, the unidirectional data link must be carefully designed with the proper modulation scheme to provide the optimum data rate. In addition, the number of stimulation channels, the error rate in the data link, the resolution of the current generator (number of bits in DAC) and pixel size is also of concern in these designs to provide an acceptable visual quality to the patients. These considerations are taken care in the works shown in Table 2.6, without severe degrading of the overall chip size and power consumption.

In Table 2.7, the state-of-the-art works of the cochlear implants are surveyed. Since the quality of the generated current pulses from the stimulator will determine the hearing restoration, the amplitude and the resolution of the current source is the key parameter in the stimulator design [47]. On the other hand, compared with the other applications, the requirement for the

Table 2.6: State-of-the-Art retinal stimulators.

	[114]	[44]	[146]	[147]	[148]	[149]	[43]
Year	2013	2013	2012	2011	2011	2011	2010
CMOS technology (μm)	0.065	0.18 HV	0.35 HV	0.5	0.35 HV	0.35	0.18 HV
Area (mm^2)	14	37.6	64	5.3	24	10.5	27.03
# of stimulation channel	512	1024	1024	15	98	1600	256
Compliance voltage (V)	$\pm$2.5	$\pm$10	$\pm$10	$\pm$2.5	8 to 20	$\pm$2	$\pm$10
Current range (mA)	0-0.05	0.003-0.5	0.004-1	0.03-0.96	0.02-1.24	0-0.1	0.003-0.5
Modulation	PSK	DPSK	Photodiode	ASK	FSK	N/A	DPSK
Data-rate (Mb/s)	20	2	0.968	0.025-0.714	2.083	N/A	2
Data link bit error rate (BER)	N/A	$2 \cdot 10^{-7}$	N/A	10^{-2} to 10^{-5} (estimation)	N/A	N/A	10^{-4}
# of bits in DAC	4	7	6	5	7	N/A	4
Pixel size (μm^2)	260×260	303×337	500×470	N/A	N/A	70×70	260×309

N/A: information not available.
HV: high voltage

Table 2.7: State-of-the-Art cochlear stimulators.

	[47]	[150]	[151]	[152]	[134]
Year	2008	2007	2006	2005	2005
Power dissipation (mW)	N/A	0.047	2.5	0.126	N/A
CMOS technology (μm)	0.35	0.7 HV	0.7 HV	0.8	1.5
Area (mm^2)	0.26	5.29	7	21	0.05
# of stimulation channel	N/A	16	4	16	4
Compliance voltage (V)	4.77	13	$\pm$2	N/A	4.25
Maximum current(mA)	1	1	0.5	0.7	0.21
# of bits in DAC	9	7	8	6	5
Output resistance ($M\Omega$)	$>$50	N/A	N/A	N/A	$>$10

N/A: information not available.
HV: high voltage

wireless data telemetry is not crucial. Therefore, in the works shown in Table 2.7, the corresponding modulation and demodulation circuits were not designed as a tradeoff to save the overall chip size and power consumption.

In Table 2.8 and Table 2.9, the state-of-the-art works of the deep brain stimulators and some general neural stimulators are reviewed. The requirements of these two applications have many metrics in common. For example, the stimulators are usually incorporated into the recording systems in the neuroprosthetic devices to enable the bidirectional data communication on a closed-loop basis [145]. The specifications of the recording systems are not shown in these two tables because it is out of the scope of this work. However, it is worthwhile to note that the existence of the recording system reduce the power and chip area budget for the stimulators, while the bidirectional communication requirements raised the design complexity of the entire system. For the works shown in these two tables, the power dissipation, area, and data transmission rates are carefully considered to meet the design challenges discussed Section 2.2.

Table 2.8: State-of-the-Art deep brain stimulators.

	[153]	[53]	[52]	[51]	[50]	[154]
Year	2016	2015	2014	2013	2012	2011
Power dissipation (mW)	N/A	N/A	0.468	15	4.1	0.375
CMOS technology (μm)	0.18	0.35	0.18	0.5	0.35 HV	0.35
Area (mm^2)	7.74	12	4	2.25	0.71	10.9
# of stimulation channel	8	4	8	4	3	4
Current range (mA)	0.0825-0.229	0.012-1.5	0-4.2	0.08-2.48	0-1.85	0-0.0945
Stimulation frequency (Hz)	60-220	7.6-244	N/A	N/A	N/A	$1k-1Meg$
Modulation	LSK/ASK	OOK/LSK	N/A	ASK/LSK	N/A	FSK/OOK
Data-rate (Mb/s)	2/0.1	0.0156	0.8	0.05	N/A	N/A

N/A: information not available.
HV: high voltage

Table 2.9: State-of-the-Art general neural stimulators.

	[155]	[155]	[56]	[55]	[103]	[49]	[156]
Year	2017	2017	2016	2014	2013	2012	2010
Power dissipation (mW)	18	<0.1	2.17	2.8	1.5	0.47	0.27
CMOS technology (μm)	0.18 HV	0.18 SOI	0.13	0.18	0.13	0.18	0.18
Area (mm^2)	29.5	9	16	13.47	12	4	4
# of stimulation channel	160	16	64	1	64	10	64
Compliance voltage (V)	$\pm$ 12	N/A	N/A	N/A	2	N/A	1.8
Current range (mA)	0.5	0-0.145	0.01-1	0-0.03	0.01-1.2	0-0.1	0-0.135
Modulation	DPSK/LSK	ASK/LSK	UWB/FSK	OOK	UWB	FSK	N/A
Data-rate (Mb/s)	2	N/A	N/A	4	10	0.8	N/A

N/A: information not available.
HV: high voltage
SOI: silicon on insulator

2.4 Summary

In this chapter, the background of implantable stimulators is introduced first. After that, the design challenges and the design techniques to meet the requirements are presented. Last, the state-of-the-art works on implantable stimulators are reviewed based on the applications. Generally, the stimulators discussed in this section employ the digital modulation schemes to generate various AC stimulation patterns to meet different application requirements. As will be discussed in Chapter 4, the special application requirements of the iEAP-based muscle prosthesis (such as the requirements of the tunable DC output voltage) will be analyzed during the development of the stimulators. The proposed stimulator will employ a novel design technique (other than the digital communication schemes reviewed in this chapter) to provide the tuning capability of the LDO's DC output voltages to actuate the iEAPs.

Chapter 3

High Precision Reference Circuits

For all modern electronic systems, such as the voltage regulator in implantable stimulators, precise voltage reference circuits are essential building blocks. A key requirement of a voltage reference circuit is to generate a voltage that is independent of temperature variations. Thermal independence is particularly important in applications where maintaining a high level of accuracy is required across wide temperature ranges [157–164].

3.1 Introduction

The most commonly used topology for the implementation of reference circuits is the BGR [165, 166]. A BGR is "ideally" designed to generate an output voltage that is referred to the bandgap energy of the background semiconductor material (which is strongly temperature independent). In Silicon (Si)-based technologies, the base-emitter voltage (V_{BE}) is related to the bandgap energy, and so it has been utilized to develop BGR circuits. However, in addition to being related to the bandgap energy, V_{BE} is also a strong function of the temperature, depending linearly ($\propto T$) and nonlinearly ($\propto T\ln(T)$) on the temperature. Therefore, a major challenge in BGR design has been to find innovative ways to cancel the temperature dependent parameters in V_{BE}.

In a conventional BGR circuit, a PTAT component is generated to cancel the temperature dependency of V_{BE} only to the first order. However, due to the existence of the high-order temperature effects, these circuits offer medium performance and are not adequate for high performance applications. To improve the temperature stability of BGR circuits, a variety of high-order temperature compensation solutions have been proposed to cancel higher order temperature effects of V_{BE} related to $T\ln(T)$ [167–188]. The majority of these solutions cancel a few higher order terms, leaving out some levels of temperature dependency in the

output voltage. In this chapter, three different kinds of curvature compensation techniques for BGR circuits are presented using IBM's Silicon-Germanium (SiGe) BiCMOS technology.

This chapter is organized as followings. A brief review of the SiGe BiCMOS technology and the design challenges of the BGR circuits are given in Section 3.2 and Section 3.3. In Section 3.4, a novel BiCMOS-based compensation technique is introduced which aims to "*directly*" cancel the nonlinear term $T\ln(T)$ in the V_{BE}, thereby, offering the possibility of achieving fully temperature-independent BGR circuits. In Section 3.5, a temperature compensation technique based on the weighted difference of Si-Si and SiGe-Si $p-n$ junction voltages for SiGe reference circuits is presented. In Section 3.6, a systematic piecewise curvature-corrected compensation technique is proposed.

3.2 Thermal Characteristics of the Devices in the SiGe BiCMOS Technology

The circuits proposed in this chapter are implemented in IBM's SiGe BiCMOS 8HP technology. In this section, the 8HP technology is introduced first. Then the operation and the thermal characteristics of CMOS, BJT and SiGe HBTs, available in this process are described.

3.2.1 SiGe BiCMOS technology

The SiGe BiCMOS technology, by offering high-speed, low-noise bandgap-engineered HBTs while maintaining integration capability with conventional Si CMOS [189,190], has emerged as a promising technology platform for the realization of a wide variety of analog, RF and mixed-signal circuits. Examples include voltage regulators [160, 191], high-speed data converters [192, 193], comparators [194], oscillators [195], RF amplifiers [196, 197], and microprocessors [198].

Generally, in analog and mixed-signal designs using this technology, the key device parameters of SiGe HBTs, such as the current gain (β), the cut-off frequency (f_T), the Early voltage (V_A) and the transconductance (g_m), are exploited for improved circuit performance, and designs are complemented by using CMOS transistors [199].

For this study, IBM's third-generation SiGe BiCMOS 8HP technology has been utilized.

Table 3.1: Performance metrics of IBM's 8HP SiGe BiCMOS technology.

Parameters	**Values**
$W_{E,eff}(\mu m)$	0.12
$peak\ \ \beta$	400
$V_A(V)$	>150
$peak\ \ f_T(GHz)$	207
$peak\ \ f_{max}(GHz)$	285
$BV_{CEO}(V)$	1.7
$BV_{CBO}(V)$	5.5
$L_{eff}(\mu m)(NMOS, PMOS)$	0.092

This commercially available SiGe BiCMOS technology is fully equipped with passive elements (polysilicon and diffused resistors, various capacitors) and three active devices: *0.13-*μm CMOS transistors, vertical bipolar junction transistors, and SiGe HBTs. Typical device performance metrics for this technology are summarized in Table 3.1 [200].

In this chapter, the SiGe BiCMOS technology is used in all of the BGR circuit design. Therefore, it is important to understand the thermal characteristics of all three types of devices: CMOS devices, BJT and SiGe HBT.

3.2.2 CMOS Transistors

It is well known that in an NMOS transistor, when the gate-source voltage (V_{GS}) is larger than its threshold voltage (V_{TH}), the drain current (I_D) is expressed as [201]:

$$I_D = \begin{cases} \frac{\mu C_{ox} W}{2L}(V_{GS} - V_{TH})^2 & \text{(Saturation)} \\ \frac{\mu C_{ox} W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] & \text{(Triode)} \end{cases} \tag{3.1}$$

where V_{DS} is the drain-source voltage, μ is the electron mobility, C_{OX} is the gate capacitance per unit area, and $\frac{W}{L}$ is the channel's aspect ratio. In both conditions of (3.1), μ and V_{TH} are the temperature dependent parameters. In deep triode region, where $V_{DS} << 2(V_{GS} - V_{TH})$, the drain current can be estimated to be

$$I_D = \frac{\mu C_{ox} W}{L}(V_{GS} - V_{TH})V_{DS}. \tag{3.2}$$

The temperature dependency of μ is described as [202]

$$\mu = \mu_0(\frac{T}{T_0})^{-m}. \tag{3.3}$$

In (3.3), μ_0 is the mobility at the reference temperature T_0, and m is a positive constant (≈ 2.3) [202]. The threshold voltage decreases linearly with temperature as [203–205],

$$V_{TH} = V_{TH0} - \alpha(T - T_0), \tag{3.4}$$

where α is a positive number and V_{TH0} is the threshold voltage at T_0.

When the V_{GS} is smaller than V_{TH}, the transistor operates in the subthreshold region, and if $V_{DS} > 3V_T$ (V_T is the thermal voltage, $V_T = \frac{kT}{q}$), I_D is estimated to be [206]:

$$I_D = \mu C_{ox}(n-1)\frac{W}{L}V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right), \tag{3.5}$$

where n is the subthreshold slope factor, which is around *1.5* [207].

In practice, V_{GS}, V_{DS} and I_D can be completely or partially controlled by external circuits. In Section 3.4 and Section 3.6, the thermal behavior of CMOS transistors will be used in the voltage reference circuits design.

3.2.3 Bipolar Junction Transistors

In IBM's SiGe BiCMOS 8HP technology platform, vertical PNP (VPNP) BJT devices are available [208, 209]. The base-emitter voltage of the BJT is described as [22, 166]:

$$V_{BE,BJT}(T) = V_{G0,Si} - [V_{G0,Si} - V_{BE0}]\frac{T}{T_0} - \frac{kT}{q}(\eta - \theta_{BJT})\ln\left(\frac{T}{T_0}\right), \tag{3.6}$$

where $V_{G0,Si}$ is the extrapolated bandgap voltage of Si at 0 Kelvin, T is the absolute temperature in Kelvin, T_0 is the reference temperature, V_{BE0} is the base-emitter voltage at the reference temperature T_0, k is the Boltzmann constant, q is the electron charge, η is a process-dependent positive constant, and θ_{BJT} represents the order of the temperature dependency of the collector current $I_{C,BJT}$, with which the transistor is biased:

$$I_{C,BJT}(T) = I_{C0,BJT}\left(\frac{T}{T_0}\right)^{\theta_{BJT}}. \tag{3.7}$$

In (3.7), $I_{C0,BJT}$ is the collector current at the reference temperature T_0. Note that when the collector current follows a PTAT behavior, $\theta_{BJT} = 1$. Re-ordering the terms in (3.6), results in

$$\begin{aligned} V_{BE,BJT}(T) &= V_{G0,Si} - \left[\frac{V_{G0,Si} - V_{BE0}}{T_0} - \frac{k}{q}\ln(T_0)^{(\eta-\theta_{BJT})}\right]T \\ &- \left[\frac{k}{q}(\eta - \theta_{BJT})\right][T\ln(T)]. \end{aligned} \tag{3.8}$$

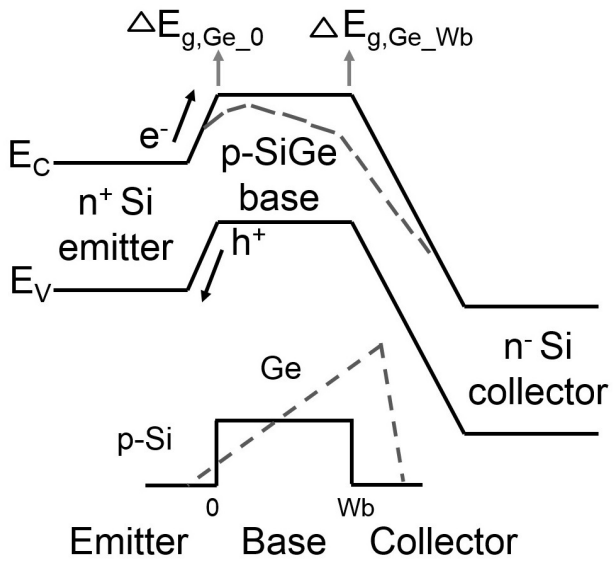


Figure 3.1: Energy band diagram for the Si BJT and the SiGe HBT (after [190]).

As can be seen from (3.8), the $V_{BE,BJT}$ is linearly ($\propto T$) and nonlinearly ($\propto T\ln(T)$) is dependent on the temperature. As it will be discussed in Section 3.3, the expression of $V_{BE,BJT}(T)$ highlights the BGR design challenges in achieving a relatively thermal independent output voltage.

3.2.4 SiGe Heterojunction Bipolar Transistors

The energy band diagram of graded-base SiGe HBT is displayed in Fig. 3.1 and is compared to that of the BJT [190]. The introduction of compositionally graded Ge in the base (shown by the dash lines) results in a finite band offset at the emitter-base junction ($\Delta E_{g,Ge_0}$) and a larger band offset at the collector-base junction ($\Delta E_{g,Ge\_Wb}$), compared to its Si counterpart. The position dependence of the band offset with respect to Si is generally expressed as $\Delta E_{g,Ge(grade)} = (\Delta E_{g,Ge\_0} - \Delta E_{g,Ge\_Wb})$. If the SiGe HBT is biased such that its collector current ($I_{C,HBT}$) follows

$$I_{C,HBT}(T) = I_{C0,HBT}\left(\frac{T}{T_0}\right)^{\theta_{HBT}}, \tag{3.9}$$

where $I_{C0,HBT}$ is the collector current at T_0 and θ_{HBT} denotes the order of the temperature dependency of the collector current, the temperature characteristics of its base-emitter voltage

($V_{BE,HBT}$) is expressed as [190]:

$$V_{BE,HBT}(T) = V_{G0,SiGe} - [V_{G0,SiGe} - V_{BE0}]\frac{T_0}{T} - \frac{kT}{q}(l - \theta_{HBT})\ln\left(\frac{T}{T_0}\right) \tag{3.10}$$
$$- \left\{\frac{kT}{q}\ln\left(\frac{1-\exp\left(\frac{-\Delta E_{g,Ge(grade)_0}}{kT_0}\right)}{1-\exp\left(\frac{-\Delta E_{g,Ge(grade)}}{kT}\right)}\right)\right\} - \left\{\frac{kT}{q}\ln\left(\frac{T_0}{T}\frac{\Delta E_{g,Ge(grade)}}{\Delta E_{g,Ge(grade)_0}}\right)\right\}.$$

In (3.10), $V_{G0,SiGe}$ is the extrapolated bandgap voltage of SiGe at *0 K*, $V_{BE0_{HBT}}$ is the base-emitter voltage, $\Delta E_{g,Ge(grade)_0}$ is the Ge grading-induced bandgap offset at T_0, and l is the saturation current temperature exponent. Assuming the Ge grading ($\Delta E_{g,Ge(grade)}$) does not change with temperature [190], rearranging the terms in (3.10) results in

$$V_{BE,HBT}(T) = V_{G0,SiGe} \tag{3.11}$$
$$\underbrace{-\left[\frac{V_{G0,SiGe} - V_{BE0_{HBT}}}{T_0} - \frac{k}{q}\ln\left(\frac{T_0^{(l-\theta_{HBT}-1)}\Delta E_{g,Ge(grade)}}{\Delta E_{g,Ge(grade)_0}}\left[1-\exp(\frac{-\Delta E_{g,Ge(grade)_0}}{kT_0})\right]\right)\right]T}_{\text{linear}}$$
$$\underbrace{-\left[\frac{k}{q}(l-\theta_{HBT}-1)\right][T\ln(T)]}_{\text{nonlinear 1}} + \underbrace{\left[\frac{kT}{q}\ln\left(1-\exp\left(-\frac{\Delta E_{g,Ge(grade)}}{kT}\right)\right)\right]}_{\text{nonlinear 2}},$$

where the linear and nonlinear temperature dependent terms have been highlighted. Since the Ge-induced bandgap offset is typically around *100* meV, the second nonlinear term in (3.11) can be neglected over a wide temperature range (for example, *-70*$^\circ C$ to *150*$^\circ C$). Neglecting the second nonlinear term in (3.11), and comparing (3.8) in Section 3.2.3 and (3.11), one can see that both $V_{BE,BJT}$ and $V_{BE,HBT}$ share similar temperature dependent terms: $\propto T$ and $\propto [T\ln(T)]$.

3.3 Design Review of Reference Circuits

In the realization of a bandgap reference, at least one design component related to the bandgap energy must be available [166, 210]. In Si-based technologies, the relation to the bandgap energy is established through the base-emitter junction. Ignoring the small temperature variations in the bandgap voltage itself, the thermal dependency of the base-emitter voltage of the Si-based bipolar junction transistor ($V_{BE,BJT}$) can be expressed as (3.6) in Section 3.2.3. With its re-ordered expression in (3.8) highlights the two temperature dependent terms in $V_{BE,BJT}(T)$: *the linear term* (T) and *the nonlinear term* ($T\ln(T)$).

In the design of BGR circuits, temperature dependent compensation components are generated and added properly to $V_{BE,BJT}$ in an attempt to cancel the temperature dependent terms in (3.8). The cancelation of the linear term is performed through the addition of the PTAT voltage/current, leading to what is known as the traditional "first-order" temperature compensated BGR circuits. For high precision reference circuits, the nonlinear term in (3.8) also needs to be canceled. This cancelation, however, due to the nature of the nonlinear term $T\ln(T)$, has been challenging to achieve. A popular approach has been to perform the Taylor series on the expression of $V_{BE,BJT}(T)$, and to design proper compensation circuits to cancel the few major high-order terms. Several solutions, including quadratic temperature compensation, second-order curvature compensation using resistor ratio, and piecewise-linear curvature correction, have been proposed for canceling the nonlinear term in (3.8) *to some degree* (e.g. up to 2^{nd} order).

3.3.1 Quadratic Temperature Compensation Technique

A popular approach has been to perform the Taylor series on the expression of $V_{BE,BJT}(T)$, and to design proper compensation circuits to cancel the few major high-order terms. In another word, 3.8 in Section 3.2.3 can be expanded to the form of

$$V_{BE,BJT}(T) = \alpha_0 + \alpha_1 T + \alpha_2 T^2 + \alpha_3 T^3 + ... + \alpha_n T^n, \tag{3.12}$$

where α_0 represents a constant term, and $\alpha_1 ... \alpha_n$ are the coefficients for their corresponding temperature terms. Once the coefficient of xth order term, α_x, in 3.12 is available, it can be compensated by a scaled $PTAT^x$ component, which can be designed based on the PTAT voltage/current. For example, in [167–171], $PTAT^2$ circuits are designed to cancel the 2^{nd} order temperature dependency of the CTAT components, while in [22], the temperature dependency is canceled up to the 4^{th} order by a $PTAT^4$ components. This technique is straightforward from the design point of view, but suffers from the increased circuits' complexity and the accuracy of the generated $PTAT^x$ components.

3.3.2 Temperature Dependent Resistor Ratio Compensation Technique

Another technique is to use different temperature dependency of various types of resistors in a given process technology in achieving the second-order curvature compensation [172–174]. For example, in [172], the resistor ratio of a poly resistor and a diffusion resistor was utilized for curvature compensation. Due to temperature coefficient difference between these two resistors, a curvature corrected BGR was realized. Although only one extra resistor is added to a first-order compensated BGR to realize the curvature compensation, this method relies on the parameters (temperature coefficients) of the passive components of the used technology, thus is not easily implantable from one process to another. Also, due to the manufacturing variations of passive components, intensive trimming networks are needed to control the overall accuracy in the mass production.

3.3.3 Nonlinearity Subtraction Technique

A series of nonlinearity subtraction circuits have been presented in the last few years [182–184, 211]. For this technique, by (weighted) subtraction of two voltages/currents containing similar temperature dependent terms, the nonlinear temperature dependent terms can be compensated to some degree. The sources in generating these two voltages/currents can be different devices, such as PNP and NPN BJTs [183, 184]. Recently, an active curvature compensation technique exploiting the bandgap narrowing effect was proposed [212] to actively adjust the temperature characteristics of the BJTs. This technique is easy to be implemented but is also constrained by the using technology, because the voltages/currents containing similar temperature dependent terms are not always available in all technologies.

3.3.4 Piecewise Curvature Corrected Technique

In this approach, nonlinear temperature dependent components are generated and used for improving the temperature stability of reference circuits. A piecewise current-mode compensation approach is proposed in [175–181, 185] to obtain an output voltage with low temperature drift. In this approach, the difference between two currents, one proportional to the PTAT component and one proportional to V_{BE}, is generated and incorporated into a segment of the temperature

Table 3.2: Comparison of reviewed curvature compensation techniques.

Compensation Techniques	Pros	Cons
$PTAT^x$ compensation	straightforward design	circuit complexity and difficulty in achieving high precision
Temperature dependent resistor ratio correction	circuit simplicity	process dependent
Nonlinearity subtraction	high precision	process dependent
Piecewise correction	straightforward design	difficulty in achieving high precision
Pseudo "$T\ln(T)$" compensation	high precision	temperature-independent current needed

range of interest in a piecewise manner. The advantage of this method is its cost effective and simplicity. However, it is not easy to precisely control the tuning point and the amplitude of the generated piecewise component to achieve the optimum thermal stability.

3.3.5 Pseudo "$T\ln(T)$" Corrected Technique

In all the work mentioned above, since the $T\ln(T)$ is not completely canceled, there always exist some levels of temperature dependency in the output voltage. In [186], currents proportional to $[T\ln(T)]$, are generated through different circuit implementations, and then used to cancel high-order temperature dependent terms. The recent work in [187] has proposed a solution to generate a current proportional to the nonlinear voltage $\frac{kT}{q}\ln\frac{T}{T_0}$, in an attempt to compensate the high order terms. However, the technique used to generate the nonlinear current requires the existence of the temperature-independent current ($\theta = 0$). This requirement introduces error in the cancelation process, as in practice $\theta \neq 0$.

3.3.6 Comparison of Reviewed Compensation Techniques

Based on the review of existing temperature compensation solutions, their pros and cons are summarized in Table 3.2.

3.4 BiCMOS-Based Compensation: Towards Fully Curvature-Corrected BGR

In the last section, challenges in designing voltage references were described. In this section, a novel BiCMOS-based compensation technique is introduced which aims to "directly" cancel the nonlinear term $T\ln(T)$ in the V_{BE}, thereby, offering the possibility of achieving fully temperature-independent BGR circuits. As it will be shown in the following discussion, the generation of the nonlinear term used for compensation is achieved through biasing the transistor with a PTAT current, which already exists in the circuit for the cancelation of the linear term in (3.8).

3.4.1 Proposed Technique for the Compensation of the Nonlinear Term

Here, we first theoretically and then through simulations, show that the gate-source voltage ($V_{GS}(T)$) of a subthreshold-operating MOSFET biased with a PTAT current, exhibits similar nonlinear $T\ln(T)$ behavior that was observed in $V_{BE}(T)$ in (3.8).

Subthreshold-operating MOSFETs have recently gained an increasing attention for the realization of low power BGR circuits [206, 213–217]. Its principle of operation has been briefly reviewed in Section 3.2. Here, we will go over it in more detail.

In the subthreshold region (where V_{GS} is set to be less than the transistor's threshold voltage (V_{TH}), the drain current (I_D) is expressed as [206]

$$I_D(T) = I_S(T)\exp(\frac{V_{GS}(T) - V_{TH}(T)}{nV_T})[1 - \exp(\frac{-V_{DS}}{V_T})], \tag{3.13}$$

where V_{DS} is the drain-source voltage and $I_S(T)$ is expressed as

$$I_S(T) = \frac{W}{L}\mu(T)(n-1)C_{ox}V_T^2. \tag{3.14}$$

In (3.14), $\mu(T)$ is the carrier mobility, C_{ox} is the gate-oxide capacitance, V_T is the thermal voltage ($V_T = \frac{kT}{q}$), n is the subthreshold slope factor (a process dependent constant around *1.5* [207]), and W and L correspond to the transistor's channel's width and length, respectively.

Under the operating condition of $V_{DS} > 3V_T$ (which is generally the case), (3.13) is simplified to

$$I_D(T) = I_S(T)\exp(\frac{V_{GS}(T) - V_{TH}(T)}{nV_T}). \tag{3.15}$$

From (3.15), $V_{GS}(T)$ can be derived as

$$V_{GS}(T) = V_{TH}(T) + nV_T \ln(\frac{I_D(T)}{I_S(T)}). \tag{3.16}$$

Replacing (3.14) in (3.16), $V_{GS}(T)$ can be re-written as

$$\begin{aligned} V_{GS}(T) = V_{TH}(T) + nV_T \ln(I_D(T)) \\ -nV_T \left[\ln(\frac{W}{L}\mu(T)(n-1)C_{ox}) + 2\ln(V_T)\right]. \end{aligned} \tag{3.17}$$

In (3.17) the main temperature-dependent parameters are the threshold voltage ($V_{TH}(T)$), the thermal voltage (V_T), the mobility ($\mu(T)$), and the drain current ($I_D(T)$) if the transistor is not biased with a temperature-independent current. The temperature dependency of the threshold voltage can be approximated as [203–205]

$$V_{TH}(T) = V_{TH0} - \alpha(T - T_0), \tag{3.18}$$

where V_{TH0} is the threshold voltage at T_0, and α is a positive constant. The temperature dependency of the carrier mobility is estimated as [202]

$$\mu(T) = \mu_0(\frac{T}{T_0})^{-m}, \tag{3.19}$$

where μ_0 is the mobility at T_0 and m is a positive constant. Taking into account equations (3.18) and (3.19), and assuming that the transistor is biased with a PTAT current described as

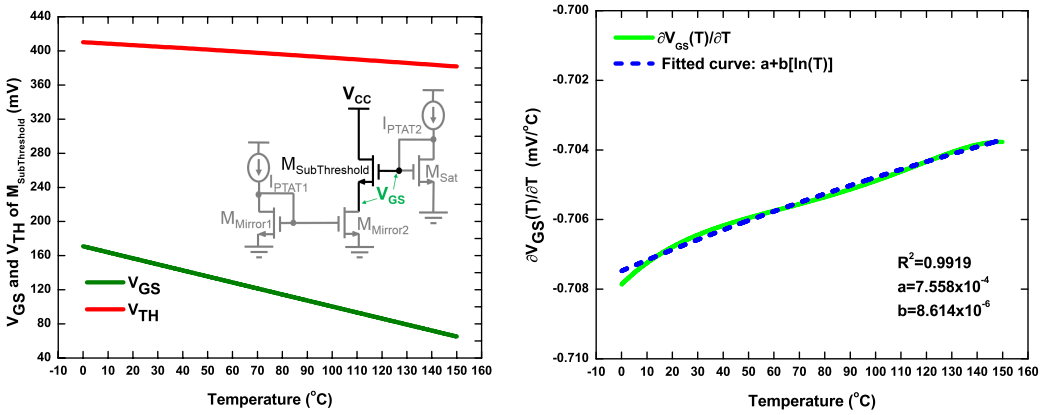
$$I_D(T) = I_{D0}\left(\frac{T}{T_0}\right), \tag{3.20}$$

where I_{D0} is the drain current at T_0, $V_{GS}(T)$ in (3.17) is obtained as

$$\begin{aligned} V_{GS}(T) = [V_{TH0} + \alpha T_0] + \underbrace{\left[\frac{nk}{q}(m-1)\right][T\ln(T)]}_{\text{nonlinear}} \\ \underbrace{-\left[\alpha + \frac{nk}{q}[\ln(\frac{k^2W}{q^2LI_{D0}}(n-1)C_{ox}\mu_0 T_0^{(m+1)})]\right]T}_{\text{linear}}. \end{aligned} \tag{3.21}$$

Equation (3.21) indicates that $V_{GS}(T)$ of a PTAT-biased subthreshold-operating MOSFET exhibits the nonlinear $T\ln(T)$ behavior, similar to what is observed for $V_{BE,BJT}(T)$ in (3.8).

To further verify the existence of $T\ln(T)$ dependency in $V_{GS}(T)$ of a PTAT-biased subthreshold-operating MOSFET, we performed further analysis. Taking the derivative of (3.21) with respect



(a) (b)

Figure 3.2: a) Simulated V_{GS}(T) and V_{TH}(T) of a subthreshold-opearating MOSFET ($M_{SubThreshold}$) as a function of temperature, with its circuit schematic, and b) $\partial V_{GS}(T)/\partial(T)$ fitted to the function $\ln(T)$.

to T we find

$$\frac{\partial V_{GS}(T)}{\partial(T)} = \underbrace{\left[\frac{nk}{q}(m-1)\right]}_{\text{coefficient } b}\ln(T) + \underbrace{\frac{nk}{q}(m-1) - \left[\alpha + \frac{nk}{q}[\ln(\frac{k^2W}{q^2LI_{D0}}(n-1)C_{ox}\mu_0 T_0^{(m+1)})]\right]}_{\text{constant } a}. \tag{3.22}$$

The existence of $T\ln(T)$ dependency in $V_{GS}(T)$ described by (3.21) therefore, can be verified by showing that its derivative follows $\ln(T)$ behavior.

To evaluate this behavior, we performed simulations using the structure shown in Fig. 3.2-a. Transistor $M_{SubThreshold}$ is biased with a PTAT current (through the current mirror $M_{Mirror1}$-$M_{Mirror2}$), and its gate terminal voltage is controlled by a self-biased transistor M_{Sat}, operating in the saturation region. The voltage at the source terminal of $M_{SubThreshold}$ is adjusted to ensure that it is operating in the subthreshold region across the temperature range of interest. Fig. 3.2-a also shows simulation results for $V_{GS}(T)$ of $M_{SubThreshold}$ as well as its $V_{TH}(T)$ vs temperature, demonstrating that $M_{SubThreshold}$ operates in the subthreshold region across the targeted temperature range.

Fig. 3.2-b shows $\frac{\partial V_{GS}(T)}{\partial(T)}$ for transistor $M_{SubThreshold}$. MATLAB was then used to evaluate

the goodness of fit of the derivative of $V_{GS}(T)$ to the function $\ln(T)$. A R^2 value of 0.9919 is obtained (with $a = 0.0007558$ and $b = 0.000008614$), supporting the existence of $T\ln(T)$ in $V_{GS}(T)$. In addition, the values estimated for constant a and coefficient b from the fitting process are in the expected range.

The existence of secondary design component in $V_{GS}(T)$ with similar nonlinear temperature dependent behavior as $V_{BE,BJT}(T)$, provides the designers with the possibility for direct compensation of the nonlinear term in BGR circuits. Additionally, an advantage of this technique is that there is no requirement for the MOSFET to be biased with a temperature-independent current, which is difficult to realize.

3.4.2 Proof of Concept

Motivated by the proposed BiCMOS-based compensation solution, a current-mode BGR circuit is designed in IBM's 8HP SiGe BiCMOS technology. Current-based references have been designed and developed in several Si technologies [175, 185–187, 213, 214, 217, 218]. Compared to voltage-mode references, the current-mode architecture provides several advantages, including being able to operate with sub-1 V power supply, or offering reference values that are different than the bandgap voltage of the background semiconductor material. While we have used a current-mode topology to realize the proposed compensation technique, the proposed BiCMOS compensation solution can also be incorporated in voltage-mode BGRs.

The circuit consists of four major blocks: the I_{PTAT} current generator, the $I_{V_{BE}}$ current generator, the $I_{V_{GS}}$ current generator, and the V_{REF} generator. Details for each block are described here.

3.4.2.1 The I_{PTAT} Current Generator

The schematic of the PTAT current generator with its startup circuit (consisting of transistors M_{S1}-M_{S4}) is shown in Fig. 3.3. The core of the PTAT current generator (right side of Fig. 3.3) consists of transistors M_1-M_6 and the resistor R_1. The operational amplifier (op-amp) uses vertical PNP BJTs as input transistors and follows the folded-cascode architecture [187], and is designed to offer large DC gain (see Fig. 3.4). Current mirrors M_1-M_2 and $M_5 - M_6$ have identical aspect ratios, and op-amp guarantees equal voltages at nodes "A" and "B" [201],

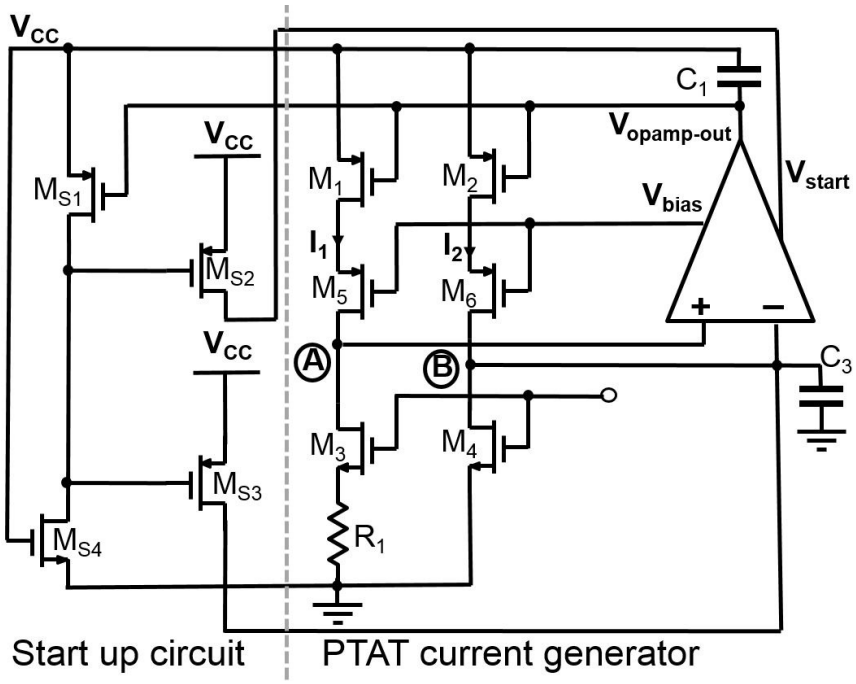


Figure 3.3: Schematic of the PTAT current generator circuit.

ensuring equal currents in two branches ($I_1 = I_2$). Transistors M_3 and M_4 have different aspect ratios and are biased to operate in the subthreshold region [219–221]. Following (3.21), it can be seen that the voltage difference between the V_{GS} of these two transistors (ΔV_{GS}) generates a PTAT voltage that falls across the resistor R_1, generating current I_{PTAT} ($= I_1 = I_2$), expressed as

$$\begin{aligned} I_{PTAT}(T) &= \frac{V_{GS4}(T) - V_{GS3}(T)}{R_1} = \frac{\Delta V_{GS}(T)}{R_1} \\ &= \frac{n \ln[\frac{(W/L)_3}{(W/L)_4}]}{R_1} V_T = \frac{nk \ln[\frac{(W/L)_3}{(W/L)_4}]}{qR_1} T. \end{aligned} \tag{3.23}$$

Since V_{TH} is temperature dependent, careful design considerations were made in choosing the aspect ratios of transistors M_3 and M_4, to ensure they remain operating in the subthreshold region over the target temperature range.

Note that while the PTAT current could also have been generated via the V_{BE} difference of two HBTs instead of the V_{GS} difference of two sub-threshold operating MOSFETs (M_3 and M_4), by using the structure shown in Fig. 3.3, we were able to save on the number of transistors used in the circuit. This is because the V_{GS} of transistor M_4 will be used later to generate $I_{V_{GS}}$ (as will be discussed in Section 3.4.2.3).

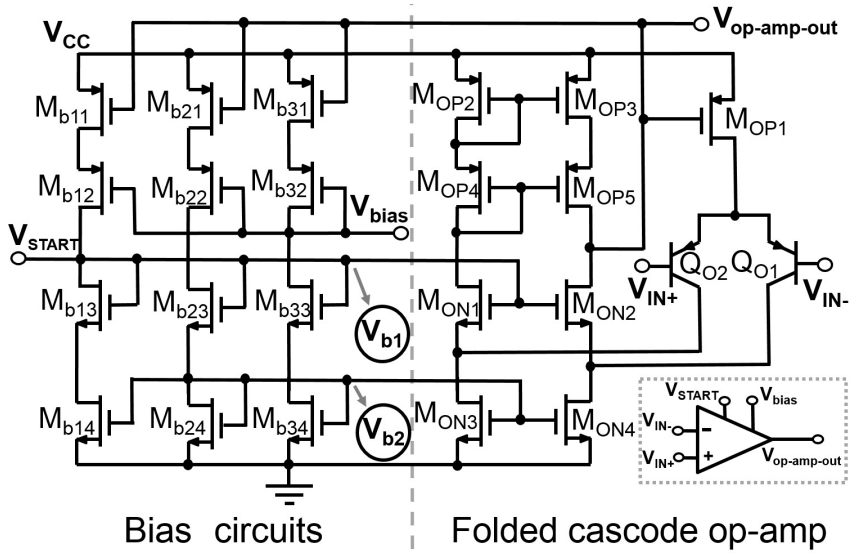


Figure 3.4: Schematic of the operational amplifier used in PTAT current generator.

3.4.2.2 The $I_{V_{BE}}$ Current Generator

The $I_{V_{BE}}$ current is generated based on the base-emitter voltage of SiGe HBTs. In Section 3.2.4, the energy band diagram of graded-based SiGe HBT has been displayed and compared to that of a BJT, while the base-emitter voltage of the SiGe HBTs can be expressed as (3.10).

Assuming the collector current of the HBT is a PTAT current (i.e. $\theta = 1$ in (3.7)), and $\Delta E_{g,Ge(grade)}$ does not change with temperature [190] and rearranging the terms in (3.10), equation (3.11) is obtained where the linear and nonlinear T dependent terms are identified. $\Delta E_{g,Ge(grade)}$ is typically around *100* meV, therefore, over the temperature range of [*0* − *150*] °C, the "nonlinear 2" term in (3.11) can be neglected, i.e.

$$\frac{kT}{q}\ln(1-\exp(-\Delta E_{g,Ge(grade)}/kT)) \approx 0.$$

Neglecting the second nonlinear term in (3.11), and comparing (3.8) and (3.11), one can see that, similar to the BJT, in the case of the HBT, the base-emitter voltage exhibits both linear ($\propto T$) and nonlinear ($\propto T\ln(T)$) temperature dependencies.

The schematic for the $I_{V_{BE}}$ current generator circuit is shown in Fig. 3.5-a [210]. A PTAT current is used to drive the HBT Q_1. Cascode current mirror pairs M_{10a}-M_{11a}, M_{10b}-M_{11b} and transistor M_{12} form a negative feedback loop [210], and capacitor C_2 is added to stabilize the loop. The base-emitter voltage of Q_1 falls across resistor R_3, generating the $I_{V_{BE}}$ current that

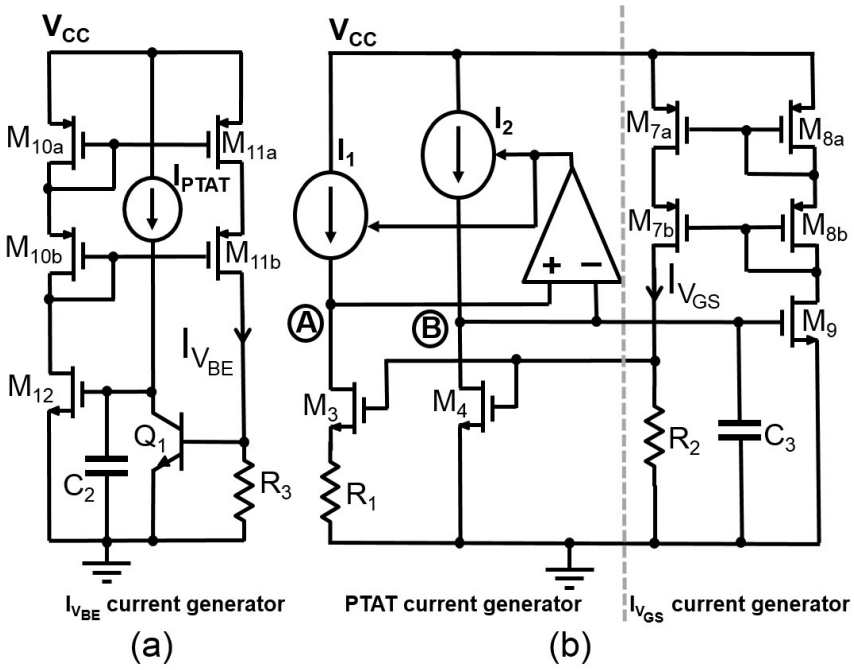


Figure 3.5: Schematic of a) $I_{V_{BE}}$ current generator circuit, and b) $I_{V_{GS}}$ current generator circuit.

is proportional to $V_{BE,HBT}(T)$ (and includes both the CTAT and nonlinear $T\ln(T)$ terms), expressed as

$$I_{V_{BE}} = \frac{V_{BE,HBT}(T)}{R_3}. \tag{3.24}$$

Note that HBTs carry very large current gain [190] (for this technology the nominal current gain for the NPN HBT is 460), and hence, the error introduced by the base current can be neglected.

3.4.2.3 The $I_{V_{GS}}$ Current Generator

To directly cancel the nonlinear $T\ln(T)$ term in $I_{V_{BE}}$, a circuit (see Fig. 3.5-b) for generating a current proportional to $V_{GS}(T)$ of a subthreshold-operating MOSFET is designed. As mentioned in Section 3.4.2.1, transistor M_4 operates in the subthreshold region. A feedback transistor, M_9, is included in the circuit [210], and the capacitor C_3 is added to stabilize the negative feedback loop. The V_{GS} of transistor M_9 equals V_{DS} of transistor M_4. The current $V_{GS}(T)$, proportional to the gate-source voltage of M_4 (which includes both linear and

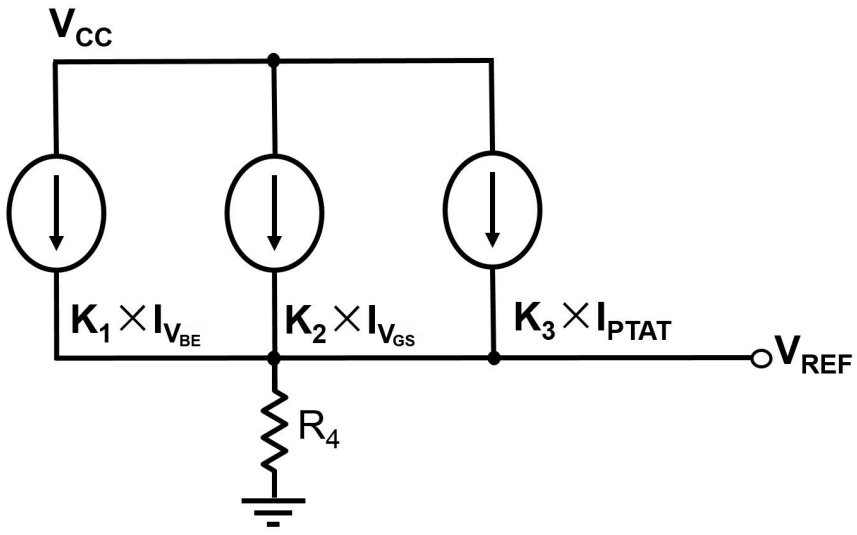


Figure 3.6: Schematic of the V_{REF} generator circuit.

nonlinear $T\ln(T)$ terms), is generated through resistor R_2 as

$$I_{V_{GS}}(T) = \frac{V_{GS4}(T)}{R_2}. \tag{3.25}$$

3.4.2.4 The V_{REF} Generator

The three currents I_{PTAT}, $I_{V_{BE}}$ and $I_{V_{GS}}$ generated by the structures described above, will be mirrored, scaled properly and added. Fig. 3.6 shows the schematic of the V_{REF} generator circuit. V_{REF} is expressed as

$$\begin{aligned} V_{REF} &= R_4[K_1 I_{V_{BE}}(T) + K_2 I_{V_{GS}}(T) + K_3 I_{PTAT}(T)] \\ &= K_1\frac{R_4}{R_3}V_{BE,Q1}(T) + K_2\frac{R_4}{R_2}V_{GS4}(T) + K_3\frac{R_4}{R_1}CV_T, \end{aligned} \tag{3.26}$$

where $C = n\ln[\frac{(W/L)_3}{(W/L)_4}]$, and parameters K_1, K_2 and K_3 are current scaling factors (determined by the aspect ratios in current mirrors) for $I_{V_{BE}}$, $I_{V_{GS}}$ and I_{PTAT} currents, respectively. These factors need to be properly determined such that the temperature dependency of the total current flowing through resistor R_4 (and thereby, the generated voltage V_{REF}), is minimized. Since the output voltage is dependent on the resistor ratio, if both resistors are made of the same material, the dependency of the output voltage to variations in resistors will be minimized.

We now find the design equations required for determining the current scaling factors K_1, K_2 and K_3. Referring to (3.21) and (3.11) for $V_{GS4}(T)$ and $V_{BE,Q1}(T)$, to minimize the

temperature dependency of V_{REF}, the following two conditions need to be met:

- cancelation of the temperature dependent "*linear*" term as

$$\begin{aligned} &K_1\frac{R_4}{R_3}\left[\frac{V_{G0,SiGe}-V_{BE0}}{T_0}\right] \\ &-K_1\frac{R_4}{R_3}\left[\frac{k}{q}\ln\left(\frac{{T_0}^{(l-2)}\Delta E_{g,Ge(grade)}}{\Delta E_{g,Ge(grade)_0}}(1-\exp(-\Delta E_{g,Ge(grade)_0}/kT_0))\right)\right] \\ &+K_2\frac{R_4}{R_2}\left[\alpha+\frac{nk}{q}[\ln(\frac{k^2W}{q^2LI_{D0}}(n-1)C_{ox}\mu_0T_0^{(m+1)})]\right]=K_3\frac{R_4}{R_1}\left[\frac{nk}{q}\ln[\frac{(W/L)_3}{(W/L)_4}]\right]. \end{aligned} \tag{3.27}$$

- cancelation of the temperature dependent "*nonlinear*" term as

$$K_1\frac{R_4}{R_3}\left[\frac{k}{q}(l-2)\right]=K_2\frac{R_4}{R_2}\left[\frac{nk}{q}(m-1)\right]. \tag{3.28}$$

Re-ordering terms in (3.28) results in the following design equation for the cancelation of the nonlinear term

$$\frac{K_1}{K_2}=\frac{R_3}{R_2}\left[\frac{n(m-1)}{(l-2)}\right]. \tag{3.29}$$

The design equation (3.29) relies on the technology-dependent parameters (m, n and l). The estimated value for the carrier mobility temperature exponent m is typically 1.5 [203, 206], and the value for the saturation current temperature exponent l has been approximated to be between 3 to 4 [190, 210, 222–224], ensuring that a positive number is obtained for the ratio of scaling factors K_1 and K_2.

Replacing (3.29) in (3.27) and re-ordering terms, the design equation for canceling the linear term ($\propto T$) is obtained as

$$\frac{K_3}{K_2}=\frac{R_1}{R_2}\left[\frac{A}{\frac{nk}{q}\ln[\frac{(W/L)_3}{(W/L)_4}]}\right], \tag{3.30}$$

where A is described as

$$\begin{aligned} A=&\frac{n(m-1)}{(l-2)}\left[\frac{V_{G0,SiGe}-V_{BE0}}{T_0}\right] \\ &-\frac{n(m-1)}{(l-2)}\left[\frac{k}{q}\ln\left(\frac{{T_0}^{(l-2)}\Delta E_{g,Ge(grade)}}{\Delta E_{g,Ge(grade)_0}}(1-\exp(-\Delta E_{g,Ge(grade)_0}/kT_0))\right)\right] \\ &+\left[\alpha+\frac{nk}{q}[\ln(\frac{k^2W}{q^2LI_{D0}}(n-1)C_{ox}\mu_0T_0^{(m+1)})]\right]. \end{aligned} \tag{3.31}$$

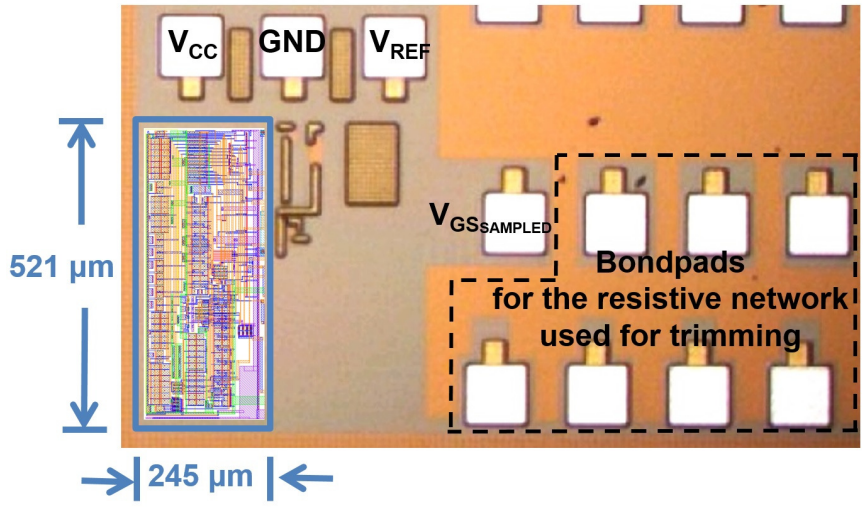


Figure 3.7: Die microphotograph and layout of the voltage reference circuit employing the proposed compensation technique.

When design conditions (3.29) and (3.30) are met, a temperature-independent V_{REF} is obtained as

$$V_{REF} = \frac{R_4}{R_3} K_1 V_{G0,SiGe} + \frac{R_4}{R_2} K_2 [V_{TH0} + \alpha T_0]. \tag{3.32}$$

3.4.3 Verification

The proposed reference circuit was designed in IBM's 8HP SiGe BiCMOS technology. p^+ polysilicon resistors, which have a very small temperature coefficient, were used to implement all of the resistors. Common-centroid layout technique was employed for the realization of the current mirrors to minimize the effects of mismatch. The micrograph of the circuit is shown in Fig. 3.7. The circuit occupies an active area of $245 \times 521\ \mu m^2$ excluding bondpads. A resistive network was also included to allow trimming of the post-fabricated circuit and to compensate for the effects of process variations, inaccuracies in simulation models, and package stress that may occur after fabrication. Additional pads (not shown in Fig. 3.7) were included to monitor the voltage values of internal nodes, to study the temperature dependency of the I_{PTAT} and the $I_{V_{GS}}$ currents (see Fig. 3.8). Since thermal characteristics of SiGe HBTs have been previously extensively investigated [157, 164, 190, 225–227], the $I_{V_{BE}}$ current is not characterized here.

For measurements, three circuits from three different wafers were characterized. Each circuit was mounted in a 28-pin ceramic DIP package and wirebonded. A thermally conductive

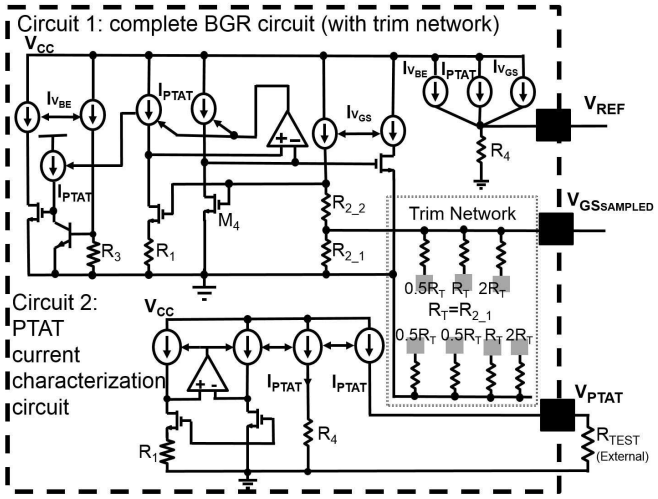


Figure 3.8: Schematic of the reference circuit, resistive network (circuit 1) and the test structure for the experimental characterization of the PTAT current (circuit 2).

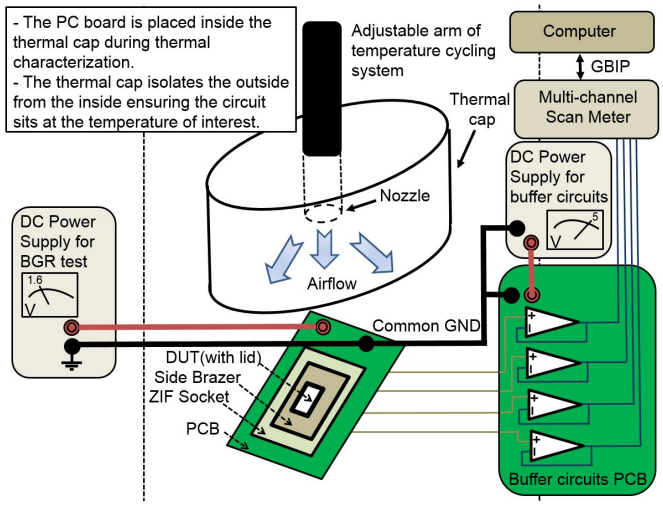


Figure 3.9: Illustration of the experimental setup for thermal characterization of the circuits.

Table 3.3: Summary of Monte Carlo simulation results for ΔV_{GS} and V_{GS4}.

		0 °C	**25 °C**	**85 °C**	**150 °C**
$\mathbf{\Delta V_{GS}}$	**Mean** (μ) (mV)	20.43	22.01	25.89	30.26
	Standard Deviation (σ) (mV)	0.477	0.478	0.569	0.691
	σ/μ (%)	2.33	2.17	2.20	2.28
$\mathbf{V_{GS4}}$	**Mean** (μ) (mV)	185.32	162.46	104.62	39.10
	Standard Deviation (σ) (mV)	13.66	13.63	13.62	12.19
	σ/μ (%)	7.37	8.39	13.02	31.17

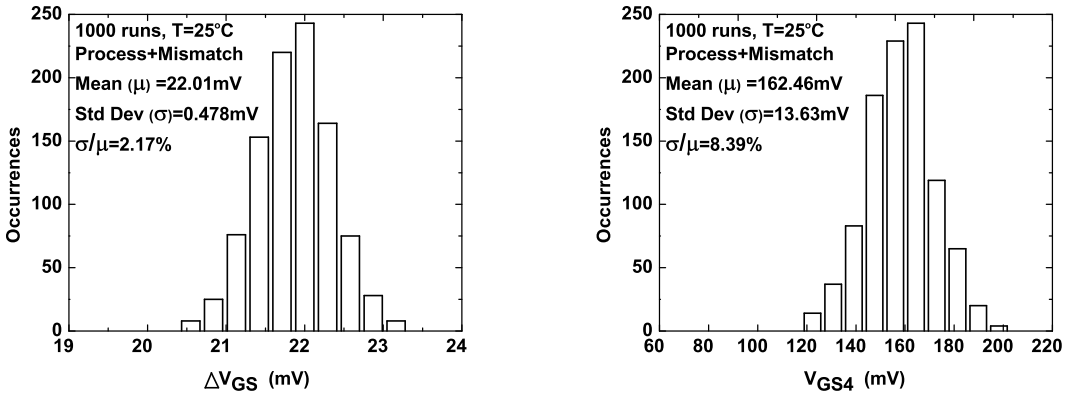
lid was used to shield the bonded die from the impact of airflow during thermal measurement. The package was placed into a zero-insertion-force (ZIF) socket soldered on a PCB. Thermal characterization was done using ThermoJet ES precision temperature cycling system from SP Scientific [228]. A thermal cap, covering the PCB, isolated the board from the exposure to the external environment. Voltage measurements were done using Keithley 2000 units. To minimize the loading effect of measurement equipment, buffers were placed between the PCB and the Keithley units [229] (see Fig. 3.9).

In addition to experimental evaluation, to further investigate the effects of mismatch and process variations, extensive Monte Carlo and corner simulations were run, with all passive devices (resistors and capacitors) and active devices (MOSFETs, SiGe HBTs and Si Vertical PNP devices) included. Simulation and experimental results for the compensation components as well the V_{REF} are presented and discussed in this section.

3.4.3.1 The I_{PTAT} Current

The PTAT current in this circuit was generated through the difference of the gate-source voltages (ΔV_{GS}) of two subthreshold-operating transistors (M_3 and M_4). To evaluate the effects of mismatch and process variation on ΔV_{GS}, Monte Carlo simulations (including process variations and mismatch) were run. Results at $T = 25$ °C are shown in Fig. 3.10-a, and are summarized for various temperatures in Table 3.3. It can be seen that the worst-case coefficient of variation (σ/μ) is 2.33% (obtained at $T = 0$ °C), indicating that mismatch and process variations have a negligible effect on ΔV_{GS}.

The I_{PTAT} current, generated by the ΔV_{GS} of two subthreshold-operating MOSFETs, was also experimentally evaluated using a test structure that was included in the circuit (see



(a) (b)

Figure 3.10: Monte Carlo simulation results (1000 runs with SiGe HBTs, MOSFETs, Si Vertical PNPs, resistors and capacitors included) at T=25 °C for a) ΔV_{GS}, and b) V_{GS4}.

Fig. 3.8-Circuit 2). In this structure, the PTAT current from the BGR circuit is mirrored and flown through an external resistor R_{TEST}. The generated PTAT voltage across this resistor was measured over $[0 - 150]$ °C, via the V_{PTAT} bondpad. Voltage measurements were then converted into current. Measurement results are shown in Fig. 3.11, clearly demonstrating a PTAT behavior.

To further analyze the linearity of the measured I_{PTAT}, its percentage deviation from a linear line ($I_{PTAT_{\text{IDEAL}}}(T)$) described as

$$I_{PTAT_{\text{IDEAL}}}(T) = I_{PTAT}(0°\text{C}) + \frac{I_{PTAT}(150°\text{C}) - I_{PTAT}(0°\text{C})}{150 - 0} \times T, \tag{3.33}$$

was calculated, following

$$\%I_{PTAT_{\text{ERROR}}}(T) = \frac{I_{PTAT_{\text{IDEAL}}}(T) - I_{PTAT}(T)}{I_{PTAT_{\text{IDEAL}}}(T)} \times 100. \tag{3.34}$$

Results are plotted in Fig. 3.11. The percentage deviation from linearity for the measured I_{PTAT} stays below 0.12% over the temperature range of interest. This result along with Monte Carlo simulations validate the feasibility of using subthreshold-operating MOSFETs to generate the PTAT components for the cancelation of the linear term, and are also of interest to subthreshold-based circuit designers.

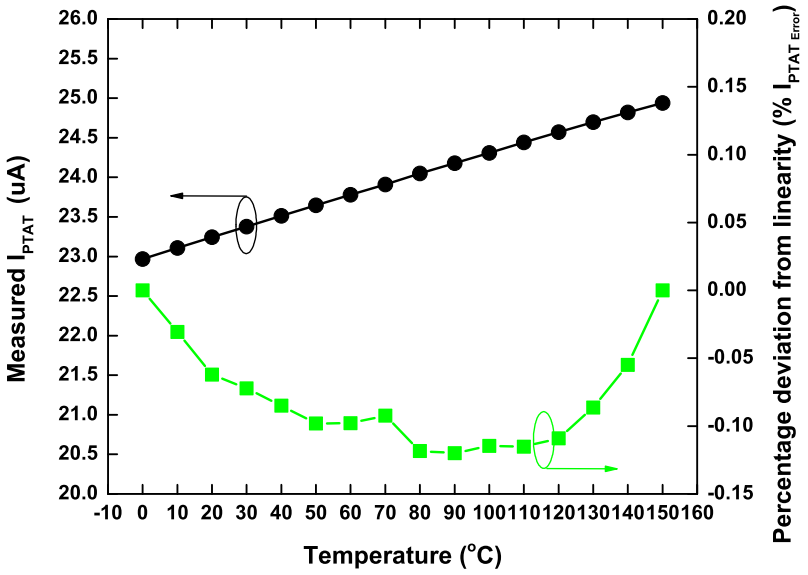


Figure 3.11: Measured I_{PTAT} and its percentage deviation from linearity as a function of temperature.

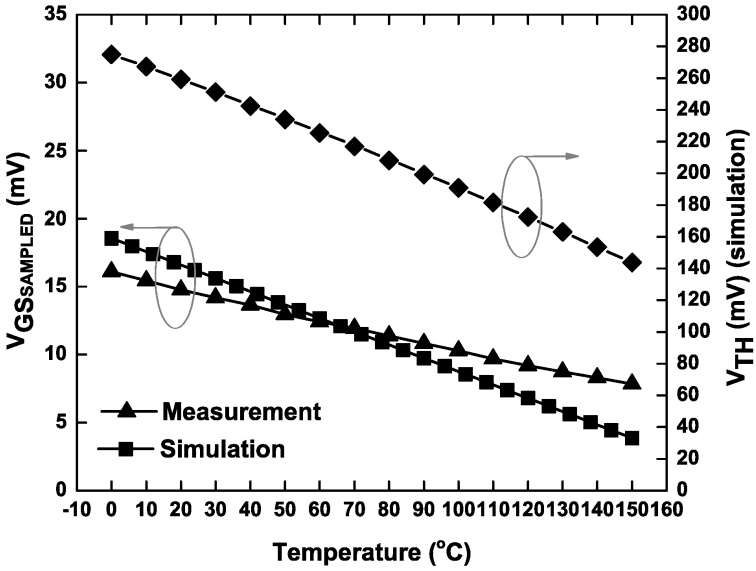


Figure 3.12: Simulated and measured $V_{GS_{\text{SAMPLED}}}$ and simulated V_{TH} as a function of temperature.

Table 3.4: TC at transistor corners.

	TT	SS	FF	SF	FS
TC across (0:150) °C (ppm/°C)	3.0	4.1	8.1	2.5	11.8

3.4.3.2 The $I_{V_{GS}}$ Current

As it was shown in Section 3.4.1 (both theoretically and through simulations), the V_{GS} of a subthreshold-operating MOSFET biased with a PTAT current, includes a term with $T\ln(T)$ behavior. This voltage was then used to generate the current $I_{V_{GS}}$, to cancel the $T\ln T$ in $I_{V_{BE}}$.

To examine the effect of mismatch and process variation on V_{GS}, Monte Carlo simulations were run for V_{GS4}. Results at $T = 25$ °C are shown in Fig. 3.10-b, and for various temperatures are summarized in Table 3.3. It can be seen that the coefficient of variation (σ/μ) is higher than what was observed for ΔV_{GS} and it increases with temperature. To compensate for this variation, a trimming network is necessary to be included.

We further experimentally examined the temperature response of V_{GS4}. Resistor R_2 in Fig. 3.5 was implemented by two series-connected resistors (R_{2_1} and R_{2_2}), with *1:9* ratio. Through the $V_{GS_{\text{SAMPLED}}}$ bondpad (see Fig. 3.8), the voltage across resistor R_{2_1} was measured over the target temperature range. This voltage represents $1/10$ of the actual V_{GS} value of transistor M_4.

Simulation and measurement results for $V_{GS_{\text{SAMPLED}}}$ are shown in Fig. 3.12, which clearly demonstrate the negative temperature dependency of the V_{GS}. While there are expected differences between the measurement and simulation results (due to process variations, and errors during measurement caused by package stress and loading effects), the outcomes are fairly close. To ensure that transistor M_4 has maintained operating in the subthreshold region across the intended temperature range, in the same figure, we also have included simulated values for the threshold voltage ($V_{TH_{\text{SIMULATED}}}$) at different temperature points. It can be seen that the difference between $V_{TH_{\text{SIMULATED}}}$ and V_{GS4} ($= 10 \times V_{GS_{\text{SAMPLED}}}$) remains larger than 100 mV across the temperature, showing that the transistor indeed maintained its subthreshold-operating status across the temperature range of [0-150] °C. Note that due to the limited number of measurement points, a similar approach discussed in Section 3.4.1 (i.e. taking the derivative of V_{GS}

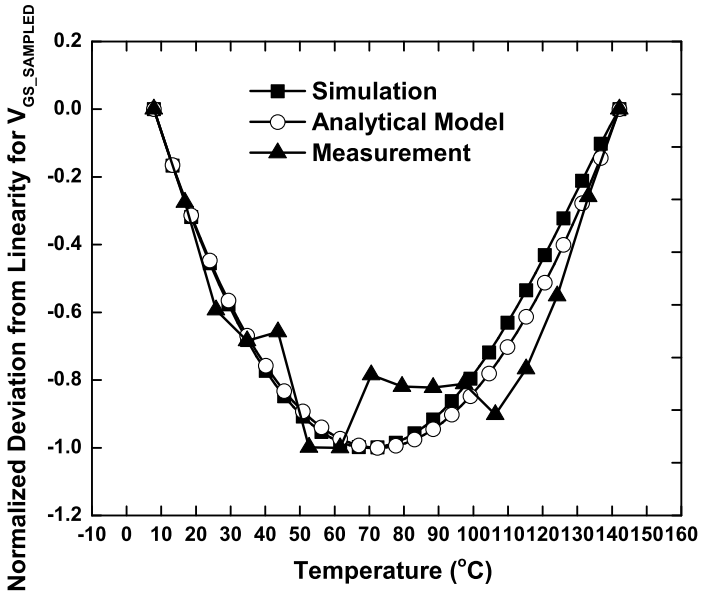
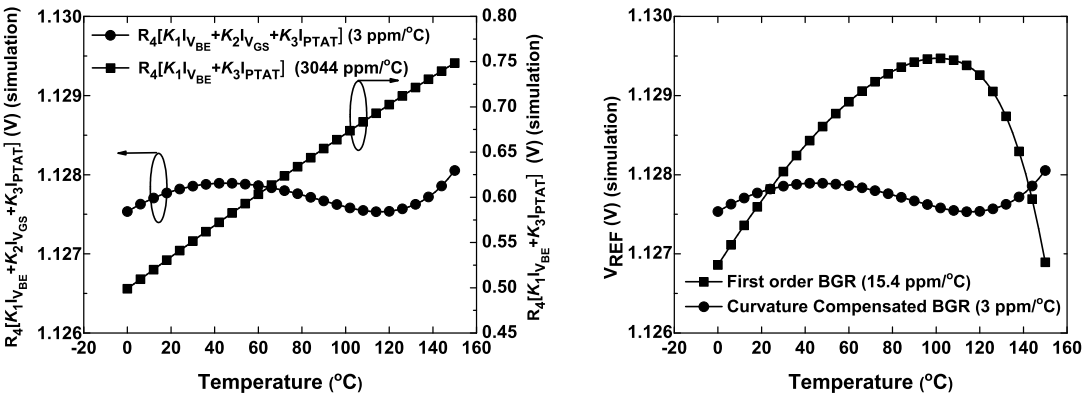


Figure 3.13: Normalized deviation from linearity for simulated and measured $V_{GS_{\text{SAMPLED}}}$, as well as for $1/10$ analytical estimation of V_{GS}.

numerically with respect to temperature), can not be taken to evaluate its nonlinearity. Normalized deviation from linearity for simulation and measured results are shown in Fig. 3.13. Here we are also showing normalized deviation from linearity obtained from the analytical model for V_{GS} obtained from (3.21). The parameters in (3.21) were estimated from the literature. Because of different scaling levels across three curves, curves were normalized to their minimum value, for the purpose of visualization. Results confirm the presence of nonlinear terms in all three cases.

3.4.3.3 The Output Voltage V_{REF}

Fig. 3.14-a shows simulation results for V_{REF} as a function of temperature. To show the effectiveness of the proposed curvature compensation technique, also shown in this figure are the simulation results for V_{REF} for the case when the $I_{V_{GS}}$ is excluded. It can be seen that the inclusion of the $I_{V_{GS}}$ significantly impacts the TC performance. Fig. 3.14-b compares the performance of the compensated circuit with that of an optimally designed first-order circuit (where the coefficients of I_{PTAT} and $I_{V_{BE}}$ are tuned to obtain an optimum first-order BGR with the nominal voltage equal to that of the designed compensated BGR). It can be seen that



(a) (b)

Figure 3.14: Simulation results for V_{REF} of a) the reference circuit employing the proposed compensation approach, with and without $I_{V_{GS}}$, and b) an optimally-designed first-order BGR, and the reference circuit employing the proposed compensation approach.

by the inclusion of the $I_{V_{GS}}$, the curvature compensated circuit achieves a much improved TC (more than 5 times better).

To investigate the effects of mismatch and process variation on V_{REF} Monte Carlo simulations were run with all components (SiGe HBTs, MOSFETs, Si Vertical PNPs, resistors and capacitors) included, and results at four temperature points are shown in Fig. 3.15. The worst-case coefficient of variation (σ/μ) is 2.21% obtained at $T = 150$ °C. Despite variations that were observed in V_{GS4}, the circuit demonstrates a reasonably robust performance against mismatch and process variations.

Table 3.4 summarizes the simulation results for MOS transistors corners. The circuit achieves a TC of less than 11.8 $ppm/$°C in the worst-case, indicating that the circuit is reasonably robust against corner variations.

To evaluate the effects of mismatch and process variations on TC of the first order BGR and the proposed curvature compensated BGR, we performed Monte Carlo simulation of 1000 runs considering both mismatch and process variations (with SiGe HBTs, MOSFETs, Si Vertical PNPs, resistors and capacitors included) at 0 °C, 30 °C, 60 °C, 90 °C, 120 °C, and 150 °C. Figs. 3.16-a and 3.16-c illustrate V_{REF} as a function of temperature for the first order and the curvature compensated BGR circuits, respectively. Figs. 3.16-b and 3.16-d show the histogram

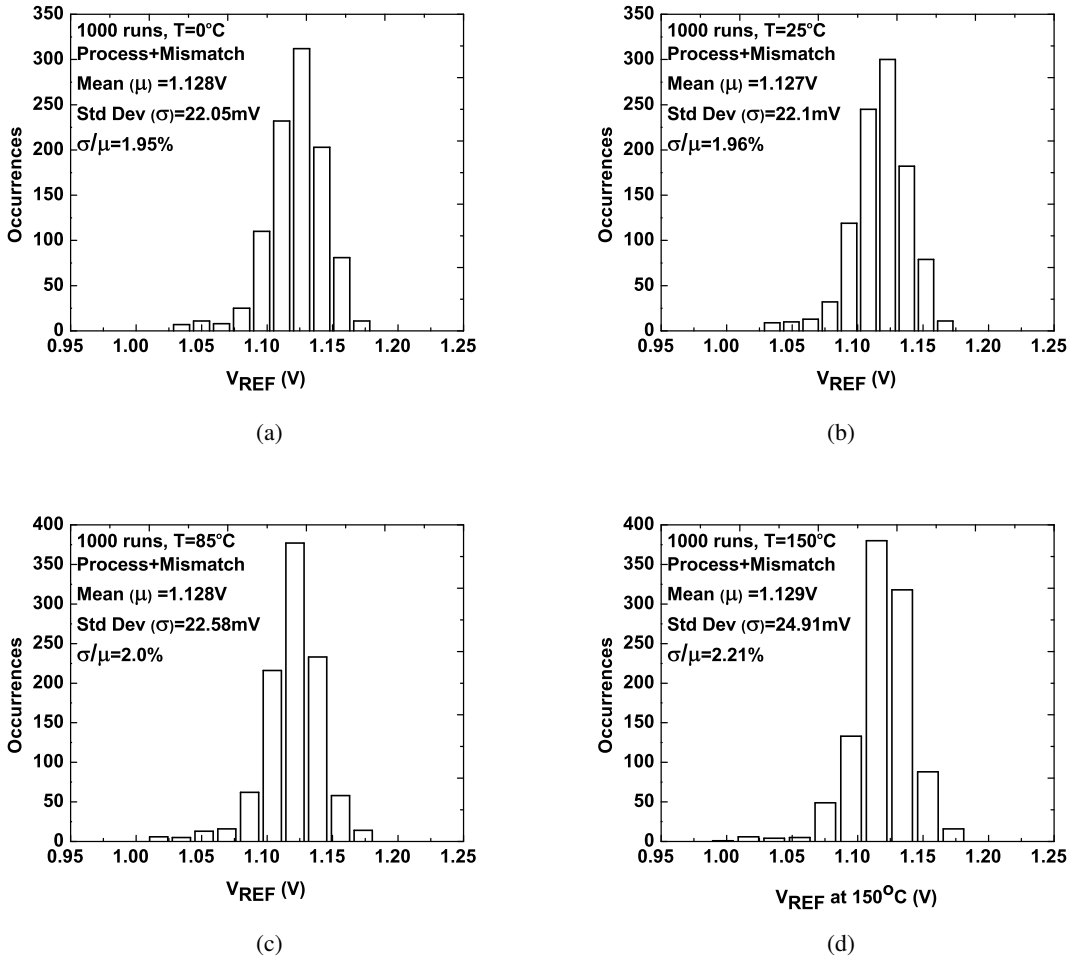


Figure 3.15: Monte Carlo simulation results (1000 runs with SiGe HBTs, MOSFETs, Si Vertical PNPs, resistors, and capacitors included) for V_{REF} at a) 0 °C, b) 25 °C, c) 85 °C, and d) 150 °C.

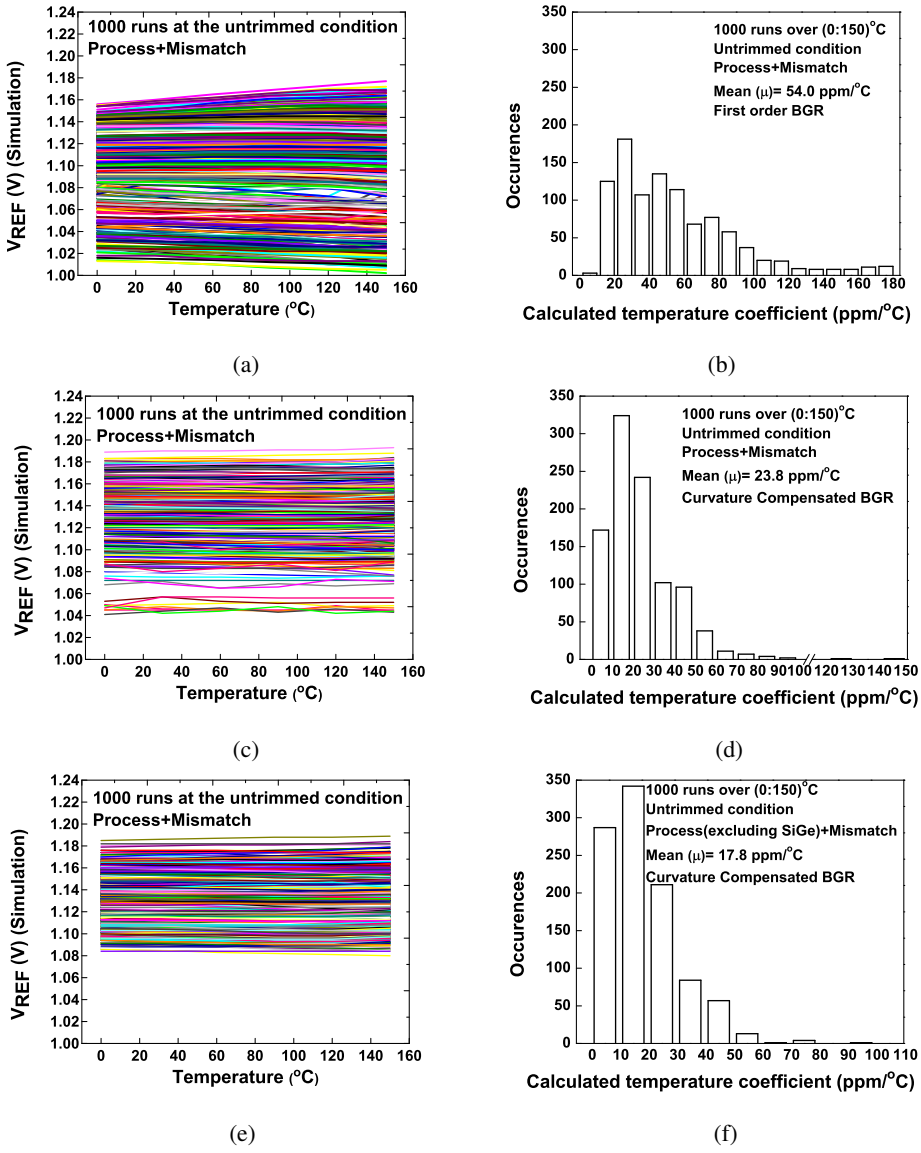


Figure 3.16: a) Monte Carlo simulation results (1000 runs, with SiGe HBTs, MOSFETs, Si Vertical PNPs, resistors and capacitors included) for first order BGR between 0 °C to 150 °C at the untrimmed condition, and b) the histogram of the calculated TC from (a). c) Monte Carlo simulation results (1000 runs, with SiGe HBTs, MOSFETs, Si Vertical PNPs, resistors and capacitors included) for V_{REF} of the proposed curvature compensated BGR between 0 °C to 150 °C at the untrimmed condition, and d) the histogram of the calculated TC from (c). e) Monte Carlo simulation results (1000 runs, with SiGe HBTs excluded) for V_{REF} of the proposed curvature compensated BGR between 0 °C to 150 °C at untrimmed condition, and f) the histogram of the calculated TC from (e).

Table 3.5: Comparison of Untrimmed and Trimmed Monte Carlo Simulation Results

Reference Circuit	**Mean TC across** 1000 **runs** (ppm/°C)	**% of Samples with TC**< 20 **ppm/°C**	**% of Samples with TC**> 50 **ppm/°C**
Untrimmed First Order BGR (including mismatch + all components in process variation)	54.0	12.8%	44.9%
Untrimmed Curvature Compensated BGR (including mismatch + all components in process variation)	23.8	49.6%	6.4%
Trimmed Curvature Compensated BGR (including mismatch + all components in process variation)	9.7	91.3%	1.8%

of the calculated TC over 1000 simulation runs, for the first order and the curvature compensated BGR circuits, respectively. The TC was calculated for $T_0 = 30$ °C, and over $[0-150]$ °C. Across 1000 runs, an average TC of 54.0 ppm/°C is achieved for the first order BGR, while this number is significantly reduced to 23.8 ppm/°C for the proposed curvature compensated BGR. The calculation of the coefficient of variation is not applicable here as Sigma is not meaningful in non-Gaussian distributions [213]. Variations are always expected in Monte Carlo simulations [213, 230], but comparing Figs. 3.16-b and 3.16-d, the number of samples showing large TC are significantly lower for the proposed curvature compensated BGR, as compared to the first order BGR. For example, 44.9% of samples show TC> 50 ppm/°C in the first order BGR, while only 6.4% of samples show TC> 50 ppm/°C for the proposed compensated BGR. Note that these Monte Carlo simulation results are obtained in the most general case where mismatch and process variations for all components (SiGe HBTs, MOSFETs, Si Vertical PNPs, resistors, and capacitors) are included. These results, along with the nominal simulation results shown in Fig. 3.14-b provide convincing evidence that the proposed curvature compensation approach outperforms the first-order BGR in terms of temperature stability and precision.

The curvature compensated BGR circuit includes subthreshold-operating MOS transistors, MOSFETs operating in the saturation region, Si Vertical BJTs and a SiGe HBT transistor. Therefore, a fair comparison with existing CMOS references cannot be made. Monte Carlo simulation results for the TC were also not available for other SiGe reference papers. To be able to do a relatively fair comparison with the state of the art CMOS reference circuits, we excluded

the SiGe HBTs in Monte Carlo simulations and ran simulations of 1000 runs with mismatch and process variation, and included MOSFETs, Si Vertical PNPs, resistors, and capacitors. Simulation results and the corresponding histogram for TC are shown in Figs. 3.16-e and 3.16-f, respectively. It can be seen that an average TC of 17.8 ppm/$^\circ$C is achieved across $[0-150]$ $^\circ$C, which is much smaller than what was observed in Fig. 3.16-d. Looking at equations (3.26), (3.27), (3.31) and (3.32), the dependence on Ge doping profile and Ge-induced bandgap offset can be seen. Therefore, removing SiGe HBTs from Monte Carlo simulation runs is expected to enhance the stability. In addition, only 1.9% of samples show TC>50 ppm/$^\circ$C in this case.

To investigate how trimming would improve the performance of the circuit, we further considered a subset of trimming options provided by the resistive network shown in Fig. 3.8, and performed Monte Carlo simulations. Considering the top three connections and the option of shorting resistor R_{2_1}, 1000 Monte Carlo simulations, including mismatch and process variation for all components, were run. The histogram of obtained TCs is shown in Fig. 3.17. As expected, compared to the untrimmed scenario, the TC in terms of the average and the range of variations, has been improved after trimming. The average TC across 1000 simulation runs after trimming is now 9.7 ppm/$^\circ$C with 91.3% of samples showing TC<20 ppm/$^\circ$C. The trimming performance, of course, can be further improved by considering more trimming options in the resistive network, and also by incorporating trimming networks for resistors R_1 and R_3. Table 3.5 summarizes the results presented in Figs. 3.16 and 3.17.

Table 3.6 compares the performance of Monte Carlo simulation results of the untrimmed proposed reference circuit, with the state of the art CMOS reference circuits that had reported their Monte Carlo simulation results for the untrimmed condition. In the table, we have included CMOS-based bandgap circuits, those that exploit zero temperature coefficient (ZTC) point, and those that have subthreshold devices. Note that there exist several CMOS reference circuits with improved TC (usually obtained after trimming), but their untrimmed Monte Carlo simulation results were not available to be included in this table. From this table, it can be seen that, in terms of TC, the untrimmed proposed compensation technique outperforms these circuits at untrimmed condition ($\approx$ twice reduction in TC compared to the best case, even when SiGe HBTs are included). This is achieved considering that for our case, the number of simulation runs is the largest, and the temperature range is wider (150 $^\circ$C) compared to most cases

Table 3.6: Performance comparison with untrimmed CMOS references (Monte Carlo simulations).

		This work	**[213]**	**[231]**	**[230]**	**[232]**
Year		2017	2015	2015	2017	2017
Technology (nm)		SiGe (130)	CMOS (90)	CMOS (65)	CMOS (65)	CMOS (180)
Bandgap/Subthreshold/ZTC		Bandgap/ Subthreshold	Bandgap	Subthreshold	ZTC	ZTC
Monte Carlo	**# of Runs**	1000	100	500	200	140
	Process/ Mismatch	both	both	both	N/A	both
	Mean V_{REF} at T_0 (V)	1.127	0.730	0.512	0.428	0.498
	Coefficient of Variation (%)	1.96	0.86	0.89	5.5	7.6
	Temperature Range (°C)	(0:150)	(0:100)	(-40:90)	(-40:125)	(-30:110)
	Mean TC (ppm/°C)	23.8(all) 17.8(no SiGe)	45.1	41.1	121	44.4

N/A:information not available.

in the table.

The measured trimmed output voltage of the reference circuit employing the proposed compensation technique, and operating with $1.6\ V$ power supply for three units coming from three wafers, as a function of temperature, is shown in Fig. 3.18. All measured units showed high stability with respect to temperature variation with unit 1 exhibiting the best TC ($9.9\ ppm/°$C across $[0-150]$ °C). The average TC across three units is $13.1\ ppm/°$C over $[0-150]$ °C. The observed difference in the nominal output voltage values across three units is most likely due to the variation in Ge doping level (and impacting $V_{G0,SiGe}$) and other process variations (e.g. V_{TH0} or α) across wafers, as each unit is coming from a different wafer.

A simple trimming procedure was followed. First, V_{REF} was observed across temperature with no resistor in the trimming network selected. Second, V_{REF} was observed across temperature with the bondpad $V_{GS_{SAMPLED}}$ in Fig. 3.8 shorted to the ground. Based on the results of these two cases, proper resistance in the trimming network was estimated to minimize the deviation across temperature. With this choice, V_{REF} was then measured across temperature. Other more effective trimming approaches such as those proposed in [187,230] can be incorporated to obtain an even better TC. Furthermore, note that here we only had the resistive network for the tuning of the $I_{V_{GS}}$. Additional trimming networks can be added for resistors R_1 and R_3 to adjust the I_{PTAT} and $I_{V_{BE}}$ currents as well, to achieve an even more highly stable output voltage.

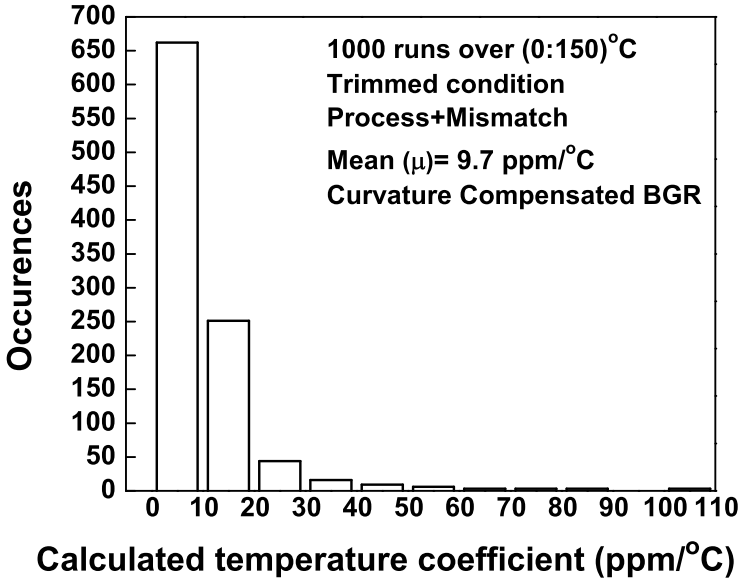


Figure 3.17: Histogram of TCs for 1000 runs obtained with considering the top three connections in the resistive network shown in Fig. 3.8. Mismatch and process variation (for all components) were included.

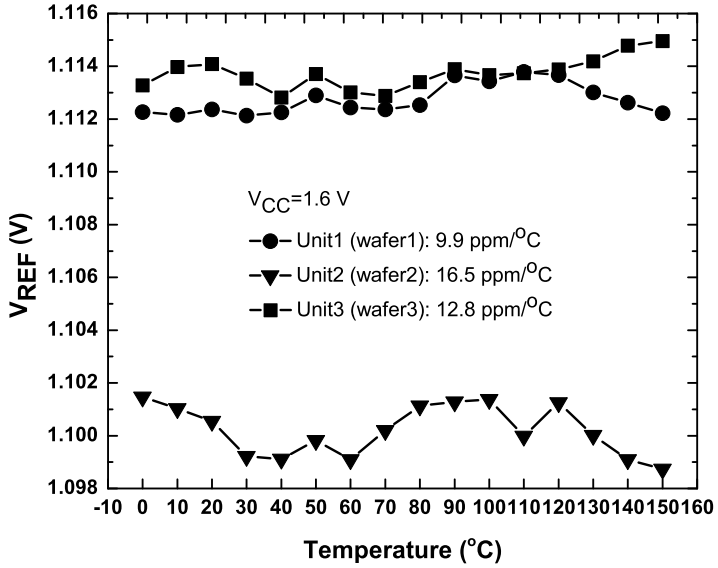


Figure 3.18: Experimental results for the trimmed output voltage of the voltage reference employing the proposed compensation solution for three units from three different wafers as a function of temperature.

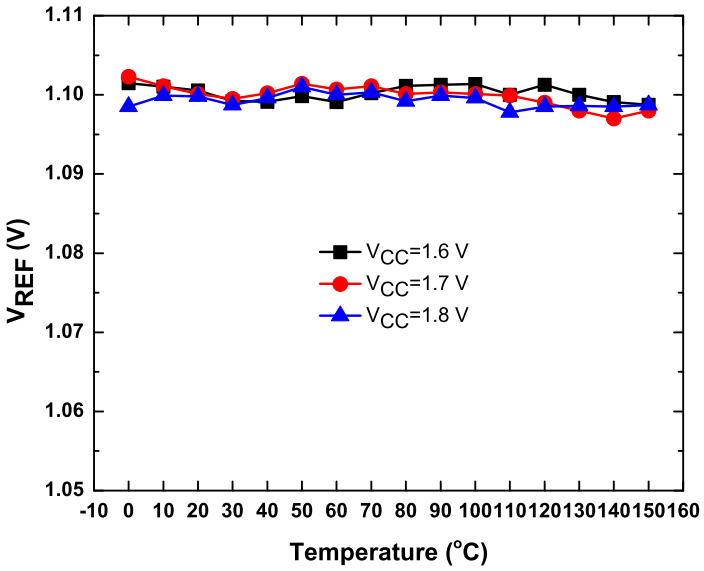


Figure 3.19: Measured output voltage (trimmed at $1.6\ V$) as a function of temperature for different supply voltages.

Fig. 3.19 shows the measured output voltage for unit 2 as a function of temperature, for the supply voltage ranging from $1.6\ V$ to $1.8\ V$. The unit was first trimmed at $1.6\ V$ supply voltage, and then measured at $1.7\ V$ and $1.8\ V$ supply voltages over the entire temperature range by preserving the same trimming option that was identified at $1.6\ V$. The proposed BGR circuit continues to exhibit high temperature stability when operating at different power supply voltage values. At room temperature, the reference circuit exhibits a line regulation of *0.24* $\%/V$ for supply voltage ranging from $1.6\ V$ to $1.8\ V$. The power supply rejection ratio (PSRR) of this BGR, measured at room temperature by Model 200 Frequency Analyzer from AP Instrument, is shown in Fig. 3.20. The circuit shows -40 dB PSRR at 10 Hz, and less than -36 dB at 100 Hz, which is comparable to what is reported in [184] and better than what is reported in [233] for a SiGe reference. The PSRR can be further improved by employing PSRR enhancement techniques such as the one proposed in [230, 234].

Fig. 3.21-a shows deviation in the output voltage of unit 2 from its mean, measured over 30 minutes, at room temperature, without using any output filtering capacitors. It can be seen that changes in the V_{REF} over time remains to be less than 0.028%. Fig. 3.21-b shows simulation results for the noise without any filtering capacitor. The simulated output noise spectral density

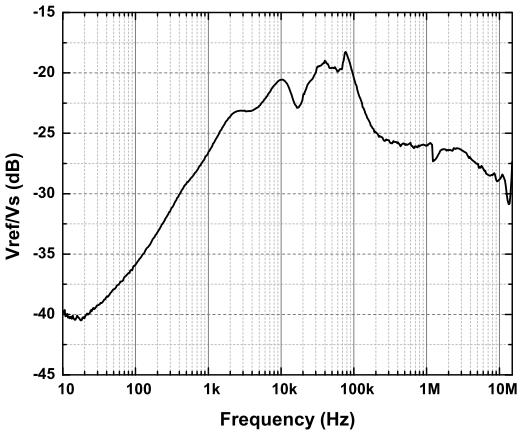


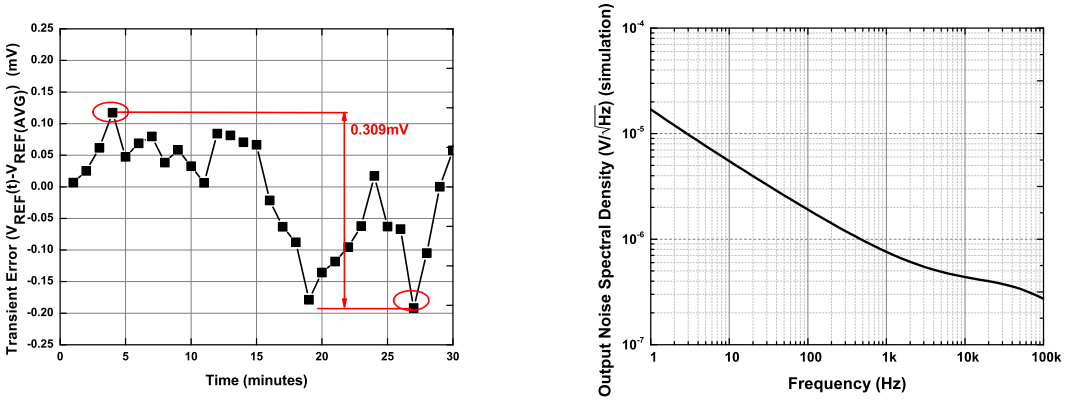
Figure 3.20: Measured PSRR at room temperature, with a 1.6 V supply, and without a filtering capacitor.

is 1.97 $\mu V/\sqrt{Hz}$ at 100 Hz. The noise spectral density can be further reduced by introducing a filtering capacitor [213].

Table 3.7 compares the performance of the proposed circuit with some of previously designed SiGe-based BGR circuits. The proposed reference circuit offers superior performance in terms of temperature stability and power consumption. Since the circuit was implemented in the SiGe technology platform, performance comparison with existing references implemented in Si technology platforms (CMOS, BJT) was not made here, due to differences in the technology. It is expected to see even a much better performance if the proposed compensation technique is realized in Si-based technology (compare (3.8) and (3.11)). This SiGe circuit in fact offers comparable performance (in terms of temperature stability) to Si-based circuits [183, 185, 186, 211, 235], despite technology differences (Si vs SiGe).

3.4.4 Discussion

In this section, we presented the theoretical basis along with simulation and experimental results for a new BiCMOS-based curvature compensation technique to achieve fully temperature-independent reference circuits. The introduction of a secondary design component with $T\ln(T)$ temperature dependency provides BGR designers with an option to achieve complete cancellation of the nonlinear term in $V_{BE}(T)$ and obtain a highly temperature-stable reference circuit.



(a) (b)

Figure 3.21: a) Measured output voltage over time at room temperature, and b) simulated output noise spectral density of the output without any buffer or filtering capacitor.

Table 3.7: Performance comparison with prior SiGe-based BGRs (Measurements).

	This work	**[236]-1**	**[236]-2**	**[157]**	**[233]**
Year	2017	2014	2014	2006	1998
SiGe Technology (nm)	130	90	90	500	350
Compensation	BiCMOS Curvature Correction	First-order	Inverse-Mode First-Order	Exponentially-Compensated	First-Order
$\mathbf{V_{CC}}$ (V)	1.6	2	2	3.3	2.5
Power Consumption (μ**W**)	288	640	556	458	1700
$\mathbf{V_{REF}}$@25 °C (V)	1.112	1.083 *	1.061 *	1.172	1.328
TC (ppm/°C)	9.9 (best) 13.1 (mean) (0:150)°C 3 samples	24 (-53:127)°C * 1 sample	43 (-53:127)°C 1 sample	28.1 (-180:27)°C 69.9 (-230:27)°C best of 3 samples	36.5 (-50:150)°C 25.1 (0:75)°C 1 sample

* Measured at pre-radiation condition

The contributions of this section are as follows: 1) we demonstrated for the first time, theoretically and through simulations, that $T\ln(T)$ temperature dependency exists in $V_{GS}(T)$ of subthreshold-operating MOSFET that is biased with a PTAT $I_D(T)$ current. We also presented measurement results for $V_{GS}(T)$ of a subthreshold-operating MOSFET and showed that the measured results closely follow theoretical derivations; 2) we presented a new BiCMOS compensation solution to directly cancel the $T\ln(T)$ dependency in $V_{BE}(T)$ using the $T\ln(T)$ dependency identified in $V_{GS}(T)$ of a subthreshold-operating MOSFET biased with a PTAT $I_D(T)$; 3) we, theoretically and experimentally, verified that a PTAT current can be generated through $\Delta V_{GS}(T)$ of two subthreshold-operating MOSFETs. Monte Carlo simulation results across various temperature points showed that mismatch and process variations have a negligible impact on $\Delta V_{GS}(T)$, and hence, the generated PTAT current; 4) as a proof of concept of the proposed compensation solution, a current-mode BGR was designed in SiGe BiCMOS technology. Design equations were derived, and simulation and measured results for the reference circuit were extensively presented, demonstrating that the circuit outperforms existing SiGe reference circuits in terms of TC, and 5) we identified differences in nonlinearities observed in $V_{BE}(T)$ of a Si BJT and $V_{BE}(T)$ of a SiGe HBT, and their impact on the proposed compensation solution.

The benefits of the proposed compensation solution can be summarized as follows: 1) it aims to directly cancel the nonlinearities in $V_{BE}(T)$; 2) it does not require temperature-independent currents for biasing the transistors (as was required in [187]), and it achieves compensation through biasing transistors with PTAT currents, which are already available in the circuit; 3) it can also be easily incorporated into existing first-order current-mode BGR circuits to further improve their thermal stability; 4) it is not limited to current-mode BGRs and can be utilized in voltage-mode BGR circuits as well; and 5) while we presented the results of a circuit implemented in a SiGe technology, it can be implemented in any BiCMOS/CMOS technology.

The measured results of the SiGe voltage reference presented here, while still demonstrating a highly temperature stable output and superior performance to existing SiGe circuits, revealed deviation from being fully temperature-independent. One reason for the observed deviation is that the $I_{V_{BE}}$ current was generated from the base-emitter voltage of the SiGe HBT, as expressed in (3.11). Several terms exist there that depend on the Ge doping profile and Ge-induced

bandgap offset. We neglected the temperature dependencies of these parameters. In addition, we neglected the temperature variation in (3.11) introduced by the "nonlinear 2" component. The temperature dependencies of these parameters have likely played roles in causing deviation from achieving complete thermal stability. In fact, comparing the expressions of $V_{BE,BJT}(T)$ and $V_{BE,HBT}(T)$ ((3.8) and (3.11)), we believe that if the proposed approach is implemented in Si technology (either BiCMOS or in CMOS by utilizing lateral or vertical BJTs) the Si-based reference circuit will achieve a much better performance in terms of temperature stability. Lack of accurate models for technology parameters in the simulator when designing the circuit could also be the reason for the observed deviation in post-fabricated measurements. In addition, in deriving the theoretical basis for the compensation approach, we assumed $V_{TH}(T)$ is a linear function of temperature [203, 213]. Depending on the technology, the high-order temperature dependency of $V_{TH}(T)$ could contribute to the deviation in V_{REF} from being fully temperature independent.

To address these issue, as well as the issue of sensitivity of subthreshold-operating transistors to process variations, trimming networks should be incorporated. In our design, we included a simple trimming network for adjusting the $I_{V_{GS}}$ current only. Additional trimming networks can be added for resistors R_1 and R_3 to adjust the I_{PTAT} and $I_{V_{BE}}$ currents as well, and more effective trimming procedures [187, 230] can be employed, to achieve a highly stable output voltage.

3.5 A SiGe Reference Circuit Utilizing Si and SiGe Bandgap Voltage Differences

As mentioned in Section 3.2.1, in IBM's SiGe BiCMOS 8HP technology platform, the designer has access to SiGe NPN HBTs as well as substrate-isolated Si VPNP transistors, in addition to conventional CMOS transistors. Compared to Si-based technology, in SiGe BiCMOS technology, a relatively smaller amount of work exists for reference circuits. A first-order temperature compensated BGR circuit was realized in [233] to demonstrate the feasibility of this technology for implementing BGRs. The influence of Ge grading on the temperature characteristics of SiGe-based reference circuits was investigated in [157, 237], demonstrating that Ge grading can impact the accuracy of references. Temperature characteristics of the current gain (β) of

SiGe HBTs was also exploited in [160, 226], for high-order temperature compensation. Recently, HBTs operating in their inverse-mode region were also utilized for realizing reference circuits [236]. While these circuits have been shown to operate reliably at temperatures as low as 1 K [226], their accuracy has not yet reached the level of their Si-based BGR counterparts.

In this section, a new compensation technique for SiGe reference circuits is presented to improve their thermal stability. The proposed technique is motivated by two key observations: the existence of two $p-n$ junctions in SiGe technology platforms-the Si-Si $p-n$ junction (through vertical PNP (VPNP) devices) and the SiGe-Si $p-n$ junction (through NPN HBTs); and the dependency of temperature-induced nonlinearities of V_{BE} on the temperature order of the collector current. As the source of the curvature appearance in the thermal characteristics of reference circuits is due to the fact that the temperature-dependent nonlinearities in V_{BE} are not completely canceled across the temperature range of interest, the proposed approach utilizes both Si-Si and SiGe-Si junctions, which exhibit similar temperature-dependent nonlinearities, under specific biasing conditions, to perform temperature compensation. Here, the compensation concept and extensive theoretical discussions are presented, and experimental results are provided. Furthermore, it is shown that the proposed reference circuit generates an output voltage that is related to the difference in the bandgap voltages of Si and SiGe. As such it can also be utilized to experimentally estimate the Ge-induced bandgap offset in a given SiGe technology.

3.5.1 Proposed Compensation Technique

To describe the proposed compensation technique, the temperature characteristics of Si BJTs presented in Section 3.2.3 and SiGe HBTs in Section 3.2.4 will be used. As discussed in Section 3.2.4, if the second nonlinear term in (3.11) is neglected, one can see that both $V_{BE,BJT}$ and $V_{BE,HBT}$ share similar temperature dependent terms: $\propto T$ and $\propto [T\ln(T)]$ by comparing (3.8) and (3.11).

The presence of similar temperature-dependent nonlinear term in both $V_{BE,BJT}$ and $V_{BE,HBT}$ suggests that through proper biasing (θ_{BJT} and θ_{HBT}) of the two transistors and appropriately weighted subtraction of the two junction voltages, the nonlinear term $[T\ln(T)]$ can be canceled.

Fig. 3.22 shows the deviation from linearity for the base-emitter voltage of a Si BJT and a

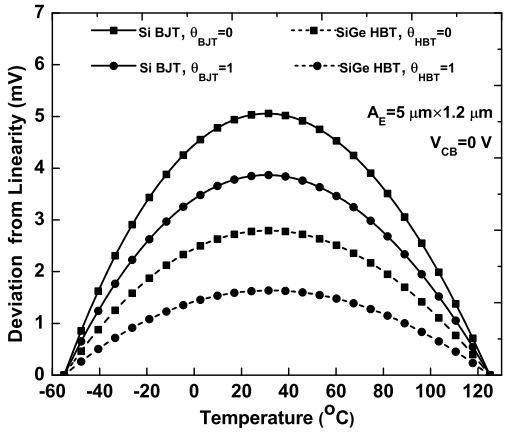


Figure 3.22: Simulated deviation from linearity in $V_{BE,BJT}$ and $V_{BE,HBT}$ for different biasing conditions: constant I_C and PTAT I_C.

SiGe HBT (with identical emitter areas) versus temperature for two different biasing conditions (collector current being temperature independent, and collector current being PTAT), obtained through simulations. The deviation from linearity was obtained by drawing a line between V_{BE}s at the two temperature ends, and then subtracting this line from simulated data [237]. The figure indicates that the deviation from linearity in both transistors decreases as the order of the temperature dependency of the collector current increases. In addition, one can see the deviation from linearity of the BJT is closest to that of HBT if the BJT is biased with temperature independent collector current and the HBT is biased with a PTAT collector current.

The expression for the weighted subtraction of the two voltages is described as

$$\begin{aligned} &\alpha_1 V_{BE,BJT}(T) - \alpha_2 V_{BE,HBT}(T) \qquad (3.35)\\ &= \underbrace{[\alpha_1 V_{G0,Si} - \alpha_2 V_{G0,SiGe}]}_{\substack{\text{weighted difference}\\ \text{of bandgap voltages}}} - \underbrace{[\alpha_1 A_1 - \alpha_2 A_2]}_{\substack{\text{weighted difference}\\ \text{of linear terms}}} T \\ &\quad \underbrace{- \frac{k}{q}[\alpha_1(\eta - \theta_{BJT}) - \alpha_2(l - \theta_{HBT} - 1)][T\ln(T)]}_{\text{weighted difference of nonlinear terms}}, \end{aligned}$$

where A_1 and A_2 represent the coefficients of the linear term ($\propto T$) in (3.8) and (3.11), respectively. Note that due to the inclusion of the graded Ge into the base of SiGe HBTs, $V_{G0,SiGe}$ is a smaller value than $V_{G0,Si}$.

We now summarize the proposed two-step compensation technique to minimize the temperature dependency of SiGe reference circuit.

Step 1. The temperature characteristics of the biasing currents (θ_{BJT} and θ_{HBT}) and the weighted subtraction coefficients α_1 and α_2, are set such that the coefficient of the nonlinear term $[T\ln(T)]$ is set to zero, i.e.,

$$\frac{\alpha_1}{\alpha_2} = \frac{l - \theta_{HBT} - 1}{\eta - \theta_{BJT}}. \tag{3.36}$$

Equation (3.36) depends on parameters η and l, which are typically between 3 and 4 [237]. As a rough estimate, if we assume $\eta = l$, to keep the ratio in (3.36) a positive value, the order of the temperature dependency of the $I_{C,HBT}$ (i.e. θ_{HBT}) needs to be set to be smaller by one unit than that of $I_{C,BJT}$ (i.e. θ_{BJT}). For example, if the collector current of the Si BJT, is designed to be PTAT (i.e. $\theta_{BJT} = 1$ in (3.7)), then $I_{C,HBT}$ needs to be temperature independent (i.e. $\theta_{HBT} = 0$ in (3.9)). A temperature independent current, to the first-order, can be generated through the summation of a PTAT current and a CTAT current. Alternatively, the BJT can be biased with a PTAT^2 current (i.e. $\theta_{BJT} = 2$), while the HBT is biased with a PTAT current (i.e. $\theta_{HBT} = 1$).

Step 2. In the second step, the linear term in (3.35) will be canceled. This can be achieved through the addition of a PTAT component such that the linear coefficient of the PTAT current (α_3) is set so

$$\alpha_3 = \alpha_1 A_1 - \alpha_2 A_2. \tag{3.37}$$

Once the temperature-dependent parameters in (3.35) are canceled, a temperature-independent output voltage related to the weighted subtraction of the two bandgap voltages of Si and SiGe, is obtained. Note that, in this step, for the complete cancellation to be realizable through the addition of the PTAT component, one has to make sure the coefficient $[\alpha_1 A_1 - \alpha_2 A_2]$ in (3.35) remains positive after the direct cancellation of the nonlinear terms. Using (3.36), and denoting $C_1 = \frac{V_{G0,Si} - V_{BE0_{BJT}}}{T_0}$, $C_2 = \frac{V_{G0,SiGe} - V_{BE0_{HBT}}}{T_0}$, and $C_3 = \frac{\Delta E_{g,Ge(grade)}}{\Delta E_{g,Ge(grade)_0}}[1 - \exp\left(\frac{-\Delta E_{g,Ge(grade)_0}}{kT_0}\right)]$ in (3.11), $[\alpha_1 A_1 - \alpha_2 A_2]$ can be expressed as

$$[\alpha_1 A_1 - \alpha_2 A_2] = \alpha_1[C_1 - \frac{\eta - \theta_{BJT}}{l - \theta_{HBT} - 1} C_2] + \frac{k}{q}\alpha_1 \frac{\eta - \theta_{BJT}}{l - \theta_{HBT} - 1}\ln(C_3). \tag{3.38}$$

The choice of emitter area for Si BJT and SiGe HBT and their collector currents (defining $V_{BE0_{BJT}}$ and $V_{BE0_{HBT}}$) should then be made in a way that (3.38) remains a positive value.

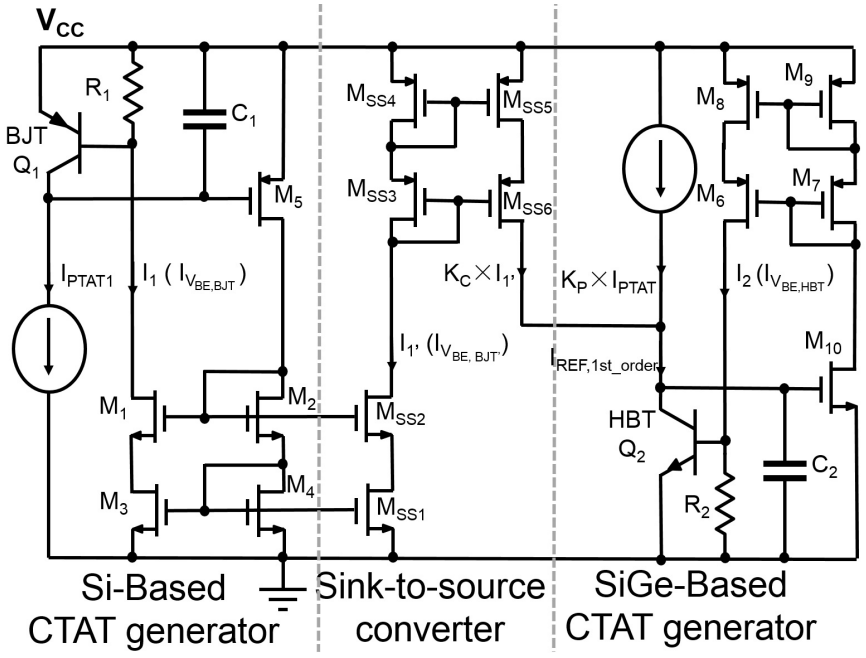


Figure 3.23: Schematic of the Si-based and SiGe-based current generator circuits.

3.5.2 Design Example

In this section, the design of a current-mode reference circuit utilizing the proposed temperature compensation technique is described. The circuit consists of four main circuit blocks: the Si-based current generator, the SiGe-based current generator, the PTAT current generator, and the V_{REF} generator. Without loss of generality, for the realization of the step 1 of the proposed solution, in this design the BJT is biased with a PTAT current (i.e. $\theta_{BJT} = 1$) and the HBT is biased with a temperature-independent current (i.e. $\theta_{HBT} \approx 0$).

3.5.2.1 Si-Based Current Generator

The schematic of the Si-based current generator is shown on the left side of Fig. 3.23. A VPNP transistor (Q_1) is biased by a PTAT current I_{PTAT1}. The PTAT current generator circuit will be discussed in Section 3.5.2.3 . The base-emitter voltage of Q_1 falls across resistor R_1, generating current I_1 related to the V_{EB} of Q_1 as

$$I_1(T) = \frac{V_{EB,Q_1}(T)}{R_1} = I_{V_{BE,BJT}}(T), \tag{3.39}$$

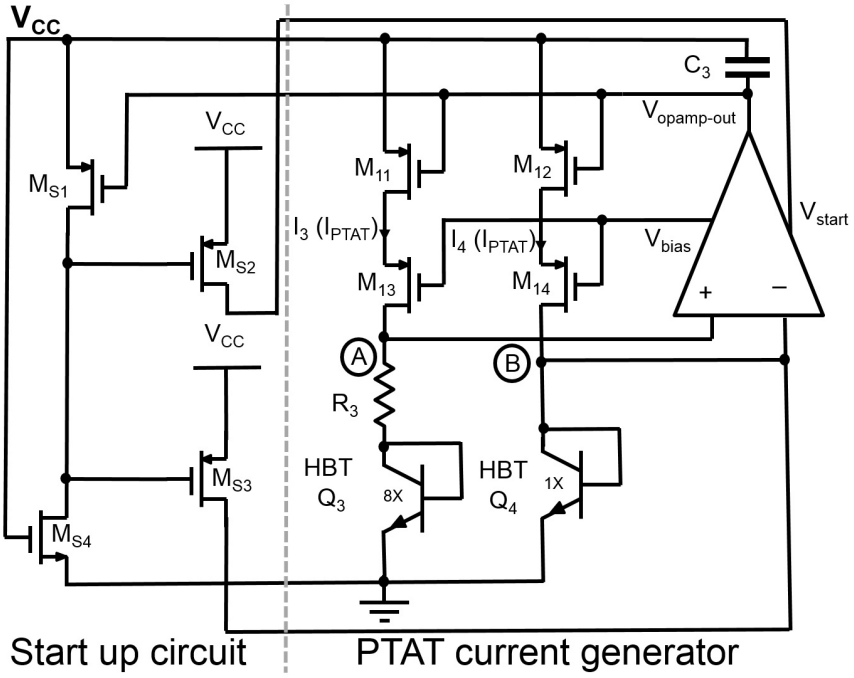


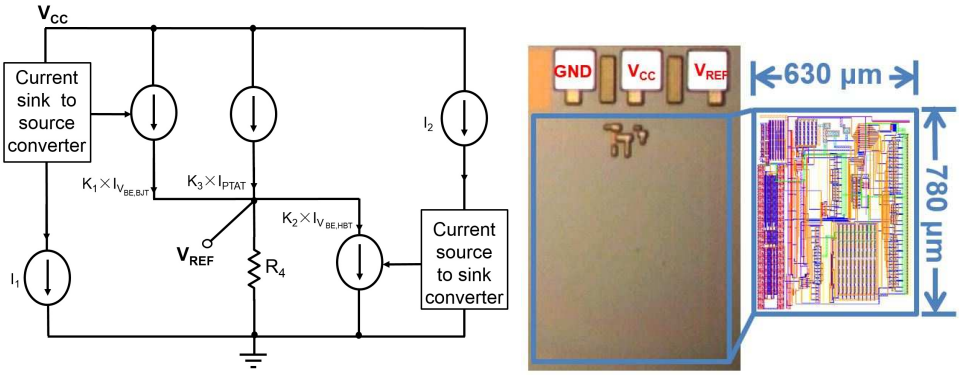
Figure 3.24: Schematic of the startup and the PTAT current generator circuits.

where $V_{EB,Q1}(T)$ follows (3.8) with $\theta_{BJT} = 1$. Transistors M_1-M_2 and M_3-M_4 form a cascode current mirror, and M_5 is the feedback transistor [210]. Capacitor C_1 is added in the circuit to stabilize the loop.

3.5.2.2 SiGe-Based Current Generator

The schematic of the SiGe-based current generator circuit is shown on the right side of Fig. 3.23. The operation of this circuit is similar to that of the Si-based current generator discussed above, except that the HBT (Q_2) is now biased with a current ($I_{REF,1st\_order}$) that is temperature independent to the first order (i.e. $\theta_{HBT} \approx 0$). This current is generated through the weighted addition of the PTAT current and the current generated through the Si-based current generator ($I_{1,}$), which decreases as the temperature increases. Proper weights (K_c and K_p) are realized through the aspect ratio of the transistors used in the current mirrors. A sink to source current converter, consisting of transistors M_{SS1}-M_{SS6}, is used for the current conversion. The base-emitter voltage of HBT Q_2 falls across resistor R_2, generating current I_2 as

$$I_2(T) = \frac{V_{BE,Q_2}(T)}{R_2} = I_{V_{BE,HBT}}(T), \tag{3.40}$$



(a) (b)

Figure 3.25: a) schematic of the V_{REF} generator circuit, and b) die microphotograph of the circuit.

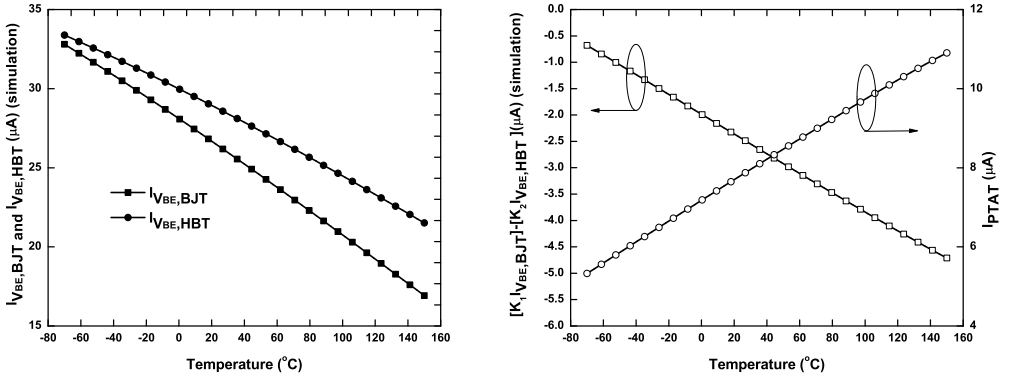
where $V_{BE,Q_2}(T)$ follows (3.11) with $\theta_{HBT} \approx 0$.

3.5.2.3 PTAT Current Generator

The schematic of the PTAT current generator with its startup circuit [218] (consisting of transistors M_{S1}-M_{S4}) is shown in Fig. 3.24. The core of the PTAT current generator (right side of Fig. 3.24) consists of MOSFET transistors M_{11}-M_{14}, HBTs Q_3 and Q_4, and the resistor R_3. The PTAT current circuit can be also made using BJTs. We have used HBTs, since they offer significantly higher current gain compared to BJTs, to minimize the influence of base currents. In this circuit, a folded-cascode op-amp with large DC gain [187] is designed to enforce identical voltage levels at the inverting and noninverting input terminals (nodes *A* and *B*), ensuring that the currents I_3 and I_4 are identical. The emitter area of transistor Q_3 is designed to be eight times larger than that of Q_4. The difference between the base-emitter voltages of the two transistors falls across the resistor R_3, generating PTAT currents I_3 and I_4 following [157]

$$I_3(T) = \frac{V_{BE,Q4}(T) - V_{BE,Q3}(T)}{R_3} = \frac{k\ln(n)}{qR_3}T = I_{PTAT}(T), \tag{3.41}$$

where n represents the emitter area ratio of transistors Q_3 and Q_4 (here $n = 8$).



(a) (b)

Figure 3.26: Simulation results for a) $I_{V_{BE,BJT}}$ and $I_{V_{BE,HBT}}$, and b) I_{PTAT}, and the weighted subtraction of $I_{V_{BE,BJT}}$ and $I_{V_{BE,HBT}}$ (right).

3.5.2.4 V_{REF} Generator

After the generation of the Si-based, the SiGe-based, and the PTAT currents, a circuit needs to be implemented to properly add the PTAT current to the weighted subtraction of the Si-based and SiGe-based currents, so a temperature-independent output voltage is generated. As discussed, the nonlinear temperature-dependent components are canceled through the weighted subtraction of Si-based and SiGe-based currents, and the remaining linear temperature-dependent component is canceled through the addition of the PTAT current.

Fig. 3.25 shows the simplified schematic of the V_{REF} generator circuit. Mirrored versions of the Si-based current and the PTAT current will be added properly together at node V_{REF}, while a portion related to the SiGe-based current, will be taken away to implement the weighted subtraction step. As such, $V_{\text{REF}}(T)$ is expressed as

$$\begin{aligned} V_{\text{REF}}(T) &= R_4[K_1 I_{V_{BE},BJT}(T) - K_2 I_{V_{BE},HBT}(T) + K_3 I_{PTAT}(T)] \\ &= \underbrace{[K_1 \frac{R_4}{R_1}]}_{\alpha_1} V_{EB,BJT}(T) - \underbrace{[K_2 \frac{R_4}{R_2}]}_{\alpha_2} V_{BE,HBT}(T) + \underbrace{[K_3 \frac{R_4 k \ln(n)}{q R_3}]}_{\alpha_3} T, \end{aligned} \tag{3.42}$$

where K_1, K_2 and K_3 are determined by the aspect ratio of the corresponding mirroring transistors.

We now proceed with finding the required design equations such that V_{REF} becomes a temperature stable voltage. Following (3.36), to cancel the nonlinear temperature-dependent component we will have

$$\frac{\alpha_1}{\alpha_2} = \frac{K_1}{K_2}\frac{R_2}{R_1} = \frac{l - \theta_{HBT} - 1}{\eta - \theta_{BJT}}. \tag{3.43}$$

Since in this design, $\theta_{HBT} \approx 0$ and $\theta_{BJT} = 1$, and assuming $l \approx \eta$, (3.43) simplifies to

$$\frac{K_1}{K_2} = \frac{R_1}{R_2}. \tag{3.44}$$

To cancel the linear temperature-dependent term, α_3 in (3.42) should be set such that (3.37) is satisfied. Assuming $\theta_{BJT} = 1$, $\theta_{HBT} \approx 0$, and $l \approx \eta$, the equation for canceling the linear term is obtained as

$$\frac{K_3}{K_1} = \frac{qR_3}{k\ln(n)R_2}\left[\frac{V_{G0,Si} - V_{G0,SiGe} - V_{BE0_{BJT}} + V_{BE0_{HBT}}}{T_0} + \frac{k}{q}\ln\left(\frac{\Delta E_{g,Ge(grade)}}{\Delta E_{g,Ge(grade)_0}}\left[1 - \exp\left(\frac{-\Delta E_{g,Ge(grade)_0}}{kT_0}\right)\right]\right)\right]. \tag{3.45}$$

Once conditions (3.44) and (3.45) are satisfied, the output voltage, related to the difference in the bandgap voltages of Si and SiGe junctions, is obtained as

$$V_{REF} = K_1\frac{R_4}{R_1}(V_{G0,Si} - V_{G0,SiGe}). \tag{3.46}$$

These theoretically driven equations can provide guidance and insight to designers on how to select circuit design parameters (resistor values, current mirror ratios, emitter area ratios) to achieve an optimum temperature coefficient. Fig. 3.26 shows simulations results for I_{PTAT}, $I_{V_{BE,BJT}}$ and $I_{V_{BE,HBT}}$, and their weighted subtraction, in this design, respectively.

3.5.3 Measurement Results

The proposed reference circuit was fabricated in IBM's SiGe 8HP BiCMOS technology. P^+ polysilicon resistors were used for all resistors since their temperature coefficient is very small. Common-centroid layout technique was employed for the realization of the current mirrors to minimize the effect of mismatch. The die microphotograph is shown in Fig. 3.25. The die was mounted in a 28 pin ceramic DIP package and wirebonded. The package was inserted into a ZIF

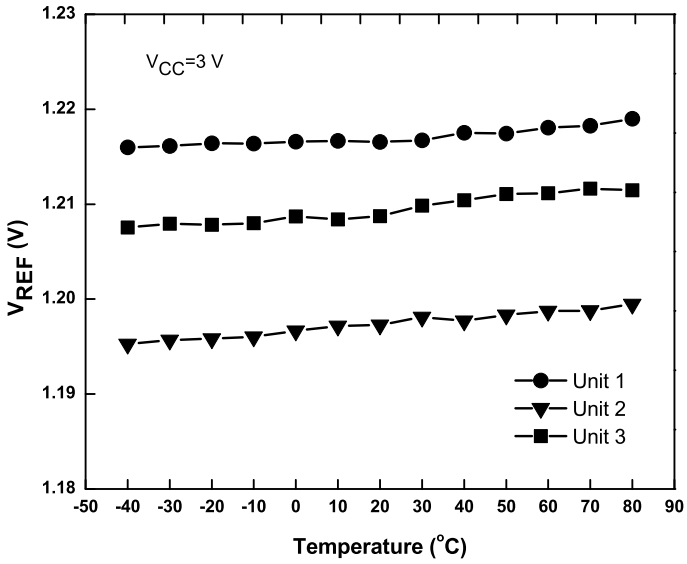


Figure 3.27: Measured output voltage of the proposed reference circuit as a function of temperature.

socket soldered on a PCB. Temperature characterization was performed using SP Scientific's ThermoJet ES precision temperature cycling system [228]. To minimize the loading effects of the measurement equipment, unity gain buffers were also incorporated.

Fig. 3.27 shows measured results for V_{REF} of three samples from different wafers as a function of temperature. Operating with a power supply of 3 V, unit 1 provides the best overall thermal performance with a TC of 17.0 ppm/°C across $(-40 : 70)$°C. The averaged TC for all measured samples across $(-40 : 70)$°C is 24.9 ppm/°C. Incorporating trimming networks would further improve the TC.

One important performance measure for BGR circuits is the PSRR, which is indicative of how well they can reject the power supply noise. PSRR of the proposed circuit was measured at -70°C, -30°C, 0°C and 20°C. As shown in Fig. 3.28, at all temperature points, the circuit shows PSRR less than -40 dB at 10 Hz and less than -30 dB up to 100 kHz. While this PSRR is comparable to that of voltage references in [233] and [172], it can be further improved by employing PSRR enhancement techniques such as the one proposed in [234]. Table 3.8 compares the performance of the proposed circuit with some of previously designed SiGe-based BGR circuits. While a direct comparison is not possible (due to the difference in technology, design,

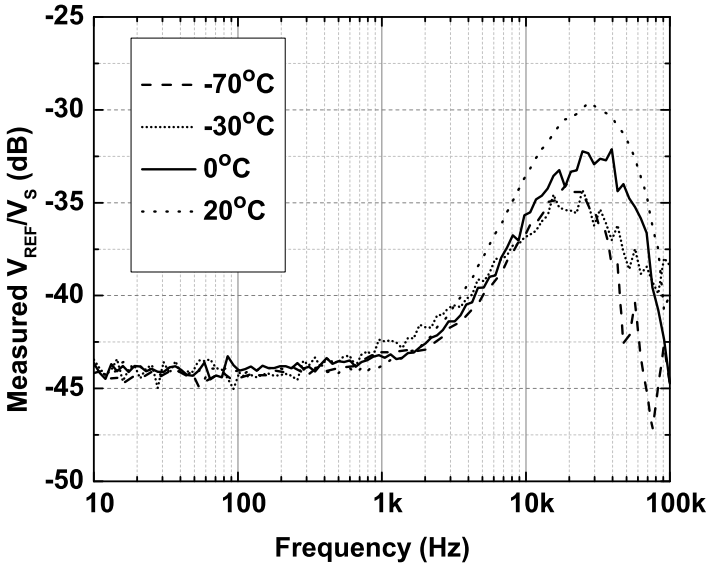


Figure 3.28: Measured PSRR of the proposed reference circuit at four different temperatures.

and reported temperature ranges for TC), the proposed reference circuit offers the smallest TC for the best case and comparable TC for the average across three units, against temperature variations, verifying the effectiveness of the proposed compensation technique.

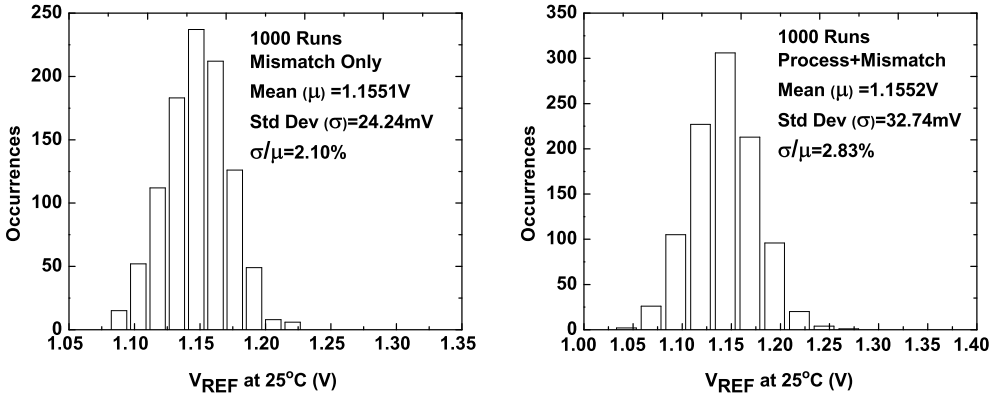
3.5.4 Discussion

The proposed temperature compensation technique, by taking advantage of the availability of two types of $p-n$ junctions, offers a new promising approach for designing highly stable reference circuits in SiGe BiCMOS technology platforms. To further evaluate the robustness of the

Table 3.8: Performance comparison of the proposed reference circuit with prior SiGe-based BGRs.

	This work	**[236]-1**	**[236]-2**	**[157]**	**[233]**
Year	2016	2014	2014	2006	1998
SiGe Technology (nm)	130	90	90	500	350
Compensation	Curvature correction, difference of Si-Si and SiGe-Si junction voltages	First-order	Inverse-Mode first-order	Exponentially-compensated	First-order
$\mathbf{V_{CC}}$ (V)	3	2	2	3.3	2.5
Nominal $\mathbf{V_{REF}}$ (V)	1.216	1.083 *	1.061 *	1.172	1.328
TC (ppm/°C)	17.0 (-40:70) best of 3 samples	24 (-53:127) * 1 sample	43 (-53:127) * 1 sample	28.1 (-180:27) 69.9 (-230:27) best of 3 samples	36.5 (-50:150) 25.1 (0:75) 1 sample

* Measured at pre-radiation condition



(a) (b)

Figure 3.29: Distributions of V_{REF}, from Monte Carlo simulation of 1000 runs, a) for mismatch only, and b) for mismatch and process variation.

circuit against process and mismatch variations, Monte Carlo simulations of 1000 runs, as well as corner simulations were performed. Fig. 3.29 shows the result of Monte Carlo simulations at $25°$C. The coefficient of variation (σ/μ) [215] for V_{REF} is obtained as 2.10% when mismatch is considered, and 2.83% when both mismatch and process variations are considered. Major sources of mismatch in reference circuits include mismatch in current mirrors, transistors and resistors. Mismatch in transistors and resistors were minimized using layout techniques for transistors, and realizing resistors with P^+ polysilicon, which offers small temperature and voltage coefficients, respectively. The observed variations could be due to mismatch in current mirrors, (which also have been identified as the dominant error in bandgap references [238]). The coefficient of variation and the temperature coefficient can be further improved by including trimming networks for R_1-R_3, specifically for R_3, since the PTAT current plays a major role in generating I_{PTAT}, $I_{VBE,BJT}$, and $I_{VBE,HBT}$. Table 3.9 summarizes the simulation results for MOS transistors corners. Temperature coefficient shows larger variations across process corners when $T > 85°$C is considered (e.g. military temperature range). This observation could be due to the fact that at high temperatures, the PTAT current dominates the overall behavior, due to changes in the op-amp loop gain and the offset voltage.

While the measurement results exhibited small TC verifying the effectiveness of the proposed approach in realizing precise SiGe references, the output voltage still revealed some

Table 3.9: TC at transistor corners.

	TT	SS	FF	SF	FS
TC across (0:70)°C (ppm/°C)	18.8	4.6	33.7	17.8	9.4
TC across (-40:85)°C (ppm/°C)	12.0	8.8	23.8	12.7	6.0
TC across (-55:125)°C (ppm/°C)	8.4	23.7	44.4	24.1	23.5

levels of temperature sensitivity. Possible reasons for the observed variations include the following. First, in the design example, it was considered that $\theta_{HBT} \approx 0$ to the first order. In practice, an exact $\theta_{HBT} = 0$ is not achieved, and some degree of temperature variability will exist. Deviation from $\theta_{HBT} = 0$ will introduce temperature sensitivity. Alternative solutions can be considered (e.g. $\theta_{HBT} = 1$ and $\theta_{BJT} = 2$) to realize the proposed compensation approach. Second, post-fabrication variations, measurement setup (e.g. the mechanical stress of the ceramic DIP packages [239]), and current mirror mismatch (as discussed above) could also have introduced variations during the measurement. Resistive trimming networks can be employed to minimize such variations.

An interesting aspect of the proposed compensation technique is that this circuit generates an output voltage that is related to the "*difference*" of the bandgap voltages of Si and SiGe. As such, it can be utilized to experimentally estimate the Ge-induced bandgap offset for different Ge grading profiles. In the circuit presented in this section, the resistors R_1 and R_2 in Fig. 3.23 were set to $25.7\ k\Omega$, resistor R_4 in Fig. 3.25 was set to $358.4\ k\Omega$, and the mirroring ratios K_1 and K_2 were both set to 1. Plugging these numbers and measured V_{REF} into (3.46), results in the bandgap voltage difference of 89.1 mV.

3.6 A Multi-Piecewise Curvature-Corrected Technique for BGR Circuits

In Section 3.3, several compensation solutions proposed to improve the temperature stability of the BGR circuits have been reviewed. One of the proposed compensation solutions is the piecewise curvature-corrected technique in which a nonlinear component is used for the compensation [175–181, 185]. Different ways for the realization of this technique have been suggested. For example, in [175], the nonlinear component is produced by the subtraction of PTAT and CTAT currents, and is added in the circuit during the higher temperature range when

the PTAT component becomes the dominant term, while in [185] a logarithmic current is included during the high temperature range to the output of an exponentially compensated BGR to achieve further temperature stability.

Two common approaches can be observed in all the existing piecewise curvature-corrected techniques: 1) the inclusion of the nonlinear term is done only during a specific temperature range (higher part), and 2) the generated nonlinear term is designed to increase with temperature. If the nonlinear terms can be included properly in the lower temperature regions, the temperature drift of the circuit will be further reduced. The proper inclusion of the nonlinear terms across all temperature ranges mandates the realization of nonlinear currents, that depending on the deviation of the output voltage from the nominal value, either decrease or increase with temperature.

In this section, with the motivation to address these issues, a systematic piecewise curvature-corrected compensation technique is proposed, along with the simulation results of a designed BGR circuit.

3.6.1 Basic Concepts

The basic concepts of device physics of CMOS transistors have been investigated in both Section 3.2.2 and Section 3.4, including the operations in both saturation and subthreshold regions. In this section, the key expressions are briefly reviewed again.

In an NMOS transistor, when V_{GS} is larger than V_{TH}, I_D can be expressed as:

$$I_D = \begin{cases} \frac{\mu C_{ox} W}{2L}(V_{GS} - V_{TH})^2 & \text{(Saturation)} \\ \frac{\mu C_{ox} W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] & \text{(Triode)} \end{cases} \tag{3.47}$$

In both conditions of (3.47), μ and V_{TH} are the temperature dependent parameters. In deep triode region, where $V_{DS} << 2(V_{GS} - V_{TH})$, the drain current can be estimated to be:

$$I_D = \frac{\mu C_{ox} W}{L}(V_{GS} - V_{TH})V_{DS}, \tag{3.48}$$

where μ can be expressed as (same as 3.3)

$$\mu = \mu_0(\frac{T}{T_0})^{-m}. \tag{3.49}$$

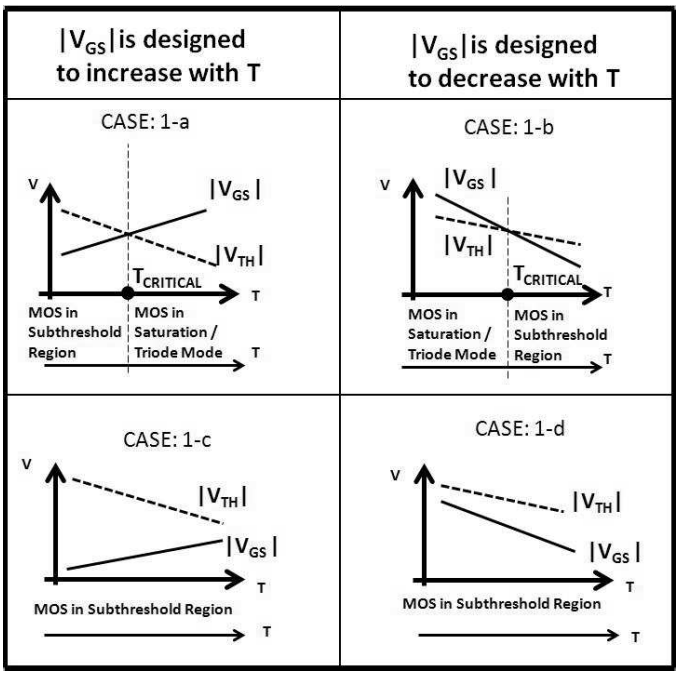


Figure 3.30: Change in the operating region of a MOS transistor based on the temperature behavior of $|V_{GS}|$.

The threshold voltage decreases linearly with temperature as:

$$V_{TH} = V_{TH0} - \alpha(T - T_0). \tag{3.50}$$

When the V_{GS} is smaller than V_{TH}, the transistor operates in the subthreshold region, and if $V_{DS} > 3V_T$ (V_T is the thermal voltage), I_D is estimated to be:

$$I_D = \mu C_{ox}(n-1)\frac{W}{L}V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right). \tag{3.51}$$

Equation (3.50) shows that the threshold voltage is a decreasing function of temperature, and therefore, depending on the applied value of V_{GS}, the operational region of the transistor can change with temperature. This feature implies that using a temperature-dependent gate-source voltage, the designer is able to control the operating region of the transistor across temperature. Note that the same argument applies when dealing with PMOS transistors.

Fig. 3.30 shows four possible cases in which depending on whether $|V_{GS}|$ is an increasing (cases 1-a and 1-c) or decreasing (cases 1-b and 1-d) function of temperature, how the region of operation of the transistor changes with temperature. For example, in case 1-a (1-b), when the operating temperature is below $T_{CRITICAL}$, (the temperature at which $|V_{GS}|$ and $|V_{TH}|$

coincide), the transistor is operating in the subthreshold (deep triode or saturation) region, and as soon as the operating temperature is above $T_{CRITICAL}$, the transistor is switching into the triode or saturation (subthreshold) region. For cases 1-c and 1-d, the rate of change in $|V_{GS}|$ is such that the transistor stays below $|V_{TH}|$ over the desired temperature range, and therefore, the transistor will stay in the subthreshold region. Note that in all these cases, it is not necessary for the gate-source voltage to maintain a linear relationship with temperature.

3.6.2 Proposed Compensation Technique

Without loss of generality, for the derivation of equations we will consider NMOS transistor, but the discussion can be applied in a similar way to PMOS transistors as well. Since the aim of the proposed idea is to generate nonlinear currents through applying a temperature dependent voltage to the gate terminal, the temperature behavior of the drain current in different operating regions can be studied first.

3.6.2.1 Temperature Behavior of I_D

In the following analysis, we assume the temperature dependent voltage (which could be taken from the available PTAT or CTAT components) applied to the gate terminal is expressed as

$$V_{GS}(T) = V_{GS0} + \gamma(T - T_0), \tag{3.52}$$

where V_{GS0} is the gate-source voltage at the nominal value and γ is a positive (for PTAT case) or negative (for CTAT case) constant.

3.6.2.1.1 Saturation Region

Replacing (3.49), (3.50) and (3.52) into (3.47) for the saturation case, I_D can be written as

$$I_D(T) = K_1(\frac{T}{T_0})^{-m}[V_0 + \lambda(T - T_0)]^2, \tag{3.53}$$

where $K_1 = \frac{1}{2}\frac{W}{L}\mu_0 C_{ox}$, $V_0 = V_{GS0} - V_{TH0}$, and $\lambda = (\gamma + \alpha)$. Following the approach in [204, 205], if the temperature raises by a small amount (δT) from T_0 to ($T_0 + \delta T$), then:

$$I_D(T_0 + \delta T) = K_1(1 + \frac{\delta T}{T_0})^{-m}[V_0 + \lambda\delta T]^2. \tag{3.54}$$

Using the Taylor series expansion

$$(1+\frac{\delta T}{T_0})^{-m} \approx (1-m\frac{\delta T}{T_0}), \tag{3.55}$$

and subtracting $I_D(T_0) = K_1 V_0^2$ from (3.54), the change in I_D with temperature is estimated to be

$$\delta I_D = \delta T[K_1 V_0(2\lambda - \frac{mV_0}{T_0})] + \delta T^2[K_1\lambda(\lambda - \frac{2mV_0}{T_0})] - \delta T^3[\frac{K_1 m\lambda^2}{T_0}]. \tag{3.56}$$

3.6.2.1.2 Deep Triode Region

Same discussion can be applied for the drain current in the deep triode region. Using (3.49), (3.50), (3.52) and (3.55), and ignoring the temperature dependency of V_{DS}, the change in I_D from (3.47) for the deep triode region when the temperature changes from T_0 to $T_0 + \delta T$ can be estimated as

$$\delta I_D = \delta T[2K_1\lambda - \frac{2K_1 mV_0}{T_0}] - \delta T^2[\frac{2mK_1\lambda}{T_0}]. \tag{3.57}$$

3.6.2.1.3 Subthreshold Region

In the subthreshold region, the drain current follows (3.51). The term inside the exponential function in (3.51) can be written as:

$$\frac{(V_{GS}-V_{TH})}{nkT/q} = \frac{\lambda}{nk/q} + \frac{1}{T}[\frac{V_0}{nk/q} - \frac{\lambda T_0}{nk/q}] = A_0 + A_1 T^{-1}, \tag{3.58}$$

where $A_0 = \frac{\lambda}{nk/q}$ and $A_1 = \frac{V_0}{nk/q} - \frac{\lambda T_0}{nk/q}$. A_1 is generally a negative term. Noting $K^{'} = 2K_1(n-1)(T_0\frac{k}{q})^2$, the current I_D from (3.51) can be rewritten as

$$I_D(T) = K^{'}(\frac{T}{T_0})^{(2-m)} \exp{(A_0 + A_1 T^{-1})}. \tag{3.59}$$

Using the Taylor expansion of $\frac{1}{1+\frac{\delta T}{T_0}} \approx 1 - \frac{\delta T}{T_0}$, the change in the drain current when the temperature varies from T_0 to $(T_0 + \delta T)$ is estimated to be

$$\delta I_D = I_D(T_0)[(1+(2-m)\frac{\delta T}{T_0})\exp(\frac{-A_1\delta T}{T_0}) - 1]. \tag{3.60}$$

Equations (3.56), (3.57), and (3.60) clearly show that I_D in each operating region has non-linear behavior with temperature and depending on the value of γ and V_0, the weighted contribution of each term could be different.

3.6.2.2 Multi-Piecewise Curvature-Corrected Technique

We now discuss the four possible conditions shown in Fig. 3.30, and see how by controlling the temperature behavior of the gate-source voltage (through γ) one can generate different non-linear components.

3.6.2.2.1 Case 1-a

As seen in Fig. 3.30, case 1-a refers to the condition in which as the temperature passes $T_{CRITICAL}$, the transistor switches from operating in the subthreshold to either the deep triode or saturation region. For this case, the gate voltage has to be an increasing function of temperature, and hence, one option is to use the already available PTAT current from the uncompensated BGR. Fig. 3.31-a shows one circuit realization option for this approach, where the gate-source voltage of the transistor M_1 is set by the voltage across resistor R through which a mirrored version of the available PTAT current is flowing. Fig. 3.31-b corresponds to the case of M_1 switching into the deep triode region, since a diode-connected transistor M_2 is included in the circuit to decrease the V_{DS} of M_1. As seen from (3.57), when a PTAT voltage is applied to the gate terminal ($\gamma > 0$), the drain current will be increasing with temperature and with the first order term being the dominant term. Fig. 3.31-c shows the case when M_1 will be switching into the saturation region.

3.6.2.2.2 Case 1-b

In case 1-b, the gate-source voltage is a decreasing function of temperature, therefore, the behavior of the drain current over the temperature will be the mirrored version of the currents in case 1-a, around a reference plane set at $T_{CRITICAL}$. Currents from case 1-b can be used to fulfill the demand of compensation in the low temperature region. The design in [176], being implemented with PMOS transistors, is similar to case 1-b.

Fig. 3.32 shows the results of corner simulations for the current I_D of an NMOS transistor biased to meet the conditions of cases 1-a and 1-b. For each case, transition to and from the deep triode region (Figs. 3.32-a and 3.32-b) and saturation region (Figs. 3.32-c and 3.32-d) are considered. As can be seen, the temperature behavior of the currents follow the pattern

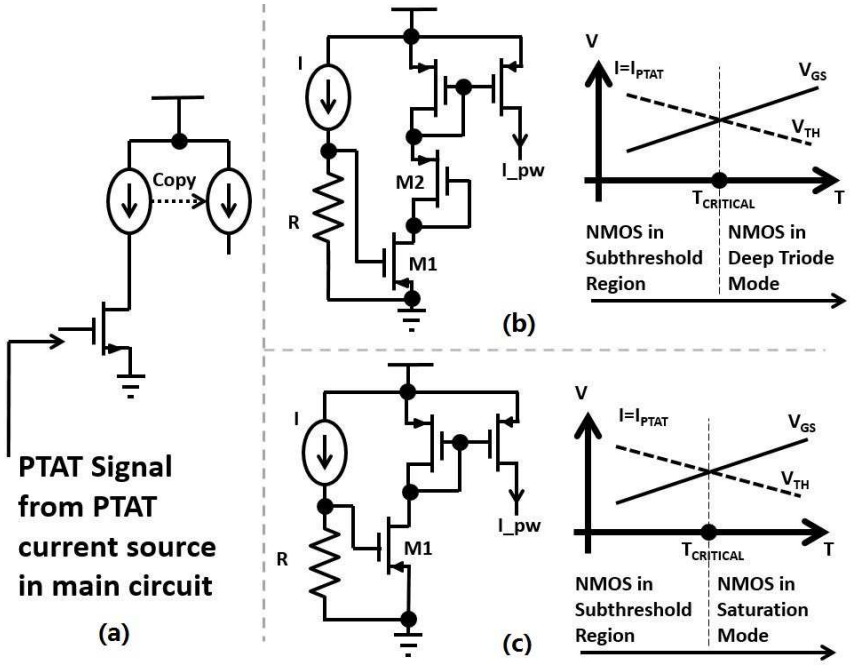


Figure 3.31: Realization of case 1-a using NMOS transistors.

predicted in Section 3.2.2.

3.6.2.2.3 Cases 1-c and 1-d

In these two cases, the transistor remains in the subthreshold region. Equation (3.60) shows that the subthreshold current should have an approximately exponential behavior with temperature (Fig. 3.33), although smaller in magnitude compared to previous two cases. This exponential increase feature can further facilitate the compensation process in certain BGR designs.

3.6.2.3 PMOS vs NMOS implementation

Both NMOS and PMOS transistors can be used for the realization of the four cases shown in Fig. 3.30. Implementation using NMOS transistors results in generating current sources (which can be used for adding the nonlinear terms to existing currents, as is the case in most of the existing piecewise compensation techniques), while with PMOS transistors, current sinks are implemented, which can be employed as current subtractor. Fig. 3.34 illustrates how using a current sink can become effective in reducing the temperature coefficient of a BGR circuit.

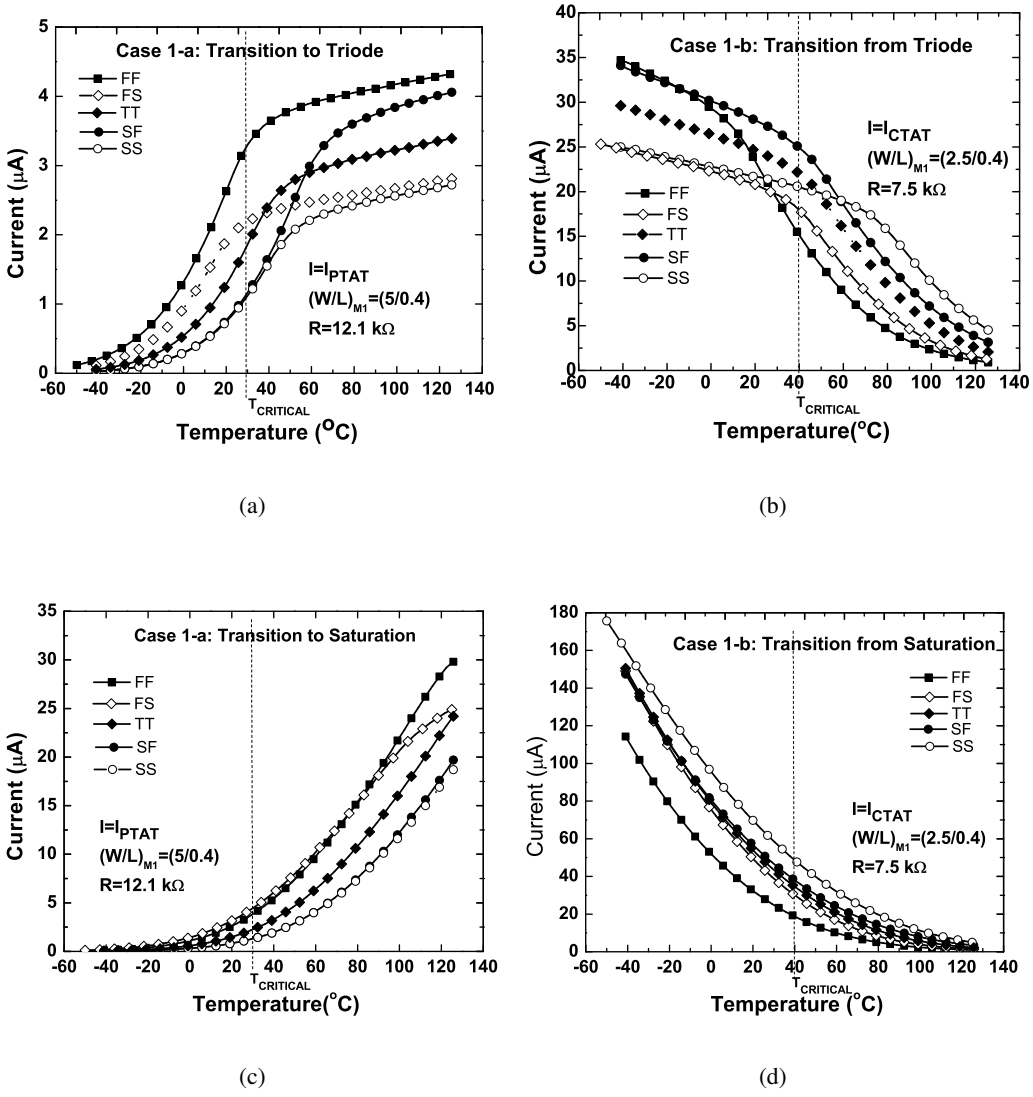


Figure 3.32: Corner simulation results for I_D: transition to/from deep triode region a) case 1-a, b) case 1-b; transition to/from saturation region, c) case 1-a, and d) case 1-b.

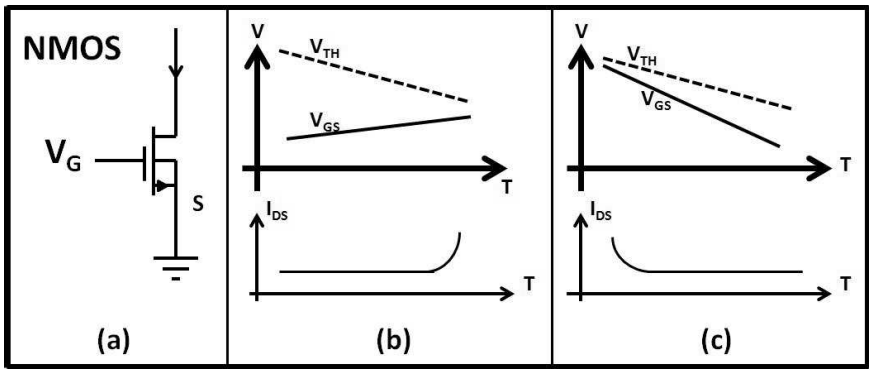


Figure 3.33: Piecewise currents b) case 1-c, and c) case 1-d.

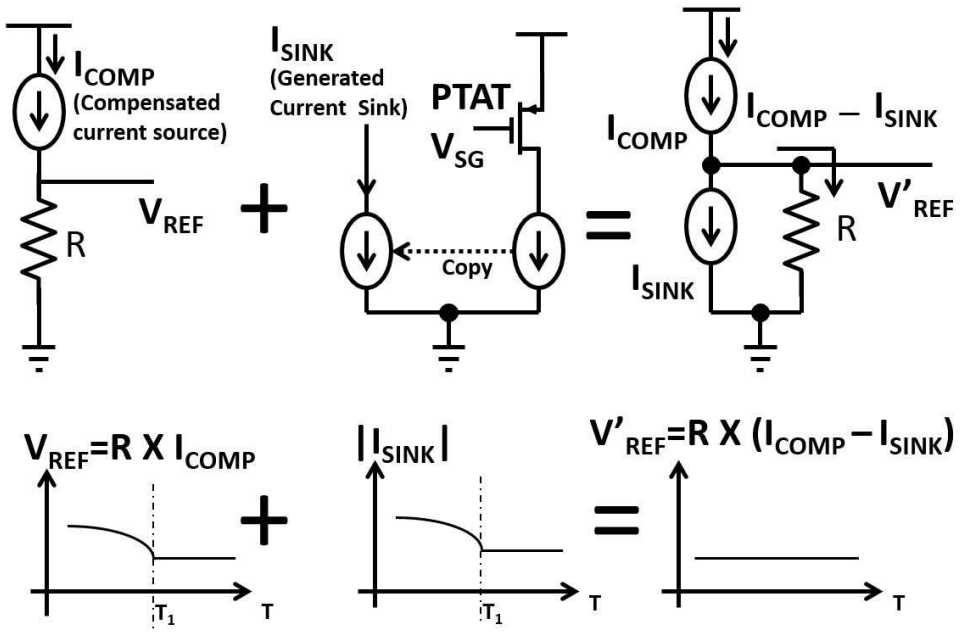


Figure 3.34: Example of using a current sink to reduce the temperature coefficient.

3.6.3 Design Consideration and A Design Example

Depending on the behavior of the BGR's output across the desired temperature range, our proposed solution can be used to minimize its temperature coefficient. Proper design considerations need to be followed to maximize the compensation. First is the selection of $T_{CRITICAL}$ point. As seen in Fig. 3.31, resistor R can be used to control the value of V_{GS}, and therefore, the value of $T_{CRITICAL}$. A good practice would be to use a tunable resistor [240] and be able to move the location of $T_{CRITICAL}$, if needed.

Looking at the current outcomes of the four cases presented in Fig. 3.30, a proper combination of these conditions can be used to achieve the maximum compensation. In addition, an array of different piecewise blocks can be designed as a trimming network, to tune the temperature coefficient of the circuit in the real circuits.

To validate the effectiveness of this technique, a first-order BGR circuit was designed and simulated. The schematic is shown in Fig. 3.35. The PTAT current is generated by the difference between base-emitter voltages of two transistors with different emitter areas. A voltage-mode compensation is achieved by adding the base-emitter voltage of transistor Q_2 and the PTAT voltage across R_1 [201]. The circuit shows a temperature coefficient of 13.7 ppm/°C

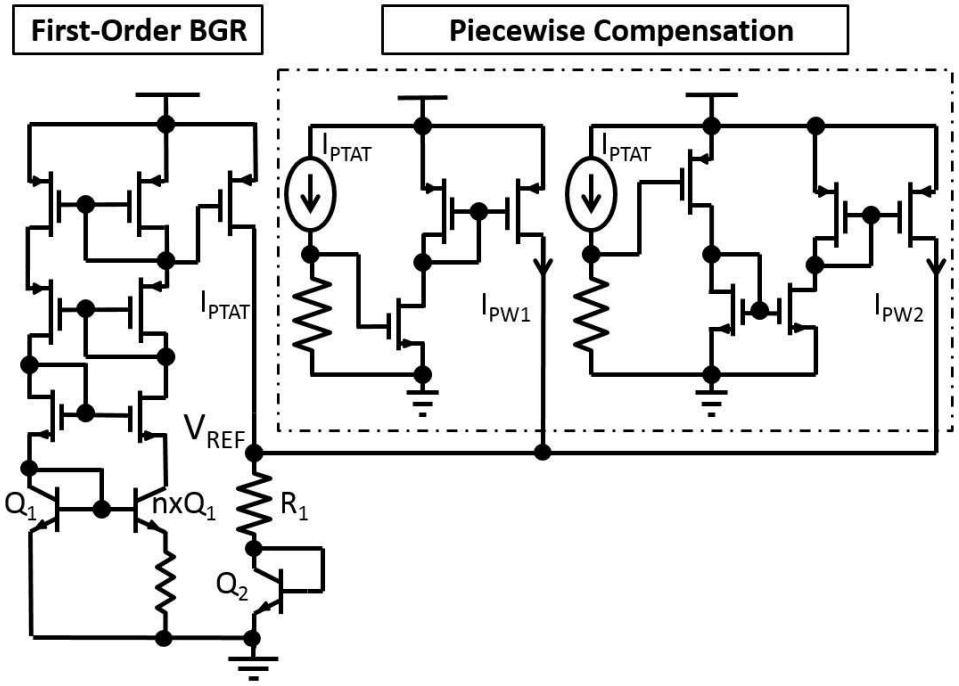


Figure 3.35: First-order and piecewise curvature-corrected BGR circuits.

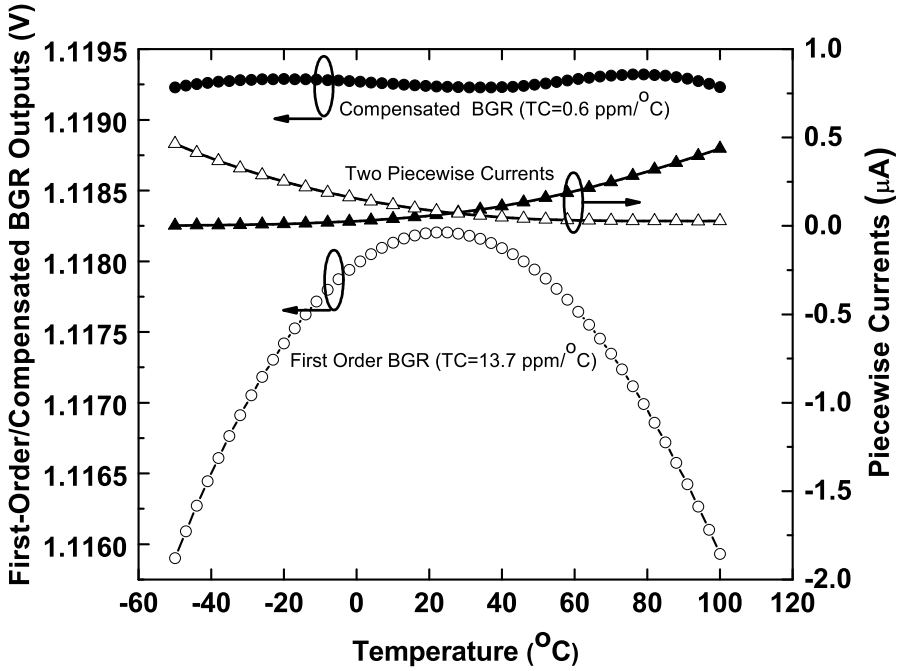


Figure 3.36: Simulation results for piecewise currents, first-order and compensated BGRs.

over (-50:100)°C temperature range (Fig. 3.36). To improve the temperature stability of the circuit, two piecewise compensation blocks were designed. One block is implemented using NMOS transistors for the condition of switching from subthreshold to saturation region (case 1-a), while another one is realized by PMOS transistors to cover the reverse switching condition (Fig. 3.36). The critical temperature of each block was determined separately. With the aid of these two compensation blocks, the temperature coefficient of the circuit is significantly decreased to 0.6 ppm/°C (Fig. 3.36), which demonstrates the effectiveness of the proposed technique.

3.7 Summary

In this chapter, three innovated temperature compensation techniques are proposed following a review of device physics of SiGe BiCMOS technology and the design challenges of the BGR circuit. In Section 3.4, a novel BiCMOS-based compensation approach for achieving fully curvature-corrected BGR circuits was presented. The proposed compensation approach via utilizing sub-threshold-operating MOSFETs introduces an innovative and elegant solution to directly cancel the nonlinear $T\ln(T)$ term in the $I_{V_{BE}}$ component, thereby, offering the possibility of achieving fully temperature-independent BGR circuits. The theoretical basis of the proposed compensation approach is extensively described, and design equations were derived. Based on the proposed BiCMOS-based compensation approach, a low temperature coefficient current-mode BGR circuit was designed and fabricated. The compensation components (the PTAT and the $I_{V_{GS}}$ components) were experimentally characterized for the first time, and results validated the theoretical analysis. Measurement results for the reference circuit showed the circuit offers highly temperature stable output across $[0 - 150]$ °C. In Section 3.5, a new temperature compensation technique based on the weighted difference of Si-Si and SiGe-Si $p - n$ junction voltages for SiGe reference circuits was presented. Unlike regular bandgap reference circuits, in which the generated output voltage is referred to the bandgap energy of the background semiconductor material, the circuit employing the proposed technique can generate an output that is related to the difference in the bandgap voltages of Si and SiGe. As such, it can be used to experimentally evaluate the Ge-induced bandgap offset in a given SiGe technology. In Section 3.6, a multi-piecewise curvature-corrected compensation technique based on

controlling the temperature behavior of the gate-source voltage of MOSFETs is proposed. Four different cases for generating piecewise currents are considered, and detailed analysis of the expected temperature behavior is provided. The technique provides the designer with additional flexibility to achieve the maximum temperature compensation. Simulation results showed that the proposed multi-piecewise curvature-corrected technique improved the temperature coefficient of a first-order BGR from 13.7 ppm/°C to 0.6 ppm/°C.

Chapter 4

Wireless Electrical Stimulators for Nanofibers

Functional loss and impairment of skeletal muscle could occur as a result of a diverse range of causes including trauma, aging, and diseases such as amyotrophic lateral sclerosis [241], vascular disease, or cancer [242]. Once a muscle is injured, satellite cells are activated to help regenerate muscle [3]. However, satellite cell incidence in the tissue is extremely low, and is dependent on the age and muscle fiber composition [3]. Several approaches, such as intramuscular injections of skeletal myoblasts [10], have been sought to aid in the regeneration of deteriorated tissue. However, existing solutions display contractility only "after" new muscle has been regenerated, which typically is a lengthy process. These limitations highlight the need for the development of new technologies that can provide function and regeneration of lost tissue in a timely manner, to improve the patient's quality of life over both short and long terms.

A possible solution to these problems is the development of new classes of subcutaneous muscle prosthesis, which are envisioned to be made by combining iEAPs [18, 19, 243–246] with their controllable electrical stimulators, forming contractile scaffolds. The development of such a subcutaneous module with the ability to actuate in a controlled way, prior to tissue regeneration, will enable restoring muscle function immediately upon the loss of skeletal muscle. Furthermore, since mechanical stimulation facilitates the formation of new muscle tissue by enhancing cellular proliferation [247], it is expected that such a module will also speed up the process of tissue regeneration. Thereby, the technology has the potential to significantly impact the quality of life of many people who deal with problems related to loss of muscle function.

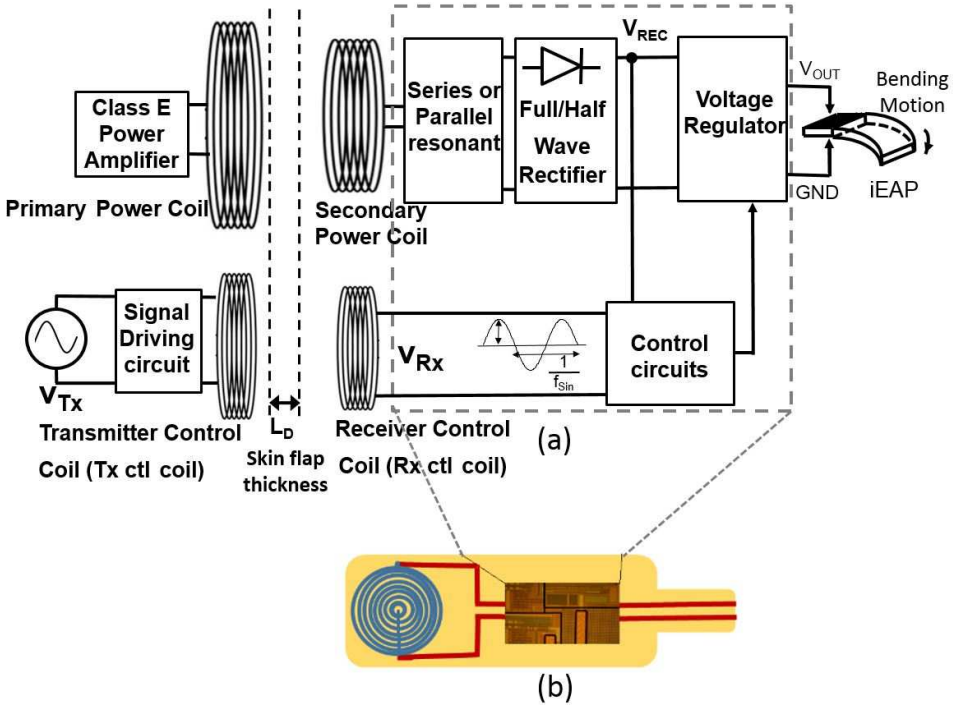


Figure 4.1: a) Block diagram of an iEAP-based subcutaneous muscle prosthesis. A conceptual representation for the movement of iEAPs, when placed inside an electric field, is also shown (after [249]). b) implantable microchip (top-view) without the encapsulation layer.

4.1 Introduction

iEAPs respond to electrical stimulation by changing in shape that is caused by ion displacement inside the polymer [246, 248]. The degree and the direction of contraction are dependent on the magnitude and the polarity of the electric field supplied by the stimulator. As such, to achieve controllable actuation after implanting the module in the body, both the magnitude and the polarity of the electric field must be wirelessly tunable.

Derived from the generic implantable stimulator architecture in Chapter 2, the configuration of the stimulator dedicated for iEAP application is depicted in Fig. 4.1. The electrical stimulation is provided by a wirelessly tunable implanted voltage regulator, integrated with iEAPs and powered-up via a WPT link. In this chapter, we will investigate the feasibility in using the LDO to provide the electrical stimulation of iEAPs, along with the appropriate wireless tuning technique to control the degree and the direction of the iEAP's contraction.

This chapter is organized as followings. In Section 4.2, an overview of iEAPs is presented, along with their actuation process and electrical model. In Section 4.3, the feasibility of using

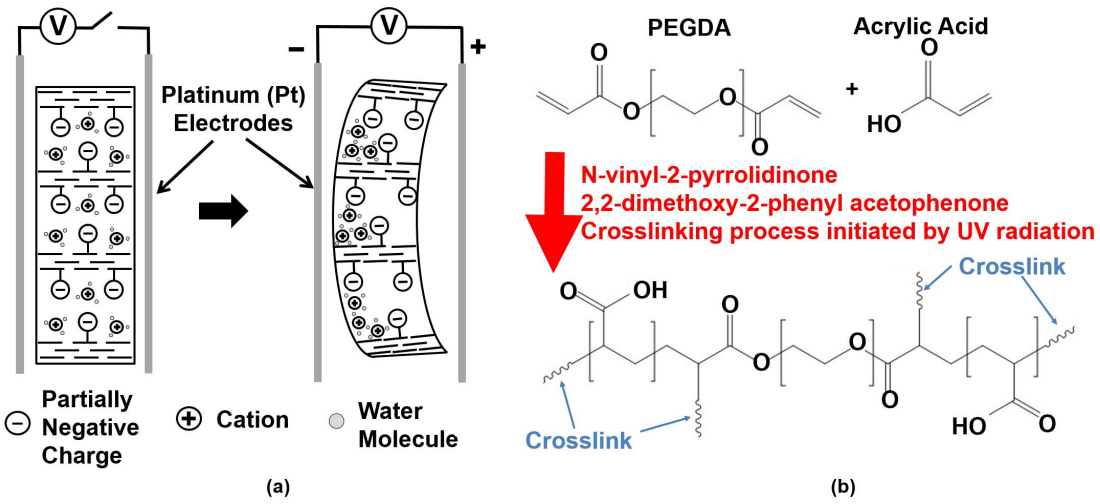


Figure 4.2: a) Conceptual illustration of the operating mechanism of iEAPs inside an electric field, and b) basic reaction used to form the PEG-PAA copolymer.

LDO as the voltage regulator in Fig. 4.1 is studied. The functionality of electrically stimulated iEAPs is evaluated under steady-state and transient conditions. Electrical characteristics of iEAPs in terms of conductance and movement characteristics of iEAPs in terms of changes in the bending angle during fixed and transient stimulation are evaluated. In Section 4.4, the challenges in designing the LDO for the iEAP application are discussed, and solutions are provided. In Section 4.5, a design technique, built upon the concept of frequency-based telemetry is presented to implement wirelessly tunable LDO. In Section 4.6, a complete system capable of wireless tuning of both the magnitude and the polarity of the voltage is presented, which is able to accommodate the stimulation requirements of iEAPs. The *in vitro* experiments are conducted by combining the proposed system and the iEAP material.

4.2 Biocompatible ionic Electroactive Polymers and its Electrical Model

In this section, the operating mechanism and the electrical model of the iEAPs will be reviewed, which will determine stimulation requirements and guide the design of the iEAP stimulator.

4.2.1 Biocompatible ionic Electroactive Polymers

iEAPs have the potential to be used as artificial muscles and as scaffolds for skeletal muscle tissue engineering, because there are parallels between the mechanism of action of iEAPs and

the physiology of native muscle tissue. When iEAP gels (hydrogels) are exposed to an electric field, charged ions diffuse through the gel and cause actuation. Fig. 4.2-a conceptually illustrates this action [30]. Inside the hydrogels, there exist fixed partial negative charges that are attached to the polymer backbone. When swelled with phosphate buffered saline (PBS), positively-charged cations associate with the water molecules via hydrogen bonds, and evenly disperse through the hydrogel. When an electric field is applied the positively-charged cations and associated water molecules move towards the negative electrode, causing one side of the hydrogel to swell. The swelling results in an overall bending actuation in the construct [250] (as seen in Fig. 4.2-a). This mechanism of action is similar to muscle tissue, in which an external source of depolarization (nerve signal) leads to conformational changes and movement (contraction for muscle) [251].

iEAPs in this study were constructed using poly(ethylene glycol) diacrylate (PEGDA, or PEG for short) and acrylic acid (AA). PEG is a biocompatible, hydrogel-forming polymer that is relatively biologically inert. Depending on the application, different polymers and moieties (e.g. poly(vinyl alcohol) (PVA), poly(acrylic acid) (PAA)) can be used to form the hydrogels, and different methods can be used to form the network (e.g. freezing, cycling, heating) [30,252, 253]. We used AA monomers because they introduce a highly polar functional group, which can easily be controlled by changing their relative concentration.

The crosslinked copolymer of PAA and PEG was created using the reaction described in Fig. 4.2-b, in which the chemistry of PEG was altered to make it more electroactive through the binding of the polar monomer AA [30]. In the fabrication process, a prepolymer solution containing AA monomer, PEGDA with a molecular weight of 4000 Daltons, and a photoinitiator solution (2,2-dimethoxy-2-phenyl acetophenone, n-vinyl-2-pyrrolidinone, 300 mg/mL) was exposed to long-wavelength UV light (365 nm, 10 mW/cm^2) for up to five minutes. The photoinitiator is converted into a free radical via cleavage and initiates the polymerization of AA into PAA, simultaneously incorporating PEGDA via the acrylate groups as it progresses [30]. Since each C=C bond provides two reactive sites, random polymerization and crosslinking of the PEG-PAA hydrogel occurs once activated by the free radical. Following these fabrication steps, the biocompatible PAA-PEG hydrogels can demonstrate reversible, repeatable actuation while supporting cell growth [30].

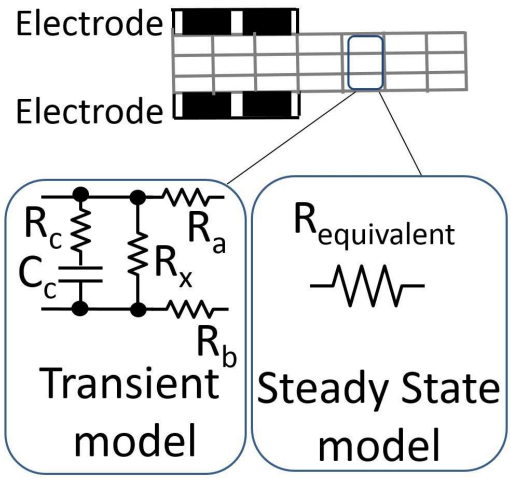


Figure 4.3: Equivalent electrical model of iEAPs (after [254])

4.2.2 Electrical Modeling of the ionic Electroactive Polymers

The electrical models for the transient and steady state for unit length iEAPs are illustrated in Fig. 4.3 [254]. In the transient model, resistors R_a and R_b denote surface resistances, resistor R_x represents the resistance of the polymer gel layer, and resistor R_c and capacitor C_c model the exponential step response characteristic observed in the experiments. In the steady state model, each unit length can be modeled with an equivalent resistor. Since in the proposed module, iEAPs will be stimulated via a constant electric field, the steady state model shown in Fig. 4.3 will be used for modeling iEAPs.

The LDO will be designed to stimulate iEAPs of different lengths. Therefore, it is necessary to determine the minimum and maximum load resistances that will be driven by the LDO. The maximum (minimum) unit conductance $G_{max}(G_{min})$ has been estimated to be 0.046 S/cm (0.022 S/cm) [18]. If the length of iEAPs varies from *1 cm* (L_{min}) to *4 cm* (L_{max}) respectively, the load resistance that the LDO is required to drive will be between R_{min} and R_{max} as derived below

$$R_{min} = \frac{1}{G_{max}L_{max}} = 5.44\,\Omega, R_{max} = \frac{1}{G_{min}L_{min}} = 45.44\,\Omega. \tag{4.1}$$

The $[R_{min} - R_{max}]$ represents the load resistance range for the LDO, with R_{min} corresponding to the heavier load condition (larger current).

4.3 *In Vitro* Characterization of the iEAP using an Tunable LDO

The degree of the movement in the iEAP-based subcutaneous muscle prosthesis will be dependent on the level of the electrical stimulation that is received by iEAPs. The electrical stimulation can be provided by an implanted voltage regulator, integrated with iEAPs and powered-up via a WPT link (see Fig. 4.1) . Commonly used architectures for implementing voltage regulators are low-dropout (LDO) [255] and inductor-based switching regulators [256]. Due to small area requirement of the implant, LDO architecture will be considered.

In this section, a manually tunable LDO is used to provide the electrical stimulation of these iEAPs. The *in vitro* experimental results of the iEAPs, under fixed and transient electrical field conditions, will be used to prove the effectiveness of using the LDO as the stimulator. In this section, the conductance (representing the electrical characteristics of iEAPs) and the angular speed (representing movement characteristics of iEAPs) are measured at different applied voltage levels.

4.3.1 Experimental Setup

The experimental setup used for the *in vitro* characterization of electrically stimulated iEAPs is described as followings.

4.3.1.1 Stimulator

In the proposed iEAP-based muscle prosthesis, the electrical stimulation will be provided via a tunable LDO (Fig. 4.1). As such, for the *in vitro* characterization of iEAPs, a prototype board is built using a commercially available IC [257] (see Fig. 4.4). This LDO does not require bulky output capacitors for maintaining the stability over a wide load range. Decoupling capacitor C_{IN} is included to improve high frequency noise rejection from the DC power supply. A 1.2 V reference voltage is generated and applied to the non-inverting input terminal of the error amplifier. Potentiometer R_{POT} is used to tune the output of the LDO. The active circuit area for the stimulator is 3.5 cm^2. Powered up with a 5.5 V power supply, the LDO can provide an output voltage in the range of 1.2 V to 5 V, via adjusting R_{POT}.

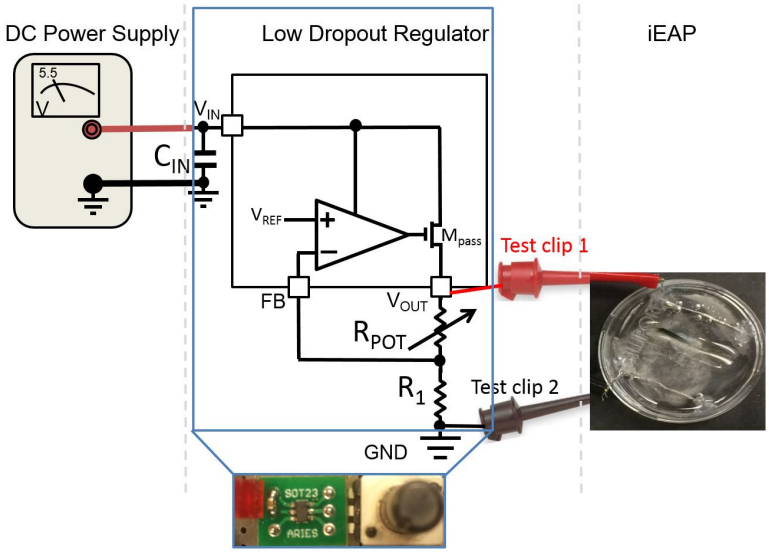


Figure 4.4: Schematic for the stimulator board and its connection for the *in vitro* characterization of iEAPs.

4.3.1.2 In Vitro Setup

Fig. 4.5 illustrates the *in vitro* setup. The electric field is applied via two Platinum (Pt) electrodes that on one end are attached to the output of the LDO and the ground terminal from the stimulator. These two electrodes are suspended, 3 cm (d=3 cm) apart from one another, in a well of PBS solution, which has similar ion concentrations as body fluids. Given that the output of the LDO ranges from 1.2 V to 5 V, assuming the electric field stays uniform and constant, the electrical field intensity (E) can be estimated to vary from 40 V/m to 167 V/m.

The PAA-PEG hydrogel sample with a dimension of $20 \times 4 \times 0.76$ mm^3 was propped-up between two pegs between the anode and the cathode electrodes. Pegs hold the sample in place during the test and prevent it from translating into the space. To improve the visibility of the hydrogel sample, the green dye is applied on its surface.

4.3.2 Experimental Results

The functionality of electronically stimulated iEAPs is evaluated under steady-state and transient conditions. At steady state, the electrical characteristics of iEAPs in terms of conductance are measured at different voltage levels. The movement characteristics of iEAPs are measured in terms of changes in the angle when a fixed voltage is applied for a given time, and when

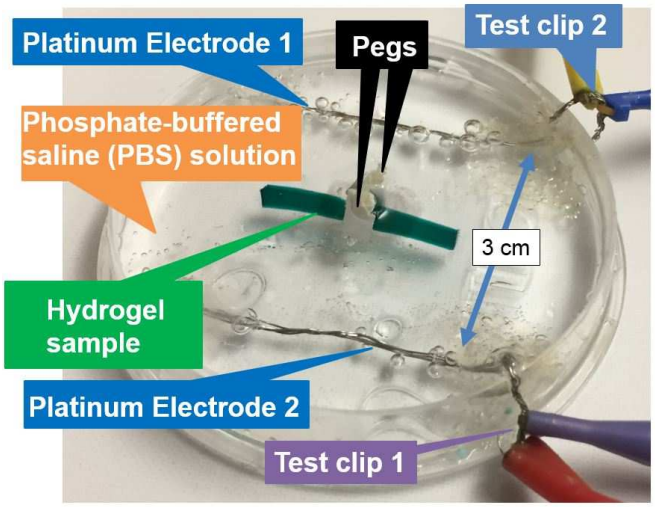


Figure 4.5: Experimental setup for the *in vitro* characterization.

there is a sudden change in the polarity of the applied voltage. In this section, we present and discuss the measurement results.

4.3.2.1 Electrical Characterization-Measuring Conductance

The load current was measured at different voltage levels at steady state condition. Measurement results are shown in Fig. 4.7. As can be seen, the load current of the LDO increases from 4 mA to 14 mA when the applied voltage from the LDO varies from 2.7 V to 5 V. A reasonably good linear relationship between the LDO's applied voltage and current can be observed from the measurement results. The mean conductance of the iEAPs under the test can be then calculated as 4.23 mS.

4.3.2.2 Movement Characterization-Measuring Angular Speed

To characterize the actuation performance of iEAPs under electrical stimuli, the angular speed is measured. To do this, an electrical voltage was applied continuously, for a given duration (here 3 minutes), and the movement of the hydrogel was videotaped throughout the stimulation process. The angle that the hydrogel achieves after 3 minutes of continuous stimulation was measured with respect to its initial state when the electrical stimuli are absent. The angular speed was then calculated as the measured angle divided by the duration of stimulation (here 3 minutes).

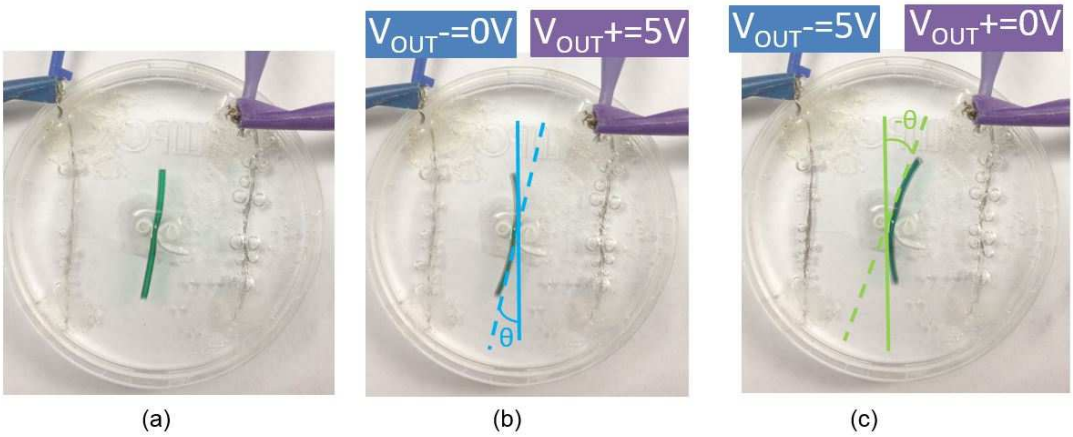


Figure 4.6: Top view of a) the initial state of the iEAP sample in the absence of electric field, b) and c) the iEAP sample bends towards the negative electrode after 3 minutes of continuous electrical stimulation at $+5$ V and -5 V output. The bending angle for each state is also shown.

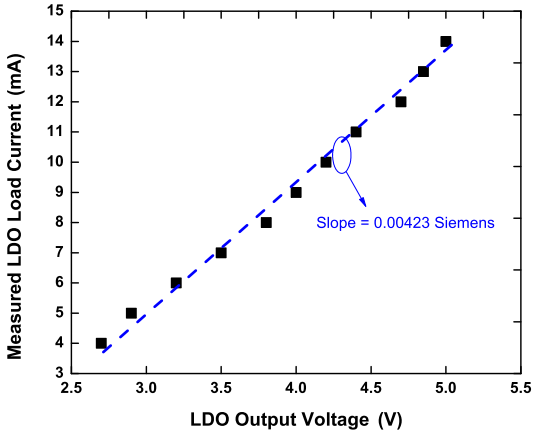


Figure 4.7: Measured LDO current for different LDO output voltages.

The initial state of the hydrogel, where no voltages are applied, is shown in Fig. 4.6-a (top view). Figs. 4.6-b and 4.6-c show how the hydrogel has bent towards the negative electrode after electrical stimulation being continuously applied for 3 minutes, for two scenarios. This process was repeated at six different voltage levels: ± 3 V, ± 4 V, and ± 5 V. The corresponding angular speed is measured at each voltage, and results are plotted in Fig. 4.8. From this figure, two observations can be made. First, the angular speed is proportional to the applied electric field, and second, the hydrogel achieves similar angular speed for a given voltage value but applied in an opposite direction.

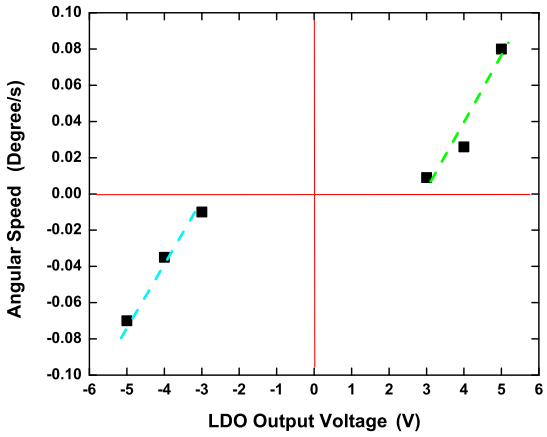


Figure 4.8: Measured results of the angular speed after three minutes of continuous electrical stimulation.

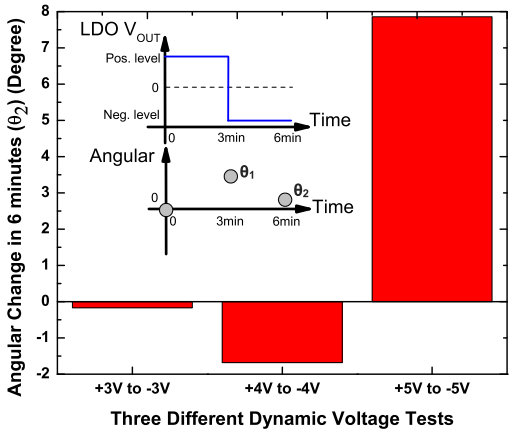


Figure 4.9: Measured changes in the angle (from 0 to θ_2 in 6 minutes) for three different dynamic tests.

4.3.2.3 Movement Characterization-Measuring Angular Changes in response to Rapid Voltage Changes

In the case of muscle prosthesis, there may be situations where the applied electric field is changed instantly to a new value. As such it is important to study how the iEAPs respond to sudden changes in the electric field level. To evaluate this, the worst case scenario was considered. That is, the electric field was continuously applied at a given value for 3 minutes, where as a result, the hydrogel bent towards the negative electrode with angle θ_1. At the end of the third minute, the polarity of the electrodes was changed, that is an electric field of the same magnitude but in the opposite direction was applied, and held for another 3 minutes, and the response of the hydrogel in terms of changes in the angle was studied.

Fig. 4.9 shows the measured results of the dynamic test, for three voltage levels. Ideally, one should expect that if a voltage of an opposite polarity is applied and held for the same duration as the initial stimulation period, the bending angle at the sixth minute (θ_2), should go back to the initial state value where there was no stimulation. However, the results demonstrate that this expectation is not held when the applied voltage increases. This observation can be related to the strength of the applied field. Since the water is bound to the positive ions that move in the field over time, an increase in the field strength leads to more water in the hydrogel, over time. If there is more water present in the hydrogel, a greater change in the angle can be expected from the initial state to the time when the polarity is changed (here the end of the 3-minute period). This behavior can be further modified by making sure that the hydrogels are completely saturated prior to testing.

4.3.3 Summary of the *In Vitro* Characterization Experiment

The experimental results presented here for the electrical and movement characteristics of the developed biocompatible iEAPs in the presence of electrical stimulation provided via an LDO, demonstrate the potential application of the proposed module for use as muscle prosthesis. The results are particularly important for providing insights on designing the stimulator and understanding the functionality and limitations of iEAPs.

4.4 Design Considerations of the LDO

The experiments in the last section demonstrates the feasibility in using the LDO to function as the stimulator. For the subcutaneous module, however, as it will be discussed in this section, there will be several added design challenges (e.g., variation in load and power supply). Here, we will discuss these challenges, and provide design solutions.

4.4.1 Design challenges of the LDO

The proposed LDO, powering-up via a WPT link, is expected to provide a stable and reliable voltage for actuating iEAPs. The design challenges for the LDO are imposed by the requirements of the application, properties of iEAPs, and the nature of WPT links. The system level design challenges have been reviewed in Section 2.2. Here, an in-depth description of the challenges for the LDO design is provided.

Area Limitation: The LDO will be integrated with the iEAPs and implanted inside the body. As a result, the circuit should occupy a very small space. Therefore, regulator architectures that require inductors will not be appropriate for this application. Since LDOs do not require inductors, they can be utilized in this application, to meet the area requirement. LDOs generally require μF level external capacitors at their outputs, where the capacitance value depends on the switching characteristics of the load. For the proposed application, due to the intrinsic non-switching property of iEAPs, as far as the stability of the LDO is not compromised, the external capacitor can be removed to save area. However, the elimination of the output capacitor makes maintaining stability a challenging task, when using conventional LDO structures. The reason is that in conventional LDOs, the only dominant pole in the loop gain transfer function is the reciprocal of the time constant formed by the output capacitance, the equivalent series resistance (ESR) of the output capacitor, and the equivalent load resistance [255]. Without the output capacitors, the LDO will suffer from the instability problem. Therefore, efforts must be made to address the tradeoff between area limitation and stability.

Load variation: The range of load variation imposed by the electrical characteristics of iEAPs is unique to this application and places design challenges for the LDO. With a supply voltage of *2.5* V, output voltage of *1.5* V, and using (4.1), the load range is expected to vary

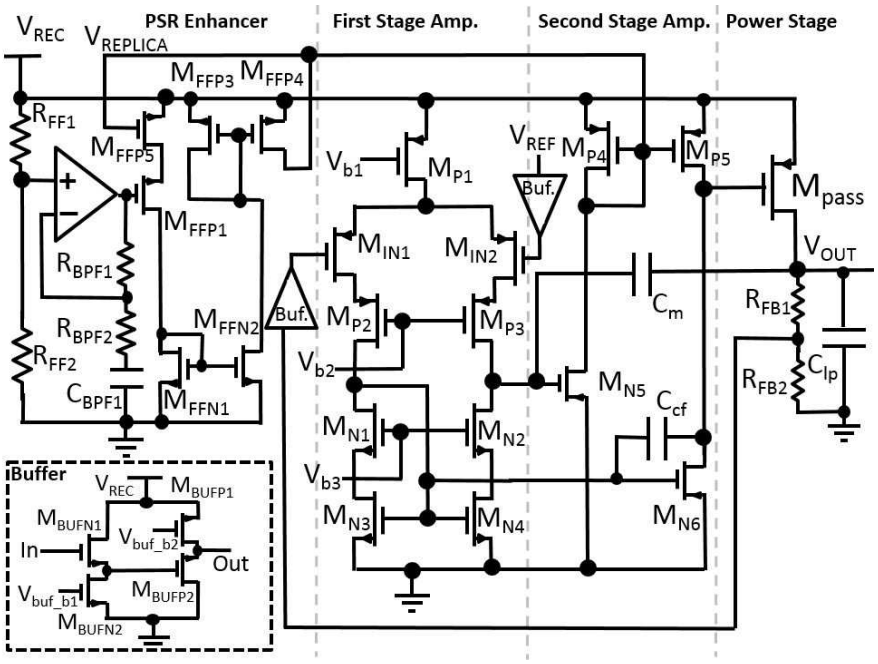


Figure 4.10: Schematic for the proposed external-capacitor-less LDO with PSR enhancer.

between *33* mA to *276* mA. As discussed before, the dominant pole will depend on the equivalent load resistance. As a result, for wide load range applications, the LDOs' stability could be compromised. Thus, the load dependency of the dominant pole in the loop gain transfer function must be suppressed or eliminated to meet wide load variation conditions.

Line variation: The LDO is powered via a WPT link, which can introduce variations in LDO's power supply. Such variations could occur by for example the misalignment between the primary and secondary coil in the inductive link [258]. Additionally, due to the switching nature of WPT, AC ripple (which depending on the switching frequency, could be in the range of *100* kHz to several MHz) could appear in the circuit's power line [258]. Therefore, the LDO, including its reference circuit, will have to exhibit strong power supply rejection in DC and mid-frequency range, to provide a very stable voltage regardless of variations in the supply rail.

4.4.2 Proposed LDO

To meet the design challenges discussed above, an external-capacitor-less LDO is designed (see Fig. 4.10), to create the electric field required for stimulating iEAPs. The design is motivated by the architecture proposed in [259]. The circuit consists of three major blocks: the PSR enhancer, an error amplifier consisting of two stages, and the power block. The PSR enhancer block is used to improve the PSR in mid-frequency range (*100* kHz to several MHz) [122]. In this structure, resistors R_{FF1} and R_{FF2} form a resistor divider to sample the AC noise from the power line. This sampled signal goes through a bandpass filter, constructed by one operational amplifier, two feedback resistors (resistors R_{BPF1} and R_{BPF2}), and capacitor C_{BPF1}. The output of the bandpass filter then drives the transistor M_{FFP1} to generate a current which contains the AC component of the power line. The transistor M_{FFP5} is driven by the feedback signal $V_{REPLICA}$ from the second stage of the error amplifier, to regulate the PSR enhancer loop. The current going through transistor M_{FFP5} and M_{FFP1} is then mirrored (via transistors M_{FFN1}, M_{FFN2}, M_{FFP3} and M_{FFP4}) and injected into the second stage of the error amplifier. Two input buffer circuits (consisting of transistors M_{BUFN1}, M_{BUFN2}, M_{BUFP1} and M_{BUFP2}) are employed to provide the appropriate common mode DC input level and better PSR at low frequencies [122]. A telescopic configuration consisting of transistors M_{IN1}, M_{IN2}, M_{P1}-M_{P3} and M_{N1}-M_{N4} form the main body of this block. The output of this stage is also connected to V_{OUT} of LDO via a Miller capacitor, C_m. In the third block, the second stage of the error amplifier, transistors M_{N5}, M_{P4} and M_{P5} form a non-inverting gain stage. Transistor M_{N6} and the capacitor C_{cf} connect this stage to the second block in order to damp the non-dominant poles (quality factor reduction) [260]. The last block forms the power stage. In this stage, the pass transistor, M_{PASS}, operates as a variable resistor to keep the output level relatively constant over the entire load range. Resistors R_{FB1} and R_{FB2} build the sampling network at the LDO output, and a *100* pF parasitic capacitor C_{lp} is used to model the capacitive properties of bond pads.

The schematic of the reference circuit [206] used in the proposed LDO is shown in Fig. 4.11. The PSR enhancer [234], an operational amplifier, PTAT current and V_{REF} generators form the four blocks of the circuit. Compared to CMOS-based bandgap references that utilize

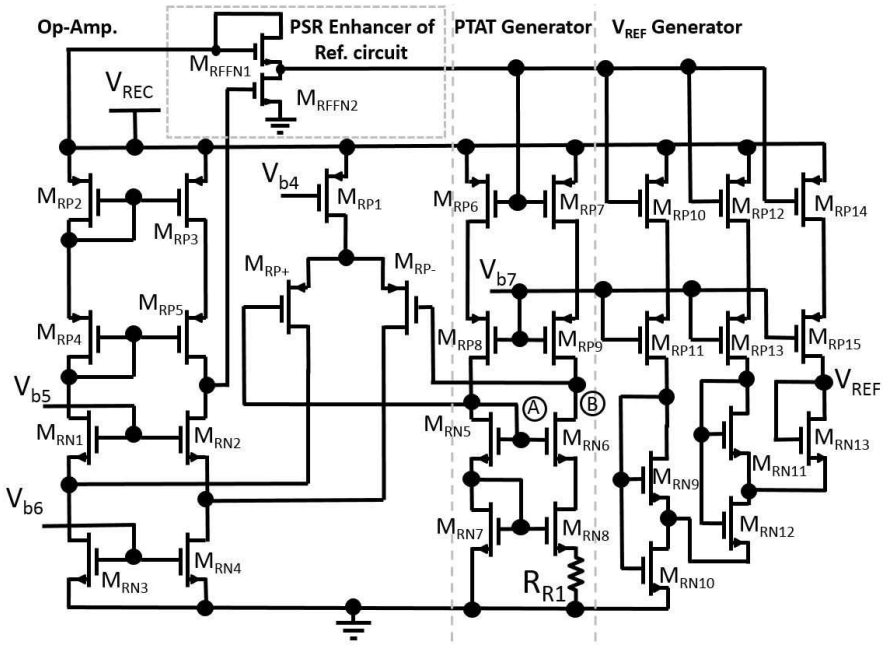


Figure 4.11: Schematic of the voltage reference circuit with PSR enhancer.

parasitic BJTs, this reference circuit offers several advantages, including reliability, low power consumption, and stable line regulation. The introduction of PSR enhancer will additionally improve the power supply rejection ratio of the reference circuit, thereby, minimizing its impact on the performance of LDO. In Fig. 4.11, the PSR enhancer stage samples the AC component from the power line V_{REC}, via transistors M_{RFFN1} and M_{RFFN2}. The output of the PSR enhancer is then used to drive the transistors in PTAT current and V_{REF} generators stages. The operational amplifier uses a folded cascode configuration (M_{RP1}, M_{RP+}, M_{RP-}, M_{RP2}-M_{RP5} and M_{RN1}-M_{RN4}), thereby, providing large-enough DC gain to maintain equal voltage levels at nodes "A" and "B" in the PTAT current generator circuit. The PTAT current generator circuit consists of cascode current mirror pairs (M_{RP6}-M_{RP9}). The PTAT Four subthreshold-operating transistors M_{RN5}-M_{RN8} are used to generate the PTAT voltage across resistor R_{R1}. The generated PTAT current is then mirrored to the V_{REF} generator block through transistors M_{RP10}-M_{RP15}. Transistors M_{RN9}-M_{RN13}) operate in weak inversion. The output voltage of this reference circuit, V_{REF}, is generated from the gate-source voltages of transistors M_{RN9}-M_{RN13}.

In what follows, we will describe how the proposed design meets the design requirements discussed in Section 4.4.1.

Area Limitation: As discussed, in this iEAP application, a tradeoff exists between chip area and stability. Therefore, the external-capacitor-less LDO architecture [261] is selected to address this challenge. In this type of architecture, due to the non-existence of output capacitors, no intrinsic dominant pole exists in low frequency range. However, in mid-frequency range, two poles can be split via Miller compensation. One will be placed within the low frequency range and could work as the dominant pole in the loop, while the other will be pushed to frequencies well above the loop bandwidth. This pole splitting technique successfully solves the stability problem when the output capacitor is not present. As a result, it will be a suitable technique to address the area-stability tradeoff.

Load variation: The LDO is required to generate a stable and precise voltage for all load conditions. Since the external-capacitor-less structure is used, to ensure stability against load variation and to keep a relatively constant bandwidth and phase margin across the entire load range, the dominant pole can be designed to be independent of the load, and the load-dependent non-dominant poles will be kept at frequencies well above the application bandwidth. Additionally, the error amplifier used in LDO should provide a large low frequency gain across the entire load range. To achieve a large gain, the two-stage structure has been used.

Line variation: To enhance line regulation (low frequency PSR) of the LDO, cascode structures (consisting of transistors M_{P2}, M_{P3}, M_{N1} and M_{N2}) [255] have been incorporated in the reference circuit and the main stage of the LDO. Additionally, two different PSR enhancers are included in the reference circuit and the main stage of the LDO, to address the mid-frequency (*100* kHz to several MHz) suppression of the noise coming from the supply line.

4.4.3 Simulation Results

The proposed LDO was designed and simulated in IBM *0.13-*μm CMOS technology. The circuit was designed to operate with a power supply of *2.5* V. Fig. 4.12-a shows the simulation results of the loop gain (magnitude and phase) for four load conditions (no load, light load (*10* mA), medium load (*50* mA) and full load (*300* mA)). It can be seen that both unity gain frequency and phase margin stay relatively the same (*500* kHz and *70*°) for all load conditions, ensuring the LDO remains stable across all load ranges. Fig. 4.12-b shows the simulation results for the PSR of the LDO (for three load conditions, with and without PSR enhancer) and

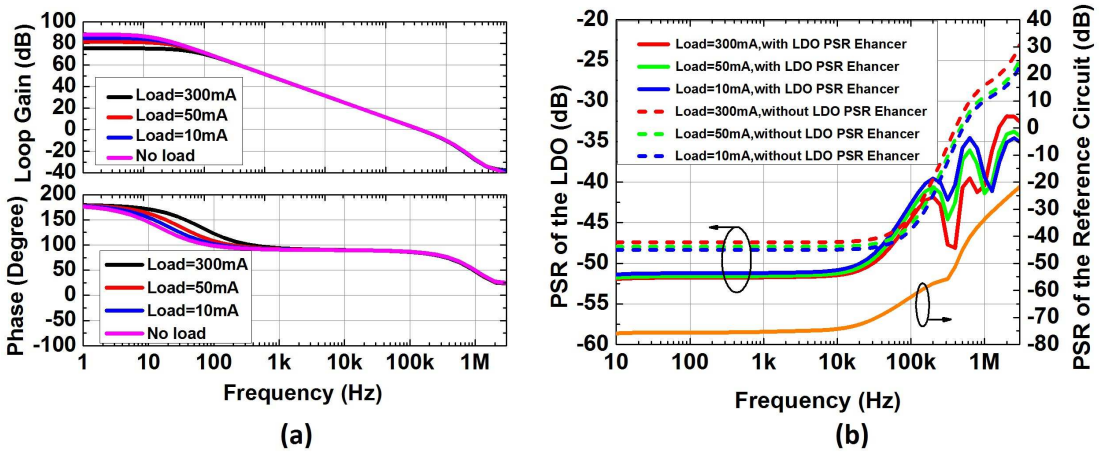


Figure 4.12: Simulation results at V_{REC}=2.5 V for a) the loop gain at four different load conditions, b) the power supply rejection (up to 3 MHz) of reference circuit and LDO at three load conditions, with and without PSR enhancer.

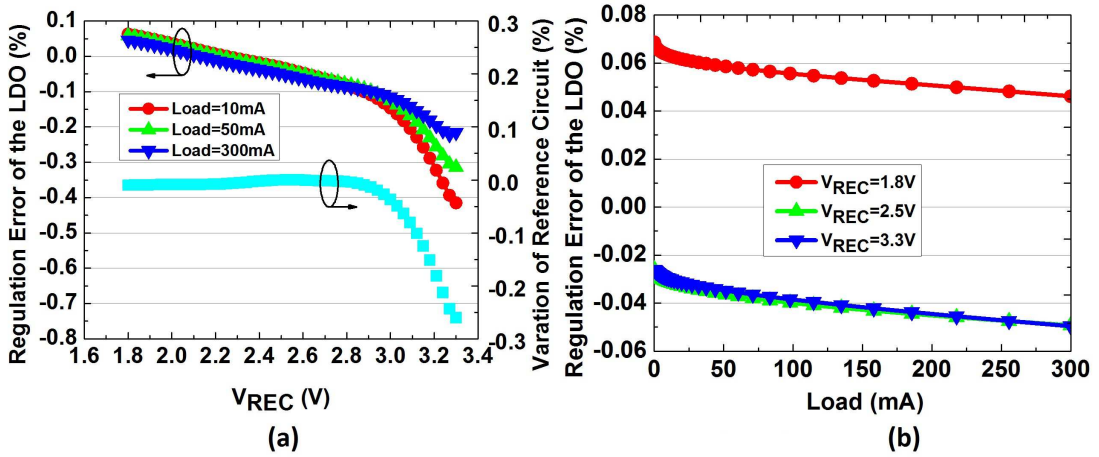


Figure 4.13: Simulation results for a) Line regulation, b) Load regulation.

the reference circuit. The circuit demonstrates good suppression of the mid-frequency (*100 kHz* to several MHz) noise. The worst case PSR is found to be *-40 dB* at *1 MHz*.

Simulation results for line and load regulations are shown in Figs. 4.13-a and 4.13-b, respectively. In Fig. 4.13-a, the percentage of output voltage variation when the power line varies from *1.8 V* to *3.3 V* is plotted. It can be seen that the error is within *-0.45 %* and *+0.1 %* for all three load conditions. Note that for this simulation, we have incorporated the variation in the reference voltage value that occurs as a consequence of changes in the supply voltage. Fig. 4.13-b shows the percentage variation in the output voltage as a function of the load, for three supply voltage values. The results indicate that the peak to peak variation stays within

Table 4.1: Performance comparison to the existing external-capacitor-less LDOs

	[259]	**[262]**	**[121]**	**This work**
Year	2012	2014	2014	2015
Technology (μm)	0.13	0.18	0.065	0.13
Type (Measurement/Simulation)	Measurement	Measurement	Sim.	Sim.
Max load (mA)	50	50	50	300
V_{OUT} (V)	1	1.6	1	1.5
C_{OUT} (pF)	20	100	100	100
Load reg. (mV/mA)	N/A	0.14	0.03	0.001163
PSR at 1 MHz (dB)	-40	-70	-48	-40

-0.06 % and *+0.08 %* over the entire load range with different line voltages. Both line and load regulation results confirm the stability of the proposed LDO, indicating that it will be a good candidate for actuating iEAPs in muscle prostheses.

The performance of the proposed LDO and existing external-capacitor-less LDO designs have been compared in Table 4.1. The proposed LDO demonstrates a comparable PSR at *1* MHz, and provides superior load regulation across a wide load range.

4.4.4 Summary of the LDO Design

In this section, an external-capacitor-less LDO with PSR enhancer circuit for providing subcutaneous electrical stimulation to iEAPs in muscle prosthesis applications was presented. The proposed LDO provides a *1.5* V stable output voltage to stimulate iEAPs of different lengths. Simulation results showed good stability, superior line and load regulations over *10* to *300* mA load range. The results suggest that the proposed LDO can be used as an effective solution for electrical stimulation of iEAPs in subcutaneous muscle prostheses.

4.5 Wireless Tuning Technique

In the last section, an external-capacitor-less LDO circuit meeting the requirements of iEAPs was presented. However, remote tuning the LDO and providing multi-level outputs were not considered. Since the iEAPs' degree of movement will be controlled by the level of the voltage provided by LDO, the LDO should be capable of providing multiple output levels. Two possible classes of solutions to develop a multi-level regulator are 1) use of one LDO with the capability

of tunable output, and 2) use of multiple LDO structures [263] along with a programmable multiple rail for enabling/disabling LDOs. Because of the limitation of area and space on the implant side, the first class of solutions will be considered here.

To remotely tune the output of the LDO, techniques for communicating with the LDO should be developed. Commonly used digital communication schemes mentioned in Section 2.3 typically require modulation and demodulation circuitry, clock generators and digital blocks, and thus adding to the overall implant size. For the application under this study, the output voltage level and the amplitude of the LDO is the main parameter that needs to be controlled. Additionally, reverse telemetry is not required. Therefore, the use of digital telemetry schemes will be neither power nor space efficient. By taking these two issues into account, a low-cost analog-based solution is highly desired for controlling both the direction and the degree of the movement of the iEAPs.

To develop an analog-based wireless tuning technique, the key point is to find a robust control variable, which can be preserved without loss during the transmission over the wireless coils. Consequently, the efforts in finding the target control variable must be paid by revisiting the basic magnetics theory. For a sinusoidal signal with the specific peak-to-peak amplitude and frequency, the useful information includes the frequency, the amplitude, and the sinusoidal shape. On the one hand, it is found that the frequency information is consistent at both transmitter side and the receiver side of the magnetic materials (the transformer, the coupled inductors, and the wireless coils). Furthermore, for the biomedical implant or other subcutaneous applications using wireless coils, the preservation of the frequency information is not affected by the presence of the tissue as the transmission medium between the coils. On the other hand, the amplitude of the sinusoidal signal is very sensitive to the operating conditions, such as the coupling strength of two coils. Likewise, the sinusoidal shape is not reliable either given that it may be distorted by the interference from the other links. In summary, the frequency information is picked as the key parameter to initialize the development of the desired wireless tuning technique. In this section, this analog-based technique that enables remote tuning of the output voltage of LDO is presented. To the best of our knowledge, this is the first time the concept is being introduced in biomedical implants.

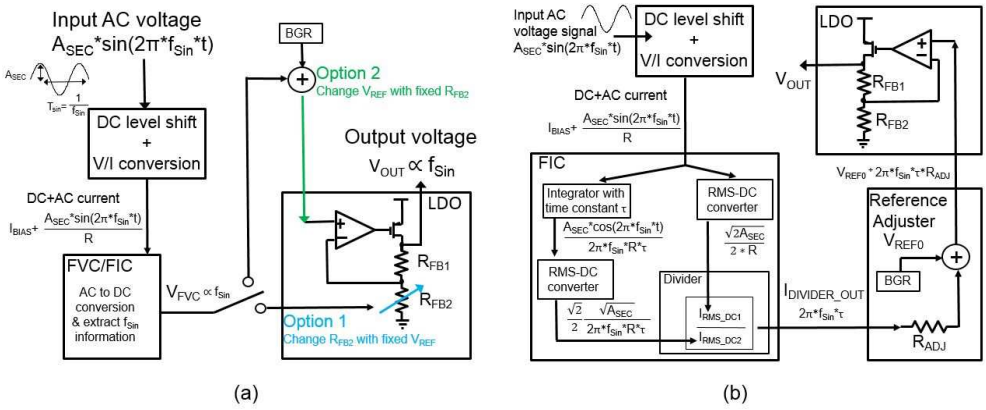


Figure 4.14: a) Conceptual representation of the frequency-based tuning technique for wirelessly tunable LDO, and b) detailed block diagram of the proposed technique.

4.5.1 Proposed Wirelessly Tunable Technique

As discussed above, the LDO with multiple voltage level capability will be required for the development of the next generation iEAP-based muscle prosthesis. To save on the power, area, and space on the implant side, the single LDO design option is considered.

The proposed idea for wirelessly tuning the LDO is realized upon the concept of frequency-based telemetry [264]. The frequency-based telemetry concept utilizes frequency-to-voltage converter (FVC) or frequency-to-current converter (FIC) to generate an electrical signal (voltage/current) at the secondary (receiver) side that will be related to the frequency of the periodic signal at the primary (transmitter) side. In the application of interest, since the frequency of generated electrical waveform at the primary and secondary sides of the inductive link will be identical [258], frequency-based telemetry can be used to provide remote tune capability to this class of biomedical implants, with the frequency at the transmitter side being the control signal. By using FIC or FVC, the electrical signal related to the frequency applied to the primary coil will be generated, which can then be used to tune the output voltage of the LDO at the receiver side.

The design of proposed tunable LDO includes two major sections: 1) design of FIC/FVC block, and 2) choice of the control mechanism that will be used to tune the output voltage of the LDO. The conceptual block diagram is shown in Fig. 4.14-a with two possible realization options for the control block.

The choice of the architecture for the frequency conversion block depends on the nature of the input signal and whether it is sinusoidal [265] or square waveform [266]. Here, we consider the input signal received at the secondary coil to be sinusoidal. We also consider the FIC architecture [265] which, as we will discuss later, offers an advantage of being insensitive to the variations in the amplitude of the input signal.

For the choice of the control mechanism block, we note that the output voltage of the LDO is determined by two main parameters: the reference level (V_{REF}) and the ratio of two resistors R_{FB1} and R_{FB2}. Based on these two parameters, two possible options for the control mechanism are illustrated in Fig. 4.14-a. In the first option (Option 1) the reference level is fixed, and the output of LDO is controlled by varying the resistors [267]. In the second option (Option 2), the resistors are fixed, and the reference level from the BGR is adjusted [268]. The realization of the first option would require the replacement of either R_{FB1} or R_{FB2} with a programmable resistor network, switches for the selection of appropriate resistors, and an analog-to-digital converter (ADC) to convert the output from FVC/FIC to a digital signal for controlling the switches. In the second option, the reference level can be adjusted based on the current generated from the FIC. To save power and area on the implant side, it is apparent that the second option is the appropriate choice for this application. Fig. 4.14-b illustrates the conceptual representation for the proposed wirelessly tunable LDO. The technique has several advantages including simplicity (no antenna/ receiver /modulator /demodulator /data recovering circuits /oscillator needed at the secondary side), integrability and CMOS compatibility, low power consumption, and low noise (no switching action is required).

4.5.2 Circuit Implementation

Here, transistor level implementation of the proposed wirelessly tunable LDO is presented. As shown in Fig. 4.14-b, the AC component of the input voltage is first converted to an AC current with DC offset. This signal is then mirrored to flow into two blocks that form the FIC (Fig. 4.15-a). The first mirrored signal is integrated and then converted to the DC level equivalent to the RMS value of the AC input signal (Fig. 4.15-b), and the second mirrored signal flows into another RMS-DC converter to generate a second level DC signal (Fig. 4.15-c). Fig. 4.15-d shows the divider circuit generating an output current that will be proportional to the input

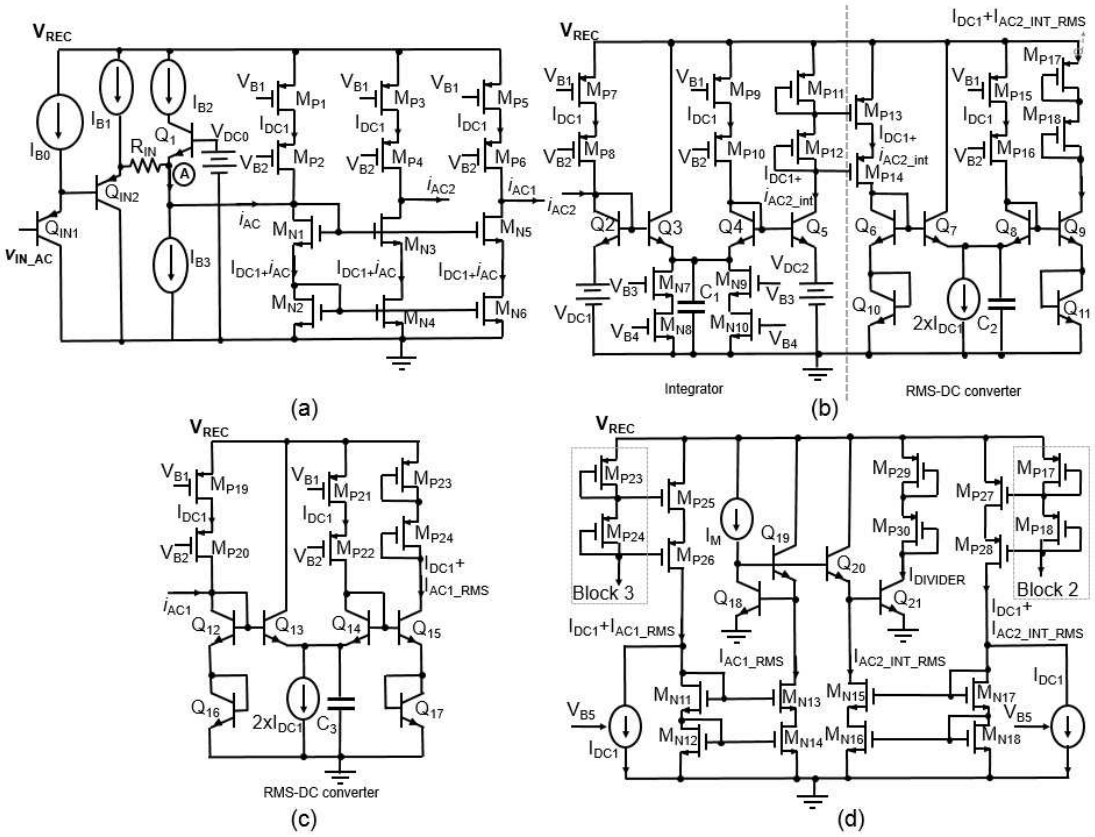


Figure 4.15: Schematic of four major blocks of FIC, a) block 1-the input stage b) block 2-the integrator and the RMS-DC converter for i_{AC2}, c) block 3- the RMS-DC converter for i_{AC1}, and d) block 4-the current divider.

frequency [265].

Both the integrator and the RMS-DC converter are implemented by bipolar transistors. However, they can also be implemented using conventional CMOS technologies. For RMS-DC converters and current dividers, the bipolar devices can be replaced by subthreshold-operating MOSFETs, and the integrator can be implemented with CMOS-based operational transconductance amplifier (OTA), with wide input range. We will now discuss details of circuit blocks used to implement the proposed wirelessly tunable LDO.

FIC: Input stage-The schematic of the input stage is shown in Fig. 4.15-a. This stage converts the input AC signal into a current that will be fed into next stages. The DC level of the input voltage is first adjusted via two PNP-based level shifters. An AC current with DC offset is then produced with node "A" being set as a virtual ground. After proper DC cancellation, the AC current will go into the current buffer. Transistors M_{P1}-M_{P6} are biased by external

DC voltages V_{B1} and V_{B2} to generate DC currents. Transistors M_{N1}-M_{N2} are self-biased to include both DC and AC components. The $DC + AC$ current is then mirrored through transistors M_{N3}-M_{N6} into two different branches. By proper DC cancellation, two AC outputs i_{AC1} and i_{AC2} are generated to go to the subsequent blocks.

FIC: Integrator stage-The integrator is shown in Fig. 4.15-b and consists of transistors M_{P7}-M_{P12}, M_{N7}-M_{N10}, Q_2-Q_5, one capacitor C_1 and two DC voltages V_{DC1} and V_{DC2}, to execute the integration operation on the current [269].

FIC: RMS-DC converter stage-The RMS-DC converters are shown in both blocks 2 (Fig. 4.15-b) and 3 (Fig. 4.15-c). Note that accurate RMS-DC conversion is achieved through the precise controlling of the current sinks [270].

FIC: Current divider stage-The current divider circuit shown in Fig. 4.15-d consists of two "biased current cancellation" circuits and the core divider. The output currents in blocks 2 and 3 both contain the biased DC current and the generated DC current from the corresponding AC inputs. For example, transistors M_{P25} and M_{P26} mirror the output current from block 3, and subtract the biased DC current I_{DC1} and feed the remaining DC current I_{AC1_RMS} to the divider. Similarly, the DC component $I_{AC2\_INT\_RMS}$ from block 2 is extracted, and finally, the output current $I_{DIVIDER}$ becomes proportional to the input frequency.

Reference level adjuster-Ideally, the output current is expected to have negligible ripple. However, due to the nonlinear operation of the current divider, the AC ripple in the current $I_{DIVIDER}$ may still be observable. One solution to reduce the AC ripple is to introduce a low pass filter (LPF). As shown in Fig. 4.16, two RC LPFs (resistors R_1, R_2 and capacitors C_4, C_5) are added at the gate terminal of transistors M_{P29} and M_{P30}. As a result, the mirrored and scaled current I_{FIC_LPF} will be a current with negligible AC ripple. This current is buffered through the transistor M_{P32} to generate the adjustable reference level V_{REF_ADJ}, and consequently, the output voltage of the LDO V_{OUT} [268].

4.5.3 Simulation Results

The proposed technique was implemented and extensively simulated in IBM's *0.13-*μm BiCMOS technology. The circuit was designed to operate with V_{REC}=2.5 V. The input frequency range was varied between 20 kHz to 100 [20]. For realizing the references and the LDO, we

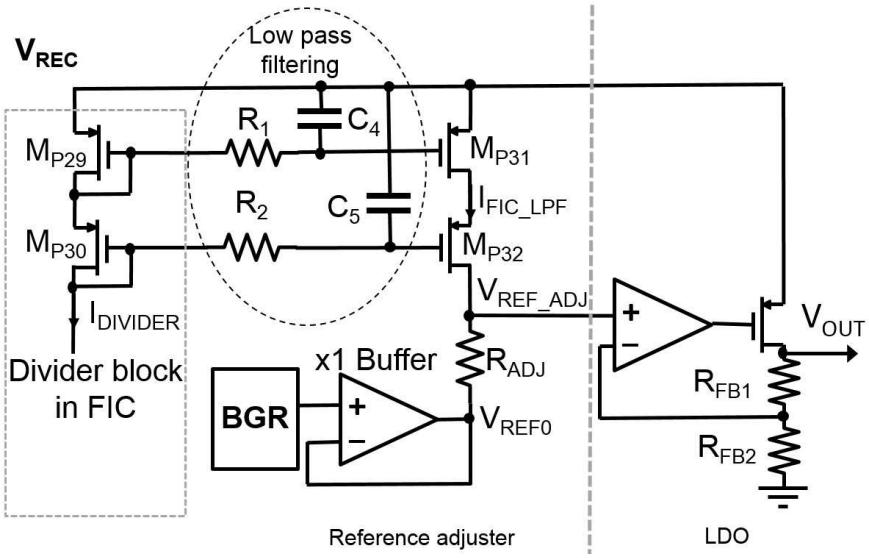


Figure 4.16: Schematic of the reference adjuster and the LDO.

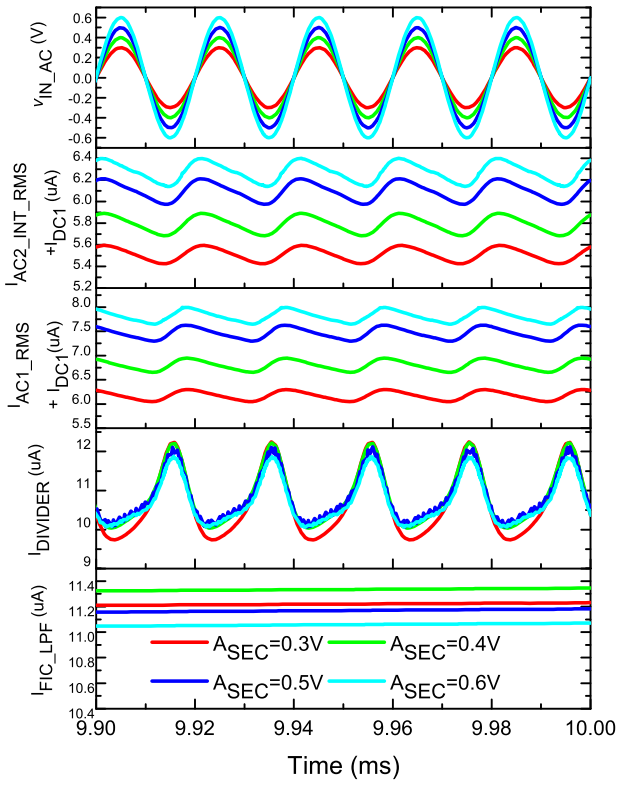


Figure 4.17: Steady state simulation results for $I_{DC1} + I_{AC2\_INT\_RMS}$, $I_{DC1} + I_{AC1\_RMS}$, $I_{DIVIDER}$ and I_{FIC_LPF} as the input signal amplitude varies from $0.3\ V$ to $0.6\ V$.

followed the structures in Section 4.4. With $V_{REC} = 2.5\ V$, the total power consumption of the circuits shown in Fig. 4.15 and Fig. 4.16 is around $400\ \mu W$, when f_{sin}=50 kHz.

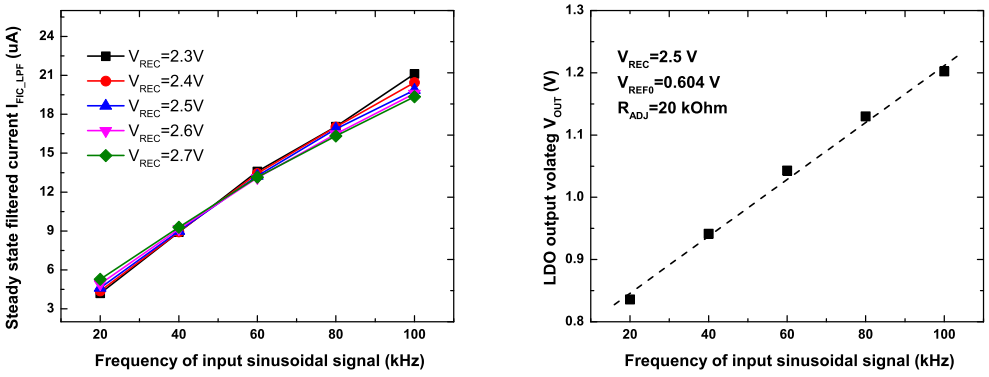
Fig. 4.17 shows steady state simulation results for currents in different parts of FIC for four different amplitudes of the input sinusoidal signal (A_{SEC}=0.3 V, 0.4 V, 0.5 V and 0.6 V) at f_{sin}=50 kHz. As shown in Fig. 4.17, variations in the input amplitude result in variations in the amplitude of the output currents of the two RMS-DC converters ($I_{DC1} + I_{AC2\_INT\_RMS}$ and $I_{DC1} + I_{AC1\_RMS}$), however, negligible variation is observed at the output current of the FIC ($I_{DIVIDER}$). After applying the LPFs, the variation in the current I_{FIC_LPF} that goes to the reference adjuster stays below $0.4\ \mu A$, with the nominal value sitting at $11.2\ \mu A$. Therefore, I_{FIC_LPF} has high stability to the variations in the amplitude of the input signal.

To validate the functionality of the proposed solution and evaluate the line regulation, different values for V_{REC} (2.3 V to 2.7 V) with input frequency ranging from 20 kHz to 100 kHz were considered, and results for I_{FIC_LPF} are plotted in Fig. 4.18-a. As can be seen, good linearity between the frequency of I_{FIC_LPF} and the input frequency is achieved for different values of V_{REC}. Furthermore, to probe the relationship between the input frequency and the LDO output, simulations were run at $V_{REC} = 2.5\ V$. The results are plotted in Fig. 4.18-b. The output voltage is linearly dependent on the frequency of the input signal.

Figs. 4.19-a and 4.19-b show simulation results for the adjustable reference level (V_{REF_ADJ}) and the output of LDO (V_{OUT}) when the frequency of the input signal transitions from 20 kHz to 80 kHz, and from 100 kHz to 50 kHz, respectively. The observed smooth transition of both V_{REF_ADJ} and V_{OUT} as the frequency varies, validates the dynamic voltage scaling capability of the proposed technique.

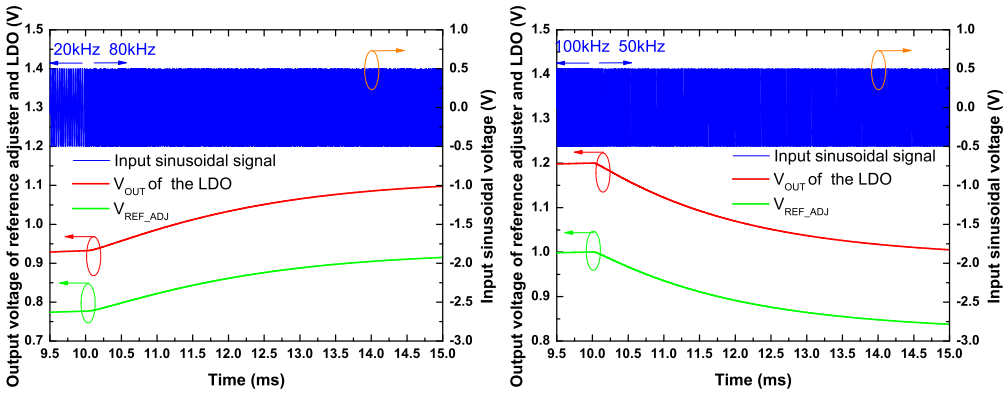
4.5.4 Summary of the Proposed Wireless Tuning Technique

In this section, a design technique for implementing wirelessly tunable LDOs was presented. Based on the frequency of the signal at the primary side, the output voltage level of the LDO at the secondary side can be tuned. Simulation results confirmed the functionality and the reliable operation of the proposed technique for different scenarios. The proposed wirelessly tunable LDO can be used as a stimulator for iEAPs in the next-generation muscle prosthesis with the advantage of enabling immediate movement restoration following implantation.



(a) (b)

Figure 4.18: Simulation results for a) steady state output current as a function of frequency at different values of V_{REC}, b) output voltage of LDO as a function of frequency at $V_{REC} = 2.5\ V$.



(a) (b)

Figure 4.19: Transient simulation results for V_{REF_ADJ} and V_{OUT} when input frequency varies a) from 20 kHz to 80 kHz, and b) from 100 kHz to 50 kHz at $V_{REC} = 2.5\ V$.

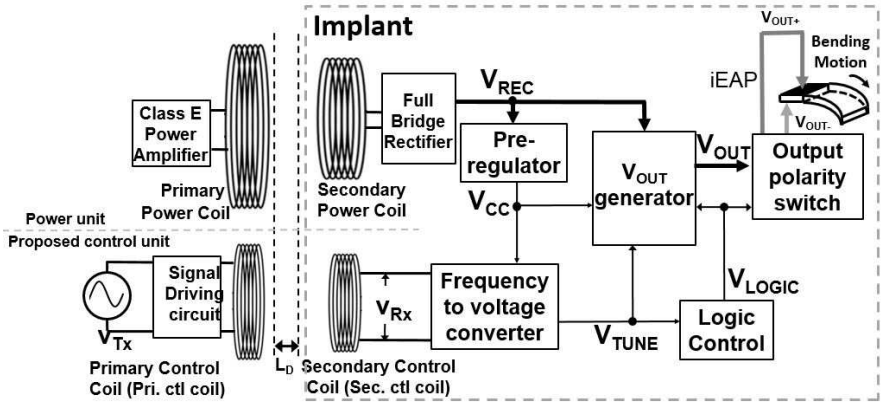


Figure 4.20: Block diagram of the proposed tunable electrical stimulator for iEAPs.

4.6 System Implementation

In the previous sections, we had demonstrated the concept of using an LDO to provide electrical stimulation to iEAPs. We also presented that the frequency can be utilized to generate tunable voltage magnitudes. However, only the voltage magnitude was made remotely tunable. In this section, we present a complete system capable of wireless tuning of both the magnitude and the polarity of the voltage, thereby, accommodating the stimulation requirements of iEAPs. While here we are targeting iEAPs, the proposed system can also be utilized in other biomedical applications where controllable electrical stimulation is required.

4.6.1 System Overview

The proposed system is designed to enable wireless tuning of both the degree and the direction of the movement of iEAPs. The application does not require stimulating a large number of sites to justify the incorporation of digital modulation schemes commonly used in implantable stimulators [111, 112, 114–116, 118]. As such, in order to save on the area and size of the implant, an alternative solution is proposed.

Fig. 4.20 shows the block diagram of the proposed stimulator, where the power unit is also included for wirelessly powering up the circuits on the secondary side. To provide tunable stimulation, the proposed control unit uses the frequency on the primary side as the control variable. This is motivated by the fact that unlike the amplitude, the frequency of the signal received at the secondary side is immune to attenuation and distortion that could be experienced

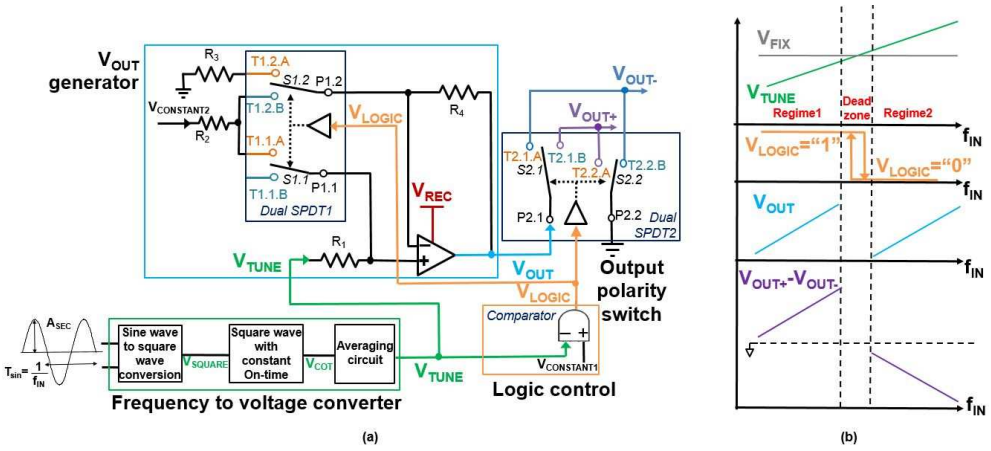


Figure 4.21: a) Block diagram of the proposed wirelessly-controlled electrical stimulator system, and b) signals versus input frequency range.

across the inductive link, particularly in biomedical implants. The overall aim here is to design a system-level solution through which both the polarity and the magnitude of the electric field at the secondary side, can be controlled by tuning the frequency at the primary side.

To be able to tune both the polarity and the magnitude of the output voltage using the input frequency, it is proposed to divide the input frequency range into three regimes (see Fig. 4.21-b). The input frequencies corresponding to “Regime 1” will be used to generate output voltages with positive polarity, and the input frequencies corresponding to “Regime 2” will be used to generate output voltages with negative polarity. Therefore, the inductive link and the resonant circuitry at the control unit should be designed such that a reasonably flat response is obtained across the frequency range considered for tuning.

In order to use the input frequency (f_{IN}) as the control variable, it needs to be converted to an electrical signal [271] with a magnitude proportional to the frequency. The conversion can be achieved through the use of FVC units. One way to realize the FVC unit is shown in Fig. 4.21-a. This FVC unit consists of three main stages. From the first stage, a square waveform, V_{SQAURE}, with the same frequency as the received signal is generated. Although the theory proposed in Section 4.5 is based on a direct conversion of the frequency of the sinusoidal signal, it is found that it is more beneficial by using the frequency of the square wave by FVC. Converting the signal into a square waveform at this stage can ensure the preservation of the frequency information, despite the distortion that may occur in the amplitude, or the shape of the received

signal after going through the inductive link. In the following stage, using the rising edges of V_{SQUARE}, the square waveform V_{COT} with the same frequency as f_{IN} but constant "On"-time duration (T_{ON}) is generated. That is, regardless of what the input frequency is, the duration of the "On" period of the square waveform V_{COT} will remain the same. Using this approach, the average of the square waveform V_{COT} will be directly related to its frequency (f_{IN}). As such, in the last stage, an averaging circuit is incorporated to generate V_{TUNE}, which equals the DC level of the V_{COT} waveform, obtained as

$$V_{\text{TUNE}} = V_{\text{CC}} \times D_{V_{\text{COT}}} = V_{\text{CC}} \times T_{\text{ON}} \times f_{\text{IN}}, \tag{4.2}$$

where $D_{\text{V}_{\text{COT}}}$ denotes the duty cycle of the V_{COT} square waveform, and V_{CC} refers to the high voltage level of the pulse during the "On" period. As (4.2) shows, the reliable conversion of the input frequency to V_{TUNE} is dependent on V_{CC}. Therefore, on the secondary side, the V_{CC} needs to be generated in a stable way and with minimum variations (which could, for example, occur due to coil misalignment in the power unit). As seen in Fig. 4.20, this goal can be achieved by using a pre-regulator. Variations in V_{REC} due to coil misalignment in the power unit will not be impacting the reliable operation of FVC unit, as long as the pre-regulator is operating normally. To further increase the reliability of the system, misalignment compensation approaches for the power links [258,272,273] can also be incorporated, but at the cost of added design complexity and increased space on the implant side.

Recall that depending on the input frequency (and to which regime in Fig. 4.21-b it belongs) the polarity and the magnitude of the output of the system should be determined. Fig. 4.21-a shows how this goal can be achieved, using V_{TUNE} and a comparator to generate a decision signal, V_{LOGIC}, which is then applied to two dual single pole double throw (SPDT) switches. The reference level input to the comparator ($V_{\text{CONSTANT1}}$) can be chosen based on the value of V_{TUNE} from the FVC unit, that is related to the frequency in the middle of the tuning range. To set the magnitude, a simple circuit for the realization of the V_{OUT} generator block in Fig. 4.20 is shown in Fig. 4.21. It is easy to see that depending on the state of V_{LOGIC}, the SPDT switch will make this stage to act as a voltage adder (when V_{LOGIC} is high) or a voltage subtractor (when V_{LOGIC} is low), to generate a frequency-dependent V_{OUT}. Resistors R_1 to R_4 can be selected such that the generated V_{OUT} for the two regimes have very close minimum and maximum

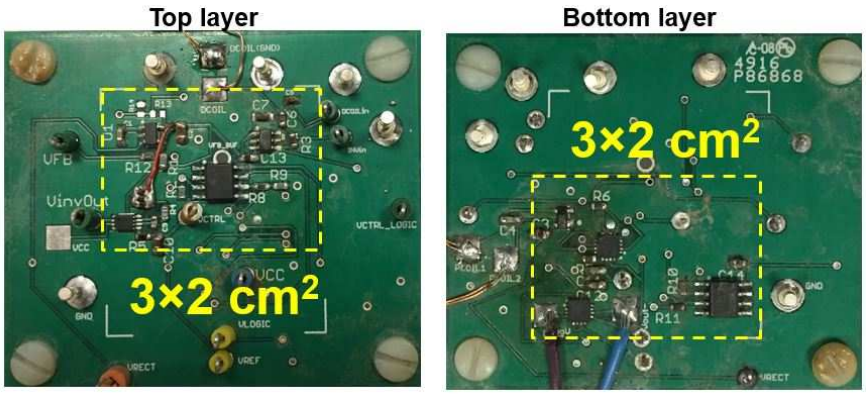


Figure 4.22: Top and bottom layers of the proof of concept circuit board.

values. Finally, to determine the polarity of the output voltage, a second dual SPDT switch is used. Based on the logic state of V_{LOGIC}, each of the two output terminals ($V_{\text{OUT-}}$ and $V_{\text{OUT+}}$) can be either at the ground level or be equal to V_{OUT}. Hence, the system is capable of providing an output voltage whose magnitude and polarity are wirelessly tunable through adjusting the frequency at the primary side.

4.6.2 Proof of Concept

As a proof of concept, the proposed system, consisting of both the power unit and the control unit, was built using commercial off-the-shelf components (COTS) products. A 2-layer PC board with an active area of $3 \times 2\ cm^2$ was designed and fabricated (Fig. 4.22). The key COTS items used in the proposed system include the pre-regulator [274], the op-amp in the V_{OUT} generator [275], and the switches with integrated comparator [276]. The information about the components used in building the class E power amplifier in the power unit, the driver circuit and the FVC unit can be found in Figs. 4.23, 4.24, and 4.25, respectively.

The system was designed to provide a tunable voltage within the range of 3 V to 5 V, with both positive and negative polarities. This voltage range was decided based on the results from Section 4.3. The carrier frequency for the power link was set at 13.56 MHz, which has also been previously used in other studies [277, 278]. The tunable frequency range for the control unit was chosen to be from 1 MHz to 5 MHz. This frequency range was selected based on the availability of coils and also making sure it is sufficiently distant from the carrier frequency of the power coil to minimize the cross talk. Frequencies in this range have been used in a series

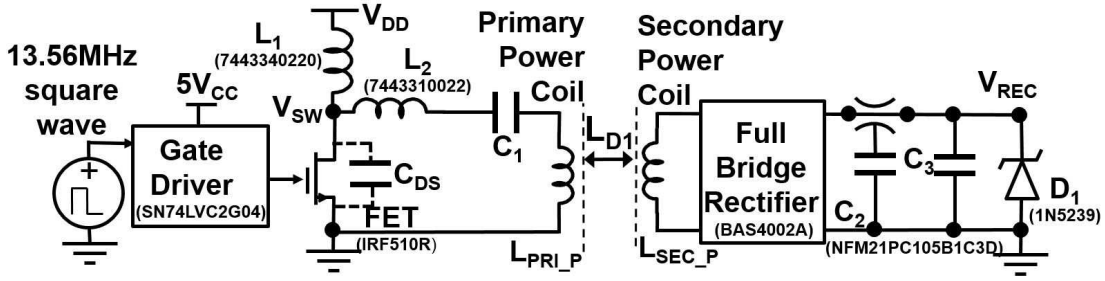


Figure 4.23: Schematic of the circuit used for the power unit.

of prior work focusing on biomedical implants [39, 279, 280]. The coils for each link were COTS products and were selected based on their Q values in the selected frequency ranges for the power and control units.

In what follows we provide details for the implementation of each block.

4.6.2.1 Power Unit

Wireless power transfer has been used in several studies for remote powering of biomedical implants [277, 278, 281–288]. The schematic of the wireless power transfer system used here to implement the power unit is shown in Fig. 4.23.

A 13.56 MHz square wave signal was used to drive the Class E power amplifier (PA) [289] on the primary side. By using a full-bridge rectifier, a raw DC voltage V_{REC} is generated to be used as the line voltage on the secondary side. A Zener diode is incorporated to avoid the instantaneous over voltage condition at V_{REC} and to protect succeeding components. Since V_{REC} can still suffer from ripples and variations (e.g. due to coil misalignment), an LDO powered up by V_{REC} is also included to generate a regulated supply voltage for the circuits used in the control unit (see Fig. 4.20).

4.6.2.2 Control Unit

Fig. 4.24-a shows the schematic for the inductive link at the control unit. The input signal via a voltage buffer goes to a seriesparallel (SP) inductively coupled data link [290]. The aim is to obtain a reasonably flat response across the considered tuning frequency range, and significant attenuation for frequencies outside this range, specially at 13.56 MHz, which is the carrier frequency in the power unit. The selected RLC components on the primary side and the

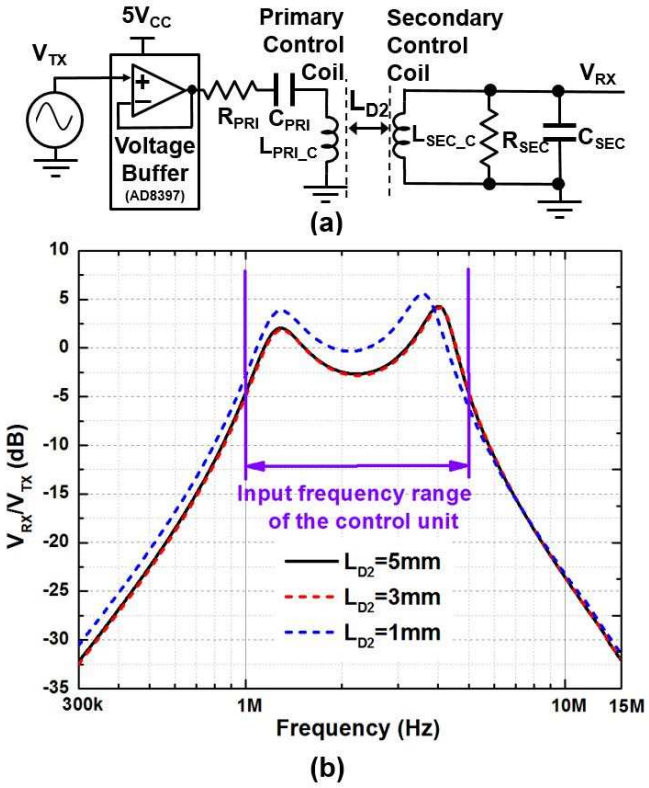


Figure 4.24: a) Schematic of inductive link in the control unit, and b) its measured frequency response under three different distances of primary and secondary coils.

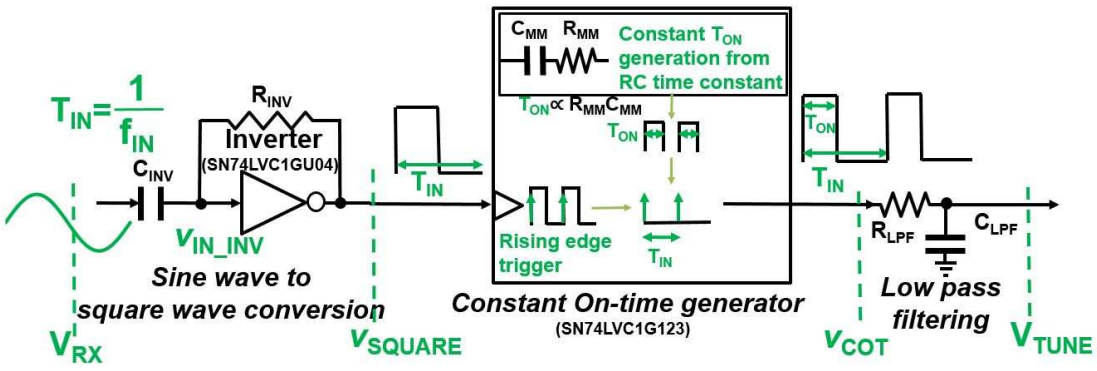


Figure 4.25: Schematic of the frequency to voltage conversion block.

secondary side form two resonant tanks around 1 MHz and 5 MHz [291]. Fig. 4.24-b shows the measured frequency response of the link for different distances between the two data coils. It can be seen that a reasonably flat response is obtained over the frequency range of 1 MHz to 5 MHz, while a rejection of more than 25 dB is achieved at 13.56 MHz. In the experiments, the distance between the two coils of the inductive link in the control unit was set to 5 mm.

The generated signal V_{Rx} in Fig. 4.24-a was then fed into the FVC block, which was implemented based on the circuit shown in Fig. 4.25. For the realization of the square waveform generator stage, capacitor C_{INV} and resistor R_{INV} along with an inverter are used. Assuming the current passing through R_{INV} is negligible, the DC voltage level at the inverter's input and the output are equal. As such, the inverter is biased in its linear mode acting as a high gain inverting amplifier [292, 293]. As a result, a square waveform can be generated at the output of the inverter with the same frequency as the input signal to the FVC stage. The constant "On"-time generator was implemented using a monostable multivibrator [294, 295]. The duration of "On" period was set to a fixed value using external components R_{MM} and C_{MM}. As discussed earlier, using this approach, the average of the generated square waveform will be directly related to the input frequency. For the last stage, an RC low pass filter (consisting of R_{LPF} and C_{LPF}) was designed to generate the averaged DC signal, V_{TUNE}. Dual SPDT switches were implemented using MAX4855. This COTS product also has an integrated comparator, which was used for realizing the logic control circuit shown in Fig. 4.21. The DC level of V_{LOGIC} determines the mode of the V_{OUT} generator (adder or subtractor) to create the targeted V_{OUT}.

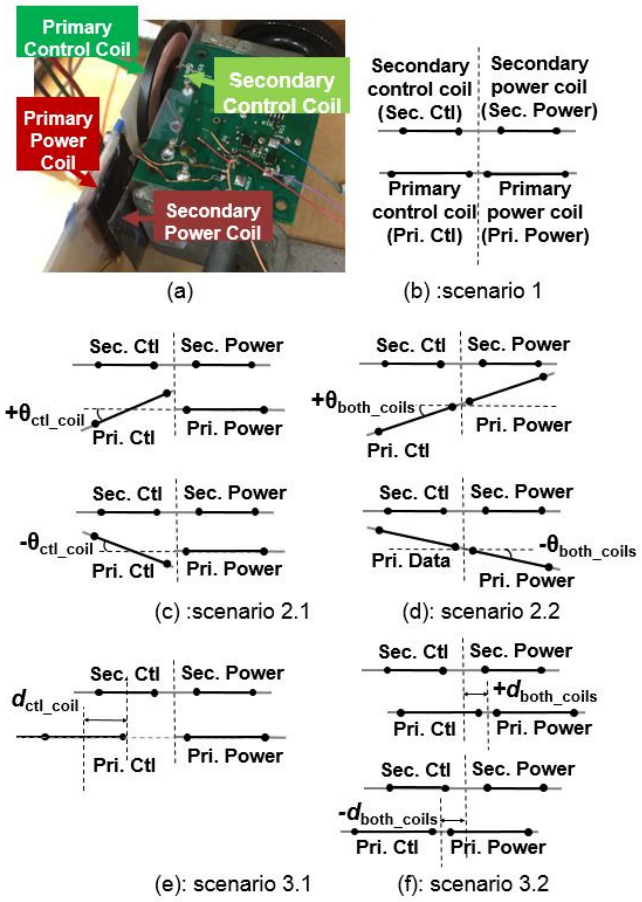


Figure 4.26: Illustration of the experimental setup and misalignment test scenarios: a) bench setup, b) *Scenario 1*: perfect alignment, c) *Scenario 2.1*: angular misalignment for the coils in the control unit, d) *Scenario 2.2*: angular misalignment for the coils in both power and control units, e) *Scenario 3.1*: axial misalignment for the coils in the control unit, and f) *Scenario 3.2*: axial misalignment for the coils of both the power and control units. In the figure, Pri., Sec., and Ctl are short for primary, secondary, and control, respectively.

4.6.3 Experimental Results-System Level Evaluation

Before utilizing the proposed system as the electrical stimulator for iEAPS, the performance of the system under different conditions was experimentally evaluated. In this section, we present and discuss these experimental results.

4.6.3.1 Experimental Setup

An Agilent 33250A function generator was used to generate the signal required for driving the class E PA in the power unit. A 7 V and a 5 V DC voltage from HP 6205C dual DC power

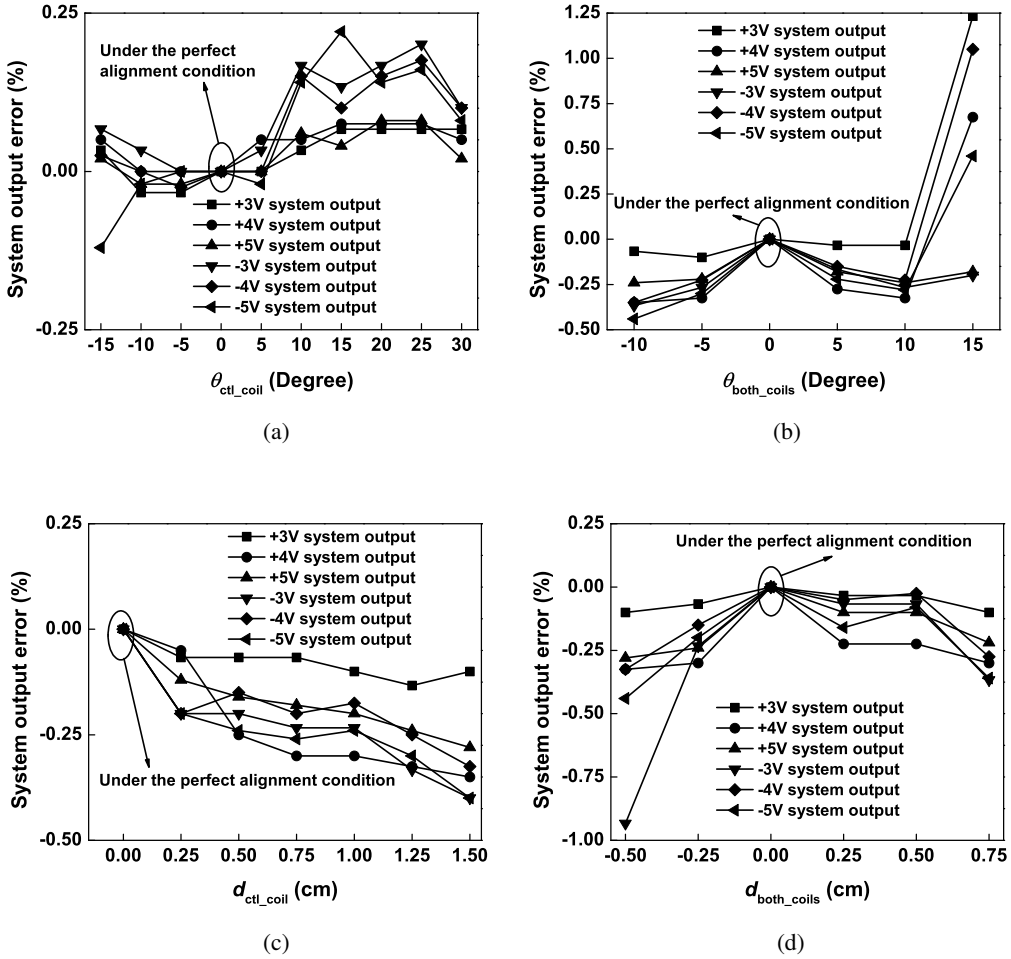


Figure 4.27: Measured percentage error in system output with respect to perfect alignment, under: a) *Scenario 2.1*- angular misalignment for the coils in the control unit, b) *Scenario 2.2*- angular misalignment for the coils in both units, c) *Scenario 3.1*- axial misalignment for the coils in the control unit, and d) *Scenario 3.2*- axial misalignment for the coils in both units.

supply were used for V_{DD} and for biasing the gate driver of the PA (see Fig. 4.23), respectively. The input signal to the transmitter side of the control unit was provided via a Tektronix AFG 3021 function generator.

4.6.3.2 Performance Evaluation in the Presence of Coil Misalignment

One of the major issues that can negatively impact the performance of the inductive links is the misalignment between the primary and secondary coils. Here, we evaluate the functionality and the robustness of the stimulator in providing reliable output under various misalignment scenarios. For each misalignment scenario, we considered two conditions, one when there is

misalignment between the coils of the control unit, and second, when there is misalignment between the coils of both the power and the control unit.

Three testing scenarios, as illustrated in Fig. 4.26, are considered. In *Scenario 1*, the primary and the secondary coils in both units are perfectly aligned (see Fig. 4.26-b). In *Scenario 2*, the coils experience angular misalignment. Under *Scenario 2.1* (Fig. 4.26-c), while the center points of the two coils in the control unit remain aligned, the primary coil is rotated by an angle $\theta_{\text{ctl\_coil}}$ from its ideal position. Under *Scenario 2.2* (Fig. 4.26-d) the primary coils in both units are rotated by an angle $\theta_{\text{both\_coils}}$ from their ideal position. In *Scenario 3*, the coils experience axial misalignment. Under *Scenario 3.1* (Fig. 4.26-e) the center point in coils in the control unit experience a shift by $d_{\text{ctl\_coils}}$, while under *Scenario 3.2* (Fig. 4.26-f), coils in both unit experience a shift by $d_{\text{both\_coils}}$. To evaluate the performance of the system under misalignment, first the system output voltage (differential voltage $V_{\text{OUT+}}$-$V_{\text{OUT-}}$) is measured under perfect alignment condition at six voltage levels (± 3 V, ± 4 V, and ± 5 V). For *Scenario 3.1* only shift in one direction was possible, as the the power coils were set to be in perfect alignment. At each misalignment testing condition, the output of the system is measured, and the percentage error with respect to output voltage at perfect alignment is calculated.

Measurement results for the percentage error in the system output are shown in Fig. 4.27 for all four misalignment testing conditions. As expected, the system is less tolerable to misalignment, when it occurs on both links. When misalignment occurs only between the coils of the control unit, the maximum error observed in differential output is lower than 0.5%, as observed in Fig. 4.27-c, for the axial misalignment related to the 1.5 cm shift. This robustness is due to the inclusion of the square-wave generator in the FVC unit, and the normal operation of the regulator. When misalignment occurs between the coils in both the control and power links, the system shows to be less tolerant. The maximum error is observed to be more than 1% for both axial and angular misalignment scenarios, which are obtained at less severe conditions as compared to when the misalignment occurred in the control unit only. This result indicates if severe cases of misalignment are expected in the application, compensation techniques need to be incorporated for the power link.

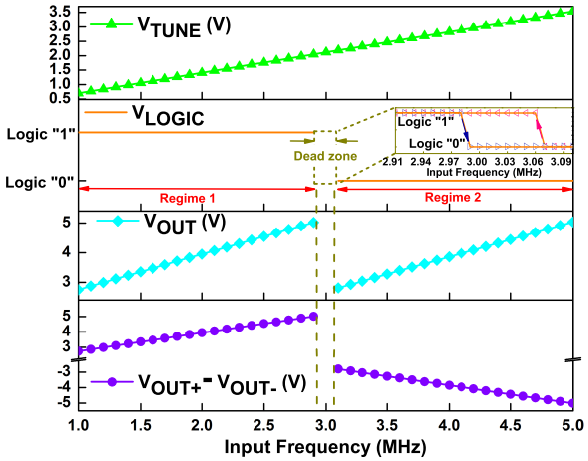


Figure 4.28: Measurement results for V_{TUNE}, V_{LOGIC}, V_{OUT} and the output of the system ($V_{\text{OUT+}}$ and $V_{\text{OUT-}}$) as a function of frequency at the primary control coil.

4.6.3.3 Controllability of the Output Voltage via Input Frequency

Next, we investigate the controllability of the magnitude and the polarity of the output voltage by varying the input frequency at the primary side. Fig. 4.28 shows the measured results for V_{TUNE}, V_{LOGIC}, V_{OUT} and the voltage difference between $V_{\text{OUT+}}$ and $V_{\text{OUT-}}$ (see Fig. 4.21) as a function of the frequency of the signal applied to the primary coil of the control unit. As can be seen, the output of the FVC stage (V_{TUNE}) is linearly dependent on the input frequency. Depending on the value of V_{TUNE}, two states are generated for V_{LOGIC}, which are then used to determine the polarity of the voltage provided by the system. The frequency ranges corresponding to these two logic levels are highlighted as "Regime 1" and " Regime 2" in Fig. 4.28. The frequency range for the "Dead zone" segment is also shown. A similar relation between measured V_{OUT} and the input frequency, across the two regimes outside the "Dead zone", is observed. For example, at the lower boundary of these two regimes (1 MHz and 3.1 MHz), the generated V_{OUT} is approximately the same (2.7 V at 1 MHz and 2.8 V at 3.1 MHz). Finally, the polarity of the output (the difference between $V_{\text{OUT+}}$ and $V_{\text{OUT-}}$) is shown to be controllable based on the state of V_{LOGIC} (and hence the input frequency range). For example, at 1 MHz, a $+2.7$ V is obtained, while at 3.1 MHz, a -2.8 V is obtained, at the output of the system. The measured results presented here demonstrate the capabilities of the proposed system in utilizing the frequency to wirelessly control both the magnitude and the polarity of the output of the

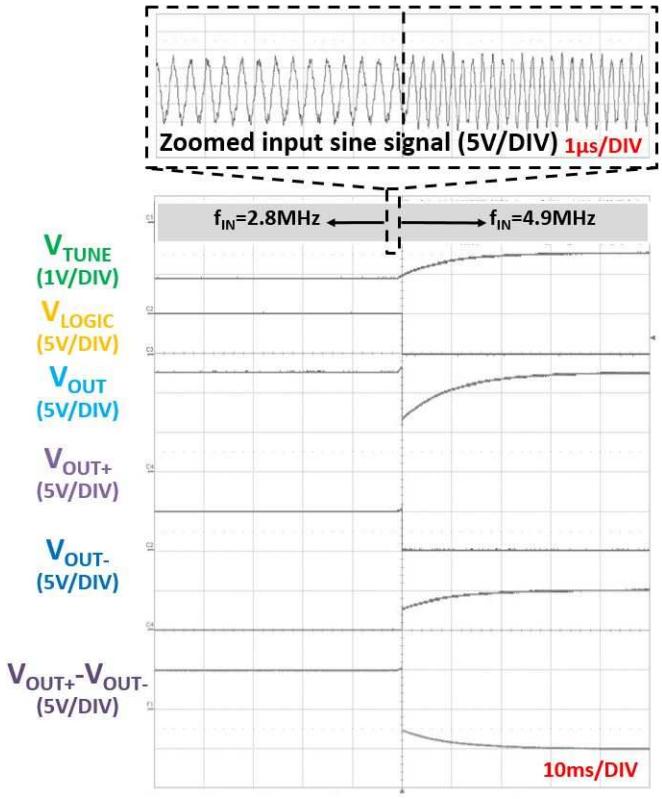


Figure 4.29: Measured transient waveform for the input signal, V_{TUNE}, V_{LOGIC}, V_{OUT}, $V_{\text{OUT}}+$, $V_{\text{OUT}}-$ and their differential signal under an instantaneous frequency change from 2.8 MHz to 4.9 MHz.

system.

4.6.3.4 Performance Evaluation in Response to Abrupt Frequency Changes

The performance of control unit was evaluated, when there is an abrupt change in the frequency of the signal applied to the primary coil. Fig. 4.29 shows the measurement results for a scenario when the input frequency changes abruptly from 2.8 MHz to 4.9 MHz (both corresponding to the same voltage magnitude but with opposite polarity). It can be seen that V_{TUNE} is smoothly adjusting to the new value, and V_{LOGIC} changes its state from high to low when V_{TUNE} triggers the comparator. V_{OUT} remains at the same level within a short transition time. With less than 25 ms, the differential voltage ($V_{\text{OUT+}}$-$V_{\text{OUT-}}$) reaches the destined voltage magnitude and polarity. This response time, which is comparable to the response time of muscles [296], can be further adjusted by the components used in the system (e.g. the settling time of R_{LPF} and C_{LPF} components in Fig. 4.25).

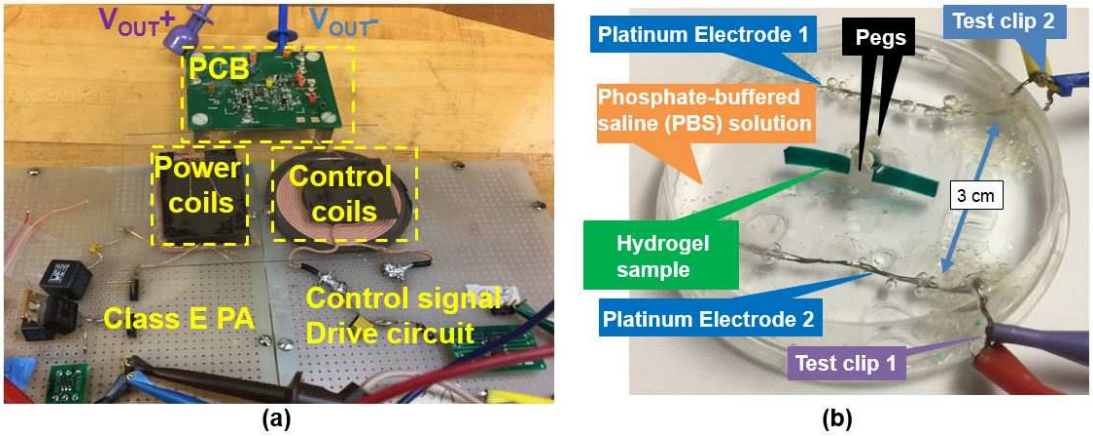


Figure 4.30: Experimental setup used for *in vitro* characterization of iEAPs with the proposed system serving as the electrical stimulator, a) the proposed stimulation system, and b) the iEAP sample test setup.

4.6.4 Experimental Results-*In Vitro* Characterization

The proposed system was used as the electrical stimulator for iEAP samples. The functionality of the end-to-end system is evaluated based on the movement characteristics of iEAP samples while being stimulated by the proposed system. Two testing conditions are considered. First, the movement of iEAPs in terms of the rate of change in the bending angle (angular speed) is characterized when the sample is continuously stimulated at a fixed voltage over a given duration of time [297]. Second, changes in the bending angle of iEAPs when there is an abrupt change in the input frequency are studied. In each test, four samples are used, which is a typical sample size for characterizing iEAPs [298]. In this section, we present and discuss the results of these *in vitro* measurements.

4.6.4.1 Experimental Setup

Fig. 4.30 illustrates the *in vitro* measurement setup. The output of the proposed system was used to provide the electrical stimulation to the iEAP samples via two Pt electrodes. The two ends of the electrodes are attached to the $V_{\text{OUT+}}$ and $V_{\text{OUT-}}$ terminals of the stimulator (see Fig. 4.30-a). The configuration of the iEAP sample in Fig. 4.30-b is the same as Fig. 4.5.

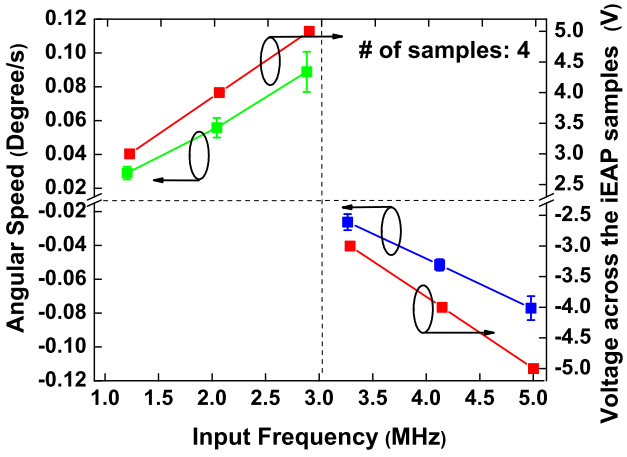


Figure 4.31: Measured results for the average of the angular speed of four samples obtained after 3 minutes of continuous electrical stimulation. The corresponding voltage generated by the system at each frequency is also shown.

4.6.4.2 Movement Characterization: Angular Speed

To evaluate how iEAPs respond to electrical stimulation provided by the proposed system, their movement was characterized by measuring the angular speed at different input frequencies (similar to Section 4.3). The angular speed for a given input frequency is obtained as follows. With the initial state of being no electrical stimulation applied (time = 0), the input frequency is set to a given value and is held for 3 minutes. The movement of the iEAP samples is then videotaped. The angle to which the sample reaches (with respect to its initial state) after 3 minutes of continuous stimulation is measured. The angular speed is then calculated using the value of the angle measured divided by 3 minutes' duration of stimulation. The top view of an iEAP sample being at the initial state, and the bent sample after 3 minutes of continuous electrical stimulation at two voltage conditions have been demonstrated in Fig. 4.6 in Section 4.3.

Measuring angular speed was performed at six different frequencies: 1.2 MHz (corresponding to $+3$ V), 2.0 MHz (corresponding to $+4$ V), 2.8 MHz (corresponding to $+5$ V), 3.2 MHz (corresponding to -3 V), 4.1 MHz (corresponding to -4 V) and 4.9 MHz (corresponding to -5 V). Fig. 4.31 shows the averaged angular speed and 1σ variation across samples, obtained for each frequency. The voltage generated by the system for each input frequency value is

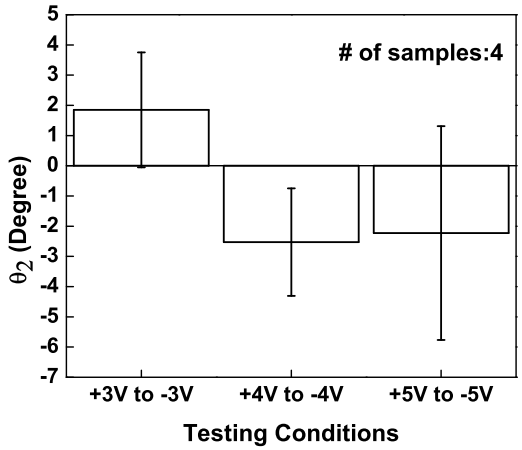


Figure 4.32: Measured results for average θ_2 and 1σ variation across four samples, under three rapid frequency change testing conditions.

also shown (in red). As can be seen, the measured angular speed is proportional to the applied voltage, as expected in Section [30, 297]. It can also be observed that for the positive and the negative polarities of a given voltage value, the angular speed that the iEAP samples achieve are almost the same. Results obtained here are also comparable with what we had previously reported in Section 4.3 where electrical stimulations to iEAP samples were provided by directly changing the voltage levels using an LDO. These results demonstrate the feasibility of using the proposed system as a reliable wireless electrical stimulator for the iEAP samples.

4.6.4.3 Movement Characterization: Response to Rapid Frequency Changes

Next, we studied how the iEAPs respond when there is a sudden change in the frequency at the input of the proposed system. To perform such a study, the input frequency is set at a given value (f_1) for 3 minutes of continuous stimulation. At the end of 3 minutes, the sample reaches the bending angle of θ_1. At the end of the third minute, the input frequency is changed to a new value (f_2) and is held for another 3 minutes. f_2 is chosen such that the generated output voltage is of the same magnitude as the one generated from f_1, but with opposite polarity. The final bending angle at which the sample reaches is then measured (θ_2). Ideally, the angle θ_2 should be close to zero degrees (initial state), since the duration and the magnitude of stimulation at opposite directions are the same.

Three testing conditions for four samples were performed: $f_1 = 1.2$ MHz and $f_2 = 3.2$ MHz (± 3 V condition), $f_1 = 2.4$ MHz and $f_2 = 4.1$ MHz (± 4 V condition), and $f_1 = 2.8$ MHz and $f_2 = 4.9$ MHz (± 5 V condition). Measured results for averaged θ_2 and 1σ variation across four samples are shown in Fig. 4.32. Variations seen in the measured θ_2 across samples as well as testing conditions are possibly due to inconsistencies in iEAP samples. It can however, be observed that overall, the averaged θ_2 is close to zero degrees, indicating that the sudden change in the frequency, and the transition time (e.g. the observed 25 msec in the case of ± 5) that the stimulator system requires to create a voltage of the same magnitude but opposite polarity, is sufficient to cause reasonable reversibility in iEAPs, within a given time window.

4.6.5 Discussion

In this section, a system-level solution for realizing a wirelessly tunable stimulator for providing controllable stimulation to iEAPs was presented. System-level and *in vitro* experimental results demonstrate the feasibility of the proposed system in being used as a reliable stimulator for iEAPs. It was also shown that the inclusion of the square wave generator stage in the FVC unit, makes the proposed control unit reasonably immune to coil misalignment in the inductive link. This is specially important for biomedical implants, as misalignment between the primary and secondary coils could naturally occur due to body movement or changes in the biological environment.

The application does not require a high data rate or a high bandwidth to justify the use of digital modulation schemes, such as ASK and other digital communication methods discussed in Chapter 2. Hence, a direct and fair comparison with commonly designed stimulation systems cannot be made here.

To achieve the ultimate goal of fully implantable iEAP-based muscle prosthesis, other technical challenges must be overcome. Some of these challenges are briefly discussed below.

Movement Characteristics of iEAPs: The movement characterization results presented in Figs. 4.31 and 4.32 demonstrate the feasibility of the proposed module for use as muscle prosthesis. However, variability in the actuation response across samples was observed. To improve the response consistency, approaches such as tuning the ratio of PEG to PAA in the

hydrogels, adjusting the total concentration of the solution in the hydrogels [253], changing the thickness of the hydrogels, and using additional electroactive side chain to alter the chemistry of the hydrogels can be taken. Furthermore, the iEAP samples here required voltages larger than 3 V for being stimulated. Reducing this voltage, decreases the power consumption on the implant side, which is a major requirement in biomedical implants.

Size and Packaging: Another major constraint for biomedical implants is the size. The proposed scheme provides an advantage that it does not use digital modulation schemes to control the stimulation, as the application does not demand high data rates. The use of the proposed scheme reduces the complexity of the design, and consequently, will save on the power consumption and the area on the implant side.

4.7 Summary

In this chapter, the design challenges for the LDO towards the development of iEAP-based muscle prothesis are analyzed. A novel tunable electrical stimulation system for iEAPs is presented based on a frequency-based wireless tuning technique. The system employs a reliable design solution to remotely tune both the degree and the direction of the movement of iEAP samples, without incorporating digital modulation schemes, thereby saving on the size and the design complexity, making it suitable for subcutaneous applications. Extensive board-level and *in vitro* experimental results demonstrated the feasibility of the proposed system in providing reliable electrical stimulation to iEAPs.

Chapter 5

Conclusions and Future work

5.1 Conclusions

This dissertation presented novel solutions for the development of integrated circuits responsible for providing electrical stimulation to iEAPs towards the development of new classes of muscle prosthesis.

The first part of the dissertation presented three novel high-performance reference circuits that advance the state-of-the-art BGRs. The contributions were summarized below:

- a novel BiCMOS-based compensation approach was presented by combining CMOS and BJT thermal properties to directly cancel the nonlinearities
- a higher order temperature compensation technique was introduced based on the difference of Si-Si and SiGe-Si $p-n$ junction voltages
- a piecewise compensation technique was proposed by exploiting the thermal behavior of the V_{GS} and V_{TH} of CMOS transistors

The second part of the dissertation focused on the system level development for implantable stimulators. The contributions were summarized below:

- an external capacitor-less LDO was proposed to meet the design challenges in serving as the iEAP stimulator
- a novel frequency-based tuning technique suitable for iEAP application was proposed as the first work in using frequency information for wireless tuning
- system level implementation of the wirelessly tunable voltage regulator was presented

- the functionality of the end-to-end system is evaluated based on the in vitro characterization of the iEAPs

5.2 Future work

Future work of this research includes the circuit and system level investigation of the stimulator, along with the improvement of the biocompatible iEAPs and the *in vivo* tests.

Future work in the stimulator's circuit and system level is summarized below:

- the IC implementation of the proposed frequency-based tuning circuits
- evaluate the total power consumption, the overall size and the current handing capability of the stimulator
- the closed loop implementation of the proposed frequency-based tuning technique to maintain a good PTE under various scenarios and monitor the voltage applied to the iEAP sample on a real-time basis
- search for novel solutions to use one link to transmit both power and control command

Future work for the biocompatible iEAPs and the *in vivo* tests is summarized below:

- other stimulation patterns (such as the monophasic and biphasic pulses) need to be evaluated in the *in vitro* tests and compared to the proposed method using DC voltage in this dissertation
- optimization of the actuation response of the iEAPs (such as tuning the ratio of PEG to PAA in the hydrogels)
- investigate technical issues related to the integration of the stimulator with iEAPs and the packaging issues of the entire muscle prosthesis into the body of human

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